PM5320

ARROW 155

ASSP Telecom Standard Product Data Sheet

Released

Issue No. 3: December 2005

Issue No.	Issue Date	Details of Change
3	December 2005	Updated ordering information including RoHS-compliant device details.
2	July 2004	Section 6 Pin numbers added to connector description. Section 7 Description of overhead byte access corrected for both transmit and receive STS-1E section and line blocks. Section and line DCC are not accessible from the PDH overhead ports. JTAG description removed and reference to JTAG App Note included instead. Section 9 Power numbers added from Characterization Report. Section 13.8 Jitter numbers added. MTIE graphs included.
1	May 2003	Document created

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1 References

1.1 Thermal

1. Electronic Industries Association. *Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device): EIA/JESD51*. December 1995.

2. Electronic Industries Alliance 1999. *Integrated Circuit Thermal Test Method Environmental Conditions -Junction-to-Board: JESD51-8*. October 1999.

3. Telcordia Technologies. *Network Equipment-Building System (NEBS) Requirements: Physical Protection: Telcordia Technologies Generic Requirements GR-63-CORE*. Issue 1. October 1995.

4. SEMI (Semiconductor Equipment and Materials International). *SEMI G30-88 Test Method for Junction-to-Case Thermal Resistance Measurements of Ceramic Packages*. 1988.

1.2 Protocol

1. ANSI, *Digital Hierarchy - Synchronous DS3 Format Specifications*, T1.103-1993.

2. ANSI, *Synchronous Optical Network (SONET) – Basic Description including Multiplex Structure, Rates, and Formats*, T1.105-1995.

3. ANSI, *Synchronous Optical Network (SONET) – Payload Mappings*, T1.105.02, October 27, 1995.

4. ANSI, *Digital Hierarchy - Formats Specifications*, T1.107-1995.

5. ANSI, *Digital Hierarchy - Supplement to Formats Specifications (DS3 Format Applications)*, T1.107a-1990.

6. ANSI, *Digital Hierarchy - Layer 1 In-Service Digital Transmission Performance Monitoring*, T1.231-1997.

7. ANSI, *Customer Installation–to-Network - DS3 Metallic Interface Specification*, T1.404-1994.

8. AT&T, *Requirements For Interfacing Digital Terminal Equipment To Services Employing The Extended Superframe Format*, TR 54016, September 1989.

9. AT&T, *Accunet T1.5 - Service Description and Interface Specification*, TR 62411, December 1990.

10. Bell Communications Research, *Asynchronous Digital Multiplexes Requirements and Objectives*, TR-TSY-000009, Issue 1, May 1986.

11. Bell Communications Research, *Alarm Indication Signal Requirements and Objectives*, TA-TSY-000191, Issue 1, May 1986.

12. Bell Communications Research, *Wideband and Broadband Digital Cross-Connect Systems Generic Criteria*, TR-NWT-000233, Issue 3, November 1993.

13. Bell Communications Research, *Digital Interface Between The SLC®96 Digital Loop Carrier System And A Local Digital Switch*, TR-TSY-000008, Issue 2, August 1987.

14. Bell Communications Research, *Integrated Digital Loop Carrier Generic Requirements, Objectives, and Interface*, TR-TSY-000303, Issue 2, December 1992.

15. Bell Communications Research, *Transport Systems Generic Requirements (TSGR): Common Requirement*, TR-TSY-000499, Issue 5, December 1993.

16. Bell Communications Research - OTGR: Network Maintenance Transport Surveillance - Generic Digital Transmission Surveillance, TR-TSY-000820, Section 5.1, Issue 1, June 1990

17. ETSI, *Generic Functional Requirements for Synchronous Digital Hierarchy (SDH) Equipment*, ETS 300 417-1-1, January 1996.

18. ETSI, *ISDN Primary Rate User-Network Interface Specification and Test Principles*, ETS 300 011, 1992.

19. IEEE. 1149.1b-1994 IEEE Standard Test Access Port and Boundary-Scan Architecture. Sept 22, 1994

20. ITU-T, *Physical/Electrical Characteristics of Hierarchical Digital Interfaces*, Recommendation G.703, 1991.

21. ITU-T, *Synchronous Frame Structures Used at Primary Hierarchical Levels*, Recommendation G.704, July 1995.

22. ITU-T, *Frame Alignment and CRC Procedures Relating to G.704 Frame Structures*, Recommendation G.706, 1991.

23. ITU-T, *Network Node Interface For The Synchronous Digital Hierarchy*, Recommendation G.707, 1996.

24. ITU-T, *Second Order Digital Multiplex Equipment Operating at 6312 kbit/s and Multiplexing Three Tributaries at 2048 kbit/s*, Recommendation G.747, 1988.

25. ITU-T, *Loss of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria*, Recommendation G.775, November 1994.

26. ITU-T, *Structure of Recommendations on Equipment for the Synchronous Design Hierarchy (SDH)*, Recommendation G781, January 1994.

27. ITU-T, *Characteristics of Synchronous Digital Hierarchy (SDH) Equipment Functional Blocks*, Recommendation G.783, October 2000.

28. ITU-T, *Characteristics of Synchronous Digital Hierarchy (SDH) Equipment Functional Blocks*, Recommendation G.783 Amendment 1, June 2002.

29. ITU-T, *The Control of Jitter and Wander within Digital Networks which are Based on the 2048 kbit/s Hierarchy*, Recommendation G.823, March 1994.

30. ITU-T, *Error Performance Measuring Equipment Operating at the Primary Rate and Above*, Recommendation O.151, October 1992.

31. ITU-T, *ISDN User-Network Interface Data Link Layer Specification*, Recommendation Q.921, March 1993.

32. International Organization for Standardization, *High-Level Data Link Control procedures - Frame Structure*, ISO 3309:1984.

33. Telcordia Technologies, *Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria*, GR-253-CORE, Issue 3, September 2000.

34. Telcordia Technologies, *SONET Add-Drop Multiplexer (SONET ADM) Generic Criteria*, GR-496-CORE, Issue 1, December 1998.

35. Telcordia Technologies. *Network Equipment-Building System (NEBS) Requirements: Physical Protection:* GR-63-CORE, Issue 1. October 1995.

36. TTC, *Frame Structures on Primary and Secondary Hierarchical Digital Interfaces*, Standard JT-G704, 1995.

37. TTC, *Frame Synchronization and CRC Procedure*, Standard JT-G706.

38. Nippon Telegraph and Telephone Corporation, *Technical Reference for High-Speed Digital Leased Circuit Services*, Third Edition, 1990.

1.3 Miscellaneous

1. PMC-Sierra, Inc., *Enhanced-LVDS (ELVDS) Electrical Specification*, PMC-2001507, Issue 1, 2002.

2. PMC-Sierra, Inc., *Extended SONET/SDH Serial Interface (ESSI) Specification*, PMC-2010653, Issue 1, 2001.

3. PMC-Sierra, Inc., *ARROW 155 Ball Map File, PMC-2031854*

4. PMC-Sierra, Inc., *ARROW 155 ASSP Telecom Standard Product Data Sheet Register Description,* PMC-2031892, Issue 1, 2004

5. PMC-Sierra, Inc., *ARROW 155 Short Form Data Sheet, PMC-2030735*

6. PMC-Sierra, Inc., *PM5319/PM5320 ARROW 622/155 Hardware Design Guide*, PMC-2030859, Issue 2, 2004

7. PMC-Sierra, Inc., *PM5319/PM5320 ARROW 622/155 Operation and Configuration Guide,* PMC-2030860, Issue 2, 2004

2 Patents

The technology discussed in this document is protected by the following patents:

- Canada 2,159,763
- Canada 2,161,921
- Canada 2,245,760
- USA 6,052,073
- USA 5,606,563
- USA 5,640,398
- USA 6,703,950
- USA 6,744,787

3 Definitions

Table 1 Definitions

Term	Definition
AIS	Alarm Indication Signal
BER	Bit Error Rate
BIP	Byte Interleaved Parity
COFA	Change of Frame Alignment
CRC	Cyclic Redundancy Check
CSU	Clock Synthesis Unit
D3E3MA	DS3 / E3 TO STS-1/STM-0 Mapper / Synchronizer
D3E3MD	STS-1/STM-0 TO E3 / DS3 Demapper / Desynchronizer
DCC	Data Communication Channel
DLL	Digital Delay Locked Loop
DS3	Digital Signal Level 3
E3 FRMR	ITU-T G.832 E3, G.751 E3 Framer
E3 TRAN	CCITT G.832 E3, G.751 E3 Transmitter
ERDI	Enhanced Remote Defect Indication
ESD	Electrostatic Discharge
EXZS	Excess Zeros
FAS	Framing Alignment Signal
F-bit	Framing Bit
FCS	Frame Check Sequence
FEAC	Far End Alarm Control
FEBE	Far End Block Error
FERF	Far End Receive Failure
FERR	Framing Bit Error
FIFO	First-In First-Out
HDLC	High-level Data Link Layer
ITU	International Telecommunications Union
JAT	Digital Jitter Attenuator
JTAG	Joint Test Action Group
LAIS	Line AIS also referred to as AIS-L
LCV	Line Code Violation
LOF	Loss of Frame
LOH	Line Overhead
LOP	Loss of Pointer
LOS	Loss of Signal
LOT	Loss of Transition
LRDI	Line RDI also referred to as RDI-L

Term	Definition
NC	No Connect, indicates an unused pin
NDF	New Data Flag
NRZ	Non Return to Zero
ODL	Optical Data Link
OOF	Out of Frame
PERR	Parity Error
PHY	Physical Layer
PLL	Phase-Locked Loop
PMDL	Path Maintenance Data Link
PMON	E3/T3 Performance Monitor
PRGD	Pseudo Random Sequence Generator/ Detector
PRGM	Pseudo Random Sequence Generator/Monitor
PSL	Path Signal Label
PSLM	Path Signal Label Mismatch
RAI	Receive Alarm Indication
RBOC	Bit Oriented Code Detector
RDI	Remote Defect Indication
RDLC	Data Link Receiver
RED	Receive Error Detection
RHPP	Receive High Order Path Processor
RRMP	Receive Regenerator and Multiplexer Section Processor
RTTP	Receive Trail Trace Processor
SARC	SONET/SDH Alarm Reporting Controller
SBER	SONET/SDH Bit Error Monitoring
SD	Signal Degrade (alarm)
SDH	Synchronous Digital Hierarchy
SF	Signal Fail
SMDS	Switched Multi-Megabit Data Service
SOH	Section Overhead
SONET	Synchronous Optical Network
SPE	Synchronous Payload Envelope
SPTB	SONET/SDH Path Trace Buffer
STSI	SONET/SDH Timeslot Interchange
SVCA	SONET/SDH Virtual Container Aligner
T3 FRMR	T3 (DS3) Framer
T3 TRAN	T3 (DS3) Transmitter
TAP	Test Access Port
TDPR	Transmit Data Link Controller with Performance Report Interface
THPP	Transmit High Order Path Processor
TIM	Trace Identifier Mismatch

Term	Definition
TIU	Trace Identifier Unstable
TOH	Transport Overhead
TRMP	Transmit Regenerator and Multiplexer Processor
TTTP	Transmit Trail Trace Processor
UI	Unit Interval
WAN	Wide Area Network
XBOC	Bit-Oriented Code Transmitter
XOR	Exclusive OR logic operator

4 Applications

This section describes some of the possible ways that the device can be used in a system application.

Figure 1 shows the ARROW 155 and the ARROW 622 on a 4x OC-3/STM-1 line card. The 4 ARROW 155 devices interface with the SONET/SDH streams, while the ARROW 622 aggregates these streams into a 622Mbps backplane.

Figure 1 Four port OC-3 to OC-12 Aggregator

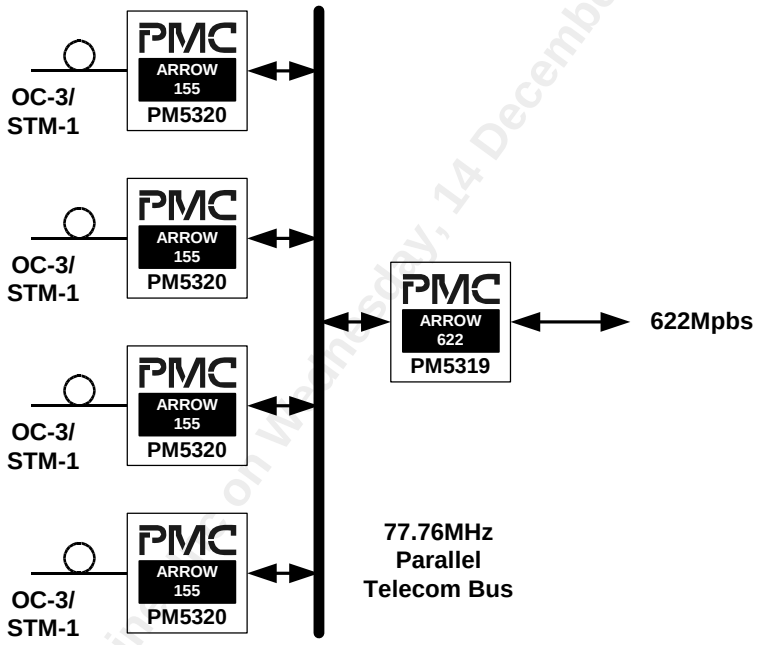


Figure 2 shows an OC-12/STM-4 terminal multiplexer example. The ARROW 622 devices provide the working and protect link to the network. The ARROW 155 can be used to manipulate an OC-3/STM-1 stream or to map/demap up to 3 PDH (DS3/E3/STS-1E) streams. The TEMAP 84 is used to map/demap DS1/E1 streams. The SBS-ARROW 8xFE combination maps Ethernet channels into SONET/SDH payload.

Figure 2 OC-12/STM-4 Terminal Mux

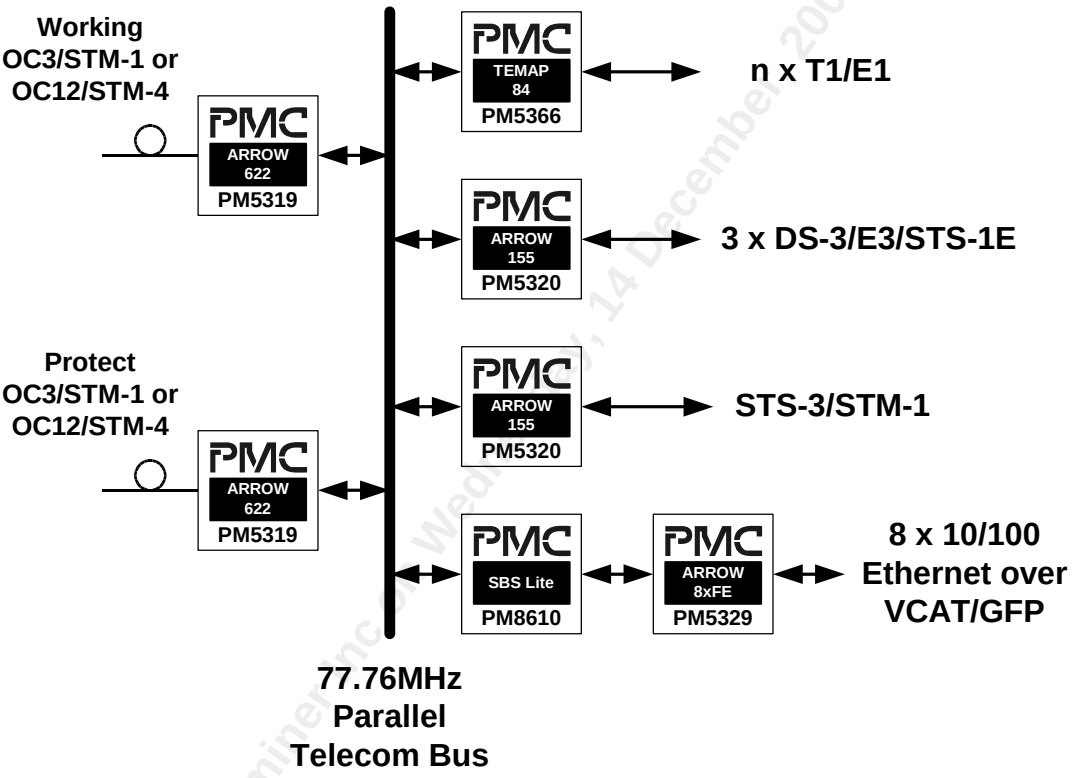


Figure 3 and Figure 4 are both examples of OC-3/STM-1 terminal mutiplexers. They illustrate the different PMC-Sierra device combination that allow the insertion/extraction of PDH streams from SONET/SDH.

Figure 3 OC-3/STM-1 Terminal Mux Example #1

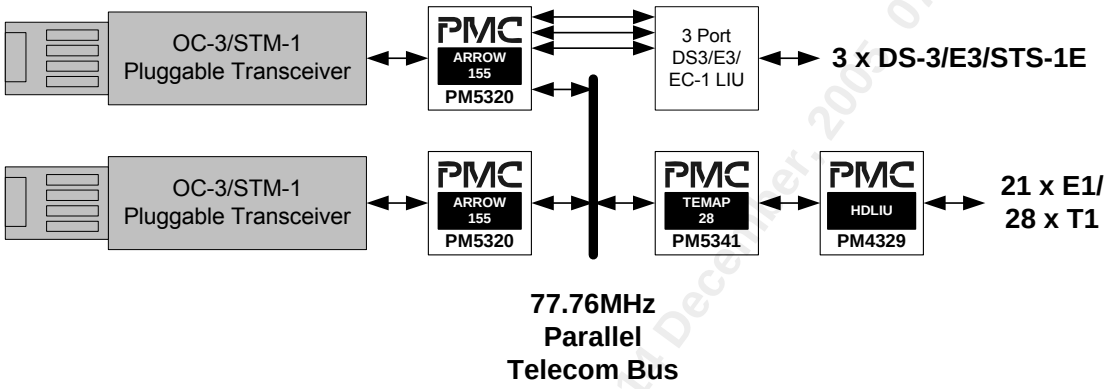


Figure 4 OC-3/STM-1 Terminal Mux Example #2

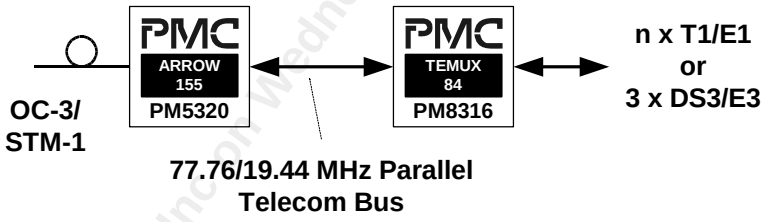


Figure 5 shows the ARROW 622 as part of a small ADM architecture. The ARROW 622 interfaces to the SONET/SDH network, while the ARROW 155 provides access to the PDH streams mapped into SONET/SDH. Figure 6 illustrates a similar application with added equipment protection.

Figure 5 CPE ADM – No Equipment Protection

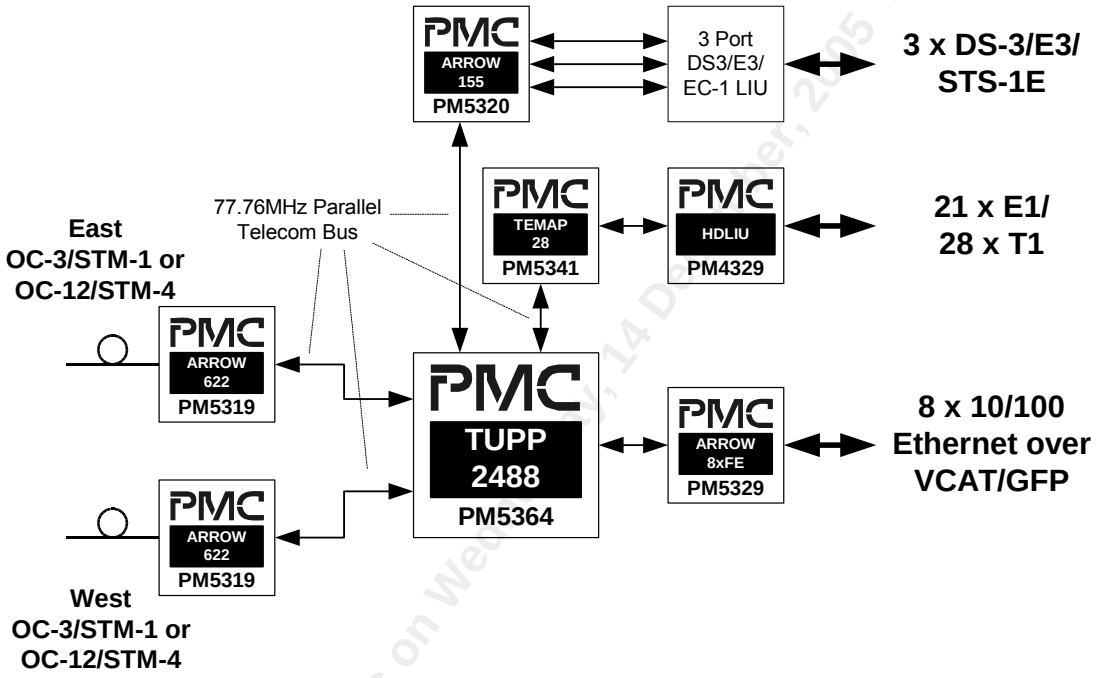
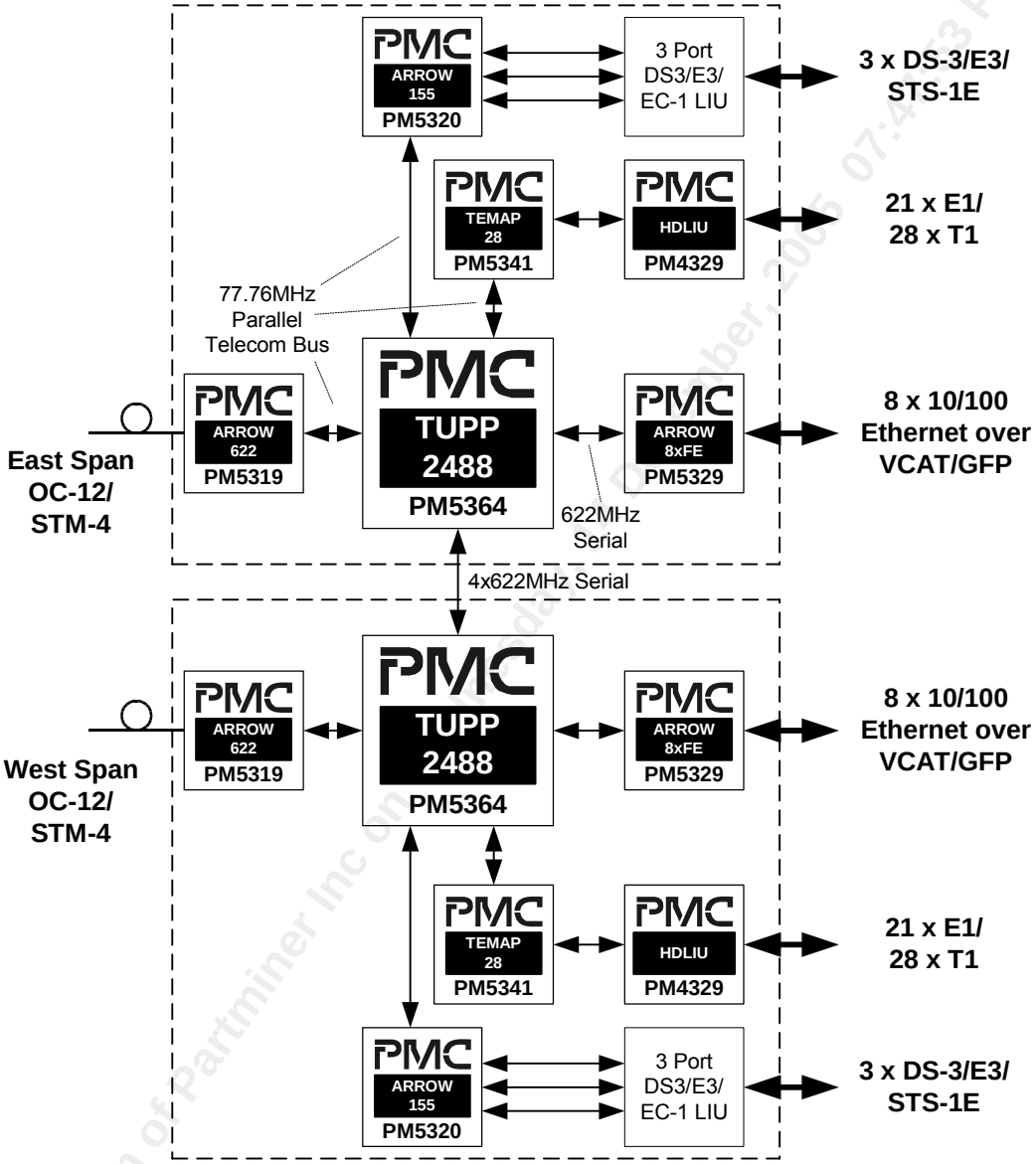


Figure 6 CPE ADM – Fully Redundant

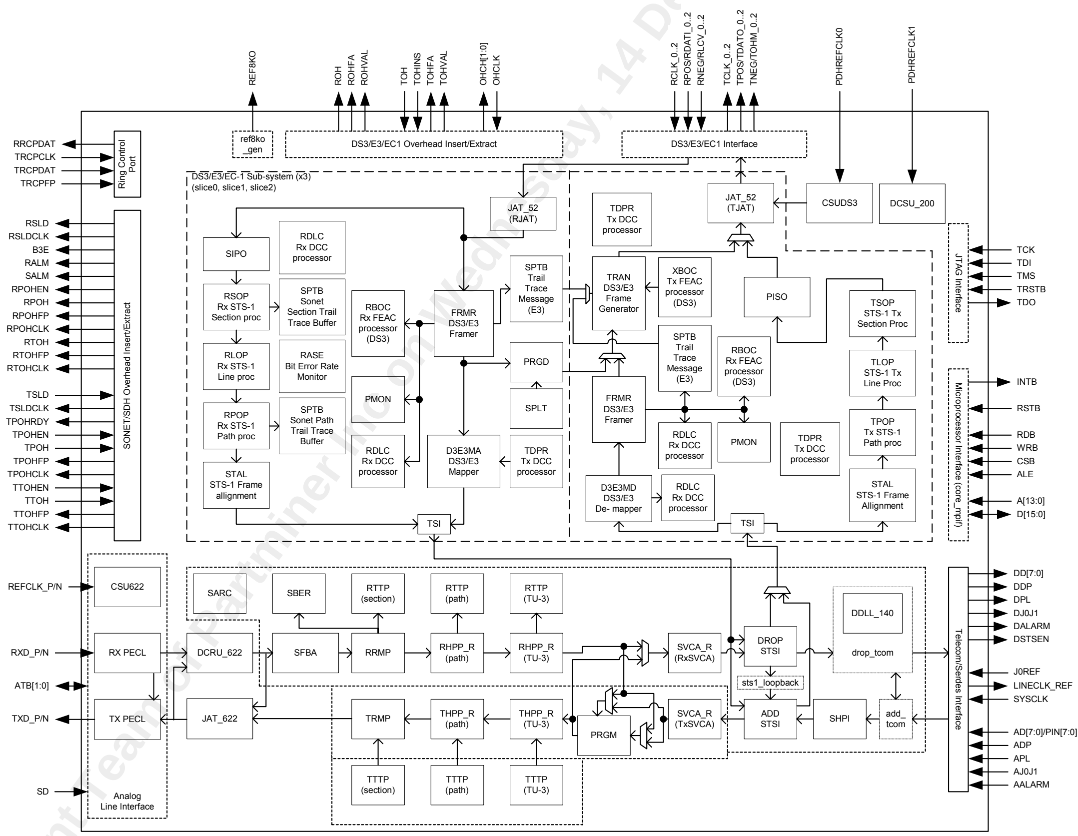


5 Overview

The ARROW 155 device is a single port OC-3 (STM-1) Framer. The ARROW 155 terminates Section, Line, and Path overhead at both the STS-n (AU-4) level and the TU-3 level. On the line side, it incorporates a multi-rate SERDES, allowing it to mate directly to an optics module or connect across a backplane. The system side interface is an 8-bit multi-drop Parallel TelecomBus, allowing multiple devices to share a single bus. The ARROW 155 maps/de-maps up to three channels of DS3/E3 or STS-1E with bi-directional traffic monitoring. The traffic may be multiplexed either into the line or system side interfaces or any combination thereof.

5.1 Block Diagram

Figure 7 Block Diagram



5.2 Interfaces

The ARROW 155 has eight distinct interfaces: Serial Line Side, SONET/SDH Overhead, Ring Control Port, DS3/E3/STS-1E Overhead, DS3/E3/STS-1E Serial, Microprocessor Interface, Parallel TelecomBus, and JTAG.

5.2.1 Serial Line Side

The serial line side consists of an AC-coupled PECL transmit pair (TXD_P, TXD_N), a PECL receive pair (RXD_P, RXD_N), and a PECL reference clock input (REFCLK_P, REFCLK_N). The transmit and receive pair operate at 155 Mbit/s. The reference clock input operates at 77.76 MHz or 155.52 MHz.

5.2.2 SONET/SDH Overhead

The ARROW 155 provides full access to all overhead bytes on the STS-3 (STM-1) SONET/SDH datapath. The SONET/SDH overhead port is implemented as four separate interfaces. The receive transport overhead bytes are available on RTOH, RTOHCLK, and RTOHFP signals from the Transport Overhead Processor (RRMP). This interface runs at a nominal 5.184 MHz. The section and line DCC bytes also appear on dedicated pins RSLD and RSLDCLK. The receive path overhead bytes are available on RPOH, RPOHEN, RPOHFP, and RPOHCLK signals from the RHPP blocks. B3E, along with a variety of other alarm signals, are available on RALM and SALM signals from the SARC. This interface runs at a nominal 20.736 MHz.

The transmit transport overhead is inserted using TTOH, TTOHEN, TTOHFP, and TTOHCLK. This interface runs at a nominal 5.184 MHz. Section and Line DCC bytes may be inserted using the dedicated pins TSLD and TSLDCLK. The transmit path overhead interface consists of the TPOH, TPOHRDY, TPOHEN, TPOHFP, and TPOHCLK signals to/from the THPP blocks. This interface runs at a nominal 20.736 MHz.

5.2.3 Ring Control Port

The ring control port allows a mate ARROW 155, or FPGA to perform real time insertion and extraction of alarms and status. The Ring Control Port consists of the RRCPDAT, TRCPDAT, TRCPCLK, and TRCPFP signals that connect to the SARC block. RPOHCLK and RPOHFP are used to indicate timing and frame alignment for the RRCPDAT signal. The functional timing section (Sections 8.13 and 8.14) provides further detail on this interface.

5.2.4 DS3/E3/STS-1E Overhead

The ARROW 155 provides access to the overhead of up to three DS3, E3, or STS-1E signals. The DS3/E3/STS-1E overhead port consists of the ROH, ROHFA, ROHVAL, TOH, TOHINS, TOHFA, TOHVAL, OHCH[1:0], and OHCLK pins. The DS3/E3/STS-1E overhead port is clocked by the OHCLK pin, and provides each channel's overhead in a timeslot multiplexed bit serial stream. The channel on the bus at each time is indicated by the OHCH[1:0] pins. Cycles where OHCH[1:0] = '11', are invalid and should be ignored.

5.2.5 DS3/E3/STS-1E Serial

The DS3/E3/STS-1E Serial interface is jitter attenuated in both the transmit and receive directions. Depending on the mode of operation, the transmit interface consists of either TCLK, TPOS, and TNEG for each channel or TCLK, TDATO, and TOHM for each channel (total of 9 pins). Depending on the mode of operation, the receive interface consists of either RCLK, RPOS, and RNEG for each channel or RCLK, RDATI, and RLCV for each channel (total of 9 pins). These signals may connect directly to an LIU without additional jitter attenuation. The DS3/E3 desynchronizer exceeds all jitter and wander specifications, and requires only a DS3 or E3 line rate clock. The PDHREFCLK[1:0] inputs are provided for this purpose.

5.2.6 Parallel TelecomBus

The Parallel TelecomBus (P-TCB) interface implements the main system side interface and is clocked relative to a single input clock (SYSCLK). On the Add side (chip data in), it consists of an 8-bit databus (AD[7:0]), a data parity signal (ADP), a payload marker (APL), a frame marker signal (AJ0J1), and an alarm forcing signal (AALARM).

On the Drop side (chip data out), it consists of an 8-bit databus (DD[7:0]), a data parity signal (DDP), a payload marker (DPL), a frame marker (DJ0J1), an alarm signal (DALARM), a frame pulse reference input (J0REF), and a timeslot tristate enable (DSTSEN).

An output clock reference signal (LINECLK_REF) provides a 77.76 MHz clock that is locked to either the recovered line side clock, or the generated line side clock. The system designer may chose to use LINECLK_REF as the source for SYSCLK to eliminate pointer movements in either the Add or Drop direction.

Where H1& H2 are valid, the SHPI block may be used rather than explicit framing, payload, and alarm signals. If the SHPI is enabled, the ADP, APL, and AALARM inputs may be grounded. If the J1SQUELCH bit is set, the AJ0J1 signal (which normally pulses high to mark the J0 and J1 bytes) is re-defined as to only carry a single frame pulse per frame. The location of that frame pulse in the frame is user programmable in the FPINDLY[13:0] bits. The ADP input may be ignored if the APE bit is not set. Note that the SHPI is enabled by default. To disable it, set the PT_PATH[x] bits in register 0x1A06.

If the J1SQUELCH bit is set, the DJ0J1 signal is modified similar to the AJ0J1 signal to create a user selectable frame pulse, which is programmed with the FPOUTDLAY[13:0] bits.

Note that although the ARROW 155 operates at 155.52 Mbit/s, the TelecomBus interface operates at 77.76 MHz. This is to provide hardware compatibility with the PM5319 ARROW 622 device and to allow multiple ARROW 155 devices to timeslot-multiplex their traffic into a 622.08 Mbit/s fabric switch or DS0 termination device. While the TelecomBus always operates at 77.76 MHz, it is compatible with 19.44 MHz systems.

5.2.7 Microprocessor

The generic microprocessor interface provides configuration and control of the ARROW 155. It consists of a 16-bit bidirectional data bus (D[15:0]), an address bus (A[13:0]), an address latch enable (ALE) for supporting multiplexed address and data bus applications, and active low read strobe (RDB), write strobe (WRB), and chip select (CSB). The device is reset by the active low RSTB pin. Alarms and events in the device can interrupt the controller via the active low open drain (INTB) interrupt pin.

5.2.8 JTAG

The standard JTAG interface consists of the TCK, TDI, TMS, TRSTB, and TDO signals.

5.3 Modes of Operation

The ARROW 155 device has several modes of operation that can be software configured. Descriptions of the main modes follow.

5.3.1 OC-3 Mode

In this mode, all rate programmable blocks (RRMP, TRMP, JAT_622, DCRU and STS3 <-> STS12 converters) are configured for STS-3 operation, and these blocks run at the reduced clock frequency of 19.44 MHz. DS3/E3/STS-1E channels are switched into the datapath by programming the appropriate timeslots of the respective SONET/SDH Timeslot Interchange (STSI) but the valid timeslots of the STSI toward the SONET/SDH line side are restricted to only one STS-3 worth of timeslots. (The DROP STSI incoming timeslots 2 to 4 are duplicates of 1, 6 to 8 are duplicates of 5 and 10 to 12 are duplicates of 9 on the STSI inputs DIN1,2 and 4 for UNEQ-P. The ADD STSI outgoing timeslots 2 to 4, 6 to 8 and 10 to 12 on output ports 1 & 4 are discarded. All DROP STSI outgoing and all ADD STSI incoming timeslots are valid.)

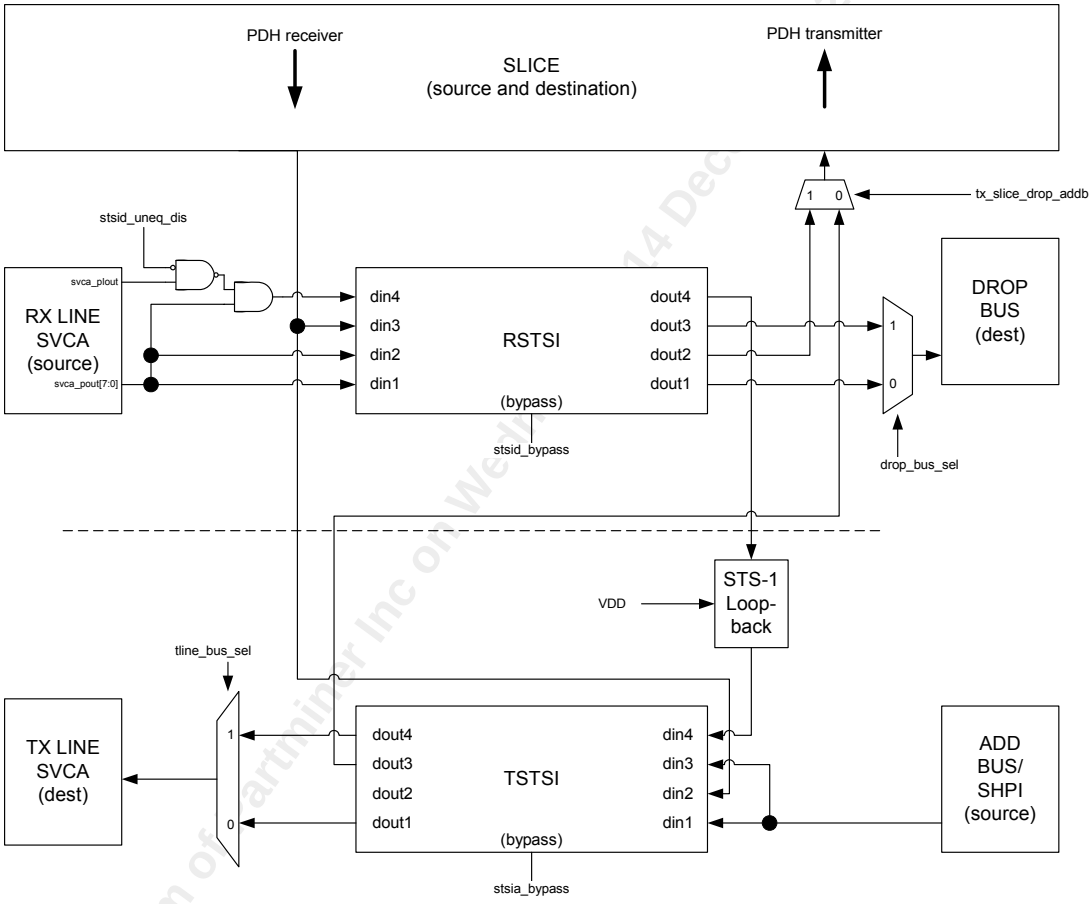
5.3.2 DS3/E3/STS-1E Mapper Mode

The SONET/SDH interface in the ARROW 155 may be turned off, allowing the device to operate strictly as a mapper for DS3, E3, and STS-1E signals. The DS3/E3/STS-1E channels must talk through the P-TCB interface. A dedicated Bypass mode is provided in the STSI's to support this mode with minimal configuration. For normal operation, the user need not provide clock to the line side in this mode. However, to use the PRBS block, a line side clock and use of the STSI block are required.

5.4 Datapath

Section 5.1 has already given a brief overview of the main SONET/SDH framer datapath. There are, however, a number of possibilities in the configuration of the STSI blocks, which can best be understood by Figure 8. The receive DIN timeslots 1, 5, and 9 contain valid data, and the other input timeslots are invalid. Similarly, transmit DOUT timeslots 1, 5, and 9 must contain the valid timeslots, and the other timeslots will be discarded.

Figure 8 STSI Datapaths



5.4.1 SONET/SDH Only Mode

If only the SONET/SDH framer is required, and no traffic from the DS3/E3/STS-1E subsystem will appear on the TelecomBus or on the serial line interface, then the user only needs to configure the DIN1 and DOUT1 ports of the Transmit and Receive STSI. If no timeslot interchange is required, this can easily be accomplished by writing a '1' to the STSID_BYPASS and STSIA_BYPASS bits. If timeslot interchange is required, the user will have to configure the DOUT1 port of both STSIs.

5.4.2 Receive STSI Datapath Configurations

The DOUT2 port of the Receive STSI can be used as the source for Transmit PDH (DS3/E3/STS-1E) traffic if RXD_P/N is the exclusive source of Transmit PDH traffic. This datapath input is selected by writing '1' to TX_SLICE_DROP_ADDB. When STSID_BYPASS is '1', all timeslots that appear on the TelecomBus are copied to the Transmit slice. The TSI of each slice can then select the appropriate timeslot for that PDH slice. When the Receive STSI is not in bypass, the DOUT2 port will have to be configured to output the required timeslots.

The DOUT3 port of the Receive STSI is provided for the DS3/E3/STS-1E mapping mode, where the Receive PDH slice is the exclusive source of Drop TelecomBus traffic. This mode is selected by writing '1' to the DROP_BUS_SEL bit.

The DOUT4 port of the Receive STSI provides a per-timeslot loopback capability, and is also used to enable the most general datapath configuration. If the datapath configuration requires that the transmit PDH traffic can come from either the PECL interface or from the TelecomBus, or if the receive PDH traffic can go out either the TelecomBus or the PECL interface, then DOUT4 must be configured to select those timeslots from the Receive SONET/SDH line that are destined for the Transmit PDH, and those timeslots from the Receive PDH that are destined for the Transmit SONET line. If a per-timeslot line loopback is required DOUT4 must be configured to select the timeslots that need to loop-back.

The DIN4 port of the Receive STSI serves a special function to support UNEQ-P insertion on the Drop bus. When the STSID_UNEQ_DIS bit is '0', DIN4 contains a copy of the timeslots on DIN1, but with the SPE forced to all 00. If a path is unused in the Drop TelecomBus, then a similar timeslot or timeslots from DIN4 should be switched onto the DOUT1/DOUT3 output as an UNEQ-P path.

5.4.3 Transmit STSI Datapath Configurations

The DIN2 port of the Transmit STSI is sourced from the Receive PDH slice. This data path source is best when the receive PDH traffic is destined exclusively for the PECL interface. Note that there is no bypass output on DOUT2, so any PDH timeslots will have to be explicitly mapped to either DOUT1 or DOUT4.

The DOUT3 port of the Transmit STSI feeds the Transmit PDH slice when the TX_SLICE_DROP_ADDB bit is '0'. This datapath setting supports the general case of PDH transmit traffic sourced from both the PECL and the Add bus, as well as the 3xETEC datapath of sourcing the Transmit PDH traffic exclusively from the Add bus. This port does support an automatic bypass, but the bypass is not recommended if Transmit SONET or PDH data is also coming from the STS-1 Loop-back. Note that if PDH transmit traffic is sourced from both the STS-1 Loopback and the Add bus, the J0 alignment of the Add bus and the Drop bus must be such that the STSLB_J0I interrupt does not assert.

The DIN4 port completes the STS-1 loop-back described above. These timeslots will have to be mapped into the DOUT1 or DOUT3 ports for their respective destinations. The DOUT4 port provides a bypass path for a full datpath line loopback at the STSIs.

5.4.4 Loopbacks

The loopbacks in this device are described in the *PMC-2030860 PM5319/PM5320 ARROW 622/155 Operation and Configuration Guide*.

6 Pin Description

The following sections describe each ball. Unless stated, all control signals are active high logic. Ball assignments may be found in the ARROW 155 Ball Map File, PMC-2031854. This file is provided in .xls format to simplify schematic symbol generation.

Table 2 Pin Type Definition

Type	Definition
Input	Input
Output	Pin is always driven
Tri-State	Pin is either driven, or held in Hi-Z
BiDi	Bidirectional
OD	Open drain. Either driven low or held in Hi-Z.

6.1 Parallel TelecomBus Transmit Interface

All pins are 3.3 V LVTTL compatible logic levels.

Pin Name	Reset State	Type	Pin No.	Function
SYSCLK	Hi-Z	Input	N2	**Parallel TelecomBus Add Clock** SYSCLK is a 77.76 MHz clock. AD[7:0], ADP, APL, AJ0J1, AALARM, and J0REF are sampled on the rising edge of SYSCLK. DD[7:0], DDP, DPL, DJ0J1, DALARM, and DSTSEN are updated on the rising edge of SYSCLK. SYSCLK should be free of glitches when RSTB is high.
AD[7] AD[6] AD[5] AD[4] AD[3] AD[2] AD[1] AD[0]	Hi-Z	Input	L2 L4 K1 K3 K4 J1 J2 J3	**Parallel TelecomBus Add Bus** The AD[7:0] input bus sources the transmit SONET/SDH frames. AD[7:0] is sampled on the rising edge of SYSCLK.
ADP	Hi-Z	Input	M3	**Parallel TelecomBus Add Data Parity** ADP reports the parity of the corresponding Add data bus (AD[7:0]). ADP reports even parity by default, however it may be configured for odd parity and to report parity over Add data bus and the control signals (APL and AJ0J1) via microprocessor control. If a parity signal is not available, ADP may be tied low if the APE bit in register 0x1809 is set low. ADP is sampled on the rising edge of SYSCLK.

Pin Name	Reset State	Type	Pin No.	Function
APL	Hi-Z	Input	L1	**Parallel TelecomBus Add Payload marker** APL distinguishes between transport overhead bytes and synchronous payload/high order virtual container bytes in the corresponding Add data bus (AD[7:0]). APL is set high to mark each payload / HO-VC byte on AD[7:0] and set low to mark each transport overhead byte on AD[7:0]. APL may be tied low if the SHPI is enabled for all timeslots. APL must be tied low if the frame pulse is moved to any position other than J0. APL is sampled on the rising edge of SYSCLK.
AJ0J1	Hi-Z	Input	M2	**Parallel TelecomBus Add J0/J1 marker** AJ0J1 pulses high when AD[7:0] carries the J0 and all J1 bytes. It is low otherwise. J0 position must be indicated, but J1 bytes may be internally decoded provided that valid H1/H2 pointers are present. By default the J0 frame pulse is indicated, but the ARROW 155 may be configured to accept a frame pulse on any byte of the SONET/SDH frame. If the frame pulse is moved from the J0 position, the APL input must also be tied low. AJ0J1 is sampled on the rising edge of SYSCLK.
AALARM	Hi-Z	Input	M1	**Parallel TelecomBus Add Alarm marker** AALARM identifies STS/STM streams on the corresponding Add data bus (AD[7:0]) that are in alarm state. Definition of the alarm condition depends on the amount of SONET/SDH processing performed by the ARROW 155. AALARM is set high when the stream on AD[7:0] is in alarm state (for instance, PAIS) and is set low when the stream is out of alarm state. AALARM may be tied low if the SHPI is enabled for all timeslots. Note that AALARM high will result in transmit path AIS regardless of SHPI settings, as AALARM is internally ORed with the SHPI output. In a concatenated data configuration (STS-3c) only the first STS-1 is defined. AALARM is sampled on the rising edge of SYSCLK.
LINECLK_REF	Low	Output	N1	**Line Clock Reference** LINECLK_REF is an output clock aligned with either the recovered receive data clock (LINECLK_REF_SEL = 0) or the transmit clock (LINECLK_REF_SEL = 1). Internal receive pointer adjustments can be avoided by using LINECLK_REF as the source for SYSCLK when the LINECLK_REF_SEL bit is '0'. Internal Transmit pointer adjustments can be avoided by using LINECLK_REF as the source of SYSCLK when the LINECLK_REF_SEL bit is '1'. If LINECLK_REF is not required, it may be powered down by writing a '1' to the LINECLK_PWRDN bit.

6.2 Parallel TelecomBus Receive Interface

All pins are 3.3V LVTTL compatible logic levels, unless stated otherwise.

Pin Name	Reset State	Type	Pin No.	Function
DD[7] DD[6] DD[5] DD[4] DD[3] DD[2] DD[1] DD[0]	Hi-Z	Tri-state Output	F1 F2 F3 E1 F4 E3 E4 D1	**Parallel TelecomBus Drop bus** The DD[7:0] output bus delivers the received SONET/SDH data. DD[7:0] defaults to tri-state on reset, and can be configured to drive tri-state on a timeslot by timeslot basis. DD[7:0] is updated on the rising edge of SYSCLK.
DDP	Hi-Z	Tri-state Output	G3	**Parallel TelecomBus Drop Data Parity** DDP reports the parity of the corresponding outgoing data bus (DD[7:0]). DDP reports even parity by default, however it may be configured for odd parity and to report parity over outgoing data bus and the control signals (DPL and DJ0J1) via microprocessor control. DDP is updated on the rising edge of SYSCLK.
DPL	Hi-Z	Tri-state Output	G4	**Parallel TelecomBus Drop Payload marker** DPL distinguishes between transport overhead bytes and synchronous payload/high order virtual container bytes in the corresponding Drop data bus (DD[7:0]). DPL is set high to mark each payload / HO-VC byte on DD[7:0] and set low to mark each transport overhead byte on DD[7:0]. DPL is updated on the rising edge of SYSCLK.
DJ0J1	Hi-Z	Tri-state Output	G2	**Parallel TelecomBus Drop J0/J1 marker** DJ0J1 pulses high when DD[7:0] carries the J0 (DPL low) and all J1 bytes (DPL high). It is low otherwise. The ARROW 155 may be configured to squelch all J1 pulses by setting the J1SQUELCH bit. By default, the J0 frame pulse is indicated, however the ARROW 155 may be configured to indicate any SONET/SDH byte as the frame pulse. DJ0J1 may be tri-stated along with the rest of the Drop bus by the DJ0J1ENB bit. DJ0J1 is updated on the rising edge of SYSCLK.
DALARM	Hi-Z	Tri-state Output	G1	**Parallel TelecomBus Drop Alarm marker** DALARM identifies STS/STM streams on the corresponding Drop data bus (DD[7:0]) that are in alarm state. Definition of the alarm condition depends on the amount of SONET/SDH processing performed by the ARROW 155. DALARM is set high when the stream on DD[7:0] is in alarm state (for instance, PAIS) and is set low when the stream is out of alarm state. DALARM may be tri-stated along with the rest of the Drop bus by the DALARMENB bit. DALARM is updated on the rising edge of SYSCLK.

Pin Name	Reset State	Type	Pin No.	Function
DSTSEN	Low	Output	J4	**Parallel TelecomBus Drop timeslot enable** DSTSEN identifies STS/STM timeslots that are currently active on the P-TCB bus. DSTSEN is high when a timeslot is active, and low when a timeslot is inactive. DSTSEN can be used to enable external tri-state buffering or muxing of a multi-drop P-TCB. When the DTBOEB bit is '1', the Drop bus is tri-state when DSTSEN is '0'. DSTSEN is updated on the rising edge of SYSCLK.
J0REF	Hi-Z	Input	H1	**J0 Reference** The J0 Reference input should pulse high for one cycle every 125 μs to provide a framing reference for the Drop TelecomBus (TBSTS3_EN = 0). For the transmit STS-12/STM-4 or STS-3/STM-1 and Drop TelecomBus (TBSTS3_EN = 1) frame, it is a rising edge trigger. J0REF may be held low after the desired frame alignment is achieved. See registers 0x1FF4 and 0x1FF5 for J0REF control bits. J0REF is sampled on the rising edge of SYSCLK.

6.3 Serial Line Interface

All pins are 3.3V LVTTL compatible logic levels, unless stated otherwise.

Pin Name	Reset State	Type	Pin No.	Function
RXD_P RXD_N	Hi-Z	Input 3.3V PECL	P10 P11	**Receive Serial Data** RXD_P/N carries the receive SONET/SDH frame at 155.52 Mbit/s (OC-3/STM-1 mode). The polarity of the RXD_P/N inputs is selectable, and the default setting is non-inverted. RXD_P/N is terminated differentially on-chip with 100Ω. Note: RXD_P/N has internal biasing and can be used AC coupled.
TXD_P TXD_N	Hi-Z	Output AC Coupled PECL	N9 P9	**Transmit Serial Data** TXD_P/N carries the transmit SONET/SDH frame at 155.52 Mbit/s (OC-3/STM-1 mode). The polarity of the TXD_P/N outputs is selectable, and the default setting is non-inverted.
REFCLK_P REFCLK_N	Hi-Z	Input 3.3V PECL	P13 N12	**Reference Clock** REFCLK_P/N is a 77.76 MHz or 155.52 MHz input clock. It is used to create a 622 MHz clock internally. REFCLK_P/N is terminated differentially on-chip with 100Ω.
SD	Hi-Z	Digital Input	M8	**Signal Detect** SD indicates a valid signal on RXD_P/N from the optics. The polarity of SD is selectable, and the default setting indicates signal is present when SD is high. When SD is low, the receive traffic is squelched.

Pin Name	Reset State	Type	Pin No.	Function
ATB[1] ATB[0]	Hi-Z	Analog I/O	N11 P12	**Analog Test Bus** The ATB[1:0] test ports are reserved for test. They should be tied to VSS in normal operation.

6.4 Serial DS3/E3/STS-1E Interface

All pins are 3.3V LVTTL compatible logic levels, unless stated otherwise.

Pin Name	Mode	Type	Pin No.	Function
TCLK_0 TCLK_1 TCLK_2	Dual rail & Single rail	Output	D8 A6 C4	**Transmit Output Clock (TCLK_*x*)** TCLK_x provides the transmit direction timing for the serial line interfac3es. TCLK_x is derived from the selected REFCLK[1:0] input using the internal digital JAT. TCLK_x is a free-running clock with nominal 50% duty cycle. The frequency of TCLK depends on the mode of operation of the particular channel. For DS3 operation TCLK frequency is 44.736 MHz, for E3 operation TCLK frequency is 34.368 MHz, for STS-1E operation TCLK frequency is 51.840 MHz. If one of these pins is not needed, it may be powered down by writing '1' to the appropriate PDH_DIS[2:0] bit.
TPOS_0 TPOS_1 TPOS_2	Dual rail	Output	C7 B6 A4	**Transmit Digital Positive Pulse (TPOS _*x*)** TPOS _*x* contains the positive pulses transmitted on the B3ZS-encoded DS3 or HDB3-encoded E3 transmission system when the dual-rail output format is selected. The TPOS /TDATO_*x* pin function selections are controlled by TFRM[1:0] and the TUNI bits in the ARROW 155 Channel Transmit Configuration Registers. Output signal polarity controls are provided by the TPOSINV bit in the ARROW 155 Channel Transmit Configuration Registers. TPOS _x is updated on the rising edge of its respective TCLK_*x*. If one of these pins is not needed, it may be powered down by writing '1' to the appropriate PDH_DIS[2:0] bit. TPOS_x are shared with TDATO_x.
TDATO_0 TDATO_1 TDATO_2	Single rail	Output	C7 B6 A4	**Transmit Data (TDATO_*x*)** TDATO_*x* contains the transmit data stream when the single-rail (unipolar) output format is enabled. The TPOS /TDATO[11:0] pin function selections are controlled by TFRM[1:0] and the TUNI bits in the ARROW 155 Channel Transmit Configuration Registers. Output signal polarity controls are provided by the TPOSINV bit in the ARROW 155 Channel Transmit Configuration Registers. TDATO_*x* is updated on the rising edge of its respective TCLK_*x*. TDATO_x are shared with TPOS_x.

Pin Name	Mode	Type	Pin No.	Function
TNEG_0 TNEG_1 TNEG_2	Dual rail	Output	D7 C6 B4	**Transmit Digital Negative Pulse (TNEG_x)** TNEG_x contains the negative pulses transmitted on the B3ZS-encoded DS3 or HDB3-encoded E3 transmission system when the dual-rail NRZ output format is selected. The TNEG/TOHM pin function selections are controlled by TFRM[1:0] and the TUNI bits in the ARROW 155 Channel Transmit Configuration Registers. Output signal polarity controls are provided by the TNEGINV bit in the ARROW 155 Channel Transmit Configuration Registers. TNEG_x is updated on the rising edge of its respective TCLK_x. If one of these pins is not needed, it may be powered down by writing '1' to the appropriate PDH_DIS[2:0] bit. TNEG_x are shared with TOHM_x.
TOHM_0 TOHM_1 TOHM_2	Single rail	Output	D7 C6 B4	**Transmit Overhead Mask (TOHM_x)** TOHM_x indicates the position of overhead bits (non-payload bits) in the transmission system stream aligned with TDATO_x. TOHM_x indicates the location of the M-frame boundary for DS3, the position of the frame boundary for E3, and the position of TBD for STS-1E when the single-rail (unipolar) NRZ input format is enabled. The TNEG/TOHM[11:0] pin function selections are controlled by the TFRM[1:0] and the TUNI bits in the ARROW 155 Channel Transmit Configuration Registers. Output signal polarity controls are provided by the TNEGINV bit in the ARROW 155 Channel Transmit Configuration Registers. TOHM_x is updated on the rising edge of its respective TCLK_x. TOHM_x are shared with TNEG_x.
RCLK_0 RCLK_1 RCLK_2	Dual rail Single rail	Input	A8 D6 A5	**Receive Input Clock (RCLK_x)** RCLK_x prvides the receive direction timing for the serial line interfaces. RCLK_x is the externally recovered transmission system baud rate clock. RCLK is a free-running clock with nominal 50% duty cycle. The frequency of RCLK depends on the mode of operation of the particular slice. For DS3 operation RCLK frequency is 44.736 MHz, for E3 operation RCLK frequency is 34.368 MHz, for STS-1E operation RCLK frequency is 51.840 MHz.

Pin Name	Mode	Type	Pin No.	Function
RPOS _0 RPOS _1 RPOS _2	Dual rail	Input	C8 B7 D5	**Receive Digital Positive Pulse (RPOS _x)** RPOS _x contains the positive pulses received on the B3ZS-encoded DS3 or the HDB3-encoded E3 transmission system when the dual-rail NRZ input format is selected. The RPOS /RDATI pin function selections are controlled by the RFRM[1:0] bits in the ARROW 155 Channel Receive Configuration Registers and by the UNI bits in the DS3 FRMR, the E3 FRMR, or the STS-1E TBD Configuration Registers. Signal polarity controls are provided by the RPOSINV bit in the ARROW 155 Channel Receive Configuration Registers. RPOS _x is sampled on the rising edge of its respective RCLK_x. RPOS_x are shared with RDATI_x.
RDATI_0 RDATI_1 RDATI_2	Single rail	Input	C8 B7 D5	**Receive Data (RDATI_x)** RDATI_x contains the data stream when the single-rail (unipolar) NRZ input format is enabled. The RPOS /RDATI pin function selections are controlled by the RFRM[1:0] bits in the ARROW 155 Channel Receive Configuration Registers and by the UNI bits in the DS3 FRMR, the E3 FRMR, or the STS-1E TBD Configuration Registers. Signal polarity controls are provided by the RPOSINV bit in the ARROW 155 Channel Receive Configuration Registers. RDATI_x is sampled on the rising edge of its respective RCLK_x. RDATI_x are shared with RPOS_x.
RNEG_0 RNEG_1 RNEG_2	Dual rail	Input	B8 A7 C5	**Receive Digital Negative Pulse (RNEG_x)** RNEG_x contains the negative pulses received on the B3ZS encoded DS3 or the HDB3-encoded E3 transmission system when the dual-rail NRZ input format is selected. The RNEG/RLCV pin function selections are controlled by the RFRM[1:0] bits in the ARROW 155 Channel Receive Configuration Registers, the UNI bits in the DS3 FRMR, E3 FRMR, or STS-1E TBD Configuration Registers. Signal polarity controls are provided by the RNEGINV bit in the ARROW 155 Channel Receive Configuration Registers. RNEG_x is sampled on the rising edge of its respective RCLK_x. RNEG_x are shared with RLCV_x.

Pin Name	Mode	Type	Pin No.	Function
RLCV_0 RLCV_1 RLCV_2	Single Rail	Input	B8 A7 C5	**Receive Line Code Violation (RLCV_x)** RLCV_x contains line code violation indications when the single-rail (unipolar) NRZ input format is enabled. Each line code violation is represented by an RCLK[11:0] period-wide pulse. The RNEG/RLCV pin function selections are controlled by the RFRM[1:0] bits in the ARROW 155 Channel Receive Configuration Registers, the UNI bits in the DS3 FRMR, E3 FRMR, or STS-1E Configuration Registers. Signal polarity controls are provided by the RNEGINV bit in the ARROW 155 Channel Receive Configuration Registers. RLCV_x is sampled on the rising edge of its respective RCLK_x. RLCV_x are shared with RNEG_x.
PDHREFCLK1 PDHREFCLK0	Dual rail & Single rail	Input	B12 D10	**Serial Jitter Attenuation Reference Clocks (PDHREFCLK[1:0])** PDHREFCLK[1:0] are the reference clocks for the jitter attenuators as well as a clock reference for other portions of each channel. For DS3 rates, PDHREFCLK[1:0] is a nominal 44.736 MHz free-running clock with 50% duty cycle. For E3 rates, PDHREFCLK[1:0] is a nominal 34.368 MHz free-running clock with 50% duty cycle. For STS-1E (STS-1E) rates, PDHREFCLK[1:0] is a nominal 51.840 MHz free-running clock with 50% duty cycle. Each channel has independent control over which Serial Jitter Attenuation Reference Clock to be used (PDHREFCLK[1:0]). In this way, the ARROW 155 may support multiple rates simultaneously. PDHREFCLK1 provides the reference clock for the Digital CSU. PDHREFCLK0 provides the reference clock for the Analog CSU. PDHREFCLK[1:0] must be jitter and wander free, as any jitter or wander on these clock inputs will directly map to the transmit data stream.

6.5 DS3/E3/STS-1E Overhead Interface

All pins are 3.3V LVTTL compatible logic levels, unless stated otherwise. If this interface is not needed, it may be powered down by writing ‘1’ to the PDH_OH_DIS bit.

Pin Name	Type	Pin No.	Function
OHCLK	Input	A3	**Serial Overhead Insertion/Extraction Clock (OHCLK)** OHCLK is a nominal 77.76 MHz free-running clock that controls the serial DS3/E3/STS-1E transmit serial overhead insertion and receive overhead serial extraction interfaces.

Pin Name	Type	Pin No.	Function
OHCH[1] OHCH[0]	Output	B3 A2	**Serial Overhead Insertion/Extraction Channel (OHCH[1:0])** OHCH[1:0] indicates which DS3/E3 or STS-1E channel's overhead control information (TOHVAL, TOHFA, ROHVAL, ROHFA, ROH) is being updated. Channel numbers 0 to 2 are valid while channel number 3 is reserved and must be ignored. OHCH[1:0] is updated on the rising edge of OHCLK.
TOHVAL	Output	B2	**Transmit Overhead Insertion Valid (TOHVAL)** TOHVAL shows whether or not data is valid on the TOHFA and whether TOH and TOHINS can be sampled for the DS3/E3/STS-1E channel displayed on OHCH[1:0]. TOHVAL is updated on the rising edge of OHCLK.
TOHFA	Output	B1	**Transmit DS3/E3/STS-1E Overhead Frame Alignment (TOHFA)** TOHFA is used to align the individual overhead bits in the transmit overhead data stream, TOH, to the DS3 M-frame, the E3 frame, or the STS-1E frame of the channel specified by OHCH[1:0]. For DS3, TOHFA is high during the X1 overhead bit position in the TOH stream. For G.832 E3, TOHFA is high during the first bit of the FA1 byte. For G.751 E3, TOHFA is high during the RAI overhead bit position in the TOH stream. For STS-1E, TOHFA is high during the first bit of the J1 byte. TOHFA is updated on the rising edge of OHCLK.
TOHINS	Input	C3	**Transmit DS3/E3/STS-1E Overhead Insertion (TOHINS)** TOHINS controls the insertion of the DS3, E3, or STS-1E, overhead bits from the TOH input for the channel specified by OHCH[1:0]. In order for the bit to be inserted, TOHVAL must also be high. When TOHINS is high, the overhead bit in the TOH stream is inserted in the transmitted DS3, E3, or STS-1E frame. When TOHINS is low, the DS3, E3, or STS-1E overhead bit is generated and inserted internally. If TOHINS is high, the TOH input has precedence over the internal data link transmitter, or any internal register bit setting. TOHINS is sampled on the rising edge of OHCLK. Special note for STS-1E operation: when TPDIS in register 0x142, 0x342, or 0x542 is set to '1', TOHINS must always be set low for the respective time slot. When TPDIS is set to '0', TOHINS will select between the TOH port and internal holding registers for the source of path overhead in the transmitted STS-1E data stream.

Pin Name	Type	Pin No.	Function
TOH	Input	C2	**Transmit DS3/E3/STS-1E Overhead Data (TOH)** When configured for DS3 operation, TOH contains the overhead bits (C, F, X, P, and M) that may be inserted in the transmit DS3 stream specified by OHCH[1:0]. When configured for G.832 E3 operation, TOH contains the overhead bytes (FA1, FA2, EM mask, TR, MA, NR, and GC) that may be inserted in the transmit G.832 E3 stream specified by OHCH[1:0]. When configured for G.751 E3 operation, TOH contains the overhead bits (RAI, National Use, Stuff Indication, and Stuff Opportunity) that may be inserted in the transmit G.751 E3 stream specified by OHCH[1:0]. When configured for STS-1E operation, TOH contains the overhead bytes (J1, B3, C2, G1, F2, H4, Z3, Z4, and Z5) that may be inserted in the transmit STS-1E stream specified by OHCH[1:0]. Note that the B3 byte acts as an error mask for the internally computed B3 byte. If TOHINS is high, the TOH input has precedence over the internal data link transmitter, or any other internal register bit setting. TOH is sampled on the rising edge of OHCLK.
ROHVAL	Output	C1	**Receive Overhead Extraction Valid (ROHVAL)** ROHVAL shows if data is valid on ROHFA and ROH for the DS3/E3/STS-1E channel specified by OHCH[1:0]. ROHVAL is updated on the rising edge of OHCLK.
ROHFA	Output	D3	**Receive DS3/E3/STS-1E Overhead Frame Alignment (ROHFA)** ROHFA locates the individual overhead bits in the received overhead data stream, ROH, for the channel specified by OHCH[1:0]. ROHFA is high during the X1 overhead bit position in the ROH stream when processing a DS3 stream. ROHFA is high during the first bit of the FA1 byte when processing a G.832 E3 stream. ROHFA is high during the RAI overhead bit position when processing a G.751 E3 stream. ROHFA is high during the first bit of the J1 byte when processing a STS-1E stream. ROHFA is updated on the rising edge of OHCLK.
ROH	Output	D2	**Receive DS3/E3/STS-1E Overhead Data (ROH)** ROH contains the overhead bits (C, F, X, P, and M) extracted from the received DS3 stream specified by OHCH[1:0]. ROH contains the overhead bytes (FA1, FA2, EM, TR, MA, NR, and GC) extracted from the received G.832 E3 streams specified by OHCH[1:0]. ROH contains the overhead bits (RAI, National Use, Stuff Indication, and Stuff Opportunity) extracted from the received G.751 E3 stream specified by OHCH[1:0]. ROH contains the overhead bytes (J1, B3, C2, G1, F2, H4, Z3, Z4, Z5) extracted from the received STS1-E stream specified by OHCH[1:0]. ROH is updated on the rising edge of OHCLK.

Pin Name	Type	Pin No.	Function
REF8KO	Output	M5	**Reference 8kHz Output (REF8KO)** REF8KO is an 8 kHz reference derived from one of the selected clocks {RCLK[2:0], TCLK[2:0], SYSCLK, RXCLK (recovered) or TXCLK (generated)}. When SYSCLK, RXCLK or TXCLK is selected as the source, a free-running divide-down counter is used to generate 50/50 duty cycle REF8KO so it will not glitch on reframe actions. When RCLK[2:0] or TCLK[2:0] is selected as the source, REF8KO will pulse high for one clock period every 125 µs. REF8KO should be treated as a glitch-free asynchronous signal. If this pin is not required, it may be powered down with the ALARM_DIS bit.

6.6 SONET/SDH Overhead Interface

All pins are 3.3V LVTTL compatible logic levels, unless stated otherwise.

Pin Name	Type	Pin No.	Function
TTOHCLK	Output	H3	**Transmit Transport Overhead Clock (TTOHCLK)** TTOHCLK provides timing for the transmit section, line, and path overhead insertion. In STS-3/STM-1 mode, TTOHCLK is a nominal 5.184 MHz clock generated by gapping a 6.48 MHz clock. In STS-12/STM-4 mode, TTOHCLK is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. TTOHCLK has a 33% high duty cycle. TTOHFP is updated on the falling edge of TTOHCLK. TTOH and TTOHEN are sampled on the rising edge of TTOHCLK. If this pin is not required, it may be powered down with the SON_OH_DIS bit.
TTOHFP	Output	H2	**Transmit Transport Overhead Frame Pulse (TTOHFP)** TTOHFP provides timing for the transmit section and line overhead insertion. TTOHFP is used to indicate the most significant bit (MSB) on TSLD and TTOH. TTOHFP is set high when the MSB of the: D1 or D4 byte should be present on TSLD. First A1 byte should be present on TTOH. TTOHFP can be sampled on the rising edge of TTOHCLK and TSLDCLK. TTOHFP is updated on the falling edge of TTOHCLK. If this pin is not required, it may be powered down with the SON_OH_DIS bit.
TTOH	Input	C10	**Transmit Transport Overhead (TTOH)** The transmit transport overhead (TTOH) signal contains the transport overhead bytes (A1, A2, J0, Z0, E1, F1, D1-D3, H3, K1, K2, D4-D12, Z1/S1, Z2/M1, and E2) to be transmitted and the error masks to be applied on B1, B2, H1 and H2. TTOH is sampled on the rising edge of TTOHCLK.

Pin Name	Type	Pin No.	Function
TTOHEN	Input	A10	**Transmit Transport Overhead Insert Enable (TTOHEN)** TTOHEN controls the insertion of the transmit transport overhead data which is inserted in the outgoing stream. When TTOHEN is high during the most significant bit of a TOH byte on TTOH, the sampled TOH byte is inserted into the corresponding transport overhead byte positions (A1, A2, J0, Z0, E1, F1, D1-D3, H3, K1, K2, D4-D12, Z1/S1, Z2/M1, and E2 bytes). When TTOHEN is low during the most significant bit of a TOH byte on TTOH, that sampled byte is ignored and the default values are inserted into these transport overhead bytes. When TTOHEN is high during the most significant bit of the H1, H2, B1, or B2 TOH byte positions on TTOH, the sampled TOH byte is logically XORed with the associated incoming byte to force bit errors on the outgoing byte. A logic low bit in the TTOH byte allows the incoming bit to go through while a bit set to logic high will toggle the incoming bit. A low level on TTOHEN during the MSB of the TOH byte disables the error forcing for the entire byte. TTOHEN is sampled on the rising edge of TTOHCLK.
TPOHCLK	Output	C9	**Transmit Path Overhead Clock (TPOHCLK)** TPOHCLK provides timing for the transmit path overhead insertion. TPOHCLK is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. TPOHCLK has a 33% high duty cycle. TPOHFP and TPOHRDY are updated on the falling edge of TPOHCLK. TPOH and TPOHEN are sampled on the rising edge of TPOHCLK. If this pin is not required, it may be powered down with the SON_OH_DIS bit.
TPOHFP	Output	D9	**Transmit Path Overhead Frame Pulse (TPOHFP)** TPOHFP provides timing for the transmit path overhead insertion. TPOHFP is used to indicate the most significant bit (MSB) on TPOH. TPOHFP is set high when the MSB of the first J1 byte should be present on TPOH. TPOHFP can be sampled on the rising edge TPOHCLK. TPOHFP is updated on the falling edge of TPOHCLK. If this pin is not required, it may be powered down with the SON_OH_DIS bit.

Pin Name	Type	Pin No.	Function
TPOH	Input	C11	**Transmit Path Overhead (TPOH)** TPOH signal contains the path overhead bytes (J1, C2, G1, F2, Z3, Z4, and Z5) to be transmitted in the SONET/SDH path overhead and the error masks to be applied on B3 and H4 on the outgoing TelecomBus stream. A path overhead byte is accepted for transmission when TPOHEN set high by an external source, indicating a valid byte, and when TPOHRDY is set high. TPOH will be ignored when TPOHEN is set low. When TPOHRDY is set low, the byte must be re-presented at the next opportunity. Note that in OC-3 mode, path overhead will still be presented for 12 paths, but only paths 1, 5, and 9 are valid. Path Overhead must presented at every opportunity for correct operation. TPOH is sampled on the rising edge of TPOHCLK.
TPOHEN	Input	B11	**Transmit Path Overhead Insert Enable (TPOHEN)** TPOHEN controls the insertion of the transmit path overhead data which is inserted in the outgoing stream. TPOHEN shall be set high during the most significant bit of a POH byte to indicate valid data on the TPOH input. This byte will be accepted for transmission if TPOHRDY is also set high. If TPOHRDY is set low, the byte is rejected and must be re-presented at the next opportunity. Accepted bytes sampled on TPOH are inserted into the corresponding path overhead byte positions (for the J1, C2, G1, F2, Z3, Z4, and Z5 bytes). The byte on TPOH is ignored when TPOHEN is set low during the most significant bit position. When the byte at the B3 or H4 byte position on TPOH is accepted, it is used as an error mask to modify the corresponding transmit B3 or H4 path overhead byte, respectively. The accepted error mask is XORed with the corresponding B3 or H4 byte before it is transmitted. Path Overhead must be presented at every opportunity for correct operation. TPOHEN is sampled on the rising edge of the TPOHCLK.
TPOHRDY	Output	A11	**Transmit Path Overhead Insert Ready (TPOHRDY)** TPOHRDY signal indicates if the TPOH is ready to accept the applied byte. TPOHRDY is set high during the most significant bit of a POH byte to indicate readiness to accept the byte on the TPOH input. This byte will be accepted if TPOHEN is also set high. If TPOHEN is set low, the byte is invalid and is ignored. TPOHRDY is set low to indicate that the ARROW 155 is unable to accept the byte, and expects the byte to be re-presented at the next opportunity. Path Overhead must be presented at every opportunity for correct operation. TPOHRDY is updated on the falling edge of TPOHCLK. If this pin is not required, it may be powered down with the SON_OH_DIS bit.

Pin Name	Type	Pin No.	Function
TSLDCLK	Output	B9	**Transmit section or Line Data Communication Channel Clock (TSLDCLK)** TSLDCLK is used to clock in the transmit section or line DCC (TSLD). When section DCC is selected, TSLDCLK is a nominal 192 kHz clock with 50% duty cycle. When line DCC is selected, TSLDCLK is a nominal 576 kHz clock with 50% duty cycle. TSLD is sampled on the rising edge of TSLDCLK and TTOHFP is used to identify the MSB of the D1 or the D4 byte on TSLD. If this pin is not required, it may be powered down with the SON_OH_DIS bit.
TSLD	Input	A9	**Transmit section or Line Data Communication Channel Data (TSLD)** TSLD signal contains the section DCC (D1-D3) or the line DCC (D4-D12) to be transmitted. TSLD is sampled on the rising edge of TSLDCLK. TTOHFP is used to identify the MSB of the D1 or the D4 byte on TSLD. The TTOH and TTOHEN inputs take precedence over TSLD.
RTOHCLK	Output	P7	**Receive Transport Overhead Clock (RTOHCLK)** RTOHCLK signal provides timing for the receive section and line overhead extraction. In STS-3/STM-1 mode, RTOHCLK is a nominal 5.184 MHz clock generated by gapping a 6.48 MHz clock. In STS-12/STM-4 mode, RTOHCLK is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. RTOHCLK has a 33% high duty cycle. If this pin is not required, it may be powered down with the SON_OH_DIS bit.
RTOHFP	Output	L8	**Receive Transport Overhead Frame Pulse (RTOHFP)** RTOHFP provides timing for the transmit section and line overhead insertion. RTOHFP is used to indicate the most significant bit (MSB) on RSLD and RTOH. RTOHFP is set high when the MSB of the: D1 or D4 byte is present on RSLD. First A1 byte is present on RTOH. RTOHFP can be sampled on the rising edge of RTOHCLK and RSLDCLK. RTOHFP is updated on the falling edge of RTOHCLK. If this pin is not required, it may be powered down with the SON_OH_DIS bit.
RTOH	Output	N3	**Receive Transport Overhead (RTOH)** RTOH contains the received transport overhead bytes (A1, A2, J0, Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, Z1/S1, Z2/M1, and E2) extracted from the Receive PECL stream. RTOH is updated on the falling edge of RTOHCLK. If this pin is not required, it may be powered down with the SON_OH_DIS bit.

Pin Name	Type	Pin No.	Function
RPOHCLK	Output	P3	**Receive Path Overhead Clock (RPOHCLK)** RPOHCLK signal provides timing for the receive path line overhead extraction. RPOHCLK is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. RPOHCLK has a 33% high duty cycle. If this pin is not required, it may be powered down with the SON_OH_DIS bit.
RPOHFP	Output	M4	**Receive Path Overhead Frame Pulse (RPOHFP)** RPOHFP provides timing for the receive path overhead extraction. RPOHFP is used to indicate the most significant bit (MSB) on RPOH, B3E, and RRCPDAT. RPOHFP is set high when the: MSB of the J1 byte is present on RPOH. First possible BIP error position is present on B3E. OOF bit position is present on RRCPDAT. RPOHFP can be sampled on the rising edge of RPOHCLK. RPOHFP is updated on the falling edge of RPOHCLK. If this pin is not required, it may be powered down with the SON_OH_DIS bit.
RPOH	Output	P2	**Receive Path Overhead (RPOH)** RPOH contains the received path overhead bytes (J1, B3, C2, G1, F2, H4, Z3, Z4, and Z5) extracted from the SONET/SDH path overhead of the Receive PECL stream. The RPOHEN signal is set high to indicate valid path overhead bytes on RPOH. RPOH is updated on the falling edge of RPOHCLK. If this pin is not required, it may be powered down with the SON_OH_DIS bit.
RPOHEN	Output	N4	**Receive Path Overhead Enable (RPOHEN)** RPOHEN signal indicates valid path overhead bytes on RPOH. When RPOHEN signal is set high, the corresponding path overhead byte presented on RPOH is valid. When RPOHEN is set low, the corresponding path overhead byte presented on RPOH is invalid. RPOHEN is updated on the falling edge of RPOHCLK. If this pin is not required, it may be powered down with the SON_OH_DIS bit.
SALM	Output	M6	**Section Alarm Indication (SALM)** SALM signal is set high when an out of frame (OOF), loss of signal (LOS), loss of frame (LOF), line alarm indication signal (AIS-L), line remote defect indication (RDI-L), APS byte failure, section trace identifier mismatch (TIM-S), section trace identifier unstable (TIU-S), signal fail (SF) or signal degrade (SD) alarm is detected. Each alarm indication can be independently enabled using bits in the SARC RSALM registers. SALM is updated on the falling edge of RPOHCLK. If this pin is not required, it may be powered down with the ALARM_DIS bit.

Pin Name	Type	Pin No.	Function
RALM	Output	L6	**Receive Alarm Indication (RALM)** RALM signal is set high for the corresponding path when a section alarm, path loss of pointer (LOP-P), path alarm indication signal (AIS-P), path remote defect indication (RDI-P), path enhance remote defect indication (ERDI-P), path label mismatch (PLM), path label unstable (PLU), path unequipped (UNEQ), path payload defect indication (PDI-P), path trace identifier mismatch (TIM-P) or path trace identifier unstable (TIU-P) alarm is detected. Each alarm indication can be independently enabled using bits in the SARC RPALM registers. RALM is updated on the falling edge of RPOHCLK. If this pin is not required, it may be powered down with the ALARM_DIS bit.
B3E	Output	P5	**Bit interleaved Parity Error (B3E)** B3E signal carries the path BIP-8 errors detected for each SONET/SDH payload. B3E is set high for one RPOHCLK clock cycle for each path BIP-8 error detected (up to eight errors per path per frame). When BIP-8 errors are treated on a block basis, B3E is set high for one RPOHCLK clock cycle for up to eight path BIP-8 errors detected (up to one error per path per frame). Path BIP-8 errors are detected by comparing the extracted path BIP-8 byte (B3) with the computed path BIP-8 byte of the previous frame. B3E is updated on the falling edge of RPOHCLK. If this pin is not required, it may be powered down with the ALARM_DIS bit.
RSLDCLK	Tristate Output	L5	**Receive section or Line Data Communication Channel Clock (RSLDCLK)** RSLDCLK is used to update the receive section or line DCC (RSLD). When section DCC is selected, RSLDCLK is a nominal 192 kHz clock with 50% duty cycle. When line DCC is selected, RSLDCLK is a nominal 576 kHz clock with 50% duty cycle. The RSLDSEL bit in the RRMP 1990H registers selects the section or line DCC and the RSLDTS bit tri-states RSLDCLK and RSLD outputs. RSLD is updated on the falling edge of RSLDCLK. RTOHFP may be used to identify the MSB of the D1 or the D4 byte on RSLD.
RSLD	Tristate Output	P4	**Receive section or Line Data Communication Channel Data (RSLD)** RSLD contains the received section DCC (D1-D3) or line DCC (D4-D12). The RSLDSEL bit in the RRMP 1990H registers selects the section or line DCC and the RSLDTS bit tri-states RSLDCLK and RSLD outputs. RSLD is updated on the falling edge of RSLDCLK. The signal should be sampled externally on the rising edge of RSLDCLK. RTOHFP is used to identify the MSB of the D1 or the D4 byte on RSLD.

6.7 Ring Control Port

All pins are 3.3V LVTTL compatible logic levels, unless stated otherwise.

Pin Name	Type	Pin No.	Function
RRCPDAT	Output	N7	**Receive ring control port data (RRCPDAT)** This signal contains the receive ring control port data stream when the ring control port is enabled. The receive ring control port data contains all of the section, line and path defects in the receive data stream. Table 20 defines the bit positions on RRCPDAT. RRCPDAT can be connected directly to the TRCPDAT input of a mate ARROW 155 in ring-based add-drop multiplexer applications. RRCPDAT is updated on the falling edge of RPOHCLK. If this pin is not required, it may be powered down with the RRCP_DIS bit. If the Ring Control Port is required, SON_OH_DIS must be '0'.
TRCPCLK	Input	N6	**Transmit ring control port clock (TRCPCLK**) This signal provides timing for the transmit ring control port when the ring control port is enabled. TRCPCLK is a 25.92 MHz clock gapped down to 20.736 MHz. TRCPCLK has a 33% high duty cycle and can be connected directly to the RPOHCLK output of a mate ARROW 155 in ring-based add-drop multiplexer applications. TRCPFP and TRCPDAT are sampled on the rising edge of TRCPCLK.
TRCPDAT	Input	M7	**Transmit ring control port data (TRCPDAT)** This signal contains the transmit ring control port data stream when the ring control port is enabled. The transmit ring control port data contains all of the section, line and path defects in the receive data stream. Table 20 defines the bit positions on TRCPDAT. TRCPDAT can be connected directly to the RRCPDAT output of a mate ARROW 155 in ring-based add-drop multiplexer applications. TRCPDAT is sampled on the rising edge of TRCPCLK.
TRCPFP	Input	P6	**Transmit ring control port frame position (TRCPFP)** This signal identifies bit positions in the transmit ring control port data (TRCPDAT) when the ring control port is enabled. TRCPFP is set high during the OOF bit position in the TRCPDAT stream. TRCPFP can be connected directly to the RPOHFP output of a mate ARROW 155 in ring-based add-drop multiplexer applications. TRCPFP is sampled on the rising edge of TRCPCLK.

6.8 Microprocessor Interface

Pin Name	Type	Pin No.	Function
CSB	Input	G14	**Active-Low Chip Select (CSB)** The CSB signal is low during ARROW 155 register accesses. When CSB is high, the RDB and WRB inputs are ignored. When CSB is low, RDB and WRB are valid. CSB must be high when RSTB is low to properly reset the chip. If CSB is not required (i.e., register accesses are controlled using the RDB and WRB signals only), CSB must be connected to an inverted version of the RSTB input.
WRB	Input	F12	**Active-Low Write Strobe (WRB)** The WRB signal is low during ARROW 155 register write accesses. The DA[15:0] bus contents are clocked into the addressed register on the rising edge of WRB while CSB is low.
RDB	Input	G12	**Active-Low Read Enable (RDB)** The RDB signal is low during ARROW 155 register read accesses. The ARROW 155 drives the DA[15:0] bus with the contents of the addressed register while RDB and CSB are low.
D[15] D[14] D[13] D[12] D[11] D[10] D[9] D[8] D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O	M14 L12 L13 L14 K12 K13 K14 J11 J12 J13 J14 H12 H13 H14 H11 G13	**Bi-Directional Data (D[15:0])** The DA[15:0] bus is used during ARROW 155 register read and write accesses.
A[13] A[12] A[11] A[10] A[9] A[8] A[7] A[6] A[5] A[4] A[3] A[2] A[1] A[0]	Input	F13 F14 F11 E11 E12 E14 D12 D14 D13 C13 C14 B14 B13 A13	**Address Bus (A[13:0])** The address bus A[13:0] selects specific registers during ARROW 155 register accesses.
RSTB	Schmitt Input Internal pull up	N14	**Reset** This active low signal provides an asynchronous reset to the ARROW 155.

Pin Name	Type	Pin No.	Function
ALE	Input Internal pull up	C12	**Address Latch Enable (ALE)** The ALE is active-high and latches the address from the Data / Address bus (DA[15:0]) when it transitions low. When ALE is high, the internal address latches are transparent.
INTB	Open Drain Output	M13	**Active-Low Interrupt (INTB)** The INTB signal is set low when a ARROW 155 interrupt source is active and that source is unmasked. The ARROW 155 may be enabled to report many alarms or events via interrupts. Examples of interrupt sources are loss of signal (LOS), loss of frame (LOF), line AIS, line remote defect indication (LRDI) detect, loss of pointer (LOP), path AIS, path remote defect indication and others. INTB is tri-stated when all the enabled interrupt sources are acknowledged via an appropriate register access. INTB is an open drain output.

6.9 JTAG & Scan Interface

All pins are 3.3V LVTTL compatible logic levels.

Pin Name	Type	Pin No.	Function
TCK	Input	L9	**Test Clock** IEEE 1149.1 JTAG test access port.
TMS	Input Internal pull up	M9	**Test Mode Select** IEEE 1149.1 JTAG test access port.
TDI	Input Internal pull up	N8	**Test Data Input** IEEE 1149.1 JTAG test access port.
TDO	Tri-state	L10	**Test Data Output** IEEE 1149.1 JTAG test access port.
TRSTB	Schmitt Input Internal pull up	P8	**Active low Test Reset** IEEE 1149.1 JTAG test access port.

6.10 Power and Ground

Pin Name	Type	Pin No.	Function
VDDO	Power	B10, B5, E13, E2, G11, H4, K2, L7, N5	**+3.3V I/O Supply Voltage** Should be connected to a well de-coupled DC supply.
VDDI	Power	E9, E7, E5, F10, G5, H10, J5, K6	**+1.8V Core Supply Voltage** Should be connected to a well de-coupled DC supply.

Pin Name	Type	Pin No.	Function
VSS	Ground	A14, A1, D11, D4, E10, E8, E6, F9, F8, F7, F6, F5, G10, G9, G8, G7, G6, H9, H8, H7, H6, H5, J10, J9, J8, J7, J6, K10, K9, K7, K5, L11, L3, M12, N13, N10, P14, P1	**Supply Ground**
AVDH	Analog Power	K11	**Analog Power High** Pins for the analog circuits. The AVDH pins should be connected through passive filtering networks to a well-decoupled +3.3V analog power supply. (See PMC-2030859 Hardware Design Guide)
AVDL1	Analog Power	K8 M10	**PECL Analog Power Low** Pins for the analog circuits. The AVDL pins should be connected through passive filtering networks to a well-decoupled +1.8V analog power supply. (See PMC-2030859 Hardware Design Guide)
AVDL2	Analog Power	M11	**CSU Analog Power Low** Pins for the analog circuits. The AVDL pins should be connected through passive filtering networks to a well-decoupled +1.8V analog power supply. (See PMC-2030859 Hardware Design Guide)
AVD1	Analog Power	A12	**CSU Analog Power High** The analog power pins for the analog core. The AVD pins should be connected through passive filtering networks to a well-decoupled +3.3V analog power supply. (See PMC-2030859 Hardware Design Guide)

7 Functional Description

7.1 Data and Clock Recovery Unit (DCRU622)

The ARROW 155 employs a digital clock and data recovery unit. The DCRU deserializes the 622 bit/s PECL input stream and recovers the receive clock from the data transitions. On device reset (hardware or software), the DCRU defaults to its power-down state. Before the DCRU can begin to recover the clock and data, ‘0’ should be written to the PWRDN bit in register 0x1AB7.

The digital DLL creates the receive clock, and is composed of two sections: the delay line and a control state machine. The state machine uses up and down control signals from the phase detector to select the appropriate delay tap of the delay line. The delay line creates an internal clock, which is used by the phase detector/data sampler to recover the data from the serial stream (the recovered clock).

The state machine adjusts the phase delay of the delay line one tap at a time to prevent glitches on the recovered clock. The state machine is limited to adjust the phase every 19.3 ns (Twelve 622 MHz cycles). After system reset, the state machine performs an initial search for 1 UI of delay by starting at the beginning of the delay line and increasing the delay until the delay line is exactly 1 UI of delay. To find the initial lock position will take a maximum 617 ns (12*32 622 MHz cycles).

When the initial lock position is found, the state machine will set the RUN signal high indicating the output-recovered clock is reasonably stable. The state machine will then start to listen to the phase detector and update the recovered clock to track the incoming serial stream.

The DLL also supports a glitchless software reset function. When a write to register 0x1AB7 occurs, the software reset is triggered. The DLL will move from its current tap back to the tap with minimum delay, one tap at a time. Once the DLL has moved back to the minimum delay point, the DLL has been initialized and will start to find phase lock again. By moving back to the minimum delay point one tap at a time, the outgoing recovered clock (externally available on LINECLK_REF) will not glitch. Maximum reset time is 1.23 µs (24*32 622 MHz cycles).

The phase detector and data sampler use the recovered clock from the delay line to sample the incoming data stream. The data sampler is also used to determine the phase difference between the recovered clock and the incoming data stream. The phase detector samples the incoming serial data stream on both the rising and falling edge of the recovered clock to determine the phase offset between the two. It can then adjust the phase of the recovered clock for correct data sampling.

7.2 SONET Frame and Byte Aligner (SFBA)

The ARROW 155 performs framing in two stages. The SFBA performs frame alignment for purposes of locating the correct byte alignment of the serial stream. Formal SONET/SDH framing is performed subsequently by the RRMP block. The SFBA is enabled when the RRMP has declared out-of-frame. The SONET Framer block searches for the framing pattern consisting of the A1, A2 framing bytes. The framing pattern is composed of three A1 bytes (F6H) followed by three A2 bytes (28H).

Upon detecting the framing bit pattern, the byte alignment of the output bus is adjusted to the new byte boundary and the output frame pulse is realigned to the first payload byte of the first STS-1/STM-0 following the J0/Z0 bytes in the STS-3/STM-1 stream. The frame pulse synchronizes the RRMP to the new frame alignment, which should verify the frame alignment by observing the framing pattern during the next frame and then remove the out-of-frame condition (OOF). When OOF is de-asserted, the current frame alignment is maintained as long as OOF remains low.

A second occurrence of the framing bit pattern while the new framing alignment is being verified by RRMP (i.e. while OOF is asserted) results in the realignment of the byte boundary of the output bus and a new frame pulse indication. Thus, mimic framing bit patterns are rejected unless the mimic framing bit pattern occurs twice precisely within a frame when OOF is asserted.

The SFBA declares Loss Of Transition if either a loss of power is detected on the SD input or a bit sequence of 97 or more consecutive ones or zeros is received on the input data bus.

7.3 Receive Regenerator and Multiplexer Processor (RRMP)

The Receive Regenerator and Multiplexer Processor (RRMP) block extracts and processes the transport overhead of the received data stream.

The RRMP frames to the data stream by operating with the upstream SFBA that searches for occurrences of the A1/A2 framing pattern and generates the frame pulse. Once the RRMP has found an A1/A2 framing pattern, the RRMP monitors for the next occurrence of the framing pattern 125µs later. Two framing pattern algorithms are provided to improve performance in the presence of bit errors. In algorithm 1, the RRMP declares frame alignment (removes OOF defect) when 3 A1 and 3A2 bytes are seen error-free. In algorithm 2, the RRMP declares frame alignment (removes OOF defect) when one A1 byte and the first four bits of one A2 byte are seen error-free. Once in frame, the RRMP monitors the framing pattern and declares OOF when one or more bit errors in the framing pattern are detected for four consecutive frames. Again, depending upon the algorithm, either 6 framing bytes or 12 framing bits are examined for bit errors in the framing pattern.

Table 3 RRMP Framing Algorithms

Algorithm	A1/A2 Bytes used for In-Frame or Out-of-Frame Detection
1	All A1 Bytes + All A2 bytes
2	First A1 Byte + first 4 bits of Last A2 Byte

The performance of these framing algorithms in the presence of bit errors and random data is robust. When looking for frame alignment, the performance of each algorithm is dominated by the alignment algorithm used in the SFBA, which always examines 3 A1 and 3 A2 framing bytes. The probability of falsely framing to random data is less than 0.00001% for either algorithm. Once in frame alignment, the RRMP continuously monitors the framing pattern. When the incoming stream contains a 10^{-3} BER, the first algorithm provides a 99.75% probability that the mean time between OOF occurrences is 1.3 seconds and the second algorithm provides a 99.75% probability that the mean time between OOF occurrences is 7 minutes.

The RRMP also detects loss of frame (LOF) defect and loss of signal (LOS) defect. LOF is declared when an out of frame (OOF) condition exists for a total period of 3 ms during which there is no continuous in frame period of 3 ms. LOF is removed when an in frame condition exists for a continuous period of 3 ms. LOS is declared when a continuous period of 20 µs without transitions on the received data stream is detected. LOS is removed when two consecutive framing patterns are found (based on algorithm 1 or algorithm 2) and during the intervening time (one frame), there are no continuous periods of 20 µs without transitions on the received data stream.

The RRMP calculates the section BIP-8 error detection code on the scrambled data of the complete frame. The section BIP-8 code is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 code is compared with the BIP-8 code extracted from the B1 byte of STS-1 (STM-0) #1 of the following frame after descrambling. Any difference indicates a section BIP-8 error. The RRMP accumulates section BIP-8 errors in a microprocessor readable 16-bit saturating counter (up to 1 second accumulation time). Optionally, block section BIP-8 errors can be accumulated.

The RRMP optionally descrambles the received data stream.

The RRMP calculates the line BIP-8 error detection codes on the de-scrambled line overhead and synchronous payload envelope bytes of the constituent STS-1 (STM-0). The line BIP-8 code is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 codes are compared with the BIP-8 codes extracted from the B2 byte of the constituent STS-1 (STM-0) of the following frame after descrambling. Any difference indicates a line BIP-8 error. The RRMP accumulates line BIP-8 errors in a microprocessor readable 24-bit saturating counter (up to 1 second accumulation time). Optionally, block BIP-24 errors can be accumulated.

The RRMP extracts the line remote error indication (REI-L) errors from the M1 byte of STS-1 (STM-0) #3 and accumulates them in a microprocessor readable 24 bits saturating counter (up to 1 second accumulation time). Optionally, block line REI errors can be accumulated.

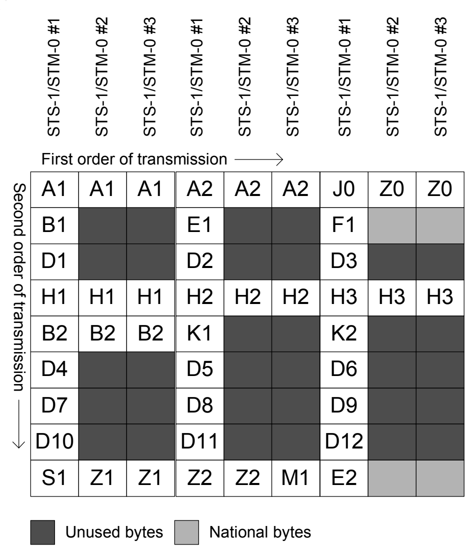
The RRMP extracts and filters the K1/K2 APS bytes for three frames. The filtered K1/K2 APS bytes are accessible through microprocessor readable registers. The RRMP also monitors the unfiltered K1/K2 APS bytes to detect APS byte failure (APSBF-L) defect, line alarm indication signal (AIS-L) defect and line remote defect indication (RDI-L) defect. APS byte failure is declared when twelve consecutive frames have been received where no three consecutive frames contain identical K1 bytes. The APS byte failure is removed upon detection of three consecutive frames containing identical K1 bytes. The detection of invalid APS codes is done in software by polling the K1/K2 APS register. Line AIS is declared when the bit pattern 111 is observed in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. Line AIS is removed when any pattern other than 111 is observed for three or five consecutive frames. Line RDI is declared when the bit pattern 110 is observed in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. Line RDI is removed when any pattern other than 110 is observed for three or five consecutive frames.

The RRMP extracts and filters the synchronization status message (SSM) for eight frames. The filtered SSM is accessible through microprocessor readable registers.

RRMP optionally inserts line alarm indication signal (AIS-L).

The RRMP extracts and serially outputs all the transport overhead (TOH) bytes on the RTOH port. The TOH bytes are output in the same order that they are received (A1, A2, J0/Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, S1/Z1, Z2/M1/Z2, and E2). RTOHCLK is the generated output clock used to provide timing for the RTOH port. RTOHCLK is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. Sampling RTOHFP high with the rising edge of RTOHCLK identifies the MSB of the first A1 byte.

Figure 9 STS-3 (STM-1) on RTOH



The RRMP optionally serially outputs the line DCC bytes on the RSLD port. RSLD is selectable to output either the section DCC bytes (D1-D3) or the line DCC bytes (D4-D12). RSLDCLK is the generated output clock used to provide timing for the RSLD port. If RSLD carries the line DCC, RSLDCLK is a nominal 576 kHz clock or if RSLD carries the section DCC, RSLDCLK is a nominal 192 kHz clock. Sampling RTOHFP high identifies the MSB of the first DCC byte on RSLD (D1 or D4).

A maskable interrupt is activated to indicate any change in the status of out of frame (OOF), loss of frame (LOF), loss of signal (LOS), line remote defect indication (RDI-L), line alarm indication signal (AIS-L), synchronization status message (COSSM), APS bytes (COAPS), and APS byte failure (APSBF) or any errors in section BIP-8, line BIP-8 and line remote error indication (REI-L).

The RRMP block provides de-scrambled data and frame alignment indication signals for use by the RHPP.

7.4 Receive Trail Trace Processor (RTTP)

The Receive Trail trace Processor (RTTP) block monitors the trail trace messages of the receive data stream for trace identifier unstable (TIU) defect and trace identifier mismatch (TIM) defect. In addition to a trail trace ignore setting (default), three trail trace algorithms are defined.

The first algorithm is BELLCORE compliant. The algorithm detects trace identifier mismatch (TIM) defect on a 16 or 64 byte trail trace message. A TIM defect is declared when none of the last 20 messages matches the expected message. A TIM defect is removed when 16 of the last 20 messages match the expected message. The expected trail trace message is a static message written in the expected page of the RTTP by an external microprocessor. Optionally, the expected message is matched when the trail trace message is all zeros.

The second algorithm is ITU compliant. The algorithm detects trace identifier unstable (TIU) defect and trace identifier mismatch (TIM) defect on a 16 or 64 byte trail trace message. The current trail trace message is stored in the captured page of the RTTP. If the length of the message is 16 bytes, the RTTP synchronizes on the MSB of the message. The byte with the MSB set high is placed in the first location of the captured page. If the length of the message is 64 bytes, the RTTP synchronizes on the CR/LF (CR = 0Dh, LF = 0Ah) characters of the message. The following byte is placed in the first location of the captured page.

A persistent trail trace message is declared when an identical message is receive for 3 or 5 consecutive multi-frames (16 or 64 frames). A persistent message becomes the accepted message. The accepted message is stored in the accepted page of the RTTP. A TIU defect is declared when one or more erroneous bytes are detected in a total of 8 messages without any persistent message in between. A TIU defect is removed when a persistent message is received.

A TIM defect is declared when the accepted message does not match the expected message. A TIM defect is removed when the accepted message matches the expected message. The expected message is a static message written in the expected page of the RTTP by an external microprocessor. Optionally, the algorithm declares a match trail trace message when the accepted message is all zeros.

The third algorithm is not BELLCORE/ITU compliant. The algorithm detects trace identifier unstable (TIU) on a single continuous trail trace byte. A TIU defect is declared when one or more erroneous bytes are detected in three consecutive 16-byte windows. The first window starts on the first erroneous byte. A TIU defect is removed when an identical byte is received for 48 consecutive frames. A maskable interrupt is activated to indicate any change in the status of trace identifier unstable (TIU) and trace identifier mismatch (TIM).

One may configure the device to monitor that Receive Trail Trace message without generating corresponding TIM or TIU related consequential actions. The TIM_DIS and TIU_DIS bits in the RHPP Pointer Interpreter Configuration Indirect Register allow TIM or TIU alarms to be blocked on a per-timeslot basis for both AU Path and TU3 Path level indications.

7.5 Receive High Order Path Processor (RHPP)

The Receive High Order Path Processor (RHPP) provides pointer interpretation, extraction of path overhead, extraction of the synchronous payload envelope (virtual container), and path level alarm and performance monitoring.

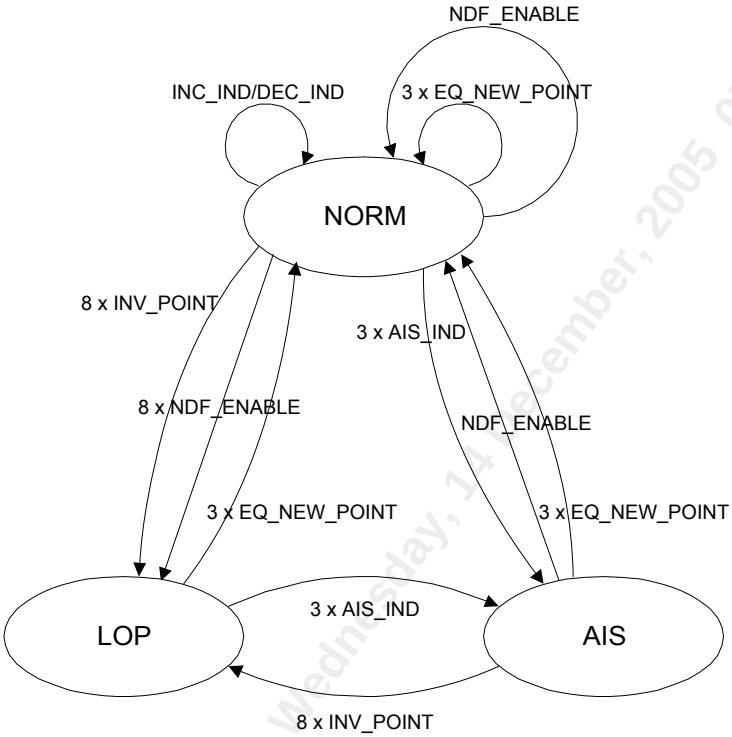
7.5.1 Pointer Interpreter

The pointer interpreter extracts and validates the H1 and H2 bytes in order to identify the location of the path overhead byte (J1) and all the synchronous payload envelop bytes (SPE) of the constituent STS-1/3c/12c (VC3/4/4-4c) payloads. The pointer interpreter is a time multiplexed finite state machine that can process any mixed of STS-1/3c/12c (AU3/4/4-4c) pointers. Within the pointer interpretation algorithm three states are defined as shown below:

- NORM_state (NORM)
- AIS_state (AIS)
- LOP_state (LOP)

The transition between states will be consecutive events (indications), e.g., three consecutive AIS indications to go from the NORM_state to the AIS_state. The kind and number of consecutive indications activating a transition is chosen such that the behavior is stable and insensitive to low BER. The only transition on a single event is the one from the AIS_state to the NORM_state after receiving a NDF enabled with a valid pointer value. It should be noted that, since the algorithm only contains transitions based on consecutive indications, non-consecutively received indications do not activate the transitions between states.

Figure 10 Pointer Interpretation State Diagram



The following events (indications) are defined:

NORM_POINT: disabled NDF + ss + offset value equal to active offset.

NDF_ENABLE: enabled NDF + ss + offset value in range of 0 to 782.

AIS_IND: H1 = FFh + H2 = FFh.

INC_IND: disabled NDF + ss + majority of I bits inverted + no majority of D bits inverted + previous NDF_ENABLE, INC_IND or DEC_IND more than 3 frames ago.

DEC_IND: disabled NDF + ss + majority of D bits inverted + no majority of I bits inverted + previous NDF_ENABLE, INC_IND or DEC_IND more than 3 frames ago.

INV_POINT: not any of the above (i.e.: not NORM_POINT, not NDF_ENABLE, not AIS_IND, not INC_IND and not DEC_IND).

NEW_POINT: disabled NDF + ss + offset value in range of 0 to 782 but not equal to active offset.

Notes on event (indication) definitions

1. Active offset is defined as the accepted current phase of the SPE (VC) in the NORM_state and is undefined in the other states.
2. Enabled NDF is defined as the following bit patterns: 1001, 0001, 1101, 1011, and 1000.
3. Disabled NDF is defined as the following bit patterns: 0110, 1110, 0010, 0100, and 0111.
4. The remaining six NDF bit patterns (0000, 0011, 0101, 1010, 1100, 1111) result in an INV_POINT indication.
5. ss bits are unspecified in SONET and have bit pattern 10 SDH (prior to G.707 2000).
6. The use of ss bits in definition of indications may be optionally disabled.
7. The requirement for previous NDF_ENABLE, INC_IND or DEC_IND be more than 3 frames ago may be optionally disabled.
8. NEW_POINT is also an INV_POINT.
9. The requirement for the pointer to be within the range of 0 to 782 in 8 X NDF_ENABLE may be optionally disabled.
10. LOP is not declared if all the following conditions exist:
    - The received pointer is out of range (>782)
    - The received pointer is static
    - The received pointer can be interpreted, according to majority voting on the I and D bits, as a positive or negative justification indication, after making the requested justification, the received pointer continues to be interpretable as a pointer justification.
    - When the received pointer returns to an in-range value, the ARROW 155 will interpret it correctly.

The transitions indicated in the state diagram are defined as follows:

INC_IND/DEC_IND: offset adjustment (increment or decrement indication)

3 x EQ_NEW_POINT: three consecutive equal NEW_POINT indications

NDF_ENABLE: single NDF_ENABLE indication

3 x AIS_IND: three consecutive AIS indications

8 x INV_POINT: eight consecutive INV_POINT indications

8 x NDF_ENABLE eight consecutive NDF_ENABLE indications

Notes on transitions indicated in state diagram

1. The transitions from NORM_state to NORM_state do not represent state changes but imply offset changes.

2. 3 x EQ_NEW_POINT takes precedence over other events and may optionally reset the INV_POINT count.

3. All three offset values received in 3 x EQ_NEW_POINT must be identical.

4. "Consecutive event counters" are reset to zero on a change of state (except the INV_POINT counter).

LOP is declared on entry to the LOP_state after eight consecutive invalid pointers or eight consecutive NDF enabled indications. Path AIS is optionally inserted in the DROP BUS when LOP is declared. The alarm condition is optionally returned to the source node by signaling the corresponding Transmit High Order Path Processor in the local ARROW 155 to insert a path RDI indication. Alternatively, if in-band error reporting is enabled, the path RDI bit in the DROP bus G1 byte is set to indicate the LOP alarm to the THPP in a remote ARROW 155.

PAIS is declared on entry to the AIS_state after three consecutive AIS indications. Path AIS is inserted in the DROP bus when AIS is declared. The alarm condition is optionally returned to the source node by signaling the corresponding Transmit High Order Path Processor in the local ARROW 155 to insert a path RDI indication. Alternatively, if in-band error reporting is enabled, the path RDI bit in the DROP bus G1 byte is set to indicate the PAIS alarm to the THPP in a remote ARROW 155.

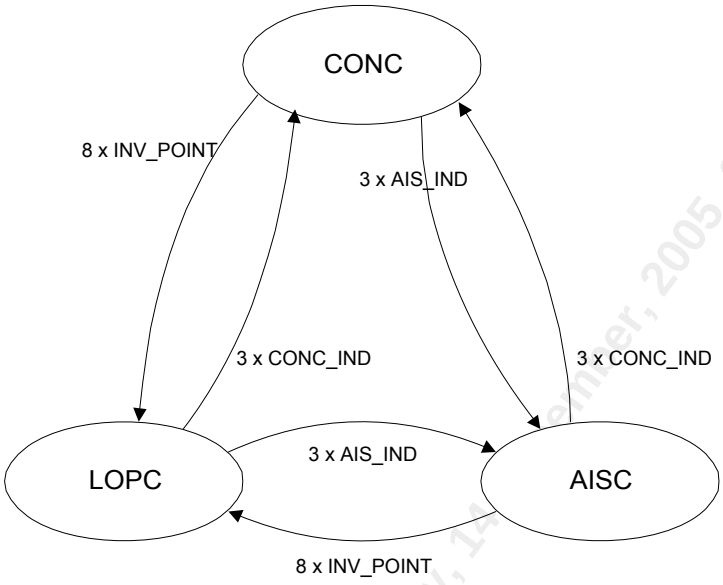
7.5.2 Concatenation Pointer Interpreter State Machine

The concatenation pointer interpreter extracts and validates the H1 and H2 concatenation bytes. The concatenation pointer interpreter is a time multiplexed finite state machine that can process any mixed of STS-1/3c/12c (AU3/4/4-4c) pointers. Within the pointer interpretation algorithm three states are defined as shown below:

- CONC_state (CONC)
- AISC_state (AISC)
- LOPC_state (LOPC)

The transitions between the states will be consecutive events (indications), e.g. three consecutive AIS indications to go from the CONC_state to the AISC_state. The kind and number of consecutive indications activating a transition is chosen such that the behavior is stable and insensitive to low BER.

Figure 11 Concatenation Pointer Interpretation State Diagram



The following events (indications) are defined:

- CONC_IND: enabled NDF + dd + "1111111111"
- AIS_IND: H1 = FFh + H2 = FFh
- INV_POINT: not any of the above (i.e.: not CONC_IND and not AIS_IND)

Notes on event (indications) definitions:

1. Enabled NDF is defined as the following bit patterns: 1001, 0001, 1101, 1011, and 1000.
2. The remaining eleven NDF bit patterns (0000, 0010, 0011, 0100, 0101, 0110, 0111, 1010, 1100, 1110, and 1111) result in an INV_POINT indication.
3. dd bits are unspecified in SONET/SDH.

The transitions indicated in the state diagram are defined as follows:

- 3 X CONC_IND: three consecutive CONC indications
- 3 x AIS_IND: three consecutive AIS indications
- 8 x INV_POINT: eight consecutive INV_POINT indications

Notes on transitions indicated in state diagram:

- Consecutive event counters are reset to zero on a change of state.

LOPC is declared on entry to the LOPC_state after eight consecutive pointers with values other than concatenation indications. Path AIS is optionally inserted in the DROP bus when LOPC is declared. The alarm condition is optionally returned to the source node by signaling the corresponding Transmit High Order Path Processor in the local ARROW 155 to insert a path RDI indication. Alternatively, if in-band error reporting is enabled, the path RDI bit in the DROP bus G1 byte is set to indicate the LOP alarm to the THPP in a remote ARROW 155.

PAISC is declared on entry to the AISC_state after three consecutive AIS indications. Path AIS is optionally inserted in the DROP bus when AISC is declared. The alarm condition is optionally returned to the source node by signaling the corresponding Transmit High Order Path Processor in the local ARROW 155 to insert a path RDI indication. Alternatively, if in-band error reporting is enabled, the path RDI bit in the DROP bus G1 byte is set to indicate the PAIS alarm to the THPP in a remote ARROW 155.

7.5.3 Error Monitoring

The RHPP calculates the path BIP-8 error detection codes on the STS-1/3c/12c (VC-3/4/4-4c) payloads. When processing a VC-3 payload, the two fixed stuff columns can be excluded from the BIP-8 calculation if the FSBIPDIS register bit is set. The path BIP-8 code is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 codes are compared with the BIP-8 codes extracted from the B3 byte of each constituent STS (VC) payload of the following frame. Any differences indicate a path BIP-8 error. The RHPP accumulates path BIP-8 errors in a microprocessor readable 16 bits saturating counter (up to 1 second accumulation time). Optionally, block BIP-8 errors can be accumulated.

The RHPP extracts the path remote error indication (REI-P) errors from bits 1, 2, 3, and 4 of the path status byte (G1) and accumulates them in a microprocessor readable 16 bits saturating counter (up to 1 second accumulation time). Optionally, block REI errors can be accumulated.

The RHPP monitors the path signal label byte (C2) payload to validate change in the accepted path signal label (APSL). The same PSL byte must be received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register) before being considered accepted.

The RHPP also monitors the path signal label byte (C2) to detect path payload label unstable (PLU-P) defect. A PSL unstable counter is increment every time the received PSL differs from the previously received PSL (an erroneous PSL will cause the counter to be increment twice, once when the erroneous PSL is received and once when the error free PSL is received). The PSL unstable counter is reset when the same PSL value is received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). PLU-P is declared when the PSL unstable counter reaches five. PLU-P is removed when the PSL unstable counter is reset.

The RHPP also monitors the path signal label byte (C2) to detect path payload label mismatch (PLM-P) defect. PLM-P is declared when the accepted PSL does not match the expected PSL according to Table 4. PLM-P is removed when the accepted PSL match the expected PSL according to Table 4. The accepted PSL is the same PSL value received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). The expected PSL is a programmable PSL value.

The RHPP also monitors the path signal label byte (C2) to detect path unequipped (UNEQ-P) defect. UNEQ-P is declared when the accepted PSL is 00H and the expected PSL is not 00H. UNEQ-P is removed when the accepted PSL is not 00H or when the accepted PSL is 00H and the expected PSL is 00H. The accepted PSL is the same PSL value received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). The expected PSL is a register programmable PSL value.

The RHPP also monitors the path signal label byte (C2) to detect path payload defect indication (PDI-P) defect. PDI-P is declared when the accepted PSL is a PDI defect that matches the expected PDI defect. PPDI is removed when the accepted PSL is not a PDI defect or when the accepted PSL is a PDI defect that does not match the expected PDI defect. The accepted PSL is the same PSL value received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). Table 5 gives the expected PDI defect based on the programmable PDI and PDI range register values.

Table 4 PLM-P, UNEQ-P and PDI-P Defects Declaration

Expected PSL		Accepted PSL			PLM-P	UNEQ-P	PDI-P
00	Unequipped	00	Unequipped		Match	Inactive	Inactive
		01	Equipped non specific		Mismatch	Inactive	Inactive
		02-E0 FD-FF	Equipped specific		Mismatch	Inactive	Inactive
		E1-FC	PDI	$=_{exp}$PDI	Mismatch	Inactive	Active
				$!=_{exp}$PDI	Mismatch	Inactive	Inactive
01	Equipped non specific	00	Unequipped		Mismatch	Active	Inactive
		01	Equipped non specific		Match	Inactive	Inactive
		02-E0 FD-FF	Equipped specific		Match	Inactive	Inactive
		E1-FC	PDI	$=_{exp}$PDI	Match	Inactive	Active
				$!=_{exp}$PDI	Mismatch	Inactive	Inactive
02-FF	Equipped specific PDI	00	Unequipped		Mismatch	Active	Inactive
		01	Equipped non specific		Match	Inactive	Inactive
		02-E0 FD-FF	Equipped specific	$=_{exp}$PSL	Match	Inactive	Inactive
				$!=_{exp}$PSL	Mismatch	Inactive	Inactive
		E1-FC	PDI	$=_{exp}$PDI	Match	Inactive	Active
				$!=_{exp}$PDI	Mismatch	Inactive	Inactive

Table 5 Expected PDI Defect Based on PDI and PDI Range Values

PDI register value	DPI range register value	Expected PDI	PDI register value	DPI range register value	Expected PDI
00000	Disable	None	01111	Disable	EF
	Enable			Enable	E1-EF
00001	Disable	E1	10000	Disable	F0
	Enable	E1-E1		Enable	E1-F0
00010	Disable	E2	10001	Disable	F1
	Enable	E1-E2		Enable	E1-F1
00011	Disable	E3	10010	Disable	F2
	Enable	E1-E3		Enable	E1-F2
00100	Disable	E4	10011	Disable	F3
	Enable	E1-E4		Enable	E1-F3
00101	Disable	E5	10100	Disable	F4
	Enable	E1-E5		Enable	E1-F4
00110	Disable	E6	10101	Disable	F5
	Enable	E1-E6		Enable	E1-F5
00111	Disable	E7	10110	Disable	F6
	Enable	E1-E7		Enable	E1-F6
01000	Disable	E8	10111	Disable	F7
	Enable	E1-E8		Enable	E1-F7
01001	Disable	E9	11000	Disable	F8
	Enable	E1-E9		Enable	E1-F8
01010	Disable	EA	11001	Disable	F9
	Enable	E1-EA		Enable	E1-F9
01011	Disable	EB	11010	Disable	FA
	Enable	E1-EB		Enable	E1-FA
01100	Disable	EC	11011	Disable	FB
	Enable	E1-EC		Enable	E1-FB
01101	Disable	ED	11100	Disable	FC
	Enable	E1-ED		Enable	E1-FC
01110	Disable	EE			
	Enable	E1-EE			

The RHPP monitors bits 5, 6, and 7 of the path status byte (G1) to detect to detect path remote defect indication (RDI-P) and path enhanced remote defect indication (ERDI-P) defects.

RDI-P is declared when bit 5 of the G1 byte is set high for five or ten consecutive frames (selectable by the RDI-P10 bit in the configuration register). RDI-P is removed when bit 5 of the G1 byte is set low for five or ten consecutive frames. ERDI-P is declared when the same 010, 100, 101, 110, or 111 pattern is detected in bits 5, 6, and 7 of the G1 byte for five or ten consecutive frames (selectable by the RDI-P10 bit in the configuration register). ERDI-P is removed when the same 000, 001, or 011 pattern is detected in bits 5, 6, and 7 of the G1 byte for five or ten consecutive frames.

The RHPP extracts and serially outputs all the path overhead (POH) bytes on the time multiplexed RPOH port. The POH bytes are output in the same order that they are received (J1, B3, C2, G1, F2, H4, Z3, Z4, and N1). RPOHCLK is the generated output clock used to provide timing for the RPOH port. RPOHCLK is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. Sampling RPOHFP high with the rising edge of RPOHCLK identifies the MSB of the first J1 byte.

7.6 SONET/SDH Bit Error Rate Monitor (SBER)

The SBER block provides two independent bit error rate-monitoring circuits (BERM block). The SBER block is used to monitor the Multiplexer Section BIP (B2) with one BERM block dedicated to monitor the Signal Degrade (SD) alarm and the other BERM block dedicated to monitor the Signal Fail (SF) alarm. These alarms can then be used to control system level features such as Automatic Protection Switching (APS).

The BERM block utilizes a sliding window based algorithm.

7.7 SONET/SDH Alarm Reporting Controller (SARC)

The SARC block receives all the section, line, and path defects detected by the receive overhead processors and, according to user specific configuration, generates consequent action indications.

- Receive section alarm (SALM) indication: SALM is asserted when an OOF, LOF, LOS, AIS-L, RDI-L, APSBF, TIU-S, TIM-S, SDBER, or SFBER defect is detected in the receive data stream. Configuration registers allow the user to remove any defect from the previous enumeration.
- Receive path alarm (RALM) indication: RALM is asserted when a SALM, AIS-P, LOP-P, PLU-P. PLM-P, UNEQ-P, PDI-P, RDI-P, ERDI-P, TIU-P, or TIM-P defect is detected in the receive data stream. Configuration registers allow the user to remove any defect from the previous enumeration.

The SARC block also sources and terminates the Ring Control Port to allow alarm information to be exchanged with a partner ARROW 155. See the functional timing description for more details on the Ring Control Port (Sections 8.13 and 8.14).

7.8 SONET/SDH Virtual Container Aligner (SVCA)

The SONET/SDH Virtual Container Aligner (SVCA) block aligns the payload data from an incoming SONET/SDH data stream to a new transport frame reference. The alignment is accomplished by recalculating the STS (AU) payload pointer value based on the offset between the transport overhead of the incoming data stream and that of the outgoing data stream.

Frequency offsets (e.g., due to plesiosynchronous network boundaries, or the loss of a primary reference timing source) and phase differences (due to normal network operation) between the incoming data stream and the outgoing data stream are accommodated by pointer adjustments in the outgoing data stream.

7.8.1 TU3 Termination

The SVCA terminates TU3 paths in the receive direction by mapping the TU3 into an AU-3 (STS-1) path for the Drop bus and the Transmit Slice. On the transmit side, the SVCA can be configured to map incoming AU-3 (STS-1) paths from the Add bus or the Receive Slice into a TU-3 path for the SONET processors downstream.

7.8.2 Elastic Store

The Elastic Store performs rate adaptation between the line side interface and the system side interface. The entire incoming payload, including path overhead bytes, is written into a first-in-first-out (FIFO) buffer at the incoming byte rate. Each FIFO word stores a payload data byte and a one-bit tag labeling the J1 byte. Incoming pointer justifications are accommodated by writing into the FIFO during the negative stuff opportunity byte or by not writing during the positive stuff opportunity byte. Data is read out of the FIFO in the Elastic Store block at the outgoing byte rate by the Pointer Generator. Analogously, outgoing pointer justifications are accommodated by reading from the FIFO during the negative stuff opportunity byte or by not reading during the positive stuff opportunity byte.

The FIFO read and write addresses are monitored. Pointer justification requests will be made to the Pointer Generator based on the proximity of the addresses relative to FIFO thresholds. The Pointer Generator schedules a pointer increment event if the FIFO depth is below the lower threshold and a pointer decrement event if the depth is above the upper threshold. FIFO underflow and overflow events are detected and path AIS is optionally inserted in the outgoing data stream for three frames to alert downstream elements of data corruption.

7.8.3 Pointer Generator

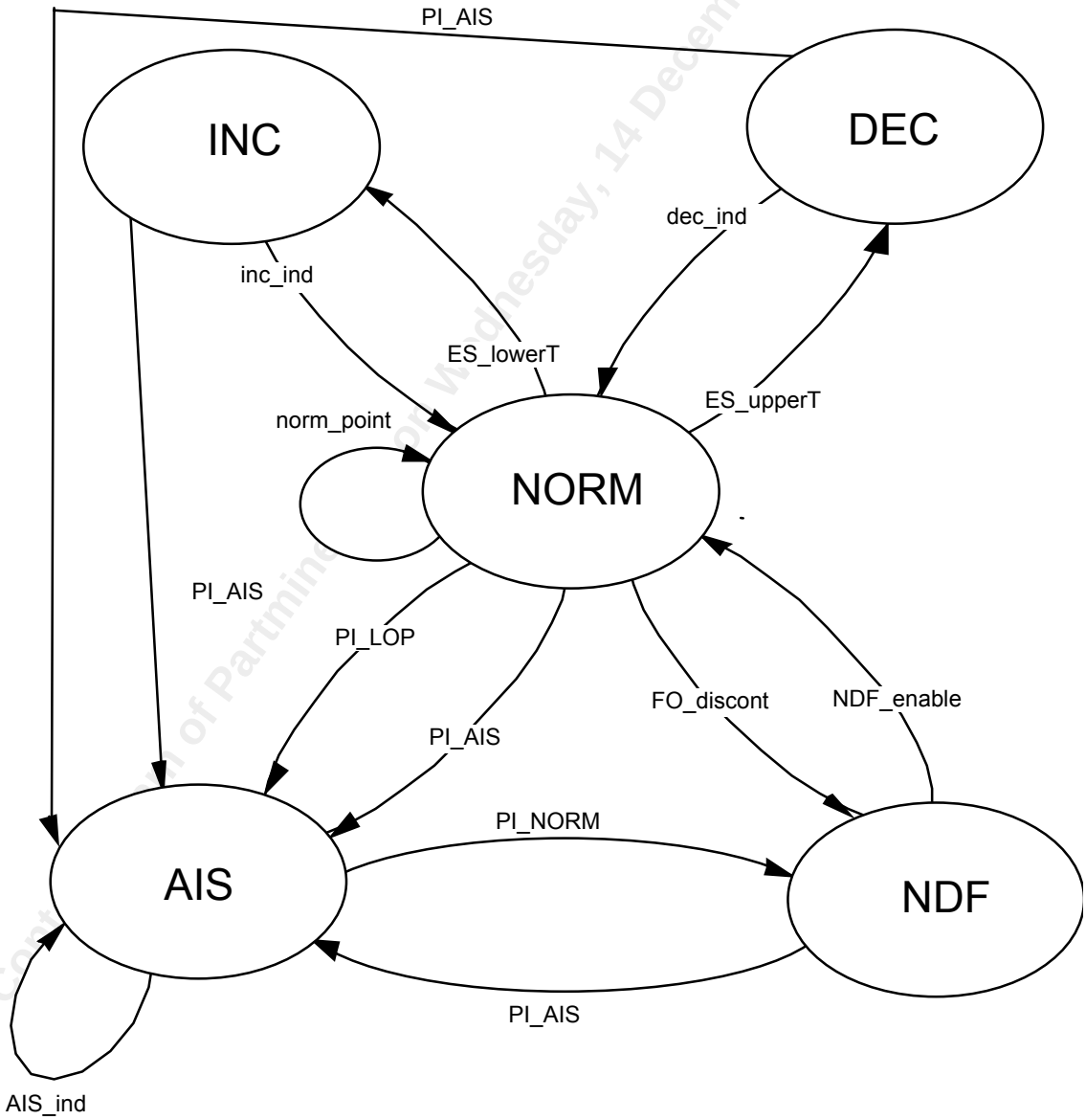
The Pointer Generator generates the H1 and H2 bytes in order to identify the location of the path overhead byte (J1) and all the synchronous payload envelop bytes (SPE) of the constituent STS-1/3c/12c/48c (VC3/4/4-4c/4-16c) payloads. The pointer generator is a time multiplexed finite state machine that can process any mixed of STS-1/3c/12c/48c (AU3/4/4-4c/4-16c) pointers. Within the pointer generator algorithm, five states are defined as shown below:

- NORM_state (NORM)
- AIS_state (AIS)

- NDF_state (NDF)
- INC_state (INC)
- DEC_state (DEC)

The transition from the NORM to the INC, DEC, and NDF states are initiated by events in the Elastic Store (ES) block. The transition to/from the AIS state are controlled by the pointer interpreter (PI) in the Receive High Order Path Processor block. The transitions from INC, DEC, and NDF states to the NORM state occur autonomously with the generation of special pointer patterns.

Figure 12 Pointer Generation State Diagram



The following events, indicated in the state diagram, are defined:

ES_lowerT: ES filling is below the lower threshold + previous inc_ind, dec_ind or NDF_enable more than three frames ago.

ES_upperT: ES filling is above the upper threshold + previous inc_ind, dec_ind or NDF_enable more than three frames ago.

FO_discont: frame offset discontinuity

PI_AIS: PI in AIS state

PI_LOP: PI in LOP state

PI_NORM: PI in NORM state

Note

1. A frame offset discontinuity occurs if an incoming NDF enabled is received, or if an ES overflow/underflow occurred.

The autonomous transitions indicated in the state diagram are defined as follows:

inc_ind: transmit the pointer with NDF disabled and inverted I bits, transmit a stuff byte in the byte after H3, increment active offset.

dec_ind: transmit the pointer with NDF disabled and inverted D bits, transmit a data byte in the H3 byte, decrement active offset.

NDF_enable: accept new offset as active offset, transmit the pointer with NDF enabled and new offset.

norm_point: transmit the pointer with NDF disabled and active offset.

AIS_ind: active offset is undefined, transmit an all-1's pointer and payload.

Note 1 active offset is defined as the phase of the SPE (VC).

Note 2 the SS bits are undefined in SONET, and has bit pattern 10 in SDH

Note 3 enabled NDF is defined as the bit pattern 1001.

Note 4 disabled NDF is defined as the bit pattern 0110.

7.9 SONET Time Slot Interchange (STSI)

The STSI allows arbitrary timeslot re-ordering in both the Add and Drop directions, as well as allowing DS3/E3/STS-1E paths, unequipped paths, or loopback paths to be switched into the main SONET data path. In SONET/SDH-only applications, the STSI can operate in bypass mode, where data flows directly from the SONET/SDH Overhead processor blocks to the Drop TelecomBus in the receive direction, and from the Add TelecomBus to the SONET/SDH Overhead processor blocks in the transmit direction. In DS3/E3/STS-1E Mapping mode, a different bypass is invoked, where data flows directly from the DS3/E3/STS-1E slice to the Drop TelecomBus in the receive direction, and from the Add TelecomBus to the DS3/E3/STS-1E slice in the Transmit direction. Alternatively, the output timeslots of the STSI can be configured to source data from any one of the input timeslots of the connected interfaces.

7.10 Drop TelecomBus Interface

The Drop TelecomBus Interface maps SONET/SDH payloads on the output STS-12/STM-4 bus. Markers for J0/J1 byte locations are given to signal the frame alignment. Payload and non-payload bytes are also marked appropriately. Alarm conditions can also be indicated on the interface. The interface is clocked with the 77.76 MHz SYSCLK. The output J0/J1 byte alignment on the parallel TelecomBus is aligned to the input J0REF signal (delayed by the DJ0DLY[13:0] bits). The outgoing clock LINECLK_REF may be used to clock the Drop TelecomBus Interface such that the line side (Recovered clock) and Drop TelecomBus interface (SYSCLK) are synchronized.

The Drop TelecomBus can also be tri-stated on a per-timeslot basis to allow multiplexing of multiple ARROW 155 devices on the same TelecomBus.

7.11 Add TelecomBus Interface

The input parallel TelecomBus Interface samples a SONET/SDH stream on the 8-bit STS-12/STM-4 bus. Markers for J0/J1 byte locations are given to indicate the frame alignment. Payload and non-payload bytes are also marked appropriately. AIS alarm conditions are also given on the interface. The interface is clocked with the 77.76 MHz SYSCLK. The outgoing clock LINECLK_REF may be used to clock the Add TelecomBus Interface such that the line side (locked to REFCLK_P/N) and TelecomBus interface are synchronized.

7.12 DS3/E3 Desynchronizer (D3E3MD)

The D3E3MD block extracts DS3 or E3 data from an STS-1 / AU3 SPE and outputs a nominal rate DS3 or E3 clock and serial data stream.

The D3E3MD is capable of demapping DS3 / E3 payloads from SONET SPEs mapped as AU3s (any TU3 paths have already been translated to AU3 paths by the SVCA). Thus, two possible demapping modes of operation are possible: (1) AU3 -> DS3, and (2) AU3 -> E3.

The locations of specific payload bytes within the incoming STS-1 frame, as well as negative and positive pointer justifications, are calculated. Positive and negative SPE pointer justification events are registered as interrupts which are visible as normal mode register bits.

The D3E3MD decomposes the incoming STS-1 data stream into a VC3 structure. The VC3 is demapped from the STS-1 payload by removing 2 fixed stuff columns. In DS3 or E3 mode, the D3E3MD demaps the incoming DS3 or E3 payload from a VC-3. The format of the incoming DS3/E3 over VC-3 mapping is shown in Figure 16.

When SONET defects are detected or the AISGEN normal mode register bit is set high, the extracted DS3 / E3 payload is overwritten by an Alarm Indication Signal (AIS) and the outgoing clock is held constant at 44.736 MHz in DS3 mode and 34.368 MHz in E3 mode.

7.12.1 FIFO

DS3/E3 Data bits extracted from the STS-1 SPE are assembled into bytes and written into a 54-byte FIFO. The depth of the FIFO has been chosen to account for the DPLL loop bandwidth, worst-case maximum consecutive pointer justifications in the same direction, ppm offsets between the read and write clocks, and payload gaps. In addition, with a 1 Hz loop bandwidth, the D3E3MD can also tolerate periodic pointer justifications in the same direction that are spaced 7.5 ms apart, as per the GR-253 2000 DS3 specifications.

The FIFO is used to monitor the phase error and aids in regulating the outgoing clock frequency. When an overflow or an underflow occur, the FIFO control block generates interrupt signals (FOVRI and FUDRI, respectively). A register bit is provided so that the FIFO may be reset by software (FIFORST).

7.12.2 Digital PLL

A Digital Phase Locked Loop (DPLL) is used to generate the output DS3/E3 clock. The DPLL consists of a phase detector, a phase modulator, and a clock generator. The default loop bandwidth of the DPLL has been selected to be approximately 1 Hz. A register bit (LOOPBW) exists which increases the loop bandwidth of the DPLL to approximately 64 Hz, if faster lock is required, at the expense of increased jitter. A second register bit LOOPBW2 reduces the default loop bandwidth from 1 Hz to 0.6 Hz, if greater jitter attenuation than that of the default loop bandwidth is desired. The PLLRST normal mode register bit provides an asynchronous reset for the DPLL circuits, if it is desired to reset the PLL without resetting the other logic in the D3E3MD.

7.12.3 Transfer Function

Jitter transfer is defined as the ratio of jitter on the output signal (serial DS3/E3) to the jitter applied to the input signal (DS3/E3 mapped into SONET). Requirements for jitter transfer are given in terms of a jitter transfer mask, which represents the maximum acceptable jitter gain (in dB) for a specified range of jitter frequencies.

The D3E3MD default jitter transfer function reflects that of a 1st order low-pass filter with corner frequency located at 0.2 Hz.

The system (including the D3E3MD) intrinsic jitter, pointer jitter, jitter tolerance, mapping wander, and pointer wander characteristics are described in Section 13.8.

Note that the clock PDH Reference clock on the PDHREFCLK[1:0] pins must be jitter and wander free, as any jitter or wander presented on those clock inputs will directly map to jitter and wander on the transmit data stream.

7.13 DS3/E3/STS-1E Jitter Attenuator (JAT)

The JAT receives serial data and clock from an external source, measures the phase difference between the DS3/E3/STS-1E reference clock and the external received clock implementing a digital PLL that performs the jitter attenuating function.

7.13.1 Digital PLL

The digital PLL is composed of three sections: delay line, phase detector, and control state machine.

To initialize the JAT, it takes a maximum 192 DS3/E3/STS-1E reference clock (one of PDHREFCLK[1:0]) cycles. When the initialization is complete, the state machine will set the RUN signal high indicating the outgoing data stream is reasonably stable.

This PLL performs the jitter attenuation of the incoming phase with a bandwidth set by the normal mode registers. The PLL supports a glitchless software reset function. Maximum reset time is 384 (one of PDHREFCLK[1:0]) cycles.

7.13.2 FIFO

The FIFO acts as an elastic storage element, which receives data at a rate determined by the incoming clock and transmits this data at a rate determined by the outgoing clock. The FIFO is comprised of two banks of 128 registers, a write and read address pointer, overflow and underflow monitors, and optional centering circuitry.

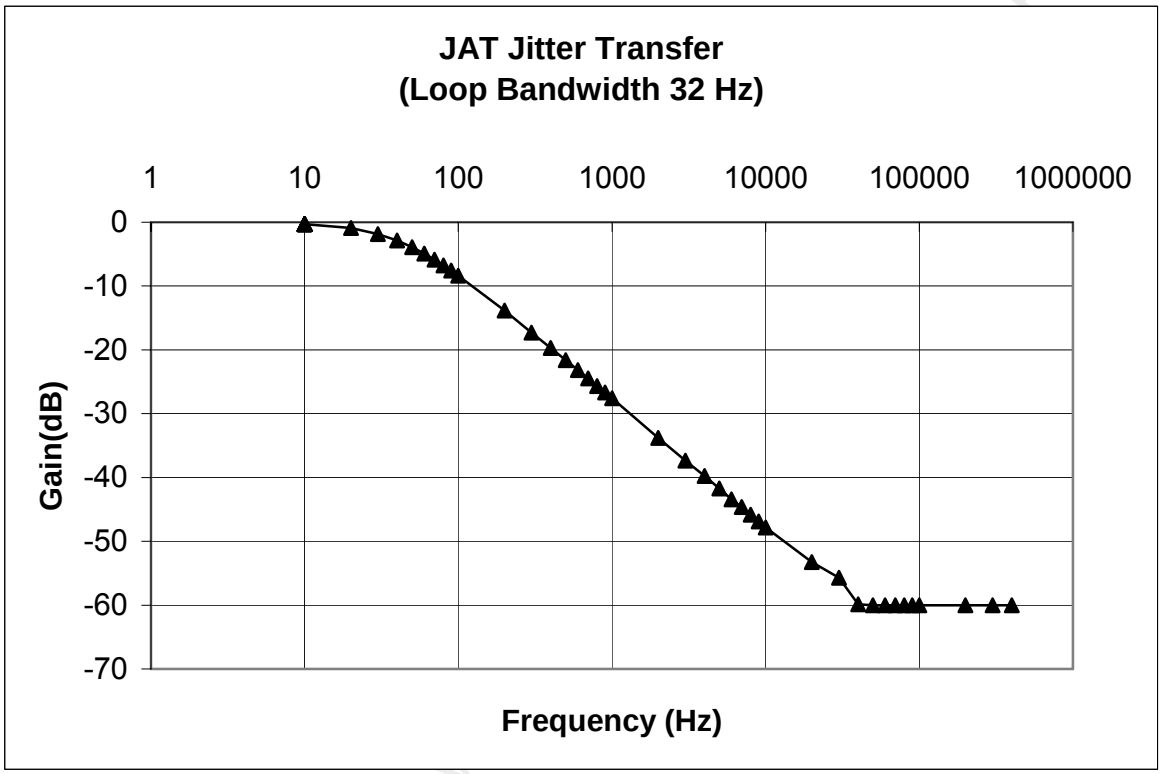
When the internal PLL is providing the outgoing clock, the FIFO can be used as an elastic store to bridge between data burst and smooth data environments. The FIFO has a self-centering circuit, which sets up the read pointer operating range to be at least 8 UI away from the end of the 128-bit registers.

When an attempt is made to read data from the FIFO when the FIFO is already empty, the UNDRI register will be set. Similarly, when an attempt is made to write data to the FIFO when the FIFO is already full, the OVERI register will be set.

7.13.3 Transfer Function

Jitter transfer is defined as the ratio of jitter on the output signal to the jitter applied to the input signal. A typical transfer function of the JAT is depicted in Figure 13. Note that the JAT loop bandwidth selected is 32 Hz and the tester equipment used to measure the jitter transfer does not go beyond –60 dB.

Figure 13 Typical JAT Jitter Transfer Function



The system (including the TJAT and RJAT) intrinsic jitter, pointer jitter, jitter tolerance, mapping wander, and pointer wander characteristics are described in Section 13.8.

The JAT may be configured to generate interrupts on error events or status changes. All sources of interrupts can be masked or acknowledged via internal registers. Internal registers are also used to configure the JAT. Access to these registers is via a generic microprocessor bus.

7.14 DS3 Framer

The DS3 Framer (T3-FRMR) Block integrates circuitry required for decoding a B3ZS-encoded signal and framing to the resulting DS3 bit stream. The T3-FRMR is directly compatible with the M23 and C-bit parity DS3 applications.

The T3-FRMR decodes a B3ZS-encoded signal and provides indications of line code violations. The B3ZS decoding algorithm and the LCV definition can be independently chosen through software. A loss of signal (LOS) defect is also detected for B3ZS encoded streams. LOS is declared when inputs RPOS and RNEG contain zeros for 175 consecutive RCLK cycles. LOS is removed when the ones density on RPOS and/or RNEG is greater than 33% for 175 ±1 RCLK cycles.

The framing algorithm examines five F-bit candidates simultaneously. When at least one discrepancy has occurred in each candidate, the algorithm examines the next set of five candidates. When a single F-bit candidate remains in a set, the first bit in the supposed M-subframe is examined for the M-frame alignment signal (i.e., the M-bits, M1, M2, and M3 are following the 010 pattern). Framing is declared, and out-of-frame is removed, if the M-bits are correct for three consecutive M-frames while no discrepancies have occurred in the F-bits. During the examination of the M-bits, the X-bits and P-bits are ignored. The algorithm gives a maximum average reframe time of 1.5 ms.

While the T3-FRMR is synchronized to the DS3 M-frame, the F-bit and M-bit positions in the DS3 stream are examined. An out-of-frame defect is detected when 3 F-bit errors out of 8 or 16 consecutive F-bits are observed (as selected by the M3O8 bit in the DS3 FRMR Configuration Register), or when one or more M-bit errors are detected in 3 out of 4 consecutive M-frames. The M-bit error criteria for OOF can be disabled by the MBDIS bit in the DS3 FRMR Configuration register. In the presence of a high bit error rate, the 3 out of 8 consecutive F-bits out-of-frame ratio provides more robust operation than the 3 out of 16 consecutive F-bits ratio. Either out-of-frame criteria allows an out-of-frame defect to be detected quickly when the M-subframe alignment patterns are lost, or optionally, when the M-frame alignment pattern is lost.

Also, line code violations, M-bit or F-bit framing bit errors, and P-bit parity errors are indicated while in frame. When C-bit parity mode is enabled, both C-bit parity errors and far end block errors are indicated. These error indications, as well as the line code violation and excessive zeros indication, are accumulated over 1 second intervals with the Performance Monitor (PMON). Note that the framer is an off-line framer, indicating both OOF and COFA events. Even if an OOF is indicated, the framer will continue indicating performance monitoring information based on the previous frame alignment.

Three DS3 maintenance signals (a RED alarm condition, the alarm indication signal, and the idle signal) are detected by the T3-FRMR. The maintenance detection algorithm employs a simple integrator with a 1:1 slope that is based on the occurrence of "valid" M-frame intervals. For the RED alarm, an M-frame is said to be a "valid" interval if it contains a RED defect, defined as an occurrence of an OOF or LOS event during that M-frame. For AIS and IDLE, an M-frame interval is "valid" if it contains AIS or IDLE, defined as the occurrence of less than 15 discrepancies in the expected signal pattern (1010... for AIS, 1100... for IDLE) while valid frame alignment is maintained. This discrepancy threshold ensures the detection algorithms operate in the presence of a 10^{-3} bit error rate.

For AIS, the expected pattern may be selected to be:

1. The framed "1010" signal; the framed arbitrary DS3 signal and the C-bits all zero;

2. The framed "1010" signal and the C-bits all zero; the framed all-ones signal (with overhead bits ignored);

3. Or the unframed all-ones signal (with overhead bits equal to ones).

Each "valid" M-frame causes an associated integration counter to increment; "invalid" M-frames cause a decrement. With the "slow" detection option, RED, AIS, or IDLE are declared when the respective counter saturates at 127, which results in a detection time of 13.5 ms. With the "fast" detection option, RED, AIS, or IDLE are declared when the respective counter saturates at 21, which results in a detection time of 2.23 ms (i.e., 1.5 times the maximum average reframe time). RED, AIS, or IDLE are removed when the respective counter decrements to 0. DS3 Loss of Frame detection is provided as recommended by ITU-T G.783 with programmable integration periods of 1 ms, 2 ms, or 3 ms. While integrating up to assert LOF, the counter will integrate up when the framer asserts an Out of Frame condition and integrates down when the framer de-asserts the Out of Frame condition. Once an LOF is asserted, the framer must not assert OOF for the entire integration period before LOF is de-asserted.

Valid X-bits are extracted by the T3-FRMR to provide indication of far end receive failure (FERF). A FERF defect is detected if the extracted X-bits are equal and are logic 0 (X1=X2=0); the defect is removed if the extracted X-bits are equal and are logic 1 (X1=X2=1). If the X-bits are not equal, the FERF status remains in its previous state. The extracted FERF status is buffered for 2 M-frames before being reported within the DS3 FRMR Status register. This buffer ensures a better than 99.99% chance of freezing the FERF status on a correct value during the occurrence of an out of frame.

When the C-bit parity application is enabled, both the far end alarm and control (FEAC) channel and the path maintenance data link are extracted. Codes in the FEAC channel are detected by the Bit Oriented Code Detector (RBOC). HDLC messages in the Path Maintenance Data Link are received by the Data Link Receiver (RDLC).

The T3-FRMR can be enabled to automatically assert the RAI indication in the outgoing transmit stream upon detection of any combination of LOS, OOF or RED, or AIS. The T3-FRMR can also be enabled to automatically insert C-bit Parity FEBE upon detection of receive C-bit parity error.

The T3-FRMR extracts the entire DS3 overhead (56 bits per M-frame) using the ROH output, along with the OHCLK, and ROHFA outputs.

The T3-FRMR may be configured to generate interrupts on error events or status changes. All sources of interrupts can be masked or acknowledged via internal registers. Internal registers are also used to configure the T3-FRMR. Access to these registers is via a generic microprocessor bus.

7.15 E3 Framer

The E3 Framer (E3-FRMR) Block integrates circuitry required for decoding an HDB3-encoded signal and framing to the resulting E3 bit stream. The E3-FRMR is directly compatible with the G.751 and G.832 E3 applications.

The E3-FRMR searches for frame alignment in the incoming serial stream based on either the G.751 or G.832 formats. For the G.751 format, the E3-FRMR expects to see the selected framing pattern error-free for three consecutive frames before declaring INFRAME. For the G.832 format, the E3-FRMR expects to see the selected framing pattern error-free for two consecutive frames before declaring INFRAME. Once the frame alignment is established, the incoming data is continuously monitored for framing bit errors and byte interleaved parity errors (in G.832 format).

While in-frame, the E3-FRMR also extracts various overhead bytes and processes them according to the framing format selected.

7.15.1 In G.832 E3 Format, the E3-FRMR Extracts:

1. The Trail Trace bytes and outputs them as a serial stream for further processing by the Trail Trace Buffer (TTB) block.

2. The FERF bit and indicates an alarm when the FERF bit is a logic 1 for 3 or 5 consecutive frames. The FERF indication is removed when the FERF bit is a logic 0 for 3 or 5 consecutive frames.

3. The FEBE bit and outputs it for accumulation in PMON.

4. The Payload Type bits and buffers them so that they can be read by the microprocessor.

5. The Timing Marker bit and asserts the Timing Marker indication when the value of the extracted bit has been in the same state for 3 or 5 consecutive frames.

6. The Network Operator byte and presents it as a serial stream for further processing by the RDLC block when the RNETOP bit in the Channel Data Link and FERF/RAI Control register is logic 1. The byte is also brought out on the ROH output with the associated OHCH[1:0] using the overhead clock, OHCLK. All 8 bits of the Network Operator byte are extracted and presented on the overhead output and, optionally, presented to the RDLC.

7. The General Purpose Communication Channel byte and presents it to the RDLC when the RNETOP bit in the ARROW 155 Data Link and FERF Control register is logic 0. The byte is also brought out on the ROH output with the associated OHCH[1:0] using the overhead clock, OHCLK.

7.15.2 In G.751 E3 Mode, the E3-FRMR Extracts:

1. The Remote Alarm Indication bit (bit 11 of the frame) and indicates a Remote Alarm when the RAI bit is a logic 1 for 3 or 5 consecutive frames. Similarly, the Remote Alarm is removed when the RAI bit is logic 0 for 3 or 5 consecutive frames.

2. The National Use reserved bit (bit 12 of the frame) and presents it as a serial stream for further processing in the RDLC when the RNETOP bit in the Channel Data Link and FERF/RAI Control register is logic 0. The bit is also brought out on the ROH output with the associated OHCH[1:0] using the overhead clock, OHCLK. Optionally, an interrupt can be generated when the National Use bit changes state.

Further, while in-frame, the E3-FRMR indicates the position of all the overhead bits in the incoming digital stream to the ATMF/SPLR block. For G.751 mode, the tributary justification bits can optionally be identified as either overhead or payload for payload mappings that take advantage of the full bandwidth.

The E3-FRMR declares out of frame alignment if the framing pattern is in error for four consecutive frames. The E3-FRMR is an "off-line" framer, where all frame alignment indications, all overhead bit indications, and all overhead bit processing continue based on the previous alignment. Once the framer has determined the new frame alignment, the out-of-frame indication is removed and a COFA indication is declared if the new alignment differs from the previous alignment.

The E3-FRMR detects the presence of AIS in the incoming data stream when less than 8 zeros in a frame are detected while the framer is OOF in G.832 mode, or when less than 5 zeros in a frame are detected while OOF in G.751 mode. This algorithm provides a probability of detecting AIS in the presence of a 10^{-3} BER as 92.9% in G.832 and 98.0% in G.751.

Loss of signal is declared when no marks have been received for 32 consecutive bit periods. Loss of signal is de-asserted after 32 bit periods during which there is no sequence of four consecutive zeros.

E3 Loss of Frame detection is provided as recommended by ITU-T G.783 with programmable integration periods of 1 ms, 2 ms, or 3 ms. While integrating up to assert LOF, the counter will integrate up when the framer asserts an Out of Frame condition and integrates down when the framer de-asserts the Out of Frame condition. Once an LOF is asserted, the framer must not assert OOF for the entire integration period before LOF is de-asserted.

The E3-FRMR can also be enabled to automatically assert the RAI/FERF indication in the outgoing transmit stream upon detection of any combination of LOS, OOF, or AIS. The E3-FRMR can also be enabled to automatically insert G.832 FEBE upon detection of receive BIP-8 errors.

7.16 STS-1E Receive Section Overhead Processor (RSOP)

The STS-1E Receive Section Overhead Processor (RSOP) provides frame synchronization, descrambling, section level alarm and performance monitoring. In addition, it may extract the section data communication channel from the section overhead and provide it through the RDLC.

7.16.1 Framer

The Framer Block determines the in-frame/out-of-frame status of the receive stream. While in-frame, the framing bytes (A1, A2) in each frame are compared against the expected pattern. Out-of-frame is declared when four consecutive frames containing one or more framing pattern errors have been received.

While out of frame, the SIPO block monitors the bit-serial STS-1E data stream for an occurrence of the framing pattern (A1, A2). The SIPO informs the RSOP Framer block when an A1 byte followed by an A2 byte has been detected to reinitializes the frame byte counter to the new alignment. The Framer block declares frame alignment on the next SONET/SDH frame when the A1 and A2 bytes are seen error-free. If the frame alignment has not changed from prior going out of frame, the Framer block could declare frame alignment on the first occurrence of error free A1 and A2 bytes.

Once in frame, the Framer block monitors the framing pattern sequence and declares out of frame (OOF) when one or more bits errors in each framing pattern are detected for four consecutive frames. Again, all framing bytes are examined for bit errors each frame.

7.16.2 Descramble

The Descramble Block utilizes a frame synchronous descrambler to process the receive stream. The generating polynomial is $x^7 + x^6 + 1$ and the sequence length is 127. Details of the descrambling operation are provided in the references. Note that the framing bytes (A1 and A2) and the trace/growth bytes (J0/Z0) are not descrambled. A register bit is provided to disable the descrambling operation.

7.16.3 Data Link Extract

The Data Link Extract Block extracts the section data communication channel (bytes D1, D2, and D3) from the STS-1 stream. The extracted bytes are output through the RDLC-STS-1E block.

7.16.4 Error Monitor

The Error Monitor Block calculates the received section BIP-8 error detection code (B1) based on the scrambled data of the complete STS-1 frame. The section BIP-8 code is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 code is compared with the BIP-8 code extracted from the B1 byte of the following frame. Differences indicate that a section level bit error has occurred. Up to 64000 (8 x 8000) bit errors can be detected per second. The Error Monitor Block accumulates these section level bit errors in a 16-bit saturating counter that can be read via the microprocessor interface. Circuitry is provided to latch this counter so that its value can be read while simultaneously resetting the internal counter to 0 or 1, if appropriate, so that a new period of accumulation can begin without loss of any events. It is intended that this counter be polled at least once per second so as not to miss bit error events.

7.16.5 Loss of Signal

The Loss of Signal Block monitors the scrambled data of the receive stream for the absence of 1's or 0’s. When 20 ± 3 µs of all zeros patterns or all ones patterns are detected, a loss of signal (LOS) is declared. Loss of signal is cleared when two valid framing words are detected and during the intervening time, no loss of signal condition is detected. The LOS signal is optionally reported on the FRMSTAT[x] bit when enabled by the LOSB Receive Alarm Control Register bit.

7.16.6 Loss of Frame

The Loss of Frame Block monitors the in-frame / out-of-frame status of the Framer Block. A loss of frame (LOF) is declared when an out-of-frame (OOF) condition persists for 3 ms. The LOF is cleared when an in-frame condition persists for a period of 3 ms. To provide for intermittent out-of-frame (or in-frame) conditions, the 3 ms timer is not reset to zero until an in-frame (or out-of-frame) condition persists for 3 ms. The LOF and OOF signals are optionally reported on the FRMSTAT[x] bit when enabled by the LOFB and OOFB Receive Alarm Control Register bits.

7.17 STS-1E Receive Line Overhead Processor (RLOP)

The STS-1E Receive Line Overhead Processor (RLOP) provides line level alarm and performance monitoring. In addition, it may extract the line data communication channel from the line overhead and provide it through the RDLC (STS-1E).

7.17.1 Line RDI Detect

The Line RDI Detect Block detects the presence of Line Remote Defect Indication (RDI-L) in the receive stream. Line RDI is declared when a 110 binary pattern is detected in bits 6, 7, and 8 of the K2 byte, for three or five consecutive frames. Line RDI is removed when any pattern other than 110 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. The RDI-L signal is optionally reported on the FRMSTAT[x] bit when enabled by the (LRDIEN) Receive Alarm Control Register bit.

7.17.2 Line AIS Detect

The Line AIS Block detects the presence of a Line Alarm Indication Signal (AIS-L) in the receive stream. Line AIS is declared when a 111 binary pattern is detected in bits 6, 7, and 8 of the K2 byte, for three or five consecutive frames. Line AIS is removed when any pattern other than 111 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. The AIS-L signal is optionally reported on the FRMSTAT[x] bit when enabled by the LAISEN Receive Alarm Control Register bit.

7.17.3 Data Link Extract Block

The Data Link Extract Block extracts the line data communication channel (bytes D4 to D12) from the STS-11 stream. The extracted bytes are available through the RDLC (STS-1E).

7.17.4 Error Monitor Block

The Error Monitor Block calculates the received line BIP-8 error detection codes based on the Line Overhead bytes and synchronous payload envelopes of the STS-1 stream. The line BIP-8 code is a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP-8 codes are compared with the BIP-8 codes extracted from the following frame. Any differences indicate that a line layer bit error has occurred. Optionally the RLOP can be configured to count a maximum of only one BIP error per frame.

This block also extracts the line remote error indication (REI-L) code from the M1 byte. The REI-L code is contained in bits 2 to 8 of the M1 byte, and represents the number of line BIP-8 errors that were detected in the last frame by the far end. The REI-L code value has 9 legal values (0 to 8) for an STS-1 stream. Illegal values are interpreted as zero errors.

The Error Monitor Block accumulates B2 error events and REI-L events in two 20-bit saturating counters that can be read via the Microprocessor Interface. The contents of these counters may be transferred to internal holding registers by writing to any one of the counter addresses, or by using the TIP register bit feature. During a transfer, the counter value is latched and the counter is reset to 0 (or 1, if there is an outstanding event). Note: These counters should be polled at least once per second to avoid saturation.

The B2 error event counters optionally can be configured to accumulate only "word" errors. A B2 word error is defined as the occurrence of one or more B2 bit error events during a frame. The B2 error counter is incremented by one for each frame in which a B2 word error occurs.

In addition, the REI-L events counters optionally can be configured to accumulate only "word" events. A REI-L word event is defined as the occurrence of one or more REI-L bit events during a frame. The REI-L event counter is incremented by one for each frame in which a REI-L event occurs. If the extracted REI-L value is in the range 1 to 4 the REI-L event counter will be incremented for each and every REI-L bit. If the extracted REI-L value is greater than 4, the REI-L event counter will be incremented by 4.

7.18 STS-1E Bit Error Monitor (RASE)

7.18.1 Bit Error Rate Monitor

The STS-1E Bit Error Monitor Block (BERM) calculates the received line BIP-24 error detection code (B2) based on the line overhead and synchronous payload envelope of the receive data stream. The line BIP-24 code is a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP code is compared with the BIP-24 code extracted from the B2 bytes of the following frame. Any differences indicate that a line layer bit error has occurred. Up to 64000 (8 BIP/frame x 8000 frames/second) for STS-1 rate.

The BERM accumulates these line layer bit errors in a 20-bit saturating counter that can be read via the microprocessor interface. During a read, the counter value is latched and the counter is reset to 0 (or 1, if there is an outstanding event). Note that this counter should be polled at least once per second to avoid saturation that in turn may result in missed bit error events.

The BERM block is able to simultaneously monitor for signal fail (SF) or signal degrade (SD) threshold crossing and provide alarms through software interrupts. The bit error rates associated with the SF or SD alarms are programmable over a range of 10^{-3} to 10^{-9}. Details are provided inthe Operations section.

7.18.2 Synchronization Status Extraction

The Synchronization Status Extraction (SSE) Block extracts the synchronization status (S1) byte from the line overhead. The SSE block can be configured to capture the S1 nibble after three or after eight frames with the same value (filtering turned on) or after any change in the value (filtering turned off). The S1 nibble can be read via the Microprocessor Interface.

7.19 STS-1E Receive Path Overhead Processor (RPOP)

The STS-1E Receive Path Overhead Processor (RPOP) provides pointer interpretation, extraction of path overhead, extraction of the synchronous payload envelope, and path level alarm indication and performance monitoring. This block may be bypassed for path transparency.

7.19.1 Pointer Interpreter

The Pointer Interpreter interprets the incoming pointer (H1, H2) as specified in the references. The pointer value is used to determine the location of the path overhead (the J1 byte) in the incoming STS-1 stream. The algorithm can be modeled by a finite state machine. Within the pointer interpretation algorithm three states are defined as shown below:

- NORM_state (NORM)
- AIS_state (AIS)
- LOP_state (LOP)

The transition between states will be consecutive events (indications), e.g., three consecutive AIS indications to go from the NORM_state to the AIS_state. The kind and number of consecutive indications activating a transition is chosen such that the behavior is stable and insensitive to low BER. The only transition on a single event is the one from the AIS_state to the NORM_state after receiving a NDF enabled with a valid pointer value. It should be noted that, since the algorithm only contains transitions based on consecutive indications, this implies that, for example, non-consecutively received invalid indications do not activate the transitions to the LOP_state.

Figure 14 Pointer Interpretation State Diagram

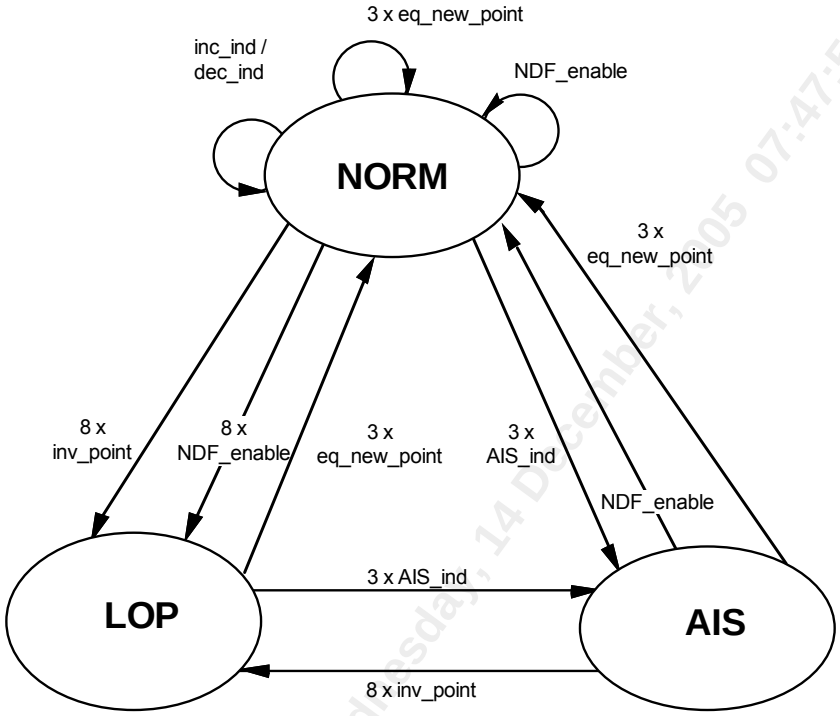


Table 6 defines the events (indications) shown in the state diagram.

Table 6 Pointer Interpreter Event (Indications) Description

Event (Indication)	Description
norm_point	disabled NDF + ss + offset value equal to active offset
NDF_enable	enabled NDF + ss + offset value in range of 0 to 782 or enabled NDF + ss, if NDFPOR bit is set (Note that the current pointer is not updated by an enabled NDF if the pointer is out of range).
AIS_ind	H1 = 'hFF, H2 = 'hFF
inc_ind	disabled NDF + ss + majority of I bits inverted + no majority of D bits inverted + previous NDF_enable, inc_ind or dec_ind more than 3 frames ago
dec_ind	disabled NDF + ss + majority of D bits inverted + no majority of I bits inverted + previous NDF_enable, inc_ind or dec_ind more than 3 frames ago
inv_point	not any of above (i.e., not norm_point, and not NDF_enable, and not AIS_ind, and not inc_ind and not dec_ind)
new_point	disabled_NDF + ss + offset value in range of 0 to 782 but not equal to active offset
inc_req	majority of I bits inverted + no majority of D bits inverted.
dec_req	majority of D bits inverted + no majority of I bits inverted.

Notes

1. The active offset is defined as the accepted current phase of the SPE (VC) in the NORM_state and is undefined in the other states.

2. Enabled NDF is defined as the following bit patterns: 1001, 0001, 1101, 1011, 1000.
3. Disabled NDF is defined as the following bit patterns: 0110, 1110, 0010, 0100, 0111.
4. The remaining six NDF codes (0000, 0011, 0101, 1010, 1100, 1111) result in an inv_ndf indication.
5. The ss bits are unspecified in SONET and has bit pattern 10 in SDH
6. The use of ss bits in definition of indications may be optionally disabled.
7. The requirement for previous NDF_enable, inc_ind or dec_ind be more than 3 frames ago may be optionally disabled.
8. The new_point is also an inv_point.
9. LOP is not declared if all the following conditions exist:
   - The received pointer is out of range (>782)
   - The received pointer is static
   - The received pointer can be interpreted, according to majority voting on the I and D bits, as a positive or negative justification indication, after making the requested justification, the received pointer continues to be interpretable as a pointer justification. When the received pointer returns to an in-range value, the S/UNI-4x155 will interpret it correctly.
10. LOP will exit at the third frame of a three frame sequence consisting of one frame with NDF enabled followed by two frames with NDF disabled, if all three pointers have the same legal value.

The transitions indicated in the state diagram are defined in Table 7.

Table 7 Pointer Interpreter Transition Description

Transition	Description
inc_ind/dec_ind	offset adjustment (increment or decrement indication)
3 x eq_new_point	three consecutive equal new_point indications
NDF_enable	single NDF_enable indication
3 x AIS_ind	three consecutive AIS indications
8 x inv_point	eight consecutive inv_point indications
8 x NDF_enable	eight consecutive NDF_enable indications

Notes

1. The transitions from NORM_state to NORM_state do not represent state changes but imply offset changes.
2. 3 x new_point takes precedence over other events and if the IINVCNT bit is set resets the inv_point count.
3. All three offset values received in 3 x eq_new_point must be identical.
4. "Consecutive event counters" are reset to zero on a change of state except for consecutive NDF count.

The Pointer Interpreter detects loss of pointer (LOP) in the incoming STS-3c/STM-1 stream. LOP is declared on entry to the LOP_state as a result of eight consecutive invalid pointers or eight consecutive NDF enabled indications. The alarm condition is reported in the receive alarm port and is optionally returned to the source node by signaling the corresponding Transmit Path Overhead Processor in the local device to insert a path RDI indication.

The Pointer Interpreter detects path AIS in the incoming STS-1 (STM-0/AU3). PAIS is declared on entry to the AIS_state after three consecutive AIS indications. The alarm condition reported in the receive alarm port and is optionally returned to the source node by signaling the corresponding Transmit Path Overhead Processor in the local SONET/SDH equipment to insert a path RDI indication.

Invalid pointer indications (inv_point), invalid NDF codes, new pointer indications (new_point), discontinuous change of pointer alignment, and illegal pointer changes are also detected and reported by the Pointer Interpreter block via register bits. An invalid NDF code is any NDF code that does not match the NDF enabled or NDF disabled definitions. The third occurrence of equal new_point indications (3 x eq_new_point) is reported as a discontinuous change of pointer alignment event (DISCOPA) instead of a new pointer event and the active offset is updated with the receive pointer value. An illegal pointer change is defined as an inc_ind or dec_ind indication that occurs within three frames of the previous inc_ind, dec_ind or NDF_enable indications. Illegal pointer changes may be optionally disabled via register bits.

The active offset value is used to extract the path overhead from the incoming stream and can be read from an internal register.

7.19.2 SPE Timing

The SPE Timing Block provides SPE timing information to the Error Monitor and the Extract blocks. The block contains a free running timeslot counter that is initialized by a J1 byte identifier (which identifies the first byte of the SPE). Control signals are provided to the Error Monitor and the Extract blocks to identify the Path Overhead bytes and to downstream circuitry to extract the SONET payload.

7.19.3 Error Monitor

The Error Monitor Block contains two 16-bit counters that are used to accumulate path BIP-8 errors (B3), and remote error indication (REI-P). The contents of the two counters may be transferred to holding registers, and the counters reset under microprocessor control.

Path BIP-8 errors are detected by comparing the path BIP-8 byte (B3) extracted from the current frame, to the path BIP-8 computed for the previous frame.

REI-Ps are detected by extracting the 4-bit REI-P field from the path status byte (G1). The legal range for the 4-bit field is between 0000 and 1000, representing zero to eight errors. Any other value is interpreted as zero errors.

Path RDI alarm is detected by extracting bit 5 of the path status byte. The RDI-P signal is set high when bit 5 is set high for five/ten consecutive frames. RDI-P is set low when bit 5 is low for five/ten consecutive frames. Auxiliary RDI alarm is detected by extracting bit 6 of the path status byte. The Auxiliary RDI alarm is indicated when bit 6 is set high for five/ten consecutive frames. The Auxiliary RDI alarm is removed when bit 6 is low for five/ten consecutive frames. The Enhanced RDI alarm is detected when the enhanced RDI code in bits 5,6,7 of the path status byte indicates the same error codepoint for five/ten consecutive frames. The Enhanced RDI alarm is removed when the enhanced RDI code in bits 5,6,and 7 of the path status byte indicates the same non-error codepoint for five/ten consecutive frames. The ERDII maskable interrupt is set high when bits 5, 6, and 7 of the path status byte (G1) byte are set to a new codepoint for five or ten consecutive frames. The ERDIV[2:0] signal reflects the state of the filtered ERDI value (G1 byte bits 5, 6, and 7).

7.20 STS-1E SONET/SDH Path Aligner

The SONET/SDH Path Aligner (STAL) synchronizes the receive STS-1E path data streams to the TelecomBus clocks.

Frequency offsets (due to receive path information) and phase differences (due to normal network operation) between a channel's path stream and the STS-12 TelecomBus are accommodated by pointer adjustments on the SONET/SDH stream. The alignment is accomplished by recalculating the SONET/SDH payload pointer value based on the offset between transport overhead of the path data stream and the TelecomBus data stream. The Add or Drop TelecomBus data stream is selected by the TX_SLICE_DROP_ADDB and the RX_SLICE_ADD_DROPB bits.

7.21 Performance Monitor Accumulator (PMON)

The Performance Monitor (PMON) Block interfaces directly with:

- Either the DS3 Framer (T3-FRMR) to accumulate line code violation (LCV) events, parity error (PERR) events, path parity error (CPERR) events, far end block error (FEBE) events, excess zeros (EXZS), and framing bit error (FERR) events using saturating counters;
- The E3 Framer (E3-FRMR) to accumulate LCV, PERR (in G.832 mode), FEBE and FERR events;

The PMON stops accumulating error signals from the E3 or DS3 Framers once frame synchronization is lost.

When an accumulation interval is signaled by a write to the PMON register address space or a write to the ARROW 155 Channel Identification, Master Reset, and Global Monitor Update register, the PMON transfers the current counter values into microprocessor accessible holding registers and resets the counters to begin accumulating error events for the next interval. The counters are reset in such a manner that error events occurring during the reset period are not missed.

When counter data is transferred into the holding registers, an interrupt is generated, providing the interrupt is enabled. If the holding registers have not been read since the last interrupt, an overrun status bit is set. In addition, a register is provided to indicate changes in the PMON counters since the last accumulation interval.

7.22 Bit-Oriented Code Detector (RBOC)

The Bit-Oriented Code Detector is only used in DS3 C-bit Parity.

The Bit-Oriented Code Detector (RBOC) Block detects the presence of 63 of the 64 possible bit-oriented codes (BOCs) contained in the DS3 C-bit parity far-end alarm and control (FEAC) channel. The 64^{th} code ("111111") is similar to the HDLC flag sequence and is ignored.

Bit-oriented codes (BOCs) are received on the FEAC channel as 16-bit sequences each consisting of 8 ones, a zero, 6 code bits, and a trailing zero ("111111110xxxxxx0"). BOCs are validated when repeated at least 10 times. The RBOC can be enabled to declare a code valid if it has been observed for 8 out of 10 times or for 4 out of 5 times, as specified by the AVC bit in the RBOC Configuration/Interrupt Enable Register. The RBOC declares that the code is removed if two code sequences containing code values different from the detected code are received in a moving window of ten code periods.

Valid BOCs are indicated through the RBOC Interrupt Status Register. The BOC bits are set to all ones ("111111") when no valid code is detected. The RBOC can be programmed to generate an interrupt when a detected code has been validated and when the code is removed.

7.23 Facility Data Link Receiver (RDLC)

The RDLC is a microprocessor peripheral used to receive LAPD/HDLC frames on any serial HDLC bit stream that provides data and clock information such as the DS3 C-bit parity Path Maintenance Data Link, the E3 G.832 Network Requirement byte or the General Purpose data link (selectable using the RNETOP bit in the ARROW 155 Data Link and FERF/RAI Control register), the E3 G.751 Network Use bit, or the DS3 Mapping Overhead Communication Channel.

The RDLC detects the change from flag characters to the first byte of data, removes stuffed zeros on the incoming data stream, receives packet data, and calculates the CRC-16.ISO-3309 frame check sequence (FCS).

In the address matching mode, only those packets whose first data byte matches one of two programmable bytes or the universal address (all ones) are stored in the FIFO. The two least significant bits of the address comparison can be masked for LAPD SAPI matching.

Received data is placed into a 128-byte-level FIFO buffer. An interrupt is generated when a programmable number of bytes are stored in the FIFO buffer. Other sources of interrupt are detection of the terminating flag sequence, abort sequence, or FIFO buffer overrun.

The Status Register contains bits that indicate the overrun or empty FIFO status, the interrupt status, and the occurrence of first flag or end of message bytes written into the FIFO. The Status Register also indicates the abort, flag, and end of message status of the data just read from the FIFO. On end of message, the Status Register indicates the FCS status and if the packet contained a non-integer number of bytes.

7.24 Pseudo-Random Sequence Generator/Detector (PRGD)

The Pseudo-Random Sequence Generator/Detector (PRGD) block is a software programmable test pattern generator, receiver and analyzer. Two types of test patterns, pseudo-random and repetitive, conform to ITU-T O.151.

The PRGD can be programmed to generate any pseudo-random pattern up to 2^{32}-1 bits in length or any user programmable bit pattern from 1 to 32 bits in length. In addition, the PRGD can insert single bit errors or a bit error rate between 10^{-1} and 10^{-7}.

The PRGD can be programmed to check for the presence of the generated pseudo-random pattern. The PRGD can perform an auto-synchronization to the expected pattern, and generate interrupts on detection and loss of the specified pattern. The PRGD can accumulate the total number of bits received and the total number of bit errors in two saturating 32-bit counters. The counters accumulate over an interval defined by writes to the ARROW 155 Identification/Master Reset, and Global Monitor Update register (register 006) or by writes to any PRGD accumulation register. When an accumulation is forced by either method, then the holding registers are updated and the counters reset to begin accumulating for the next interval. The counters are reset in such a way that no events are missed. The data is then available in the holding registers until the next accumulation. In addition to the two counters, a record of the 32 bits received immediately prior to the accumulation is available.

The PRGD may also be programmed to check for repetitive sequences. When configured to detect a pattern of length N bits, the PRGD will load N bits from the detected stream and determine whether the received pattern repeats itself every N subsequent bits. Should it fail to find such a pattern, it will continue loading and checking until it finds a repetitive pattern. All the features (error counting, auto-synchronization, etc.) available for pseudo-random sequences are also available for repetitive sequences. Whenever a PRGD accumulation is forced, the PRGD stores a snapshot of the 32 bits received immediately prior to the accumulation. This snapshot may be examined in order to determine the exact nature of the repetitive pattern received by PRGD.

The pseudo-random or repetitive pattern can be inserted/extracted in the DS3 or E3 payloads.

7.25 JAT622

The JAT622 serializes the SONET/SDH frame and outputs it to the PECL transmitter.

In normal mode, the JAT acts as a simple PISO. Transmit data is clocked in byte-wise, serialized, and then transmitted. In this mode, the JAT can achieve a normal mode output intrinsic jitter of less than 0.1 UIpp as measured at the optical output.

7.26 Transmit Regenerator Multiplexer Processor (TRMP)

The Transmit Regenerator and Multiplexer Processor (TRMP) block inserts the transport overhead bytes in the transmit data stream.

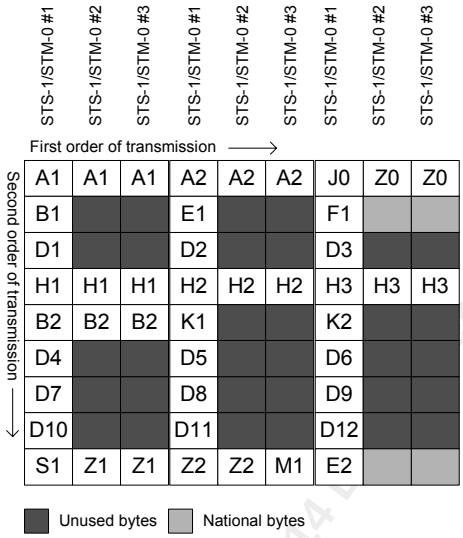
The TRMP accumulates the line BIP-8 errors detected by the RRMP during the last receive frame. The line BIP-8 errors are returned to the far end as line remote error indication (REI-L) during the next transmit frame. Because the RRMP and the TRMP are in two different clock domains, none, one or two line BIP-8 errors can be accumulated per transmit frame (if configured for block BIP mode). The minimum value between the maximum REI-L given in Table 8 and the accumulator count is returned as the line REI-L in the M1 byte of STS-1 (STM-0) #3. Optionally, block BIP-24 errors can be accumulated.

Table 8 Maximum Line REI Errors per Transmit Frame

SONET/SDH	Maximum Single BIP-8 errors LREIBLK=0	Maximum Block BIP-24 errors LREIBLK=1
STS-3/STM-1	0001 1000	0000 0001
STS-12/STM-4	0110 0000	0000 0100

The TRMP serially inputs all the transport overhead (TOH) bytes from the TTOH port. The TOH bytes must be input in the same order that they are transmitted (A1, A2, J0/Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, S1/Z1, Z2/M1/Z2 and E2). TTOHCLK is the generated output clock used to provide timing for the TTOH port. TTOHCLK is a nominal 5.18 MHz clock generated by gapping a 6.48 MHz clock. Sampling TTOHFP high with the rising edge of TTOHCLK identifies the MSB of the first A1 byte. TTOHEN port is used to validate the byte insertion on a byte per byte basis. When TTOHEN is sampled high on the MSB of the serial byte, the serial byte is inserted. When TTOHEN is sampled low on the MSB of the serial byte, the serial byte is discarded.

Figure 15 STS-3 (STM-1) On TTOH



The TRMP serially inputs the line DCC bytes from the TSLD ports. TSLD is selectable to input either the section DCC bytes (D1-D3) or the line DCC bytes (D4-D12). TSLDCLK is the generated output clock used to provide timing for the TSLD port. If TSLD carries the line DCC, TSLDCLK is a nominal 576 kHz clock or if TSLD carries the section DCC, TSLDCLK is a nominal 192 kHz clock. Sampling TTOHFP high identifies the MSB of the first DCC byte on TSLD (D1 or D4).

The TRMP also inserts most of the transport overhead bytes from internal registers. Since there are multiple sources for the same overhead byte, the TOH bytes must be prioritized according to Table 9 before being inserted into the data stream.

Table 9 TOH Insertion Priority

Byte	HIGHEST priority					LOWEST priority
A1		76h (A1ERR=1)	F6h (A1A2EN=1)	TTOH (TTOHEN=1)		A1 = 0xF6
A2			28h (A1A2EN=1)	TTOH (TTOHEN=1)		A2 = 0x28
J0	STS-1/STM-0 # (J0Z0INCEN=1)	J0[7:0] (TRACEEN=1)	J0V (J0REGEN=1)	TTOH (TTOHEN=1)		J0 = 0x00
Z0	STS-1/STM-0 # (J0Z0INCEN=1)		Z0V (Z0REGEN=1)	TTOH (TTOHEN=1)		Z0 = 0x00
B1	All-ones B1DIS = 1			Calculated B1 XOR TTOH (TTOHEN=1 & B1MASKEN=1)		Calculated B1 XOR B1MASK
				TTOH (TTOHEN=1 & B1MASKEN=0)		

Byte	HIGHEST priority					LOWEST priority
E1			E1V (E1REGEN=1)	TTOH (TTOHEN=1)		E1 = 0x00
F1			F1V (F1REGEN=1)	TTOH (TTOHEN=1)		F1 = 0x00
D1 - D3			D1D3V (D1D3REGEN=1)	TTOH (TTOHEN=1)	TSLD (TSLDSEL=0 & TSLDEN=1)	D1-D3 = 0x00
H1				H1 pass through XOR TTOH (TTOHEN=1 & HMASKEN=1)		H1 from SVCA XOR H1MASK
				TTOH (TTOHEN=1 & HMASKEN=0)		
H2				H2 pass through XOR TTOH (TTOHEN=1 & HMASKEN=1)		H2 pass through from SVCA XOR H2MASK
				TTOH (TTOHEN=1 & HMASKEN=0)		
H3				TTOH (TTOHEN=1)		H3 from SVCA
B2	All-ones B2DIS = 1			Calculated B2 XOR TTOH (TTOHEN=1 & B2MASKEN=1)		Calculated B2 XOR B2MASK
				TTOH (TTOHEN=1 & B2MASKEN=0)		
K1		APS[15:8] (APSEN=1)	K1V (K1K2REGEN=1)	TTOH (TTOHEN=1)		K1 = 0x00
K2		APS[7:0] (APSEN=1)	K2V (K1K2REGEN=1)	TTOH (TTOHEN=1)		K2 = 0x00
D4 - D12			D4D12V (D4D12REGEN=1)	TTOH (TTOHEN=1)	TSLD (TSLDSEL=1 & TSLDEN=1)	D4-D12 = 0x00
S1			S1V (S1REGEN=1)	TTOH (TTOHEN=1)		S1 = 0x00
Z1			Z1V (Z1REGEN=1)	TTOH (TTOHEN=1)		Z1 = 0x00
Z2			Z2V (Z2REGEN=1)	TTOH (TTOHEN=1)		Z2 = 0x00
M1			LREI[7:0] (LREIEN=1)	TTOH (TTOHEN=1)		M1 = 0x00
E2			E2V (E2REGEN=1)	TTOH (TTOHEN=1)		E2 = 0x00
Natio nal			NATIONALV (NATIONALEN=1)	TTOH (TTOHEN=1)		National = 0x00

Byte	HIGHEST priority					LOWEST priority
Unused			UNUSEDV (UNUSEDEN=1)	TTOH (TTOHEN=1)		Unused = 0x00
PLD						PLD = 0x00

The Z0DEF register bit defines the Z0/NATIONAL growth bytes for row #1. When Z0DEF is set to logic one, the Z0/NATIONAL bytes are defined according to ITU. When Z0DEF is set to logic zero, the Z0/NATIONAL bytes are defined according to BELLCORE.

Table 10 Z0/National Growth Bytes Definition for Row #1

TRMP Mode	Type	Z0DEF = 1	Z0DEF = 0
STS-3/STM-1	Z0	None	From STS-1/STM-0 #2 to #3
	National	From STS-1/STM-0 #2 to #3	None
STS-12/STM-4 master mode	Z0	From STS-1/STM-0 #2 to #4	From STS-1/STM-0 #2 to #12
	National	From STS-1/STM-0 #5 to #12	None

The H1, H2, B1 and B2 bytes input from the TTOH port are inserted or are used as a mask to toggle bits in the corresponding H1, H2, B1 and B2 bytes depending on the HMASK B1MASK and B2MASK register bits. When the HMASK, B1MASK or B2MASK register bit is set low and TTOHEN is sampled high on the MSB of the serial H1, H2, B1 or B2 byte, the serial byte is inserted in place of the corresponding byte. When the HMASK, B1MASK or B2MASK register bit is set high and TTOHEN is sampled high on the MSB of the serial H1, H2, B1 or B2 byte, the serial byte is XORed with the corresponding path payload pointer (already in the data stream) or the calculated BIP-8 byte before being inserted.

The TRMP inserts the APS bytes detected by the RRMP during the last receive frame. The APS bytes are returned to the far end by the TRMP during the next transmit frame. Because the RRMP and the TRMP are in two different clock domains, none, one, or two APS bytes can be sampled per transmit frame. The last received APS bytes are transmitted.

The TRMP inserts the line remote defect indication (RDI-L) into the data stream. When line RDI must be inserted, the “110” pattern is inserted in bits 6, 7, and 8 of the K2 byte of STS-1 (STM-0) #1. Line RDI insertion has priority over TOH byte insertion. The TRMP also inserts the line alarm indication signal (AIS-L) into the data stream. When line AIS must be inserted, all ones are inserted in the line overhead and in the payload (all bytes of the frame except the section overhead bytes). Line AIS insertion has priority over line RDI insertion and TOH byte insertion.

The TRMP calculates the line BIP-8 error detection codes on the transmit data stream. One line BIP-8 error detection code is calculated for each of the constituent STS-1 (STM-0). The line BIP-8 byte is calculated on the unscrambled bytes of the STS-1 (STM-0) except for the 9 SOH bytes. The line BIP-8 byte is based on a bit interleaved parity calculation using even parity. For each STS-1 (STM-0), the calculated BIP-8 error detection code is inserted in the B2 byte of the following frame before scrambling.

The TRMP optionally scrambles the transmit data stream.

The TRMP calculates the section BIP-8 error detection code on the transmit data stream. The section BIP-8 byte is calculated on the scrambled bytes of the complete frame. The section BIP-8 byte is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 error detection code is inserted in the B1 byte of STS-1 (STM-0) #1 of the following frame before scrambling.

7.27 Transmit Trail trace Processor (TTTP)

The Transmit Trail trace Processor (TTTP) block generates the trail trace messages to be transmitted. The TTTP can generate a 16 or 64 byte trail trace message. The message is sourced from an internal RAM and must have been previously written by an external microprocessor. Optionally, the trail trace message can be reduced to a single continuous trail trace byte.

The trail trace message must include synchronization because the TTTP does not add synchronization. The synchronization mechanism is different for a 16-byte message and for a 64-byte message. When the message is 16 bytes, the synchronization is based on the MSB of the trail trace byte. Only one of the 16 bytes has its MSB set high. The byte with its MSB set high is considered the first byte of the message. When the message is 64 bytes, the synchronization is based on the CR/LF (CR = 0Dh, LF = 0Ah) characters of trail trace message. The byte following the CR/LF bytes is considered the first byte of the message.

To avoid generating an unstable/mismatch message, the TTTP forces the message to all zeros while the microprocessor updates the internal RAM.

7.28 Transmit High Order Path Processor (THPP)

The Transmit High Order Path Processor (THPP) block inserts the path overhead bytes in the transmit data stream.

The THPP accumulates the path BIP-8 errors detected by the RHPP during the last receive frame. The path BIP-8 errors are returned to the far end as path remote error indication (REI-P) during the next transmit frame. Because the RHPP and the THPP are in two different clock domains, none, one, or two path BIP-8 errors can be accumulated per transmit frame (if configured for block BIP mode). The minimum value between the maximum REI-P and the accumulator count is returned as the path REI in the G1 byte. Optionally, block BIP-8 errors can be accumulated.

The THPP serially inputs all the path overhead (POH) bytes from the TPOH port. The POH bytes must be input in the same order that they are transmitted (J1, B3, C2, G1, F2, H4, F3, K3, and N1). TPOHCLK is the generated output clock used to provide timing for the TPOH port. TPOHCLK is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. Sampling TPOHFP high with the rising edge of TPOHCLK identifies the MSB of the first J1 byte. The TPOHEN port is used to validate the byte insertion on a byte per byte basis. When TPOHEN is sampled high on the MSB of the serial byte, the serial byte is inserted. When TPOHEN is sampled low on the MSB of the serial byte, the serial byte is discarded.

The THPP calculates the path BIP-8 error detection code on the transmit data stream. The path BIP-8 byte is calculated on all the payload bytes. The path BIP-8 byte is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 error detection code is inserted in the B3 byte of the following frame.

Table 11 Path overhead byte source priority

Byte	Highest Priority						Lowest Priority
J1	UNEQV (UNEQ=1)	J1 pass through (TDIS=1 OR PAIS=1)	Path trace buffer (PTBJ1=1)	J1 ind. reg. (SRCJ1=1)		TPOH (TPOHEN=1)	J1 pass through
B3	UNEQV (UNEQ=1)	B3 pass through (TDIS=1 OR PAIS=1)			Calculated B3 XOR TPOH (TPOHEN=1 AND B3MASKEN=1)	TPOH (TPOHEN=1)	Calculated B3 XOR B3MASK
C2	UNEQV (UNEQ=1)	C2 pass through (TDIS=1 OR PAIS=1)	C2 ind. reg. (SRCC2=1)			TPOH (TPOHEN=1)	C2 pass through
G1	UNEQV (UNEQ=1)	G1 pass through (TDIS=1 OR PAIS=1 OR IBER=1)	PRDI[2:0] and PREI[3:0] (ENG1REC =1)	G1 ind. reg. (SRCG1=1)		TPOH (TPOHEN=1)	G1 pass through
F2	UNEQV (UNEQ=1)	F2 pass through (TDIS=1 OR PAIS=1)	F2 ind. reg. (SRCF2=1)			TPOH (TPOHEN=1)	F2 pass through
H4	UNEQV (UNEQ=1)	H4 pass through (TDIS=1 OR PAIS=1)	H4 pass through XOR H4 ind. reg. (SRCH4=1 AND ENH4MAS K=1)	H4 ind. reg. (SRCH4=1)	H4 pass through XOR TPOH (TPOHEN=1 AND H4MASK=1)	TPOH (TPOHEN=1)	H4 pass through
Z3	UNEQV (UNEQ=1)	Z3 pass through (TDIS=1 OR PAIS=1)	Z3 ind. reg. (SRCZ3=1)			TPOH (TPOHEN=1)	Z3 pass through
Z4	UNEQV (UNEQ=1)	Z4 pass through (TDIS=1 OR PAIS=1)	Z4 ind. reg. (SRCZ4=1)			TPOH (TPOHEN=1)	Z4 pass through
Z5	UNEQV (UNEQ=1)	Z5 pass through (TDIS=1 OR PAIS=1)	Z5 ind. reg. (SRCZ5=1)			TPOH (TPOHEN=1)	Z5 pass through

7.29 Transmit Add TelecomBus Pointer Interpreter (SHPI)

The Transmit Add TelecomBus Pointer Interpreter (SHPI) block takes a SONET/SDH data stream from the ADD TelecomBus bus, interprets the STS-1/3c (AU3/4) pointers, indicates the J1 byte locations and detects alarm conditions (e.g. AIS-P).

The SHPI block allows the ARROW 155 to operate with TelecomBus like back plane systems which do not indicate the J1 byte positions. Each timeslot may be individually enabled with the PT_PATH[12:1] bits. (Note that all paths are enabled by default.) When enabled, the SHPI reads the H1/H2 bytes for that timeslot to generate the AJ1, APL, and AALARM signals. When disabled, the SHPI passes the AJ1, APL and AALARM signals transparently from the TelecomBus for that timeslot. Note that the AALARM input signal is ORed with the generated AALARM signal for downstream blocks, so regardless of the value of PT_PATH[12:1], a path alarm indicated by a ‘1’ on AALARM input will cause AIS insertion in the transmit stream.

7.30 SONET/SDH PRBS Generator and Monitor (PRGM)

The SONET/SDH Pseudo-Random bit sequence Generator and Monitor (PRGM) block generates and monitors an unframed 2^{23}-1 payload test sequence on the TelecomBus ADD or DROP bus.

The PRGM can generate PRBS in an STS-1/3c (AU3/4) payload. The path overhead column, and the fixed stuff column #30 and #59 in an STS-1 (AU3) payload do not contain any PRBS data. The PRGM generator can be configured to preserve payload framing and overwrite the payload bytes or can be configured to autonomously generate payload framing and overwrite the payload bytes.

The PRBS monitor of the PRGM block monitors the recovered payload data for the presence of an unframed 2^{23}-1 test sequence and accumulates pattern errors based on this pseudo-random pattern. The PRGM declares synchronization when a sequence of 32 correct pseudo-random patterns (bytes) are detected consecutively. Pattern errors are only counted when the PRGM is in synchronization with the input sequence. When 16 consecutive pattern errors are detected, the PRGM will fall out of synchronization and will continuously attempt to re-synchronize to the input sequence until it is successful.

A maskable interrupt is activated to indicate any change in the synchronization status.

7.31 DS3/E3 Mapper (D3E3MA)

The D3E3MA accepts either a DS3 or E3 serial stream and maps it into an STS-1 SPE via AU-3 mapping (AU-3 paths are optionally mapped into TU3 paths in the SVCA). The D3E3MA performs the DS3/E3 to STS-1 mapping, and keeps mapping jitter within ITU and ANSI specifications.

7.31.1 FIFO

The Elastic Store FIFO is 32 bytes deep. The Elastic Store FIFO can be reset via normal mode register bit. Upon reset, overflow or underflow, the FIFO read and write pointers are set as far away from each other as possible. The Elastic Store FIFO also maintains FIFO centering through simple peak detection, or through a secondary centering method which maintains the FIFO fill level at an optimal operation position.

Both FIFO centering mechanisms can be enabled/disabled via normal mode register bit GAPCALCB and FIFOCTRB.

7.31.2 AIS Generator

The AIS Generator creates the E3 and DS3 Alarm Indication Signal that is inserted into the bit stream to indicate failure conditions. The AIS Generator is controlled via normal mode register bits (DS3E3B, AISGEN) and upstream AIS generation signals. The AIS pattern is described in section the operations document.

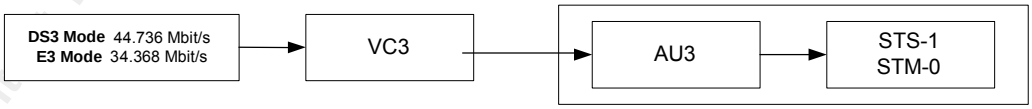
During AIS mode, the stuff commands from the DPLL are ignored and nominal stuffing is applied by driving the respective outputs accordingly. Nominal Rate stuffing requires the insertion of an information bit into the stuff opportunity position 3 times per STS-1 frame.

7.31.3 Mapper

The Mapper block receives E3 or DS3 payload data from the FIFO, maps the data according to Figure 16 and outputs the data to the downstream block. The Mapper also performs Overhead Communication Channel Insertion.

The D3E3MA maps either DS3 or E3 into AU3. These mapping modes can be set via the DS3E3B register bit. Regardless of the incoming data source (AIS or FIFO) the D3E3MA first maps the DS3 or E3 stream to a common VC-3 structure. The VC-3 is then mapped to an STS-1/ STM-0 SPE via AU3. The overall mapping structure implemented is depicted in Figure 16.

Figure 16 Mapping Structure



In DS3 or E3 mode, the D3E3MA maps the incoming DS3 or E3 payload into a VC-3. The DS3 or E3 payload is always demapped from a VC-3, regardless of whether the SPE has been mapped according to AU3 specifications. The asynchronous DS3 or E3 to VC-3 mapping is shown in the operations document.

The overhead communications channel is inserted from the microprocessor interface via TDPR block. The insertion of the Overhead communication channel is only valid during DS3 operation. If the D3E3MA is operating in E3 mode, the Overhead Communication Channel is ignored.

7.31.4 DPLL

The Digital Phase Lock Loop (DPLL) tracks changes in frequency between the serial DS3/E3 clock and the SONET clock and provides information to the mapper regarding stuff opportunities.

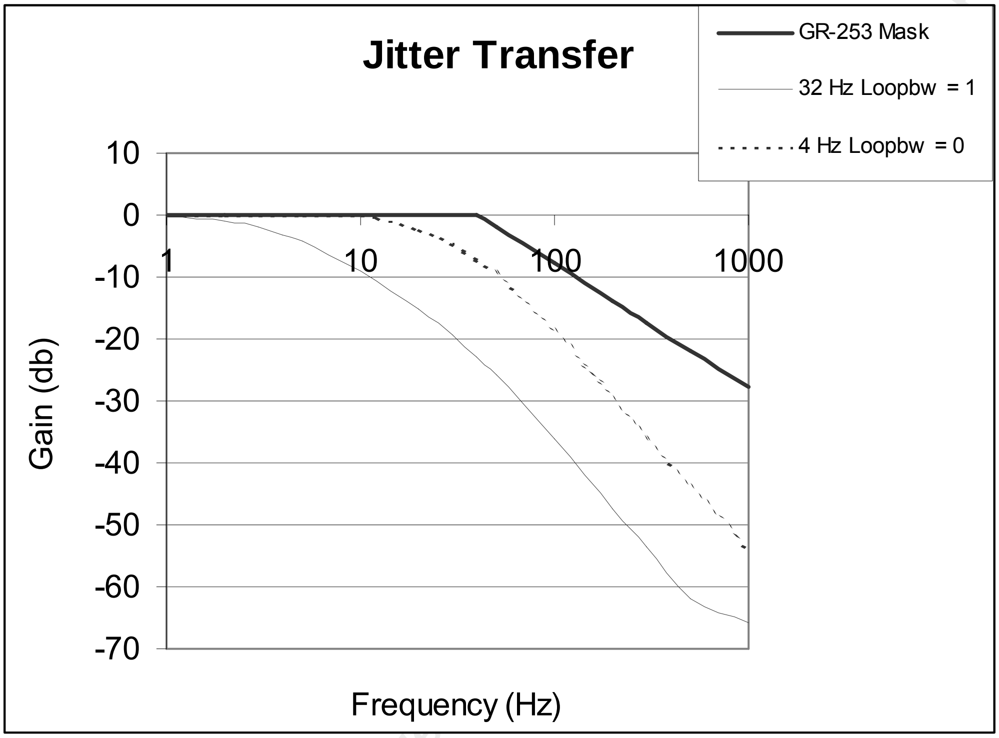
The DPLL has two modes for locking to the incoming signal: fast and normal. Under fast operation the loop bandwidth is increased causing the DPLL to lock more quickly to a change in frequency, but consequently the DPLL is less sensitive to small variations in frequency. The loop bandwidth can be selected via normal mode register bit LOOPBW.

7.31.5 Transfer Function

Jitter transfer is defined as the ratio of jitter on the output signal (DS3/E3 mapped into SONET) to the jitter applied to the input signal (serial DS3/E3). Requirements for jitter transfer are given in terms of a jitter transfer mask, which represents the maximum acceptable jitter gain (in dB) for a specified range of jitter frequencies.

Typical D3E3MA jitter transfer characteristics are show in the Figure 17.

Figure 17 Typical D3E3MA Jitter Transfer



The system (including the D3E3MA) intrinsic jitter, pointer jitter, jitter tolerance, mapping wander, and pointer wander characteristics are described in Section 13.8.

The D3E3MA may be configured to generate interrupts on error events or status changes. All sources of interrupts can be masked or acknowledged via internal registers. Internal registers are also used to configure the D3E3MA. Access to these registers is via a generic microprocessor bus.

7.32 DS3 Transmitter

The DS3 Transmitter (T3-TRAN) Block integrates circuitry required to insert the overhead bits into a DS3 bit stream and produce a B3ZS-encoded signal. The T3-TRAN is directly compatible with the M23 and C-bit parity DS3 formats.

Status signals such as far end receive failure (FERF), the alarm indication signal, and the idle signal can be inserted when their transmission is enabled by internal register bits. FERF can also be automatically inserted on detection of any combination of LOS, OOF or RED, or AIS by the T3-FRMR.

A valid pair of P-bits is automatically calculated and inserted by the T3-TRAN. When C-bit parity mode is selected, the path parity bits and far end block error (FEBE) indications are automatically inserted.

When enabled for C-bit parity operation, the FEAC channel is sourced by the XBOC bit-oriented code transmitter. The path maintenance data link messages are sourced by the TDPR data link transmitter. These overhead signals can also be overwritten by using the TOH and TOHINS inputs.

When enabled for M23 operation, the C-bits are forced to logic 1 with the exception of the C-bit Parity ID bit (first C-bit of the first M-subframe), which is forced to toggle every M-frame.

The T3-TRAN supports diagnostic modes in which it inserts parity or path parity errors, F-bit framing errors, M-bit framing errors, invalid X or P-bits, line code violations, or all-zeros.

User control of each of the overhead bits in the DS3 frame is provided. Overhead bits may be inserted on a bit-by-bit basis from a user supplied data stream. An overhead clock (at 526 kHz) and a DS3 overhead alignment output are provided to allow for control of the user provided stream.

7.33 E3 Transmitter

The E3 Transmitter (E3-TRAN) Block integrates circuitry required to insert the overhead bits into an E3 bit stream and produce an HDB3-encoded signal. The E3-TRAN is directly compatible with the G.751 and G.832 framing formats.

The E3-TRAN generates the frame alignment signal and inserts it into the incoming serial stream based on either the G.751 or G.832 formats and an alignment pulse applied to it by the SPLT block. All overhead and status bits in each frame format can be individually controlled by register bits or by the transmit overhead stream. While in certain framing format modes, the E3-TRAN generates various overhead bytes according to the following:

7.33.1 In G.832 E3 Format, the E3-TRAN:

1. Inserts the BIP-8 byte calculated over the preceding frame.

2. Inserts the Trail Trace bytes through the Trail Trace Buffer (TTB) block.

3. Inserts the FERF bit via a register bit or, optionally, when the E3-FRMR declares OOF, or when the loss of cell delineation (LCD) defect is declared.

4. Inserts the FEBE bit, which is set to logic 1 when one or more BIP-8 errors are detected by the receive framer. If there are no BIP-8 errors indicated by the E3-FRMR, the E3-TRAN sets the FEBE bit to logic 0.

5. Inserts the Payload Type bits based on the register value set by the microprocessor.

6. Inserts the Tributary Unit multi-frame indicator bits either via the TOH overhead stream or by register bit values set by the microprocessor.

7. Inserts the Timing Marker bit via a register bit.

8. Inserts the Network Operator (NR) byte from the TDPR block when the TNETOP bit in the Channel Data Link and FERF/RAI Control register is logic 1; otherwise, the NR byte is set to all ones. The NR byte can be overwritten using the TOH and TOHINS input pins. All 8 bits of the Network Operator byte are available for use as a data link.

9. Inserts the General Purpose Communication Channel (GC) byte from the TDPR block when the TNETOP bit in the Channel Data Link and FERF/RAI Control register is logic 0; otherwise, the byte is set to all ones. The GC byte can be overwritten using the TOH and TOHINS input pins.

7.33.2 In G.751 E3 Mode, the E3-TRAN:

1. Inserts the Remote Alarm Indication bit (bit 11 of the frame) either via a register bit or, optionally, when the E3-FRMR declares OOF.

2. Inserts the National Use reserved bit (bit 12 of the frame) either as a fixed value through a register bit or from the TDPR block as configured by the TNETOP bit in the Channel Data Link and FERF/RAI Control register and the NATUSE bit in the E3 TRAN Configuration register.

3. Optionally identifies the tributary justification bits and stuff opportunity bits as either overhead or payload to SPLT for payload mappings that take advantage of the full bandwidth.

4. Further, the E3-TRAN can provide insertion of bit errors in the framing pattern or in the parity bits, and insertion of single line code violations for diagnostic purposes. Most of the overhead bits can be overwritten using the TOH and TOHINS input pins.

7.34 STS-1E Transmit Section Overhead Processor (TSOP)

The Transmit Section Overhead Processor (TSOP) provides frame pattern insertion (A1, A2), scrambling, section level alarm signal insertion, and section BIP-8 (B1) insertion. In addition, it may insert the section data communication channel provided via the TDPR.

7.34.1 Line AIS Insert

Line AIS insertion results in all bits of the SONET/SDH frame being set to 1 before scrambling except for the section overhead. The Line AIS Insert Block substitutes all ones as described when enabled by the TLAIS input or through an internal register accessed through the microprocessor interface. Activation or deactivation of line AIS insertion is synchronized to frame boundaries.

7.34.2 Data Link Insert

The Data Link Insert Block inserts the section data communication channel (bytes D1, D2, and D3) into the STS-3c/STM-1 stream when enabled by an internal register accessed via the microprocessor interface. The bytes to be inserted are input through the TDPR (STS-1E).

7.34.3 BIP-8 Insert

The BIP-8 Insert Block calculates and inserts the BIP-8 error detection code (B1) into the transmit stream.

The BIP-8 calculation is based on the scrambled data of the complete STS-3c/STM-1 frame. The section BIP-8 code is based on a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP-8 code is then inserted into the B1 byte of the following frame before scrambling. BIP-8 errors may be continuously inserted under register control for diagnostic purposes.

7.34.4 Framing and Identity Insert

The Framing and Identity Insert Block inserts the framing bytes (A1, A2) and trace/growth bytes (J0/Z0) into the STS-3c/STM-1 frame. Framing bit errors may be continuously inserted under register control for diagnostic purposes.

7.34.5 Scrambler

The Scrambler Block utilizes a frame synchronous scrambler to process the transmit stream when enabled through an internal register accessed via the microprocessor interface. The generating polynomial is $x^7 + x^6 + 1$. Precise details of the scrambling operation are provided in the references. Note that the framing bytes and the identity bytes are not scrambled. All zeros may be continuously inserted (after scrambling) under register control for diagnostic purposes.

7.35 STS-1E Transmit Line Overhead Processor (TLOP)

The Transmit Line Overhead Processor (TLOP) provides line level alarm signal insertion, and line BIP-24 insertion (B2). In addition, it inserts the line data communication provided through the TDPR.

7.35.1 APS Insert

The APS Insert Block inserts the two automatic protection switch (APS) channel bytes in the Line Overhead (K1 and K2) into the transmit stream when enabled by an internal register.

7.35.2 Data Link Insert

The Data Link Insert Block inserts the line data communication channel (DCC) (bytes D4 to D12) into the STS-3c/STM-1 stream when enabled by an internal register. The D4 to D12 bytes are input through the TDPR (STS-1E) block.

7.35.3 Line BIP Calculate

The Line BIP Calculate Block calculates the line BIP-24 error detection code (B2) based on the line overhead and synchronous payload envelope of the transmit stream. The line BIP-24 code is a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP-24 code is inserted into the B2 byte positions of the following frame. BIP-24 errors may be continuously inserted under register control for diagnostic purposes.

7.35.4 Line RDI Insert

The Line RDI Insert Block controls the insertion of line remote defect indication. Line RDI insertion is enabled through register control. Line RDI is inserted by transmitting the code 110 (binary) in bit positions 6, 7, and 8 of the K2 byte contained in the transmit stream.

7.35.5 Line REI Insert

The Line REI Insert Block accumulates line BIP-24 errors (B2) detected by the Receive Line Overhead Processor and encodes remote error indications in the transmit Z2 byte.

7.36 STS-1E Transmit Path Overhead Processor (TPOP)

The Transmit Path Overhead Processor (TPOP) provides transport frame alignment generation, pointer generation (H1, H2), path overhead insertion and the insertion of path level alarm signals.

7.36.1 Pointer Generator

The Pointer Generator Block generates the outgoing payload pointer (H1, H2) as specified in the references. The concatenation indication (the NDF field set to 1001, I-bits, and D-bits set to all ones, and unused bits set to all zeros) is inserted in the second and third pointer byte locations in the transmit stream.

1. A "normal pointer value" locates the start of the SPE. Note: 0 ≤ "normal pointer value" ≤ 782, and the new data flag (NDF) field is set to 0110. Note that values greater than 782 may be inserted, using internal registers, to generate a loss of pointer alarm in downstream circuitry.

2. Arbitrary "pointer values" may be generated using internal registers. These new values may optionally be accompanied by a programmable new data flag. New data flags may also be generated independently using internal registers.

3. Positive pointer movements may be generated using a bit in an internal register. A positive pointer movement is generated by inverting the five I-bits of the pointer word. The SPE is not inserted during the positive stuff opportunity byte position, and the pointer value is incremented by one. Positive pointer movements may be inserted once per frame for diagnostic purposes.

4. Negative pointer movements may be generated using a bit in an internal register. A negative pointer movement is generated by inverting the five D-bits of the pointer word. The SPE is inserted during the negative stuff opportunity byte position, the H3 byte, and the pointer value is decremented by one. Negative pointer movements may be inserted once per frame for diagnostic purposes.

The pointer value is used to insert the path overhead into the transmit stream. The current pointer value may be read via internal registers.

7.36.2 BIP-8 Calculate

The BIP-8 Calculate Block performs a path bit interleaved parity calculation on the SPE of the transmit stream. Details are provided in the references. The resulting parity byte is inserted in the path BIP-8 (B3) byte position of the subsequent frame. BIP-8 errors may be continuously inserted under register control for diagnostic purposes.

7.36.3 Path REI Calculate

The Path REI Calculate Block accumulates path remote error indications (REI-P) on a per frame basis, and inserts the accumulated value (up to maximum value of eight) in the REI-P bit positions of the path status (G1) byte. The REI-P information is derived from path BIP-8 errors detected by the receive path overhead processor, RPOP. Remote error indications may be inserted under register control for diagnostic purposes.

7.37 Bit Oriented Code Generator (XBOC)

The Bit Oriented Code Generator (XBOC) Block transmits 63 of the possible 64 bit oriented codes (BOC) in the C-bit parity Far End Alarm and Control (FEAC) channel. A BOC is a 16-bit sequence consisting of 8 ones, a zero, 6 code bits, and a trailing zero (111111110xxxxxx0) which is repeated as long as the code is not 111111. The code to be transmitted is programmed by writing the XBOC Code Register. The 64^{th} code (111111) is similar to the HDLC idle sequence and is used to disable the transmission of any bit-oriented codes. When transmission is disabled, the FEAC channel is set to all ones.

7.38 Trail Trace Buffer (TTB)

The Trail Trace Buffer (TTB) extracts and sources the trail trace message carried in the TR byte of the G.832 E3 stream. The message is used by the OS to prevent delivery of traffic from the wrong source and is 16 bytes in length. The 16-byte message is framed by the PTI Multi-frame Alignment Signal (TMFAS = 'b10000000 00000000). One bit of the TMFAS is placed in the most significant bit of each message byte. In the receive direction, the trail trace message is extracted from the serial overhead stream output by the E3-FRMR. The extracted message is stored in the internal RAM for review by an external microprocessor. By default, the TTB will write the byte of a 16-byte message with its most significant bit set high to the first location in the RAM. The extracted trail trace message is checked for consistency between consecutive multi-frames. A message received unchanged three or five times (programmable) is accepted for comparison with the copy previously written into the internal RAM by the external microprocessor. Alarms are raised to indicate reception of unstable and mismatched messages. In the transmit direction, the TTB sources the trail trace message from the internal RAM for insertion into the TR byte by the E3-TRAN.

The TTB also extracts the Payload Type label carried in the MA byte of the G.832 E3 stream. The label is used to ensure that the adaptation function at the trail termination sink is compatible with the adaptation function at the trail termination source. The Payload Type label is checked for consistency between consecutive multi-frames. A Payload Type label received unchanged for five frames, is accepted for comparison with the copy previously written into the TTB by the external microprocessor. Alarms are raised to indicate reception of unstable and mismatched Payload Type label bits.

7.39 Facility Data Link Transmitter (TDPR)

The Facility Data Link Transmitter (TDPR) provides a serial data link for the C-bit parity path maintenance data link in DS3, the serial Network Operator byte or the General Purpose data link in G.832 E3, the National Use bit data link in G.751 E3, the DS3 Mapping Overhead Communication Channel, or the Transmit SONET/SDH Path DCC Channel.

The TDPR is used under microprocessor control to transmit HDLC data frames. It performs all of the data serialization, CRC generation, zero-bit stuffing, as well as flag and abort sequence insertion. Upon completion of the message, a CRC-16.ISO-3309 frame check sequence (FCS) can be appended, followed by flags. If the TDPR transmit data FIFO underflows, an abort sequence is automatically transmitted.

When enabled, the TDPR continuously transmits flags (01111110) until data is ready to be transmitted. Data bytes to be transmitted are written into the TDPR Transmit Data Register. The TDPR automatically begins transmission of data when at least one complete packet is written into its FIFO. All complete packets of data will be transmitted if no error condition occurs. After the last data byte of a packet, if CRC insertion has been enabled, the CRC FCS and a flag are transmitted. If CRC insertion has not been enabled only a flag is transmitted. The TDPR then returns to the transmission of flag characters until the next packet is available for transmission. The TDPR will also force transmission of the FIFO data once the FIFO depth has surpassed the programmable upper limit threshold. Transmission commences regardless of whether or not a packet has been completely written into the FIFO. The user must be careful to avoid overfilling the FIFO. Underruns can only occur if the packet length is greater than the programmed upper limit threshold because, in such a case, transmission will begin before a complete packet is stored in the FIFO.

An interrupt can be generated once the FIFO depth has fallen below a user configured lower threshold as an indicator for the user to write more data. Interrupts can also be generated if the FIFO underflows while transmitting a packet, when the FIFO is full, or if the FIFO is overrun. The TDPR only processes one packet at a time; therefore, if a packet is sent to the TDPR before the previous packet is complete, the lower threshold must not be used as the only indicator to write more data, because small packets may be less than the lower threshold limit. A combination of the lower threshold limit AND the FIFO full flags must be used to indicate when to write more data to the TDPR.

If there are more than five consecutive ones in the raw transmit data or in the CRC data, a zero is stuffed into the serial data output. This prevents the unintentional transmission of flag or abort sequences.

Abort sequences (01111111 sequence where the 0 is transmitted first) can be continuously transmitted at any time by setting a control bit. During packet transmission, an underrun situation can occur if data is not written to the TDPR Transmit Data register before the previous byte has been depleted. In this case, an abort sequence is transmitted and the controlling processor is notified via the UDR register bit. An abort sequence will also be transmitted if the user overflows the FIFO with a packet of length greater than 128 bytes. Overflows where other complete packets are still stored in the FIFO will not generate an abort. Only the packet that caused the overflow is corrupted and an interrupt is generated to the user via the OVR register bit. The other packets remain unaffected.

When the TDPR is disabled, a logical 1 (Idle) is inserted in the path maintenance data link.

7.40 JTAG Test Access Port

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE, and STCTEST instructions are supported.

Refer to *PMC-2021518 JTAG Test Features Description Applications Note* for more information.

The ID code for ARROW 155 is constructed from the following bit fields:

JTAG_ID[31:28] = 0h	Rev ID
JTAG_ID[27:12] = 5320h	Device ID
JTAG_ID[11:0] = 0CDh	PMC_ID

7.41 Microprocessor Interface

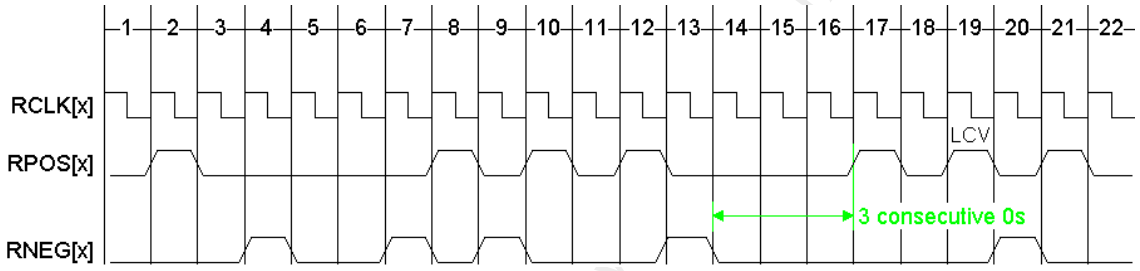
The microprocessor interface block provides access to normal mode registers, and the logic required to connect to the microprocessor interface. The normal mode registers are required for normal operation, and test mode registers are used to enhance the testability of the ARROW 155. The register descriptions for the ARROW 155 are located in PMC-2031892, *ARROW 155 Telecom Standard Product Data Sheet Register Description.* For all register accesses, CSB must be low.

8 Functional Timing

All functional timing diagrams assume that polarity control is not being applied to input and output data and clock lines (i.e. polarity control bits in the ARROW 155 registers are set to their default states).

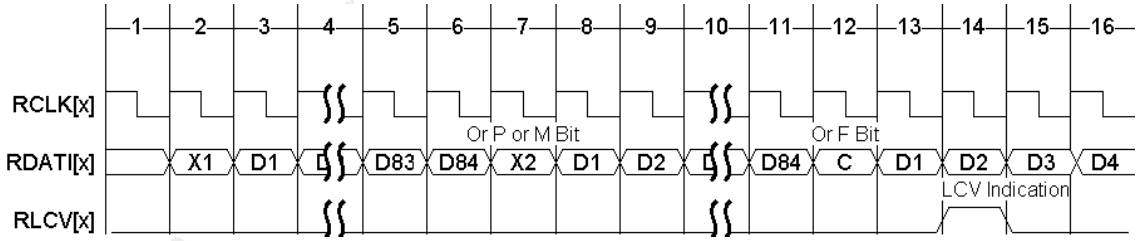
8.1 Receive PDH Serial Formats

Figure 18 Receive Bipolar DS3 Stream



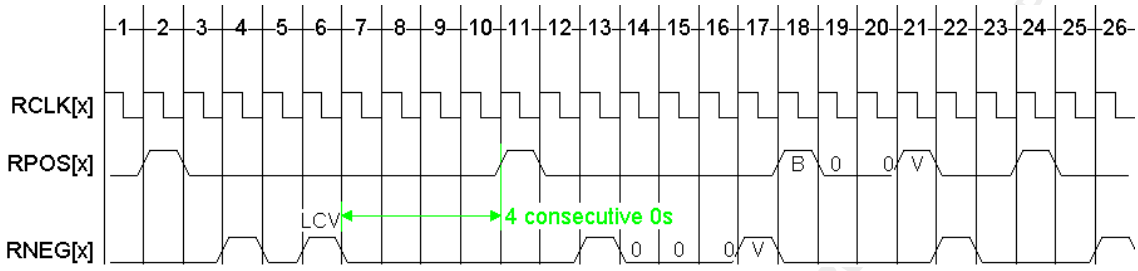
The Receive Bipolar DS3 Stream diagram (Figure 18) shows the operation of the ARROW 155 while processing a B3ZS encoded DS3 stream on inputs RPOS[x] and RNEG[x]. It is assumed that the first bipolar violation (on RNEG[x]) illustrated corresponds to a valid B3ZS signature. A line code violation is declared upon detection of three consecutive zeros in the incoming stream, or upon detection of a bipolar violation which is not part of a valid B3ZS signature.

Figure 19 Receive Unipolar DS3 Stream



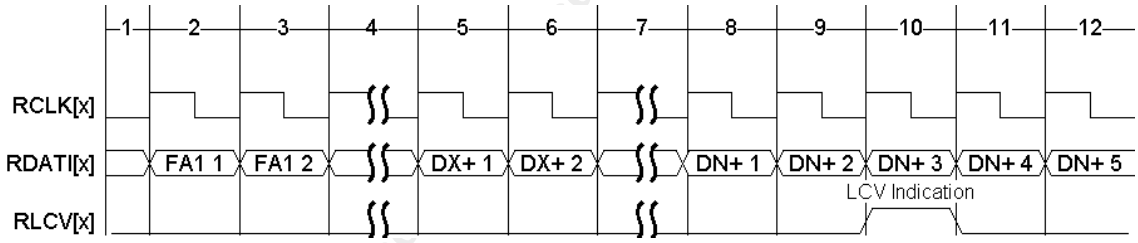
The Receive Unipolar DS3 Stream diagram (Figure 19) shows the complete DS3 receive signal on the RDATI[x] input. Line code violation indications, detected by an upstream B3ZS decoder, are indicated on input RLCV[x]. RLCV[x] is sampled each bit period. The PMON Line Code Violation Event Counter is incremented each time a logic 1 is sampled on RLCV[x].

Figure 20 Receive Bipolar E3 Stream



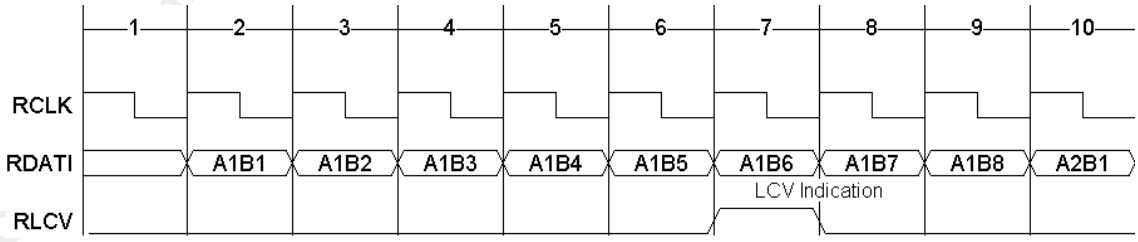
The Receive Bipolar E3 Stream diagram (Figure 20) shows the operation of the ARROW 155 while processing an HDB3-encoded E3 stream on inputs RPOS[x] and RNEG[x]. It is assumed that the first bipolar violation (on RNEG[x]) illustrated corresponds to a valid HDB3 signature (HDB3 Signature Pattern is X00V). A line code violation is declared upon detection of four consecutive zeros in the incoming stream, or upon detection of a bipolar violation, which is not part of a valid HDB3 signature.

Figure 21 Receive Unipolar E3 Stream



The Receive Unipolar E3 Stream diagram (Figure 21) shows the unipolar E3 receive signal on the RDATI[x] input. Line code violation indications, detected by an upstream HDB3 decoder, are indicated on input RLCV. RLCV is sampled each bit period. The PMON Line Code Violation Event Counter is incremented each time a logic 1 is sampled on RLCV.

Figure 22 Receive Unipolar STS-1E Stream



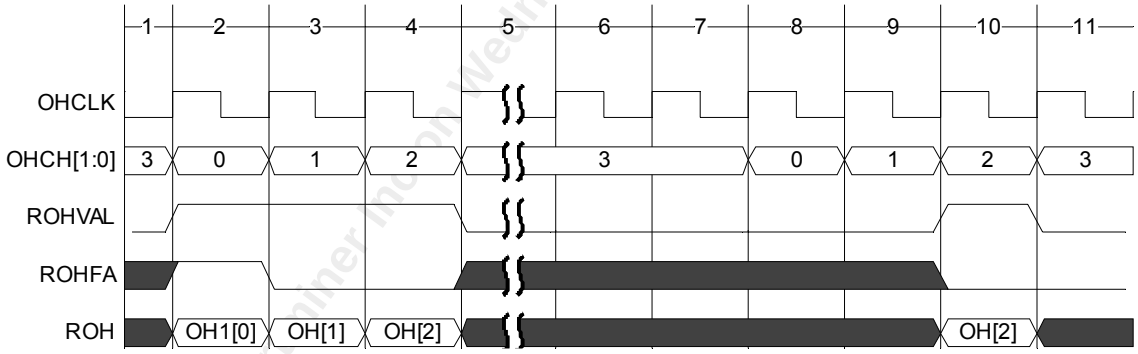
The Receive Unipolar STS-1E Stream diagram (Figure 22) shows the unipolar STS-1E receive signal on the RDATI[x] input. Line code violation indications, detected by an upstream B3ZS decoder, are indicated on input RLCV. RLCV is sampled each bit period. The PMON Line Code Violation Event Counter is incremented each time a logic 1 is sampled on RLCV.

8.2 Receive PDH Overhead Extraction

On each rising edge of OHCLK, the OHCH[1:0] channel ID increments through three valid channels {0, 1, 2} or waits at invlid channel (3) for 9 cycles. If valid data is available for the channel indicated by OHCH[1:0], then the overhead bit for that channel appears on ROH, and ROHVAL is high. Otherwise ROHVAL is low and ROH and ROHFA are invalid. For each channel, ROHFA signals the beginning of the frame and overhead sequence for the channel in OHCH[1:0].

DS3, E3 and STS-1E overhead extraction is output on the ROHVAL, ROHFA, and ROH pins. Because different channels may be processing different overhead types, Figure 23 depicts the generic operation of the receive overhead extraction interface. In Figure 23, OH1 [X], on ROH, depicts the first overhead bit for a given channel [X]. Other overhead bits are shown as OH [X] where X is the channel. The order in which the overhead bits are extracted is discussed below.

Figure 23 Receive Overhead Extraction Structure



For DS3 overhead extraction, ROHFA is asserted once every 56 bits to mark the X1 bit for each active channel. For each DS3 channel, the order of the overhead bit extraction is shown in Table 12, starting from the top left X1 bit, proceeding to the right, and then from sub-frame 1 to sub-frame 7:

Table 12 DS3 Receive Overhead Bits

M-subframe	DS3 Overhead Bits							
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
1	X_1	N/U	C_1	N/U	C_2	N/U	C_3	N/U
2	X_2	N/U	C_1	N/U	C_2	N/U	C_3	N/U
3	P_1	N/U	C_1	N/U	C_2	N/U	C_3	N/U

M-subframe	DS3 Overhead Bits							
	1	2	3	4	5	6	7	8
4	P_2	N/U	C_1	N/U	C_2	N/U	C_3	N/U
5	M_1	N/U	C_1	N/U	C_2	N/U	C_3	N/U
6	M_2	N/U	C_1	N/U	C_2	N/U	C_3	N/U
7	M_3	N/U	C_1	N/U	C_2	N/U	C_3	N/U

The DS3 framing bits (F-bits) are not extracted on the overhead port; however, the bit positions for the framing bits (F-bits) are still maintained. The bit positions corresponding to the F-bits in the extracted stream are marked N/U in the above table and should be ignored. The ROH stream for a particular channel is invalid when the DS3 frame alignment is lost for that channel.

For Receive G.751 E3 Overhead extraction, ROHFA is asserted once every 48 bits to mark the RAI bit for each active channel. The RAI and Na bits are always extracted. The justification indication bits (C_{JK}) along with the justification opportunity bits (J_1-J_4) are extracted when they are treated as overhead (PYLD&JUST bit in the E3 FRMR Maintenance Options register set to logic 0). For each G.751 E3 channel, the order of the overhead bit extraction is shown in Table 13, starting from the top left bit, proceeding to the right.

Table 13 G.751 E3 Receive Overhead Bits

Byte	G.751 E3 Overhead Bits							
	1	2	3	4	5	6	7	8
1	RAI	Na	C11	C21	C31	C41	C12	C22
2	C32	C42	C13	C23	C33	C43	J1	J2
3	J3	J4	N/U	N/U	N/U	N/U	N/U	N/U
4	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U
5	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U
6	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U

The bits in gray in Table 13 may not be valid based on (PYLD&JUST) bit in the E3 FRMR Maintenance Options register; however, the bit position must still be maintained in the overhead sequence. The bit positions marked as N/U in Table 13 must be maintained in the overhead sequence and may be ignored. The ROH stream for a particular channel is invalid when the G.751 E3 frame alignment is lost for that channel.

For G.832 E3 Overhead extraction, ROHFA goes high once every 134 bits to mark the first bit of the FA1 octet for each active channel. For each G.832 channel, the order of the overhead bit extraction is shown in Table 14, starting from the top left FA(1) bit, proceeding to the right, and then to from byte 1 to byte 17 (Note byte 17, is a partial byte).

Table 14 G.832 E3 Receive Overhead Bits

Byte	G.832 E3 Overhead Bits							
	1	2	3	4	5	6	7	8
1	FA1(1)	FA1(2)	FA1(3)	FA1(4)	FA1(5)	FA1(6)	FA1(7)	FA1(8)

Byte	G.832 E3 Overhead Bits							
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
2	FA2(1)	FA2(2)	FA2(3)	FA2(4)	FA2(5)	FA2(6)	FA2(7)	FA2(8)
3	EM(1)	EM(2)	EM(3)	EM(4)	EM(5)	EM(6)	EM(7)	EM(8)
4	TR(1)	TR(2)	TR(3)	TR(4)	TR(5)	TR(6)	TR(7)	TR(8)
5	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U
6	MA(1)	MA(2)	MA(3)	MA(4)	MA(5)	MA(6)	MA(7)	MA(8)
7	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U
8	NR(1)	NR(2)	NR(3)	NR(4)	NR(5)	NR(6)	NR(7)	NR(8)
9	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U
10	GC(1)	GC(2)	GC(3)	GC(4)	GC(5)	GC(6)	GC(7)	GC(8)
11-16	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U
17	N/U	N/U	N/U	N/U	N/U	N/U		

The bit positions marked as N/U in Table 14 must be maintained in the overhead sequence and may be ignored. The ROH stream for a particular channel is invalid when the G.832 E3 frame alignment is lost for that channel.

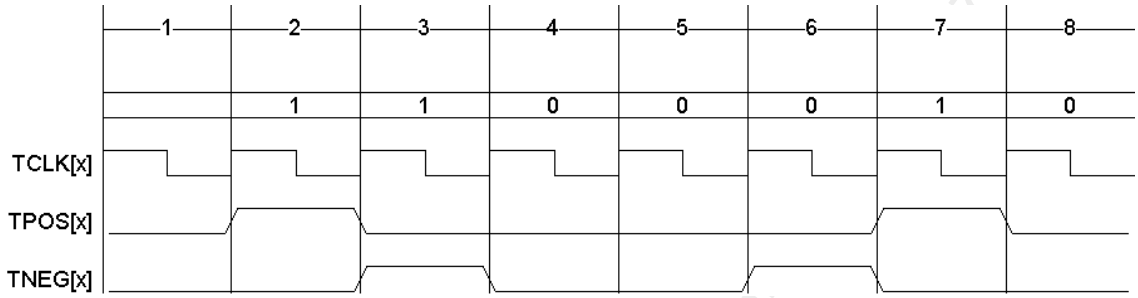
For STS-1E overhead extraction, ROHFA is asserted high once every 72 bits to mark the first bit of the J1 octet for each active channel. For each STS-1E channel, the order of the overhead bit insertion is shown in Table 19, starting from the top left J1 bit, proceeding to the right, and then to from byte 1 to byte 9.

Table 15 STS-1E Receive Overhead Bits

Byte	STS-1E Overhead Bits							
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
1	J1(bit1)	J1(bit2)	J1(bit3)	J1(bit4)	J1(bit5)	J1(bit6)	J1(bit7)	J1(bit8)
2	B3(bit1)	B3(bit2)	B3(bit3)	B3(bit4)	B3(bit5)	B3(bit6)	B3(bit7)	B3(bit8)
3	C2(bit1)	C2(bit2)	C2(bit3)	C2(bit4)	C2(bit5)	C2(bit6)	C2(bit7)	C2(bit8)
4	G1(bit1)	G1(bit2)	G1(bit3)	G1(bit4)	G1(bit5)	G1(bit6)	G1(bit7)	G1(bit8)
5	F2(bit1)	F2(bit2)	F2(bit3)	F2(bit4)	F2(bit5)	F2(bit6)	F2(bit7)	F2(bit8)
6	H4(bit1)	H4(bit2)	H4(bit3)	H4(bit4)	H4(bit5)	H4(bit6)	H4(bit7)	H4(bit8)
7	Z3(bit1)	Z3(bit2)	Z3(bit3)	Z3(bit4)	Z3(bit5)	Z3(bit6)	Z3(bit7)	Z3(bit8)
8	Z4(bit1)	Z4(bit2)	Z4(bit3)	Z4(bit4)	Z4(bit5)	Z4(bit6)	Z4(bit7)	Z4(bit8)
9	Z5(bit1)	Z5(bit2)	Z5(bit3)	Z5(bit4)	Z5(bit5)	Z5(bit6)	Z5(bit7)	Z5(bit8)

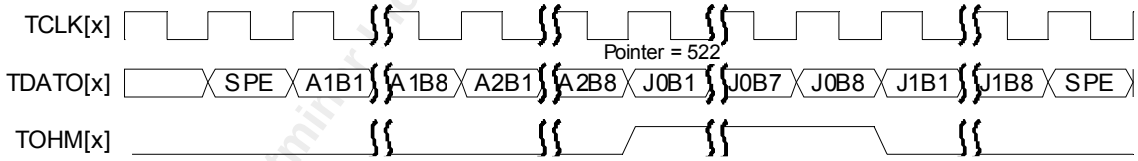
8.3 Transmit PDH Serial Formats

Figure 24 Transmit Bipolar DS3 Stream



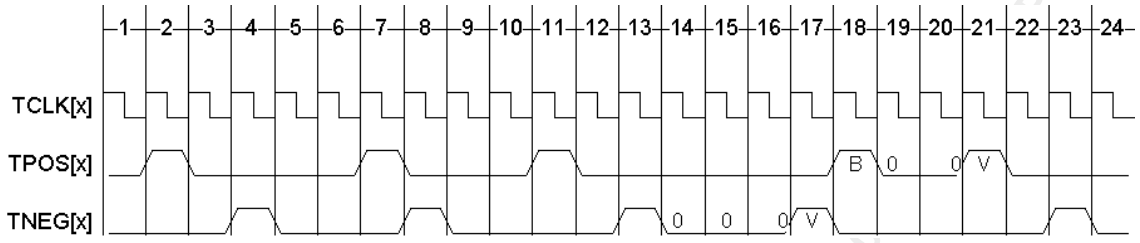
The Transmit Bipolar DS3 Stream diagram (Figure 24) illustrates the generation of a bipolar DS3 stream. The B3ZS encoded DS3 stream is present on TPOS and TNEG. These outputs, along with the transmit clock, TCLK, can be directly connected to a DS3 line interface unit. Note that TCLK is a flow through clock from REFCLK[1:0] or an internally generated clock from the DS3 de-synchronizer (D3E3MD) depending on the mode of operation of that channel.

Figure 25 Transmit Unipolar DS3 Stream



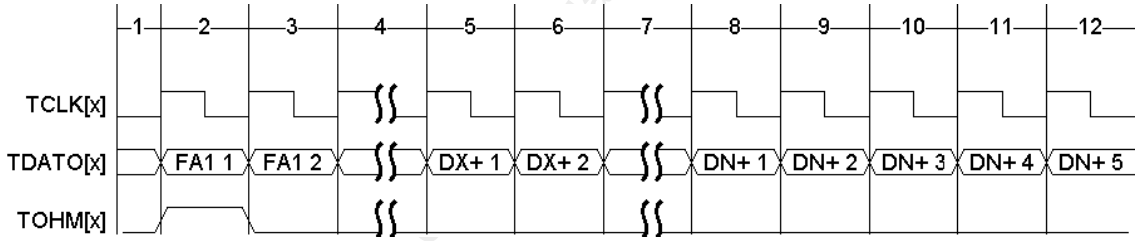
The Transmit Unipolar DS3 Stream diagram (Figure 25) illustrates the unipolar DS3 stream generation. The ATM cell stream, along with valid DS3 overhead bits is contained in TDATO. The TOHM output marks the M-frame boundary (the X1 bit) in the transmit stream. Note that TCLK is a flow through clock from REFCLK[1:0] or an internally generated clock from the DS3 de-synchronizer (D3E3MD) depending on the mode of operation of that channel.

Figure 26 Transmit Bipolar E3 Stream



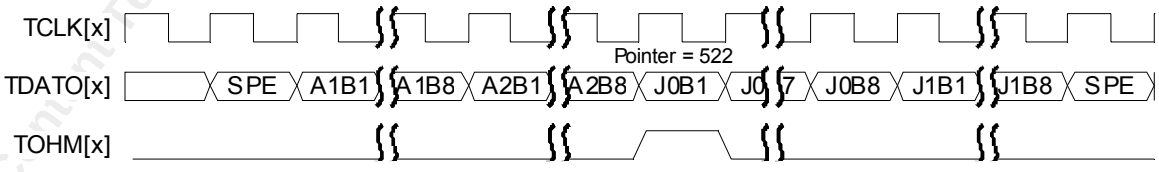
The Transmit Bipolar E3 Stream diagram (Figure 26) illustrates the generation of a bipolar E3 stream. The HDB3 encoded E3 stream is present on TPOS and TNEG (HDB3 Signature Pattern is X00V). These outputs, along with the transmit clock, TCLK, can be directly connected to a E3 line interface unit. Note that TCLK is a flow through clock from REFCLK[1:0] or an internally generated clock from the DS3 de-synchronizer (D3E3MD) depending on the mode of operation of that channel.

Figure 27 Transmit Unipolar E3 Stream



The Transmit Unipolar E3 Stream diagram (Figure 27) illustrates the unipolar E3 stream generation. The ATM cell stream, along with valid E3 overhead bits is contained in TDATO. The TOHM output shown marks the G.832 frame boundary (the first bit of the FA1 frame alignment byte) in the transmit stream. Note that TCLK is a flow through clock from REFCLK[1:0] or an internally generated clock from the DS3 de-synchronizer (D3E3MD) depending on the mode of operation of that channel.

Figure 28 Transmit Unipolar STS-1E Stream



The Transmit Unipolar STS-1E Stream diagram (Figure 28) illustrates the unipolar STS-1E stream generation. The STS-1 SPE along with valid section/line/path overhead bits is contained in TDATO. The TOHM output shown marks the J0 frame boundary (high for all 8 bits of the J0 byte) in the transmit stream.

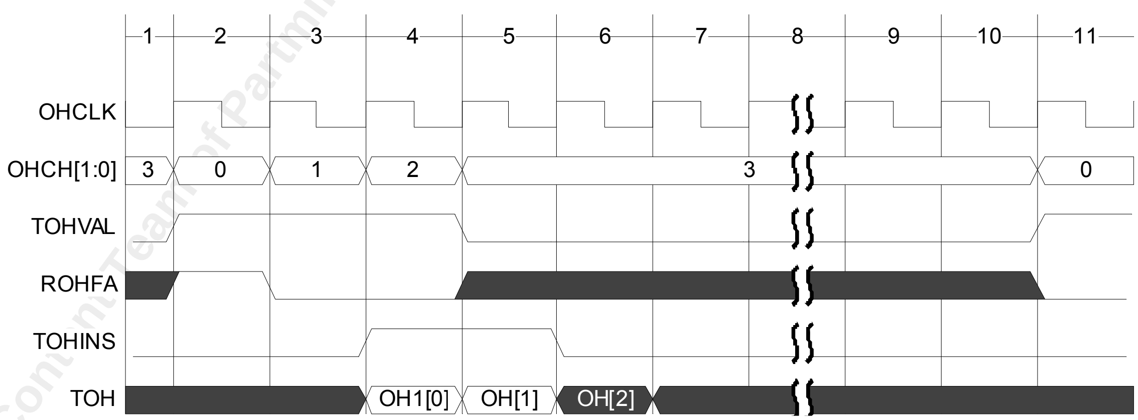
8.4 Transmit PDH Overhead Insertion

On each rising edge of OHCLK, the OHCH[1:0] channel ID increments through three valid channels {0, 1, 2} or waits at invalid channel (3) for 9 cycles. If valid data is available for the channel indicated by OHCH[1:0], then the TOHVAL will be asserted. Otherwise TOHVAL is low and TOHFA is invalid. For each channel, TOHFA signals the beginning of the frame and overhead sequence for the channel in OHCH[1:0].

As shown in Figure 29, if the internal processor for the channel indicated by OHCH[1:0] is ready to receive an overhead bit, then TOHVAL will be high for that cycle. The values on TOH and TOHINS will then be sampled by the ARROW 155 for that channel on the 3rd rising edge of OHCLK after the valid channel cycle began. If the sampled value of TOHINS for that channel is high, then the sampled value of TOH will be used to overwrite the current overhead bit. If TOHINS is low, the default overhead bit for that position is used. TOHFA signal will be high when the bit being requested is the first bit of that channel's overhead sequence. TOHFA will be low otherwise. When TOHVAL is low, TOHFA is invalid in the current cycle, and TOH and TOHINS are not sampled in the 3rd cycle.

DS3 and E3 overhead insertion is input on the TOHINS and TOH pins. Because different channels may be processing different overhead types, Figure 29 depicts the generic operation of the receive overhead extraction interface. In Figure 29, OH1[X], on TOH, depicts the first overhead bit for a given channel [X]. Other overhead bits are shown as OH[X] where X is the channel. The order in which the overhead bits are extracted is discussed below.

Figure 29 Overhead Insertion



For each DS3 channel, the order of the overhead bit insertion is as shown in Table 16, starting from the top left X1 bit, proceeding to the right, and then from sub-frame 1 to sub-frame 7. TOHFA is asserted once every 56 bits to mark the X1 bit for each active channel.

Table 16 DS3 Transmit Overhead Bits

M-subframe	DS3 Overhead Bits							
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
1	X_1	F_1	C_1	F_2	C_2	F_3	C_3	F_4
2	X_2	F_1	C_1	F_2	C_2	F_3	C_3	F_4
3	P_1	F_1	C_1	F_2	C_2	F_3	C_3	F_4
4	P_2	F_1	C_1	F_2	C_2	F_3	C_3	F_4
5	M_1	F_1	C_1	F_2	C_2	F_3	C_3	F_4
6	M_2	F_1	C_1	F_2	C_2	F_3	C_3	F_4
7	M_3	F_1	C_1	F_2	C_2	F_3	C_3	F_4

For transmit G.751 E3 overhead insertion, TOHFA is asserted once every 48 bits to mark the RAI bit for each active channel. For each G.751 E3 channel, the order of overhead bit insertion is shown in Table 17, starting from the top left bit, proceeding to the right and then down.

Table 17 G.751 E3 Transmit Overhead Bits

Byte	G.751 E3 Overhead Bits							
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
1	RAI	Na	C11	C21	C31	C41	C12	C22
2	C32	C42	C13	C23	C33	C43	J1	J2
3	J3	J4	N/U	N/U	N/U	N/U	N/U	N/U
4	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U
5	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U
6	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U

The bit positions marked as N/U in Table 17 must be maintained in the overhead sequence and may be ignored. The PYLD&JUST bit in the E3 TRAN Status and Diagnostics Options register has no affect on the insertion of the justification service and the tributary justification bits through the TOH and the TOHINS inputs.

For G.832 E3 overhead insertion, TOHFA is asserted high once every 134 bits to mark the first bit of the FA1 octet for each active channel. For each G.832 channel, the order of the overhead bit insertion is shown in Table 18, starting from the top left FA(1) bit, proceeding to the right, and then to from byte 1 to byte 17 (Note byte 17 is a partial byte).

Table 18 G.832 E3 Transmit Overhead Bits

Byte	G.832 E3 Overhead Bits							
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
1	FA1(1)	FA1(2)	FA1(3)	FA1(4)	FA1(5)	FA1(6)	FA1(7)	FA1(8)
2	FA2(1)	FA2(2)	FA2(3)	FA2(4)	FA2(5)	FA2(6)	FA2(7)	FA2(8)
3	EM(1)	EM(2)	EM(3)	EM(4)	EM(5)	EM(6)	EM(7)	EM(8)
4	TR(1)	TR(2)	TR(3)	TR(4)	TR(5)	TR(6)	TR(7)	TR(8)

Byte	G.832 E3 Overhead Bits							
	1	2	3	4	5	6	7	8
5	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U
6	MA(1)	MA(2)	MA(3)	MA(4)	MA(5)	MA(6)	MA(7)	MA(8)
7	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U
8	NR(1)	NR(2)	NR(3)	NR(4)	NR(5)	NR(6)	NR(7)	NR(8)
9	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U
10	GC(1)	GC(2)	GC(3)	GC(4)	GC(5)	GC(6)	GC(7)	GC(8)
11-16	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U
17	N/U	N/U	N/U	N/U	N/U	N/U		

The bit positions marked as N/U in Table 18 must be maintained in the overhead sequence and may be ignored. Also note that the EM byte behaves as an error mask, that is the binary value sampled on TOH in the EM byte location is not inserted directly into the transmit overhead but, rather, the value is XORed with the calculated BIP-8 and inserted in the transmit overhead.

For STS-1E overhead insertion, TOHFA is asserted high once every 72 bits to mark the first bit of the J1 octet for each active channel. For each STS-1E channel, the order of the overhead bit insertion is shown in Table 19, starting from the top left J1 bit, proceeding to the right, and then to from byte 1 to byte 9. Note that the B3 byte serves as an error mask for the internally calculated B3 byte.

Table 19   STS-1E Transmit Overhead Bits

Byte	STS-1E Overhead Bits							
	1	2	3	4	5	6	7	8
1	J1(bit1)	J1(bit2)	J1(bit3)	J1(bit4)	J1(bit5)	J1(bit6)	J1(bit7)	J1(bit8)
2	B3(bit1)	B3(bit2)	B3(bit3)	B3(bit4)	B3(bit5)	B3(bit6)	B3(bit7)	B3(bit8)
3	C2(bit1)	C2(bit2)	C2(bit3)	C2(bit4)	C2(bit5)	C2(bit6)	C2(bit7)	C2(bit8)
4	G1(bit1)	G1(bit2)	G1(bit3)	G1(bit4)	G1(bit5)	G1(bit6)	G1(bit7)	G1(bit8)
5	F2(bit1)	F2(bit2)	F2(bit3)	F2(bit4)	F2(bit5)	F2(bit6)	F2(bit7)	F2(bit8)
6	H4(bit1)	H4(bit2)	H4(bit3)	H4(bit4)	H4(bit5)	H4(bit6)	H4(bit7)	H4(bit8)
7	Z3(bit1)	Z3(bit2)	Z3(bit3)	Z3(bit4)	Z3(bit5)	Z3(bit6)	Z3(bit7)	Z3(bit8)
8	Z4(bit1)	Z4(bit2)	Z4(bit3)	Z4(bit4)	Z4(bit5)	Z4(bit6)	Z4(bit7)	Z4(bit8)
9	Z5(bit1)	Z5(bit2)	Z5(bit3)	Z5(bit4)	Z5(bit5)	Z5(bit6)	Z5(bit7)	Z5(bit8)

8.5 Add TelecomBus

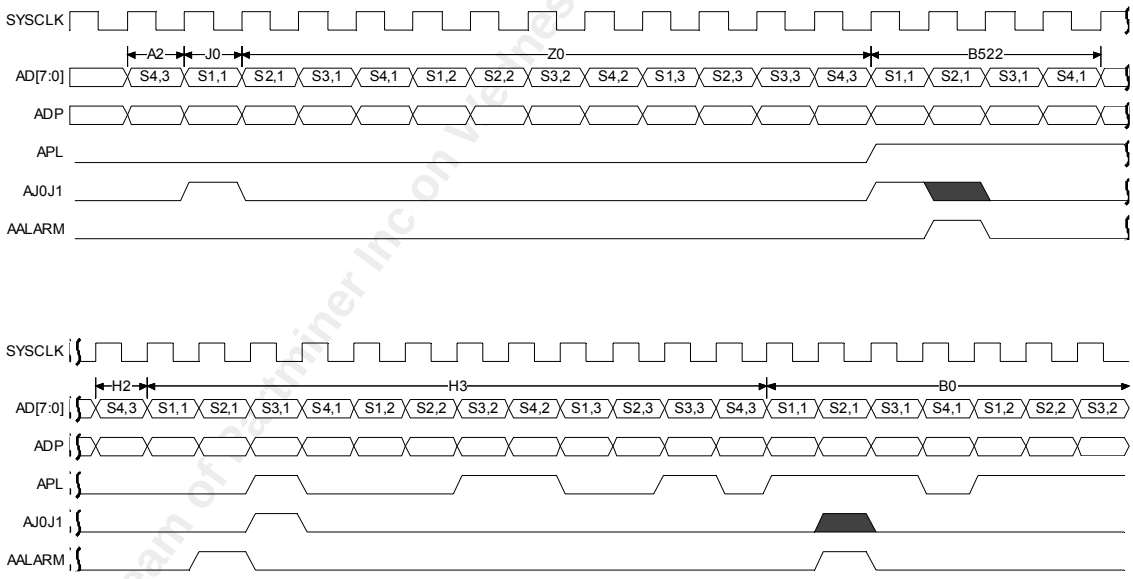
Figure 30 shows the timing of the Add TelecomBus interface. Timing is provided by SYSCLK. SONET/SDH data is carried in the AD[7:0]. The bytes are arranged in order of transmission in an STS-12/STM-4 stream (unless re-ordered in the Add STSI. Each transport/section overhead byte is labeled by Sx,y and type. Payload bytes are labeled by Sx,y and Bn, where ‘n’ is the active offset of the byte.

A timeslot naming strategy and assignment on an AD[7:0] bus is shown in Figure 30. Within Sx,y, the STS-3/STM-1 number is given by 'x' and the column number within the STS-3/STM-1 is given by 'y'. The APL signal is set high to mark payload bytes and is set low at all other bytes. The composite transport frame and payload frame signal AJ0J1 is set high with APL set low to mark the J0 byte of a transport frame. AJ0J1 is set high with APL also set high to mark the J1 byte of all the streams within AD[7:0].

High order streams in AIS alarm are indicated by the AALARM signal.

In Figure 30, timeslots numbers S1,x, S2,y, and S4,z are configured as STS-1/STM-0 operation. Timeslot number S3,n is configured for STS-3c/STM-1 operation. Stream S1,1 (STM-1 #1, AU3 #1) is shown to have an active offset of 522 by the high level on APL and AJ0J1 at byte S1,1/B522. Stream S2,1 (STM-1 #2, AU3 #1) is shown to be in high-order path AIS (AALARM set high at bytes S2,1/Z0, S2,1/B522, S2,1/H3 and S2,1/B0). STM-1 #3 is configured in AU4 mode and is shown to undergo a negative pointer justification event, changing its active offset from 0 to 782. This is shown by AJ0J1 being set high at byte S3,1/H3 and APL being set high at bytes S3,1/H3, S3,2/H3 and S3,3/H3.

Figure 30 Add Parallel TelecomBus Timing



8.6 Drop TelecomBus

Figure 31 shows the timing of the Drop TelecomBus interface. Timing is provided by SYSCLK. SONET/SDH data is carried in the DD[7:0]. The bytes are arranged in order of reception in an STS-12/STM-4 stream (unless re-ordered in the Drop STSI.

The timeslot naming strategy and assignment is shown in Figure 31. Each transport/section overhead byte is labeled by Sx,y and type. Payload bytes are labeled by Sx,y and Bn, where 'n' is the active offset of the byte. Within Sx,y, the STS-3/STM-1 number is given by 'x' and the column number within the STS-3/STM-1 is given by 'y'. The DPL signal is set high to mark payload bytes and is set low at all other bytes. The DJ0J1 signal is set high with the DPL signal set low to mark the J0 byte of a transport frame. DJ0J1 is set high with DPL also set high to mark the J1 byte of each of the streams within DD[7:0]. High order streams in alarm are indicated by the DALARM signal. For Figure 31 DJ0DLY[13:0] is set to 0x0000.

In Figure 31, timeslots S1,x, S2,y, and S4,z are configured for STS-1/STM-0 operation. Timeslot S3,n is configured for STS-3c/STM-1 operation. Stream S1,1 (STM-1 #1, AU3 #1) is shown to have an active offset of 522 by the high level on DPL and DJ0J1 at byte S1,1/B522. Stream S2,1 (STM-1 #2, AU3 #1) is shown to be in high-order path alarm (DALARM set high at bytes S2,1/Z0, S2,1/B522, S2,1/H3 and S2,1/B0). STM-1 #3 is a configured in AU4 mode and is shown to undergo a negative pointer justification event, changing its active offset from 0 to 782. This is shown by DJ0J1 being set high at byte S3,1/H3 and DPL being set high at bytes S3,1/H3, S3,2/H3 and S3,3/H3. Stream S4,1 is shown to undergo a positive pointer justification event as indicated by the low level on DPL at byte S4,1/B0.

Figure 31 Drop TelecomBus (J1SQUELCH = 0)

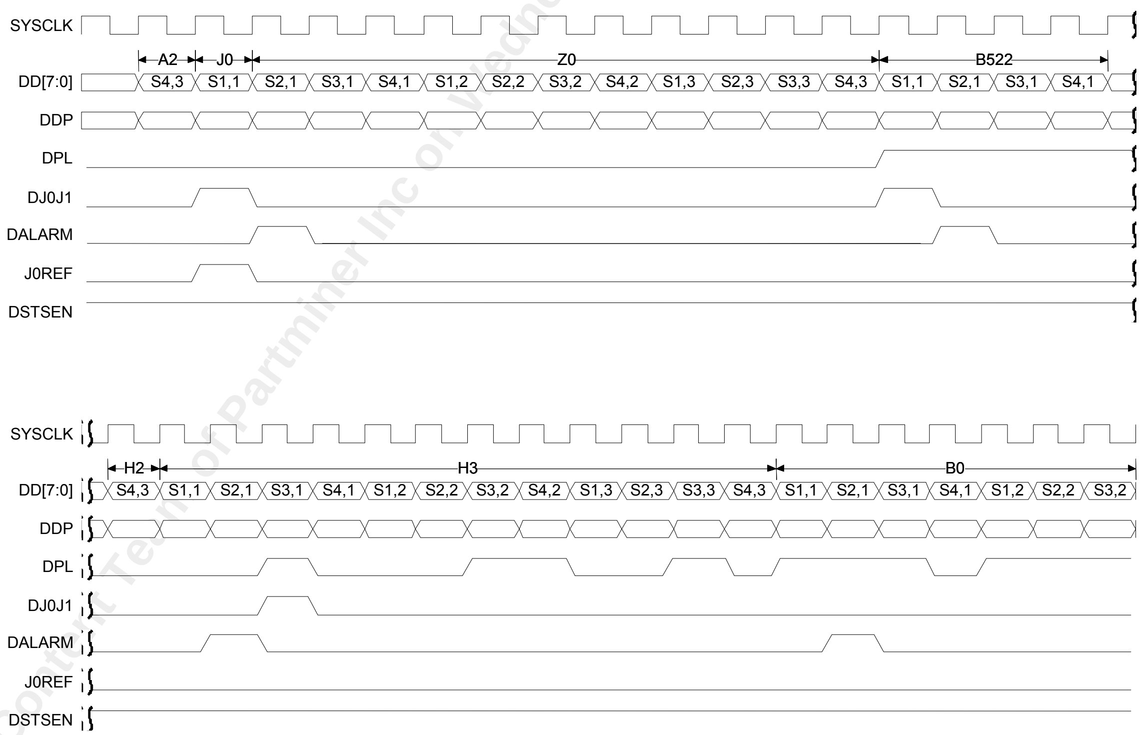
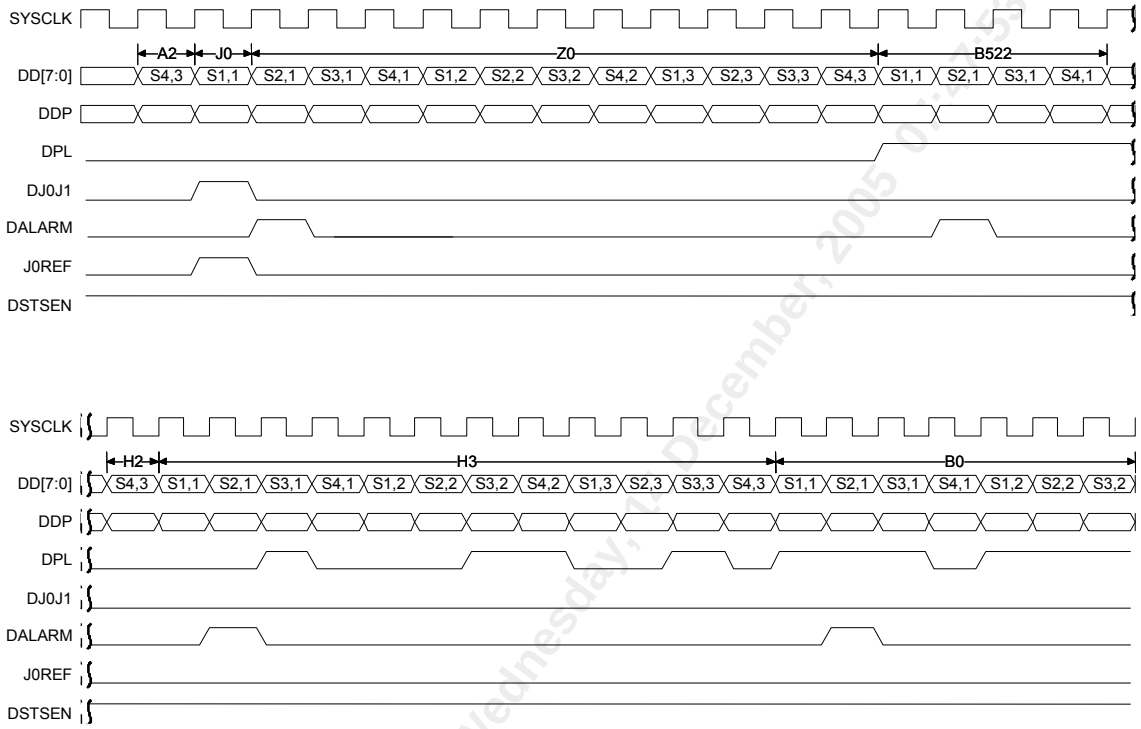


Figure 32 is like Figure 31 except that the J1SQUELCH bit is set to 1 to allow only a single J0 framing pulse on DJ0J1. This mode is useful when the TelecomBus sink is expecting to extract J1 markers from the H1/H2 pointer bytes.

Figure 32 Drop TelecomBus (J1SQUELCH = 1)



8.7 Receive SONET Transport Overhead

Figure 33 RTOH Output Timing (OC-12 Mode)

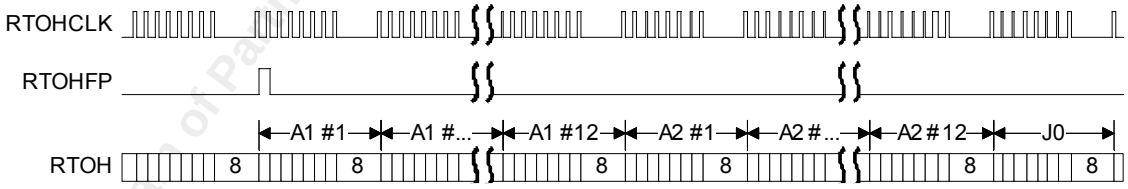


Figure 34 RTOH Output Timing (OC-3 Mode)

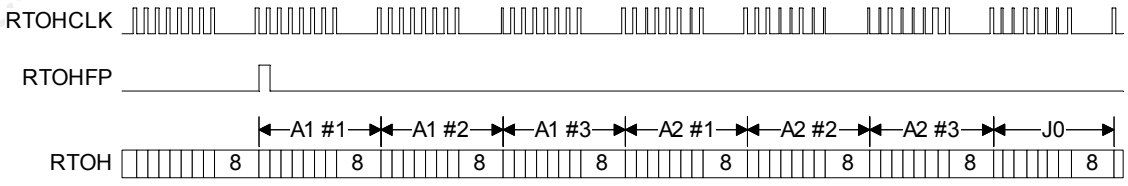


Figure 35 RTOH and RTOHFP Output Timing

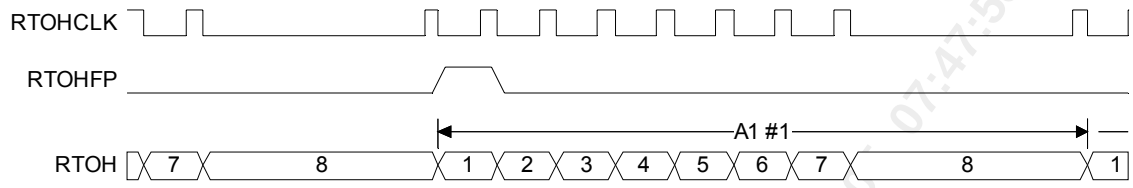


Figure 33 shows the receive transport overhead (RTOH) functional timings in OC-12 mode. RTOHCLK is a 20.736 MHz clock generated by gapping a 25.92 MHz clock (33% high duty cycle). 2592 bits (9x3x12 bytes) are output on RTOH between two RTOHFP assertions.

Figure 34 shows the receive transport overhead (RTOH) functional timings in OC-3 mode. RTOHCLK is a 5.184 MHz clock generated by gapping a 6.48 MHz clock (33% high duty cycle). 648 bits (9x3x3 bytes) are output on RTOH between two RTOHFP assertions.

Figure 35 shows that RTOH and RTOHFP are aligned with the falling edge of RTOHCLK. The rising edge of RTOHCLK should be used to sample RTOH and RTOHFP. Sampling RTOHFP high identifies the MSB of the first A1 byte on RTOH.

8.8 Receive SONET Section and Line DCC

Figure 36 RTOHFP and RSLD output timing (RSLDSEL = 0)

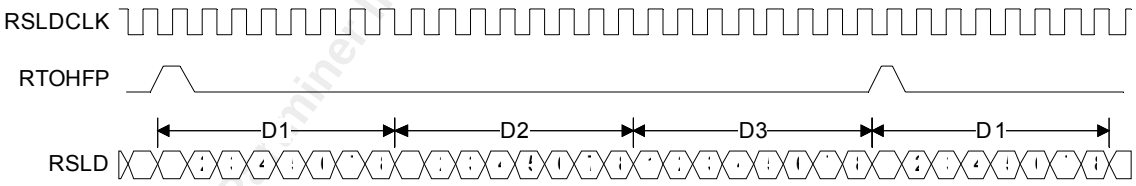


Figure 37 RTOHFP and RSLD Output Timing (RSLDSEL = 1)

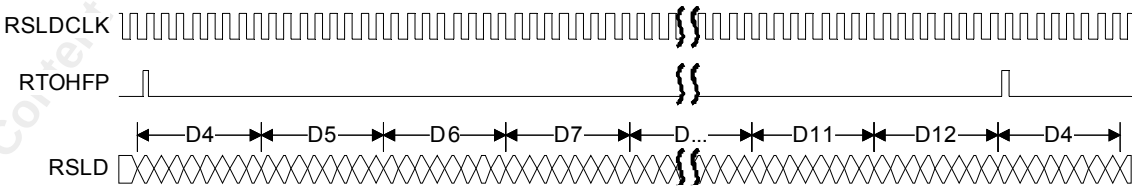


Figure 36 and Figure 37 show the receive section/line DCC (RSLD) functional output timing. When RSLDSEL is set to zero, RSLD and RSLDCLK are carrying the section DCC bytes (D1-D3). When RSLDSEL is set to one, RSLD and RSLDCLK are carrying the line DCC bytes (D4-D12).

RSLDCLK is a 192 kHz clock when carrying the section DCC and a 576 kHz clock when carrying the line DCC. RSLD is aligned with the falling edge of RSLDCLK. The rising edge of RSLDCLK should be used to sample RSLD and RTOHFP. Sampling RTOHFP high identifies the MSB of the D1 or D4 byte on the RSLD output.

8.9 Receive SONET Path Overhead Port

Figure 38 shows the receive path overhead (RPOH) functional timing. The RPOH port (RPOH, RPOHEN, and B3E) is used to output the POH bytes of the STS (VC) payloads and the path BIP-8 errors. The POH bytes are output on RPOH MSB first in the same order that they are received. Since RPOHFP is synchronized on the transport frame, zero, one, or two path overhead can be output per path per frame. RPOHEN is used to indicate new POH bytes on RPOH. RPOHEN is either asserted or de asserted for the nine POH bytes. The path BIP-8 errors are output on B3E at the same time the path trace byte is output on RPOH. Optionally, block BIP-8 errors can be output on B3E.

Note that RPOHEN will be asserted to validate zero, one, or two opportunities per path per frame out of three opportunities. RPOHEN opportunities will alternate from path to path and from frame to frame based on pointer movement.

Figure 38 shows that RPOH and RPOHEN are aligned with the falling edge of RPOHCLK. The rising edge of RPOHCLK should be used to sample RPOH and RPOHEN. Sampling RPOHFP high identifies the MSB of the path trace byte of STS-1/STM-0 #1 on RPOH and the first possible path BIP-8 error of STS-1/STM-0 #1 on B3E.

Figure 38 RPOH Output Timing

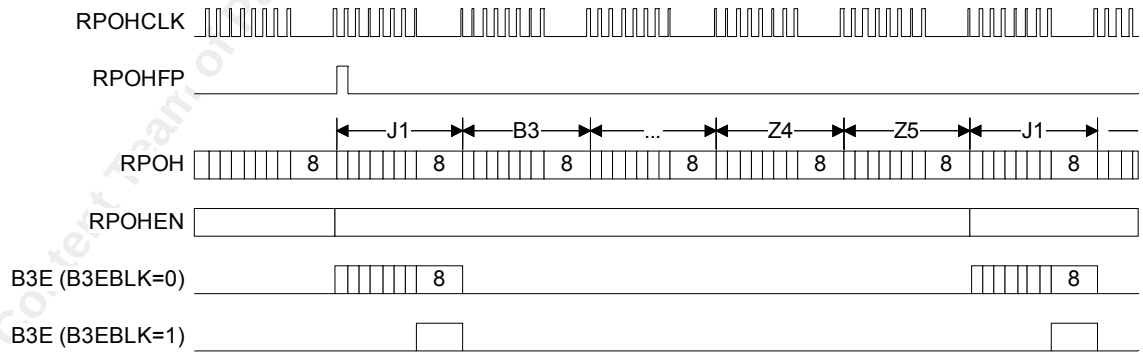
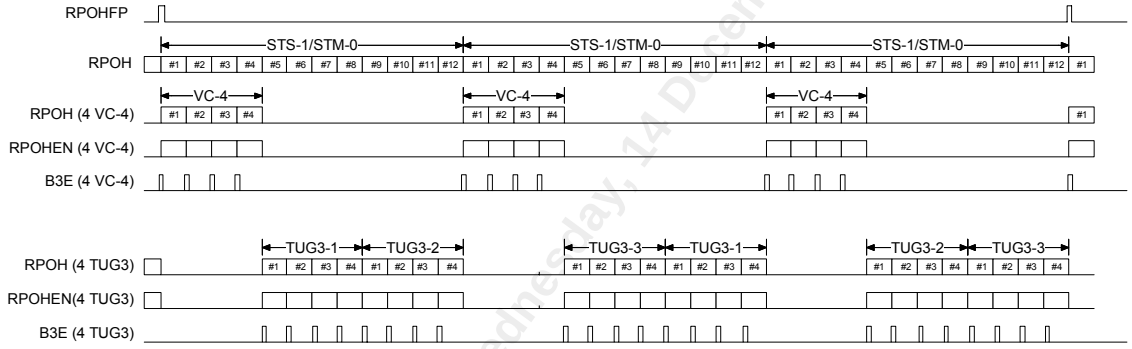


Figure 39 shows the STS-1/STM-0 time slots assignment on RPOH. Since RPOHFP is synchronized on the transport frame, zero, one, or two path overhead can be output per path per frame. To avoid loosing any POH bytes, three time slots are assigned per path per frame. In STS (AU) mode, the time slots are repeatedly assigned from STS-1/STM-0 #1 to #12. Figure 39 shows the case of a STM-4 data stream carrying four VC-4 payloads. Only the master VC-4 STS-1/STM-0 time slots contain valid POH bytes. Figure 39 also includes the case of four VC-4 payloads carrying four TUG3 payloads. Both the master and the slave VC-4 STS-1/STM-0 time slots contain valid POH bytes (the master timeslots contain the VC-4 POH and the slave timeslots contain the VC-3 POH). If the ARROW 155 is configured for STS-3c/STM-1(AU-4/VC-4) operation, timeslots 2,3,4,6,7,8,10,11, and 12 do not contain valid information.

Figure 39 RPOH STS-1/STM-0 Time Slots Output Timing



8.10 Transmit SONET Transport Overhead

Figure 40 TTOH and TTOHEN Input Timing

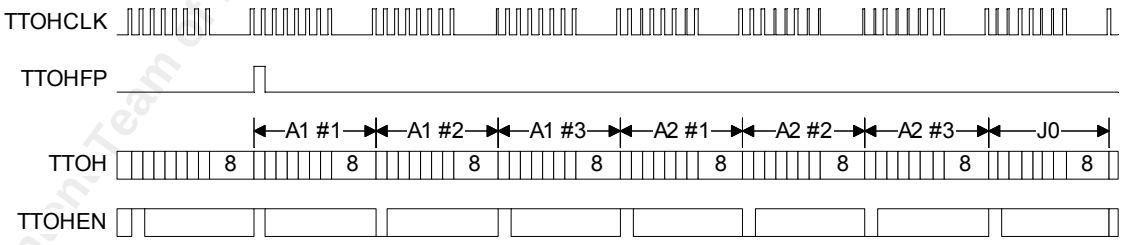


Figure 41 TTOH and TTOHFP Input Timing

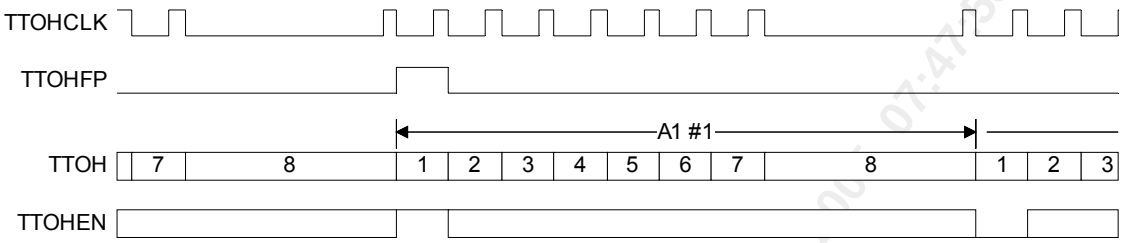


Figure 40 shows the transmit transport overhead (TTOH) functional timings. TTOHCLK is a 5.184 MHz clock generated by gapping a 6.48 MHz clock (33% high duty cycle). 648 bits (9x3x3 bytes) are input on TTOH between two TTOHFP assertions.

TTOHEN is used to validate the insertion of the corresponding byte on TTOH. When TTOHEN is sampled high on the MSB of the byte, the byte will be inserted in the transport overhead. When TTOHEN is sampled low on the MSB of the byte, the byte is not inserted. TTOH and TTOHEN are sampled with the rising edge of TTOHCLK. TTOHFP is aligned with the falling edge of TTOHCLK. The rising edge of TTOHCLK should be used to sample TTOHFP. Sampling TTOHFP high identifies the MSB of the first A1 byte on TTOH.

8.11 Transmit SONET Section and Line DCC

Figure 42 TTOHFP and TSLD Output Timing (TSLDSEL = 0)

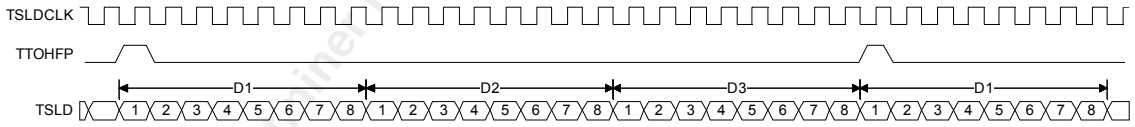


Figure 43 TTOHFP and TSLD Output Timing (TSLDSEL = 1)

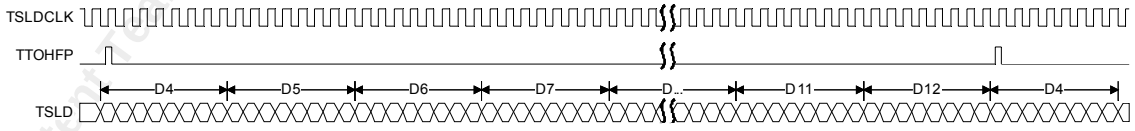


Figure 42 and Figure 43 show the transmit section/line DCC (TSLD) functional input timing. When TSLDSEL is set to zero, TSLD and TSLDCLK are carrying the section DCC bytes (D1-D3). When TSLDSEL is set to one, TSLD and TSLDCLK are carrying the line DCC bytes (D4-D12).

TSLDCLK is a 192 kHz clock when carrying the section DCC and a 576 kHz clock when carrying the line DCC. TSLD is sampled with the rising edge of TSLDCLK. TSLDCLK is generated such that the rising edge of TSLDCLK can be used by external logic to sample TTOHFP with proper setup and hold time. Sampling TTOHFP high identifies the MSB of the D1 or D4 byte on TSLD.

8.12 Transmit SONET Path Overhead

Figure 44 shows the transmit path overhead (TPOH) functional timing. The TPOH port (TPOH, TPOHEN, and TPOHRDY) is used to input the POH bytes of the STS (VC) payloads. The POH bytes are input on TPOH MSB first in the same order that they are transmit. Since TPOHFP is synchronized on the transport frame, zero, one, or two path overhead can be input per path per frame.

TPOHRDY is asserted to indicate that the ARROW 155 is ready to receive POH bytes. If the TPOH input is used, the POH byte must be validated with TPOHEN at every TPOHRDY request (zero, once or twice per frame). Otherwise invalid data may be inserted. TPOHEN is used to validate the insertion of the corresponding byte on TPOH. If TPOHRDY is logic high and TPOHEN is sampled high on the MSB of the byte, the byte will be inserted in the path overhead. When TPOHEN is sampled low on the MSB of the byte, the byte is not inserted in the output stream. If TPOHRDY is logic low and TPOHEN is sample high on the MSB of the byte, the byte will not be inserted in the path overhead and must be represented at the next opportunity.

TPOH and TPOHEN are sampled with the rising edge of TPOHCLK. TPOHRDY is aligned with the falling edge of TPOHCLK. The rising edge of TPOHCLK should be used to sample TPOHRDY. Sampling TPOHFP high identifies the MSB of the path trace byte of STS-1/STM-0 #1 on TPOH.

Figure 44 TPOH Input Timing

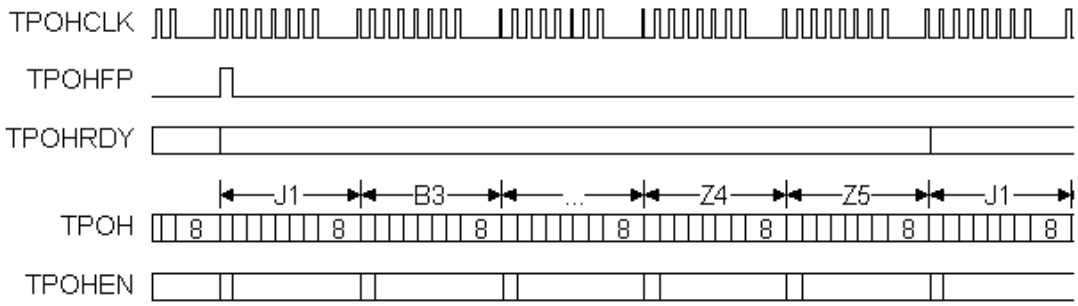
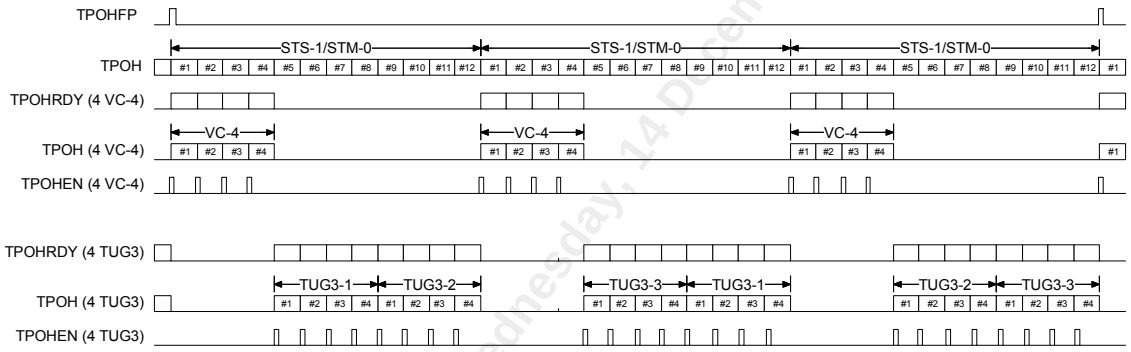


Figure 45 shows the STS-1/STM-0 time slots assignment on TPOH. Since TPOHFP is synchronized on the transport frame, zero, one, or two path overhead can be input per path per frame. To avoid loosing any POH bytes, three time slots are assigned per path per frame. In STS (AU) mode, the time slots are repeatedly assigned from STS-1/STM-0 #1 to #12. Figure 45 shows the case of a STM-4 data stream carrying four VC-4 payloads. Only the master VC-4 STS-1/STM-0 time slots contain valid POH bytes (the master timeslots contain the VC-4 POH and the slave timeslots contain the VC-3 POH). Figure 45 also includes the case of four VC-4 payloads carrying four TUG3 payloads. Both the master and the slave VC-4 STS-1/STM-0 time slots contain valid POH bytes. Because the ARROW 155 processes only STS-3/STM-1 worth of traffic, timeslots 2,3,4,6,7,8,10,11 and 12 will be discarded.

Figure 45 TPOH STS-1/STM-0 Time Slots Input Timing



8.13 Receive Ring Control Port

Figure 48 shows the receive ring control port (RRCP) functional timing. RRCPDAT serially outputs all the section, line, and path defects detected in the receive data stream. Since RPOHFP is synchronized on the transport frame, two path overheads are output per path per frame.

RRCPDAT is aligned with the falling edge of RPOHCLK. The rising edge of RPOHCLK should be used to sample RRCPDAT. Sampling RPOHFP high with RPOHCLK identifies the OOF defect on RRCP. Table 20 defines RRCP in function of the bit position. In order to maintain compatibility with the ARROW 622,bit positions for timeslots 2, 3, 4, 6, 7, 8, 10, 11, 12 are present, but invalid.

Figure 46 RRCP Output Timing

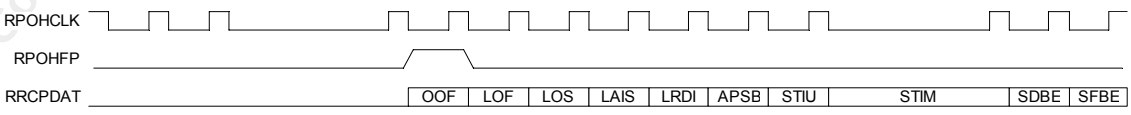


Table 20 Ring Control Port Bit Definition

Bit Position	Type	Defect
1	Section	OOF
2	Section	LOF
3	Section	LOS
4	Section	LAIS
5	Section	LRDI
6	Section	APSBF
7	Section	STIU
8	Section	STIM
9	Section	SDBER
10	Section	SFBER
11-12	Section	GROWTH[1:0]
13-16	Section	0
17-32	Section	APS[15:0]
33-40	Section	LBIPCNT[7:0]
41	Section	LRDIINS
42-64	Section	0
65	Path	PLOP
66	Path	PAIS
67	Path	PPLU
68	Path	PPLM
69	Path	PUNEQ
70	Path	PPDI
71	Path	PRDI
72	Path	PERDI
73-75	Path	PERDIV[2:0]
76	Path	PTIU
77	Path	PTIM
78-79	Path	PGROWTH[1-0]
80	Path	0
81-84	Path	PBIPCNT[3:0]
85-87	Path	PERDIINS[2:0]
88-96	Path	0
97-128	Path	STS-1/STM-0 #2
...	...	...
417-448	Path	STS-1/STM-0 #12
449-480	TU3 Path	TU3 STS-1/STM-0 #1
...	...	...
801-832	TU3 Path	TU3 STS-1/STM-0 #12
833-864	Path	STS-1/STM-0 #1

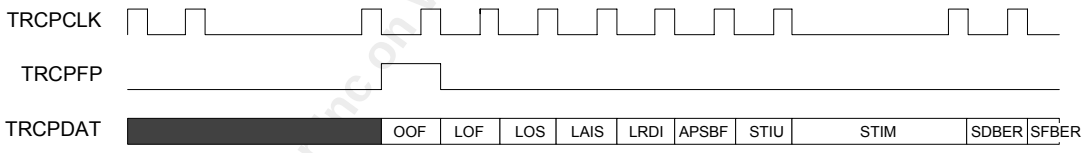
Bit Position	Type	Defect
...	...	...
1185-1216	Path	STS-1/STM-0 #12
1217-1248	TU3 Path	TU3 STS-1/STM-0 #1
...	...	...
1569-1600	TU3 Path	TU3 STS-1/STM-0 #12
1601-2592	None	0

8.14 Transmit Ring Control Port

Figure 47 shows the transmit ring control port (TRCP) functional timing. TRCPDAT serially inputs all the section, line, and path defects detected in the receive data stream. The TRCP port is usually connected to the RRCP port of a mate ARROW device. TRCP is not restricted to a RRCP port as long as the format and the timings between TRCPCLK, TRCPFP, and TRCPDAT are met.

Sampling TRCPFP high with TRCPCLK identifies the OOF defect on TRCPDAT. TRCPFP must be asserted to initiate TRCPDAT capture. Only the first 1600 bits, after TRCPFP assertion, are considered valid and part of the ring control port. Table 20 defines TRCPDAT in function of the bit position.

Figure 47 TRCP Input Timing



9 Power

9.1 Normal Operating Conditions

Table 21 Normal Operating Voltages for 0.18 um CMOS

	Operating Range[1]			Reference (approx.)
Supply Voltages	**Minimum (V)**	**Typical (V)**	**Maximum (V)**	
1.8V Core Supply Voltage (VDDI)	1.71	1.80	1.89	+/- 5%
1.8V Analog Supply Voltage (AVDL1, AVDL2)	1.71	1.80	1.89	+/- 5%
3.3V Analog Supply Voltage (AVDH, AVD1)	3.13	3.3	3.47	+/- 5%
3.3V I/O Supply Voltage (VDDO)	3.13	3.3	3.47	+/- 5%

Note

1. Power supply, D.C. characteristics, and A.C. timing are characterized across these operating ranges, unless otherwise stated.

9.2 Power Consumption

Table 22 Power Requirements

Conditions	Parameter	Typ	High	Max	Units
OC-12 Operation Mode	IDDOP (VDDI)	0.4729	—	0.6177	A
	IDDOP (VDDO)	0.0936	—	0.1272	A
	IDDOP (AVDL)	0.0847	—	0.1417	A
	IDDOP (AVDH)	0.0118	—	0.0141	A
	Total Power	1.352	1.687	—	W
OC-3 Operation Mode	IDDOP (VDDI)	0.4321	—	0.5695	A
	IDDOP (VDDO)	0.0695	—	0.1085	A
	IDDOP (AVDL)	0.0827	—	0.1386	A
	IDDOP (AVDH)	0.0122	—	0.0140	A
	Total Power	1.196	1.525	—	W

Typ = Mean, High = Mean+2*Sigma, Max = Mean+6*Sigma

Notes:

1. Outputs loaded with 30 pF, and a normal amount of traffic or signal activity.

2. Power values are calculated using the formula:

   Power = ∑ i (VDD x IDD)

   Where i denotes all the various power supplies on the device, VDD is the voltage for supply i in accordance with the condition, and IDD is the current for supply i.

Table 23 Conditions for Power Requirements

	Typical	Power For Thermal Calulations	Maximum Current
Process	Nominal	Nominal +2 sigmas of process variation*	Nominal +6 sigmas of process variation
Voltage	Nominal Vdd	Maximum Operating Vdd	Maximum Vdd
Temperature	Tj=75C	Tj=105C	T=125C

* The power number for nominal process + 2 sigma of process variation is recommended for thermal calculations as it will be highest power dissipation of all parts in almost all applications.

10 Thermal Information

10.1 Package and Thermals

This product is designed to operate over a wide temperature range when used with a heat sink and is suited for outside plant equipment[1].

Table 24 Package and Thermal Information

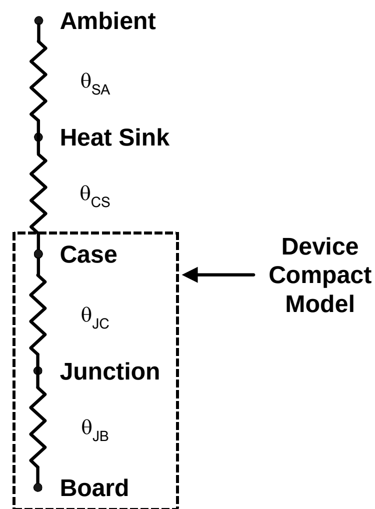
Package	[package]
Maximum long-term operating junction temperature (T_J) to ensure adequate long-term life.	105 °C
Maximum junction temperature (T_J) for short-term excursions with guaranteed continued functional performance[2]. This condition will typically be reached when the local ambient temperature reaches 85 °C.	125°C
Minimum ambient temperature (T_A)	-40 °C

Table 25 Device Compact Model[3]

Junction-to-Case Thermal Resistance, θ_{JC}	4.61 °C/W
Junction-to-Board Thermal Resistance, θ_{JB}	12.43 °C/W

Table 26 Heat Sink Requirements

$\theta_{SA}+\theta_{CS}$[4]	The sum of θ_{SA} + θ_{CS} must be less than or equal to: $[(105 - T_A) / P_D] - \theta_{JC}]$ °C/W where: T_A is the ambient temperature at the heat sink location P_D is the operating power dissipated in the package[5]
	θ_{SA} and θ_{CS} are required for long-term operation



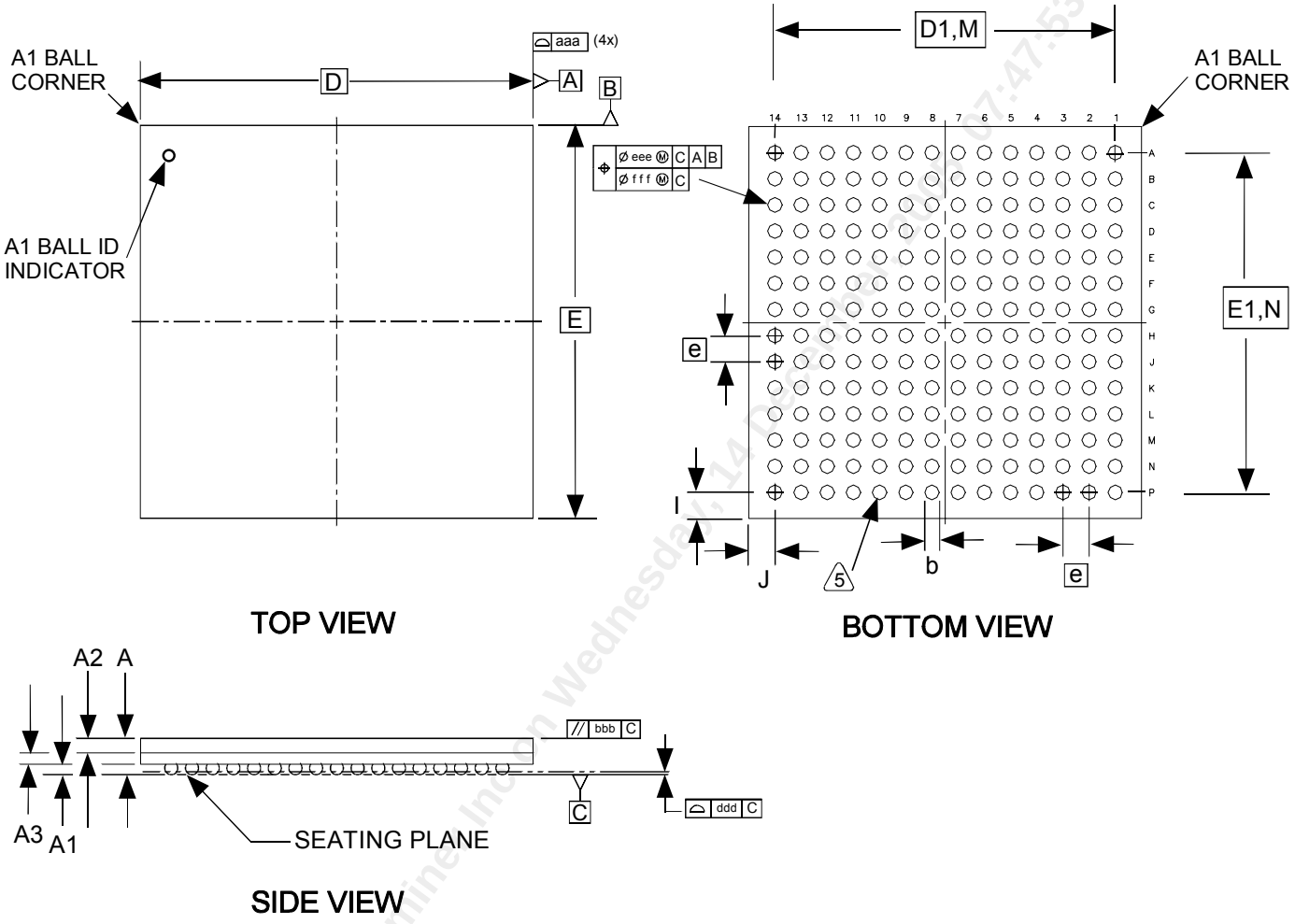
Notes

1. The minimum ambient temperature requirement for Outside Plant Equipment meets the minimum ambient temperature requirement for Industrial Equipment
2. Short-term is used as defined in Telcordia Technologies Generic Requirements GR-63-Core Core; for more information about this standard, see Telcordia Technologies. Network Equipment-Building System (NEBS) Requirements: Physical Protection: Telcordia Technologies Generic Requirements GR-63-CORE. Issue 1. October 1995.
3. θJC, the junction-to-case thermal resistance, is a measured nominal value plus two sigma. θJB, the junction-to-board thermal resistance, is obtained by simulating conditions described in JEDEC Standard JESD 51-8; for more information about this standard, see Electronic Industries Alliance 1999. Integrated Circuit Thermal Test Method Environmental Conditions -Junction-to-Board: JESD51-8. October 1999.

4. θSA is the thermal resistance of the heat sink to ambient. θCS is the thermal resistance of the heat sink attached material. The maximum θSA required for the airspeed at the location of the device in the system with all components in place.

Power depends upon the operating mode.

11 Package Specification



NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES PACKAGE BODY PROFILE.
3) DIMENSION bbb DENOTES PARALLEL.
4) DIMENSION ddd DENOTES COPLANARITY.
5) SOLDER MASK OPENING 0.435 +/- 0.03 MM DIAMETER (SMD).
6) PACKAGE COMPLIANT TO JEDEC REGISTERED OUTLINE MO-192, VARIATION AAE-1.

PACKAGE TYPE : 196 CHIP ARRAY BALL GRID ARRAY - CABGA																		
BODY SIZE : 15 x 15 x 1.40 MM																		
Dim.	A	A_1	A_2	A_3	D	D_1	E	E_1	M,N	I	J	b	e	aaa	bbb	ddd	eee	f f f
Min.	1.30	0.31	0.65	0.34	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Nom.	1.40	0.36	0.70	0.34	15.00 BSC	13.00 BSC	15.00 BSC	13.00 BSC	14x14	1.00	1.00	0.46	1.00 BSC	-	-	-	-	-
Max.	1.50	0.41	0.75	0.34	-	-	-	-	-	-	-	-	-	0.10	0.10	0.12	0.15	0.08

12 DC Characteristics

T_a = -40°C to T_j = 125°C, V_{DDI} = $VDDI_{typical}$ ± 5%, V_{DDO} = $VDDO_{typical}$ ± 5%, AVDL = $AVDL_{typical}$ ± 5%, AVDH = $AVDH_{typical}$ ± 5%

Typical Conditions: T_a = 25°C, VDDI = 1.8V, VDDO = 3.3V, AVDH = 3.3V, AVDL = 1.8V

Table 27 DC Characteristics for Pins

Symbol	Parameter	Min (V)	Typ (V)	Max (V)	Conditions
VIL	Input Low Voltage	-0.5	—	0.8	Guaranteed Input LOW Voltage
VIH	Input High Voltage	2.0	—	VDDO+0.5	Guaranteed Input HIGH Voltage
VOL	Output or Bidirectional Low Voltage	—	0.1	0.4	VDDO = min, IOL = 8 mA[3]
VOH	Output or Bidirectional High Voltage	2.4	2.7	—	VDDO = min, IOH = 8 mA[3]

Table 28 DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{T+}	Reset Input High Voltage	2.0	—	—	Volts	TTL Schmitt
V_{T-}	Reset Input Low Voltage	—	—	0.8	Volts	TTL Schmitt
V_{TH}	Reset Input Hysteresis Voltage	—	0.5	—	Volts	TTL Schmitt
I_{ILPU}	Input Low Current	+20	+83	+200	µA	VIL = GND[1,3]
I_{IHPU}	Input High Current	-10	0	+10	µA	VIH = VDDO[1,3]
I_{IL}	Input Low Current	-10	0	+10	µA	VIL = GND[2,3]
I_{IH}	Input High Current	-10	0	+10	µA	VIH = VDDO[2,3]
C_{IN}	Input Capacitance	—	5	—	pF	Excluding Package, Package Typically 2 pF
C_{OUT}	Output Capacitance	—	5	—	pF	Excluding Package, Package Typically 2 pF
C_{IO}	Bidirectional Capacitance	—	5	—	pF	Excluding Package, Package Typically 2 pF
I_{DDQ}	IDDQ Current Draw (CSU_AVDL2 only)	35	45	90	nA	Total current from CSU_AVDL2 digital supply
P_{D_MABC}	SONET Analog Block Power Down	—	—	60	mW	Prime contributor is CSU622 block

Symbol	Parameter	Min	Typ	Max	Units	Conditions
	Dissipation					
V_{PECL}	PECL 100E Differential Levels	1.19	1.50	1.86	Vppd	
V_{RXID}	RX Differential Input Voltage Range	0.2	—	2.0	Vppd	
$V_{RXREFID}$	RXREF Differential Input Voltage Range	0.2	—	2.0	Vppd	
$V_{IH-PECL}$	RXD, RXREF, PECL Input Logic High Level	-1.16	-0.95	-0.88	V	Referenced to VCC (2.5V, 3.3V, for RXREF also 5V) .
$V_{IL-PECL}$	RXD, RXREF, PECL Input Logic Low Level	-1.81	-1.70	-1.48	V	Referenced to VCC (2.5V, 3.3V, for RXREF also 5V)
V_{TXOD}	TXD Differential Output Voltage Range	1.1	1.4	1.6	Vppd	Differentially terminated with 100 Ohm +/-1%

Notes

1. Input pin or bi-directional pin with internal pull-up resistor.
2. Input pin or bi-directional pin without internal pull-up resistor.
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).

13 AC Timing Characteristics

13.1 General

Figure 48 RSTB Timing

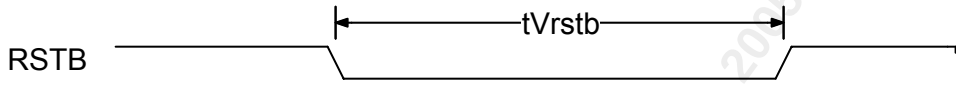


Table 29 RSTB Timing (Figure 70)

Symbol	Description	Min	Typ	Max	Units
tV_{RSTB}	RSTB Pulse Width	—	100	—	ns

13.2 Microprocessor Interface

Figure 49 Microprocessor Interface Read Timing

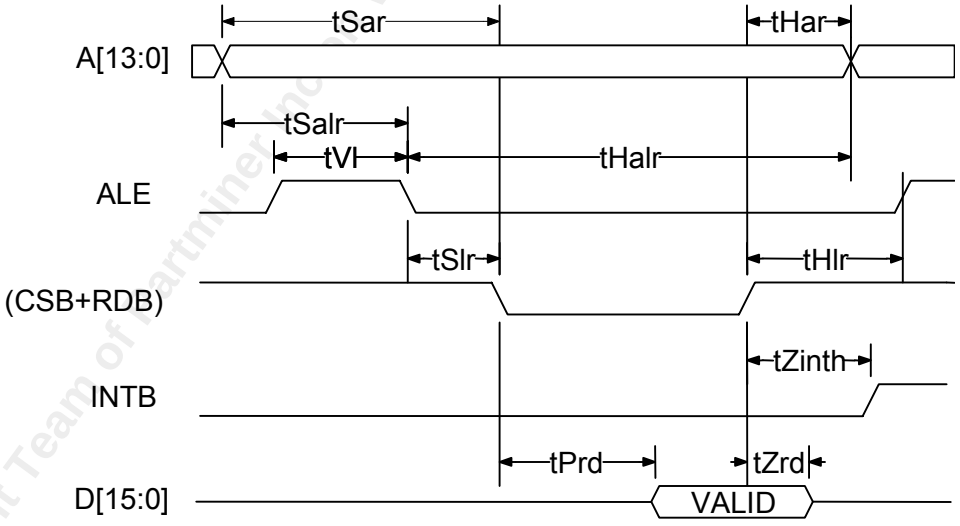


Table 30 Microprocessor Interface Read Access (Figure 49)

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	10	—	ns
tH_{AR}	Address to Valid Read Hold Time[5]	5	—	ns

Symbol	Parameter	Min	Max	Units
tS_{ALR}	Address to Latch Set-up Time[4]	10	—	ns
tH_{ALR}	Address to Latch Hold Time[4]	10	—	ns
tV_{L}	Valid Latch Pulse Width[4]	5	—	ns
tS_{LR}	Latch to Read Set-up[4]	0	—	ns
tH_{LR}	Latch to Read Hold[4]	5	—	ns
tP_{RD}	Valid Read to Valid Data Propagation Delay	—	70	ns
tZ_{RD}	Valid Read Negated to Output Tri-state	—	20	ns
tZ_{INTH}	Valid Read Negated to Output Tri-state	—	50	ns

Notes on Microprocessor Interface Read Timing

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[15:0]).
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALR}, tH_{ALR}, tV_{L}, tS_{LR}, and tH_{LR} are not applicable.
5. Parameter tH_{AR} is not applicable if address latching is used.
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Figure 50 Microprocessor Interface Write Timing

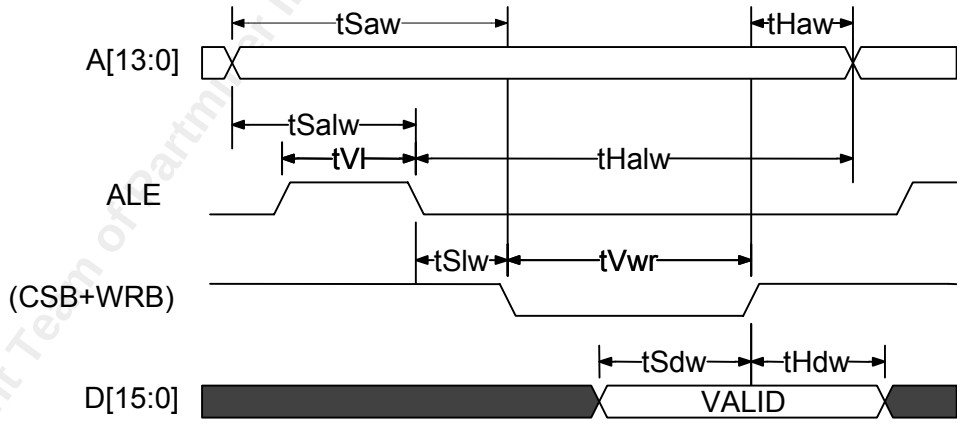


Table 31 Microprocessor Interface Write Access (Figure 50)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	10	—	ns

Symbol	Parameter	Min	Max	Units
tS_{DW}	Data to Valid Write Set-up Time	20	—	ns
tS_{ALW}	Address to Latch Set-up Time[2]	10	—	ns
tH_{ALW}	Address to Latch Hold Time[2]	10	—	ns
tV_{L}	Valid Latch Pulse Width[2]	5	—	ns
tS_{LW}	Latch to Write Set-up[2]	0	—	ns
tH_{LW}	Latch to Write Hold[2]	5	—	ns
tH_{DW}	Data to Valid Write Hold Time	5	—	ns
tH_{AW}	Address to Valid Write Hold Time[3]	5	—	ns
tV_{WR}	Valid Write Pulse Width	40	—	ns

Notes on Microprocessor Interface Write Timing

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.
2. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALW}, tH_{ALW}, tV_{L}, tS_{LW}, and tH_{LW} are not applicable.
3. Parameter tH_{AW} is not applicable if address latching is used.
4. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
5. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

13.3 PECL Line Interface Timing

Table 32 PECL Line Interface Timing

Symbol	Parameter	Min	Max	Units
$F_{REFCLK(155)}$	Frequency of REFCLK_P/N (155MHz Mode)	155.517	155.523	MHz
$F_{REFCLK(77)}$	Frequency of REFCLK_P/N	77.759	77.762	MHz
D_{REFCLK}	Duty Cycle for REFCLK_P/N	40	60	%
J_{REFCLK}	Jitter on REFCLK_P/N	—	4	ps (rms)

13.4 PDH Reference Clock Timing

Table 33 PDH Reference Clock Timing

Symbol	Description	Min	Typ	Max	Units
tR_{PDHREF}	Rise time for PDHREFCLK[1:0]	—	—	1	ns
tF_{PDHREF}	Fall Time for PDHREFCLK[1:0]	—	—	1	ns
tD_{PDHREF}	PDHREFCLK[1:0] Duty Cycle	40	50	60	%
$F_{PDHREF(DS3)}$	PDHREFCLK[1:0] Frequency for DS3	—	44.736	52	MHz
$F_{PDHREF(E3)}$	PDHREFCLK[1:0] Frequency for E3	—	34.368	52	MHz
$F_{PDHREF(STS-1E)}$	PDHREFCLK[1:0] Frequency for STS-1E	—	51.840	52	MHz

13.5 TelecomBus Interface Timing

Figure 51 Drop TelecomBus Interface Timing

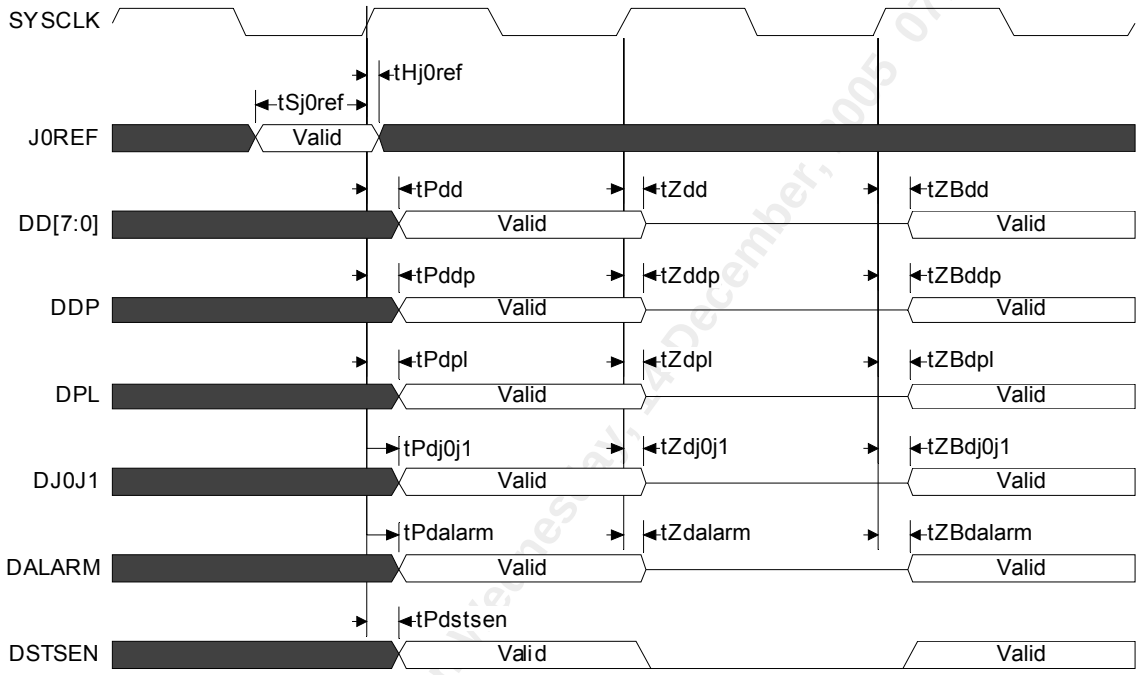


Table 34 Drop TelecomBus Interface (Figure 51)

Symbol	Description	Min	Typical	Max	Units
F_{SYSCLK}	SYSCLK Frequency	77.76	77.76	77.76	MHz
D_{SYSCLK}	SYSCLK Duty Cycle	40	50	60	%
tS_{J0REF}	J0REF Setup time to SYSCLK	2.5	—	—	ns
tH_{J0REF}	J0REF Hold time to SYSCLK	0	—	—	ns
tP_{DD}	SYSCLK High to DD[7:0] Valid	1	—	5	ns
tZ_{DD}	SYSCLK High to DD[7:0] Tri-state	1	—	5	ns
tZB_{DD}	SYSCLK High to DD[7:0] Driven	1	—	—	ns
tP_{DDP}	SYSCLK High to DDP Valid	1	—	5	ns
tZ_{DDP}	SYSCLK High to DDP Tri-state	1	—	5	ns
tZB_{DDP}	SYSCLK High to DDP Driven	1	—	—	ns
tP_{DPL}	SYSCLK High to DPL Valid	1	—	5	ns
tZ_{DPL}	SYSCLK High to DPL Tri-state	1	—	5	ns
tZB_{DPL}	SYSCLK High to DPL Driven	1	—		ns
tP_{DJ0J1}	SYSCLK High to DJ0J1 Valid	1	—	5	ns
tZ_{DJ0J1}	SYSCLK High to DJ0J1 Tri-state	1	—	5	ns

Symbol	Description	Min	Typical	Max	Units
tZB_{DJ0J1}	SYSCLK High to DJ0J1 Driven	1	—		ns
tP_{DALARM}	SYSCLK High to DALARM Valid	1	—	5	ns
tZ_{DALARM}	SYSCLK High to DALARM Tri-state	1	—	5	ns
tZB_{DALARM}	SYSCLK High to DALARM Driven	1	—	—	ns
tP_{STSEN}	SYSCLK High to DSTSEN Valid	1	—	5	ns

Figure 52 Add TelecomBus Interface Timing

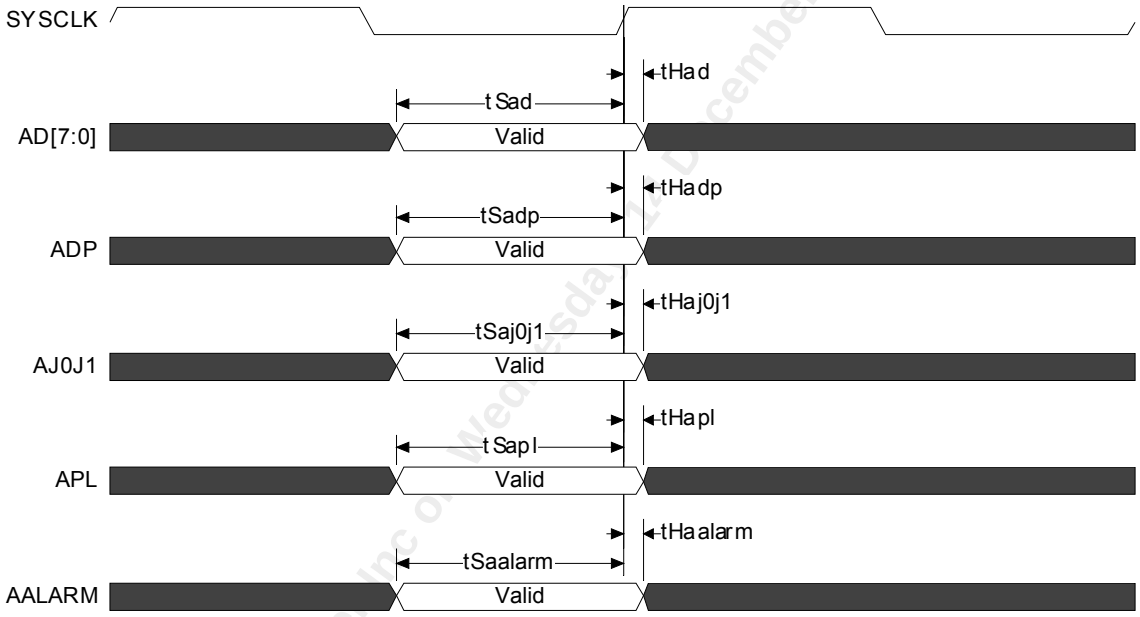


Table 35 Add TelecomBus Interface (Figure 52)

Symbol	Description	Min	Typical	Max	Units
tS_{AD}	AD[7:0] Setup time to SYSCLK	2.5	—	—	ns
tH_{AD}	AD[7:0] Hold time to SYSCLK	0	—	—	ns
tS_{ADP}	ADP Setup time to SYSCLK	2.5	—	—	ns
tH_{ADP}	ADP Hold time to SYSCLK	0	—	—	ns
tS_{AJ0J1}	AJ0J1 Setup time to SYSCLK	2.5	—	—	ns
tH_{AJ0J1}	AJ0J1 Hold time to SYSCLK	0	—	—	ns
tS_{APL}	APL Setup time to SYSCLK	2.5	—	—	ns
tH_{APL}	APL Hold time to SYSCLK	0	—	—	ns
tS_{AALARM}	AALARM Setup time to SYSCLK	2.5	—	—	ns
tH_{AALARM}	AALARM Hold time to SYSCLK	0	—	—	ns

Notes on Input Timing

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.
3. This parameter is guaranteed by design. No production tests are done on this parameter.
4. High pulse width is measured from the 1.4 Volt points of the rise and fall ramps. Low pulse width is measured from the 1.4 Volt points of the fall and rise ramps.

Notes on Output Timing

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum output propagation delays are measured with a 30 pF load on the outputs. Minimum output propagation delays are measured with a 0 pF load on the outputs.

13.6 SONET/SDH Overhead Interface Timing

Figure 53 Transmit SONET/SDH Overhead Interface Timing

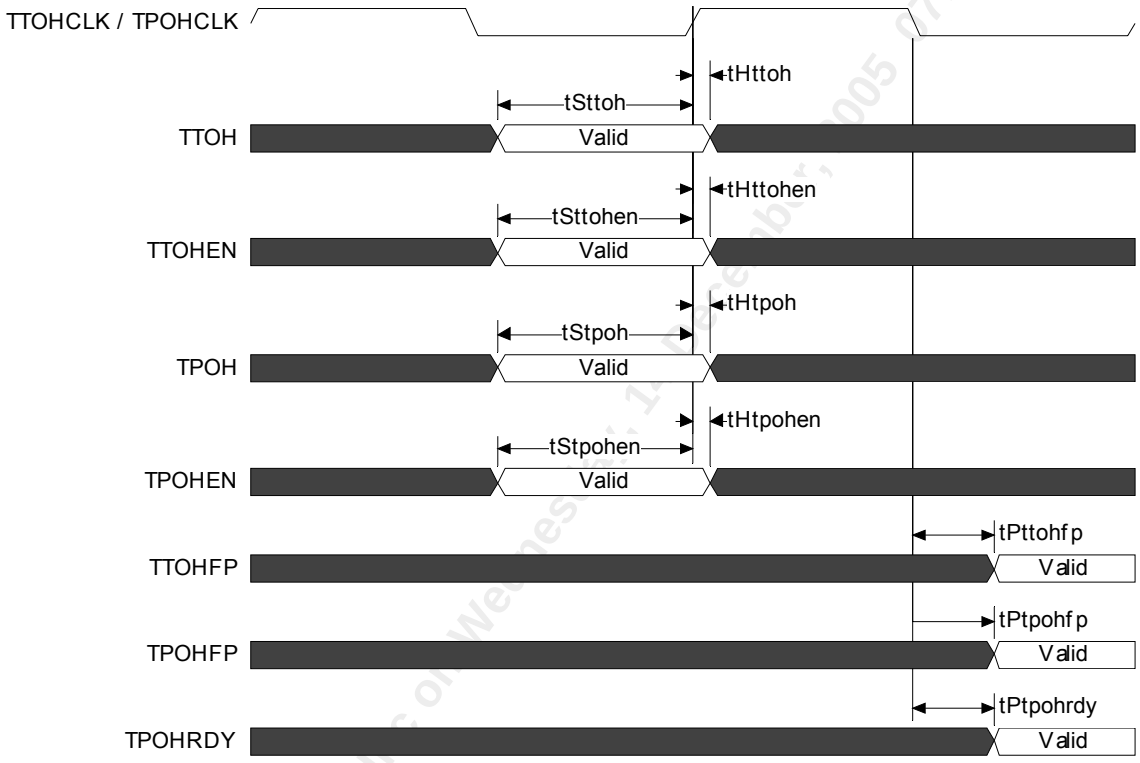


Table 36 Transmit SONET/SDH Overhead TTOH/TPOH Interface (Figure 53)

Symbol	Description	Min	Typical	Max	Units
tS_{TTOH}	TTOH Setup time to TTOHCLK rising edge	14	—	—	ns
tH_{TTOH}	TTOH Hold time to TTOHCLK rising edge	0	—	—	ns
tS_{TTOHEN}	TTOHEN Setup time to TTOHCLK rising edge	14	—	—	ns
tH_{TTOHEN}	TTOHEN Hold time to TTOHCLK rising edge	0	—	—	ns
tS_{TPOH}	TPOH Setup time to TPOHCLK rising edge	14	—	—	ns
tH_{TPOH}	TPOH Hold time to TPOHCLK rising edge	0	—	—	ns
tP_{TTOHFP}	TTOHCLK falling edge to TTOHFP Valid	-7	—	7	ns
tP_{TPOHFP}	TPOHCLK falling edge to TPOHFP Valid	-7	—	7	ns
tP_{TPOHEN}	TPOHCLK falling edge to TPOHEN Valid	-7	—	7	ns
$tP_{TPOHRDY}$	TPOHCLK falling edge to TPOHRDY Valid	-7	—	7	ns

Figure 54 Transmit SONET/SDH Overhead Interface Timing

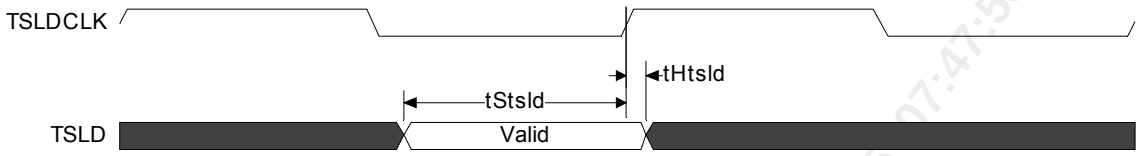


Table 37 Transmit SONET/SDH Overhead TSLDCLK Interface (Figure 54)

Symbol	Description	Min	Typical	Max	Units
tS_{TSLD}	TSLD Setup time to TTOHCLK rising edge	14	—	—	ns
tH_{TSLD}	TSLD Hold time to TTOHCLK rising edge	0	—	—	ns

Figure 55 Transmit Ring Control Input Timing Diagram

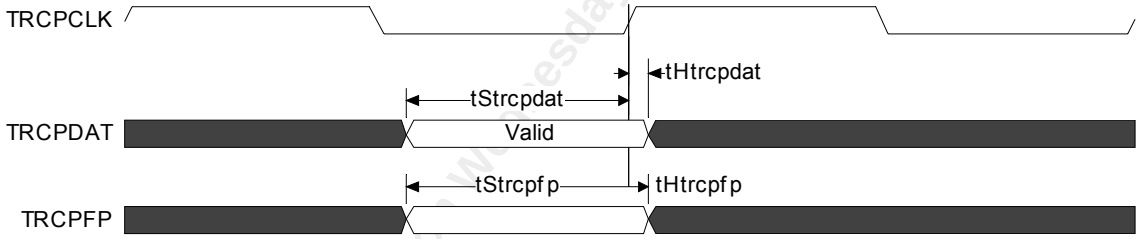


Table 38 Transmit Ring Control Input Timing

Symbol	Description	Min	Max	Units
	TRCPCLK frequencies	12.8	66	MHz
	TRCPCLK duty cycle	40	60	%
tS_{TRCPFP}	TRCPFP Set-up time to TRCPCLK rising edge	10	—	ns
tH_{TRCPFP}	TRCPFP Hold time to TRCPCLK rising edge	5	—	ns
$tS_{TRCPDAT}$	TRCPDAT Set-up time to TRCPCLK rising edge	10	—	ns
$tH_{TRCPDAT}$	TRCPDAT Hold time to TRCPCLK rising edge	5	—	ns

Figure 56 Receive SONET/SDH Overhead RTOH/RPOH Interface Timing

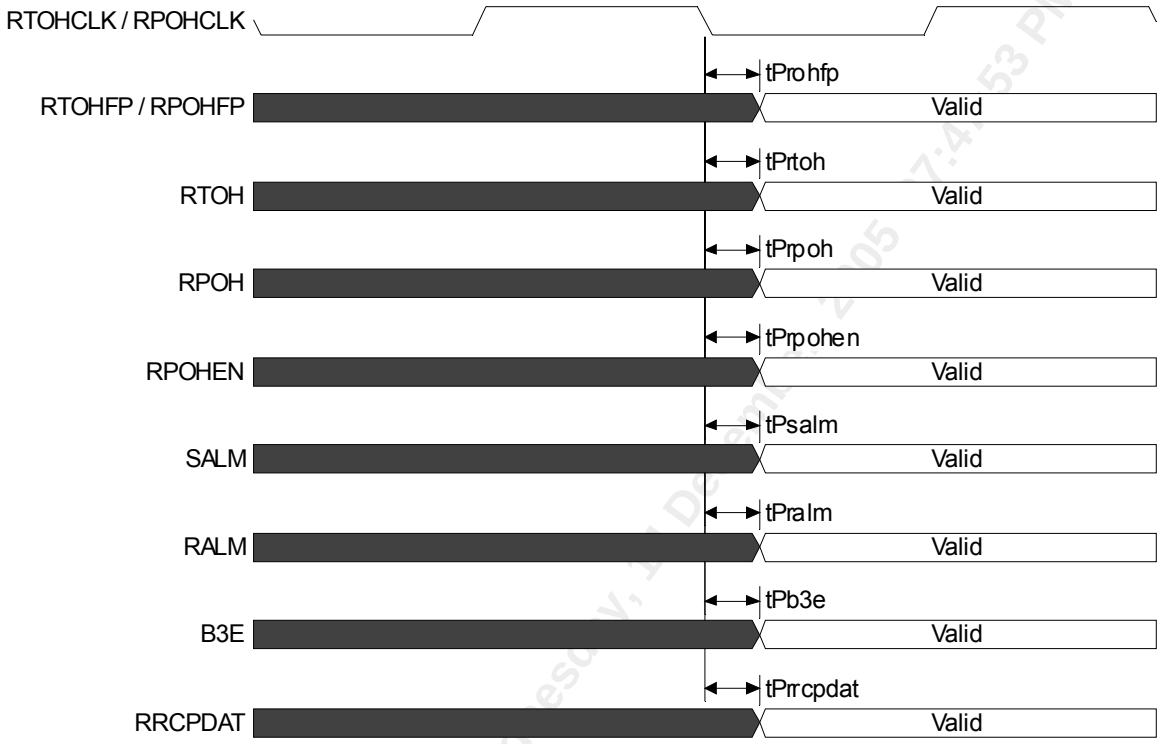


Table 39 Receive SONET/SDH Overhead RTOH/RPOH Interface (Figure 55)

Symbol	Description	Min	Typical	Max	Units
tP_{RTOHFP}	RTOHCLK falling edge to RTOHFP Valid	-7	—	7	ns
tP_{RPOHFP}	RPOHCLK falling edge to RPOHFP Valid	-7	—	7	ns
tP_{RTOH}	RTOHCLK falling edge to RTOH Valid	-7	—	7	ns
tP_{RPOH}	RPOHCLK falling edge to RPOH Valid	-7	—	7	ns
tP_{RPOHEN}	RPOHCLK falling edge to RPOHEN Valid	-7	—	7	ns
tP_{SALM}	RPOHCLK falling edge to SALM Valid	-7	—	7	ns
tP_{RALM}	RPOHCLK falling edge to RALM Valid	-7	—	7	ns
tP_{B3E}	RPOHCLK falling edge to B3E Valid	-7	—	7	ns
$tP_{RRCPDAT}$	RPOHCLK falling edge to RRCPDAT valid	-7	—	7	ns

Figure 57 Receive SONET/SDH Overhead RSLDCLK Interface Timing

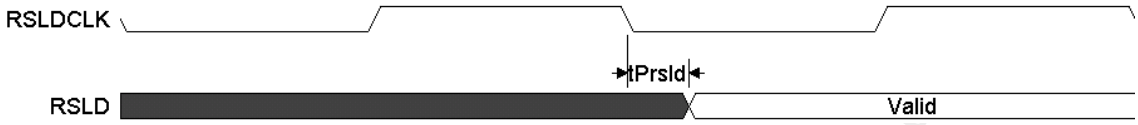


Table 40 Receive SONET/SDH Overhead RSLDCLK Interface (Figure 57)

Symbol	Description	Min	Typical	Max	Units
tP_{RSLD}	RSLDCLK falling edge to RSLD Valid	-7	—	—	ns

Notes on Input Timing

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.
3. This parameter is guaranteed by design. No production tests are done on this parameter.
4. High pulse width is measured from the 1.4 Volt points of the rise and fall ramps. Low pulse width is measured from the 1.4 Volt points of the fall and rise ramps.

Notes on Output Timing

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum and minimum output propagation delays are measured with a 30 pF load on the outputs.

13.7 PDH Interface Timing

Figure 58 Transmit PDH Interface Timing

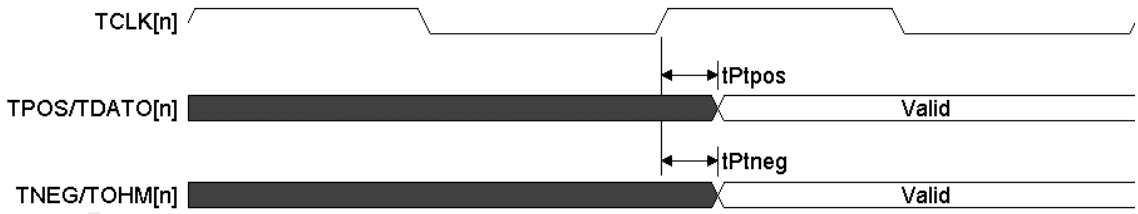


Table 41 Transmit PDH Interface (Figure 58)

Symbol	Description	Min	Typical	Max	Units
$F_{TCLK(STS-1E)}$	TCLK[n] Frequency (STS-1E Operation)	—	51.840	—	MHz
$F_{TCLK(DS3)}$	TCLK[n] Frequency (DS3 Operation)	—	44.736	—	MHz

Symbol	Description	Min	Typical	Max	Units
$F_{TCLK(E3)}$	TCLK[n] Frequency (E3 Operation)	—	34.368	—	MHz
D_{TCLK}	TCLK[n] Duty Cycle	40	50	60	%
tP_{TPOS}	TCLK[n] to TPOS/TDATO[n] Valid	1	—	10	ns
tP_{TNEG}	TCLK[n] to TNEG/TOHM[n] Valid	1	—	10	ns

Figure 59 Receive PDH Interface Timing

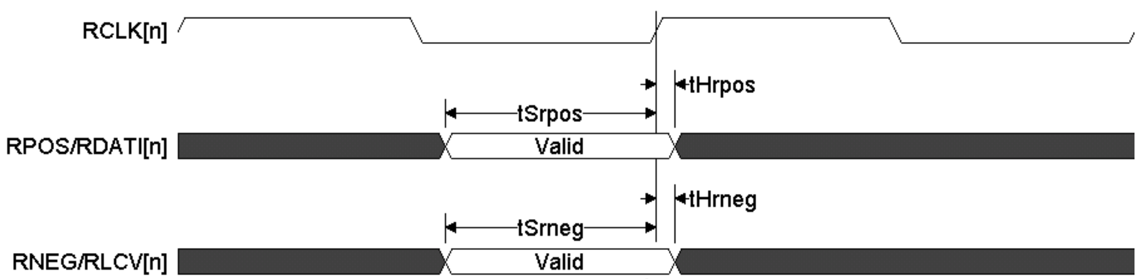


Table 42 Receive PDH Interface (Figure 59)

Symbol	Description	Min	Typical	Max	Units
$F_{RCLK(STS-1E)}$	RCLK[n] Frequency (STS-1E Operation)	—	51.840	—	MHz
$F_{RCLK(DS3)}$	RCLK[n] Frequency (DS3 Operation)	—	44.736	—	MHz
$F_{RCLK(E3)}$	RCLK[n] Frequency (E3 Operation)	—	34.368	—	MHz
D_{RCLK}	RCLK[n] Duty Cycle	40	50	60	%
tS_{RPOS}	RPOS/RDATI[n] Setup time to RCLK[n]	3	—	—	ns
tH_{RPOS}	RPOS/RDATI[n] Hold time to RCLK[n]	1	—	—	ns
tS_{RNEG}	RNEG/RLCVI[n] Setup time to RCLK[n]	3	—	—	ns
tH_{RNEG}	RNEG/RLCVI[n] Hold time to RCLK[n]	1	—	—	ns

Notes on Input Timing

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.
3. This parameter is guaranteed by design. No production tests are done on this parameter.
4. High pulse width is measured from the 1.4 Volt points of the rise and fall ramps. Low pulse width is measured from the 1.4 Volt points of the fall and rise ramps.

Notes on Output Timing

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum and minimum output propagation delays are measured with a 30 pF load on the outputs.

13.8 DS3/E3 Serial Interface Timing Characteristics

Intrinsic/Mapping Jitter is defined as the sum of the intrinsic payload mapping jitter and the jitter that is generated as a result of the asynchronous mapping. Intrinsic/Mapping Jitter is measured in the absence of pointer movements and input jitter.

Pointer Jitter is defined as the jitter measured due to pointer movements in the SONET/SDH network. Pointer jitter is measured as per ANSI T1.105.3b, ITU G.783, and GR-253 CORE.

Input jitter tolerance is defined as the maximum amplitude sinusoidal jitter that the ARROW 155 can tolerate without error while mapping the DS3/E3 stream into SONET.

Intrinsic/Mapping Wander is defined as the sum of the wander generation of the clocks and the wander that is generated as a result from asynchronous mapping. Intrinsic/Mapping wander is measured in the absence of pointer movements, wander on synchronizing signals, input jitter, and input wander.

Pointer Wander is defined as the wander measured due to pointer movements in the SONET/SDH network. Pointer wander is measured as per ANSI T1.105.3b, ITU G.783, and GR-253 CORE.

Table 43 DS3 Serial Interface Timing Characteristics

Symbol	Description	Min	Typical	Max	Units
JG_{DS3}	Peak to peak Intrinsic Jitter in DS3 mode. 10Hz – 400kHz (worst-case) 30kHz – 400kHz (worst-case)	—	 0.245 0.053	—	UIpp
JP_{DS3}	Peak to Peak Pointer Jitter in DS3 Mode All 10Hz – 400kHz (unless otherwise specified)	—	—	—	—
	Single Pointer Adjustment	—	0.131	0.138	UIpp
	Burst of 3 Pointer Adjustments	—	0.182	0.380	UIpp
	Phase Transient Pointer Adjustment Burst	—	0.242	0.317	UIpp
	Periodic Pointer Adjustments no Add/Cancel	—	0.230	0.526	UIpp
	Periodic Pointer Adjustments with Add	—	0.333	0.621	UIpp
	Periodic Pointer Adjustments with Cancel	—	0.347	0.658	UIpp
WG_{DS3}	MTIE Mapping Wander in DS3 Mode	See Figure 60			
WP_{DS3}	MTIE Pointer Wander in DS3 Mode				
	Single Pointer Adjustment	See Figure 61			
	Burst of 3 Pointer Adjustments	See Figure 62			
	Phase Transient Pointer Adjustment Burst	See Figure 63			
	87-3 Pointer Sequence	See Figure 64			
	Periodic Pointer Adjustments	See Figure 65			

Notes

1. Typical Pointer Jitter is the average of all measurements. Maximum pointer jitter is the maximum jitter of all measurements.
2. Typical Periodic Pointer Jitter is the average jitter measured over 7.5ms < T < 1s.

3. Maximum Periodic Pointer Jitter is measured with a time constant 7.5ms < T < 1s.
4. Pointer Wander shown is measured with time constant T = 34ms, unless otherwise specified. The wander was also measured and passed all masks with T = 7.5ms.

Figure 60 DS3 Mapping Wander MTIE

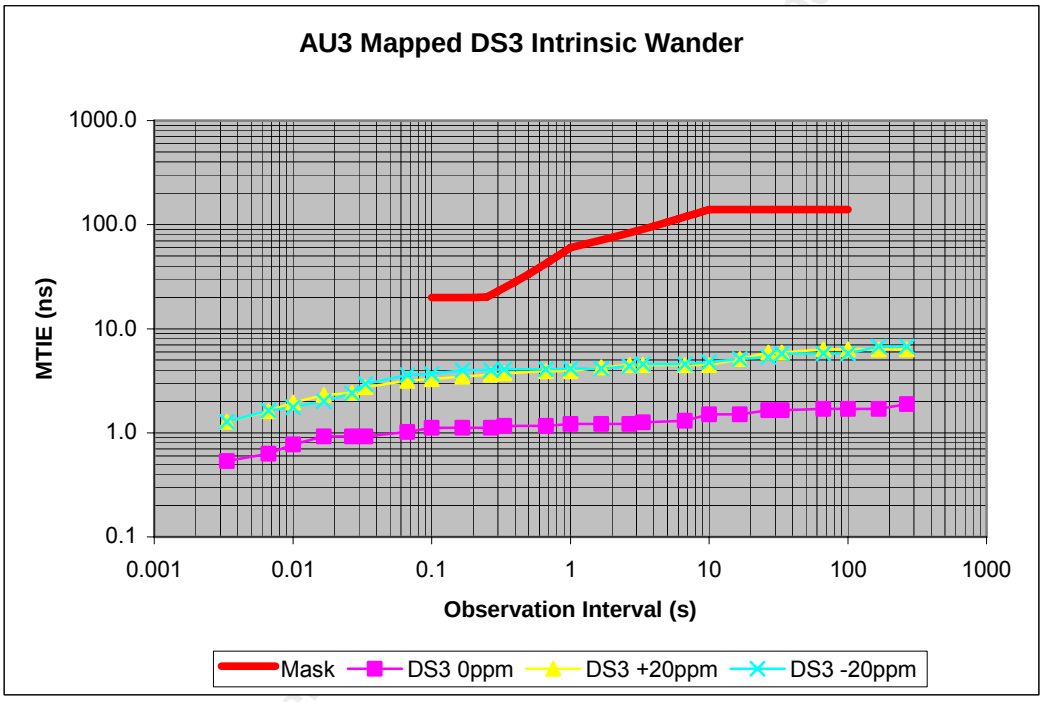


Figure 61 DS3 Pointer Wander MTIE (Single Pointer Adjustment)

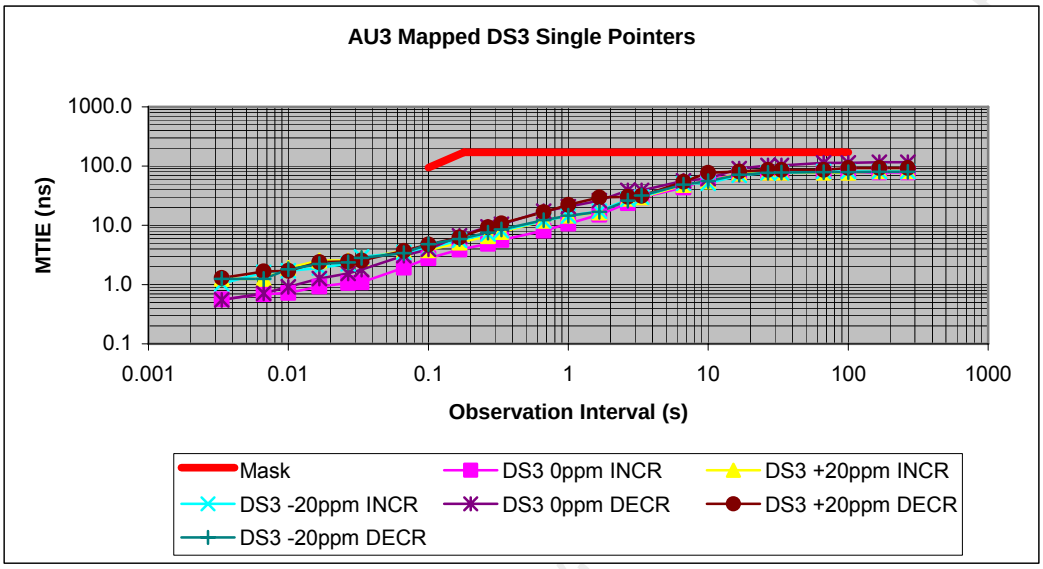


Figure 62 DS3 Pointer Wander MTIE (Burst of 3 Pointer Adjustments)

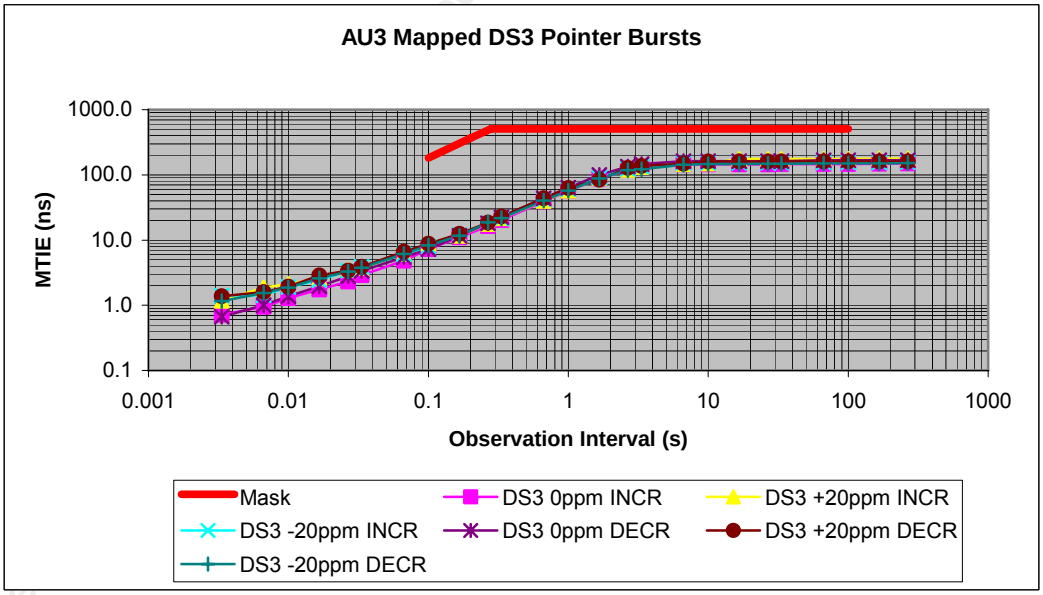


Figure 63 DS3 Pointer Wander MTIE (Phase Transient Pointer Adjustment Burst)

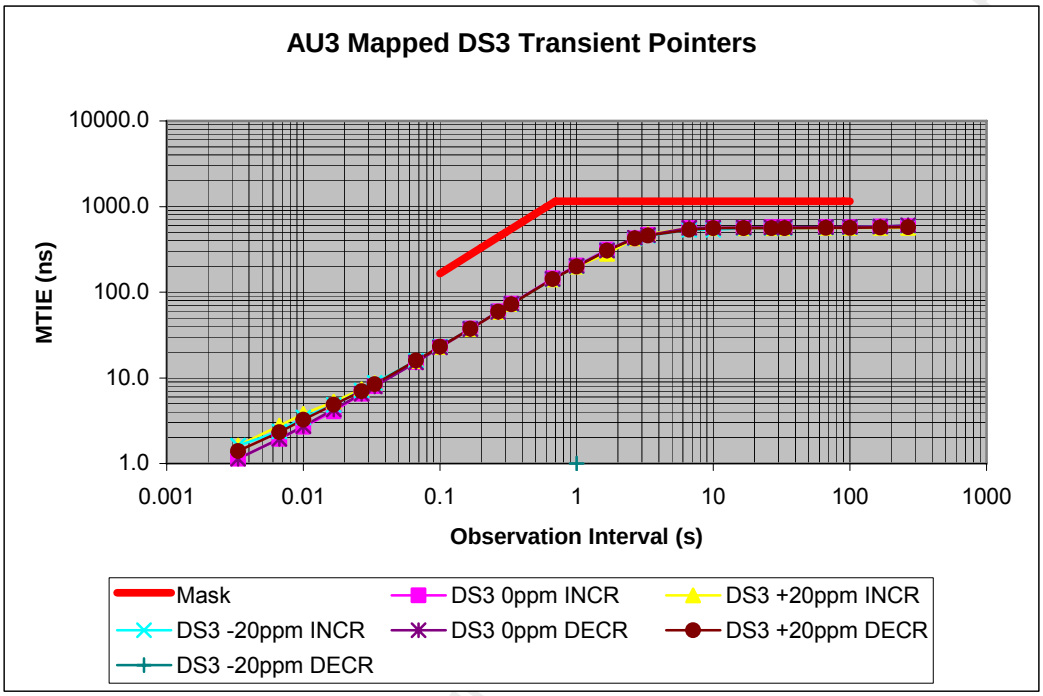


Figure 64 DS3 Pointer Wander MTIE (87-3 Pointer Sequence)

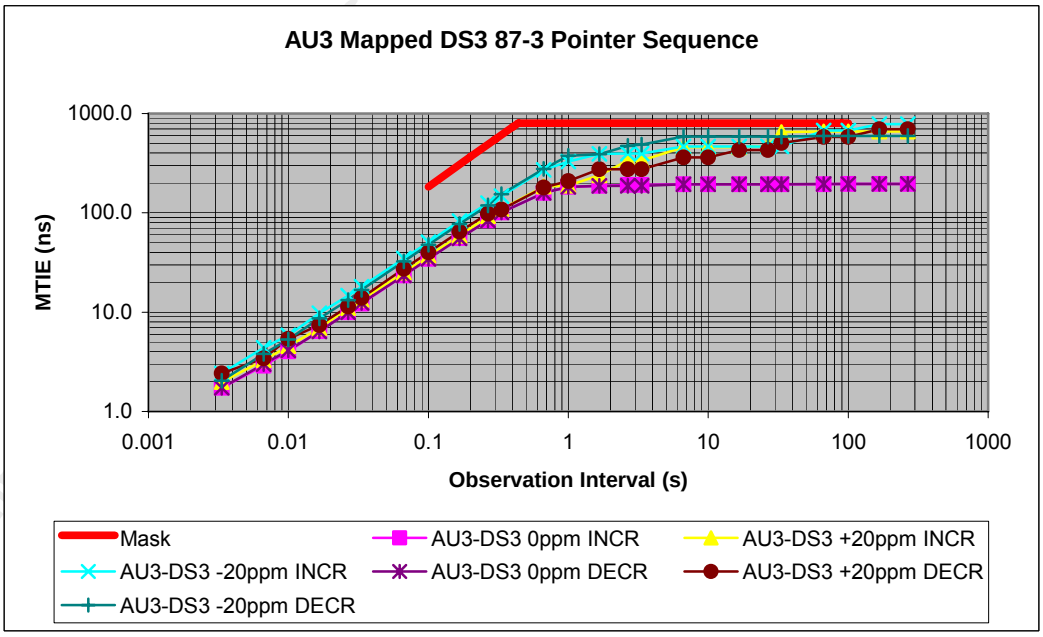


Figure 65 DS3 Pointer Wander MTIE (Periodic Pointer Adjustments)

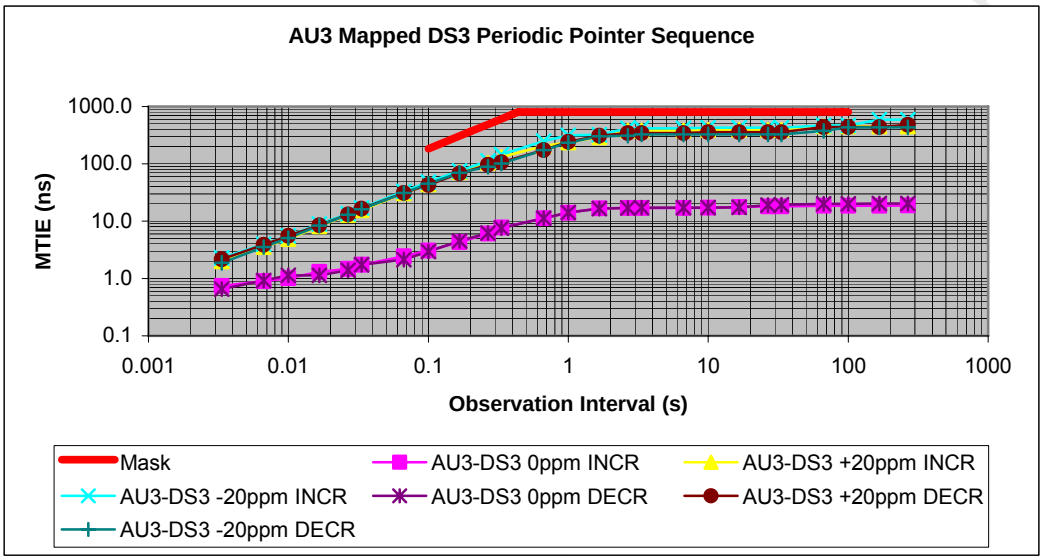


Table 44 E3 Serial Interface Timing Characteristics

Symbol	Description	Min	Typical	Max	Units
JG_{DS3}	Peak to peak Intrinsic Jitter in E3 mode. 100Hz – 800kHz 10kHz – 800kHz	—	 0.104 0.049	—	UIpp
JP_{DS3}	Peak to Peak Pointer Jitter in E3 Mode	—	—	—	—
	Single pointers of opposite polarity 100Hz – 800kHz 10kHz – 800kHz	—	 0.064 0.021	 0.145 0.026	UIpp
	Regular Pointers plus one double pointer 100Hz – 800kHz 10kHz – 800kHz	—	 0.071 0.021	 0.216 0.028	UIpp
	Regular Pointers with one missing pointer 100Hz – 800kHz 10kHz – 800kHz	—	 0.068 0.021	 0.171 0.028	UIpp
	Double pointers of opposite polarity 100Hz – 800kHz 10kHz – 800kHz	—	 0.066 0.021	 0.145 0.026	UIpp
WG_{DS3}	MTIE Mapping Wander in E3 Mode	See Figure 66			
WP_{DS3}	MTIE Pointer Wander in E3 Mode				
	Single pointers of opposite polarity	See Figure 67			
	Regular Pointers plus one double pointer	See Figure 68			
	Regular Pointers with one missing pointer	See Figure 69			
	Double pointers of opposite polarity	See Figure 70			

Notes

1. Typical Peak to peak Intrinsic Jitter is the average worst case results.

2. Typical Pointer Jitter is average jitter of all measurements. Maximum Pointer Jitter is the maximum jitter of all measurements.

Figure 66 E3 Mapping Wander MTIE

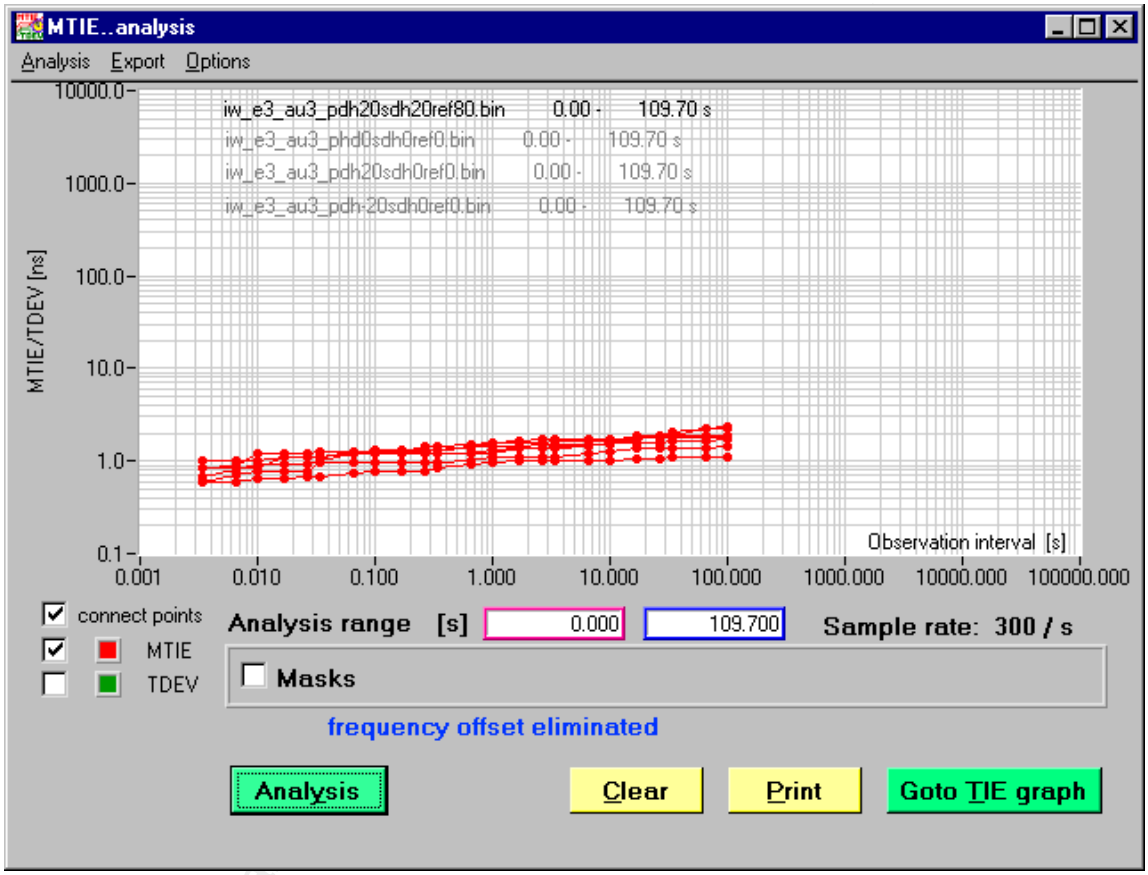


Figure 67 E3 Pointer Wander MTIE (Single Pointers of opposite polarity)

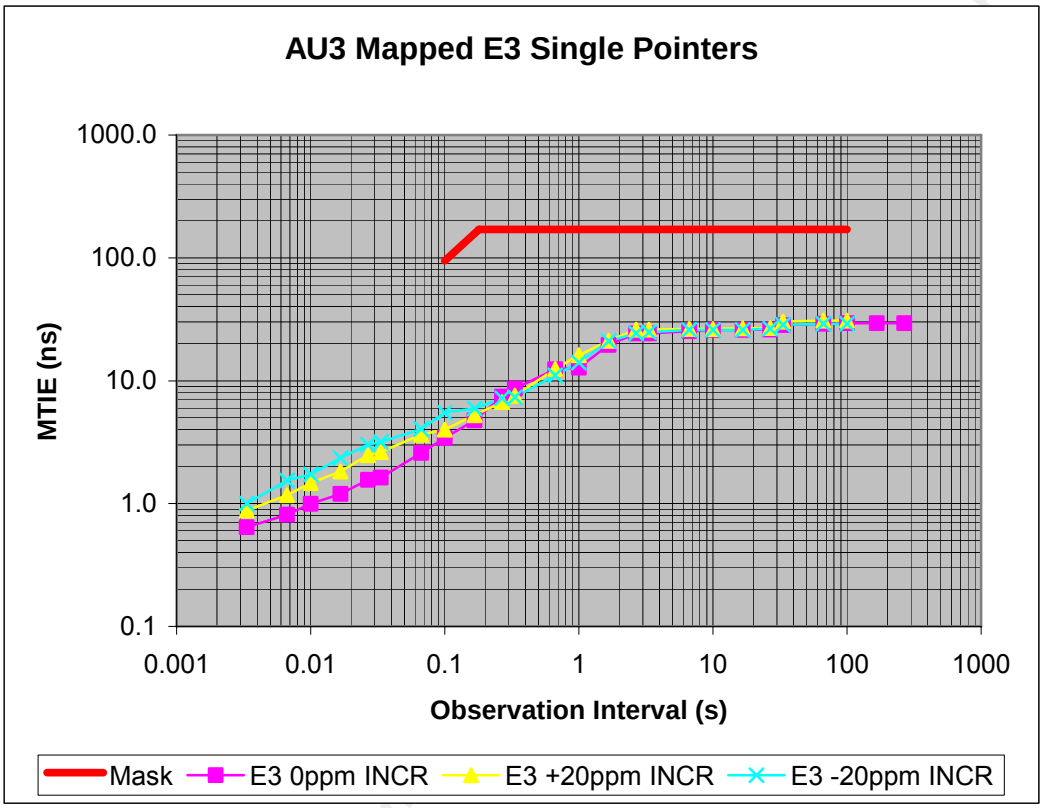


Figure 68 E3 Pointer Wander MTIE (Regular Pointers plus one double pointer)

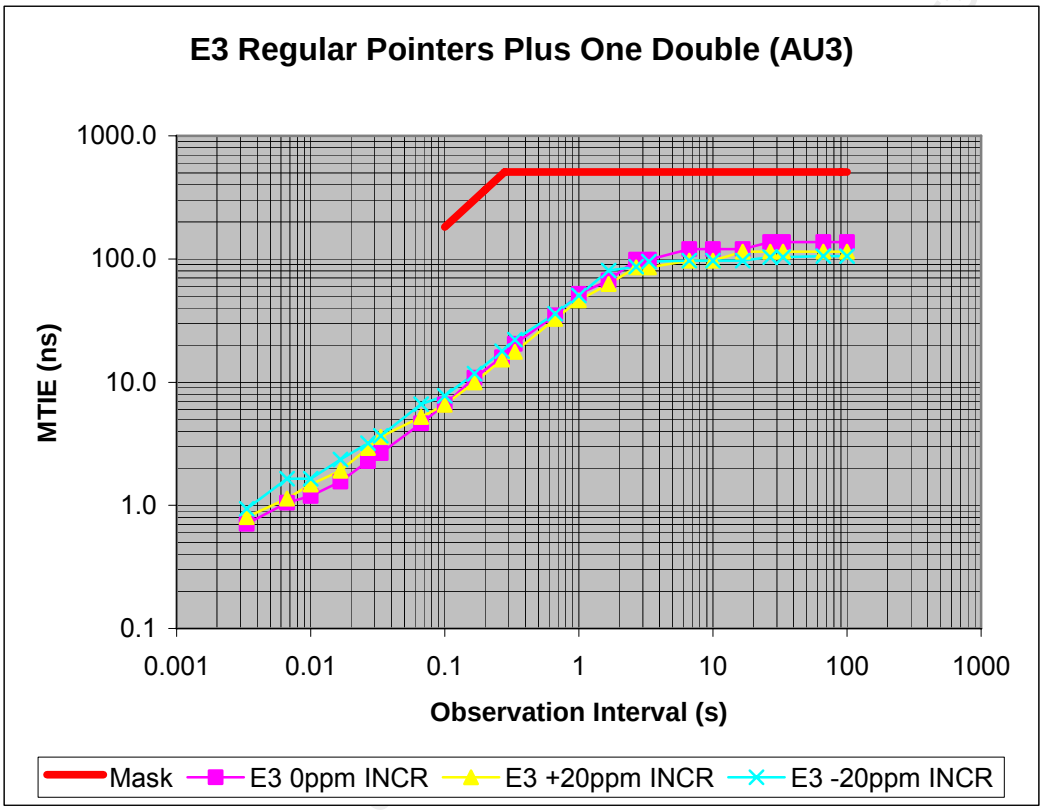


Figure 69 E3 Pointer Wander MTIE (Regular Pointers with one missing pointer)

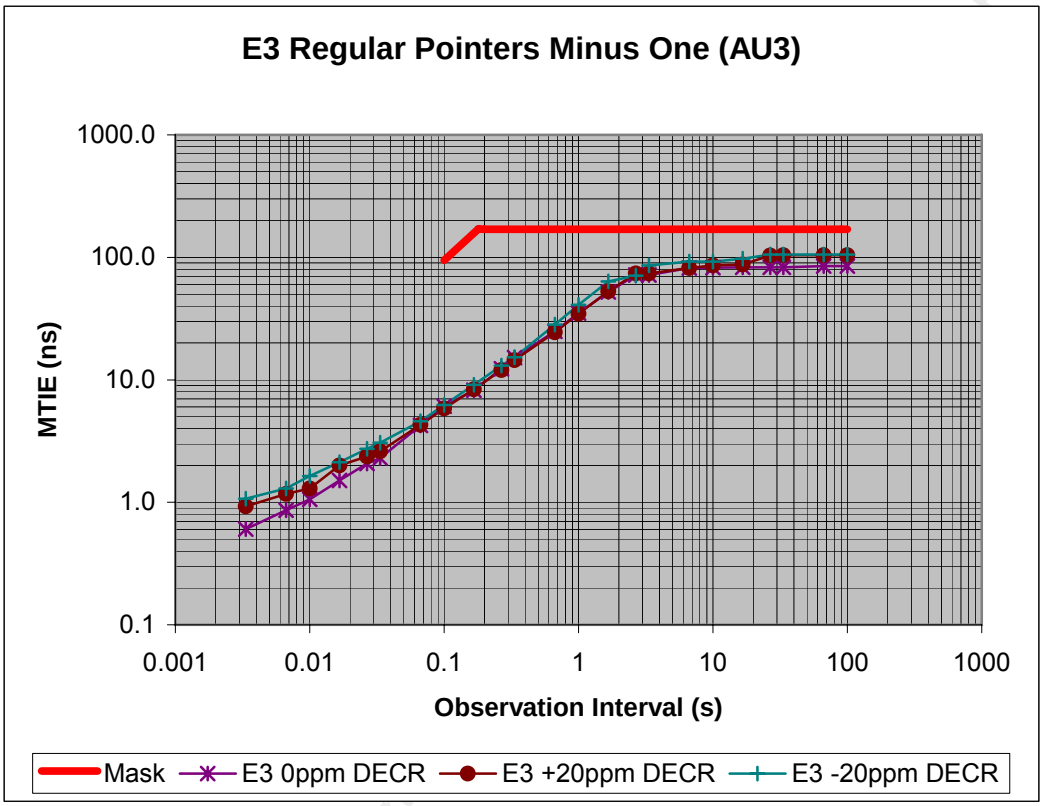
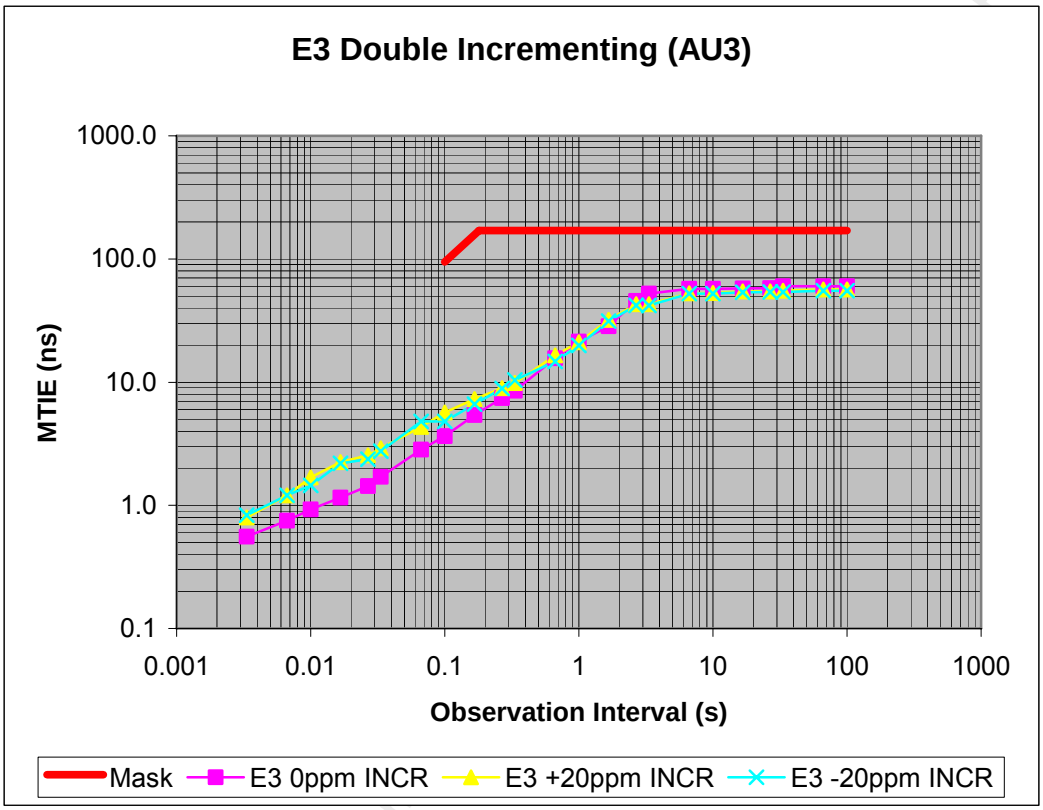


Figure 70 E3 Pointer Wander MTIE (Double pointers of opposite polarity)



13.9 PDH Overhead Interface Timing

Figure 71 PDH Overhead Insertion & Extraction Interface Timing

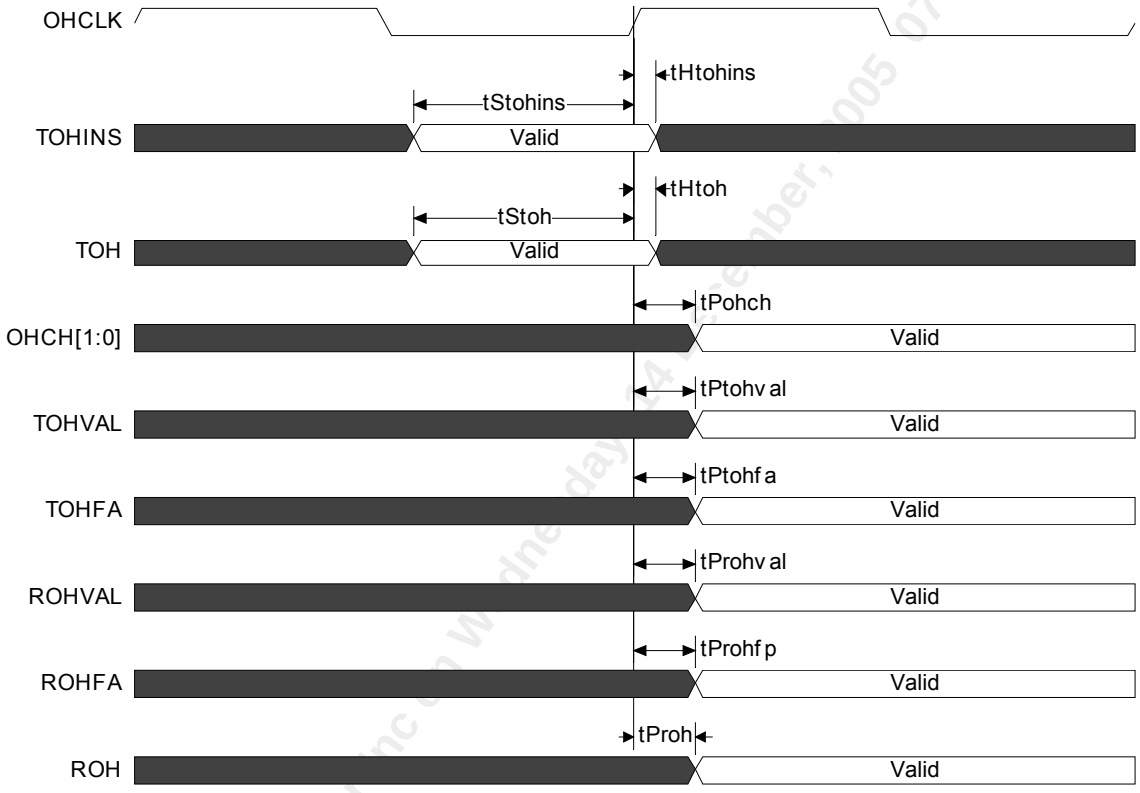


Table 45 PDH Overhead Insertion & Extraction Interface (Figure 71)

Symbol	Description	Min	Typical	Max	Units
tS_{TOHINS}	TOHINS Setup time to OHCLK	2.5	—	—	ns
tH_{TOHINS}	TOHINS Hold time to OHCLK	0	—	—	ns
tS_{TOH}	TOH Setup time to OHCLK	2.5	—	—	ns
tH_{TOH}	TOH Hold time to OHCLK	0	—	—	ns
tP_{OHCH}	OHCLK to OHCH[1:0] Valid	1	—	7	ns
tP_{TOHVAL}	OHCLK to TOHVAL Valid	1	—	7	ns
tP_{TOHFA}	OHCLK to TOHFA Valid	1	—	7	ns
tP_{ROHVAL}	OHCLK to ROHVAL Valid	1	—	7	ns
tP_{ROHFA}	OHCLK to ROHFA Valid	1	—	7	ns
tP_{ROH}	OHCLK to ROH Valid	1	—	7	ns

Notes on Input Timing

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.
3. This parameter is guaranteed by design. No production tests are done on this parameter.
4. High pulse width is measured from the 1.4 Volt points of the rise and fall ramps. Low pulse width is measured from the 1.4 Volt points of the fall and rise ramps.

Notes on Output Timing

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum and minimum output propagation delays are measured with a 30 pF load on the outputs.

13.10 JTAG

Table 46 JTAG Port Interface

Symbol	Description	Min	Max	Units
fCLK	TCLK Frequency	—	1	MHz
Tlw	TCLK low pulse width	400	—	ns
Thw	TCLK high pulse width	400	—	ns
Ts	TDI, TMS Set-up time to TCLK rising edge	50	—	ns
Th	TDI, TMS Hold time to TCLK rising edge	50	—	ns
Tnp	TCLK falling edge to TDO Valid	2	50	ns
Tnz	TCLK falling edge to TDO High-Impedance	2	50	ns
Tnzb	TCLK falling edge to TDO Driven	2	50	ns

14 Ordering Information

Table 47 Ordering Information

Part No.	Description
PM5320-NI	196-Pin CABGA, 15 x 15 x 1.62 mm, 1.00 mm BP
PM5320-NGI	196-Pin CABGA, 15 x 15 x 1.62 mm, 1.00 mm BP (RoHS-compliant)

Notes

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