PM5360

S/UNI® MULTI-48™

Multi-rate SATURN® User Network Interface for 1x2488, 4x622, and 4x155

DATA SHEET

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Granted

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U.S. Patent Numbers: 5,606,563; 5,640,398; 5,835,602; 6,052,073; 6,150,965; 6,188,692; 6,301,318; 6,621,360

Canadian Patent Numbers: 2,149,076; 2,159,763; 2,161,921; 2,194,919; 2,245,760

U.K. Patent Number 2,290,438

Other relevant patent grants may also exist.

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Revision History

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1	July 2002	Document created.
2	Sept 2002	Added pin-out diagram and mappings.
3	February 2003	Major post tape-out update. Changes in all major sections.
4	September 2003	Minor updates in all major sections.
5	September 2003	Included Register bits added with Rev B and operation section on interoperability via 777LVDS links. Updated status to reflect production release

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1 Definitions

Table 1 defines the terms and abbreviations used in this document.

Table 1 Definitions

Term	Definition
AIS	Alarm Indication Signal
APISO	APS Parallel to Serial Converter
APS	Automatic Protection Switching
ASSP	Application Specific Standard Product
ATM	Asynchronous Transfer Mode
BER	Bit Error Rate
BIP	Byte Interleaved Parity
CMOS	Complementary Metal Oxide Semiconductor
CRC	Cyclic Redundancy Check
CRU	Clock Recovery Unit
CSU	Clock Synthesis Unit
DCC	Data Communication Channel
DCRU	Digital Clock Recovery Unit
DRU	Data Recovery Unit
ECL	Emitter-Coupled Logic
ERDI	Enhanced Remote Defect Indication
ESD	Electrostatic Discharge
FCS	Frame Check Sequence
RFI	Far-End Block Error
FIFO	First-In First-Out
GFC	Generic Flow Control
HCS	Header Check Sequence
HDLC	High-level Data Link Controller
JAT	Jitter Attenuator
LAS	Line Analog Shim (Wrapper)
LCD	Loss of Cell Delineation
LFSR	Linear Feedback Shift Register
LOF	Loss of Frame
LOP	Loss of Pointer
LOS	Loss of Signal
LVDS	Low Voltage Differential Signaling
LVTTL	Low-Voltage Transistor-Transistor Logic
MABC	Multi-function Analog Block Component
NC	No Connect - indicates an unused pin
NDF	New Data Flag
NNI	Network-Network Interface

Term	Definition
NRZ	Non-Return-to-Zero
ODL	Optical Data Link
OOF	Out of Frame
PECL	Pseudo-ECL
PISO	Parallel-In-Serial-Out (Parallel to Serial Converter)
PLL	Phase-Locked Loop
POS	Packet Over SONET
PPP	Point-to-Point Protocol
PRBS	Pseudo-Random Bit Sequence
PRGM	SONET/SDH PRBS Generator/Monitor Block
PSL	Path Signal Label
PL3	POS-PHY Level 3: SATURN-compatible interface for packet over SONET physical layer and link layer devices [19]
PLM	Path Signal Label Mismatch
RCAS12	Receive 12 Channel Assigner Block
RCFP	Receive Cell and Frame Processor Block for STS-48c (VC-4-16c) and STS-12c (VC-4-4c) channels
RDI-L	Line Remote Defect Indication
RHPP	Receive High Order Path Processor
RRMP	Receive Regenerator and Multiplexer Processor
RTDP	Receive Time-sliced Datacom Processor Block for sub-STS-12c (VC-4-4c) channels
RTTP	Receive Trail Trace Processor
RXPHY	Receive PHY Interface
RXSDQ	Receive Scalable Data Queue FIFO
RDI	Remote Defect Indication
SARC	SONET/SDH Alarm Reporting Controller
SBER	SONET/SDH Bit Error Rate Monitor
SD	Signal Detect (pin); Signal Degrade (BER related line defect)
SDH	Synchronous Digital Hierarchy
SF	Signal Fail
SIPO	Serial-In Parallel-Out (Serial to Parallel Converter)
SIRP	SONET/SDH In-band Error Report Processor
SONET	Synchronous Optical Network
SPE	Synchronous Payload Envelopes
STLI	SONET/SDH Transmit Line Interface
STSI	Space and Timeslot Interchange
SVCA	SONET/SDH Virtual Container Aligner
TCAS12	Transmit 12 Channel Assigner Block
TCFP	Transmit Cell and Frame Processor for STS-48c (VC-4-16c) and STS-12c (VC-4-4c) channels
THPP	Transmit High Order Path Processor
TIM	Trace Identifier Mismatch
TIU	Trace Identifier Unstable

Term	Definition
TOH	Transport Overhead
TRMP	Transmit Regenerator Multiplexer Processor
TTDP	Transmit Time-sliced Datacom Processor Block for sub-STS-12c (VC-4-4c) channels
TTTP	Transmit Trail trace Processor
TXPHY	Transmit PHY Interface
TXSDQ	Transmit Scalable Data Queue FIFO
UI	Unit Interval
UL3	UTOPIA 3 Physical Layer Interface [14]
UNI	User-Network Interface
VCI	Virtual Connection Indicator
VPI	Virtual Path Indicator
WAN	Wide Area Network
XOR	Exclusive OR logic operator

2 Features

2.1 General

- Single chip ATM and POS User-Network Interface supporting 1x2488.32 Mbit/s or a combination of up to 4x622.08 Mbit/s or up to 4x155.52 Mbit/s.
- Implements the ATM Forum User Network Interface Specification and the ATM physical layer for Broadband ISDN according to CCITT Recommendation I.432.
- Implements the Point-to-Point Protocol (PPP) over SONET/SDH specification according to RFC 2615(1619)/1662 of the PPP Working Group of the Internet Engineering Task Force (IETF).
- Processes a duplex bit-serial 2488.32 Mbit/s STS-48 (STM-16) data stream with on-chip clock and data recovery and clock synthesis. The STS-48 (STM-16) stream may contain an STS-48c (VC-4-16c) or a combination of STS-12c (VC-4-4c) and STS-3c (VC-4).
- Processes up to four duplex bit-serial 622.08 Mbit/s STS-12 (STM-4) data streams with on-chip clock and data recovery and clock synthesis. Each STS-12 (STM-4) may contain a combination of STS-12c (VC-4-4c) or STS-3c (VC-4).
- Processes up to four duplex bit-serial 155.52 Mbit/s STS-3 (STM-1) data streams with on-chip clock and data recovery and clock synthesis. Each STS-3 (STM-1) may contain only an STS-3c (VC-4).
- Each of the four duplex links capable of 622.08 Mbit/s STS-12 (STM-4) and 155.52 Mbit/s STS-3 (STM-1) operation can be independently configured for either rate.
- Complies with Telcordia GR-253-CORE jitter tolerance, jitter transfer, and intrinsic jitter criteria.[1]
- Provides termination for SONET Section, Line and Path overhead or SDH Regenerator Section, Multiplexer Section, and High Order Path overhead.
- Provides cross-bar functionality to swap STS-12 (STM-4) and STS-3 (STM-1) clients to/from different line-side interfaces.
- Provides support for automatic protection switching (APS) via a 4-bit LVDS 777.6 MHz port.
- Provides cross-bar functionality to swap STS-12 (STM-4) and STS-3 (STM-1) lines and/or clients to/from different APS interfaces.
- Provides a UTOPIA Level 3 32-bit wide System Interface (clocked up to 104 MHz) with parity support for ATM applications.
- Provides a SATURN® POS-PHY Level 3™ 32-bit System Interface (clocked up to 104 MHz) for Packet over SONET (POS) or ATM applications.
- Supports independent loop-timed operation for each transmit serial stream.

[1] Telcordia GR-253-CORE intrinsic jitter criteria is not met in loop-timed mode.

- Supports an independent line loopback from each line side receive stream to the corresponding transmit stream as well as an independent diagnostic loopback from the line side transmit stream to the corresponding line side receive stream interface.
- Provides PRBS-23 generator/monitor for off-line link verification.
- Provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.
- Provides a generic 16-bit microprocessor bus interface for configuration, control, and status monitoring.
- Low power 1.8 V CMOS core logic with 3.3 V CMOS/TTL compatible digital inputs and digital outputs. PECL inputs and outputs are 3.3 V compatible.
- Industrial temperature range (-40°C to +85°C).
- 500-ball UBGA package.

2.2 SONET Section and Line / SDH Regenerator and Multiplexer Section

- Frames to the SONET/SDH receive stream(s) and inserts the framing bytes (A1, A2) into the transmit stream(s); descrambles the received stream(s) and scrambles the transmit stream(s).
- Calculates and compares the bit interleaved parity (BIP) error detection codes (B1, B2) for the receive stream. Calculates and inserts B1 and B2 in the transmit stream. Accumulates near end errors (B1, B2) and far end errors (M1) and inserts line remote error indications (REI) into the M1 byte based on received B2 errors.
- Detects signal degrade (SD) and signal fail (SF) threshold crossing alarms based on received B2 errors.
- Extracts and optionally inserts the SONET/SDH transport overhead on dedicated pins.
- Extracts and filters the automatic protection switch (APS) channel (K1, K2) bytes into internal registers. Inserts the APS channel into the transmit stream.
- Extracts and filters the synchronization status message (S1) byte into an internal register for the receive stream. Inserts the synchronization status message (S1) byte into the transmit stream.
- Extracts a 64-byte (Telcordia compatible) or 16-byte (ITU compatible) section trace (J0) message using an internal register bank for the receive stream(s). Detects an unstable message or mismatch message with an expected message. Provides access to the accepted message via the microprocessor port. Inserts a 64-byte or 16-byte section trace (J0) message using an internal register bank for the transmit stream(s).
- Detects loss of signal (LOS), out of frame (OOF), loss of frame (LOF), line remote defect indication (RDI-L), line alarm indication signal (AIS-L), and protection switching byte failure alarms on the receive stream(s).
- Configurable to force Line AIS in the transmit stream(s).

- Provides automatic transmit line RDI insertion following detection of various received alarms (SD, LOS, DOOL, OOF, LOF, AIS-L, SD(BER), SF(BER), STIM, STIU and RDI-L).
- Provides automatic PAIS insertion following detection of various received alarms (LOS, LOF, AIS-L, SD, SF, STIM, and STIU).
- Supports Automatic Protection Switching (APS) via a mate protection port.

2.3 SONET Path / SDH High Order Path

- Interprets the received payload pointer (H1, H2) and extracts the synchronous payload envelope and path overhead.
- Detects loss of pointer (LOP), path alarm indication signal (PAIS), and path (normal and enhanced) remote defect indication (RDI) for the receive stream(s). Optionally inserts path alarm indication signal (PAIS) and path remote defect indication (RDI) in the transmit stream(s).
- Extracts the received path payload label (C2) byte into an internal register and detects for payload label unstable (PLU), payload label mismatch (PLM), payload unequipped (UNEQ), and payload defect indication (PDI). Inserts the path payload label (C2) byte from an internal register for the transmit stream(s).
- Extracts a 64-byte or 16-byte path trace (J1) message using an internal register bank for the receive stream(s). Detects an unstable message or mismatch message with an expected message. Provides access to the captured, accepted, and expected message via the microprocessor port. Inserts a 64-byte or 16-byte path trace (J1) message using an internal register bank for the transmit stream(s).
- Detects received path BIP-8 and counts received path BIP-8 errors for performance monitoring purposes. BIP-8 errors are selectable to be treated on a bit basis or block basis. Optionally calculates and inserts path BIP-8 error detection codes for the transmit stream(s).
- Counts received path remote error indications (REI's) for performance monitoring purposes. Optionally inserts the path REI count into the path status byte (G1) based on bit or block BIP-8 errors detected in the receive path. Reporting of BIP-8 errors is on a bit or block basis independent of the accumulation of BIP-8 errors and is given on an output pin.
- Provides automatic transmit path RDI and path Enhanced RDI insertion following detection of various received alarms (AIS-L, LOP, PAIS, PTIM, PTIU, PLM, PLU, UNEQ and LCD).

2.4 APS Interface

- Provides four 777.6 Mbit/s LVDS transmit APS links that can be independently connected to the transmit UL3/PL3 channel(s) or to the receive line channel(s).
- Provides four 777.6 Mbit/s LVDS receive APS links that can be independently connected to the receive UL3/PL3 channel(s) or to the transmit line channel(s).

- Each 777.6 Mbit/s LVDS link carries an STS-12 stream encoded in a special 8B/10B scheme to guarantee transition density, mark the J0 framing position, and the J1 path overhead position.

2.5 X-Bar

- Allows swapping of any transmit UL3/PL3 channel to any transmit line payload.
- Allows swapping of any receive line payload to any receive UL3/PL3 channel.
- Allows swapping of any receive line interface or any transmit UL3/PL3 channel to any transmit APS interface.
- Allows swapping of any receive APS interface to any receive UL3/PL3 channel or any transmit line interface.

2.6 The Receive ATM Processor

- Extracts ATM cells from the received SONET/SDH (STS-48c/VC-4-16c, STS-12c/VC-4-4c, STS-3c/VC-4) channel payloads using ATM cell delineation.
- Provides ATM cell payload de-scrambling.
- Performs header check sequence (HCS) error detection and idle/unassigned cell filtering.
- Detects out of cell delineation (OCD) and loss of cell delineation (LCD) alarms.
- Counts the number of received cells, idle cells, erroneous cells, and dropped cells.
- Provides UTOPIA Level 3 and POS-PHY Level 3 32-bit wide data path interfaces (clocked up to 104 MHz) with parity support to read extracted cells from an internal scalable channel FIFO.

2.7 The Receive POS Processor

- Supports packet based link layer protocols using byte synchronous HDLC framing.
- Performs self-synchronous POS data de-scrambling on the received STS-48c/VC-4-16c, STS-12c/VC-4-4c, and STS-3c/VC-4 channel payloads using the $x^{43}+1$ polynomial.
- Performs flag sequence detection and terminates the received POS/HDLC frames.
- Performs frame check sequence (FCS) validation for CRC-CCITT and CRC-32 polynomials.
- Performs control escape de-stuffing or byte de-stuffing of the POS/HDLC stream.
- Detects packet abort sequence.
- Checks for minimum and maximum packet lengths and marks them as erroneous.
- Permits FCS stripping on the POS-PHY Level 3 output data stream.
- Provides a SATURN POS-PHY Level 3 compliant 32-bit data path interface (clocked up to 104 MHz) with parity support to read packet data from an internal scalable channel FIFO.

2.8 The Transmit ATM Processor

- Provides idle/unassigned cell insertion.
- Provides HCS generation/insertion and ATM cell payload scrambling.
- Counts the number of transmitted cells.
- Provides UTOPIA Level 3 and POS-PHY Level 3 32-bit wide data path interfaces (clocked up to 104 MHz) with parity support for writing cells into an internal channel FIFO.

2.9 The Transmit POS Processor

- Supports any packet-based link layer protocol using byte synchronous framing.
- Performs self-synchronous POS data scrambling using the $1+X^{43}$ polynomial.
- Encapsulates packets within a POS/HDLC frame.
- Performs flag sequence insertion.
- Performs byte stuffing for transparency processing.
- Optionally performs frame check sequence generation using the CRC-CCITT and CRC-32 polynomials.
- Aborts the affected packets when the FIFO experiences an underflow or overflow or when the upstream PL-3 host commands it.
- Provides a SATURN POS-PHY Level 3 compliant 32-bit wide data path (clocked up to 104 MHz) with parity support to an internal FIFO buffer.

3 Applications

- ATM and Multi-service Switches, Routers, and Switch/Routers.
- SONET/SDH Add/Drop Multiplexers with Data Processing Capabilities.
- Uplink Cards.
- SONET/SDH ATM/POS Test Equipment.

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21. Telcordia Technologies. *Network Equipment-Building System (NEBS) Requirements: Physical Protection: Telcordia Technologies Generic Requirements GR-63-CORE*. Issue 1. October 1995.

5 Application Examples

Figure 1 shows how the S/UNI MULTI-48 device can be used in a multi-rate ATM switch port application. In this example, the SYSCLK oscillator is optional.

Figure 1 Multi-rate ATM Switch Port Application

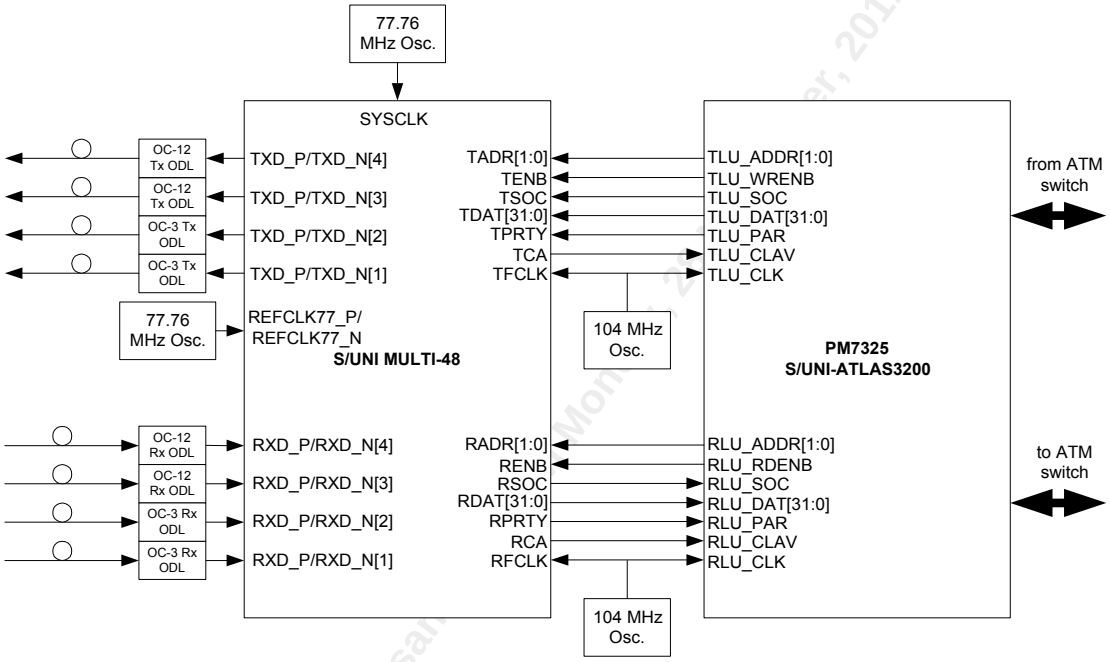


Figure 2 shows how the S/UNI MULTI-48 device can be used in a multi-rate IP switch port application. In this example, the SYSCLK oscillator is optional.

Figure 2 Multi-Rate IP Switch Port Application

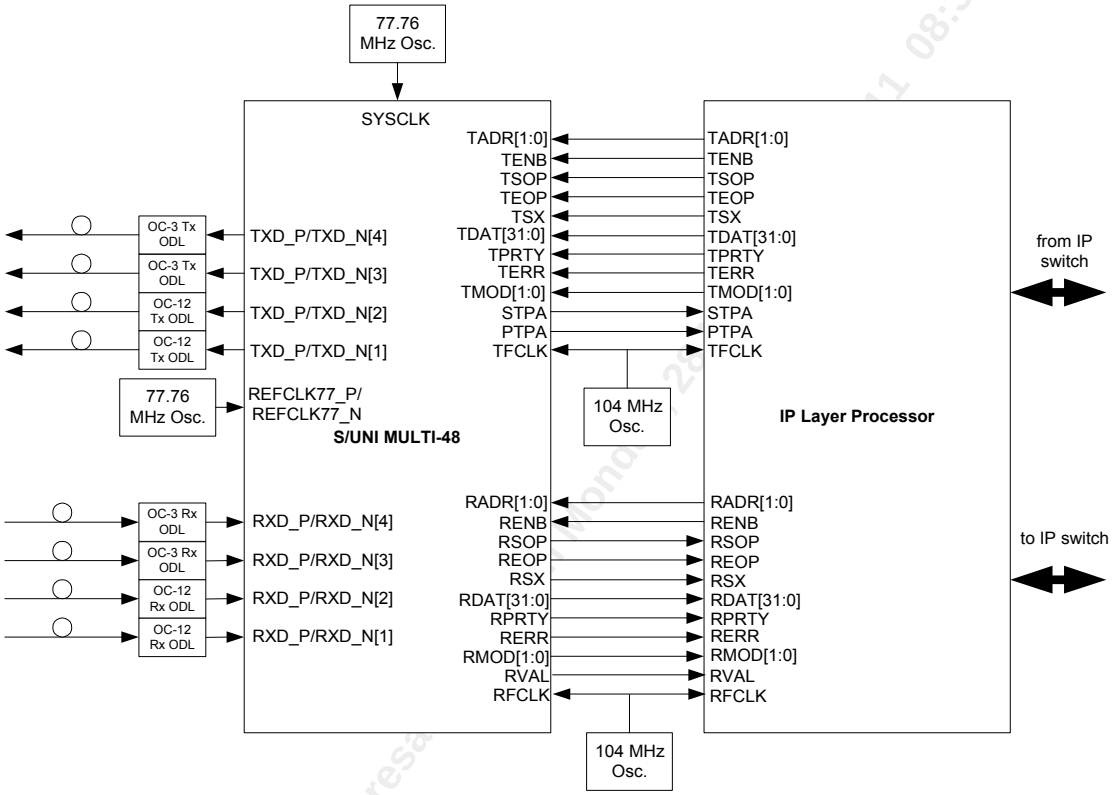
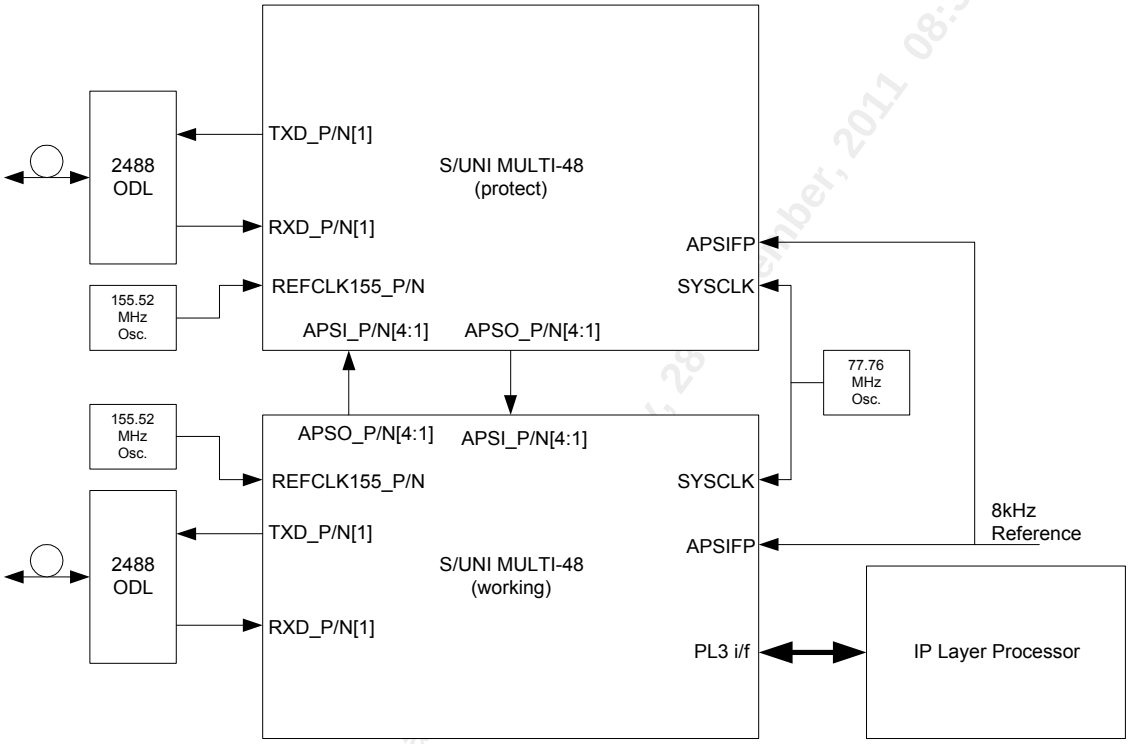


Figure 3 shows how two S/UNI MULTI-48 devices can be used in a 1:1 protection scheme. In this example, the SYSCLK oscillator and 8 kHz reference are optional.

Figure 3 APS Protection Application



6 Block Diagram

Figure 4 Block Diagram

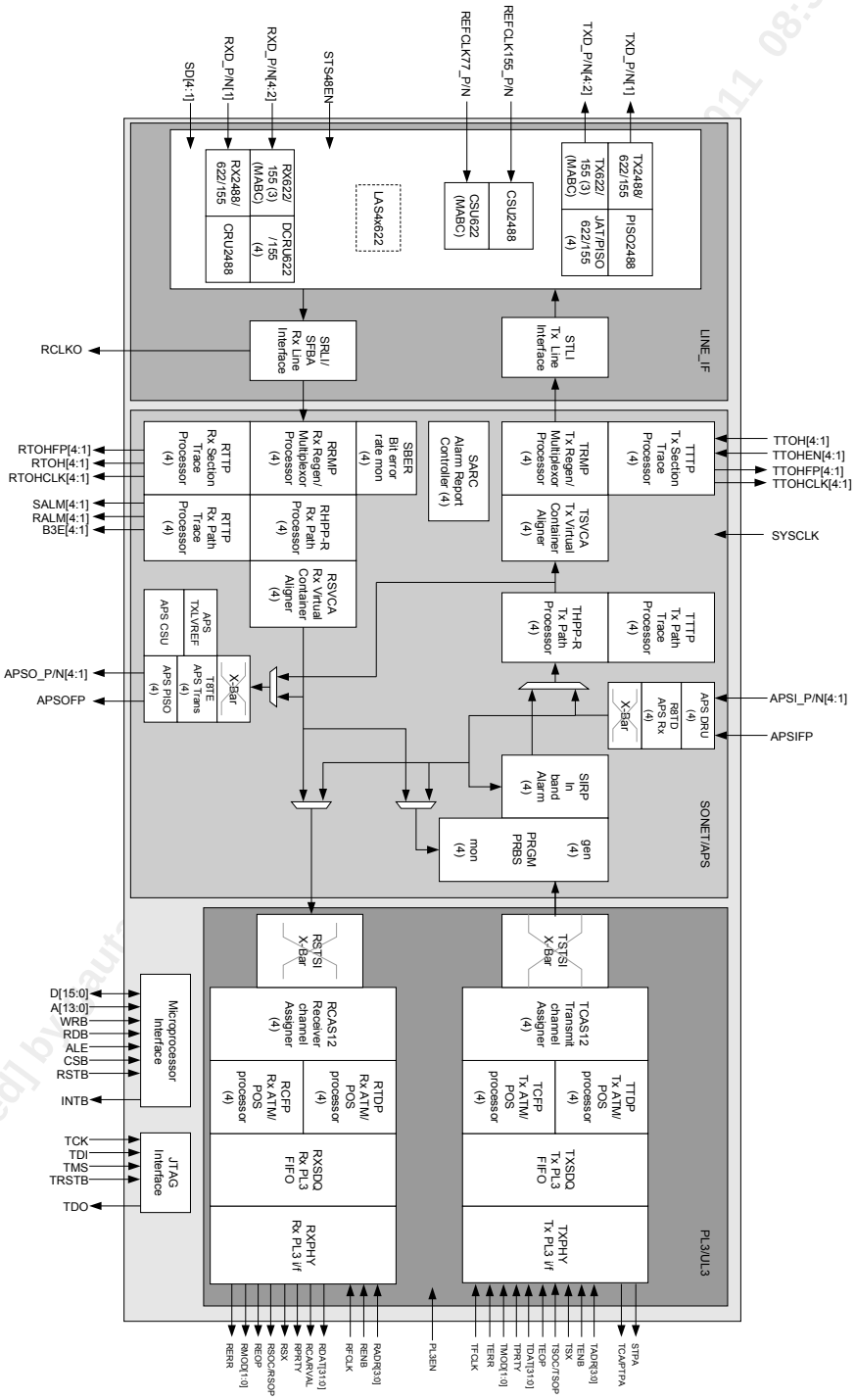


Figure 5 Serial Diagnostic Loopback

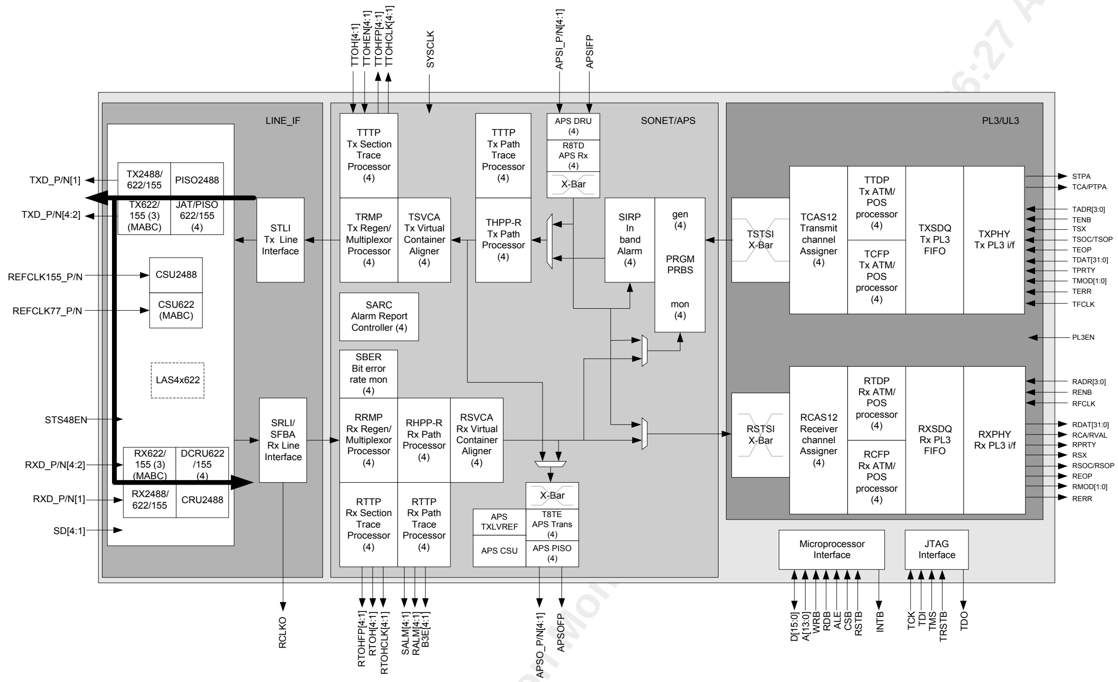


Figure 6 Parallel Diagnostic Loopback

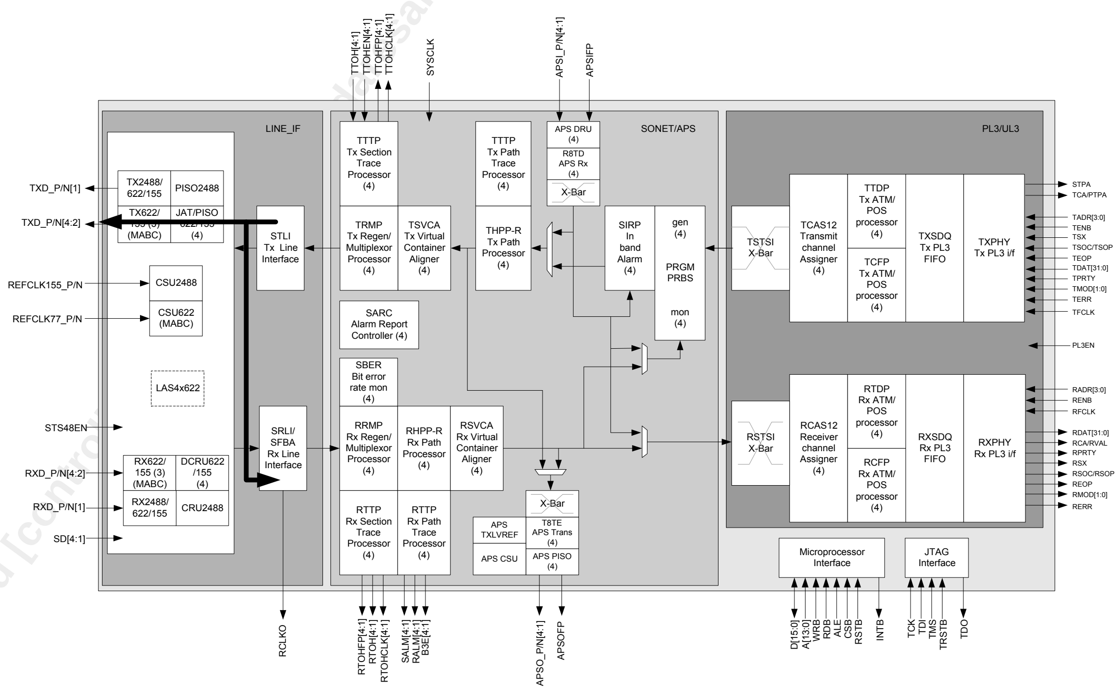


Figure 7 Line Loopback

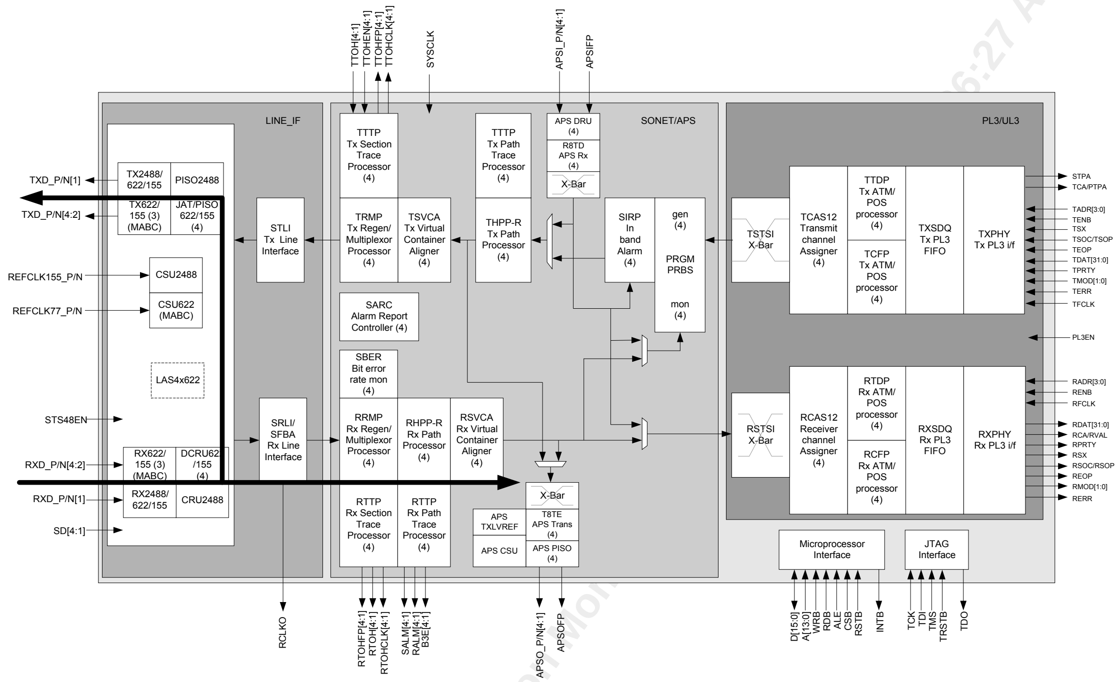


Figure 8 APS Protection Configuration

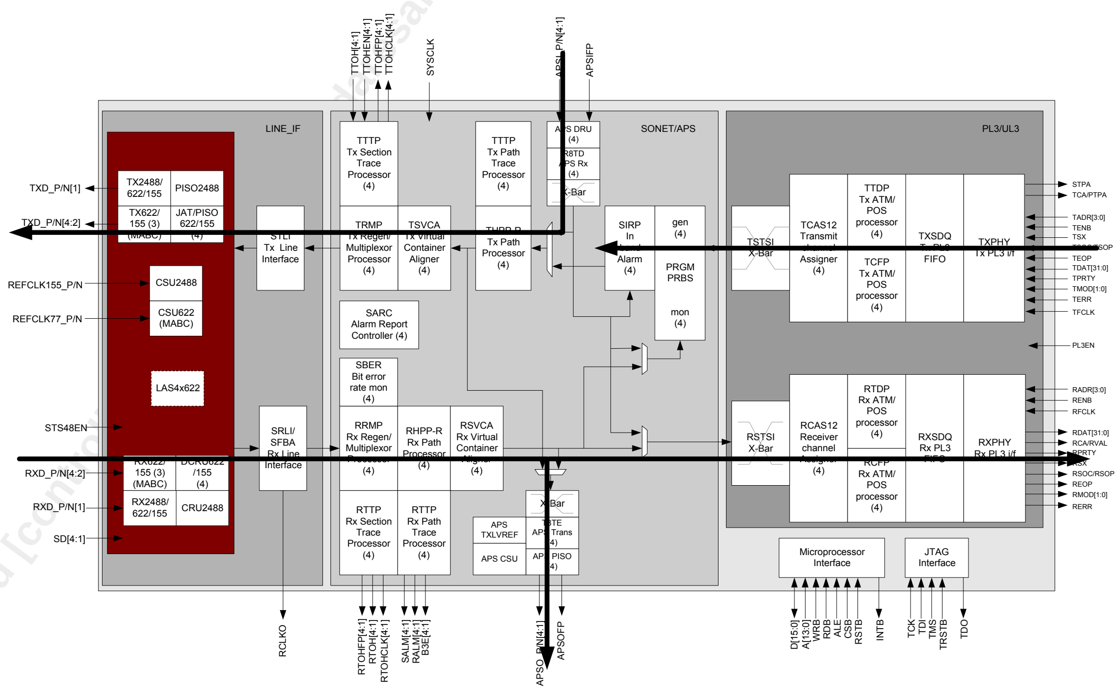


Figure 9 APS Working Configuration

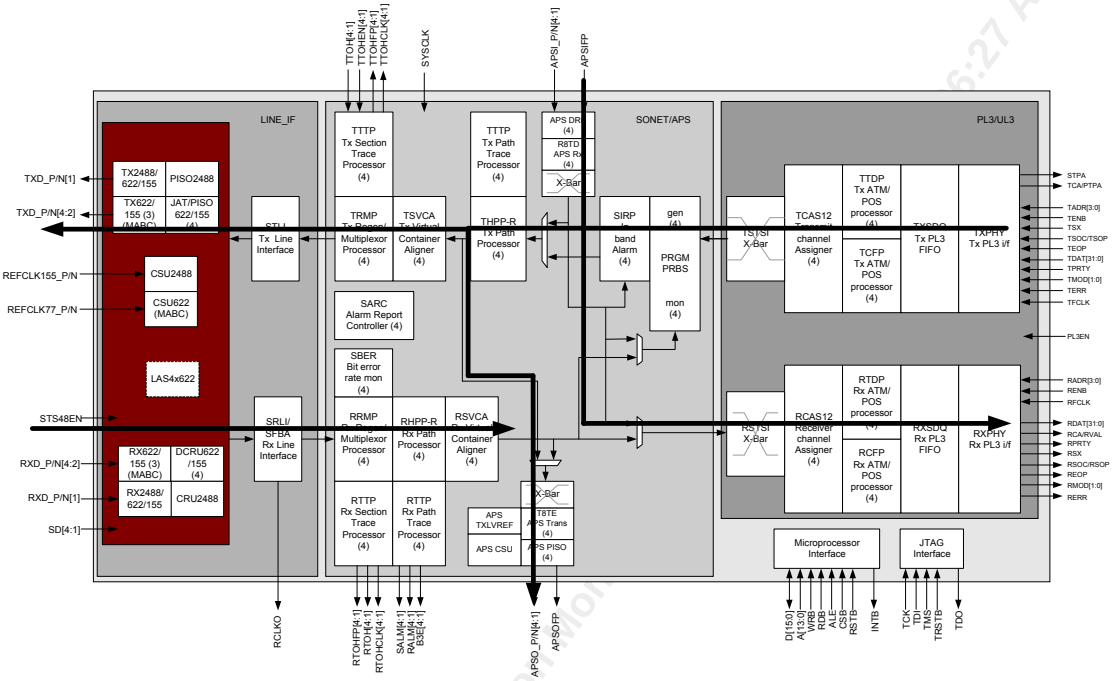
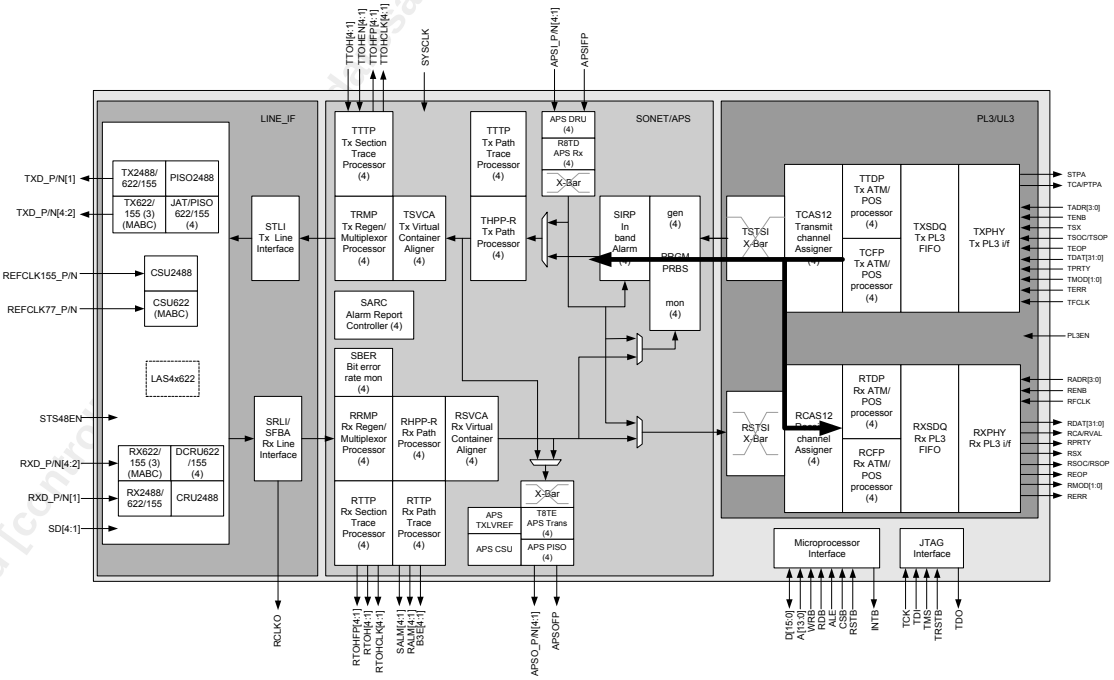


Figure 10 Cell/Packet Loopback



7 Description

The PM5360 S/UNI MULTI-48 SATURN User Network Interface is a monolithic integrated circuit implementing SONET/SDH processing, ATM mapping and Packet over SONET mapping technology for a channelized[2] STS-48 (STM-16) 2488.32 Mbit/s stream, up to four channelized STS-12 (STM-4) 622.08 Mbit/s streams, or up to four STS-3 (STM-1) 155.52 Mbit/s streams. The S/UNI MULTI-48 device is configurable as a single 2488.32 Mbit/s stream aggregating one STS-48c (VC-4-16c) or a combination of STS-12c (VC-4-4c) and STS-3c (VC-4) streams. It can also be configured as a combination of four 622.08 Mbit/s and 155.52 Mbit/s streams aggregating STS-12c (VC-4-4c) and STS-3c (VC-4).

The S/UNI MULTI-48 device receives SONET/SDH streams using bit serial interfaces, recovers the clock and data, and processes section, line, and path overhead. It also performs framing (A1, A2) and de-scrambling functions, detects alarm conditions, and monitors section, line, and path bit interleaved parity (B1, B2, B3). The S/UNI MULTI-48 provides performance monitoring features including error count accumulation at each level as well as line and path remote error indication (M1, G1) accumulation. In addition, the device interprets the received payload pointers (H1, H2) and extracts the synchronous payload envelope (SPE) that carries the received ATM cells or POS frames.

When implementing an ATM UNI (user network interface) or NNI (network-network interface) in the receive direction, the S/UNI MULTI-48 device uses cell delineation to frame to the ATM payload. Idle/unassigned cells may be optionally dropped. Cells are also dropped when a header check sequence (HCS) error is detected. The ATM cell payloads are descrambled and written to a scalable FIFO buffer (programmable FIFO depth). The received cells are then read from the FIFO using a 32-bit wide UTOPIA Level 3 or POS-PHY Level 3 (clocked up to 104 MHz) data path interface. Erroneous received ATM cell headers are independently counted and accumulated for performance monitoring purposes.

When implementing packet transmission over a SONET/SDH link in the receive direction, the S/UNI MULTI-48 device extracts Packet over SONET (POS) frames from the SONET/SDH synchronous payload envelope. Frames are verified for correct construction and size and the control escape characters are removed. The frame check sequence is optionally verified for correctness and the extracted packets are placed in a receive scalable FIFO (programmable FIFO depth – all packets are 16 byte block aligned). The received packets are then read from the FIFO through a 32-bit POS-PHY Level 3 (clocked up to 104 MHz) system side interface. Valid and FCS (frame check sequence) erroneous packet counts are provided for performance monitoring. The S/UNI MULTI-48 Packet over SONET implementation is flexible enough to support several link layer protocols, including HDLC and PPP.

[2] channelized downto STS-3c (VC-4)

The S/UNI MULTI-48 device transmits SONET/SDH streams using a bit serial interface(s). In STS-48 (STM-16) mode, the S/UNI MULTI-48 device synthesizes the transmit clock from a 155.52 MHz frequency reference. In STS-12 (STM-4) and STS-3 (STM-1) modes, the S/UNI MULTI-48 synthesizes the transmit clock from a 77.76 MHz frequency reference. It performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and creates section, line, and path bit interleaved parity codes (B1, B2, and B3) as required for performance monitoring at the far end. Line and path remote error indications (M1, G1) are also inserted. The S/UNI MULTI-48 generates the payload pointer (H1, H2) and inserts the synchronous payload envelope that carries the ATM or POS frames. It also supports the insertion of a large variety of errors into the transmit stream, such as framing pattern errors, bit interleaved parity errors, and illegal pointers, which are useful for system diagnostics and tester applications. Any of the transmit streams can be loop-timed to their corresponding receive link.

When implementing an ATM UNI or NNI in the transmit direction, ATM cells are written to an internal scalable FIFO (programmable FIFO depth) using a 32-bit wide UTOPIA Level 3 or POS-PHY Level 3 (clocked up to 104 MHz) data path interface. Idle/unassigned cells are automatically inserted when the internal FIFO contains less than one complete cell. The S/UNI MULTI-48 device provides two transmit cell processing functions: header check sequence generation and payload scrambling of the ATM cells. Each of these functions can be enabled or bypassed.

When implementing a Packet over SONET/SDH link in the transmit direction, the S/UNI MULTI-48 device inserts POS frames into the SONET/SDH synchronous payload envelope. Packets to be transmitted are written into a scalable FIFO (with a programmable FIFO depth – all packets are 16-byte block aligned) through a 32-bit SATURN POS-PHY Level 3 (clocked up to 104 MHz) system side interface. POS frames are built by inserting the flags, control escape characters, and FCS fields. The CRC-CCITT or the CRC-32 can be computed and added to the frame. Several counters are provided for performance monitoring.

All transport overhead bytes can be inserted from or extracted to an external device through specialized I/O pins.

The S/UNI MULTI-48 device provides an APS (automatic protection switching) port to connect to a mate working or protection device. The APS interface is based on a specialized 8B/10B encoded LVDS interface that encodes the framing and path overhead positions, marks the AIS state, and guarantees transition density on the descrambled SONET/SDH payload. On both the working and protection devices, this APS functionality is performed on the system side of the path overhead processors and is timed with a common clock.

The S/UNI MULTI-48 device doesn't require line rate clocks because it synthesizes the transmit clock and recovers the receive clock using a 155.52 MHz reference clock (for STS-48/STM-16 mode) or a 77.76 MHz reference clock (for STS-12/STM-4 and STS-3/STM-1 modes). The S/UNI MULTI-48 outputs differential CML line data (TXD_P[4:1]/ TXD_N[4:1]).

The S/UNI MULTI-48 device is configured, controlled, and monitored with a generic 16-bit microprocessor bus interface. It also provides a standard five signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.

The S/UNI MULTI-48 device is implemented in low power, +1.8 Volt, CMOS technology. It has LVTTL/CMOS compatible digital inputs and LVTTL/CMOS compatible digital outputs. High speed inputs and outputs support 3.3 V compatible pseudo-ECL (PECL). The S/UNI MULTI-48 is packaged in a 500-ball UBGA package.

8 Pin Diagram

Figure 11 S/UNI MULTI-48 Pin Diagram: Top-Right Side Ball View

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Date: Aug 21 17:21:27 2002
VSS	D[15]	VSS	D[10]	D[4]	VSS	CSB	A[13]	A[10]	VSS	A[5]	A[0]	VDDI	VSS	VSS	A
STPA	D[14]	D[11]	D[6]	D[3]	INTB	ALE	A[11]	A[9]	A[6]	A[1]	CSUCLKO	VDDI	VSS	VSS	B
TCA_PTPA	D[13]	D[9]	VDDO	D[1]	WRB	VDDI_JAT4	VDDO	VDDI_JAT2	A[2]	VDDO	VDDO	VDDI	VDDI	VDDI	C
RSTB	VDDI	D[8]	D[5]	D[0]	VDDI	A[12]	A[7]	A[3]	VDDO	VSS	VDDI	VSS	VSS	VSS	D
PL3EN	D[12]	D[7]	D[2]	RDB	VDDI_JAT3	A[8]	A[4]	VDDO	VSS	VDDI	QAVD	CSUT_AVDL1	ATB[0]	ATB[1]	E
										CSUT_AVDL0	VSS	VDDI	VSS	VSS	F
										CSUT_AVDH	VSS	VSS	REFCLK77_N	REFCLK77_P	G
										CSUR_AVDL1	VDDO	VSS	VSS	VSS	H
										CSUR_AVDL0	REXT	VSS	TXD4_P	TXD4_N	J
										RXD4_N	RXD4_P	VSS	VSS	VSS	K
										CDRU_AVDL4	VSS	VDDI	TXD3_P	TXD3_N	L
										RXD3_N	RXD3_P	VSS	VSS	VSS	M
										CDRU_AVDL3	VSS	VSS	TXD2_P	TXD2_N	N
										RXD2_N	RXD2_P	VDDI	VSS	VSS	P
										CDRU_AVDL2	VSS	VSS	LCOUT_P	LCOUT_N	R

Figure 12 S/UNI MULTI-48 Pin Diagram: Bottom-Right Side Ball View

										LC_AVDL	CDRU_AVDL1	VSS	VSS	VSS	T
										AVDH_T2	QAVD_T	VSS	REFCLK155_N	REFCLK155_P	U
										AVDH_T1	VDDI_A	VSS	VSS	VSS	V
										C0_CSU	C1_CSU	VSS	VSS	TXD1_P	W
										AVDH_T0	VSS	VSS	VSS	TXD1_N	Y
										AVDH_R2	VDDI_A	VSS	VSS	VSS	AA
										ATP_LINE[0]	ATP_LINE[1]	VSS	RXD1_P	RXD1_N	AB
										AVDH_R1	VDDI_A	VSS	VSS	VSS	AC
										QAVD_R	AVDH_R0	VSS	C1_CRU	C0_CRU	AD
										VDDI_A	VSS	VDDI_A	VSS	VSS	AE
TTOHFP3	TTOH1	RTOHFP4	RTOHCLK3	RTOH1	RALM1	B3E4	SD4	STS48EN	VSS	VDDI	VSS	VSS	VSS	VSS	AF
TTOH2	VDDI	SD_TEST	RTOHCLK4	RTOH2	VDDI	SALM4	VDDI_JAT1	SD3	VDDO	VSS	VDDI	VSS	VSS	VSS	AG
TTOHCLK3	TTOHFP2	TTOHFP1	VDDO	RTOHFP2	RTOHFP1	RALM3	VDDO	B3E3	SD2	VSS	VSS	VDDI	VDDI	VDDI	AH
TTOHEN3	TTOHCLK2	TTOHEN1	RTOH4	RTOH3	RTOHCLK2	RALM4	SALM3	SALM1	B3E2	SD1	CRUCLKO	VDDI	VSS	VSS	AJ
VSS	TTOHEN2	VSS	TTOHCLK1	RTOHFP3	VSS	RTOHCLK1	RALM2	SALM2	VSS	B3E1	RCLKO	VDDI	VSS	VSS	AK
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Date: Aug 21 17:21:27 2002

Figure 13 S/UNI MULTI-48 Pin Diagram: Top-Left Side Ball View

Date: Aug 21 17:21:27 2002	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
A	VSS	VSS	VDDI	TPRTY	TENB	VSS	TDAT[5]	TDAT[9]	TDAT[12]	VSS	TDAT[20]	TDAT[26]	VSS	TDAT[31]	VSS
B	VSS	VSS	VDDI	TFCLK	TMOD[1]	TDAT[0]	TDAT[4]	TDAT[6]	TDAT[11]	TDAT[15]	TDAT[19]	TDAT[22]	TDAT[27]	TDAT[30]	TADR[0]
C	VDDI	VDDI	VDDI	VSS	TSX	TMOD[0]	TDAT[1]	VDDO	TDAT[10]	TDAT[14]	TDAT[17]	VDDO	TDAT[25]	TDAT[29]	TADR[1]
D	VDDO	VDDO	VSS	VDDI	VSS	VDDO	TERR	TDAT[2]	TDAT[7]	VDDI	TDAT[16]	TDAT[21]	TDAT[24]	VDDO	TADR[3]
E	TDI	TCK	VDDO	VSS	VDDI	VSS	TSOC_TSOP	TEOP	TDAT[3]	TDAT[8]	TDAT[13]	TDAT[18]	TDAT[23]	TDAT[28]	TADR[2]
F	VSS	TDO	TMS	VDDO	VSS										
G	RSX	VSS	TRSTB	VSS	VDDO										
H	RMOD[1]	RMOD[0]	VDDO	VSS	VSS										
J	RCA_RVAL	RERR	REOP	VSS	VDDO										
K	VSS	RPRTY	RSOC_RSOP	VDDI	VSS										
L	RDAT[29]	RDAT[30]	RDAT[31]	VSS	VDDO										
M	RDAT[26]	RDAT[28]	VDDO	VSS	VSS										
N	VSS	RDAT[25]	RDAT[27]	VSS	VDDO										
P	RDAT[22]	RDAT[23]	RDAT[24]	VDDI	VSS										
R	VSS	RDAT[20]	RDAT[21]	VSS	VDDO										

Figure 14 S/UNI MULTI-48 Pin Diagram: Bottom-Left Side Ball View

	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
T	VSS	RDAT[19]	RDAT[18]	VSS	VDDO										
U	RDAT[17]	RDAT[16]	RDAT[15]	VDDI	VSS										
V	VSS	RDAT[14]	RDAT[12]	VSS	VDDO										
W	RDAT[13]	RDAT[11]	VDDO	VSS	VSS										
Y	RDAT[10]	RDAT[9]	RDAT[8]	VSS	VDDO										
AA	VSS	RDAT[7]	RDAT[6]	VDDI	VSS										
AB	RDAT[5]	RDAT[4]	RDAT[3]	VSS	VDDO										
AC	RDAT[2]	RDAT[1]	VDDO	VSS	VSS										
AD	RDAT[0]	RFCLK	RADR[0]	VSS	VDDO										
AE	VSS	RADR[1]	RADR[3]	VDDO	VSS										
AF	RADR[2]	RENB	VDDO	VSS	VDDI	VSS	AVDL_A1	QAVD_A	APSI_P[2]	APSI_P[4]	APSO_P[1]	VSS	APSO_P[3]	APSOFP	TTOHCLK4
AG	VDDO	VDDO	VSS	VDDI	VSS	VDDO	AVDL_A2	CSU_AVDH	APSI_N[2]	APSI_N[4]	APSO_N[1]	VDDO	APSO_N[3]	APSIFP	TTOHEN4
AH	VDDI	VDDI	VDDI	VSS	AVDH_A0	RESK	VSS	VSS	VSS	VDDI	VSS	VSS	VSS	SYSCLK	TTOHFP4
AJ	VSS	VSS	VDDI	VSS	RES	AVDL_A0	APSI_P[1]	AVDL_A3	APSI_N[3]	AVDH_A1	APSO_P[2]	AVDH_A3	APSO_P[4]	TTOH4	TTOH3
AK	VSS	VSS	VDDI	ATP_APS[0]	ATP_APS[1]	VSS	APSI_N[1]	VSS	APSI_P[3]	AVDH_A2	APSO_N[2]	VSS	APSO_N[4]	VDDO	VSS

9 Pin Description

Note: By convention, if a bus has multiple pins, its index will indicate which quadrant the pin applies to. For example, for RXD_P[4:1], RXD_P[4] applies to quadrant #4, RXD_P[1] applies to quadrant #1, and so on.

9.1 Serial Line Side Interface Signals (26)

Pin Name	Type	Pin No.	Function
STS48EN	Input	AF7	The **STS-48 (STM-16) Line Selection** (STS48EN) input is used to select the expected REFCLK_P/REFCLK_N input. This input signal is internally logically XORed with the STS48ENB bit in register 001CH. When the resulting signal is logic 1, then a 155.52 MHz input clock is selected from REFCLK155_P/REFCLK155_N. When the resulting signal is logic 0, then a 77.76 MHz input clock is selected from REFCLK77_P/REFCLK77_N.
REFCLK155_P REFCLK155_N	Differential PECL - compatible Input	U1 U2	The differential **reference clock** inputs (REFCLK155_P / REFCLK155_N) provide a low-jitter 155.52 MHz reference clock for both the clock recovery and the clock synthesis circuits in STS-48 mode. The two PECL inputs are internally terminated with differential 100-Ω termination. <u>For STS-48 (STM-16) configuration:</u> The reference clock must be 155.52 MHz, with a duty cycle between 45% and 55%. In practice, jitter on REFCLK155_P/REFCLK155_N inputs must be less than 1 psec RMS, in 12kHz to 20MHz band, for the S/UNI MULTI-48 to comply with Telcordia GR-253 intrinsic jitter specs on transmit data outputs. REFCLK155_P/REFCLK155_N should be AC coupled PECL signals. REFCLK155_P/REFCLK155_N must be externally AC coupled with a 0.1 uF capacitor **Note:** Any jitter on REFCLK155_P / REFCLK155_N up to about 20 MHz will also appear at the transmit data output. <u>For STS-12 (STM-4) and STS-3 (STM-1) configurations:</u> REFCLK155_P/REFCLK155_N are not used in this mode. These pins can be left floating (or driven with any valid differential PECL signal) if the proper 2488 analog blocks are powered down appropiately. Refer to the Operation section for instructions on how to disable the needed analog blocks.

Pin Name	Type	Pin No.	Function
REFCLK77_P REFCLK77_N	Differential PECL - compatible Input	G1 G2	The differential **reference clock** inputs (REFCLK77_P/REFCLK77_N) provide a low-jitter 77.76 MHz reference clock for both the clock recovery and the clock synthesis circuits in quad mode. The two PECL inputs are internally terminated with differential 112-Ω termination. The REFCLK77_P/N can be at 3.3 V coupled PECL levels. <u>For STS-12 (STM-4) and STS-3 (STM-1) configurations:</u> For the device to comply with Telcordia GR-253 intrinsic jitter specification on transmit data outputs, REFCLK77 inputs should have jitter less than: 4x622 mode: 4ps rms (12kHz to 5MHz) (see note) 4x155 mode: 16ps rms (12kHz to 1.3MHz) (see note) mixed 155/622 mode: 4ps rms (12kHz to 5MHz) (see note) **Note**: If this clock is also used as a source for the APS CSU (SYSCLK pin disabled), then it should also have less than 5.4ps rms (in 12kHz to 20MHz band). <u>For STS-48 (STM-16) configuration:</u> REFCLK77_P/REFCLK77_N are not used in this mode. These pins can be left floating (or driven with any valid differential PECL signal) whenever STS-48 (STM-16) mode is enabled.
RXD_P[4] RXD_N[4] RXD_P[3] RXD_N[3] RXD_P[2] RXD_N[2] RXD_P[1] RXD_N[1]	Differential PECL-compatible Input	K4 K5 M4 M5 P4 P5 AB2 AB1	The **receive differential data** PECL-compatible inputs (RXD_P[4:1]/ RXD_N[4:1]) contain the NRZ bit serial receive stream. The two receive inputs are internally terminated with differential 100-Ω termination. The receive clock is recovered from the RXD_P/ RXD_N bit stream. For the STS-48 configuration, only the RXD_P[1]/RXD_N[1] is used. For the STS-12 (STM-4) and STS-3 (STM-1) configurations, RXD_P[4:1]/RXD_N[4:1] can either be 622.08 Mbit/s or 155.52 Mbit/s serial streams. RXD_P[4:1]/RXD_N[4:1] must be externally AC coupled with 0.1 uF capacitor. Note that most SFP optics modules already include this AC coupling capacitor.
SD[4] SD[3] SD[2] SD[1]	TTL Input	AF8 AG7 AH6 AJ5	The **receive signal detect** TTL inputs (SD[4:1]) indicate the presence of valid receive signal power from the Optical Physical Medium Dependent Device. A logic high indicates the presence of valid data. A logic low indicates a loss of signal. Unless SD[x] detection is disabled, deassertion of SD[x] will cause the 2488 CRU or the corresponding 622/155 DRU to go into training mode where it locks to REFCLK155_P/REFCLK155_N or REFCLK77_P/REFCLK77_N respectively. For STS-48 (STM-16) mode, only SD[1] is used.
SD_TEST	TTL Input	AG13	The SD TEST (SD_TEST) is used for PMC production test purposes only. It must be connected to ground during the normal mode of operation.

Pin Name	Type	Pin No.	Function
RCLKO	Output	AK4	The **receive clock** (RCLKO) signal provides timing reference for the receive interface. RCLKO is frequency locked with the receive line recovered data rate. This pin is driven by a digital pad and is not intended to be used as a clock source. To use this pin as a clock source, an external PLL is required to smooth the clock. RCLKO is a nominal 77.76 MHz 50% duty cycle clock in STS-48 (STM-16) mode. In quad 622/155 mode, the source and frequency of RCLKO depends on the selected channel number. RCLKO is a nominal 77.76 MHz 50% duty cycle clock when the selected channel is in STS-12 (STM-4) mode, and a nominal 19.44 MHz 50% duty cycle clock when the selected channel is in STS-3 (STM-1) mode.
TXD_P[4] TXD_N[4] TXD_P[3] TXD_N[3] TXD_P[2] TXD_N[2] TXD_P[1] TXD_N[1]	Differential CML-compatible Output	J2 J1 L2 L1 N2 N1 W1 Y1	The **transmit differential data** CML-compatible outputs (TXD_P[4:1]/ TXD_N[4:1]) contain the NRZ bit serial transmit streams. The TXD_P[x]/ TXD_N[x] outputs are driven using the synthesized clock from the CSU. These must be externally AC coupled with 0.1 uF capacitor. Note that most SFP optics modules already include this AC coupling capacitor. In STS-48 (STM-16) mode, only TXD_P[1]/TXD_N[1] is used. Signal swing is typically 2/3rd of the standard PECL levels but is compatible with the requirements of most optical modules.

9.2 Alarms Signals and B3 Error Indications (12)

Pin Name	Type	Pin No.	Function
SALM[4] SALM[3] SALM[2] SALM[1]	Output	AG9 AJ8 AK7 AJ7	The **section alarm** (SALM[4:1]) signals are set high when any of the following alarms are detected: out of frame (OOF), loss of signal (LOS), loss of frame (LOF), line alarm indication signal (AIS-L), line remote defect indication (RDI-L), section trace identifier mismatch (TIM-S), section trace identifier unstable (TIU-S), signal fail (SF), or signal degrade (SD). Each alarm indication can be independently enabled using bits in the corresponding SARC Section SALM Enable registers. SALM[x] is set low when none of the enabled alarms are active in the corresponding channel. For STS-48 (STM-16) mode, only SALM[1] is valid. SALM[4:1] are asynchronous output signals.
RALM[4] RALM[3] RALM[2] RALM[1]	Output	AJ9 AH9 AK8 AF10	The **Receive Alarm** (RALM[4:1]) signals contain the alarm outputs of the receive path. Each alarm represents the logical OR of the SALM, LOP-P, AIS-P, RDI-P, ERDI-P, LOPC-P, PAISC-P, UNEQ-P, PSLU, PSLM, PDI-P, TIU-P, TIM-P, and LCD status of the path. The selection of alarms to be reported is controlled by the corresponding SARC Path RALM Enable registers. For STS-48c (VC-4-16c) mode, only RALM[1] is valid. RALM[x] is updated on the falling edge of RTOHCLK[x].

Pin Name	Type	Pin No.	Function
B3E[4] B3E[3] B3E[2] B3E[1]	Output	AF9 AH7 AJ6 AK5	The **bit interleaved parity error** (B3E[4:1]) signals carry the path BIP-8 errors detected for the STS-Nc SONET payload. B3E[x] will toggle for each STS-Nc path BIP-8 error detected (up to eight errors per path per frame). When BIP-8 errors are treated on a block basis, the B3E signal will only toggle once per frame to indicate up to eight path BIP-8 errors. Path BIP-8 errors are detected by comparing the extracted path BIP-8 byte (B3) with the computed path BIP-8 byte of the previous frame. For STS-48c (VC-4-16c) mode, only B3E[1] is valid. B3E[x] is updated on the falling edge of RTOHCLK[x].

9.3 Receive Section/Line Overhead Extraction Signals (12)

Pin Name	Type	Pin No.	Function
RTOHCLK[4] RTOHCLK[3] RTOHCLK[2] RTOHCLK[1]	Output	AG12 AF12 AJ10 AK9	The **receive transport overhead clock** (RTOHCLK[4:1]) signals provide timing for the receive transport overhead. RTOHCLK[x] is a 6.48 MHz clock gapped down to 5.184 MHz in STS-3 (STM-1) mode or a 25.92 MHz clock gapped down to 20.736 MHz in STS-12 (STM-4) and STS-48 (STM-16) mode. RTOHCLK[x] has a 33% high duty cycle. RTOH[x] and RTOHFP[x] are updated on the falling edge of RTOHCLK[x].
RTOHFP[4] RTOHFP[3] RTOHFP[2] RTOHFP[1]	Output	AF13 AK11 AH11 AH10	The **receive transport overhead frame pulse** (RTOHFP[4:1]) signals provide references for the receive section and line overhead extraction. RTOHFP[x] is used to indicate the most significant bit (MSB) on RTOH[x] and to synchronize RALM[X] and B3E[X]. RTOHFP[x] can be sampled on the rising edge of RTOHCLK[x].
RTOH[4] RTOH[3] RTOH[2] RTOH[1]	Output	AJ12 AJ11 AG11 AF11	The **receive transport overhead** (RTOH[4:1]) signals contain all of the received transport overhead bytes (A1, A2, J0, Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, Z1/S1, Z2/M1, E2, and unused bytes). RTOH[x] is updated on the falling edge of RTOHCLK[x].

9.4 Transmit Section/Line Overhead Insertion Signals (16)

Pin Name	Type	Pin No.	Function
TTOHCLK[4] TTOHCLK[3] TTOHCLK[2] TTOHCLK[1]	Output	AF16 AH15 AJ14 AK12	The **transmit transport overhead clock** (TTOHCLK[4:1]) signals provide timing for the transmit section, and line overhead insertion. TTOHCLK[x] is a 6.48 MHz clock gapped down to 5.184 MHz in STS-3 (STM-1) mode or a 25.92 MHz clock gapped down to 20.736 MHz in STS-12 (STM-4) or STS-48 mode. TTOHCLK[x] has a 33% high duty cycle. TTOHFP[x] is updated on the falling edge of TTOHCLK[x]. TTOH[x] and TTOHEN[x] are sampled on the rising edge of TTOHCLK[x].
TTOHFP[4] TTOHFP[3] TTOHFP[2] TTOHFP[1]	Output	AH16 AF15 AH14 AH13	The **transmit transport overhead frame pulse** (TTOHFP[4:1]) signals provide timing for the transmit section and line overhead insertion. TTOHFP[x] is set high when the MSB of the first A1 byte should be present on TTOH[x]. TTOHFP[x] is updated on the falling edge of TTOHCLK[x].
TTOH[4] TTOH[3] TTOH[2] TTOH[1]	Input	AJ17 AJ16 AG15 AF14	The **transmit transport overhead** (TTOH[4:1]) signals contain the transport overhead bytes (A1, A2, J0, Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, Z1/S1, Z2/M1, E2, and unused bytes) to be transmitted and the error masks to be applied on B1, B2, H1, and H2. TTOH[x] must be grounded if not in use. TTOH[x] is sampled on the rising edge of TTOHCLK[x].

Pin Name	Type	Pin No.	Function
TTOHEN[4] TTOHEN[3] TTOHEN[2] TTOHEN[1]	Input	AG16 AJ15 AK14 AJ13	The active high **transmit transport overhead enable** (TTOHEN[4:1]) signals enable, on a byte-by-byte basis, the transport overhead insertion from TTOH[4:1]. When TTOHEN[x] is high during the most significant bit of a byte on TTOH[x], the sampled byte is inserted into the corresponding transport overhead byte positions (A1, A2, J0, Z0, E1, F1, D1-D3, H3, K1, K2, D4-D12, Z1/S1, Z2/M1, and E2 bytes). When TTOHEN[x] is low during the most significant bit of a byte on TTOH[x], the sampled byte is ignored and the default values are inserted into the transport overhead bytes. When TTOHEN[x] is high during the most significant bit of the H1, H2, B1, or B2 byte positions on TTOH[x], the sampled byte is logically XORed with the associated incoming byte. This will force bit errors on the outgoing byte. A logic low bit in the TTOH[x] byte allows the incoming bit to go through while a bit set to logic high will toggle the outgoing bit. A low level on TTOHEN[x] during the MSB of the byte disables the error forcing for the entire byte. TTOHEN[x] must be grounded if it is not used. TTOHEN[x] can be aligned externally with the falling edge of TTOHCLK[x]. TTOHEN[x] is sampled on the rising edge of TTOHCLK[x].

9.5 System Side UTOPIA and POS-PHY L3 Signals (94)

Pin Name	Type	Pin No.	Function
PL3EN	Input	E15	The **UTOPIA/POS-PHY interface select (**PL3EN**)** signal selects between UTOPIA Level 3 and POS-PHY Level 3 modes for the system side interface. The PL3EN input signal is internally logically XORed with the PL3EN bit of register 0004H. When the resulting PL3EN is logic 0, the UTOPIA Level 3 interface is selected. When the resulting PL3EN is logic 1, the POS-PHY Level 3 interface is selected.
RFCLK	Input	AD29	The **UTOPIA receive FIFO read clock** (RFCLK) signal is used to read ATM cells from the receive cell FIFO. RFCLK is expected to cycle between 60 MHz and 104 MHz.
			The **POS-PHY receive FIFO read clock** (RFCLK) signal is used to read packet data from the receive packet FIFO. RFCLK is expected to cycle between 60 MHz and 104 MHz.
RPRTY	Output	K29	The **UTOPIA receive parity** (RPRTY) signal indicates the parity of the RDAT[31:0] bus. Odd or even parity may be selected. RPRTY is valid only when RENB has been sampled low in the previous clock cycle. RPRTY is updated on the rising edge of RFCLK.

Pin Name	Type	Pin No.	Function
			The **POS-PHY receive parity** (RPRTY) signal indicates the parity of the RDAT[31:0] bus. Odd or even parity may be selected. RPRTY is valid only when either RVAL or RSX are asserted. RPRTY is updated on the rising edge of RFCLK.
RDAT[31:0]	Output	L28 L29 L30 M29 N28 M30 N29 P28 P29 P30 R28 R29 T29 T28 U30 U29 U28 V29 W30 V28 W29 Y30 Y29 Y28 AA29 AA28 AB30 AB29 AB28 AC30 AC29 AD30	The **UTOPIA receive cell data** (RDAT[31:0]) bus carries the ATM cell octets that are read from the receive FIFO. RDAT[31:24] contains the most significant byte in the word. RDAT[31:0] is updated on the rising edge of RFCLK. The **POS-PHY receive packet data** (RDAT[31:0]) bus carries the POS packet octets that are read from the receive FIFO. The RDAT[31:0] signals are valid when RVAL and RENB are asserted. RDAT[31:24] contains the most significant byte in the word. RDAT[31:0] is updated on the rising edge of RFCLK.
RENB	Input	AF29	The **UTOPIA receive read enable** (RENB) signal is used to initiate reads from the receive FIFO. RENB can only be asserted and de-asserted as specified in the ATM Forum's UTOPIA Level 3 Specification. A read is not performed and RDAT[31:0] does not change when RENB is sampled high. When RENB is sampled low, the word on the RDAT[31:0] bus is read from the receive FIFO and RDAT[31:0] changes to the next value on the next clock cycle. RENB is sampled on the rising edge of RFCLK.

Pin Name	Type	Pin No.	Function
			The **POS-PHY receive read enable** (RENB) signal is used to initiate reads from the receive FIFO. During a data transfer, RVAL must be monitored since it will indicate if the data is valid. The system may deassert RENB at any time if it is unable to accept more data. A read is not performed and RDAT[31:0] does not change when RENB is sampled high. When RENB is sampled low, the word on the RDAT[31:0] bus is read from the receive FIFO and RDAT[31:0] changes to the next value on the next clock cycle. RENB is sampled on the rising edge of RFCLK.
RSOC	Output	K28	The **UTOPIA receive start of cell** (RSOC) signal marks the start of a cell structure on the RDAT[31:0] bus. The first word of the cell structure is present on the RDAT[31:0] bus when RSOC is high. RSOC is updated on the rising edge of RFCLK.
RSOP			The **POS-PHY receive start of packet** (RSOP) signal indicates the start of a packet on the RDAT[31:0] bus. RSOP is set high for the first word of a packet on RDAT[31:0]. RSOP is updated on the rising edge of RFCLK
RCA	Output	J30	The **UTOPIA receive cell available (RCA)** signal can be polled to provide status indication of when a cell is available in the receive FIFO. RCA will be high two cycles after a channel address is presented on RADR[3:0] to indicate that a cell can be read out of that channel. If no cell is available for that channel, RCA will be low two cycles after RADR[3:0] is presented. RCA is updated on the rising edge of RFCLK.
RVAL			The **POS-PHY receive data valid** (RVAL) signal indicates the validity of the receive data signals. When RVAL is high, the receive signals, RDAT[31:0], RPRTY, RSOP, REOP, RMOD[1:0], and RERR are valid. When RVAL is low, all receive signals are invalid and must be disregarded. RVAL will be high when there is valid data on the RDAT[31:0] bus. RVAL will transition low when the FIFO has no data to transfer. RVAL will remain low until a programmable minimum number of bytes or an end-of-packet (EOP) exists in the receive FIFO. The threshold is configurable. RVAL is updated on the rising edge of RFCLK.
RADR[3] RADR[2] RADR[1] RADR[0]	Input	AE28 AF30 AE29 AD28	The **UTOPIA receive channel select (RADR[3:0])** signal selects the channel whose cell FIFO status is to be polled using RCA or selects the channel for which a cell transfer is desired. RADR[3:0] is sampled on the rising edge of RFCLK.

Pin Name	Type	Pin No.	Function
RERR	Output	J29	The **POS-PHY receive error** (RERR) signal indicates that the current packet is invalid due to an error such as invalid FCS, excessive length, or received abort. RERR only asserts when REOP is asserted, marking the last word of the packet. RERR is only used in POS-PHY Level 3 mode and is updated on the rising edge of RFCLK.
REOP	Output	J28	The **POS-PHY receive end of packet** (REOP) signal marks the end of packet on the RDAT[31:0] bus. It is legal for RSOP to be high at the same time REOP is high. REOP is set high to mark the last word of the packet presented on the RDAT[31:0] bus. When REOP is high, RMOD[1:0] specifies if the last word has 1, 2, 3, or 4 valid bytes of data. REOP is only used in POS-PHY Level 3 mode and is updated on the rising edge of RFCLK.
RMOD[1] RMOD[0]	Output	H30 H29	The **POS-PHY receive modulo** (RMOD[1:0]) bus indicates the size of the current word when configured for POS-PHY Level 3 mode. During a packet transfer, every word on RDAT[31:0] must contain four valid bytes of packet data except at the end of the packet where the word is composed of 1, 2, 3, or 4 valid bytes. The number of valid bytes in this last word is specified by RMOD[1:0]. RMOD[1:0] = “00” RDAT[31:0] valid RMOD[1:0] = “01” RDAT[31:8] valid RMOD[1:0] = “10” RDAT[31:16] valid RMOD[1:0] = “11” RDAT[31:24] valid RMOD[1:0] is considered valid only when RVAL is asserted. RMOD[1:0] is only used in POS-PHY Level 3 operation and is updated on the rising edge of RFCLK.
RSX	Output	G30	The **POS-PHY receive start of transfer** (RSX) signal indicates the start of a packet transfer. When RSX is high, the channel number being transferred is indicated on RDAT[31:0]. RSX is only used in POS-PHY Level 3 mode and is updated on the rising edge of RFCLK.
TFCLK	Input	B27	The **UTOPIA transmit FIFO write clock** (TFCLK) signal is used to write ATM cells to the transmit FIFO. TFCLK is expected to cycle between 60 MHz and 104 MHz rate. The **POS-PHY transmit FIFO write clock** (TFCLK) signal is used to write packet data into the transmit packet FIFO. TFCLK is expected to cycle between 60 MHz and 104 MHz rate.
TADR[3] TADR[2] TADR[1] TADR[0]	Input	D16 E16 C16 B16	The **UTOPIA transmit channel select (TADR[3:0])** signal selects the channel whose cell FIFO status is to be polled using TCA or selects the channel for which a cell transfer is desired. TADR[3:0] is sampled on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
			The **POS-PHY polled channel select (TADR[3:0])** signal selects the channel whose FIFO status is polled using PTPA. TADR[3:0] is sampled on the rising edge of TFCLK.
TDAT[31:0]	Input	A17 B17 C17 E17 B18 A19 C18 D18 E18 B19 D19 A20 B20 E19 C20 D20 B21 C21 E20 A22 B22 C22 A23 E21 D22 B23 A24 B24 E22 D23 C24 B25	The **UTOPIA transmit cell data** (TDAT[31:0]) bus carries the ATM cell octets that are written to the transmit FIFO. TDAT[31:0] is considered valid only when TENB is asserted at the same time. TDAT[31:0] is sampled on the rising edge of TFCLK.
			The **POS-PHY transmit packet data** (TDAT[31:0]) bus carries the POS packet octets that are written to the transmit FIFO. The TDAT[31:0] bus is considered valid only when TENB is asserted at the same time. TDAT[31:0] is sampled on the rising edge of TFCLK.
TPRTY	Input	A27	The **UTOPIA transmit bus parity** (TPRTY) signal indicates the parity on the TDAT[31:0] bus. A parity error is indicated by a status bit and a maskable interrupt. Cells with parity errors are still inserted in the transmit stream, so the TPRTY input may be unused. Odd or even parity may be selected. TPRTY is considered valid only when TENB is asserted at the same time. TPRTY is sampled on the rising edge of TFCLK.
			The **POS-PHY transmit bus parity** (TPRTY) signal indicates the parity on the TDAT[31:0] bus. A parity error is indicated by a status bit and a maskable interrupt. Packets with parity errors are still inserted in the transmit stream, so the TPRTY input may be unused. Odd or even parity may be selected. TPRTY is considered valid only when TENB or TSX is asserted at the same time. TPRTY is sampled on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
TSOC	Input	E24	The **UTOPIA transmit start of cell** (TSOC) signal marks the start of a cell structure on the TDAT[31:0] bus. The first word of the cell structure is present on the TDAT[31:0] bus when TSOC is high. TSOC must be present for each cell. TSOC is considered valid only when TENB is asserted at the same time. TSOC is sampled on the rising edge of TFCLK.
TSOP			The **POS-PHY transmit start of packet** (TSOP) signal indicates the start of a packet on the TDAT[31:0] bus. TSOP is required to be present at all instances for proper operation. TSOP must be set high for the first word of a packet on TDAT[31:0]. TSOP is considered valid only when TENB is asserted at the same time. TSOP is sampled on the rising edge of TFCLK.
TENB	Input	A26	The **UTOPIA transmit write enable** (TENB) signal is an active low input used to initiate writes to the transmit FIFOs. TENB can only be asserted and de-asserted as specified in the ATM Forum's UTOPIA Level 3 Specification. When TENB is sampled high, the information sampled on the TDAT[31:0], TPRTY, and TSOC signals are invalid. When TENB is sampled low, the information sampled on the TDAT[31:0], TPRTY, and TSOC signals is valid and written into the transmit FIFO. TENB is sampled on the rising edge of TFCLK.
			The **POS-PHY transmit write enable** (TENB) signal is an active low input used to initiate writes to the transmit FIFOs. When TENB is sampled high, the information sampled on the TDAT[31:0], TPRTY, TSOP, TEOP, TMOD[1:0], and TERR signals is invalid. When TENB is sampled low, the information sampled on the TDAT[31:0], TPRTY, TSOP, TEOP, TMOD[1:0], and TERR signals is valid and is written into the transmit FIFO. TENB is sampled on the rising edge of TFCLK.
TCA	Output	C15	The **UTOPIA transmit cell available** (TCA) signal can be polled to provide status indication of when room exists to receive a cell in the transmit FIFO. TCA is high two cycles after a FIFO address is presented on TADR[3:0], indicating that a cell can be written into that FIFO. If no space is available for that FIFO, TCA will be low two cycles after TADR[3:0] is presented. TCA is updated on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
PTPA			The **POS-PHY polled transmit packet available** (PTPA) signal provides status indication on the fill status of the polled (using TADR[3:0]) transmit FIFO. Note**:** regardless of what fill level PTPA is set to indicates as "full" the FIFO still has the ability to store data up to its actual capacity. When PTPA transitions high, it indicates that the polled transmit FIFO has enough room to store a configurable number of data bytes. When PTPA transitions low, it indicates that the polled transmit FIFO is either full or near full as configured. PTPA is updated on the rising edge of TFCLK.
STPA	Output	B15	The **POS-PHY selected-PHY Transmit Packet Available (STPA)** provides FIFO status indication for the selected channel of the S/UNI MULTI-48 . STPA is asserted when the minimum number of bytes (user programmable) are available in the transmit FIFO specified by the in-band address on TDAT[31:0]. Once asserted, STPA indicates the transmit FIFO is not full. When STPA deasserts, it indicates that the transmit FIFO is full or near full (user programmable). STPA is updated on the rising edge of TFCLK.
TEOP	Input	E23	The **POS-PHY transmit end of packet** (TEOP) signal marks the end of packet on the TDAT[31:0] bus when configured for packet data. The TEOP signal marks the last word of a packet on the TDAT[31:0] bus. The TMOD[1:0] signal indicates how many bytes are in the last word. It is legal to set TSOP high at the same time as TEOP high in order to support 1, 2, 3, or 4 byte packets. TEOP is only valid when TENB is simultaneously asserted. TEOP is only used in POS-PHY Level 3 mode and is sampled on the rising edge of TFCLK.
TERR	Input	D24	The **POS-PHY transmit error** (TERR) signal indicates that the current packet must be aborted. Packets marked with TERR will have the abort sequence appended when transmitted. TERR should only be asserted during the last word of the packet being transferred on TDAT[31:0]. TERR is only considered valid when TENB and TEOP are asserted at the same time. TERR is only used in POS-PHY Level 3 mode and is sampled on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
TSX	Input	C26	The **POS-PHY transmit start of transfer (TSX)** signal indicates the start of a packet transfer. When TSX is high, the channel number to be selected for transfers is expected to be present on TDAT[31:0]. TSX is only used in POS-PHY Level 3 mode and is sampled on the rising edge of TFCLK. TSX must be tied to logic 0 when UTOPIA Level 3 mode is used. **Note:** All TSX assertions are considered valid, regardless of TENB. Thus, TSX must only be asserted when TENB is deasserted. For single PHY applications, TSX is optional and can be tied to logic 0 if INBANDADDR is set to logic 0 (Register 1330H).
TMOD[1] TMOD[0]	Input	B26 C25	The **POS-PHY transmit word modulo** (TMOD[1:0]) bus indicates the size of the current word when configured for packet mode. During a packet transfer, every word on TDAT[31:0] must contain four valid bytes of packet data except at the end of the packet where the word is composed of 1, 2, 3, or 4 valid bytes. The number of valid bytes in this last word is specified by TMOD[1:0] TMOD[1:0] = “00” TDAT[31:0] valid TMOD[1:0] = “01” TDAT[31:8] valid TMOD[1:0] = “10” TDAT[31:16] valid TMOD[1:0] = “11” TDAT[31:24] valid TMOD[1:0] is considered valid only when TENB is asserted at the same time. TMOD[1:0] is only used in POS-PHY Level 3 mode and is sampled on the rising edge of TFCLK.

9.6 System Clock and APS Serial Data Interface (19)

Pin Name	Type	Pin No.	Function
SYSCLK	Input	AH17	The **system reference clock** (SYSCLK) signal provides a low-jitter 77.76 MHz reference clock used to clock the system side of the S/UNI MULTI-48 device, sample the APS input frame pulse (APSIFP), and serve as a reference for the 777.6 MHz Clock Synthesis Unit of the APS Port. Jitter on SYSCLK input must be less than 5.4 psec RMS, in 12kHz to 20MHz band. SYSCLK is optional. When not used, this input can be grounded and the internal system side of the S/UNI MULTI-48 can be run with an internally generated 77.76 MHz clock derived from REFCLK77_P/N or REFCLK155_P/N. **Note:** In STS-48 (STM-16) looptime enabled mode, when the SYSCLK pin is disabled, the internal system clock is sourced from the recovered Line clock, not REFCLK155_P/N. Thus, SYSCLK must be enabled in order to use the APS port when the S/UNI MULTI-48 is configured in STS-48 (STM-16) looptime mode. This restriction does not apply to STS-12 (STM-4) and STS-3 (STM-1) configurations.
APSI_P[4] APSI_N[4] APSI_P[3] APSI_N[3] APSI_P[2] APSI_N[2] APSI_P[1] APSI_N[1]	Analog LVDS Compatible Input	AF21 AG21 AK22 AJ22 AF22 AG22 AJ24 AK24	The differential **APSI** input (APSI_P/ APSI_N[4:1]) serial data links carry SONET/SDH STS-48 (STM-16), STS-12 (STM-4), and/or STS-3 (STM-1) frame data from a mate in bit serial format. Each differential pair has the capacity of one STS-12(STM-4). Data on APSI_P/ APSI_N[4:1] is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is transmitted first and bit 'j' is transmitted last. The four differential pairs in APSI_P/ APSI_N[4:1] are frequency locked to SYSCLK (or to an internally generated 77.76 MHz clock derived from REFCLK77_P/N or REFCLK155_P/N when SYSCLK is not used). The four differential pairs are not phase locked to each other. APSI_P/ APSI_N[4:1] are nominally 777.6 Mbit/s data streams. When a given APSI_P/APSI_N[X] differential pair is unused, APSI_P[X] must be tied to ground and APSI_N[X] must be tied to 1.8V or 3.3V with R=4.7kΩ.
APSIFP	Input	AG17	The **APS input frame pulse** signal (APSIFP) provides a system reference for the APS input serial interface. APSIFP is set high once every 9720 SYSCLK cycles, or multiple thereof, to indicate that the J0 frame boundary 8B/10B character has been delivered on the differential LVDS bus (APSI_P/ APSI_N[4:1]). APSIFP is optional. APSIFP is sampled on the rising edge of SYSCLK when SYSCLK is enabled. APSIFP's rising edge is detected to indicate the J0 frame boundary when SYSCLK is not provided to the S/UNI MULTI-48. In both cases, when enabled, APSIFP must always be frequency locked to the APS data rate.

Pin Name	Type	Pin No.	Function
APSO_P[4] APSO_N[4] APSO_P[3] APSO_N[3] APSO_P[2] APSO_N[2] APSO_P[1] APSO_N[1]	Analog LVDS Compatible Output	AJ18 AK18 AF18 AG18 AJ20 AK20 AF20 AG20	The differential **APS output** (APSO_P/ APSO_N[4:1]) serial data links carry SONET/SDH STS-48 (STM-16), STS-12 (STM-4), and/or STS-3 (STM-1) frame data to a mate in bit serial format. Each differential pair has the capacity of one STS-12(STM-4). Data on APSO_P/ APSO_N[4:1] is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is received first and bit 'j' is received last. The four differential pairs in APSO_P/ APSO_N[4:1] are frequency locked to SYSCLK (or to an internally generated 77.76 MHz clock derived from REFCLK77_P/N or REFCLK155_P/N when SYSCLK is not used). The differential pairs are not phase locked to each other. APSO_P/ APSO_N[4:1] are nominally 777.6 Mbit/s data streams.
APSOFP	Output	AF17	The **APS output frame pulse** signal (APSOFP) provides system timing for the APS output serial interface. APSOFP is set high once every 9720 SYSCLK (or internally generated 77.76MHz clock derived from REFCLK77_P/N or REFCLK155_P/N when SYSCLK is not used) cycles to indicate the **approximate** location of the J0 frame boundary 8B/10B character on the differential LVDS bus (APSO_P/ APSO_N[4:1]). This signal cannot be used as a source for APSIFP. Note that APSOFP can sometimes be up to 4 SYSCLK (or internally generated 77.76MHz clock derived from REFCLK77_P/N or REFCLK155_P/N when SYSCLK is not used) cycles wide, and could also be asserted twice within this possible 4 clock cycles range. APSOFP is updated on the rising edge of SYSCLK or the internal 77.76 MHz system clock.

9.7 Microprocessor Interface and Test Signals(37)

Pin Name	Type	Pin No.	Function
CSB	CMOS/TTL compatible Schmitt Input	A9	The active low **chip select** (CSB) signal is low during S/UNI MULTI-48 register accesses. Note that when not being used, CSB must be tied low. If CSB is not required (i.e. register accesses controlled using the RDB and WRB signals only), CSB must be connected to an inverted version of the RSTB input.
RDB	Input	E11	The active low **read enable** (RDB) signal is low during S/UNI MULTI-48 register read accesses. The S/UNI MULTI-48 drives the D[15:0] bus with the contents of the addressed register while RDB and CSB are low.
WRB	Input	C10	The active low **write strobe** (WRB) signal is low during S/UNI MULTI-48 register write accesses. The D[15:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low (or the rising CSB edge when WRB is low).

Pin Name	Type	Pin No.	Function
D[15] D[14] D[13] D[12] D[11] D[10] D[9] D[8] D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O	A14 B14 C14 E14 B13 A12 C13 D13 E13 B12 D12 A11 B11 E12 C11 D11	The bi-directional **data bus**, D[15:0], is used during S/UNI MULTI-48 read and write accesses.
A[13]/TRS	Input	A8	The **test register select** signal (TRS) selects between normal and test mode register accesses. TRS is high during test mode register accesses and is low during normal mode register accesses. TRS may be tied low.
A[12] A[11] A[10] A[9] A[8] A[7] A[6] A[5] A[4] A[3] A[2] A[1] A[0]	Input	D9 B8 A7 B7 E9 D8 B6 A5 E8 D7 C6 B5 A4	The **address** bus (A[12:0]) selects specific registers during S/UNI MULTI-48 register accesses.
RSTB	CMOS/TTL compatible Schmitt Input	D15	The active low **reset** (RSTB) signal provides an asynchronous S/UNI MULTI-48 reset. RSTB is a Schmitt triggered input with an internal pull-up resistor.
ALE	Input	B9	The **address latch enable** (ALE) is an active-high signal that latches the address bus A[13:0] when low. When ALE is high, the internal address latches are transparent. ALE allows the S/UNI MULTI-48 to interface to a multiplexed address/data bus. The ALE input has an internal pull-up resistor.
INTB	OD Output	B10	The active low **interrupt** (INTB) signal is set low when a S/UNI MULTI-48 enabled interrupt source is active. The S/UNI MULTI-48 may be enabled to report many alarms or events via interrupts. INTB is tri-stated when the interrupt is acknowledged via the appropriate register access. INTB is an open drain output.

9.8 JTAG Test Access Port (TAP) Signals (5)

Pin Name	Type	Pin No.	Function
TCK	CMOS/TTL compatible Schmitt Input	E29	The **test clock** (TCK) signal provides timing for test operations that are carried out using the IEEE P1149.1 test access port.
TMS	Input	F28	The **test mode select** (TMS) signal controls the test operations that are carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an internal pull-up resistor.
TDI	Input	E30	When the S/UNI MULTI-48 is configured for JTAG operation, the **test data input** (TDI) signal carries test data into the S/UNI MULTI-48 via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an internal pull-up resistor.
TDO	Tristate Output	F29	The **test data output** (TDO) signal carries test data out of the S/UNI MULTI-48 via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output that is inactive except when scanning of data is in progress.
TRSTB	CMOS/TTL compatible Schmitt Input	G28	The active low **test reset** (TRSTB) signal provides an asynchronous S/UNI MULTI-48 test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an internal pull-up resistor. Note that for normal device operation, the boundary scan state machine must be reset. This can be done either by pulling TRSTB low through a 4.7 k (or smaller value) resistor or by strobing TRSTB low at the same time as the active-low chip reset pin. If the boundary scan state machine is not reset, some or all device I/O pins may be held in test modes.

9.9 Analog Miscellaneous Signals (15)

Pin Name	Type	Pin No.	Function
ATP_LINE[0] ATP_LINE[1] ATP_APS[0] ATP_APS[1] ATB[0] ATB[1]	Analog	AB5 AB4 AK27 AK26 E2 E1	Six **analog test ports** are provided for production testing only. These pins must be left unconnected during normal operation. ATP_LINE[1:0] are the test ports for the 2488 Mbit/s line-side analog circuitry. ATP_APS[1:0] are the test ports for the 777.6 MHz LVDS APS analog circuitry. ATB[1:0] are only used in quad 622/155 Mbit/s mode for production testing.
C0_CRU C1_CRU	Analog	AD1 AD2	The analog **C0_CRU** and **C1_CRU** pins are reserved for an external capacitor for the STS-48 clock recovery unit. A 10 nF non-polarized capacitor across the two pins is required for all applications. The C0_CRU and C1_CRU pins must not be left floating (no connection).
C0_CSU C1_CSU	Analog	W5 W4	The analog **C0_CSU** and **C1_CSU** pins are reserved for an external capacitor for the STS-48 clock synthesis unit. A 100 nF capacitor must be placed between these two pins. The C0_CSU and C1_CSU pins must not be left floating (no connection).

Pin Name	Type	Pin No.	Function
RES RESK	Analog	AJ26 AH25	The **Reference Resistor Connection** (RES/RESK) is an off-chip 3.16 kΩ ±1% resistor connected between the positive resistor reference pin RES and a Kelvin ground contact RESK for the APS port LVDS reference. An on-chip negative feedback path will force the 0.8 V VREF voltage onto RES, thereby forcing 252 µA of current to flow through the resistor. RESK is electrically connected to VSS within the block, but should not be connected to VSS, either on-chip or off-chip.
REXT	Analog	J4	The **external resistor pin** (REXT) should be connected to an off-chip resistor of 10kΩ (±1%). It is used to set internal reference currents for use in the 4x622/155 analog block. The other side of the external resistor should be connected to a low impedance PCB ground. REXT is used in quad 622/155 mode only.
LCOUT_P / LCOUT_N	Analog	R2 R1	The two **analog test ports** are provided for reserved debug testing only. These two pins must be left unconnected during normal operation. These pins are ESD protected and latchup compliant. They are only used for testing.
CSUCLKO	TTL Tristate Output	B4	The **T-CSU output clock** (CSUCLKO) is used for PMC test purposes only. It must be left as a no-connect (NC) during the normal mode of operation.
CRUCLKO	TTL Tristate Output	AJ4	The **CRU output clock** (CRUCLKO) is used for PMC test purposes only. It must be left as a no-connect (NC) during the normal mode of operation.

9.10 Analog Power

Pin Name	Pin Type	PIN No.	Function
AVDH_T2 AVDH_T1 AVDH_T0 AVDH_R2 AVDH_R1 AVDH_R0 AVDH_A3 AVDH_A2 AVDH_A1 AVDH_A0 CSUT_AVDH CSU_AVDH	Analog Power	U5 V5 Y5 AA5 AC5 AD4 AJ19 AK21 AJ21 AH26 G5 AG23	The **analog power** (AVDH) pins are used for the analog core. The AVDH pins should be connected through passive filtering networks to a well-decoupled +3.3 V analog power supply. Refer to the Operation section for detailed information.

Pin Name	Pin Type	PIN No.	Function
AVDL_A3 AVDL_A2 AVDL_A1 AVDL_A0 CSUT_AVDL1 CSUT_AVDL0 CSUR_AVDL1 CSUR_AVDL0 CDRU_AVDL4 CDRU_AVDL3 CDRU_AVDL2 CDRU_AVDL1	Analog Power	AJ23 AG24 AF24 AJ25 E3 F5 H5 J5 L5 N5 R5 T4	The **analog power** (AVDL) pins are used for the analog core. The AVDL pins should be connected through passive filtering networks to a well-decoupled +1.8 V analog power supply. Refer to the Operation section for detailed information.
LC_AVDL	Analog Power	T5	The LC_AVDL pin should be grounded completely.
QAVD_T QAVD_R QAVD_A QAVD	Analog Power	U4 AD5 AF23 E4	The **quiet power** (QAVD) pins are used for the analog core. QAVD should be connected to a well-decoupled analog +3.3 V supply.
VDDI_A[4:0]	Analog Power	V4 AA4 AC4 AE5 AE3	The **analog blocks power** (VDDI_A) pins should be connected to a well-decoupled +1.8 V analog power supply.

9.11 Digital Power

Pin Name	Pin Type	PIN No.	Function
VDDI[40:0]	Core Power	A28 A3 B28 B3 C30 C29 C28 C3 C2 C1 D27 D21 D14 D10 D4 E26 E5 F3 K27 L3 P27 P3 U27 AA27 AF26 AF5 AG27 AG14 AG10 AG4 AH30 AH29 AH28 AH21 AH3 AH2 AH1 AJ28 AJ3 AK28 AK3	The core power (VDDI) pins should be connected to a well-decoupled +1.8 V digital power supply.
VDDI_JAT4 VDDI_JAT3 VDDI_JAT2 VDDI_JAT1	1.8 V Digital Power	C9 E10 C7 AG8	The **JAT digital power** (VDDI_JAT) pins should be connected to a well-decoupled +1.8 V digital power supply.

Pin Name	Pin Type	PIN No.	Function
VDDO[38:0]	I/O power	C23 C19 C12 C8 C5 C4 D30 D29 D25 D17 D6 E28 E7 F27 G26 H28 H4 J26 L26 M28 N26 R26 T26 V26 W28 Y26 AB26 AC28 AD26 AE27 AF28 AG30 AG29 AG25 AG19 AG6 AH12 AH8 AK17	**I/O power (VDDO).** The VDDO pins should be connected to a well-decoupled +3.3 V power supply.

9.11.1 Ground

Pin Name	Pin Type	Pin No.	Function
VSS[143:0]	Ground	A30 A29 A25 A21 A18 A16 A15 A13 A10 A6 A2 A1 B30 B29 B2 B1 C27 D28 D26 D5 D3 D2 D1 E27 E25 E6 F30 F26 F4 F2 F1 G29 G27 G4 G3 H27 H26 H3 H2 H1 J27 J3 K30 K26 K3 K2 K1 L27	The **ground** (VSS) pins should be connected to a low inductance ground plane connected to both the digital and analog power supplies.

Pin Name	Pin Type	Pin No.	Function
		L4 M27 M26 M3 M2 M1 N30 N27 N4 N3 P26 P2 P1 R30 R27 R4 R3 T30 T27 T3 T2 T1 U26 U3 V30 V27 V3 V2 V1 W27 W26 W3 W2 Y27 Y4 Y3 Y2 AA30 AA26 AA3 AA2 AA1 AB27 AB3 AC27 AC26 AC3 AC2 AC1 AD27 AD3 AE30 AE26 AE4 AE2 AE1 AF27 AF25 AF19 AF6 AF4 AF3 AF2 AF1 AG28 AG26 AG5 AG3 AG2 AG1 AH27 AH24 AH23 AH22 AH20 AH19 AH18 AH5 AH4 AJ30 AJ29 AJ27 AJ2 AJ1 AK30 AK29 AK25 AK23 AK19 AK16 AK15 AK13 AK10 AK6 AK2 AK1	

Notes on Pin Descriptions:

1. All S/UNI MULTI-48 inputs and bidirectionals present minimum capacitive loading and operate at CMOS/LVTTL logic levels except the REFCLK155_P / REFCLK155_N, REFCLK77_P / REFCLK77_N RXD_P[4:1] / RXD_N[4:1], TXD_P[4:1] / TXD_N[4:1] pins, which operate at pseudo-ECL (PECL) logic levels and the APSI_P / APSI_N[4:1], APSO_P / APSO_N[4:1] pins, which operate at LVDS logic levels.

2. The S/UNI MULTI-48 digital outputs and bidirectionals that have 8 mA drive capability are: TTOHFP[4:1], TTOHCLK[4:1], RTOHCLK[4:1], RTOHFP[4:1], RTOH[4:1], RALM[4:1], SALM[4:1], and B3E[4:1].

   The S/UNI MULTI-48 digital output that has 12 mA drive capability is: APSOFP.

   The S/UNI MULTI-48 digital outputs and bidirectionals that have 16 mA drive capability are: D[15:0], TDO and INTB.

   The S/UNI MULTI-48 digital outputs and bidirectionals that have 20 mA drive capability are: TCA/PTPA, STPA, RSX, RMOD[1:0], REOP, RERR, RCA/RVAL, RSOC/RSOP, RDAT[31:0], RPRTY, and RCLKO.

3. The S/UNI MULTI-48 digital inputs are 3.3 V tolerant. The SD[4:1] digital inputs are 5 V (TTL) tolerant.
4. Inputs ALE, RSTB, TMS, TDI, and TRSTB have internal pull-up resistors.
5. It is mandatory that every digital ground pin (VSS) be connected to the printed circuit board ground plane to ensure reliable device operation.
6. It is mandatory that every digital power pin (VDD) be connected to the printed circuit board power plane to ensure reliable device operation.
7. All analog power pins can be sensitive to noise. They must be isolated from the digital power. Care must be taken to correctly decouple these pins. Refer to the Operation section for more information.
8. Due to ESD protection structures in the pads, it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions, it is possible to damage these ESD protection devices or trigger latch up. Please adhere to the power supply sequencing recommendations in section 21.3.
9. Follow recommendations in Section 13.2 for analog power supply filtering.
10. Do not exceed 100 mA of current on any pin during the power-up or power-down sequence.
11. Before any input activity occurs, ensure that the device power supplies are within their nominal voltage range.
12. Hold the device in the reset condition until the device power supplies are within their nominal voltage range.

10 Functional Description

10.1 Receive Line Interface

The Receive Line Interface allows the S/UNI MULTI-48 device to directly interface to optical modules (ODLs) or other medium interfaces. This block performs clock and data recovery on the incoming 2488.32 Mbit/s quad 622.08 Mbit/s, or quad 155.52 Mbit/s data streams.

Modes

In STS-48/STM-16 mode, the receive line interface only uses the RX2488 block.

In STS-12/STM-4 mode, the receive line interface uses the LAS4x622 and 4x622 MABC blocks (Quad 622 Rx). It also borrows part of the receiver analog circuitry from RX2488 for line link 1 (RXD_P/N[1]).

In STS-3/STM-1 mode, the receive line interface uses the DCRU155_622 block and a smaller part of LAS4x622 and 4x622 MABC (Quad 622 Rx). It also borrows part of the receiver analog circuitry from RX2488 for line link 1 (RXD_P/N[1]).

Clock Recovery Unit (CRU)

The clock recovery unit (CRU) recovers the clock from the incoming bit serial data stream. It is compliant with SONET and SDH jitter tolerance requirements. The clock recovery unit uses a low frequency reference clock (155.52 MHz for 2488 mode and 77.76 MHz for 622 and 155 modes) to train and monitor its clock recovery PLL. The clock recovery unit provides different status bits that indicate whether it is locked to data, to the reference clock, or has lost minimum signal transition density. The receive line interface also supports a diagnostic line loopback in all modes.

PLL

Upon start-up, the PLL locks to the reference clock, REFCLK155 or REFCLK77. When the recovered clock's frequency is close enough to the reference clock's frequency, the PLL attempts to lock to the data.

In STS-48/STM-16 and STS-12/STM-4 modes, once in data lock, the PLL reverts to the reference clock if no data transitions occur in 128-bit periods or if the recovered clock drifts beyond 1000 ppm of the reference clock. To avoid bit errors due to lack of edges, a transition density of approximately 50% over 1 second is required. This is generally assured when using SONET scrambling.

In STS-3/STM-1 mode, the PLL, once locked on REFCLK77, adapts to the received data rate using regular phase offsets.

The loop filter transfer function is optimized to enable the PLL to track the jitter and tolerate the minimum transition density expected in a received SONET data signal. The total loop dynamics of the clock recovery PLL yield a jitter tolerance that exceeds the minimum tolerance specified for SONET equipment by GR-253-CORE.

An unframed PRBS pattern can be optionally monitored on the receive line in STS-48/STM-16 and STS-12/STM-4 modes. STS-12/STM-4 mode also supports fixed pattern monitoring. The PRBS is based on the $X^{23}+X^{18}+1$ polynomial (PRBS^23) and is implemented by a Linear Feedback Shift Register (LFSR).

10.2 SONET STS-48/QUAD STS-12/3 Receive Line Interface (SRLI/SFBA)

Based on the SONET/SDH A1/A2 framing pattern, the SONET/SDH receive line interface blocks (SRLI and SFBA) perform byte and frame alignment on the incoming 2488 Mbit/s, 622 Mbit/s, or 155 Mbit/s data streams.

In STS-48/STM-16 and STS-12/STM-4 modes, the SONET receive line interface uses the SRLI block. In STS-3/STM-1 mode, the interface uses the SFBA block.

While out of frame, the SRLI/SFBA monitors the receive data stream for an occurrence of the A1/A2 framing pattern. The SRLI/SFBA adjusts its byte and frame alignment when three consecutive A1 bytes followed by three consecutive A2 bytes occur in the data stream. The SRLI/SFBA informs the RRMP framer block when the framing pattern has been detected, to reinitialize to the new transport frame alignment. While in frame, the SRLI/SFBA maintains the same byte and frame alignment until the RRMP declares out of frame alignment.

10.3 Receive Regenerator and Multiplexer Processor (RRMP)

The Receive Regenerator and Multiplexer Processor (RRMP) block extracts and processes the transport overhead of the received data stream.

The RRMP frames to the data stream by operating with an upstream pattern detector (SRLI or SFBA) which searches for occurrences of the A1/A2 framing pattern. When the SRLI/SFBA finds an A1/A2 framing pattern, the RRMP monitors for the next occurrence of the framing pattern, 125 µs later. Two framing pattern algorithms are provided to improve performance in the presence of bit errors. In algorithm 1, the RRMP declares frame alignment (removes OOF defect) when the twelve A1 and twelve A2 bytes are seen error-free in the single STS-48/STM-16 or the quad STS-12/STM-4 processing modes or when the three A1 and the three A2 bytes are seen error-free in the quad STS-3/STM-1 processing mode. In algorithm 2, the RRMP declares frame alignment (removes OOF defect) only when the first A1 byte and the first four bits of the last A2 byte are seen error-free. Once in frame, the RRMP monitors the framing pattern and declares OOF when one or more bit errors in the framing pattern are detected for four consecutive frames. Table 2 and Table 3 summarize these algorithms.

Table 2 A1/A2 Bytes Used for Out Of Frame Detection

SONET/SDH	Algorithm 1	Algorithm 2
STS-3/STM-1	All A1 & A2 bytes	First A1 byte Last A2 byte (first four bits only)
STS-12/STM-4	All A1 & A2 bytes	First A1 byte Last A2 byte (first four bits only)

SONET/SDH	Algorithm 1	Algorithm 2
STS-48/STM-16	STS-12 #1 All A1 bytes STS-12 #4 All A2 bytes	STS-12 #1 First A1 byte STS-12 #4 Last A2 byte (first four bits only)

Table 3 A1/A2 Bytes Used for In Frame Detection

SONET/SDH	Algorithm 1	Algorithm 2
STS-3/STM-1	All A1 & A2 bytes	First A1 byte Last A2 byte (first four bits only)
STS-12/STM-4	All A1 & A2 bytes	First A1 byte Last A2 byte (first four bits only)
STS-48/STM-16	STS-12 #1 All A1 bytes STS-12 #1 All A2 bytes	STS-12 #1 First A1 byte STS-12 #1 Last A2 byte (first four bits only)

The performance of these framing algorithms in the presence of bit errors and random data is robust. When looking for frame alignment, the performance of each algorithm is dominated by the alignment method used in the SRLI/SFBA, which always examines three A1 and three A2 framing bytes. The probability of falsely framing to random data is less than 0.00001% for either algorithm. Once in frame alignment, the RRMP continuously monitors the framing pattern. When the incoming stream contains a 10^{-3} BER, the first algorithm provides a 99.75% probability that the mean time between OOF occurrences is 1.3 seconds and the second algorithm provides a 99.75% probability that the mean time between OOF occurrences is 7 minutes.

The RRMP also detects loss of frame (LOF) defect and loss of signal (LOS) defect. LOF is declared when an OOF condition exists for a total period of 3 ms during which there is no continuous in frame period of 3 ms. LOF output is removed when an in frame condition exists for a continuous period of 3 ms. LOS is declared when a continuous period of 20 µs without transitions is detected on the receive data stream. LOS is removed when two consecutive framing patterns are found (based on algorithm 1 or algorithm 2) and there are no continuous periods of 20 µs without transitions on the received data stream during the intervening time (one frame).

The RRMP calculates the section BIP-8 error detection code on the scrambled data of the complete frame. The section BIP-8 code is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 code is compared with the BIP-8 code extracted from the B1 byte of STS-1 (STM-0) #1 of the following frame after de-scrambling. Any difference indicates a section BIP-8 error. The RRMP accumulates section BIP-8 errors in a microprocessor readable 16-bit saturating counter (up to 1 second accumulation time). Optionally, block section BIP-8 errors can be accumulated.

The RRMP optionally de-scrambles the received data stream.

The RRMP calculates the line BIP-8 error detection codes on the de-scrambled line overhead and synchronous payload envelope (SPE) bytes of the constituent STS-1 (STM-0). The line BIP-8 code is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 codes are compared with the BIP-8 codes extracted from the B2 byte of the constituent STS-1 (STM-0) of the following frame after de-scrambling. Any difference indicates a line BIP-8 error. The master RRMP accumulates line BIP-8 errors in a microprocessor readable 24-bit saturating counter (up to 1 second accumulation time). Optionally, block BIP-24 errors can be accumulated.

The RRMP extracts line remote error indication (REI-L) errors from the M1 byte of STS-1 (STM-0) #3 and accumulates them in a microprocessor readable 24-bit saturating counter (up to 1 second accumulation time). Optionally, block line REI errors can be accumulated.

The RRMP extracts and filters the K1/K2 APS bytes for three frames. The filtered K1/K2 APS bytes are accessible through microprocessor readable registers. The RRMP also monitors the unfiltered K1/K2 APS bytes to detect APS byte failure (APSBF-L) defect, line alarm indication signal (AIS-L) defect, and line remote defect indication (RDI-L) defect. APS byte failure is declared when 12 consecutive frames have been received where no three consecutive frames contain identical K1 bytes. The APS byte failure is removed upon detection of three consecutive frames containing identical K1 bytes. The detection of invalid APS codes must be done in software by polling the K1/K2 APS register. Line AIS is declared when the bit pattern 111 is observed in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. Line AIS is removed when any pattern other than 111 is observed for three or five consecutive frames. Line RDI is declared when the bit pattern 110 is observed in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. Line RDI is removed when any pattern other than 110 is observed for three or five consecutive frames.

The RRMP extracts and filters the synchronization status message (SSM) for eight frames. The filtered SSM is accessible through microprocessor readable registers.

The RRMP optionally inserts line alarm indication signal (AIS-L).

The RRMP extracts and serially outputs all of the transport overhead (Used and Unused TOH) bytes on the RTOH port. The TOH bytes are output in the same order that they are received (A1, A2, J0/Z0, Unused, B1, E1, Unused, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, S1/Z1, Z2/M1/Z2, and E2).Figure 15, Figure 16, and Figure 17 show the transport overhead bytes on RTOH1-4 for the case where the S/UNI MULTI-48 device is processing quad STS-12/STM-4 or STS-3/STM-1 streams as well as a STS-48/STM-16 stream.

Figure 15 STS-3/STM-1 on RTOH 1-4

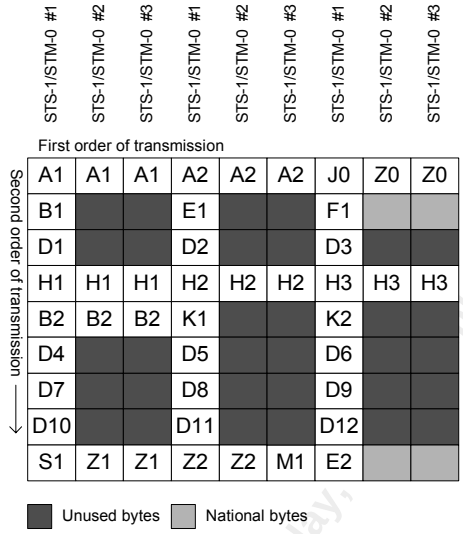


Figure 16 STS-12/STM-4 on RTOH 1-4 or STS-48/STM-16 on RTOH1

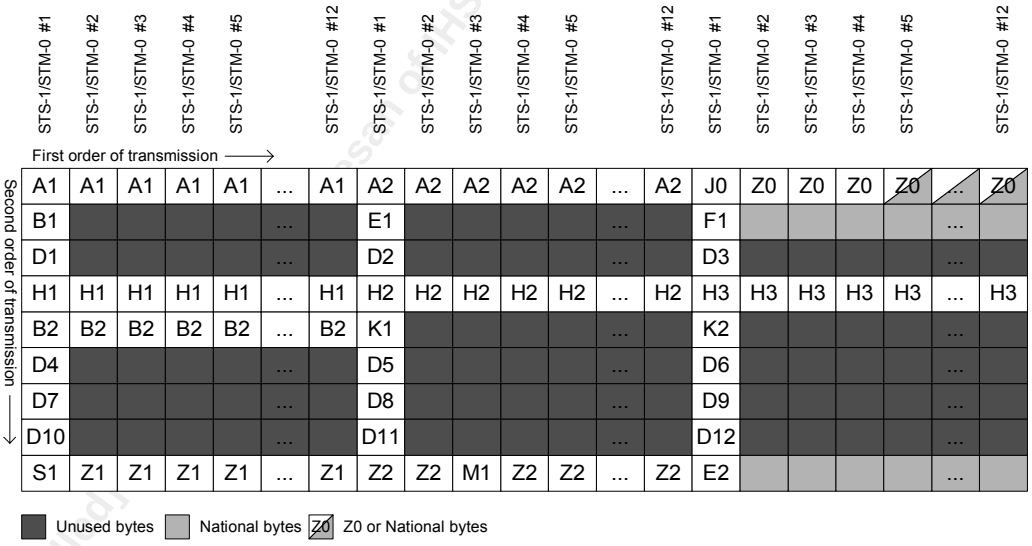
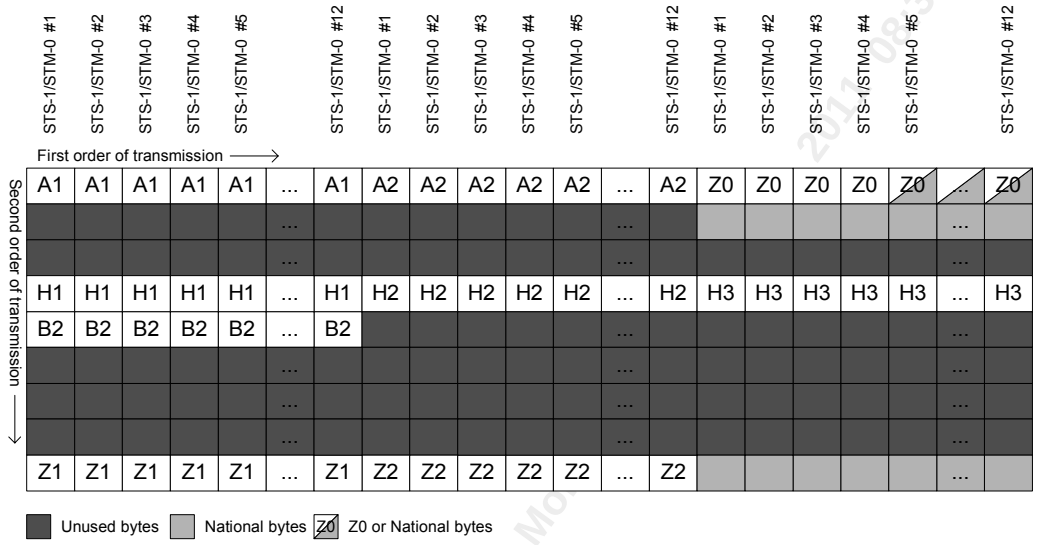


Figure 17 STS-48 (STM-16) on RTOH2-4

RTOH2 extracts the STS-1/STM-0 #13 to #24 transport overhead bytes
RTOH3 extracts the STS-1/STM-0 #25 to #36 transport overhead bytes
RTOH4 extracts the STS-1/STM-0 #37 to #48 transport overhead bytes



A maskable interrupt is activated to indicate any change in the status of OOF, LOF, LOS, line remote defect indication (RDI-L), line alarm indication signal (AIS-L), synchronization status message (COSSM), APS bytes (COAPS), and APS byte failure (APSBF) or any errors in section BIP-8, line BIP-8, and line remote error indication (REI-L).

The RRMP block provides de-scrambled data and frame alignment indication signals for use by the Receive High Order Path Processor (RHPP).

10.4 Receive High Order Path Processor (RHPP)

The Receive High Order Path Processor (RHPP) provides pointer interpretation, extraction of path overhead, extraction of the SPE (virtual container), and path level alarm and performance monitoring.

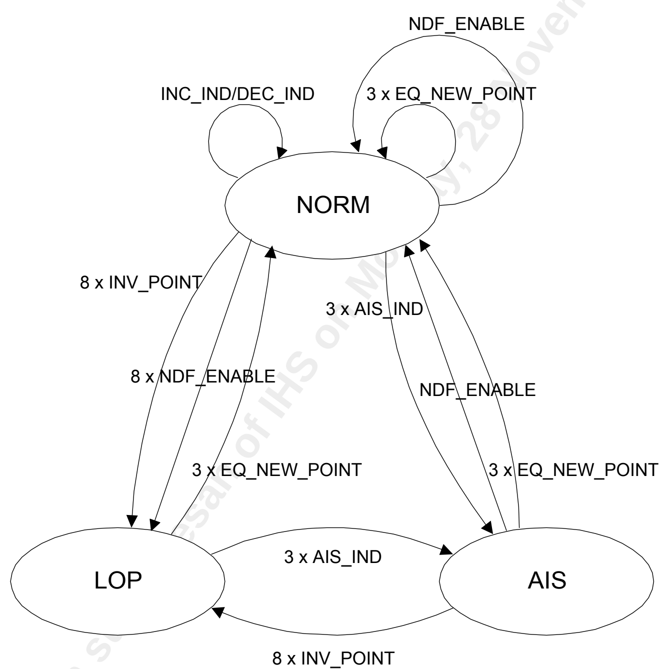
10.4.1 Pointer Interpreter

The pointer interpreter extracts and validates the H1 and H2 bytes to identify the location of the path overhead byte (J1) and all the SPEs of the constituent STS-3c/12c/48c (VC-4/4-4c/4-16c) payloads. The pointer interpreter is a time multiplexed finite state machine that can process STS-3c/12c/48c (AU-4/4-4c/4-16c) pointers. Within the pointer interpretation algorithm, three states are defined:

- NORM_state (NORM)
- AIS_state (AIS)
- LOP_state (LOP)

The transition between states will be consecutive events (indications). For example, it takes three consecutive AIS indications to go from the NORM_state to the AIS_state. The kind and number of consecutive indications activating a transition is chosen such that the behavior is stable and insensitive to low BER. The only transition on a single event is the one from the AIS_state to the NORM_state after receiving an NDF enabled with a valid pointer value. **Note**: since the algorithm only contains transitions based on consecutive indications, it is implied that, for example, non-consecutively received invalid indications do not activate the transitions to the LOP_state.

Figure 18   Pointer Interpretation State Diagram



The following events (indications) are defined:

NORM_POINT: Disabled NDF + ss + offset value equal to active offset.

NDF_ENABLE: Enabled NDF + ss + offset value in range of 0 to 782.

AIS_IND: H1 = FFh + H2 = FFh.

INC_IND: Disabled NDF + ss + majority of I bits inverted + no majority of D bits inverted + previous NDF_ENABLE, INC_IND or DEC_IND more than three frames ago.

DEC_IND: Disabled NDF + ss + majority of D bits inverted + no majority of I bits inverted + previous NDF_ENABLE, INC_IND or DEC_IND more than three frames ago.

INV_POINT: Not any of the above (i.e.: not NORM_POINT, not NDF_ENABLE, not AIS_IND, not INC_IND and not DEC_IND).

NEW_POINT: Disabled NDF + ss + offset value in range of 0 to 782 but not equal to active offset.

Notes

Active offset is defined as the accepted current phase of the SPE (VC) in the NORM_state and is undefined in the other states.

1. Enabled NDF is defined as the following bit patterns: 1001, 0001, 1101, 1011, and 1000.
2. Disabled NDF is defined as the following bit patterns: 0110, 1110, 0010, 0100, and 0111.
3. The remaining six NDF bit patterns (0000, 0011, 0101, 1010, 1100, 1111) result in an INV_POINT indication.
4. ss bits are unspecified in SONET and have bit pattern 10 in SDH.
5. The use of ss bits in definition of indications may be optionally disabled.
6. The requirement for previous NDF_ENABLE, INC_IND or DEC_IND be more than 3 frames ago may be optionally disabled.
7. NEW_POINT is also an INV_POINT.
8. The requirement for the pointer to be within the range of 0 to 782 in 8 X NDF_ENABLE may be optionally disabled.
9. LOP is not declared if all the following conditions exist:
   - the received pointer is out of range (>782),
   - the received pointer is static,
   - the received pointer can be interpreted, according to majority voting on the I and D bits, as a positive or negative justification indication, after making the requested justification, the received pointer continues to be interpretable as a pointer justification.
   - When the received pointer returns to an in-range value, the S/UNI MULTI-48 will interpret it correctly.

The transitions indicated in the state diagram are defined as follows:

INC_IND/DEC_IND: Offset adjustment (increment or decrement indication)

3 x EQ_NEW_POINT: Three consecutive equal NEW_POINT indications

NDF_ENABLE: Single NDF_ENABLE indication

3 x AIS_IND: Three consecutive AIS indications

8 x INV_POINT: Eight consecutive INV_POINT indications

8 x NDF_ENABLE: Eight consecutive NDF_ENABLE indications

Notes

The transitions from NORM_state to NORM_state do not represent state changes but imply offset changes.

1. 3 x EQ_NEW_POINT takes precedence over other events and may optionally reset the INV_POINT count.
2. All three offset values received in 3 x EQ_NEW_POINT must be identical.
3. "Consecutive event counters" are reset to zero on a change of state (except the INV_POINT counter).

LOP is declared on entry to the LOP_state after eight consecutive invalid pointers or eight consecutive NDF enabled indications. Path AIS is optionally inserted in the Drop bus when LOP is declared. The alarm condition is optionally returned to the source node by signaling the corresponding THPP in the local S/UNI MULTI-48 device to insert a path RDI indication. Alternatively, if in-band error reporting is enabled, the path RDI bit in the APS port G1 byte is set to indicate the LOP alarm to the THPP in a remote S/UNI MULTI-48.

PAIS is declared on entry to the AIS_state after three consecutive AIS indications. The alarm condition is optionally returned to the source node by signaling the corresponding THPP in the local S/UNI MULTI-48 device to insert a path RDI indication. Alternatively, if in-band error reporting is enabled, the path RDI bit in APS port G1 byte is set to indicate the PAIS alarm to the THPP in a remote S/UNI MULTI-48.

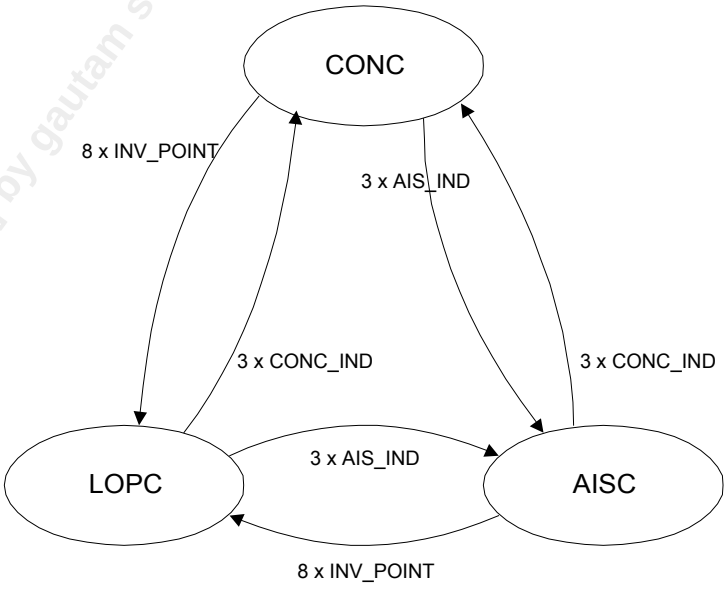
10.4.2 Concatenation Pointer Interpreter State Machine

The concatenation pointer interpreter extracts and validates the H1 and H2 concatenation bytes. The concatenation pointer interpreter is a time multiplexed finite state machine that can process an STS-3c/12c/48c (AU-4/4-4c/4-16c) pointers. Within the pointer interpretation algorithm three states are defined:

- CONC_state (CONC)
- AISC_state (AISC)
- LOPC_state (LOPC)

The transitions between the states are consecutive events (indications). For example, it takes three consecutive AIS indications to go from the CONC_state to the AISC_state. The kind and number of consecutive indications activating a transition is chosen such that the behavior is stable and insensitive to low BER.

Figure 19 Concatenation Pointer Interpretation State Diagram



The following events (indications) are defined:

CONC_IND: Enabled NDF + dd + "1111111111"

AIS_IND: H1 = FFh + H2 = FFh

INV_POINT: Not any of the above (i.e.: not CONC_IND and not AIS_IND)

Notes

Enabled NDF is defined as the following bit patterns: 1001, 0001, 1101, 1011, and 1000.

1. The remaining eleven NDF bit patterns (0000, 0010, 0011, 0100, 0101, 0110, 0111, 1010, 1100, 1110, 1111) result in an INV_POINT indication.
2. dd bits are unspecified in SONET/SDH.

The transitions indicated in the state diagram are defined as follows:

3 X CONC_IND: Three consecutive CONC indications

3 x AIS_IND: Three consecutive AIS indications

8 x INV_POINT: Eight consecutive INV_POINT indications

Note:

1. "Consecutive event counters" are reset to zero on a change of state.

LOPC is declared on entry to the LOPC_state after eight consecutive pointers with values other than concatenation indications. The alarm condition is optionally returned to the source node by signaling the corresponding THPP in the local S/UNI MULTI-48 device to insert a path RDI indication. Alternatively, if in-band error reporting is enabled, the path RDI bit in APS port G1 byte is set to indicate the LOP alarm to the THPP in a remote S/UNI MULTI-48 device.

PAISC is declared on entry to the AISC_state after three consecutive AIS indications. The alarm condition is optionally returned to the source node by signaling the corresponding THPP in the local S/UNI MULTI-48 device to insert a path RDI indication. Alternatively, if in-band error reporting is enabled, the path RDI bit in APS port G1 byte is set to indicate the PAIS alarm to the THPP in a remote S/UNI MULTI-48 device.

10.4.3 Error Monitoring

The RHPP calculates the path BIP-8 error detection codes on the STS-3c/12c/48c (VC-4/4-4c/4-16c) payloads. The path BIP-8 code is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 codes are compared with the BIP-8 codes extracted from the B3 byte of each constituent STS (VC) payload of the following frame. Any differences indicate a path BIP-8 error. The RHPP accumulates path BIP-8 errors in a microprocessor readable 16-bit saturating counter (up to 1 second accumulation time). Optionally, block BIP-8 errors can also be accumulated.

The RHPP extracts the path remote error indication (REI-P) errors from bits 1, 2, 3, and 4 of the path status byte (G1) and accumulates them in a microprocessor readable 16-bit saturating counter (up to 1 second accumulation time). Optionally, block REI errors can be also accumulated.

The RHPP monitors the path signal label byte (C2) payload to validate change in the accepted path signal label (APSL). The same PSL byte must be received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register) before it's considered accepted.

The RHPP also monitors the path signal label byte (C2) to detect path payload label unstable (PLU-P) defect. A PSL unstable counter is incremented every time the received PSL differs from the previously received PSL (an erroneous PSL will cause the counter to be incremented twice; once when the erroneous PSL is received and once when the error free PSL is received). The PSL unstable counter is reset when the same PSL value is received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). PLU-P is declared when the PSL unstable counter reaches five. PLU-P is removed when the PSL unstable counter is reset.

The RHPP also monitors the path signal label byte (C2) to detect path payload label mismatch (PLM-P) defect. PLM-P is declared when the accepted PSL does not match the expected PSL according to Table 4. PLM-P is removed when the accepted PSL match the expected PSL according to Table 4. The accepted PSL is the same PSL value received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). The expected PSL is a programmable PSL value.

The RHPP also monitors the path signal label byte (C2) to detect path unequipped (UNEQ-P) defect. UNEQ-P is declared when the accepted PSL is 00H and the expected PSL is not 00H. UNEQ-P is removed when the accepted PSL is not 00H or when the accepted PSL is 00H and the expected PSL is 00H. The accepted PSL is the same PSL value received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). The expected PSL is a register programmable PSL value.

The RHPP also monitors the path signal label byte (C2) to detect path payload defect indication (PDI-P) defect. PDI-P is declared when the accepted PSL is a PDI defect that matches the expected PDI defect. PPDI is removed when the accepted PSL is not a PDI defect or when the accepted PSL is a PDI defect that does not match the expected PDI defect. The accepted PSL is the same PSL value received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). Table 5 gives the expected PDI defect based on the programmable PDI and PDI range register values.

Table 4 PLM-P, UNEQ-P and PDI-P Defects Declaration

Expected PSL		Accepted PSL			PLM-P	UNEQ-P	PDI-P
00	Unequipped	00	Unequipped		Match	Inactive	Inactive
		01	Equipped non specific		Mismatch	Inactive	Inactive
		02-E0 FD-FF	Equipped specific		Mismatch	Inactive	Inactive
		E1-FC	PDI	=expPDI	Mismatch	Inactive	Active
				!=expPDI	Mismatch	Inactive	Inactive
01	Equipped non specific	00	Unequipped		Mismatch	Active	Inactive
		01	Equipped non specific		Match	Inactive	Inactive
		02-E0 FD-FF	Equipped specific		Match	Inactive	Inactive
		E1-FC	PDI	=expPDI	Match	Inactive	Active
				!=expPDI	Mismatch	Inactive	Inactive
02-FF	Equipped specific PDI	00	Unequipped		Mismatch	Active	Inactive
		01	Equipped non specific		Match	Inactive	Inactive
		02-E0 FD-FF	Equipped specific	= expPSL	Match	Inactive	Inactive
				!=expPSL	Mismatch	Inactive	Inactive
		E1-FC	PDI	=expPDI	Match	Inactive	Active
				!=expPDI	Mismatch	Inactive	Inactive

Table 5 Expected PDI Defects Based on PDI and PDI Range Values

PDI register value	DPI range register value	Exp PDI	PDI register value	DPI range register value	Exp PDI
00000	Disable	None	01111	Disable	EF
	Enable			Enable	E1-EF
00001	Disable	E1	10000	Disable	F0
	Enable	E1-E1		Enable	E1-F0
00010	Disable	E2	10001	Disable	F1
	Enable	E1-E2		Enable	E1-F1
00011	Disable	E3	10010	Disable	F2
	Enable	E1-E3		Enable	E1-F2
00100	Disable	E4	10011	Disable	F3
	Enable	E1-E4		Enable	E1-F3
00101	Disable	E5	10100	Disable	F4
	Enable	E1-E5		Enable	E1-F4
00110	Disable	E6	10101	Disable	F5
	Enable	E1-E6		Enable	E1-F5
00111	Disable	E7	10110	Disable	F6
	Enable	E1-E7		Enable	E1-F6
01000	Disable	E8	10111	Disable	F7
	Enable	E1-E8		Enable	E1-F7
01001	Disable	E9	11000	Disable	F8

PDI register value	DPI range register value	Exp PDI	PDI register value	DPI range register value	Exp PDI
	Enable	E1-E9		Enable	E1-F8
01010	Disable	EA	11001	Disable	F9
	Enable	E1-EA		Enable	E1-F9
01011	Disable	EB	11010	Disable	FA
	Enable	E1-EB		Enable	E1-FA
01100	Disable	EC	11011	Disable	FB
	Enable	E1-EC		Enable	E1-FB
01101	Disable	ED	11100	Disable	FC
	Enable	E1-ED		Enable	E1-FC
01110	Disable	EE			
	Enable	E1-EE			

The RHPP monitors bits 5, 6, and 7 of the path status byte (G1) to detect path remote defect indication (RDI-P) and path enhanced remote defect indication (ERDI-P) defects.

RDI-P is declared when bit 5 of the G1 byte is set high for five or ten consecutive frames (selectable by the PRDI10 bit in the configuration register). RDI-P is removed when bit 5 of the G1 byte is set low for five or ten consecutive frames. ERDI-P is declared when the same 010, 100, 101, 110, or 111 pattern is detected in bits 5, 6, and 7 of the G1 byte for five or ten consecutive frames (selectable by the PRDI10 bit in the configuration register). ERDI-P is removed when the same 000, 001, or 011 pattern is detected in bits 5, 6, and 7 of the G1 byte for five or ten consecutive frames.

10.5 Receive Section and Path Trace Processor (RTTP)

The Receive Trail Trace Processor (RTTP) block monitors the trail trace messages of the receive data stream for trace identifier unstable (TIU) defect and trace identifier mismatch (TIM) defect. Three trail trace algorithms are defined. It is mandatory to select one of the algorithms for the RTTP to monitor the received message.

Algorithm #1

The first algorithm is Telcordia-compliant. This algorithm detects trace identifier mismatch (TIM) defect on a 16 or 64-byte trail trace message. A TIM defect is declared when none of the last 20 messages matches the expected message. A TIM defect is removed when 16 of the last 20 messages match the expected message. The expected trail trace message is a static message written in the expected page of the RTTP by an external microprocessor. Optionally, the expected message is matched when the trail trace message is all zeros.

Algorithm #2

The second algorithm is ITU compliant. This algorithm detects trace identifier unstable (TIU) defect and trace identifier mismatch (TIM) defect on a 16 or 64-byte trail trace message. The current trail trace message is stored in the captured page of the RTTP. If the length of the message is 16 bytes, the RTTP synchronizes on the MSB of the message. The byte with the MSB set high is placed in the first location of the captured page. If the length of the message is 64 bytes, the RTTP synchronizes on the CR/LF (CR = 0Dh, LF = 0Ah) characters of the message. The following byte is placed in the first location of the captured page.

A persistent trail trace message is declared when an identical message is received for three or five consecutive multi-frames (16 or 64 frames). A persistent message becomes the accepted message. The accepted message is stored in the accepted page of the RTTP. A trace identifier unstable (TIU) defect is declared when one or more erroneous bytes are detected in a total of eight messages without any persistent message in between.

A TIU defect is removed when a persistent message is received. A TIM defect is declared when the accepted message does not match the expected message. A TIM defect is removed when the accepted message matches the expected message. The expected message is a static message written in the expected page of the RTTP by an external microprocessor. Optionally, the algorithm declares a match trail trace message when the accepted message is all zeros.

Algorithm #3

The third algorithm is not Telcordia or ITU-compliant. The algorithm detects trace identifier unstable (TIU) on a single continuous trail trace byte. A TIU defect is declared when one or more erroneous bytes are detected in three consecutive 16-byte windows. The first window starts on the first erroneous byte. A TIU defect is removed when an identical byte is received for 48 consecutive frames. A maskable interrupt is activated to indicate any change in the status of trace identifier unstable (TIU) and trace identifier mismatch (TIM).

10.6 SONET Bit Error Rate Monitor (SBER)

The SONET Bit Error Rate (SBER) Monitor provides two independent bit error rate monitoring circuits (BERM block), used to monitor line bit error rate indicator (B2). One BERM block is dedicated to monitor the Signal Degrade (SD) alarm and the other BERM block dedicated to monitor the Signal Fail (SF) alarm. These alarms can be used to control system level features such as Automatic Protection Switching (APS).

The BERM block uses a sliding window-based algorithm. This algorithm provides a significantly better performance for detection, clearing, and false detection than a simple jumping-window (resetable counter being polled at a regular interval) algorithm.

10.7 SONET Alarm Report Controller (SARC)

The SONET Alarm Report Controller (SARC) receives all of the section, line, path, and payload defects detected by the receive overhead processors and the ATM cell processors. It then generates consequent action indications according to user specific configuration. Possible action indications include:

- Receive section alarm (RSALM) indication: RSALM is asserted when an OOF, LOF, LOS, AIS-L, RDI-L, APSBF, TIU-S, TIM-S, SDBER, or SFBER defect is detected in the receive data stream. Configuration registers allow the user to remove any defect from the previous enumeration.
- Receive line AIS insertion (RLAISINS) indication: RLAISINS is asserted when a OOF, LOF, LOS, AIS-L, RDI-L, APSBF, TIU-S, TIM-S, SDBER, or SFBER defect is detected in the receive data stream. Configuration registers allow the user to enable/disable any defect from the previous enumeration.
- Transmit line RDI insertion (TLRDIINS) indication: TLRDIINS is asserted when a OOF, LOF, LOS, AIS-L, RDI-L, APSBF, TIU-S, TIM-S, SDBER, or SFBER defect is detected in the receive data stream. Configuration registers allow the user to enable/disable any defect from the previous enumeration.
- Receive path alarm (RPALM) indication: RPALM is asserted when a RSALM, AIS-P, LOP-P, PLU-P, PLM-P, UNEQ-P, PDI-P, RDI-P, ERDI-P, TIU-P, or TIM-P defect is detected in the receive data stream. It is also asserted when a Loss of Cell Delineation is detected by the ATM cell processor. Configuration registers allow the user to enable/disable any defect from the previous enumeration.
- Receive path alarm insertion (RPAISINS) indication: RPAISINS is asserted when a RLAISINS, AIS-P, LOP-P, PLU-P, PLM-P, UNEQ-P, PDI-P, RDI-P, ERDI-P, TIU-P, or TIM-P defect is detected in the receive data stream. It is also asserted when a Loss of Cell Delineation is detected by the ATM cell processor. Configuration registers allow the user to enable/disable any defect from the previous enumeration.
- Transmit path ERDI insertion (TPERDIINS[2:0]) indication: TPERDIINS[2:0] is updated when a PLU-P, PLM-P, TIU-P, TIM-P, UNEQ-P, LOP-P, or a AIS-P defect is detected in the receive data stream. It is also asserted when a Loss of Cell Delineation is detected by the ATM cell processor. Configuration registers allow the user to enable/disable any defect from the previous enumeration.

10.8 Receive SONET Virtual Container Aligner (RSVCA)

The Receive SONET/SDH Virtual Container Aligner (RSVCA) block aligns the payload data from an incoming SONET/SDH data stream to a new transport frame reference. The alignment is accomplished by recalculating the STS (AU) payload pointer value based on the offset between the transport overhead of the incoming data stream and that of the outgoing data stream.

Frequency offsets (due, for example, to plesiochronous network boundaries) or the loss of a primary reference timing source and phase differences (due to normal network operation) between the incoming data stream and the outgoing data stream are accommodated by pointer adjustments in the outgoing data stream.

The RSVCA also terminates the transport overhead. All transport overhead bytes are set to "00H" except for the A1, A2, H1, H2, and H3 bytes.

10.8.1 Elastic Store

The Elastic Store performs rate adaptation between the line side interface and the system side interface. The entire incoming payload, including path overhead bytes, is written into a first-in-first-out (FIFO) buffer at the incoming byte rate. Each FIFO word stores a payload data byte as well as one bit tag labeling the J1 byte. Incoming pointer justifications are accommodated by writing into the FIFO during the negative stuff opportunity byte or by not writing during the positive stuff opportunity byte. Data is read out of the FIFO in the Elastic Store block at the outgoing byte rate by the Pointer Generator. Similarly, outgoing pointer justifications are accommodated by reading from the FIFO during the negative stuff opportunity byte or by not reading during the positive stuff opportunity byte.

The FIFO read and write addresses are monitored. Pointer justification requests will be made to the Pointer Generator based on the proximity of the addresses relative to programmable thresholds. The Pointer Generator schedules a pointer increment event if the FIFO depth is below the lower threshold and a pointer decrement event if the depth is above the upper threshold. FIFO underflow and overflow events are detected and path AIS is optionally inserted in the outgoing data stream for three frames to alert downstream elements of data corruption.

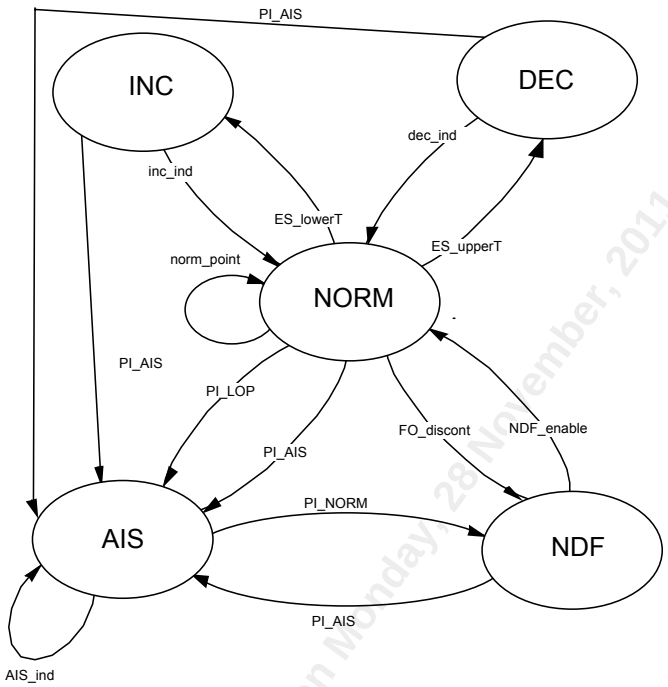
Pointer Generator

The Pointer Generator generates the H1 and H2 bytes to identify the location of the path overhead byte (J1) as well as all of the SPE bytes of the constituent STS-3c/12c/48c (VC-4/4-4c/4-16c) payloads. The pointer generator is a time multiplexed finite state machine that can process STS-3c/12c/48c (AU-4/4-4c/4-16c) pointers. Within the pointer generator algorithm, five states are defined:

- NORM_state (NORM)
- AIS_state (AIS)
- NDF_state (NDF)
- INC_state (INC)
- DEC_state (DEC)

The transition from the NORM to the INC, DEC, and NDF states are initiated by events in the Elastic Store (ES) block. The transition to/from the AIS state are controlled by the pointer interpreter (PI) in the Receive High Order Path Processor block. The transitions from INC, DEC, and NDF states to the NORM state occur autonomously with the generation of special pointer patterns.

Figure 20 Pointer Generation State Diagram



The following events, indicated in the state diagram, are defined:

ES_lowerT: ES filling is below the lower threshold + previous inc_ind, dec_ind or NDF_enable more than three frames ago.

ES_upperT: ES filling is above the upper threshold + previous inc_ind, dec_ind or NDF_enable more than three frames ago.

FO_discont: Frame offset discontinuity

PI_AIS: PI in AIS state

PI_LOP: PI in LOP state

PI_NORM: PI in NORM state

Note

1. A frame offset discontinuity occurs if an incoming NDF enabled is received, or if an ES overflow/underflow occurred.

The autonomous transitions indicated in the state diagram are defined as follows:

inc_ind: Transmit the pointer with NDF disabled and inverted I bits, transmit a stuff byte in the byte after H3, increment active offset.

dec_ind: Transmit the pointer with NDF disabled and inverted D bits, transmit a data byte in the H3 byte, decrement active offset.

NDF_enable: Accept new offset as active offset, transmit the pointer with NDF enabled and new offset.

norm_point: Transmit the pointer with NDF disabled and active offset.

AIS_ind: Active offset is undefined, transmit an all-1's pointer and payload.

Notes

1. Active offset is defined as the phase of the SPE (VC).
2. The ss bits are undefined in SONET, and has bit pattern 10 in SDH
3. Enabled NDF is defined as the bit pattern 1001.
4. Disabled NDF is defined as the bit pattern 0110.

10.9 Transmit Line Interface

The Transmit Line Interface allows the S/UNI MULTI-48 device to directly interface with optical modules (ODLs) or other medium interfaces. This block performs clock synthesis and performs parallel to serial conversion of the outgoing 2488.32 Mbit/s data stream or the quad 622.08 Mbit/s or 155.52 Mbit/s data streams.

In STS-48/STM-16 mode, the transmit line interface only uses the TX2488 block.

In STS-12/STM-4 mode, the transmit line interface uses the LAS4x622, 4x622 MABC (Quad 622 Tx), and JAT622 blocks. It also borrows part of the transmitter analog circuitry from TX2488 for line link 1 (TXD_P/N[1]).

In STS-3/STM-1 mode, the transmit line interface uses the JAT622 block as well as a smaller part of LAS4x622 and 4x622 MABC (Quad 622 Tx). It also borrows part of the transmitter analog circuitry from TX2488 for line link 1 (TXD_P/N[1]).

The transmit clock is synthesized from a 155.52 MHz reference clock in STS-48/STM-16 mode or a 77.76 MHz reference clock in quad STS-12/STM-4 or STS-3/STM-1 modes. For the S/UNI MULTI-48 device to comply with the GR-253-CORE intrinsic jitter specification, jitter on the reference clock must be less than 1 ps RMS in a 12KHz – 20MHz band in STS-48/STM-16 mode, less than 4 ps RMS in a 12KHz – 5MHz band in quad STS-12/STM-4 mode (or mixed STS-12/STM-4 and STS-3/STM-1 mode), or less than 16 ps RMS in a 12KHz – 1.3MHz band in quad STS-3/STM-1 mode.

The REFCLK155 or REFCLK77 reference should be within ±20 ppm to meet the SONET free-run accuracy requirements specified in GR-253-CORE.

The Parallel to Serial Converter (PISO) converts the transmit byte serial stream to a bit serial stream. The transmit bit serial stream appears on the TXD_P/N [1] in STS-48/STM-16 mode or TXD_N/P[4:1] in quad STS-12/STM-4 or STS-3/STM-1 modes.

An unframed PRBS sequence or fixed pattern can optionally be inserted on the transmit line in STS-48/STM-16 and STS-12/STM-4 modes. The PRBS is based on the $X^{23}+X^{18}+1$ polynomial (PRBS^23) and is implemented by a Linear Feedback Shift Register (LFSR).

10.10 SONET STS-48/QUAD STS-12/3 Transmit Line Interface (STLI)

The SONET/SDH transmit line interface block properly formats the outgoing 2488 Mbit/s data stream, the quad 622 Mbit/s, or 155 Mbit/s data streams. This block interfaces the Transmit Regenerator and Multiplexer Section Processor (TRMP) block to the transit line interface.

10.11 Transmit Regenerator and Multiplexer Section Processor (TRMP)

The Transmit Regenerator and Multiplexer Processor (TRMP) block inserts the transport overhead bytes in the transmit data stream.

The TRMP accumulates the line BIP-8 errors detected by the RRMP during the last receive frame. The line BIP-8 errors are returned to the far end as line remote error indication (REI-L) during the next transmitted frame. The minimum value between the maximum REI-L given in Table 6 and the accumulator count is returned as the line REI-L in the M1 byte of STS-1 (STM-0) #3. Optionally, block BIP-24 errors can be accumulated.

The TRMP serially inputs all of the transport overhead (TOH) bytes from the TTOH port. The TOH bytes must be input in the same order that they are transmitted (A1, A2, J0/Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, S1/Z1, Z2/M1/Z2, and E2). Figure 21, Figure 22, and Figure 23 show the transport overhead bytes on TTOH1-4 for the case where the S/UNI MULTI-48 device is processing STS-3/STM-1,STS-12/STM-4, or STS-48/STM-16 streams.

Table 6 Maximum Line REI Errors Per Transmit Frame

SONET/SDH	Maximum single BIP-8 errors LREIBLK=0	Maximum block BIP-24 errors LREIBLK=1
STS-3/STM-1	0001 1000	0000 0001
STS-12/STM-4	0110 0000	0000 0100
STS-48/STM-16	1111 1111	0001 0000

Figure 21 STS-3/STM-1 on TTOH 1-4

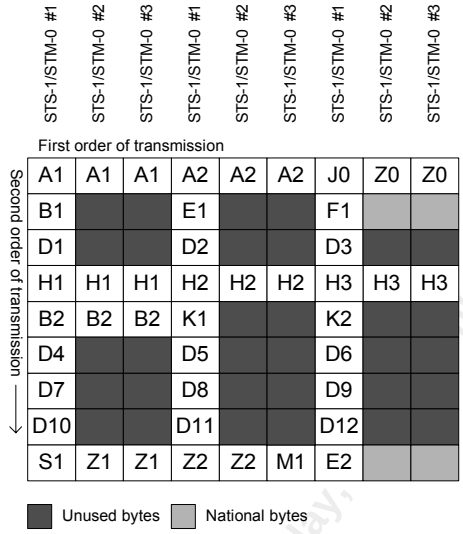


Figure 22 STS-48 (STM-16) on TTOH1 or STS-12/STM-4 on TTOH 1-4

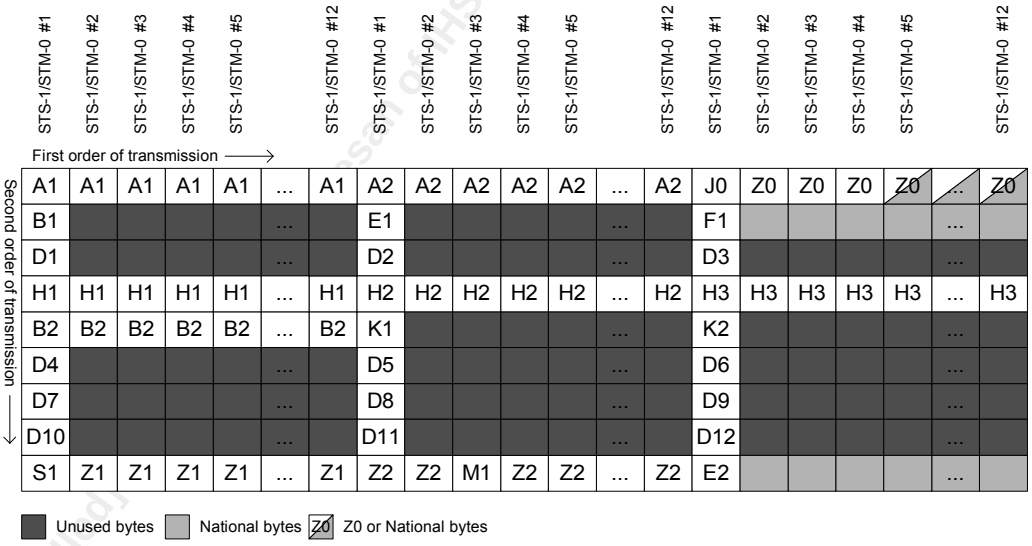
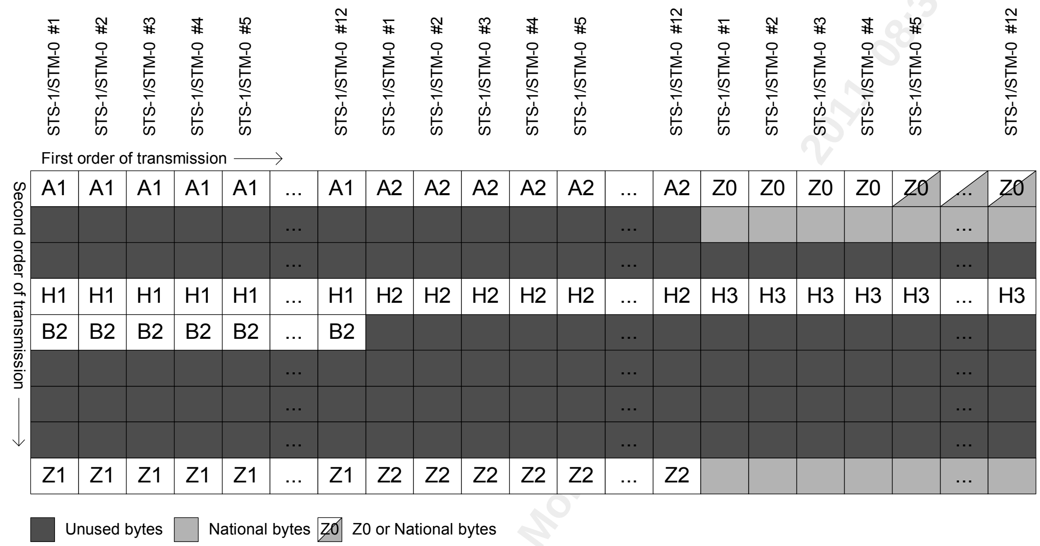


Figure 23 STS-48 (STM-16) on TTOH2-4

TTOH2 inserts the STS-1/STM-0 #13 to #24 transport overhead bytes
TTOH3 inserts the STS-1/STM-0 #25 to #36 transport overhead bytes
TTOH4 inserts the STS-1/STM-0 #37 to #48 transport overhead bytes



The TRMP also inserts most of the transport overhead bytes from internal registers. Since there are multiple sources for the same overhead byte, the TOH bytes must be prioritized according to Table 7 before being inserted into the data stream.

The Z0DEF register bit defines the Z0/NATIONAL growth bytes for row #1. When Z0DEF is set to logic one, the Z0/NATIONAL bytes are defined according to ITU. When Z0DEF is set to logic zero, the Z0/NATIONAL bytes are defined according to Telcordia.

Table 7 TOH Insertion Priority

BYTE	HIGHEST Priority						LOWEST Priority
A1		76h (A1ERR=1)	F6h (A1A2EN=1)	TTOH (TTOHEN=1)			A1 pass through
A2			28h (A1A2EN=1)	TTOH (TTOHEN=1)			A2 pass through
J0	STS-1/STM-0 # (J0Z0INCEN=1)	J0[7:0] (TRACEEN=1)	J0V (J0REGEN=1)	TTOH (TTOHEN=1)			J0 pass through
Z0	STS-1/STM-0 # (J0Z0INCEN=1)		Z0V (Z0REGEN=1)	TTOH (TTOHEN=1)			Z0 pass through
B1				Calculated B1 xor TTOH (TTOHEN=1 & B1MASKEN=1)			Calculated B1 xor B1MASK
				TTOH (TTOHEN=1 & B1MASKEN=0)			
E1			E1V (E1REGEN=1)	TTOH (TTOHEN=1)			E1 pass through
F1			F1V (F1REGEN=1)	TTOH (TTOHEN=1)			F1 pass through
D1-D3			D1D3V (D1D3REGEN=1)	TTOH (TTOHEN=1)			D1-D3 pass through

BYTE	HIGHEST Priority						LOWEST Priority
H1				H1 pass through xor TTOH (TTOHEN=1 & HMASKEN=1) TTOH (TTOHEN=1 & HMASKEN=0)			H1 pass through xor H1MASK
H2				H2 pass through xor TTOH (TTOHEN=1 & HMASKEN=1) TTOH (TTOHEN=1 & HMASKEN=0)			H2 pass through xor H2MASK
H3				TTOH (TTOHEN=1)			H3 pass through
B2				Calculated B2 xor TTOH (TTOHEN=1 & B2MASKEN=1) TTOH (TTOHEN=1 & B2MASKEN=0)			Calculated B2 xor B2MASK
K1		APS[15:8] (APSEN=1)	K1V (K1K2REGEN=1)	TTOH (TTOHEN=1)			K1 pass through
K2		APS[7:0] (APSEN=1)	K2V (K1K2REGEN=1)	TTOH (TTOHEN=1)			K2 pass through
D4-D12			D4D12V (D4D12REGEN=1)	TTOH (TTOHEN=1)			D4-D12 pass through
S1			S1V (S1REGEN=1)	TTOH (TTOHEN=1)			S1 pass through
Z1			Z1V (Z1REGEN=1)	TTOH (TTOHEN=1)			Z1 pass through
Z2			Z2V (Z2REGEN=1)	TTOH (TTOHEN=1)			Z2 pass through
M1			LREI[7:0] (LREIEN=1)	TTOH (TTOHEN=1)			M1 pass through
E2			E2V (E2REGEN=1)	TTOH (TTOHEN=1)			E2 pass through
National			NATIONALV (NATIONALEN=1)	TTOH (TTOHEN=1)			National pass through
Unused			UNUSEDV (UNUSEDEN=1)	TTOH (TTOHEN=1)			Unused pass through
PLD							PLD pass through

Table 8 Definition of Z0/National Growth Bytes for Row #1

TRMP Mode	Type	Z0DEF = 1	Z0DEF = 0
STS-3/STM-1 line mode	Z0	None	From STS-1/STM-0 #2 to #3
	National	From STS-1/STM-0 #2 to #3	None
STS-12/STM-4 line mode or STS-48/STM-16 line mode (master slice)	Z0	From STS-1/STM-0 #2 to #4	From STS-1/STM-0 #2 to #12
	National	From STS-1/STM-0 #5 to #12	None
STS-48/STM-16 line mode (slave slice)	Z0	From STS-1/STM-0 #1 to #4	From STS-1/STM-0 #1 to #12
	National	From STS-1/STM-0 #5 to #12	None

The H1, H2, B1, and B2 bytes input from the TTOH port are inserted or are used as a mask to toggle bits in the corresponding H1, H2, B1, and B2 bytes depending on the HMASK, B1MASK, and B2MASK register bits. When the HMASK, B1MASK, or B2MASK register bit is set low and TTOHEN is sampled high on the MSB of the serial H1, H2, B1, or B2 byte, the serial byte is inserted in place of the corresponding byte. When the HMASK, B1MASK, or B2MASK register bit is set high and TTOHEN is sampled high on the MSB of the serial H1, H2, B1, or B2 byte, the serial byte is XORed with the corresponding path payload pointer (already in the data stream) or the calculated BIP-8 byte before being inserted.

The TRMP inserts the APS bytes detected by the RRMP during the last receive frame. The APS bytes are returned to the far end by the TRMP during the next transmit frame. Because the RRMP and the TRMP are in two different clock domains, two, one, or no APS bytes can be sampled per transmit frame. The last received APS bytes are transmitted.

The TRMP inserts the line remote defect indication (RDI-L) into the data stream. When line RDI is inserted, the 110 pattern is inserted in bits 6, 7, and 8 of the K2 byte of STS-1 (STM-0) #1. Line RDI insertion has priority over TOH byte insertion. The TRMP also inserts the line alarm indication signal (AIS-L) into the data stream. When line AIS must be inserted, all ones are inserted in the line overhead and in the payload (all bytes of the frame except the section overhead bytes). Line AIS insertion has priority over line RDI insertion and TOH byte insertion.

The TRMP calculates the line BIP-8 error detection codes on the transmit data stream. One line BIP-8 error detection code is calculated for each of constituent STS-1 (STM-0). The line BIP-8 byte is calculated on the unscrambled bytes of the STS-1 (STM-0) except for the nine SOH bytes. The line BIP-8 byte is based on a bit interleaved parity calculation using even parity. For each STS-1 (STM-0), the calculated BIP-8 error detection code is inserted in the B2 byte of the following frame before scrambling.

The TRMP optionally scrambles the transmit data stream.

The TRMP calculates the section BIP-8 error detection code on the transmit data stream. The section BIP-8 byte is calculated on the scrambled bytes of the complete frame. The section BIP-8 byte is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 error detection code is inserted in the B1 byte of STS-1 (STM-0) #1 of the following frame before scrambling.

10.12 Transmit Path High Order Processor (THPP)

The Transmit High Order Path Processor (THPP) block inserts the path overhead bytes in the transmit data stream. Path overhead bytes can be sourced from different possible sources. All overhead bytes may optionally be passed-through the THPP block.

The path overhead bytes can be sourced from internal registers. There are eight bits in the THPP Source & Pointer Control Register (TSPCR) that are used to determine the origin of path overhead bytes. They are SRCJ1, SRCC2, SRCG1, SRCF2, SRCH4, SRCZ3, SRCZ4, and SRCZ5.

The THPP calculates the path BIP-8 error detection code on the transmit data stream. The path BIP-8 byte is calculated on all of the payload bytes. The path BIP-8 byte is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 error detection code is optionally inserted in the B3 byte of the following frame. The path trace byte (J1) can be optionally sourced from the Transmit Path Trace Buffer.

The THPP accumulates the path BIP-8 errors detected by the RHPP during the last receive frame. The path BIP-8 errors are optionally returned to the far end as path remote error indication (REI-P: G1 Bytes) during the next transmit frame. The minimum value between the maximum REI-P and the accumulator count is returned as the path REI in the G1 byte. Optionally, block BIP-8 errors can be accumulated. Table 9 shows the source priority for each overhead byte.

Table 9 Path Overhead Byte Source Priority

Byte	Highest Priority					Lowest Priority
J1	UNEQV (UNEQ=1)	J1 pass through (TDIS=1 OR PAIS=1)	Path trace buffer (PTBJ1=1)	J1 ind. reg. (SRCJ1=1)		J1 pass through
B3	UNEQV (UNEQ=1)	B3 pass through (TDIS=1 OR PAIS=1)			Calculated B3	Calculated B3 XOR B3MASK
C2	UNEQV (UNEQ=1)	C2 pass through (TDIS=1 OR PAIS=1)	C2 ind. reg. (SRCC2=1)			C2 pass through
G1	UNEQV (UNEQ=1)	G1 pass through (TDIS=1 OR PAIS=1 OR IBER=1)	PRDI[2:0] and PREI[3:0] (ENG1REC=1)	G1 ind. reg. (SRCG1=1)		G1 pass through
F2	UNEQV (UNEQ=1)	F2 pass through (TDIS=1 OR PAIS=1)	F2 ind. reg. (SRCF2=1)			F2 pass through
H4	UNEQV (UNEQ=1)	H4 pass through (TDIS=1 OR PAIS=1)	H4 pass through XOR H4 ind. reg. (SRCH4=1 AND ENH4MASK=1)	H4 ind. reg. (SRCH4=1)	H4 pass through	H4 pass through
Z3	UNEQV (UNEQ=1)	Z3 pass through (TDIS=1	Z3 ind. reg. (SRCZ3=1)			Z3 pass through

Byte	Highest Priority					Lowest Priority
		OR PAIS=1)				
Z4	UNEQV (UNEQ=1)	Z4 pass through (TDIS=1 OR PAIS=1)	Z4 ind. reg. (SRCZ4=1)			Z4 pass through
Z5	UNEQV (UNEQ=1)	Z5 pass through (TDIS=1 OR PAIS=1)	Z5 ind. reg. (SRCZ5=1)			Z5 pass through

10.13 Transmit Section and Path Trace Processor (TTTP)

The Transmit Trail Trace Processor (TTTP) block generates the trail trace messages to be transmitted. The TTTP block can generate a 16 or 64-byte trail trace message. The message is sourced from an internal RAM and must have been previously written by an external microprocessor. Optionally, the trail trace message can be reduced to a single continuous trail trace byte.

The user must include synchronization in the programmed trail trace message because the TTTP does not add synchronization. The synchronization mechanism is different for a 16-byte message and for a 64-byte message. For a 16-byte message, the synchronization is based on the MSB of the trail trace byte. MSB is only set high for one of the 16 bytes. The byte with its MSB set high is considered the first byte of the message. For a 64-byte message, the synchronization is based on the CR/LF (CR = 0Dh, LF = 0Ah) characters of trail trace message. The byte following the CR/LF bytes is considered the first byte of the message.

To avoid generating an unstable/mismatch message, the TTTP block forces the message to all zeros while the microprocessor updates the internal RAM.

10.14 Transmit SONET Virtual Container Aligner (TSVCA)

See the Receive SONET Virtual Container Aligner (RSVCA) in Section 10.8.

10.15 APS Serial TelecomBus (LVDS)

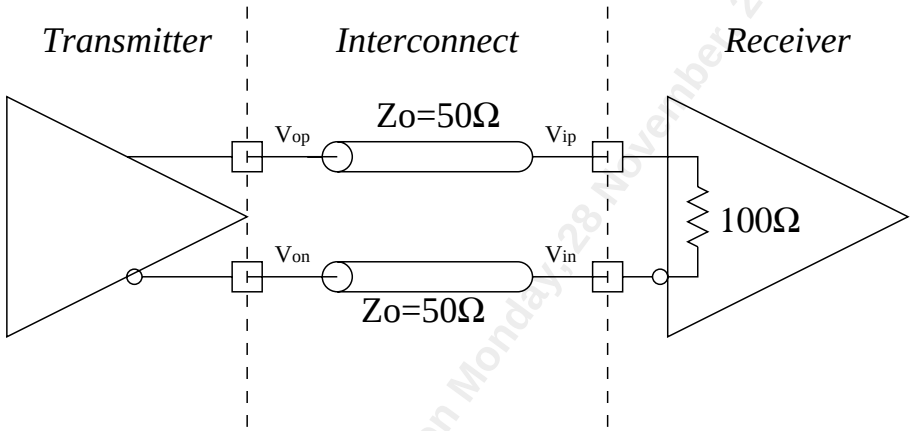
10.15.1 LVDS Overview

The LVDS system is comprised of the LVDS Receiver (RXLV), Data Recovery Unit (DRU), Receive 8B/10B TelecomBus Decoder (R8TD), Transmit 8B/10B TelecomBus Encoder (T8TE), APS Parallel to Serial converter (APISO), LVDS Transmitter (TXLV) and Transmitter LVDS Reference (TXLVREF), and Clock Synthesis Unit (CSU) blocks.

The LVDS APS Port implements the 777.6 Mbit/s LVDS links. Four 777.6 Mbit/s LVDS links form a high-speed serial TelecomBus interface for passing four STS-12/STM-4 aggregate data streams.

Figure 24 illustrates a generic LVDS link compliant with IEEE 1596.3-1996. In this diagram, the transmitter drives a differential signal through a pair of 50Ω characteristic interconnects, such as board traces, backplane traces, or short lengths of cable. The receiver presents a 100Ω differential termination impedance to terminate the lines. Sufficient common-mode range is included in the standard for the receiver to accommodate as much as 925 mV of common-mode ground difference.

Figure 24 Generic LVDS Link Block Diagram



Complete SERDES transceiver functionality is provided. Ten-bit parallel data is sampled by the line rate divided-by-10 clock (77.76 MHz SYSCLK or internally generated 77.76 MHz clock derived from REFCLKx when SYSCLK is not used) and then serialized at the line rate on the LVDS output pins by a 777.6 MHz clock synthesized from a divided version of SYSCLK or REFCLKx. Serial line rate LVDS data is sampled and de-serialized to 10-bit parallel data. Parallel output transfers are synchronized to a gated line rate divided-by-10 clock. The 10-bit data is passed to an 8B/10B decoding block. The gating duty cycle is adjusted such that the throughput of the parallel interface equals the receive input data rate (Line Rate +/- 100ppm). The transmitter's clock source is expected to be the same as the receiver's clock source, to ensure the data throughput at both ends of the link are identical.

Data must contain sufficient transition density to allow reliable operation of the data recovery units. 8B/10B block coding and decoding is provided by the T8TE and R8TD blocks.

At the system level, reliable operation will be obtained if proper signal integrity is maintained through the signal path and the receiver requirements are respected. That is, a worst case eye opening of 0.7 UI and 100 mV differential amplitude is needed. These conditions should be achievable with a system architecture consisting of board traces, two sets of backplane connectors, and up to 1 m of backplane interconnects. This assumes proper design of 100Ω differential lines and minimization of discontinuities in the signal path. Due to power constraints, the output differential amplitude is approximately 350 mV.

10.15.2LVDS Receiver (RXLV)

The LVDS Receiver (RXLV) analog block is a 777.6 Mbit/s Low Voltage Differential Signaling (LVDS) Receiver that is compliant with the IEEE 1596.3-1996 LVDS Specification.

The RXLV analog receiver accepts up to 777.6 Mbit/s LVDS signals from the transmitter, amplifies them, converts them to digital signals, and then passes them to a data recovery unit (DRU). As per the IEEE 1596.3-1996 specification, the RXLV has a differential input sensitivity better than 100 mV and includes at least 25 mV of hysteresis.

10.15.3 APS Data Recovery Unit (APSDRU)

The ASP Data Recovery Unit (APSDRU) is a fully integrated data recovery and serial to parallel converter, used for 777.6 Mbit/s NRZ data. An 8B/10B block code is used to guarantee transition density for optimal performance. The APSDRU recovers data and outputs a 10-bit word synchronized with a line rate divided by 10 gated clock to allow frequency deviations between the data source and the local oscillator. The APSDRU accumulates ten data bits and then outputs them on the next clock edge.

The APSDRU provides moderate high frequency jitter tolerance suitable for inter-chip serial link applications. It can support frequency deviations up to ±100ppm.

10.15.4 APS Parallel to Serial Converter (APISO)

The APS Parallel to Serial Converter (APISO) is a parallel-to-serial converter designed for high-speed transmit operation, supporting up to 777.6 Mbit/s.

10.15.5 LVDS Transmitter (TXLV)

The LVDS Transmitter (TXLV) is a 777.6 Mbit/s Low Voltage Differential Signaling (LVDS) Transmitter compliant with the IEEE 1596.3-1996 LVDS Specification. The TXLV accepts 777.6 Mbit/s differential data from the APSIO circuit and transmits the data off-chip as a low voltage differential signal. The TXLV uses the reference current and voltage from the TXLVREF to control the output differential voltage amplitude and the output common-mode voltage.

10.16 Receive 8B/10B TelecomBus Decoder (R8TD)

The Receiver 8B/10B TelecomBus Decoder (R8TD) works in conjunction with the upstream APSDRU (which packs consecutive bits from an incoming 8B/10B serial link into a 10-bit wide stream with arbitrary alignment to the 8B/10B character boundaries).

The Receive 8B/10B TelecomBus Decoder (R8TD) block frames to the receive stream to find 8B/10B character boundaries. It also contains a FIFO to bridge between the timing domain of the receive LVDS links and the system clock timing domain. Four R8TD blocks are instantiated in the S/UNI MULTI-48 device.

The FIFO buffer sub-block provides isolation between the timing domain of the associated 4 LVDS links and the system clock (internal SYSCLK). Data with arbitrary alignment to 8B/10B characters are written into a 10-bit by 24-word deep FIFO at the link clock rate. Data is read from the FIFO at every internal SYSCLK cycle.

The Receiver 8B/10B TelecomBus Decoder (R8TD) contains three sub-blocks: 1) character alignment; 2) frame alignment; and 3) character decode.

10.16.1 Character Alignment

The character alignment sub-block locates character boundaries in the incoming 8B/10B data stream. The framer logic may be in one of two states, SYNC state or HUNT state. The character alignment block uses the 8B/10B control character (K28.5), used to encode the SONET/SDH J0 byte, to locate character boundaries and enter the SYNC state. This sub-block also monitors the receive data stream for line code violations (LCV). An LCV is declared when the running disparity of the receive data is not consistent with the previous character or the data is not one of the characters defined in the IEEE standard 802.3. Excessive LCVs are used to transition the framer logic to the HUNT state.

Normal operation occurs when the character alignment sub-block is in the SYNC state. 8B/10B characters are extracted from the FIFO using the character alignment of the K28.5 character that caused entry to the SYNC state. Mimic K28.5 characters at other alignments are ignored. The receive data is constantly monitored for line code violations. If five or more LCVs are detected in a window of 15 characters, the character alignment sub-block transitions to the HUNT state. It will search all possible alignments in the receive data for the K28.5 character. In the meantime, the original character alignment is maintained until a K28.5 character is found. At that point, the character alignment is moved to this new location and the sub-block transitions to the SYNC state.

10.16.2 Frame Alignment

The frame alignment sub-block monitors the data read from the FIFO buffer sub-block for the J0 byte. When the frame counter sub-block indicates the J0 byte position, a J0 character is expected to be read from the FIFO. If a J0 byte is read out of the FIFO at other byte positions, a J0 byte error counter is incremented. When the counter reaches three, the frame alignment sub-block transitions to HUNT state. The next time a J0 character is read from the FIFO, the associated read address is latched and the sub-block transitions back to the SYNC state. The J0 byte error counter is cleared when a J0 byte is read from the FIFO at the expected position.

10.16.3 Character Decode

The character decode sub-block decodes the incoming 8B/10B control characters into an extended set of TelecomBus control signals. Table 10 shows the mapping of TelecomBus control bytes and signals into 8B/10B control characters. The table is divided into two sections: 1) Multiplex Section Termination (MST) mode; and 2) High-order Path Termination (HPT) mode. The character decoder sub-block itself is not mode-sensitive. For the S/UNI MULTI-48 device to work properly, the character decoder must be set to operate in the HPT mode.

Table 10 Serial TelecomBus 8B/10B Character Decoding

Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Decoded Signals Description
Multiplex Section Termination (MST) Mode			
K28.5	001111 1010	110000 0101	OJ0='b1' Transport frame alignment OD[7:0] = 'h01

Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Decoded Signals Description
K.28.4-	001111 0010	—	OPAIS='b1' High-order path AIS OD[7:0] = 'hFF
High-Order Path Termination (HPT) Mode			
K28.0-	001111 0100	—	OPL = 'b0, High-order path H3 byte, no negative justification event OD[7:0] = 'h00
K28.0+	—	110000 1011	OPL = 'b0 High-order path PSO byte, positive justification event OD[7:0] = 'h00
K28.6	001111 0110	110000 1001	OJ1='b1' High-order path frame alignment OD[7:0] = 'h00

10.17 Transmit 8B/10B TelecomBus Encoder (T8TE)

The APS transmit 8B/10B Encoder block (T8TE) constructs an 8B/10B character stream from an incoming TelecomBus carrying an STS-12/STM-4 stream. Four T8TE blocks are instantiated in the S/UNI MULTI-48 device.

The T8TE encodes a TelecomBus data stream and encodes it into an extended 8B/10B format for transmission on the serial LVDS links. The T8TE encodes TelecomBus control signals such as transport frame and payload boundaries, pointer justification events, and alarm conditions into three levels of an extended set of 8B/10B characters. It also performs the IEEE mode conversion on data. To identify more TelecomBus bytes and events than the twelve control characters available in the standard set, those control characters with balanced line codes for both positive and negative running disparity (K28.0, K28.4, K28.5, K28.6, K28.7, K23.7, K27.7, K29.7, and K30.7) are treated specially. The positive and negative disparity codes are each associated with a different SONET/SDH byte or event.

10.17.1 Character Encode

The T8TE operates in one of two modes: multiplex section termination (MST) or high-order path termination (HPT) mode. In MST mode, the upstream block is a multiplex section terminator with identified transport frame boundaries. The first J0 byte (J0) on each STS-12 data link is encoded by an 8B/10B control character. In HPT mode, the upstream block is a high-order path terminator that performs pointer processing to identify STS/AU level pointer justification events. It processes all of the STS/VC path overhead bytes. In the absence of negative pointer justification events, the H3 bytes may be encoded. Similarly, in the presence of positive pointer justification events, the PSO byte may be encoded. Alternately, the J1 byte may be encoded.

Table 11 shows the mapping of TelecomBus control bytes and signals into 8B/10B control characters. The table is divided into two sections, one for each software configurable mode of operation.

Table 11 Serial TelecomBus 8B/10B Character Mapping

Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Encoded Signals Description
Multiplex Section Termination (MST) Mode			
K28.5	001111 1010	110000 0101	IJ0 = ’b1 IPL = ‘b0 Transport frame alignment
K.28.4-	001111 0010	-	IPAIS = ’b1 High-order path AIS
High-Order Path Termination (HPT) Mode			
K28.0-	001111 0100	-	IPL = ‘b0 High-order path H3 byte position, no negative justification event
K28.0+	-	110000 1011	IPL = ‘b0 High-order path PSO byte position, positive justification event
K28.6	001111 0110	110000 1001	IJ1 = ’b1 IPL = ‘b1 High-order path frame alignment

10.18 Space Slot Interchange (X-BAR)

The SONET/SDH Space Slot Interchange (X-BAR) block grooms the SONET/SDH data stream to and from APS port by performing STS-12 (STM-4) space switching. Any STS-12 (STM-4) stream can be switched to any STS-12/STM-4 space slot.

10.19 SONET In-band Error Report Processor (SIRP)

The SONET In-band Error Report Processor (SIRP) block is used for error reporting from a remote APS protect mate when operating as the working mate under a failure condition. In the failure condition, the remote protect mate performs section, line, and path termination and passes the expected P-REI and P-RDI indications back to the working mate in-band in the G1 byte via its output APS port. The SIRP block processes remote alarm indications in the SONET/SDH data stream from the Input APS port. The SIRP in the companion working mate can be configured to extract remote defect indications (RDI) and remote error indications (REI) from an STS-3/STM-1, an STS-12/STM-4, or an STS-48/STM-16 incoming data stream. Accumulated remote error indications and remote defect indications are reported to the THPP block. Both RDI and extended RDI modes are available. The RDI report is configurable to be asserted for at least 10 frames or 20 frames.

10.20 Pseudo-Random Bit Sequence Generator and Monitor (PRGM)

The SONET/SDH Pseudo-Random bit sequence Generator and Monitor (PRGM) block generates and monitors an unframed 2^{23}-1 payload test sequence on the TelecomBus ADD or DROP bus.

The PRGM can generate PRBS in an STS-3c/12c/48c (VC-4/4-4c/4-16c) payload. The path overhead column, the fixed stuff columns #2 to #4 in an STS-12c (VC-4-4c) payload and the fixed stuff columns #2 to16 in an STS-48c (VC-4-16c) payload do not contain any PRBS data. The PRGM generator preserves payload framing and overwrites the payload bytes with PRBS data.

When processing a concatenated STS-48c (VC-4-16c) payload, the master PRGM co-ordinates the distributed PRBS generation between itself and the slave PRGMs. Each PRGM generates one quarter of the complete X23+X18+1 PRBS sequence. To ensure that the slave PRGMs are synchronized with the master PRGM, a signature is continuously broadcast by the master PRGM to allow the slave PRGMs to check their relative states. A signature mismatch is flagged as an out-of-synch state by the slave PRGM. A re-synchronization of the PRBS generation must be initiated by the master PRGM (under software control).

The PRBS monitor of the PRGM block monitors the recovered payload data for the presence of an unframed 2^{23}-1 test sequence and accumulates pattern errors detected based on this pseudo-random pattern. The PRGM declares synchronization when a sequence of 32 correct pseudo-random patterns (bytes) are detected consecutively. Pattern errors are only counted when the PRGM is in synchronization with the input sequence. When 16 consecutive pattern errors are detected, the PRGM will fall out of synchronization and will continuously attempt to re-synchronize to the input sequence until it is successful.

When processing an STS-48c (VC-4-16c) payload, the master PRGM and the slave PRGMs independently monitor one quarter of the complete X23+X18+1 PRBS sequence. To ensure that the slave PRGMs are synchronized with the master PRGM, the same signature matching will be performed as described for the PRBS generation.

A maskable interrupt is activated to indicate any change in the synchronization status.

10.21 SONET Timeslot Interchange (STSI)

The SONET Timeslot Interchange (STSI) cross-connects any transmit UL3/PL3 channel to any transmit line payload. It also cross-connects any receive line payload to any receive UL3/PL3 channel.

10.22 Receive Channel Assigner (RCAS12)

The Receive Channel Assigner (RCAS12) groups STS-1/STM-0 system timeslots into channels. Channel numbers are associated with the UTOPIA/POS interface RADR[3:0] values.

The RCAS12 works on an STS-12/STM-4 data stream. It allows the STS-12/STM-4 data stream to be split into up to four STS-3c/VC-4 or one STS-12c/STM-4 channel.

An RCAS12 block can assign data streams to one of four possible channel numbers. STS-12c/VC-4-4c or 1 x STS-3c/VC-4 channels should be assigned to chanel 0, ending up as channels 0, 4, 8, and 12 or 0, 1, 2, and 3 on the UL3/PL3 interface, depending on the CHAN4SEL register bit (register 0004H). 4 x STS-3c/VC-4 channels should be assigned to channels 0 to 3 within each RCAS12 instance, ending up as channels 0 to 15 on the UL3/PL3 interface.

An STS-48c stream will occupy all timeslots and will be transmitted across four RCAS12 blocks. An STS-48c data stream must be assigned to channel 0.

10.23 Receive Time-sliced Datacom Processor (RTDP)

The Receive Time-sliced Datacom Processor (RTDP) performs both ATM cells and packets processing. It can process four STS-3c/VC-4 channels inside an STS-12/STM-4 master (STS-12) or slave (part of an STS-48) stream, or one STS-3c/VC-4 channel inside an STS-3/STM-1 stream.

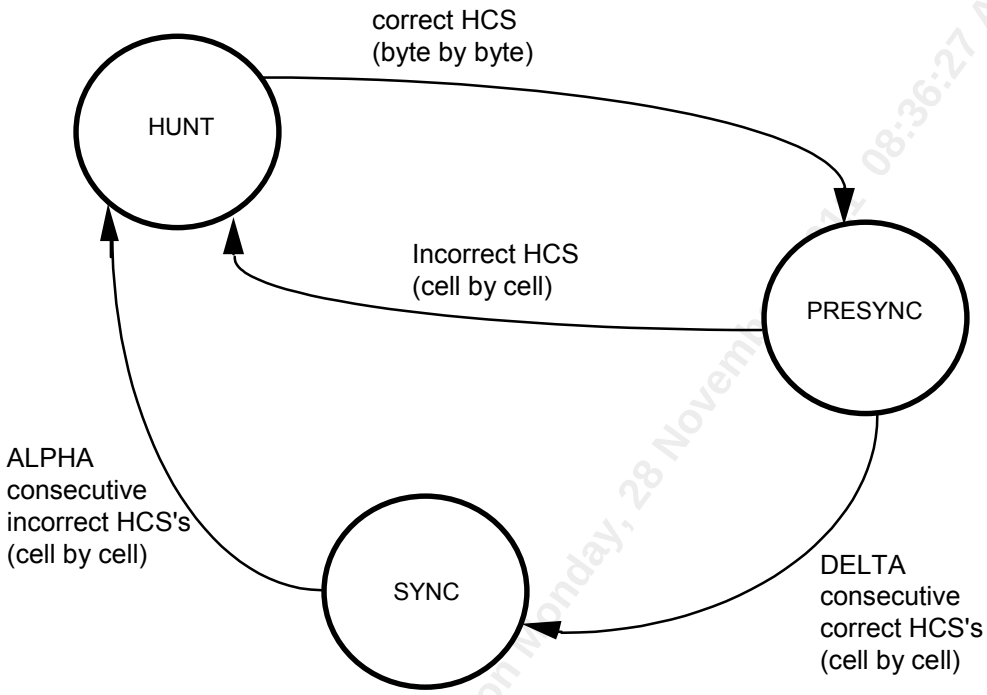
10.23.1 RTDP ATM Processor

In ATM mode, the RTDP performs ATM cell delineation, provides cell filtering based on idle/unassigned cell detection and HCS error detection, and performs ATM cell payload descrambling

Cell Delineation

Cell Delineation is the process of framing to ATM cell boundaries using the header check sequence (HCS) field found in the cell header. The HCS is a CRC-8 calculation over the first four octets of the ATM cell header. When performing delineation, correct HCS calculations are assumed to indicate cell boundaries. Cells are assumed to be byte-aligned to the synchronous payload envelope. The cell delineation algorithm searches the 53 possible cell boundary candidates individually to determine the valid cell boundary location. While searching for the cell boundary location, the cell delineation circuit is in the HUNT state. When a correct HCS is found, the cell delineation state machine locks on the particular cell boundary, corresponding to the correct HCS, and enters the PRESYNC state. The PRESYNC state validates the cell boundary location. If the cell boundary is invalid, an incorrect HCS will be received within the next DELTA cells, at which time a transition back to the HUNT state is executed. If no HCS errors are detected in this PRESYNC period, the SYNC state is entered. While in the SYNC state, synchronization is maintained until ALPHA consecutive incorrect HCS patterns are detected. In such an event, a transition is made back to the HUNT state. The state diagram of the delineation process is shown in Figure 25.

Figure 25 Cell Delineation State Diagram



The values of ALPHA and DELTA determine the robustness of the delineation process. ALPHA determines the robustness against false misalignments due to bit errors. DELTA determines the robustness against false delineation in the synchronization process. ALPHA is chosen to be 7 and DELTA is chosen to be 6. These values result in an average time to delineation of 2 µs for the STS-48c/VC-4-16c rate, 8 µs for the STS-12c/VC-4-4c rate, and 31 µs for the STS-3c/VC-4 rate. Note that although seven consecutive HCS errors will cause the cell processor to lose cell alignment, the last erroneous HCS will not be counted.

Descrambler

The self-synchronous descrambler operates on the 48 byte cell payload only. The circuitry descrambles the information field using the $x^{43} + 1$ polynomial. The descrambler is disabled for the duration of the header and HCS fields and may optionally be disabled for the payload.

Cell Filter and HCS Verification

Cells are filtered (or dropped) based on HCS errors and/or a cell header pattern. Cell filtering is optional and is enabled through the RTDP registers. Cells are passed to the receive FIFO while the cell delineation state machine is in the SYNC state as described above. When both filtering and HCS checking are enabled, cells are dropped if HCS errors are detected or if the header contents match the pattern contained in the RTDP Idle Cell Header and Mask register. Idle cell filtering is accomplished by writing the appropriate cell header pattern into the RTDP Idle Cell Header and Mask Pattern and register. Idle/Unassigned cells are assumed to contain the all zeros pattern in the VCI and VPI fields. The RTDP Idle Cell Header and Mask register allow filtering control over the contents of the GFC, PTI, and CLP fields of the header.

The HCS is a CRC-8 calculation over the first four octets of the ATM cell header. The RTDP block verifies the received HCS using the polynomial, $x^8 + x^2 + x + 1$. The coset polynomial, $x^6 + x^4 + x^2 + 1$, is added (modulo 2) to the received HCS octet before comparison with the calculated result.

Performance Monitor

The Performance Monitor consists of two 16-bit saturating HCS error event counters, a 32-bit saturating receive cell counter, and a 32-bit saturating Idle cell counter. The first error counter accumulates HCS errors. A 32-bit receive cell counter counts all cells written into the receive FIFO. Filtered Idle cells are counted in another 32-bit counter.

Each counter may be read through the microprocessor interface. If required, circuitry is provided to latch these counters so that their values can be read while simultaneously resetting the internal counters to 0 or 1. This will result in a new period of accumulation without loss of any events. It is intended that the counter be polled at least once per second to avoid missing any counted events.

10.23.2 RTDP Packet Processor

The RTDP Packet Processor performs PPP and HDLC packet extraction, provides FCS error detection, performs packet payload descrambling, and provides performance monitoring functions.

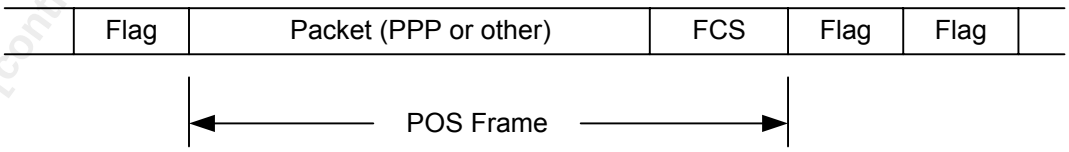
Descrambler

When enabled, the self-synchronous descrambler operates on the PPP Frame data, descrambling the data with the polynomial $x^{43} + 1$. Descrambling is performed on the raw HDLC/PPP data stream before any PPP frame delineation or byte destuffing is performed. Data scrambling provides a more robust system, preventing the injection of hostile patterns into the data stream.

PPP/HDLC Frame Delineation

The PPP/HDLC Frame Delineation is performed on the descrambled data and consists of arranging the framed octets. Frame boundaries are found by searching for the Flag Character (0x7E). Flags are also used to fill inter-packet spacing. This block removes the Flag and Idle Sequences and passes the data onto the Bit or Byte Destuffing block. The PPP/HDLC Frame format is shown on Figure 26.

Figure 26 PPP/HDLC Over SONET Frame Format



In the event of a FIFO overflow caused by the FIFO being full while a packet is being received, the packet is marked with an error so it can be discarded by the system. Subsequent bytes associated with this now aborted frame are discarded. Reception of PPP/HDLC data resumes when a Start of Packet is encountered and the FIFO level is below a programmable Reception Initialization Level.

Byte Destuffing

The byte destuffing algorithm searches the Control Escape character (0x7D). These characters, listed in Table 12, are added for transparency in the transmit direction and must be removed to recover the user data. When the Control Escape character is encountered, it is removed and the following data byte is XORed with 0x20. Therefore, any escaped data byte will be processed properly by the S/UNI MULTI-48 device.

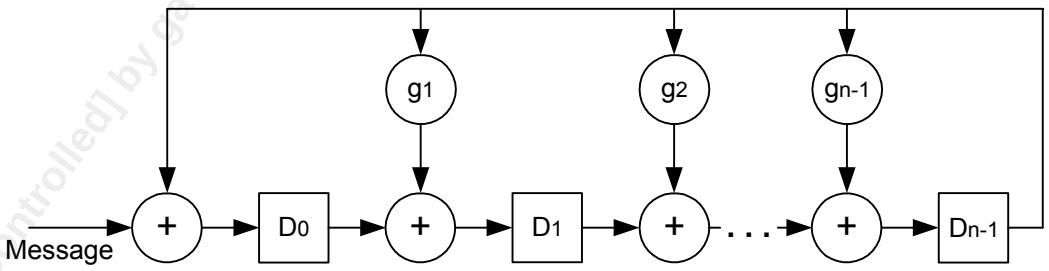
Table 12 Byte Destuffing

Original	Escaped
7E (Flag Sequence)	7D-5E
7D (Control Escape)	7D-5D
Aborted Packet	7D-7E

FCS Check

The FCS Generator performs a CRC-CCITT or CRC-32 calculation on the whole POS frame, after byte destuffing and data descrambling scrambling. A parallel implementation of the CRC polynomial is used. The CRC algorithm for the frame checking sequence (FCS) field is either a CRC-CCITT or CRC-32 function. The CRC-CCITT is two bytes in size and has a generating polynomial $g(X) = 1 + X^5 + X^{12} + X^{16}$. The CRC-32 is four bytes in size and has a generating polynomial $g(X) = 1 + X + X^2 + X^4 + X^5 + X^7 + X^8 + X^{10} + X^{11} + X^{12} + X^{16} + X^{22} + X^{23} + X^{26} + X^{32}$. The first FCS bit transmitted is the coefficient of the highest term. Packets with FCS errors are marked as such and should be discarded by the system.

Figure 27 CRC Decoder



Performance Monitor

The Performance Monitor consists of four 16-bit saturating error event counters, one 32-bit saturating received good packet counter, and one 32-bit counter for accumulating packet bytes. One of the error event counters accumulates FCS errors. The second error event counter accumulates minimum length violation packets. The third error event counter accumulates maximum length violation packets. The fourth error event counter accumulates aborted packets. The 32-bit receive good packet counter counts all error free packets.

Each counter may be read through the microprocessor interface. Circuitry is provided to latch these counters so that their values can be read while simultaneously resetting the internal counters to 0 or 1, whichever is appropriate, so that a new period of accumulation can begin without loss of any events. The counters should be polled at least once per second so error events will not be missed.

The RTDP monitors the packets for both minimum and maximum length errors. When a packet size is smaller than MINPL[7:0], the packet is marked with an error but still written into the FIFO. Malformed packets are packets that do not at least contain four bytes. They are discarded and the MINPLI interrupt will be counted as a minimum packet size violation asserted, but the malformed packet will not be counted. When the packet size exceeds MAXPL[16:0], the packet is marked with an error and the bytes beyond the maximum count are discarded.

10.24 Receive Cell and Frame Processor (RCFP)

The Receive Cell and Frame Processor (RCFP) performs both ATM and PPP processing. It can process a single STS-12c/VC-4-4c channel or a single STS-48c/VC-4-16c channel.

RCFP ATM Cell Processor

In ATM mode, the RCFP performs ATM cell delineation, provides cell filtering based on idle/unassigned cell detection and HCS error detection, and performs ATM cell payload descrambling. Details on each of these functions can be found in the RTDP description (See Section 10.23).

RCFP POS Frame Processor

The RCFP POS Frame Processor performs PPP packet extraction, provides FCS error detection, performs packet payload descrambling, and provides performance monitoring functions. Details on each of these functions can be found in the RTDP description in Section 10.23.

The RCFP handles malformed packets (smaller than four bytes) differently than the RTDP. In the RCFP, the minimum packet violation is counted in MINPL, while for the RTDP, they only cause MINPLI to be asserted. Note that the FCS calculation in the RCFP will proceed independently of any errors detected upstream. Thus, under abort, max length violations, etc, one might also get FCS violations.

10.25 Receive ATM and Packet FIFO (RXSDQ)

The Receive ATM and Packet FIFO (RXSDQ) block provides FIFOs for each channel to separate the receive line-side timing from the higher layer ATM/Packets system timing. FIFO space can be allocated to different channels in blocks of 16 bytes. The receive FIFO holds a maximum of 768 blocks. For example, if the S/UNI MULTI-48 device is configured to carry one STS-12c and 12 STS-3c POS channels, the FIFO can allocate space for 192 blocks for the STS-12c channel and 48 blocks for each of the 12 STS-3c. This would fully utilize the entire FIFO storage space. The maximum value that can be allocated to any single channel is 192 blocks.

The RXPHY provides either a UTOPIA Level 3 or a POS-PHY Level 3 interface to read data from the FIFO.

ATM Receive FIFO

The Receive FIFO is responsible for holding cells until they are read by Receive System Interface.

Receive FIFO management functions include: filling the receive FIFO, indicating when cells are available to be read from the receive FIFO, maintaining the receive FIFO read and write pointers, and detecting FIFO overrun conditions. Upon detection of an overrun, the FIFO discards the current cell and subsequent cells until there is room in the FIFO. FIFO overruns are indicated through a maskable interrupt and register bit and are considered a system error.

POS Receive FIFO

The Receive FIFO block contains storage capacity of 768 octets per STS-3c channel, 3072 octets per STS-12c or STS48c channel, along with management circuitry for reading and writing the FIFO. The receive FIFO provides for the separation of the physical layer timing from the system timing.

Receive FIFO management functions include filling the receive FIFO, indicating when packets or bytes are available to be read from the receive FIFO, maintaining the receive FIFO read and write pointers, and detecting FIFO overrun and underrun conditions. Upon detection of an overrun, the FIFO aborts the current packet and subsequent bytes until there is room in the FIFO. Once enough room is available, as defined by the BT[7:0] register bit settings, the RXSDQ will wait for the next start of packet before writing any data into the FIFO. FIFO overruns are indicated through a maskable interrupt and register bit, and are considered a system error. A FIFO underrun is caused when the System Interface tries to read more data words while the FIFO is empty. This action will be detected and reported through the FUDRI interrupt, but it is not considered a system error. The system will continue to operate normally. In that situation, RVAL can be used by the Link Layer device to find out if valid or invalid data is provided on the System Interface.

10.26 Receive UL3 and PL3 Interface (RXPHY)

The S/UNI MULTI-48 system interface can be configured for ATM or POS mode. When configured for ATM applications, the system interface provides a 32-bit UTOPIA Level 3 compatible bus to allow the transfer of ATM cells between the ATM layer device and the S/UNI MULTI-48. When configured for POS applications, the system interface provides a 32-bit POS-PHY Level 3 compliant bus for the transfer of ATM cells and data packets between the link layer device and the S/UNI MULTI-48. The link layer device can implement various protocols, including PPP and HDLC.

10.27 Transmit Channel Assigner (TCAS12)

The Transmit Channel Assigner (TCAS12) maps channel numbers from the UTOPIA/POS interface (TADR[3:0] values) into STS-1 timeslots.

The TCAS12 works on an STS-12/STM-4 data stream from an upstream TTDP or TCFP block. It allows the STS-12/STM-4 data stream from the TTDP or TCFP to be split into up to four STS-3c/VC-4 or one STS-12c/STM-4 channel.

A TCAS12 block can assign data streams from one of four possible channels. STS-12c/VC-4-4c or 1 x STS-3c/VC-4 timeslots should be taken from channel 0 (equivalent to channels 0, 4, 8, and 12 or 0, 1, 2, and 3 on the UL3/PL3 interface, depending on the CHAN4SEL register bit (register 0004H)). 4 x STS-3c/VC-4 timeslots can be taken from channels 0 to 3 within each TCAS12 instance (equivalent to channels 0 to 16 on the UL/PL3 interface).

An STS-48c channel will occupy all timeslots and will be transmitted across four TCAS12 blocks. An STS-48c data stream must be taken from channel 0.

10.28 Transmit Time-sliced Datacom Processor (TTDP)

The Transmit Time-sliced Datacom Processor (TTDP) performs both ATM and PPP/HDLC processing. It can process four STS-3c/VC-4 channels inside an STS-12/STM-4 master (STS-12) or slave (part of an STS-48) stream, or 1 STS-3c/VC-4 channel inside an STS-3/STM-1 stream.

10.28.1 TTDP ATM Processor

In ATM mode, the TTDP performs rate adaptation via idle/unassigned cell insertion, provides HCS generation and insertion, and performs ATM cell scrambling.

Idle/Unassigned Cell Generator

The Idle/Unassigned Cell Generator inserts idle or unassigned cells into the cell stream when enabled. Registers are provided to program the GFC, PTI, and CLP fields of the idle cell header and the idle cell payload. The idle cell HCS is automatically calculated and inserted.

Scrambler

The Scrambler scrambles the 48 octet information field. Scrambling is performed using a parallel implementation of the self-synchronous scrambler ($x^{43} + 1$ polynomial) described in the references. The cell headers are transmitted unscrambled, and the scrambler may optionally be disabled.

HCS Generator

The HCS Generator performs a CRC-8 calculation over the first four header octets. A parallel implementation of the polynomial, x^8+x^2+x+1, is used. The coset polynomial, $x^6+x^4+x^2+1$, is added (modulo 2) to the residue. The HCS Generator optionally inserts the result into the fifth octet of the header.

10.28.2 TTDP Packet Processor

The TTDP Packet Processor provides rate adaptation by transmitting flag sequences (0x7E) or Idle sequences (0xFF) between packets, provides FCS generation and insertion, performs byte stuffing and data scrambling, and provides performance monitoring functions.

PPP/HDLC Frame Generator

The PPP/HDLC Frame Generator generates packets whose format is shown in Figure 26. Flags or Idle sequences are inserted whenever the Transmit FIFO (TXSDQ) is empty and there is no data to transmit. When there is enough data to be transmitted, the block operates normally; it removes packets from the Transmit FIFO and transmits them. In addition, FCS generation, error insertion, byte stuffing, and scrambling can be optionally enabled.

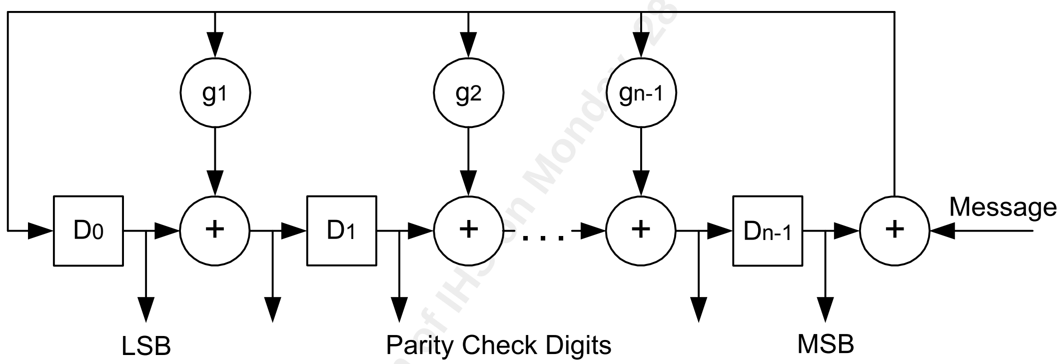
In the event of a FIFO underflow caused by the TXSDQ FIFO being empty while a packet is being transmitted, the packet is aborted by transmitting the Abort Sequence. The PPP Abort Sequence consists of an Escape Control character (0x7D) followed by the Flag Sequence (0x7E). Bytes associated with this aborted frame are still read from the FIFO but are discarded and replaced with the Flag Sequence in the outgoing data stream. Transmission of data resumes when a Start of Packet is encountered in the FIFO data stream.

The POS Frame Generator also performs Inter Packet Gapping. This operation consists of inserting a programmable number of Flag and Idle Sequence characters between each PPP/HDLC Frame transmission. This feature allows one to control the system effective data transmission rate if required.

FCS Generator

The FCS Generator performs a CRC-CCITT or CRC-32 calculation on the whole POS frame, before byte stuffing and data scrambling. A parallel implementation of the CRC polynomial is used. The CRC algorithm for the frame checking sequence (FCS) field is either a CRC-CCITT or CRC-32 function. The CRC-CCITT is two bytes in size and has a generating polynomial $g(X) = 1 + X^{5} + X^{12} + X^{16}$. The CRC-32 is four bytes in size and has a generating polynomial $g(X) = 1 + X + X^{2} + X^{4} + X^{5} + X^{7} + X^{8} + X^{10} + X^{11} + X^{12} + X^{16} + X^{22} + X^{23} + X^{26} + X^{32}$. The first FCS bit transmitted is the coefficient of the highest term. When transmitting a packet from the Transmit FIFO, the FCS Generator appends the result after the last data byte, before the closing flag. Note that the Frame Check Sequence is the one's complement of the CRC register after calculation ends. FCS calculation and insertion can be disabled.

Figure 28 CRC Generator



An error insertion mechanism is provided for system diagnosis purposes. Error insertion is performed by inverting the resulting FCS value, before transmission. This should cause an FCS Error at the far end.

Byte Stuffing

The PPP Frame generator provides transparency by performing byte stuffing. This operation is done after the FCS calculation. Two characters are escaped, the Flag Sequence (0x7E) and the Escape Character itself (0x7D). When a character is escaped, it is XORed with 0x20 before transmission and preceded by the Control Escape (0x7D) character.

Table 13 Byte Stuffing

Original	Escaped
7E (Flag Sequence)	7D-5E
7D (Control Escape)	7D-5D
Abort Sequence	7D-7E

Data Scrambling

The Scrambler will optionally scramble the whole packet data, including the FCS and the flags. Scrambling is performed after the POS frame is formed using a parallel implementation of the self-synchronous scrambler polynomial, $x^{43}+1$. The scrambler may optionally be completely disabled. Data scrambling can provide for a more robust system preventing the injection of hostile patterns into the data stream.

Note: see the Transmit Cell and Frame Processor (TCFP) functionnal description section for differences between TTDP and TCFP.

10.29 Transmit Cell and Frame Processor (TCFP)

The Transmit Cell and Frame Processor (TCFP) performs both ATM and PPP processing. It can process a single STS-12c/VC-4-4c channel or a single STS-48c/VC-4-16c channel.

TCFP ATM Cell Processor

In ATM mode, the TCFP provides rate adaptation via idle/unassigned cell insertion, provides HCS generation and insertion, performs ATM cell scrambling, and provides performance monitoring functions. Details on each of these functions can be found in the TTDP description (See Section 10.28).

TCFP PPP Frame Processor

The TCFP provides rate adaptation by transmitting flag sequences (0x7E) between packets, provides FCS generation and insertion, performs byte stuffing and packet data scrambling, and provides performance monitoring functions. Details on each of these functions can be found in the TTDP description in Section 10.28.

Differences between TTDP and TCFP

The TCFP differs from that of the TTDP in the behavior of counters for an aborted packet due to under-run. The TCFP counters are not aware of the under-run condition, and thus the Abort counter is not incremented for this condition, and all remaining bytes of the aborted packet are counted.

Also, as opposed to the TCFP, the TTDP does not generate the FCS bytes when it receives an aborted packet due to TERR. It will only overwrite the last data byte with the abort byte. TCFP generates the FCS bytes and then overwrites the last FCS byte with the abort byte. Their respective transmit byte counters will thus report a slightly different byte count when packets are aborted (TERR).

10.30 Transmit ATM and Packet FIFO (TXSDQ)

The Transmit ATM and Packet FIFO (TXSDQ) provides FIFOs for each channel to separate the system link layer timing from line-side timing. FIFO space can be allocated to different channels in blocks of 16 bytes. The transmit FIFO holds a maximum of 768 blocks. For instance, if the S/UNI MULTI-48 is configured to carry one STS-12c and 12 STS-3c POS channels, the FIFO can allocate space of 192 blocks for the STS-12c channel and 48 blocks for each of the 12 STS-3c. This would fully utilize the entire FIFO storage space. The maximum value that can be allocated to any single channel is 192 blocks.

The TXPHY provides either a UTOPIA Level 3 or a POS-PHY Level 3 interface to transfer data to the FIFO.

ATM Transmit FIFO

The Transmit FIFO is responsible for holding cells provided through the Transmit System Interface until they are transmitted. The cells are written in with a single 32-bit data bus running off TFCLK and are read out at the channel rate. Internal read and write pointers track the cells and indicate the fill status of the Transmit FIFO. Separate read and write clock domains provide for separation of the physical layer line timing from the System Link layer timing (TFCLK).

POS Transmit FIFO

The Transmit FIFO is responsible for holding packets provided through the Transmit System Interface until they are transmitted. Octets are written in with a single 32-bit data bus running off TFCLK and are read out at the channel rate. Separate read and write clock domains provide for separation of the physical layer line timing from the System Link layer timing.

Internal read and write pointers track the insertion and removal of octets, and indicate the fill status of the Transmit FIFO. These status indications are used to detect underrun and overrun conditions, abort packets as appropriate on both System and Line sides, control flag insertion, and generate the STPA and PTPA outputs.

10.31 Transmit UL3 and PL3 Interface (TXPHY)

The S/UNI MULTI-48 transmit system interface can be configured for ATM or POS mode. When configured for ATM applications, the system interface provides a 32-bit transmit UTOPIA Level 3 compatible bus to allow the transfer of ATM cells between the ATM layer device and the S/UNI MULTI-48. When configured for POS applications, the system interface provides a 32-bit POS-PHY Level 3 compliant bus for the transfer of ATM cells and/or data packets between the link layer device and the S/UNI MULTI-48. The link layer device can implement various protocols, including PPP and HDLC.

10.32 JTAG Test Access Port

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The S/UNI MULTI-48 identification code is 053600CD hexadecimal.

10.33 Microprocessor Interface

The Microprocessor Interface Block provides the logic required to interface the generic microprocessor bus with the normal mode and test mode registers within the S/UNI MULTI-48. The normal mode registers are used during normal operation to configure and monitor the S/UNI MULTI-48. The test mode registers are used to enhance the testability of the S/UNI MULTI-48. The register set is accessed as shown in the Table 14. In the following section, every register is documented and identified using the register numbers in Table 14. The corresponding memory map address is identified by the address column of the table. Addresses that are not shown are not used and must be treated as Reserved.

Table 14 Register Memory Map

A[12] RX/TX	A[11:10]	A[9:0] (HEX)	Register Description
0	00	000H	S/UNI MULTI-48 DEVICE ID Register
0	00	001H	S/UNI MULTI-48 Manufacturer Code and Revision Number
0	00	002H	S/UNI MULTI-48 Global Performance Monitor Update and Clock Activity Monitor
0	00	003H	S/UNI MULTI-48 Master Software Resets Register
0	00	004H	S/UNI MULTI-48 Master Configuration Register #1
0	00	005H	S/UNI MULTI-48 Master Configuration Register #2
0	00	006H	S/UNI MULTI-48 Line Side Receive Configuration
0	00	007H	S/UNI MULTI-48 Line Side Transmit Configuration
0	00	008H	S/UNI MULTI-48 Diagnostic
0	00	009H	S/UNI MULTI-48 Reserved #1
0	00	00AH	S/UNI MULTI-48 APS X-Bar Configuration
0	00	00BH	S/UNI MULTI-48 Master Interrupt Status #1
0	00	00CH	S/UNI MULTI-48 Master Interrupt Status #2
0	00	00DH	S/UNI MULTI-48 Master Interrupt Status #3
0	00	00EH	S/UNI MULTI-48 Master Interrupt Status #4
0	00	00FH	S/UNI MULTI-48 Master Interrupt Status #5
0	00	010H	S/UNI MULTI-48 Master Interrupt Status #6
0	00	011H	S/UNI MULTI-48 Master Interrupt Status #7
0	00	012H	S/UNI MULTI-48 Master Interrupt Status #8
0	00	013H	S/UNI MULTI-48 System Side Receive and Transmit Configuration
0	00	014H	S/UNI MULTI-48 Reserved #2
0	00	015H	S/UNI MULTI-48 APSIFP Enable and APS Input TelecomBus Synchronization Delay
0	00	016H	S/UNI MULTI-48 APS Output TelecomBus Synchronization Delay
0	00	017H	S/UNI MULTI-48 Rx APS J0 FIFO Interrupt Enable
0	00	018H	S/UNI MULTI-48 Rx APS J0 FIFO Interrupt Status
0	00	019H	S/UNI MULTI-48 APS SMART framing configuration
0	00	01AH	S/UNI MULTI-48 Miscellaneous Defect Configuration #1
0	00	01BH	S/UNI MULTI-48 Miscellaneous Defect Configuration #2

A[12] RX/TX	A[11:10]	A[9:0] (HEX)	Register Description
0	00	01CH	S/UNI MULTI-48 Miscellaneous Defect Configuration #3
0	00	01DH	S/UNI MULTI-48 Miscellaneous Defect Configuration #4
0	00	01EH	S/UNI MULTI-48 Free Register
0	00	01FH	Reserved
RECEIVE			
Rx2488 Analog			
0	00	020H	Rx2488 Analog Interrupt Status
0	00	021H	Rx2488 Analog Interrupt Control
0	00	022H	Rx2488 Analog CRU Control
0	00	023H	Rx2488 Analog CRU Clock Training Configuration and Status
0	00	024H	Rx2488 Analog PRBS Control
0	00	025-02FH	Rx2488 Reserved
QUAD 622 RX MABC			
0	00	030H	QUAD 622 RX MABC General Control Register
0	00	031H	QUAD 622 RX MABC Control Register
0	00	032H	QUAD 622 RX MABC Reserved
0	00	033H	QUAD 622 RX MABC Interrupt Enable Register
0	00	034H	QUAD 622 RX MABC Interrupt Status Register
QUAD 622 RX MABC offset = 0035H, 0435H, 0835H and 0C35H			
0	XX	035H	QUAD 622 RX MABC Channel Control Register
0	XX	036H	QUAD 622 RX Channel Data Path Control Register
0	XX	037H	QUAD 622 RX Channel Data Path PRBS Control Register
0	XX	038H	QUAD 622 RX Channel Data Interrupt Status Register
0	XX	039H	QUAD 622 RX Channel Data Path PRBS Status Register
0	XX	03A-03FH	QUAD 622 RX Channel Reserved
SRLI			
0	00	040H	SRLI Clock Configuration
0	00	041-04FH	SRLI Reserved
0	00	050-05FH	Reserved
SBER offset = 0060H, 0460H, 0860H and 0C60H			
0	XX	060H	SBER Configuration
0	XX	061H	SBER Status
0	XX	062H	SBER Interrupt Enable
0	XX	063H	SBER Interrupt Status
0	XX	064H	SBER SF BERM Accumulation Period (LSB)
0	XX	065H	SBER SF BERM Accumulation Period (MSB)
0	XX	066H	SBER SF BERM Saturation Threshold (LSB)
0	XX	067H	SBER SF BERM Saturation Threshold (MSB)
0	XX	068H	SBER SF BERM Declaring Threshold (LSB)
0	XX	069H	SBER SF BERM Declaring Threshold (MSB)
0	XX	06AH	SBER SF BERM Clearing Threshold (LSB)

A[12] RX/TX	A[11:10]	A[9:0] (HEX)	Register Description
0	XX	06BH	SBER SF BERM Clearing Threshold (MSB)
0	XX	06CH	SBER SD BERM Accumulation Period (LSB)
0	XX	06DH	SBER SD BERM Accumulation Period (MSB)
0	XX	06EH	SBER SD BERM Saturation Threshold (LSB)
0	XX	06FH	SBER SD BERM Saturation Threshold (MSB)
0	XX	070H	SBER SD BERM Declaring Threshold (LSB)
0	XX	071H	SBER SD BERM Declaring Threshold (MSB)
0	XX	072H	SBER SD BERM Clearing Threshold (LSB)
0	XX	073H	SBER SD BERM Clearing Threshold (MSB)
0	XX	074-07FH	SBER Reserved
RRMP offset = 0080H, 0480H, 0880H and 0C80H			
0	XX	080H	RRMP Configuration
0	XX	081H	RRMP Status
0	XX	082H	RRMP Interrupt Enable
0	XX	083H	RRMP Interrupt Status
0	XX	084H	RRMP Receive APS
0	XX	085H	RRMP Receive SSM
0	XX	086H	RRMP AIS enable
0	XX	087H	RRMP Section BIP Error Counter
0	XX	088H	RRMP Line BIP Error Counter (LSB)
0	XX	089H	RRMP Line BIP Error Counter (MSB)
0	XX	08AH	RRMP Line REI Error Counter (LSB)
0	XX	08BH	RRMP Line REI Error Counter (MSB)
0	XX	08C-09FH	RRMP Reserved
RTTP SECTION offset = 00A0H, 04A0H, 08A0H and 0CA0H			
0	XX	0A0H	RTTP SECTION Indirect Address
0	XX	0A1H	RTTP SECTION Indirect Data
0	XX	0A2H	RTTP SECTION Trace Unstable Status
0	XX	0A3H	RTTP SECTION Trace Unstable Interrupt Enable
0	XX	0A4H	RTTP SECTION Trace Unstable Interrupt Status
0	XX	0A5H	RTTP SECTION Trace Mismatch Status
0	XX	0A6H	RTTP SECTION Trace Mismatch Interrupt Enable
0	XX	0A7H	RTTP SECTION Trace Mismatch Interrupt Status
0	XX	0A8-0BFH	RTTP SECTION Reserved
RTTP PATH offset = 00C0H, 04C0H, 08C0H and 0CC0H			
0	XX	0C0H	RTTP PATH Indirect Address
0	XX	0C1H	RTTP PATH Indirect Data
0	XX	0C2H	RTTP PATH Trace Unstable Status
0	XX	0C3H	RTTP PATH Trace Unstable Interrupt Enable
0	XX	0C4H	RTTP PATH Trace Unstable Interrupt Status
0	XX	0C5H	RTTP PATH Trace Mismatch Status

A[12] RX/TX	A[11:10]	A[9:0] (HEX)	Register Description
0	XX	0C6H	RTTP PATH Trace Mismatch Interrupt Enable
0	XX	0C7H	RTTP PATH Trace Mismatch Interrupt Status
0	XX	0C8-0DFH	RTTP PATH Reserved
0	XX	0E0-0FFH	Unused
RHPP offset = 0100H, 0500H, 0900H and 0D00H			
0	XX	100H	RHPP Indirect Address
0	XX	101H	RHPP Indirect Data
0	XX	102H	RHPP Reserved
0	XX	103H	RHPP Counters Update
0	XX	104H	RHPP Path Interrupt Status
0	XX	105H	RHPP Pointer Concatenation Processing Disable
0	XX	106H	RHPP Unused
0	XX	107H	RHPP Unused
0	XX	108H	RHPP Pointer Interpreter Status STS-1/STM-0 #1
0	XX	109H	RHPP Pointer Interpreter Interrupt Enable STS-1/STM-0 #1
0	XX	10AH	RHPP Pointer Interpreter Interrupt Status STS-1/STM-0 #1
0	XX	10BH	RHPP Error Monitor Status STS-1/STM-0 #1
0	XX	10CH	RHPP Error Monitor Interrupt Enable STS-1/STM-0 #1
0	XX	10DH	RHPP Error Monitor Interrupt Status STS-1/STM-0 #1
0	XX	10EH	RHPP Reserved STS-1/STM-0 #1
0	XX	10FH	RHPP Reserved STS-1/STM-0 #1
…	…	…	…
0	XX	160H	RHPP Pointer Interpreter Status STS-1/STM-0 #12
0	XX	161H	RHPP Pointer Interpreter Interrupt Enable STS-1/STM-0 #12
0	XX	162H	RHPP Pointer Interpreter Interrupt Status STS-1/STM-0 #12
0	XX	163H	RHPP Error Monitor Status STS-1/STM-0 #12
0	XX	164H	RHPP Error Monitor Interrupt Enable STS-1/STM-0 #12
0	XX	165H	RHPP Error Monitor Interrupt Status STS-1/STM-0 #12
0	XX	166H	RHPP Reserved STS-1/STM-0 #12
0	XX	167H	RHPP Reserved STS-1/STM-0 #12

A[12] RX/TX	A[11:10]	A[9:0] (HEX)	Register Description
0	XX	168-17FH	RHPP Reserved
0	XX	180-1FFH	Unused
RSVCA offset = 0200H, 0600H, 0A00H and 0E00H			
0	XX	200H	RSVCA Indirect Address
0	XX	201H	RSVCA Indirect Data
0	XX	202H	RSVCA Reserved #1
0	XX	203H	RSVCA Positive Justification Interrupt Status
0	XX	204H	RSVCA Negative Justification Interrupt Status
0	XX	205H	RSVCA FIFO Overflow Interrupt Status
0	XX	206H	RSVCA FIFO Underflow Interrupt Status
0	XX	207H	RSVCA Pointer Justification Interrupt Enable
0	XX	208H	RSVCA FIFO Interrupt Enable
0	XX	209H	RSVCA Reserved #2
0	XX	20AH	RSVCA Reserved #3
0	XX	20BH	RSVCA Performance Monitor Trigger
0	XX	20C-21FH	RSVCA Reserved
0	XX	220-25FH	Unused
SARC offset = 0260H, 0660H, 0A60H and 0E60H			
0	XX	260H	SARC Indirect Path Register
0	XX	261H	SARC Unused
0	XX	262H	SARC Section Configuration
0	XX	263H	SARC Section RSALM enable
0	XX	264H	SARC Section RLAISINS enable
0	XX	265H	SARC Section TLRDIINS enable
0	XX	266H	SARC Unused
0	XX	267H	SARC Unused
0	XX	268H	SARC Path Configuration
0	XX	269H	SARC Path RALM Enable
0	XX	26AH	SARC Path RPAISINS Enable
0	XX	26B-26FH	SARC Reserved
0	XX	270H	SARC LOP Pointer Status
0	XX	271H	SARC LOP Pointer Interrupt Enable
0	XX	272H	SARC LOP Pointer Interrupt Status
0	XX	273H	SARC AIS Pointer Status
0	XX	274H	SARC AIS Pointer Interrupt Enable
0	XX	275H	SARC AIS Pointer Interrupt Status
0	XX	276-27FH	SARC Reserved
R8TD offset = 0280H, 0680H, 0A80H and 0E80H			
0	XX	280H	R8TD APS Control and Status
0	XX	281H	R8TD APS Interrupt Status
0	XX	282H	R8TD APS Line Code Violation Count

A[12] RX/TX	A[11:10]	A[9:0] (HEX)	Register Description
0	XX	283H	R8TD APS Analog Control 1
0	XX	284H	R8TD APS Analog Control 2
0	XX	285-28FH	R8TD Reserved
CSTR			
0	00	290H	CSTR Control
0	00	291H	CSTR Interrupt Enable and APS CSU Lock Status
0	00	292H	CSTR APS CSU Lock Interrupt Indication
0	00	293-29FH	CSTR Reserved
RDLL			
0	00	2A0H	RDLL Configuration
0	00	2A1H	RDLL Reserved #1
0	00	2A2H	RDLL Reserved #2
0	00	2A3H	RDLL Control Status
0	00	2A4-2AFH	RDLL Reserved
0	XX	2B0-2FFH	Unused
RSTSI			
0	00	300H	RSTSI Control Page Indirect Address
0	00	301H	RSTSI Control Page Indirect Data
0	00	302H	RSTSI Configuration
0	00	303H	RSTSI Interrupt Status
0	00	303-30FH	RSTSI Reserved
RCFP offset = 0310H, 0710H, 0B10H and 0F10H			
0	XX	310H	RCFP Configuration
0	XX	311H	RCFP Interrupt Enable
0	XX	312H	RCFP Interrupt Indication and Status
0	XX	313H	RCFP Minimum Packet Length
0	XX	314H	RCFP Maximum Packet Length
0	XX	315H	RCFP LCD Count Threshold
0	XX	316H	RCFP Idle Cell Header and Mask
0	XX	317H	RCFP Receive Byte/Idle Cell Counter (LSB)
0	XX	318H	RCFP Receive Byte/Idle Cell Counter
0	XX	319H	RCFP Receive Byte/Idle Cell Counter (MSB)
0	XX	31AH	RCFP Receive Packet/Cell Counter (LSB)
0	XX	31BH	RCFP Receive Packet/ATM Cell Counter (MSB)
0	XX	31CH	RCFP Receive Erroneous FCS/HCS Counter
0	XX	31DH	RCFP Receive Aborted Packet Counter
0	XX	31EH	RCFP Receive Minimum Length Packet Error
0	XX	31FH	RCFP Receive Maximum Length Packet Error Counter
RXSDQ			
0	00	320H	RXSDQ FIFO Reset
0	00	321H	RXSDQ FIFO Interrupt Enable

A[12] RX/TX	A[11:10]	A[9:0] (HEX)	Register Description
0	00	322H	RXSDQ Reserved
0	00	323H	RXSDQ FIFO Overflow Port and Interrupt Indication
0	00	324H	RXSDQ FIFO EOP Error Port and Interrupt Indication
0	00	325H	RXSDQ FIFO SOP Error Port and Interrupt Indication
0	00	326-327H	RXSDQ Reserved
0	00	328H	RXSDQ FIFO Indirect Address
0	00	329H	RXSDQ FIFO Indirect Configuration
0	00	32AH	RXSDQ FIFO Indirect Data Available Threshold
0	00	32BH	RXSDQ FIFO Indirect Cells and Packets Count
0	00	32CH	RXSDQ FIFO Cells and Packets Accepted Aggregate Count (LSB)
0	00	32DH	RXSDQ FIFO Cells and Packets Accepted Aggregate Count (MSB)
0	00	32EH	RXSDQ FIFO Cells and Packets Dropped Aggregate Count
0	00	32FH	RXSDQ Reserved
RXPHY			
0	00	330H	RXPHY Configuration
0	00	331H	RXPHY Interrupt Status
0	00	332H	RXPHY Interrupt Enable
0	00	333H	RXPHY Indirect Burst Size
0	00	334H	RXPHY Calendar Length
0	00	335H	RXPHY Calendar Indirect Address Data
0	00	336H	RXPHY Data Type Field
0	00	337-33FH	RXPHY Reserved
RTDP offset = 0340H, 0740H, 0B40H and 0F40H			
0	XX	340H	RTDP Indirect Channel Select
0	XX	341H	RTDP Indirect Configuration
0	XX	342H	RTDP Indirect Minimum Packet Length and Bit Order
0	XX	343H	RTDP Indirect Maximum Packet Length
0	XX	344H	RTDP Indirect LCD Count Threshold
0	XX	345H	RTDP Indirect Idle Cell Header and Mask
0	XX	346H	RTDP Indirect Receive Byte/Idle Cell Counter (LSB)
0	XX	347H	RTDP Indirect Receive Byte/Idle Cell Counter (MSB)
0	XX	348H	RTDP Indirect Packet/Cell Counter (LSB)
0	XX	349H	RTDP Indirect Receive Packet/Cell Counter (MSB)
0	XX	34AH	RTDP Indirect Receive Erroneous FCS/HCS Counter
0	XX	34BH	RTDP Indirect Receive Aborted Packet Counter
0	XX	34CH	RTDP Indirect Receive Minimum Length Packet Error Counter
0	XX	34DH	RTDP Indirect Receive Maximum Length Packet Error Counter
0	XX	34E-34FH	RTDP Reserved
0	XX	350H	RTDP Interrupt Enable Channels 0 and 1
0	XX	351H	RTDP Interrupt Enable Channels 2 and 3

A[12] RX/TX	A[11:10]	A[9:0] (HEX)	Register Description
0	XX	352-355H	RTDP Reserved
0	XX	356H	RTDP Interrupt Indication Channels 0 and 1
0	XX	357H	RTDP Interrupt Indication Channels 2 and 3
0	XX	358-35BH	RTDP Reserved
0	XX	35CH	RTDP OOF Status
0	XX	35DH	RTDP LOF Status
0	XX	35E-35FH	RTDP Reserved
RCAS12 offset = 0360H, 0760H, 0B60H and 0F60H			
0	XX	360H	RCAS12 Channel Disable
0	XX	361H	RCAS12 Channel Loopback Enable
0	XX	362H	RCAS12 Timeslot 0 Configuration
0	XX	363H	RCAS12 Timeslot 1 Configuration
0	XX	364H	RCAS12 Timeslot 2 Configuration
0	XX	365H	RCAS12 Timeslot 3 Configuration
0	XX	366H	RCAS12 Timeslot 4 Configuration
0	XX	367H	RCAS12 Timeslot 5 Configuration
0	XX	368H	RCAS12 Timeslot 6 Configuration
0	XX	369H	RCAS12 Timeslot 7 Configuration
0	XX	36AH	RCAS12 Timeslot 8 Configuration
0	XX	36BH	RCAS12 Timeslot 9 Configuration
0	XX	36CH	RCAS12 Timeslot 10 Configuration
0	XX	36DH	RCAS12 Timeslot 11 Configuration
0	XX	36E-36FH	RCAS12 Reserved
SFBA offset = 0370H, 0770H, 0B70H and 0F70H			
0	XX	370H	SFBA Configuration and Status
0	XX	371H	SFBA Interrupt Enable
0	XX	372H	SFBA Interrupt Status
0	XX	373-37FH	SFBA Reserved
DCRU155_622 offset = 0380H, 0780H, 0B80H and 0F80H			
0	XX	380H	DCRU155_622 Reserved
0	XX	381H	DCRU155_622 Status and Interrupt Enable
0	XX	382H	DCRU155_622 Interrupt Status
0	XX	383H	DCRU155_622 Powerdown
0	XX	384-38FH	DCRU155_622 Configuration
0	00	390-3FFH	Unused
TRANSMIT			
1	00	000-01FH	Reserved
Tx2488 Analog			
1	00	020H	Tx2488 Analog Control/Status
1	00	021H	Tx2488 ABC Control
1	00	022H	Tx2488 Fixed Pattern Register

A[12] RX/TX	A[11:10]	A[9:0] (HEX)	Register Description
1	00	023-02FH	Tx2488 Analog Reserved
QUAD 622 Tx MABC			
1	00	030H	QUAD 622 Tx MABC CSUT Control Register
1	00	031H	QUAD 622 TX CSUT Clock Detector Control Register
1	00	032H	QUAD 622 TX CSUT Interrupt Status Register
QUAD 622 TX MABC offset = 1033H, 1433H, 1833H and 1C33H			
1	XX	033H	QUAD 622 TX MABC and JAT622 Channel Control & Status Register
1	XX	034H	QUAD 622 TX Channel Data Path & PRBS Control Register
1	XX	035-03FH	QUAD 622 TX Slice Reserved
STLI			
1	00	040H	STLI Clock Configuration
1	00	041-05FH	STLI Reserved
JAT622 offset = 1060H, 1460H, 1860H and 1C60H			
1	XX	060H	JAT622 Configuration
1	XX	061H	JAT622 Configuration and Interrupt Enable
1	XX	062H	JAT622 Status
1	XX	063H	JAT622 Powerdown
1	XX	064-07FH	Unused
TRMP offset = 1080H, 1480H, 1880H and 1C80H			
1	XX	080H	TRMP Configuration
1	XX	081H	TRMP Register Insertion
1	XX	082H	TRMP Error Insertion
1	XX	083H	TRMP Transmit J0 and Z0
1	XX	084H	TRMP Transmit E1 and F1
1	XX	085H	TRMP Transmit D1D3 and D4D12
1	XX	086H	TRMP Transmit K1 and K2
1	XX	087H	TRMP Transmit S1 and Z1
1	XX	088H	TRMP Transmit Z2 and E2
1	XX	089H	TRMP H1 and H2 Mask
1	XX	08AH	TRMP B1 and B2 Mask
1	XX	08B-08FH	TRMP Reserved
1	XX	090-09FH	Unused
TTTP SECTION offset = 10A0H, 14A0H, 18A0H and 1CA0H			
1	XX	0A0H	TTTP SECTION Indirect Address
1	XX	0A1H	TTTP SECTION Indirect Data
1	XX	0A2-0AFH	TTTP SECTION Reserved
1	XX	0B0-0BFH	Unused
TTTP PATH offset = 10C0H, 14C0H, 18C0H and 1CC0H			
1	XX	0C0H	TTTP PATH Indirect Address
1	XX	0C1H	TTTP PATH Indirect Data

A[12] RX/TX	A[11:10]	A[9:0] (HEX)	Register Description
1	XX	0C2-0CFH	TTTP PATH Reserved
1	XX	0D0-0FFH	Unused
THPP offset = 1100H, 1500H, 1900H and 1D00H			
1	XX	100H	THPP Indirect Address
1	XX	101H	THPP Indirect Data
1	XX	102H	THPP Reserved
1	XX	103-17FH	THPP Reserved
1	XX	180-1FFH	Reserved
TSVCA offset = 1200H, 1600H, 1A00H and 1E00H			
1	XX	200H	TSVCA Indirect Address
1	XX	201H	TSVCA Indirect Data
1	XX	202H	TSVCA Reserved #1
1	XX	203H	TSVCA Positive Justification Interrupt Status
1	XX	204H	TSVCA Negative Justification Interrupt Status
1	XX	205H	TSVCA FIFO Overflow Interrupt Status
1	XX	206H	TSVCA FIFO Underflow Interrupt Status
1	XX	207H	TSVCA Pointer Justification Interrupt Enable
1	XX	208H	TSVCA FIFO Interrupt Enable
1	XX	209H	TSVCA Reserved #2
1	XX	20AH	TSVCA Reserved #3
1	XX	20BH	TSVCA Performance Monitor Trigger
1	XX	20C-20FH	TSVCA Reserved
1	00	210-23FH	Unused
PRGM offset = 1240H, 1640H, 1A40H and 1E40H			
1	XX	240H	PRGM Indirect Address
1	XX	241H	PRGM Indirect Data
1	XX	242H	PRGM Generator Payload Configuration
1	XX	243H	PRGM Monitor Payload Configuration
1	XX	244H	PRGM Monitor Byte Error Interrupt Status
1	XX	245-248H	PRGM Reserved
1	XX	249H	PRGM Monitor Synchronization Interrupt Status
1	XX	24AH	PRGM Monitor Synchronization Interrupt Enable
1	XX	24BH	PRGM Monitor Synchronization Status
1	XX	24CH	PRGM Performance Counters Transfer Trigger
1	XX	24D-25FH	PRGM Reserved
SIRP offset = 1260H, 1660H, 1A60H and 1E60H			
1	XX	260H-263H	SIRP Timeslot Configuration
1	XX	264-26BH	SIRP Reserved
1	XX	26CH	SIRP Configuration
1	XX	26D-26FH	SIRP Reserved

A[12] RX/TX	A[11:10]	A[9:0] (HEX)	Register Description
1	XX	270-27FH	Unused
T8TE offset = 1280H, 1680H, 1A80H and 1E80H			
1	XX	280H	T8TE APS Control and Status
1	XX	281H	T8TE APS Interrupt Status
1	XX	282H	T8TE APS TelecomBus Mode #1
1	XX	283H	T8TE APS TelecomBus Mode #2
1	XX	284H	T8TE APS Test Pattern
1	XX	285H	T8TE APS Analog Control
1	XX	286H	T8TE APS DTB Bus
1	XX	287-28FH	T8TE APS Reserved
1	XX	290-29FH	Unused
TDLL			
1	00	2A0H	TDLL Configuration
1	00	2A1H	TDLL Reserved #1
1	00	2A2H	TDLL Reserved #2
1	00	2A3H	TDLL Control Status
1	00	2A4-2AFH	TDLL Reserved Control Page
1	00	2B0-2FFH	Unused
TSTSI			
1	00	300H	TSTSI Control Page Indirect Address
1	00	301H	TSTSI Control Page Indirect Data
1	00	302H	TSTSI Configuration
1	00	303H	TSTSI Interrupt Status
1	00	304-30FH	TSTSI Reserved
TCFP offset = 1310H, 1710H, 1B10H and 1F10H			
1	XX	310H	TCFP Configuration
1	XX	311H	TCFP Interrupt Indication
1	XX	312H	TCFP Idle/Unassigned ATM Cell Header
1	XX	313H	TCFP Diagnostics
1	XX	314H	TCFP Transmit Cell/Packet Counter (LSB)
1	XX	315H	TCFP Transmit Cell/Packet Counter (MSB)
1	XX	316H	TCFP Transmit Byte Counter (LSB)
1	XX	317H	TCFP Transmit Byte Counter
1	XX	318H	TCFP Transmit Byte Counter (MSB)
1	XX	319H	TCFP Aborted Packet Counter
1	XX	31A-31FH	TCFP Reserved
TXSDQ			
1	00	320H	TXSDQ FIFO Reset
1	00	321H	TXSDQ FIFO Interrupt Enable
1	00	322H	TXSDQ Reserved
1	00	323H	TXSDQ FIFO Overflow Port and Interrupt Indication

A[12] RX/TX	A[11:10]	A[9:0] (HEX)	Register Description
1	00	324H	TXSDQ FIFO EOP Error Port and Interrupt Indication
1	00	325H	TXSDQ FIFO SOP Error Port and Interrupt Indication
1	00	326H	TXSDQ Reserved
1	00	327H	TXSDQ Reserved
1	00	328H	TXSDQ FIFO Indirect Address
1	00	329H	TXSDQ FIFO Indirect Configuration
1	00	32AH	TXSDQ FIFO Indirect Data and Buffer Available Thresholds
1	00	32BH	TXSDQ FIFO Indirect Cells and Packets Count
1	00	32CH	TXSDQ FIFO Cells and Packets Accepted Aggregate Count (LSB)
1	00	32DH	TXSDQ FIFO Cells and Packets Accepted Aggregate Count (MSB)
1	00	32EH	TXSDQ FIFO Cells and Packets Dropped Aggregate count
1	00	32FH	TXSDQ Reserved
TXPHY			
1	00	330H	TXPHY Configuration
1	00	331H	TXPHY Interrupt Status
1	00	332H	TXPHY Interrupt Enable
1	00	333H	TXPHY Data Type Field
1	00	334-33FH	TXPHY Reserved
TTDP offset = 1340H, 1740H, 1B40H and 1F40H			
1	XX	340H	TTDP Indirect Channel Select
1	XX	341H	TTDP Indirect Configuration
1	XX	342H	TTDP Indirect Idle/Unassigned ATM Cell Header
1	XX	343H	TTDP Indirect Diagnostics
1	XX	344H	TTDP Indirect Transmit Cell/Packet Counter (LSB)
1	XX	345H	TTDP Indirect Transmit Cell/Packet Counter (MSB)
1	XX	346H	TTDP Indirect Transmit Byte Counter (LSB)
1	XX	347H	TTDP Indirect Transmit Byte Counter (MSB)
1	XX	348H	TTDP Indirect Aborted Packet Counter
1	XX	349H	TTDP CRC Error Mask
1	XX	34AH	TTDP Interrupt Enable 1
1	XX	34BH	TTDP Interrupt Enable 2
1	XX	34CH	TTDP Interrupt 1
1	XX	34DH	TTDP Interrupt 2
1	XX	34EH	TTDP Transmit Off
1	XX	34FH	TTDP Reserved
1	00	350-35FH	Unused
TCAS12 offset = 1360H, 1760H, 1B60H and 1F60H			
1	XX	360H	TCAS12 Channel Configuration
1	XX	361H	TCAS12 Reserved
1	XX	362H	TCAS12 Timeslot 0 Configuration

A[12] RX/TX	A[11:10]	A[9:0] (HEX)	Register Description
1	XX	363H	TCAS12 Timeslot 1 Configuration
1	XX	364H	TCAS12 Timeslot 2 Configuration
1	XX	365H	TCAS12 Timeslot 3 Configuration
1	XX	366H	TCAS12 Timeslot 4 Configuration
1	XX	367H	TCAS12 Timeslot 5 Configuration
1	XX	368H	TCAS12 Timeslot 6 Configuration
1	XX	369H	TCAS12 Timeslot 7 Configuration
1	XX	36AH	TCAS12 Timeslot 8 Configuration
1	XX	36BH	TCAS12 Timeslot 9 Configuration
1	XX	36CH	TCAS12 Timeslot 10 Configuration
1	XX	36DH	TCAS12 Timeslot 11 Configuration
1	XX	36EH	TCAS12 Idle Timeslot Fill Data
1	XX	36FH	TCAS12 Reserved
1	00	370-3FFH	Unused

Notes on Register Memory Map

1. For all register accesses, CSB must be low.
2. Addresses that are not shown must be treated as Reserved.
3. A[13] is the test resister select (TRS) and should be set to logic 0 for normal mode register access.

11 Normal Mode Register Description

Normal mode registers are used to configure and monitor the operation of the S/UNI MULTI-48 device.

Normal mode registers (as opposed to test mode registers) are selected when TRS(A[13]) is low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of this product, unused register bits must be written with logic 0. Reading back unused bits can produce either a logic 1 or a logic 0; therefore, unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the S/UNI MULTI-48 to determine the programming state of the device.

3. Writeable normal mode register bits are cleared to logic 0 upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect S/UNI MULTI-48 operation unless otherwise noted.

5. Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the S/UNI MULTI-48 device operates as intended, reserved register bits must only be written with the logic level as specified. Writing to reserved registers should be avoided unless otherwise specified.

11.1 Registers

Register 0000H: S/UNI MULTI-48 DEVICE ID Register

Bit	Type	Function	Default
15	R	ID[15]	0
14	R	ID[14]	1
13	R	ID[13]	0
12	R	ID[12]	1
11	R	ID[11]	0
10	R	ID[10]	0
9	R	ID[9]	1
8	R	ID[8]	1
7	R	ID[7]	0
6	R	ID[6]	1
5	R	ID[5]	1
4	R	ID[4]	0
3	R	ID[3]	0
2	R	ID[2]	0
1	R	ID[1]	0
0	R	ID[0]	0

ID[15:0]

The ID[15:0] bits contain the BCD encoded number 5360.

Register 0001H: S/UNI MULTI-48 Manufacturer Code and Revision Number

Bit	Type	Function	Default
15	R	JTAG[11]	0
14	R	JTAG[10]	0
13	R	JTAG[9]	0
12	R	JTAG[8]	0
11	R	JTAG[7]	1
10	R	JTAG[6]	1
9	R	JTAG[5]	0
8	R	JTAG[4]	0
7	R	JTAG[3]	1
6	R	JTAG[2]	1
5	R	JTAG[1]	0
4	R	JTAG[0]	1
3	R	REV[3]	0
2	R	REV[2]	0
1	R	REV[1]	0
0	R	REV[0]	1

REV[3:0]

The REV[3:0] bits contain the revision number of this device. The value 1 is for revision B.

JTAG[0]

The JTAG[0] bit is logic 1.

JTAG[11:1]

The JTAG[11:1] bits contain the JTAG manufacturer's code .

Register 0002H: S/UNI MULTI-48 Global Performance Monitor Update and Clock Activity Monitor

Bit	Type	Function	Default
15	R	TIP	X
14	—	Unused	X
13	—	Unused	X
12	—	Unused	X
11	—	Unused	X
10	—	Unused	X
9	—	Unused	X
8	R	SYSCLKACT	X
7	R	Unused	X
6	R	Unused	X
5	R	Unused	X
4	R	Unused	X
3	R	Unused	X
2	R	Unused	X
1	R	Unused	X
0	R	Unused	X

This register is the global performance monitor update register. Writing any value to this register will trigger a global update of all the performance monitoring counters of the device.

Note that RFCLK and TFCLK activity monitors are located within the RDLL and TDLL registers. RFCLKI bit in register 02A3H (RDLL Control Status) and TFCLKI bit in register 12A3H (TDLL Control Status) respectively monitor RFCLK and TFCLK. REFCLK77 activity monitor is located in register 0034H (Quad 622 Rx MABC Interrupt Status Register), while REFCLK155 activity monitor is located in register 1020H (Tx2488 Analog Control/Status).

SYSCLKACT

The SYSCLKACT bit transitions to logic 1 when a rising edge is detected over the SYSCLK pin. It is reset to logic 0 after a read of this register is performed. Note that this bit is only valid when the SYSCLK pin is enabled (SYSCLK_EN set to logic 1, register 0016H).

TIP

The TIP bit transitions to logic 1 when this register is written to. It returns to logic 0 after all active blocks have updated their performance monitor counters.

Register 0003H: S/UNI MULTI-48 Master Software Resets Register

Bit	Type	Function	Default
15	—	Unused	X
14	R/W	APS_DRESET[4]	0
13	R/W	APS_DRESET[3]	0
12	R/W	APS_DRESET[2]	0
11	R/W	APS_DRESET[1]	0
10	R/W	RESETSL[4]	0
9	R/W	RESETSL[3]	0
8	R/W	RESETSL[2]	0
7	R/W	RESETSL[1]	0
6	R/W	DRESET	0
5	R/W	ARST_1X2488	0
4	R/W	ARST_4X622	0
3	R/W	RST_LAS4x622	0
2	R/W	RST_JAT622	0
1	R/W	DRST_DCRU155_622	0
0	R/W	APS_RESET	0

APS_RESET

The APS_RESET bit is used to reset all of the APS ports analog and digital circuitry, except for the smart framing logic. When APS_RESET is logic 1, the reset is enabled. When APS_RESET is logic 0, the reset is not enabled. When used, APS_RESET should be asserted for at least 1 ms to reset circuitry properly. Note that this reset bit should not be used as an analog power saving mode when APS ports are not used. Analog blocks should rather be powered down using their individual reset or enable bits. These bits are located in the R8TD APS Analog Control 1 register (0283H), CSTR Control register (0290H) and T8TE APS Analog Control register (1285H).

DRST_DCRU155_622

The DRST_DCRU155_622 software reset (DRST_DCRU155_622) bit resets the DCRU155_622 digital clock recovery unit. When a logic 1 is written to DRST_DCRU155_622, the DCRU155_622 is held in reset. When a logic 0 is written to DRST_DCRU155_622, the DCRU155_622 operates normally. When used, DRST_DCRU155_622 should be asserted for at least 100 ns to reset circuitry properly.

RST_JAT622

The RST_JAT622 software reset bit resets the JAT622 block. When a logic 1 is written to RST_JAT622, the JAT622 block is held in reset. When a logic 0 is written to RST_JAT622, the JAT622 block operates normally. When used, RST_JAT622 should be asserted for at least 100 ns to reset circuitry properly.

RST_LAS4x622

The RST_LAS4x622 software reset bit resets the LAS4x622 block. When a logic 1 is written to RST_LAS4x622, the LAS4x622 block is held in reset. When a logic 0 is written to RST_LAS4x622, the LAS4x622 block operates normally. When used, RST_LAS4x622 should be asserted for at least 100 ns to reset circuitry properly.

ARST_4x622

The 4x622 Analog software reset (ARST_4x622) bit resets the 4x622 analog circuit. When a logic 1 is written to ARST_4x622, the 4x622 analog is held in reset. When a logic 0 is written to ARST_4x622, the 4x622 analog operates normally. When used, ARST_4x622 should be asserted for at least 106 us to reset circuitry properly.

ARST_1x2488

The 1x2488 Analog software reset (ARST_1x2488) bit resets the 1x2488 analog circuit. When a logic 1 is written to ARST_1x2488, the 1x2488 analog is held in reset. When a logic 0 is written to ARST_1x2488, the 1x2488 analog operates normally. When used, ARST_1x2488 should be asserted for at least 2 ms to reset circuitry properly.

DRESET

The DRESET bit is used as a software controlled reset signal for all the digital logic in the device (see note) except this register's bits 0 to 10. All register 0003H soft resets except the APS_DRESET[4:1] bits are not affected by DRESET. When DRESET is logic 1, the reset is enabled. When DRESET is logic 0, the reset is not enabled. When used, DRESET should be asserted for at least 100 ns to reset circuitry properly.

Note: DRESET does not affect the following blocks (nor their respective registers): LAS4x622 (Quad 622 Rx and Quad 622 Tx), use RST_LAS4x622 instead; JAT622, use RST_JAT622 instead; DCRU155_622, use RST_DCRU155_622 instead; CSTR, use APS_RESET instead

RESETSL[4:1]

The slice software reset (RESETSL[4:1]) bits reset the corresponding SONET/SDH STS-12/STM-4 processing slice. When a logic 1 is written to RESETSL[X], SONET/SDH STS-12/STM-4 slice X (SBER, RRMP, RTTPs, RHPP, RSVCA, TSVCA, SARC, TTTPs, THPP, TRMP, PRGM, SIRP) is held in reset. When a logic 0 is written to RESETSL[X], SONET/SDH STS-12/STM-4 slice X operates normally. When used, RESETSL[X] should be asserted for at least 100 ns to reset circuitry properly.

APS_DRESET[4:1]

The APS digital software reset (APS_DRESET[4:1]) bits reset the corresponding APS link. When APS_DRESET[X] is set to logic 1, the digital part of APS link X (R8TD, T8TE) is held in reset. When APS_DRESET[X] is set to logic 0, APS link X operates normally. When used, APS_DRESET[X] should be asserted for at least 100 ns to reset circuitry properly. Note that APS_DRESET[4:1] bits do not reset the CSTR digital logic or registers.

Register 0004H: S/UNI MULTI-48 Master Configuration Register #1

Bit	Type	Function	Default
15	R/W	GINTE	0
14	R/W	Reserved	0
13	R/W	Reserved	0
12	R/W	Reserved	0
11	R/W	WCIMODE	0
10	R/W	CHAN4SEL	0
9	R/W	TSTS12EN[4]	0
8	R/W	TSTS12EN[3]	0
7	R/W	TSTS12EN[2]	0
6	R/W	TSTS12EN[1]	0
5	R/W	RSTS12EN[4]	0
4	R/W	RSTS12EN[3]	0
3	R/W	RSTS12EN[2]	0
2	R/W	RSTS12EN[1]	0
1	R/W	PL3EN	0
0	R	STS48EN	X

STS48EN

The STS48EN bit monitors the STS48EN input pin with regards to the STS48ENB register bit (register 001CH: S/UNI MULTI-48 Miscellaneous Defect Configuration #3). The STS48EN pin value can be inverted using the STS48ENB register bit. The STS48EN register bit reports the value of: STS48EN pin XOR STS48ENB register bit.

PL3EN

The POS-PHY Level 3 Select bit (PL3EN) is XOR'ed with the PL3EN pin to select POS-PHY Level 3 mode on the system interface. When the result of PL3EN pin XOR PL3EN register bit is logic 1, the system bus operates in POS-PHY Level 3 mode. When the result of PL3EN pin XOR PL3EN register bit is logic 0, the bus operates as a UTOPIA Level 3 bus. Reading this bit gives back the value written in this register bit.

RSTS12EN[4:1]

The RSTS12EN[x] bit is used to select STS-12 line interface mode for the channel associated with RXD_P[x]/RXD_N[x]. RSTS12EN[x] takes lower precedence than STS48EN. When STS48EN is logic 0 and RSTS12EN[x] is logic 1, then STS-12 mode is selected. When STS48EN is logic 0 and RSTS12EN[x] is logic 0, then STS-3 mode is selected.

TSTS12EN[4:1]

The TSTS12EN[x] bit is used to select STS-12 line interface mode for the channel associated with TXD_P[x]/TXD_N[x]. TSTS12EN[x] takes lower precedence than STS48EN. When STS48EN is logic 0 and TSTS12EN[x] is logic 1, then STS-12 mode is selected. When STS48EN is logic 0 and TSTS12EN[x] is logic 0, then STS-3 mode is selected.

CHAN4SEL

The CHAN4SEL bit is used to select the number of channels on the UL3/PL3 bus. When CHAN4SEL is logic 1, then only 4 channels are available on the UL3/PL3 bus (RADR[3:0]/TADR[3:0]) at addresses 0000, 0001, 0010 and 0011. When CHAN4SEL is logic 0, then 16 channels are available on the UL3/PL3 bus.

WCIMODE

The write on clear interrupt mode (WCIMODE) bit selects the clear interrupt mode. When a logic 1 is written to WCIMODE, the clear interrupt mode is clear on write. When a logic 0 is written to WCIMODE, the clear interrupt mode is clear on read.

GINTE

The Global Interrupt Enable (GINTE) bit controls the assertion of the interrupt pin (INTB) output. When a logic 1 is written to GINTE, any pending interrupt will assert the interrupt (INTB) output. When a logic 0 is written to GINTE, pending interrupt will not assert the interrupt (INTB) output.

Register 0005H: S/UNI MULTI-48 Master Configuration Register #2

Bit	Type	Function	Default
15	R/W	T8TE_MUX[4]	0
14	R/W	T8TE_MUX[3]	0
13	R/W	T8TE_MUX[2]	0
12	R/W	T8TE_MUX[1]	0
11	R/W	RSTSI_MUX[4]	0
10	R/W	RSTSI_MUX[3]	0
9	R/W	RSTSI_MUX[2]	0
8	R/W	RSTSI_MUX[1]	0
7	R/W	PRGM_MUX[4]	0
6	R/W	PRGM_MUX[3]	0
5	R/W	PRGM_MUX[2]	0
4	R/W	PRGM_MUX[1]	0
3	R/W	THPP_MUX[4]	0
2	R/W	THPP_MUX[3]	0
1	R/W	THPP_MUX[2]	0
0	R/W	THPP_MUX[1]	0

THPP_MUX[4:1]

The THPP_MUX[x] bit is used to select the source of the data to the xth THPP block. When THPP_MUX[x] is logic 0, the source of the data to the xth THPP block is the transmit UL3/PL3 interface (TXPHY→TXSDQ→TCFP→TSTSI→PRGM→SIRP→THPP). When THPP_MUX[x] is logic 1, the source of the data to the xth THPP block is the receive APS interface (R8TD→x-bar→THPP).

PRGM_MUX[4:1]

The PRGM_MUX[x] bit is used to select the source of the data to the xth PRGM monitor. When PRGM_MUX[x] is logic 0, the source of the data to the xth PRGM monitor is the receive line interface (RRMP→RHPP→RSVCA→PRGM). When PRGM_MUX[x] is logic 1, the source of the data to the xth PRGM monitor is the receive APS interface (R8TD→x-bar→PRGM).

RSTSI_MUX[4:1]

The RSTSI_MUX[x] bit is used to select the source of the data to the xth RSTSI block. When RSTSI_MUX[x] is logic 0, the source of the data to the xth RSTSI block is the receive line interface (RRMP→RHPP→RSVCA→RSTSI). When RSTSI_MUX[x] is logic 1, the source of the data to the xth RSTSI block is the receive APS interface (R8TD→x-bar→RSTSI).

T8TE_MUX[4:1]

The T8TE_MUX[x] bit is used to select the source of the data to the xth T8TE block. When T8TE_MUX[x] is logic 0, the source of the data to the xth T8TE block is the transmit PL3 interface (TXPHY→TXSDQ→TCFP→TSTSI→PRGM→SIRP→THPP→x-bar→T8TE). When T8TE_MUX[x] is logic 1, the source of the data to the xth T8TE block is the receive line interface (RRMP→RHPP→RSVCA→x-bar→T8TE).

Register 0006H: S/UNI MULTI-48 Line Side Receive Configuration

Bit	Type	Function	Default
15	—	Unused	X
14	—	Unused	X
13	R/W	RCLKOSEL[1]	0
12	R/W	RCLKOSEL[0]	0
11	R/W	RSTSISW[1]	0
10	R/W	RSTSISW[0]	1
9	R/W	RDDS	0
8	—	Unused	X
7	R/W	RSTS12C[4]	0
6	R/W	RSTS12C[3]	0
5	R/W	RSTS12C[2]	0
4	R/W	RSTS12C[1]	0
3	R/W	RSTS12CSL[4]	0
2	R/W	RSTS12CSL[3]	0
1	R/W	RSTS12CSL[2]	0
0	R/W	RSTS12CSL[1]	0

RSTS12CSL[4:1]

The line side receive STS-12 slave concatenation mode (RSTS12CSL[4:1]) bits enable the processing of a slave STS-12c (VC-4-4c) payload for the corresponding STS-12/STM-4 SONET/SDH receive slice. RSTS12CSL[4:1] should be written with “1110” for STS-48c (VC-4-16c) payload processing. For sub-STS-48c (VC-4-16c) payload types, RSTS12CSL[4:1] should be written with “0000”.

RSTS12C[4:1]

The line side receive STS-12 concatenation mode (RSTS12C[4:1]) bits enable the processing of a master or slave STS-12c (VC-4-4c) payload for the corresponding SONET/SDH STS-12/STM-4 slice. RSTS12C[x] should be written with a logic 1 value when the receive SONET/SDH STS-12/STM-4 slice x processes part of an STS-48c (VC-4-16c) payload or an STS-12c (VC-4-4c) payload. RSTS12C[x] should be written with a logic 0 value when the receive SONET/SDH STS-12/STM-4 slice x processes sub-STS-12c (VC-4-4c) payload types.

RDDS

The receive disable descrambling (RDDS) bit disables the de scrambling of the SONET/SDH input line data stream. When a logic 1 is written to RDDS, the input line data stream is not de scrambled. When a logic 0 is written to RDDS, the input line data stream is de-scrambled.

RSTSISW[1:0]

The receive RSTSI switching mode (RSTSISW[1:0]) bits select the operational switching mode of the RSTSI. RSTSISW[1:0] must be set to "10" in STS-48c (VC-4-16c) payload mode. RSTSISW[1:0] must be set to "00" in sub STS-48c (VC-4-16c) payload modes when using the XBAR features of the RSTSI block. RSTSISW[1:0] must be set to "01" in sub STS-48c (VC-4-16c) payload modes for basic usage.

RSTSISW[1:0]	Mode
00	User configured timeslot mapping
01	Bypass mode (no remapping)
10	STS-48c (VC-4-16c) mode
11	Reserved

RCLKOSEL[1:0]

The RCLKO channel selection (RCLKOSEL[1:0]) bits select which internal receive clock will be driven on the S/UNI MULTI-48 RCLKO output pin. When RCLKOSEL[1:0] is "00", receive clock from slice 1 will be driven on the RCLKO pin. When RCLKOSEL[1:0] is "01", "10" or "11", receive clock from slice 2, 3 or 4 (respectively) will be driven on the RCLKO pin.

Register 0007H: S/UNI MULTI-48 Line Side Transmit Configuration

Bit	Type	Function	Default
15	R/W	RXAPS_PSEUDO_MST[3]	0
14	R/W	RXAPS_PSEUDO_MST[2]	0
13	R/W	RXAPS_PSEUDO_MST[1]	0
12	R/W	RXAPS_PSEUDO_MST[0]	0
11	R/W	TSTSISW[1]	0
10	R/W	TSTSISW[0]	1
9	R/W	TDS	0
8	—	Unused	X
7	R/W	TSTS12C[4]	0
6	R/W	TSTS12C[3]	0
5	R/W	TSTS12C[2]	0
4	R/W	TSTS12C[1]	0
3	R/W	TSTS12CSL[4]	0
2	R/W	TSTS12CSL[3]	0
1	R/W	TSTS12CSL[2]	0
0	R/W	TSTS12CSL[1]	0

TSTS12CSL[4:1]

The line side transmit STS-12 slave concatenation mode (TSTS12CSL[4:1]) bits enable the processing of a slave STS-12c (VC-4-4c) payload for the corresponding STS-12/STM-4 SONET/SDH transmit slice. RSTS12CSL[4:1] should be written with “1110” for STS-48c (VC-4-16c) payload processing. For sub-STS-48c (VC-4-16c) payload types, RSTS12CSL[4:1] should be written with “0000”.

TSTS12C[4:1]

The line side transmit STS-12 concatenation mode (TSTS12C[4:1]) bits enable the processing of a master or slave STS-12c (VC-4-4c) payload for the corresponding SONET/SDH STS-12/STM-4 slice. TSTS12C[x] should be written with a logic 1 value when the transmit SONET/SDH STS-12/STM-4 slice x processes part of an STS-48c (VC-4-16c) payload or an STS-12c (VC-4-4c) payload. RSTS12C[x] should be written with a logic 0 value when the transmit SONET/SDH STS-12/STM-4 slice x processes sub-STS-12c (VC-4-4c) payload types.

TDS

The transmit disable scrambling (TDS) bit disables the scrambling of the SONET/SDH output line data stream. When a logic 1 is written to TDS, the output line data stream is not scrambled. When a logic 0 is written to TDS, the output line data stream is scrambled.

TSTSISW[1:0]

The transmit TSTSI switching mode (TSTSISW[1:0]) bits select the operational switching mode of the TSTSI. TSTSISW[1:0] must be set to "11" in STS-48c (VC-4-16c) payload mode. TSTSISW[1:0] must be set to "00" in sub STS-48c (VC-4-16c) payload modes when using the XBAR features of the TSTSI block. TSTSISW[1:0] must be set to "01" in sub STS-48c (VC-4-16c) payload modes for basic usage.

TSTSISW[1:0]	Mode
00	User configured timeslot mapping
01	bypass mode (no remapping)
10	Reserved
11	STS-48c (VC-4-16c) mode

RXAPS_PSEUDO_MST[3:0]

The RXAPS_PSEUDO_MST bits force the selection of the following control signals J1, PL and POH to be selected from the SIRP instead of the APS port. In this mode, the datapath comes from the APS port while the J1, PL and POH control signals come from the TCAS-12 frame generator with pointer position at 0 or 522 only. These bits should be set when interfacing the S/UNI MULTI 48 with a device that only operates in MST mode over the 777MHz LVDS interface. The TCAS-12 needs to be provisionning before enabling these bit.

Register 0008H: S/UNI MULTI-48 Diagnostic

Bit	Type	Function	Default
15	R/W	PDLB[4]	0
14	R/W	PDLB[3]	0
13	R/W	PDLB[2]	0
12	R/W	PDLB[1]	0
11	—	Unused	X
10	—	Unused	X
9	—	Unused	X
8	—	Unused	X
7	R/W	PDLB	0
6	R/W	Reserved0	1
5	R/W	Reserved1	0
4	—	Unused	X
3	—	Unused	X
2	—	Unused	X
1	R/W	Reserved	0
0	R/W	Reserved	0

This register contains diagnostic features. Note that the serial diagnostic loopback and line loopback functions are enabled in the analog control registers (RX2488 and TX2488 for STS-48/STM-16 mode and JAT622 and DCRU155_622 for STS-12/STM-4 and STS-3/STM-1 modes).

Reserved

All Reserved bits must be set to their default values for proper operation.

Reserved1

This register bit must be set to logic 1 for normal operation.

Reserved0

This register bit must be set to logic 0 for normal operation.

PDLB

The parallel diagnostic loop back (PDLB) bit enables the parallel loopback from STLI to SRLI in 1x2488 mode. When a logic 1 is written to PDLB, the transmit data and clock from STLI is looped back into SRLI. When a logic 0 is written to PDLB the parallel diagnostic loop back is inactive.

Note: For parallel diagnostic loop back in 1x2488 to work, 1x2488 Analog has to be active.

PDLB[4:1]

The parallel diagnostic loop back (PDLB[4:1]) bits are used to enable diagnostic loopback from the STLI to the SRLI/SFBA for each of the STS-12 slice in quad 622 or 155 mode. For proper operation in STS-12 and STS-3 mode, the TSTS12EN[x] and RSTS12EN[x] bits in register 0004H must be the same for slice x. When PDLB[x] is logic 1, parallel diagnostic loopback is enabled for channel x, the transmit data and clock from STLI is looped back into SRLI/SFBA. When PDLB[x] is logic 0, parallel diagnostic loopback is not enabled for channel x.

Note 1: For parallel diagnostic loop back in quad mode to work, 4x622/155 Analog has to be active.

Note 2: Each of the four channels can be loopbacked independently.

Register 0009H: S/UNI MULTI-48 Transmit PAIS Enable

Bit	Type	Function	Default
15	—	Unused	X
14	—	Unused	X
13	R/W	Reserved	0
12	R/W	Reserved	0
11	R/W	Reserved	0
10	R/W	Reserved	0
9	R/W	Reserved	0
8	R/W	Reserved	0
7	R/W	Reserved	0
6	R/W	Reserved	0
5	R/W	TPAIS_EN[4]	1
4	R/W	TPAIS_EN[3]	1
3	R/W	TPAIS_EN[2]	1
2	R/W	TPAIS_EN[1]	1
1	R/W	Reserved	0
0	R/W	Reserved	0

TPAIS_EN[4:1]

The Transmit Path AIS Enable TPAIS_EN[x] bit controls the insertion of Transmit Path AIS in channel x from APS input port AIS-P requests. When logic 0, TPAIS_EN[x] will prevent Transmit Path AIS from being generated on channel x. When logic 1, TPAIS_EN[x] will enable Transmit Path AIS being requested (from APS input port AIS-P requests) on channel x. When in STS-48c (VC-4-4c) mode, all TPAIS_EN[4:1] must be set to the same value. Note that TPAIS_EN[x] is applied on AIS-P requests from APS channel x right at the output of the R8TD block, prior to the APS-Input XBAR channel realignment. TPAIS_EN channel assignments must thus be consequent with APS-Input port channels rather than channels at the output of the APS-In XBAR.

Register 000AH: S/UNI MULTI-48 APS X-Bar Configuration

Bit	Type	Function	Default
15	R/W	RAPS4[1]	1
14	R/W	RAPS4[0]	1
13	R/W	RAPS3[1]	1
12	R/W	RAPS3[0]	0
11	R/W	RAPS2[1]	0
10	R/W	RAPS2[0]	1
9	R/W	RAPS1[1]	0
8	R/W	RAPS1[0]	0
7	R/W	TAPS4[1]	1
6	R/W	TAPS4[0]	1
5	R/W	TAPS3[1]	1
4	R/W	TAPS3[0]	0
3	R/W	TAPS2[1]	0
2	R/W	TAPS2[0]	1
1	R/W	TAPS1[1]	0
0	R/W	TAPS1[0]	0

TAPS4[1:0], TAPS3[1:0], TAPS2[1:0], TAPS1[1:0]

The transmit APS X-Bar destination bits (TAPSx[1:0]) configure the source STS-12/STM-4 slice for the APSO_P/N[x] output port. For instance, TAPS1[1:0] = “11” selects the STS-12/STM-4 slice #4 to be transmit on APSO_P/N[1].

RAPS4[1:0], RAPS3[1:0], RAPS2[1:0], RAPS1[1:0]

The receive APS X-Bar destination bits (RAPSx[1:0]) configure the source APSI_P/N input port for the STS-12/STM-4 slice #x data stream. For instance, RAPS1[1:0] = “11” selects the APSI_P/N[4] port to be transmit over STS-12/STM-4 slice #1.

Register 000BH: S/UNI MULTI-48 Master Interrupt Status #1

Bit	Type	Function	Default
15	R/W	INTE[1]	0
14	—	Unused	X
13	—	Unused	X
12	R	PRGMI[1]	X
11	R	TSVCAI[1]	X
10	—	Unused	X
9	—	Unused	X
8	R	SARCI[1]	X
7	R	RSVCAI[1]	X
6	—	Unused	X
5	R	SFBAI[1]	X
4	R	PATHRTTPI[1]	X
3	R	RHPPI[1]	X
2	R	SBERI[1]	X
1	R	SECTIONRTTPI[1]	X
0	R	RRMPI[1]	X

This register allows the source of an active interrupt to be identified down to the block level. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

RRMPI[1]…PRGMI[1]

The RRMPI[1] to PRGMI[1] are interrupt status indicators for the corresponding block. The interrupt status is set to logic 1 to indicate a pending interrupt from the corresponding block. The interrupt status bits are independent of the interrupt enable bit.

INTE[1]

The interrupt enable (INTE[1]) bit controls the assertion of the interrupt (INTB) output. When a logic 1 is written to INTE[1], the RRMPI[1]…PRGMI[1] pending interrupt will assert the interrupt (INTB) output (if GINTE is set to logic 1). When a logic 0 is written to INTE[1], the RRMPI[1]…PRGMI[1] pending interrupt will not assert the interrupt (INTB) output.

Register 000CH: S/UNI MULTI-48 Master Interrupt Status #2

Bit	Type	Function	Default
15	R/W	INTE[2]	0
14	—	Unused	X
13	—	Unused	X
12	R	PRGMI[2]	X
11	R	TSVCAI[2]	X
10	—	Unused	X
9	—	Unused	X
8	R	SARCI[2]	X
7	R	RSVCAI[2]	X
6	—	Unused	X
5	R	SFBAI[2]	X
4	R	PATHRTTPI[2]	X
3	R	RHPPI[2]	X
2	R	SBERI[2]	X
1	R	SECTIONRTTPI[2]	X
0	R	RRMPI[2]	X

This register allows the source of an active interrupt to be identified down to the block level. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

RRMPI[2]…PRGMI[2]

The RRMPI[2] to PRGMI[2] are interrupt status indicators for the corresponding block. The interrupt status is set to logic 1 to indicate a pending interrupt from the corresponding block. The interrupt status bits are independent of the interrupt enable bit.

INTE[2]

The interrupt enable (INTE[2]) bit controls the assertion of the interrupt (INTB) output. When a logic 1 is written to INTE[2], the RRMPI[2]…PRGMI[2] pending interrupt will assert the interrupt (INTB) output (if GINTE is set to logic 1). When a logic 0 is written to INTE[2], the RRMPI[2]…PRGMI[2] pending interrupt will not assert the interrupt (INTB) output.

Register 000DH: S/UNI MULTI-48 Master Interrupt Status #3

Bit	Type	Function	Default
15	R/W	INTE[3]	0
14	—	Unused	X
13	—	Unused	X
12	R	PRGMI[3]	X
11	R	TSVCAI[3]	X
10	—	Unused	X
9	—	Unused	X
8	R	SARCI[3]	X
7	R	RSVCAI[3]	X
6	—	Unused	X
5	R	SFBAI[3]	X
4	R	PATHRTTPI[3]	X
3	R	RHPPI[3]	X
2	R	SBERI[3]	X
1	R	SECTIONRTTPI[3]	X
0	R	RRMPI[3]	X

This register allows the source of an active interrupt to be identified down to the block level. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

RRMPI[3]…PRGMI[3]

The RRMPI[3] to PRGMI[3] are interrupt status indicators for the corresponding block. The interrupt status is set to logic 1 to indicate a pending interrupt from the corresponding block. The interrupt status bits are independent of the interrupt enable bit.

INTE[3]

The interrupt enable (INTE[3]) bit controls the assertion of the interrupt (INTB) output. When a logic 1 is written to INTE[3], the RRMPI[3]…PRGMI[3] pending interrupt will assert the interrupt (INTB) output (if GINTE is set to logic 1). When a logic 0 is written to INTE[3], the RRMPI[3]…PRGMI[3] pending interrupt will not assert the interrupt (INTB) output.

Register 000EH: S/UNI MULTI-48 Master Interrupt Status #4

Bit	Type	Function	Default
15	R/W	INTE[4]	0
14	—	Unused	X
13	—	Unused	X
12	R	PRGMI[4]	X
11	R	TSVCAI[4]	X
10	—	Unused	X
9	—	Unused	X
8	R	SARCI[4]	X
7	R	RSVCAI[4]	X
6	—	Unused	X
5	R	SFBAI[4]	X
4	R	PATHRTTPI[4]	X
3	R	RHPPI[4]	X
2	R	SBERI[4]	X
1	R	SECTIONRTTPI[4]	X
0	R	RRMPI[4]	X

This register allows the source of an active interrupt to be identified down to the block level. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

RRMPI[4]…PRGMI[4]

The RRMPI[4] to PRGMI[4] are interrupt status indicators for the corresponding block. The interrupt status is set to logic 1 to indicate a pending interrupt from the corresponding block. The interrupt status bits are independent of the interrupt enable bit.

INTE[4]

The interrupt enable (INTE[4]) bit controls the assertion of the interrupt (INTB) output. When a logic 1 is written to INTE[4], the RRMPI[4]…PRGMI[4] pending interrupt will assert the interrupt (INTB) output (if GINTE is set to logic 1). When a logic 0 is written to INTE[4], the RRMPI[4]…PRGMI[4] pending interrupt will not assert the interrupt (INTB) output.

Register 000FH: S/UNI MULTI-48 Master Interrupt Status #5

Bit	Type	Function	Default
15	R/W	INTE[5]	0
14	—	Unused	X
13	—	Unused	X
12	R	RSTSII	X
11	—	Unused	X
10	—	Unused	X
9	R	RXPHYI	X
8	R	RXSDQI	X
7	R	RTDPI[4]	X
6	R	RTDPI[3]	X
5	R	RTDPI[2]	X
4	R	RTDPI[1]	X
3	R	RCFPI[4]	X
2	R	RCFPI[3]	X
1	R	RCFPI[2]	X
0	R	RCFPI[1]	X

This register is used to indicate interrupts generated from blocks associated with the receive UTOPIA/POS-PHY interfaces, FIFO, and cell/frame processors.

RCFPI[4:1]

The RCFPI[X] interrupt event indication transitions to logic 1 when a hardware interrupt event is sourced from RCFP block. This bit is cleared to logic 0 when the interrupt is cleared.

RTDPI[4:1]

The RTDPI[X] interrupt event indication transitions to logic 1 when a hardware interrupt event is sourced from RTDP block. This bit is cleared to logic 0 when the interrupt is cleared.

RXSDQI

The RXSDQI interrupt event indication transitions to logic 1 when a hardware interrupt event is sourced from the receive system FIFO RXSDQ block. This bit is cleared to logic 0 when the interrupt is cleared.

RXPHYI

The RXPHYI interrupt event indication transitions to logic 1 when a hardware interrupt event is sourced from the receive system UTOPIA/POS-PHY interface RXPHY block. This bit is cleared to logic 0 when the interrupt is cleared.

RSTSII

The RSTSI interrupt event indication transitions to logic 1 when a hardware interrupt event is sourced from the receive RSTSI block. This bit is cleared to logic 0 when the interrupt is cleared.

INTE[5]

The interrupt enable (INTE[5]) bit controls the assertion of the interrupt (INTB) output. When a logic 1 is written to INTE[5], the RCFPI, RXSDQI or RXPHYI pending interrupt will assert the interrupt (INTB) output (if GINTE is set to logic 1). When a logic 0 is written to INTE[5], the RCFPI, RXSDQI or RXPHYI pending interrupt will not assert the interrupt (INTB) output.

Register 0010H: S/UNI MULTI-48 Master Interrupt Status #6

Bit	Type	Function	Default
15	R/W	INTE[6]	0
14	—	Unused	X
13	—	Unused	X
12	R	TSTSII	X
11	—	Unused	X
10	—	Unused	X
9	R	TXPHYI	X
8	R	TXSDQI	X
7	R	TTDPI[4]	X
6	R	TTDPI[3]	X
5	R	TTDPI[2]	X
4	R	TTDPI[1]	X
3	R	TCFPI[4]	X
2	R	TCFPI[3]	X
1	R	TCFPI[2]	X
0	R	TCFPI[1]	X

This register is used to indicate interrupts generated from blocks associated with the transmit UTOPIA/POS-PHY interfaces, FIFO, and cell/frame processors.

TCFPI[4:1]

The TCFPI[X] interrupt event indication transitions to logic 1 when a hardware interrupt event is sourced from TCFP block. This bit is cleared to logic 0 when the interrupt is cleared.

TTDPI[4:1]

The TTDPI[X] interrupt event indication transitions to logic 1 when a hardware interrupt event is sourced from TTDP block. This bit is cleared to logic 0 when the interrupt is cleared.

TXSDQI

The TXSDQI interrupt event indication transitions to logic 1 when a hardware interrupt event is sourced from the receive system FIFO TXSDQ block. This bit is cleared to logic 0 when the interrupt is cleared.

TXPHYI

The RXPHYI interrupt event indication transitions to logic 1 when a hardware interrupt event is sourced from the transmit system UTOPIA/POS-PHY interface TXPHY block. This bit is cleared to logic 0 when the interrupt is cleared.

TSTSII

The TSTSI interrupt event indication transitions to logic 1 when a hardware interrupt event is sourced from the receive TSTSI block. This bit is cleared to logic 0 when the interrupt is cleared.

INTE[6]

The interrupt enable (INTE[6]) bit controls the assertion of the interrupt (INTB) output. When a logic 1 is written to INTE[6], the TCFPI, TXSDQI or TXPHYI pending interrupt will assert the interrupt (INTB) output (if GINTE is set to logic 1). When a logic 0 is written to INTE[6], the TCFPI, TXSDQI or TXPHYI pending interrupt will not assert the interrupt (INTB) output.

Register 0011H: S/UNI MULTI-48 Master Interrupt Status #7

Bit	Type	Function	Default
15	R/W	INTE[7]	0
14	—	Unused	X
13	R	RX_APSI	X
12	R	CSTRI	X
11	R	T8TE4I	X
10	R	T8TE3I	X
9	R	T8TE2I	X
8	R	T8TE1I	X
7	—	Unused	X
6	—	Unused	X
5	R	DLL_TFCLKI	X
4	R	DLL_RFCLKI	X
3	R	R8TD4I	X
2	R	R8TD3I	X
1	R	R8TD2I	X
0	R	R8TD1I	X

This register allows the source of an active interrupt to be identified down to the block level. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

R8TD1I, R8TD2I, R8TD3I, R8TD4I

The R8TDxI interrupt event indication transitions to logic 1 when a hardware interrupt event is sourced from the R8TD1, R8TD2, R8TD3 or R8TD4 blocks. This bit is cleared when the interrupt is cleared.

DLL_RFCLKI, DLL_TFCLKI

The DLL_RFCLKI and DLL_TFCLKI interrupt event indications transition to logic 1 when a hardware interrupt event is sourced from the DLL_RFCLK or DLL_TFCLK, respectively. This bit is cleared when the interrupt is cleared. T8TE1I, T8TE2I, T8TE3I, T8TE4I

The T8TExI interrupt event indication transitions to logic 1 when a hardware interrupt event is sourced from the T8TE1, T8TE2, T8TE3 or T8TE4 blocks. This bit is cleared when the interrupt is cleared.

CSTRI

The CSTRI interrupt event indication (CSTRI) transitions to logic 1 when a hardware interrupt event is sourced from the CSTR block (analog control for the APS Port). This bit is cleared when the interrupt is cleared.

RX_APSI

The RX_APSI interrupt event indication transitions to logic 1 when one of the APS J0 character to APSIFP alignment interrupts is detected (register 0018H). This bit is cleared when the interrupt is cleared.

INTE[7]

The interrupt enable (INTE[7]) bit controls the assertion of the interrupt (INTB) output. When a logic 1 is written to INTE[7], the R8TDxI, DLL_RFCLKI, DLL_TFCLKI, RXANALOGI, TXANALOGI T8TexI or CSTRI pending interrupt will assert the interrupt (INTB) output (if GINTE is set to logic 1). When a logic 0 is written to INTE[6], the R8TDxI, DLL_RFCLKI, DLL_TFCLKI, RXANALOGI, TXANALOGI T8TexI or CSTRI pending interrupt will not assert the interrupt (INTB) output.

Register 0012H: S/UNI MULTI-48 Master Interrupt Status #8

Bit	Type	Function	Default
15	R/W	INTE[8]	0
14	—	Unused	X
13	—	Unused	X
12	—	Unused	X
11	R	DCRU155_622I[3]	X
10	R	DCRU155_622I[2]	X
9	R	DCRU155_622I[1]	X
8	R	DCRU155_622I[0]	X
7	R	JAT622I[3]	X
6	R	JAT622I[2]	X
5	R	JAT622I[1]	X
4	R	JAT622I[0]	X
3	—	Unused	X
2	R	LAS4x622I	X
1	R	TX2488I	X
0	R	RX2488I	X

The Interrupt Status Register is provided at r/w address 0011H.

RX2488I to DCRU155_622I[3:0]

The RX2488I to DCRU155_622I [3:0] are interrupt status indicators for the corresponding block. The interrupt status is set to logic 1 to indicate a pending interrupt from the corresponding block. The interrupt status bits are independent of the interrupt enable bit.

INTE[8]

The interrupt enable (INTE[8]) bit controls the activation of the interrupt (INTB) output. When a logic 1 is written to INTE[8], the RX2488I to DCRU155_622I [3:0] pending interrupt will assert the interrupt (INTB) output (if GINTE is set to logic 1). When a logic 0 is written to INTE[8], the RX2488I to DCRU155_622I [3:0] pending interrupt will not assert the interrupt (INTB) output.

Register 0013H: S/UNI MULTI-48 System Side Receive and Transmit Configuration

Bit	Type	Function	Default
15	R/W	SYS_TSTS12C[4]	0
14	R/W	SYS_TSTS12C[3]	0
13	R/W	SYS_TSTS12C[2]	0
12	R/W	SYS_TSTS12C[1]	0
11	R/W	SYS_TSTS12CSL[4]	0
10	R/W	SYS_TSTS12CSL[3]	0
9	R/W	SYS_TSTS12CSL[2]	0
8	R/W	SYS_TSTS12CSL[1]	0
7	R/W	SYS_RSTS12C[4]	0
6	R/W	SYS_RSTS12C[3]	0
5	R/W	SYS_RSTS12C[2]	0
4	R/W	SYS_RSTS12C[1]	0
3	R/W	SYS_RSTS12CSL[4]	0
2	R/W	SYS_RSTS12CSL[3]	0
1	R/W	SYS_RSTS12CSL[2]	0
0	R/W	SYS_RSTS12CSL[1]	0

SYS_RSTS12CSL[4:1]

The system receive STS-12 slave concatenation mode (SYS_RSTS12CSL[4:1]) bits enable the processing of a slave STS-12c (VC-4-4c) payload for the corresponding STS-12/STM-4 system slice. SYS_RSTS12CSL[4:1] should be written with “1110” for STS-48c (VC-4-16c) payload processing. For sub-STS-48c (VC-4-16c) payload types, SYS_RSTS12CSL[4:1] should be written with “0000”.

SYS_RSTS12C[4:1]

The system receive STS-12 concatenation mode (SYS_RSTS12C[4:1]) bits enable the processing of a master or slave STS-12c (VC-4-4c) payload for the corresponding STS-12/STM-4 system slice. SYS_RSTS12C[x] should be written with a logic 1 value when the system receive STS-12/STM-4 slice x processes part of an STS-48c (VC-4-16c) payload or an STS-12c (VC-4-4c) payload. SYS_RSTS12C[x] should be written with a logic 0 value when the system receive STS-12/STM-4 slice x processes sub-STS-12c (VC-4-4c) payload types.

SYS_TSTS12CSL[4:1]

The system transmit STS-12 slave concatenation mode (SYS_TSTS12CSL[4:1]) bits enable the processing of a slave STS-12c (VC-4-4c) payload for the corresponding STS-12/STM-4 system slice. SYS_TSTS12CSL[4:1] should be written with “1110” for STS-48c (VC-4-16c) payload processing. For sub-STS-48c (VC-4-16c) payload types, SYS_TSTS12CSL[4:1] should be written with “0000”.

SYS_TSTS12C[4:1]

The system transmit STS-12 concatenation mode (SYS_TSTS12C[4:1]) bits enable the processing of a master or slave STS-12c (VC-4-4c) payload for the corresponding STS-12/STM-4 slice. SYS_TSTS12C[x] should be written with a logic 1 value when the system transmit STS-12/STM-4 slice x processes part of an STS-48c (VC-4-16c) payload or an STS-12c (VC-4-4c) payload. SYS_TSTS12C[x] should be written with a logic 0 value when the system transmit STS-12/STM-4 slice x processes sub-STS-12c (VC-4-4c) payload types.

Register 0014H: S/UNI MULTI-48 General Purpose Configuration #2

Bit	Type	Function	Default
15	—	Unused	X
14	—	Unused	X
13	—	Unused	X
12	—	Unused	X
11	R/W	Reserved	0
10	R/W	Reserved	0
9	R/W	Reserved	0
8	R/W	Reserved	0
7	R/W	Reserved	0
6	R/W	Reserved	0
5	R/W	Reserved	0
4	R/W	Reserved	0
3	R/W	Reserved	0
2	R/W	Reserved	0
1	R/W	Reserved	0
0	R/W	Reserved	0

Register 0015H: S/UNI MULTI-48 APSIFP Enable and APS Input TelecomBus Synchronization Delay

Bit	Type	Function	Default
15	R	APS_TIP	X
14	R/W	APSIFP_EN	0
13	R/W	AIJ0DLY[13]	0
12	R/W	AIJ0DLY[12]	0
11	R/W	AIJ0DLY[11]	0
10	R/W	AIJ0DLY[10]	0
9	R/W	AIJ0DLY[9]	0
8	R/W	AIJ0DLY[8]	0
7	R/W	AIJ0DLY[7]	0
6	R/W	AIJ0DLY[6]	0
5	R/W	AIJ0DLY[5]	0
4	R/W	AIJ0DLY[4]	0
3	R/W	AIJ0DLY[3]	0
2	R/W	AIJ0DLY[2]	0
1	R/W	AIJ0DLY[1]	0
0	R/W	AIJ0DLY[0]	0

AIJ0DLY[13:0]

The APS Input transport frame delay bits (AIJ0FP[13:0]) control the delay, in internal SYSCLK cycles, inserted by the S/UNI MULTI-48 before processing the J0 characters delivered by the APS Input serial data links (APSI_P/ APSI_N[4:1]). AIJ0DLY is set such that after the specified delay, all active APS Input links would have delivered the J0 character. The relationships of AIJ0FP, AIJ0DLY[13:0] and the system configuration are described in the Functional Timing section.

Valid values of AIJ0DLY[13:0] are 0000H to 25F7H.

APSIFP_EN

The APS input frame pulse (APSIFP_EN) enables the use of the APSIFP input. When APSIFP_EN is logic 1, the input APS port uses the APSIFP input as a frame pulse and the APS port can use any framing method. When APSIFP_EN is logic 0, the input APS port ignores the APSIFP input and the APS port uses the “SMART” framing algorithm. See Operation section for more details.

APS_TIP

The APS transfer in progress bit (APS_TIP) indicates that S/UNI MULTI-48 Smart Framing Configuration is going to be updated. APS_TIP is asserted when a write access is done to Register 0019H and remains high until the APSFP2J0DLY register bits are updated.

Register 0016H: S/UNI MULTI-48 APS Output TelecomBus Synchronization Delay

Bit	Type	Function	Default
15	R/W	SYSCLK_EN	0
14	R/W	AOJ0DLY_EN	0
13	R/W	AOJ0DLY[13]	0
12	R/W	AOJ0DLY[12]	0
11	R/W	AOJ0DLY[11]	0
10	R/W	AOJ0DLY[10]	0
9	R/W	AOJ0DLY[9]	0
8	R/W	AOJ0DLY[8]	0
7	R/W	AOJ0DLY[7]	0
6	R/W	AOJ0DLY[6]	0
5	R/W	AOJ0DLY[5]	0
4	R/W	AOJ0DLY[4]	0
3	R/W	AOJ0DLY[3]	0
2	R/W	AOJ0DLY[2]	0
1	R/W	AOJ0DLY[1]	0
0	R/W	AOJ0DLY[0]	0

AOJ0DLY[13:0]

The APS Output transport frame delay bits (AOJ0DLY[13:0]) control the delay, in internal SYSCLK cycles, inserted by the S/UNI MULTI-48 between receiving a reference J0 frame pulse on APSIFP, and presenting the outgoing J0 transmit frame pulse on APSOFP and APSO_P[4:1]/APSO_N[4:1]. AOJ0DLY is set such that after the specified delay, APSO_P[4:1]/APSO_N[4:1] will have the J0 frame pulse on it. The relationships bwteen APSIFP, AOJ0DLY[13:0] and the system configuration are described in the Functional Timing section.

Valid values of AOJ0DLY[13:0] are 0000H to 25F7H.

AOJ0DLY_EN

The APS Output transport frame delay enable bit (AOJ0DLY_EN) enables the use of the AOJ0DLY[13:0] delay. When AOJ0DLY_EN is set to logic 1, the APSOFP output is a delayed version of APSIFP. When AOJ0DLY_EN is set to logic 0, the APSOPFP is synchronised with R8TD J0 indication output. Whenever one or more links of the S/UNI MULTI-48 are configured to use APS ports to interface with the PL3/UL3 sub-system, AOJ0DLY_EN must be set to logic 0 to align all frames for the PL3/UL3 sub-system. When APS ports are used only to interface with the SONET sub-system, AOJ0DLY_EN must be set to logic 1. In a working/protect setup, AOJ0DLY_EN must be set to logic 0 for the working device. AOJ0DLY_EN must be set to logic 1 in the protect device.

SYSCLK_EN

The SYSCLK_EN register bit enables the use of the SYSCLK input. When SYSCLK_EN is logic 1, then SYSCLK input is used to sample APSIFP and to clock the system side of the S/UNI MULTI-48. When SYSCLK_EN is logic 0, REFCLK155/77_P/N is used to generate the system side clock of the S/UNI MULTI-48. The APS ports can still be used, with APSIFP's rsing edge being detected. APSIFP input remains optional in all cases.

Note: SYSCLK must be enabled (SYSCLK_EN set to logic 1) in order to use the APS port when the S/UNI MULTI-48 is configured in STS-48 (STM-16) looptime mode. This restriction does not apply to STS-12 (STM-4) and STS-3 (STM-1) configurations.

Register 0017H: S/UNI MULTI-48 Rx APS J0 FIFO Interrupt Enable

Bit	Type	Function	Default
15	R/W	NOJ04E	0
14	R/W	NOJ03E	0
13	R/W	NOJ02E	0
12	R/W	NOJ01E	0
11	R/W	Reserved	0
10	R/W	Reserved	0
9	R/W	EXJ04E	0
8	R/W	EXJ03E	0
7	R/W	EXJ02E	0
6	R/W	EXJ01E	0
5	R/W	Reserved	0
4	R/W	Reserved	0
3	R/W	OKJ04E	0
2	R/W	OKJ03E	0
1	R/W	OKJ02E	0
0	R/W	OKJ01E	0

OKJ0*x*E

The APS correct J0 indication interrupt enable bit (OKJ0*x*E) for APS link number *x* enables the assertion of a hardware interrupt on INTB when the corresponding APS link's J0 character is detected at the expected time. When OKJ0*x*E is logic 1, the hardware interrupt is enabled for APS link number *x*. When OKJ0*x*E is logic 0, the hardware interrupt is disabled for APS link number *x*.

EXJ0*x*E

The APS extra J0 indication interrupt enable bit (EXJ0*x*E) for APS link number *x* enables the assertion of a hardware interrupt on INTB when the corresponding APS link's J0 character is detected at an unexpected time. When EXJ0*x*E is logic 1, the hardware interrupt is enabled for APS link number *x*. When EXJ0*x*E is logic 0, the hardware interrupt is disabled for APS link number *x*.

NOJ0*x*E

The APS J0 absent indication interrupt enable bit (NOJ0*x*E) for APS link number *x* enables the assertion of a hardware interrupt on INTB when the corresponding APS link's J0 character is not detected at an unexpected time. When NOJ0*x*E is logic 1, the hardware interrupt is enabled for APS link number *x*. When NOJ0*x*E is logic 0, the hardware interrupt is disabled for APS link number *x*.

Register 0018H: S/UNI MULTI-48 Rx APS J0 FIFO Interrupt Status

Bit	Type	Function	Default
15	R	NOJ04I	X
14	R	NOJ03I	X
13	R	NOJ02I	X
12	R	NOJ01I	X
11	—	Unused	X
10	—	Unused	X
9	R	EXJ04I	X
8	R	EXJ03I	X
7	R	EXJ02I	X
6	R	EXJ01I	X
5	—	Unused	X
4	—	Unused	X
3	R	OKJ04I	X
2	R	OKJ03I	X
1	R	OKJ02I	X
0	R	OKJ01I	X

OKJ0*x*I

The APS correct J0 indication interrupt indication bit (OKJ0*x*I) for APS link number *x* shows when the corresponding APS link's J0 character is detected at the expected time. When a correct J0 is detected, OKJ0*x*I is set to logic 1. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read.

EXJ0*x*I

The APS extra J0 indication interrupt indication bit (EXJ0*x*I) for APS link number *x* shows when an unexpected J0 character is detected on the corresponding APS link. When an unexpected J0 is detected, EXJ0*x*I is set to logic 1. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read.

NOJ0*x*I

The APS absent J0 indication interrupt indication bit (NOJ0*x*I) for APS link number *x* shows when the corresponding APS link's J0 character is not detected at the expected time. When the expected J0 is not detected, NOJ0*x*I is set to logic 1. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read.

Register 0019H: S/UNI MULTI-48 APS SMART Framing Configuration

Bit	Type	Function	Default
15	R/W	APSLINKSEL[1]	0
14	R/W	APSLINKSEL[0]	0
13	R	APSFP2J0DLY[13]	X
12	R	APSFP2J0DLY[12]	X
11	R	APSFP2J0DLY[11]	X
10	R	APSFP2J0DLY[10]	X
9	R	APSFP2J0DLY[9]	X
8	R	APSFP2J0DLY[8]	X
7	R	APSFP2J0DLY[7]	X
6	R	APSFP2J0DLY[6]	X
5	R	APSFP2J0DLY[5]	X
4	R	APSFP2J0DLY[4]	X
3	R	APSFP2J0DLY[3]	X
2	R	APSFP2J0DLY[2]	X
1	R	APSFP2J0DLY[1]	X
0	R	APSFP2J0DLY[0]	X

Any write access to this register will assert APS_TIP bit (register 0015H) and trigger an access to APS frame pulse to J0 delay counters.

APSFP2J0DLY[13:0]

The frame pulse to J0 delay bits (APSFP2J0DLY[13:0]) indicate the number of clock cycles between the frame pulse provided by the internal frame counter and the J0 indication output of the selected R8TD. The R8TD is selected by the APSLINKSEL[1:0] register bits. The APSFP2J0DLY[13:0] bits are used by the APS "SMART" framing algorithm (see Operation section for more detail).

APSLINKSEL[1:0]

The APS link bits (APSLINKSEL[1:0]) select the link that is used in the calculation of APSFP2J0DLY[13:0]. Any write to these bits will assert the APS_TIP bit (register 0015H: S/UNI MULTI-48 APSIFP Enable and APS Input TelecomBus Synchronization Delay) and force the calculation of the frame pulse to J0 delay (APSFP2J0DLY) for the given link. The APSLINKSEL[1:0] bits are used by the APS "SMART" framing algorithm (see Operation section for more detail). **Note** that these bits should not be written with a value referring to an unused APS link. Any APSFP2J0DLY calculation trial for a link that is not receiving J0 codes will result in a hanging APS_TIP bit.

Register 001AH: S/UNI MULTI-48 Miscellaneous Defect Configuration #1

Bit	Type	Function	Default
15	—	Unused	X
14	R/W	Reserved	1
13	R/W	RXAPS_LINK_PAIS	1
12	R/W	Reserved	1
11	—	Unused	X
10	—	Unused	X
9	—	Unused	X
8	R/W	Reserved	0
7	R	Reserved	X
6	R/W	Reserved	0
5	R	Reserved	X
4	—	Unused	X
3	R/W	Reserved	0
2	R/W	Reserved	0
1	R/W	Reserved	0
0	R/W	Reserved	0

RXAPS_LINK_PAIS

The RXAPS_LINK_PAIS is used to configure the four Rx APS link AIS indications as 4 separate STS-12/STM-4 channel or as one STS-48/STM-16 channel. When RXAPS_LINK_PAIS is set to logic 1, the 4 APS links are treated as one STS-48/STM-16 channel. If any one of the APS links loses J0 alignment or character alignment (OFA detected in R8TD), then data from all four links will be forced to AIS-P state. When RXAPS_LINK_PAIS is set to logic 0, the 4 APS links are treated separately.

Note that RXAPS_LINK_PAIS is only meaningful when OFAAIS is set to logic 1 (Register 0280H 0680H 0A80H 0E80H: R8TD APS Control and Status) . In this case, RXAPS_LINK_PAIS should be set to logic 1 when processing STS-48c (VC-4-16c) payload. In all other cases, RXAPS_LINK_PAIS should be set to logic 0.

Register 001BH: S/UNI MULTI-48 Miscellaneous Defect Configuration #2

Bit	Type	Function	Default
15	R/W	DOOL_DEFECT_EN [4]	0
14	R/W	DOOL_DEFECT_EN [3]	0
13	R/W	DOOL_DEFECT_EN[2]	0
12	R/W	DOOL_DEFECT_EN[1]	0
11	R/W	LOS_DEFECT_EN[4]	1
10	R/W	LOS_DEFECT_EN[3]	1
9	R/W	LOS_DEFECT_EN[2]	1
8	R/W	LOS_DEFECT_EN[1]	1
7	R/W	SD_DEFECT_EN [4]	1
6	R/W	SD_DEFECT_EN [3]	1
5	R/W	SD_DEFECT_EN [2]	1
4	R/W	SD_DEFECT_EN [1]	1
3	—	Unused	X
2	R/W	DOOL_DEFECT_EN	0
1	R/W	LOS_DEFECT_EN	1
0	R/W	SD_DEFECT_EN	1

SD_DEFECT_EN

The SD_DEFECT_EN bit is used to force an AIS-L on the internal datapath immediately when SD is deasserted (after programmable inversion in wrapper) for 1x2488 mode. This will prevent the internal framer's (RRMP) descrambler from producing a scrambled all 0's pattern which, when passed through a transmitter's scrambler will generate the all 0's pattern again. An extended all 0's pattern at the transmitter could potentially cause a loss of lock a the downstream receiver. This bit should be set to logic 0 in quad STS-12/STS-3 (STM-4/STM-1) mode.

LOS_DEFECT_EN

The LOS_DEFECT_EN bit is used to force an AIS-L on the internal datapath immediately when an LOS is detected for 1x2488 mode. This will prevent the internal framer's (RRMP) descrambler from producing a scrambled all 0's pattern which, when passed through a transmitter's scrambler will generate the all 0's pattern again. An extended all 0's pattern at the transmitter could potentially cause a loss of lock a the downstream receiver. This bit should be set to logic 0 in quad STS-12/STS-3 (STM-4/STM-1) mode.

DOOL_DEFECT_EN

The DOOL_DEFECT_EN bit is used to force an AIS-L on the internal datapath immediately when an DOOL is detected for 1x2488 mode. This will prevent the internal framer's (RRMP) descrambler from producing a scrambled all 0's pattern which, when passed through a transmitter's scrambler will generate the all 0's pattern again. An extended all 0's pattern at the transmitter could potentially cause a loss of lock a the downstream receiver. This bit should be set to logic 0 in quad STS-12/STS-3 (STM-4/STM-1) mode.

SD_DEFECT_EN[4:1]

The SD_DEFECT_EN[x] bit is used to force an AIS-L on the internal datapath of channel x immediately when SD is deasserted (after programmable inversion in wrapper) for STS-12 (STM-4) mode only. This will prevent the internal framer's (RRMP) descrambler from producing a scrambled all 0's pattern which, when passed through a transmitter's scrambler will generate the all 0's pattern again. An extended all 0's pattern at the transmitter could potentially cause a loss of lock a the downstream receiver. This bit should be set to logic 0 in STS-48 (STM-16) and STS-3 (STM-1) mode.

LOS_DEFECT_EN[4:1]

The LOS_DEFECT_EN[x] bit is used to force an AIS-L on the internal datapath of channel x immediately when an LOS is detected for STS-12 (STM-4) mode OR when an LOT (combination of LOS and SD) is detected for STS-3 (STM-1) mode. This will prevent the internal framer's (RRMP) descrambler from producing a scrambled all 0's pattern which, when passed through a transmitter's scrambler will generate the all 0's pattern again. An extended all 0's pattern at the transmitter could potentially cause a loss of lock a the downstream receiver. This bit should be set to logic 0 in STS-48 (STM-16) mode.

DOOL_DEFECT_EN[4:1]

The DOOL_DEFECT_EN[x] bit is used to force an AIS-L on the internal datapath of channel x immediately when an DOOL is detected for STS-12 (STM-4) mode only. This will prevent the internal framer's (RRMP) descrambler from producing a scrambled all 0's pattern which, when passed through a transmitter's scrambler will generate the all 0's pattern again. An extended all 0's pattern at the transmitter could potentially cause a loss of lock a the downstream receiver. This bit should be set to logic 0 in STS-48 (STM-16) and STS-3 (STM-1) mode.

Register 001CH: S/UNI MULTI-48 Miscellaneous Defect Configuration #3

Bit	Type	Function	Default
15	R/W	STS48ENB	0
14	—	Unused	X
13	—	Unused	X
12	—	Unused	X
11	—	Unused	X
10	R/W	Reserved	X
9	R/W	CELL_RESET[4]	0
8	R/W	CELL_RESET[3]	0
7	R/W	CELL_RESET[2]	0
6	R/W	CELL_RESET[1]	0
5	R/W	SYS_RESET	0
4	R/W	SYS_EN	1
3	R/W	SONET_EN[4]	1
2	R/W	SONET_EN[3]	1
1	R/W	SONET_EN[2]	1
0	R/W	SONET_EN[1]	1

SONET_EN[4:1]

The SONET processing bits (SONET_EN[4:1]) enable the use of the SONET/SDH sub-system. When SONET_EN[X] is set to logic 1, the corresponding receive and transmit SONET/SDH sub-systems (RRMP, RTTP section, SBER, RHPP, RTTP path, SVCAs, TRMP and TTTP section) are enabled. When SONET_EN[X] is set to logic 0, the clock of the corresponding receive and transmit SONET/SDH sub-systems are killed.

SYS_EN

The system processing bits (SYS_EN) enable the use of the UL3/PL3 sub-system. When SYS_EN is set to logic 1, the receive and transmit UL3/PL3 sub-systems are enabled. When SYS_EN is set to logic 0, the clock of the receive and transmit UL3/PL3 sub-systems are killed. Affected blocks are: RXSDQ, TXSDQ, TSTSI, TCAS12, TCFP, TTDP. Unaffected blocks are: RSTSI, RCAS12, RCFP, RTDP.

SYS_RESET

The system global reset bit (SYS_RESET) holds the UL3/PL3 sub-system (RSTSI, RCAS12, RCFP, RTDP, RXSDQ, RXPHY, TSTSI, TCAS12, TCFP, TTDP, TXSDQ, TXPHY) in reset. When SYS_RESET is set to logic 1, the UL3/PL3 sub-system is held in reset. When SYS_RESET is set to logic 0, the UL3/PL3 sub-system works normally. When used, SYS_RESET should be asserted for at least 100 ns to reset circuitry properly.

CELL_RESET[4:1]

The cell reset bits (CELL_RESET[4:1]) hold the cell processors (TCAS12, TTDP, TCFP, RCAS12, RTDP, RCFP) of the UL3/PL3 sub-system in reset. When CELL_RESET[X] is set to logic 1, the cell processors from slice X are held in reset. When CELL_RESET[X] is set to logic 0, the cell processors from slice X work normally. When used, CELL_RESET[X] should be asserted for at least 100 ns to reset circuitry properly.

STS48ENB

The STS48EN input pin inverter bit (STS48ENB) changes the logic of the STS48EN input pin. When STS48ENB is set to logic 0, the single mode is active when the STS48EN input pin is set to logic 1. When STS48ENB is set to logic 1, the single mode is active when the STS48EN input pin is set to logic 0.

Register 001DH: S/UNI MULTI-48 Miscellaneous Defect Configuration #4

Bit	Type	Function	Default
15	—	Unused	X
14	—	Unused	X
13	—	Unused	X
12	R/W	Reserved	0
11	R/W	Reserved	0
10	R/W	Reserved	0
9	R/W	Reserved	0
8	R/W	Reserved	0
7	R/W	Reserved	0
6	R/W	Reserved	0
5	R/W	Reserved	0
4	R/W	Reserved	0
3	R/W	DCRU155_622EN[4]	0
2	R/W	DCRU155_622EN[3]	0
1	R/W	DCRU155_622EN[2]	0
0	R/W	DCRU155_622EN[1]	0

DCRU155_622EN[4:1]

The DCRU155_622 enable bits (DCRU155_622EN[4:1]) force the use of the corresponding DCRU155_622 and SFBA blocks. When DCRU155_622EN[x] is set to logic 1, receive line channel x will use the DCRU155_622 to recover the receive clock and data and SFBA for SONET/SDH framing. When DCRU155_622EN[x] is set to logic 0, receive line channel x will not use the DCRU155_622 nor SFBA. It will rather use the 2488/622 analog blocks to recover the receive clock and data and SRLI block for SONET/SDH framing. Note that DCRU155_622EN[x] must be set to logic 1 when line channel x is in STS-3/STM-1 mode, and to logic 0 when line channel x is in STS-12/STM-4 mode. DCRU155_622EN[4:1] should be set to all zeros in STS-48/STM-16 mode.

Register 001EH: S/UNI MULTI-48 Free Register

Bit	Type	Function	Default
15:0	R/W	FREE[15:0]	0

FREE[15:0]

These are general-purpose read/write register bits. These do not affect the operation of the device in any way but will hold a value written to them.

Register 0020H: Rx2488 Analog Interrupt Status

Bit	Type	Function	Default
Bit 15	R	CRU_CLOCK	X
Bit 14	R	Reserved	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R	PRBS_SYNC_I	X
Bit 4	R	PRBS_ERR_I	X
Bit 3	R	Reserved	X
Bit 2	R	LOS_I	X
Bit 1	R	DOOL_I	X
Bit 0	R	ROOL_I	X

ROOL_I

The recovered reference out of lock status indicates that the clock recovery phase locked loop is unable to lock to the reference clock on REFCLK155. At startup, ROOL_I may remain at logic 1 for several hundred milliseconds while the PLL obtains lock. If WCIMODE is logic 1, only over-writing with a '1' clears this bit. If WCIMODE is logic 0, then a read of this register automatically clears the bit.

DOOL_I

The recovered data out of lock status indicates that the clock recovery phase locked loop is unable to recover and lock to the input data stream. DOOL_I is a logic one if the divided down recovered clock frequency is not within ±1000 ppm of the REFCLK155 frequency or if no transitions have occurred on the RXD input for more than LOS_COUNT[4:0] bits. Note: recall that LOS_COUNT is specified as the upper 5 bits of a 9 bit number and has an accuracy of ±15. If WCIMODE is logic 1, only over-writing with a '1' clears this bit. If WCIMODE is logic 0, then a read of this register automatically clears the bit.

If the optical signal is lost, the SD[1] input pin should be deasserted. This will cause the CRU into training mode where it will lock onto the REFCLK155 input. However, the state-machine which controls DOOL_I will continue to search for lock to data and is expected to toggle during this time. When the optical signal is restored and the SD[1] input pin is asserted, the CRU will once again attempt to lock onto the data signal. Once lock is found, DOOL_I will stop toggling and DOOLV can be examined to verify the CRU is in fact locked to the data.

Note: The DOOL detection accuracy is affected by jitter on the recovered clock. As a result, the clock skew needed to declare DOOL could exceed +/- 999 ppm.

LOS_I

The loss of signal status indicates that the receive signal has exceeded a maximum number of consecutive ones or zeros. LOS_I is a logic zero if the SD[1] input is high or less than LOS_COUNT consecutive ones or zeros have been received. LOS_I is a logic one if the SD[1] input is low or LOS_COUNT consecutive ones or zeros have been received. Note: recall that LOS_COUNT is specified as the upper 5 bits of a 9 bit number and has an accuracy of ±15. If WCIMODE is logic 1, only over-writing with a '1' clears this bit. If WCIMODE is logic 0, then a read of this register automatically clears the bit.

PRBS_ERR_I

The PRBS Bit Error bit provides a status indication that a bit error has been detected in the comparison between the incoming data and the locally generated data. The PRBS_ERR_I is set high when the monitor is in the synchronized state and when an error in a PRBS word is detected. If WCIMODE is logic 1, only over-writing with a '1' clears this bit. If WCIMODE is logic 0, then a read of this register automatically clears the bit.

PRBS_SYNC_I

The PRBS Synchronization bit indicates that a change in the status of the PRBS Monitor has occurred. The comparison between the incoming data and the internal PRBS^23 pattern is generated locally. The PRBS_SYNC_I is set high when the monitor is in the synchronized state and has received two consecutive errored words forcing the PRBS monitor to resynchronize. If WCIMODE is logic 1, only over-writing with a '1' clears this bit. If WCIMODE is logic 0, then a read of this register automatically clears the bit.

CRU_CLOCK

The CRU_CLOCK status bit monitors the state of the CRU clock. Each time this Register is read, the sampling register is reset. The CRU_CLOCK is set high when the CRU clock transitions from low to high at least once. The CRU_CLOCK is reset low after Register 00H is read and will remain low if no transitions occur on the CRU clock.

Register 0021H: Rx2488 Analog Interrupt Control

Bit	Type	Function	Default
Bit 15	R/W	SD_DISABLE_2488	0
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	PRBS_SYNC_EN	0
Bit 4	R/W	PRBS_ERR_EN	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	LOS_EN	0
Bit 1	R/W	DOOL_EN	0
Bit 0	R/W	ROOL_EN	0

ROOL_EN

The Reference Out Of Lock Enable bit connects the ROOL_I status bit to the INT pin of the RX2488 block. When ROOL_EN is set to logic one, an interrupt on the INT pin is generated upon assertion of the ROOL_I register bit. When ROOL_EN is set low, a change in the ROOL_I status does not generate an interrupt.

DOOL_EN

The Data Out Of Lock Enable bit connects the DOOL_I status bit to the INT pin of the RX2488 block. When DOOL_EN is set to logic one, an interrupt on the INT is generated upon assertion of the DOOL_I register bit. When DOOL_EN is set low, a change in the DOOL_I status does not generate an interrupt.

Note: The DOOL detection accuracy is affected by jitter on the recovered clock. As a result, the clock skew needed to declare DOOL could exceed +/- 999 ppm.

LOS_EN

The Loss of Signal Enable bit connects the LOS_I status bit to the INT pin of the RX2488 block. When LOS_EN is set to logic one, an interrupt on the INT is generated upon assertion of the LOS_I register bit. When LOS_EN is set low, a change in the LOS_I status does not generate an interrupt.

PRBS_ERR_EN

The PRBS Error Enable bit connects the PRBS_ERR_I status bit to the INT pin of the RX2488 block. When PRBS_ERR_EN is set to logic one, an interrupt on the INT is generated upon assertion of the PRBS_ERR_I register bit. When PRBS_ERR_EN is set low, a change in the PRBS_ERR_I status does not generate an interrupt.

PRBS_SYNC_EN

The PRBS Synchronized Enable bit connects the PRBS_SYNC_I status bit to the INT pin of the RX2488 block. When PRBS_SYNC_EN is set to logic one, an interrupt on the INT is generated upon assertion of the PRBS_SYNC_I register bit. When PRBS_SYNC_EN is set low, a change in the PRBS_SYNC_I status does not generate an interrupt.

SD_DISABLE_2488

The Signal Detect Disable bit controls the operation of the SD[1] input pin in 2488 mode. When SD_DISABLE_2488 is set to a logic one the SD[1] input will be ignored and the internal signal will be forced to the active state and all down stream blocks will operate normally. When SD_DISABLE_2488 is set to logic zero the internal signal follows the state of the SD[1] input pin and the state of SDI_INV_2488 bit.

Register 0022H: Rx2488 Analog CRU Control

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	CRU_RESET	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	RX2488_ENABLE	1
Bit 11	R/W	CRU_ENABLE	1
Bit 10	R/W	LOCK_TO_REF	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	SLICE1_RX622_EN	0
Bit 7	R/W	SDLE2488	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	1
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	1
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

SDLE2488

The Serial Diagnostic Loopback Enable (SDLE2488) bit, when set to '1', loops the data from the transmit line PISO to the receive side CRU/SIPO. In the loopback mode, the CRU locks to the loopback data.

SLICE1_RX622_EN

Rx 622/155 Slice #1 enable. The SLICE1_RX622_EN bits controls the receive link #1 ports using RXD1_P/N. This bit must be set to logic 1 when S/UNI MULTI-48 is in quad 622/155 mode. This bit must be set to logic 0 when S/UNI MULTI-48 is in single 2488 mode. Note that RX2488_ENABLE must also be set to logic 1 when SLICE1_RX622_EN is set logic 1.

LOCK_TO_REF

The Lock to Reference bit controls the operation of the CRU state machine. When LOCK_TO_REF is set to logic one the CRU state machine will hold the CRU in the Lock-to-Reference state. When the CRU is reset to logic zero the CRU state machine operates normally.

CRU_ENABLE

The Clock Recovery Unit Enable bit provides a global power down of the CRU Analog Block Circuit. When set to ‘0’, this bit forces the CRU to a low power state and functionality is disabled. When set to ‘1’, the CRU operates in the normal mode of operation.

RX2488_ENABLE

The 2.488GHz Receiver Enable bit provides a global power down of the RX2488 Analog Block Circuit. When set to ‘0’, this bit forces the RX2488 to a low power state and functionality is disabled. When set to ‘1’, the RX2488 operates in the normal mode of operation.

CRU_RESET

The Clock Recovery Unit Reset bit provides a complete reset of the CRU Analog Block Circuit. When set to ‘1’, this bit forces the CRU to a known initial state. While the bit is set to ‘1’, the functionality of the block is disabled. When set to ‘0’, the CRU operates in the normal mode. This bit is not self-clearing. Therefore a ‘0’ must be written to the bit to remove the reset condition. When used, CRU_RESET should be asserted for at least 100 us to reset circuitry properly.

Register 0023H: Rx2488 Analog CRU Clock Training Configuration and Status

Bit	Type	Function	Default
Bit 15	R/W	LOS_COUNT[4]	0
Bit 14	R/W	LOS_COUNT[3]	1
Bit 13	R/W	LOS_COUNT[2]	0
Bit 12	R/W	LOS_COUNT[1]	0
Bit 11	R/W	LOS_COUNT[0]	0
Bit 10	R/W	LOSEN	1
Bit 9	R/W	LINE_LOOP_BACK	0
Bit 8	R/W	SDI_INV_2488	0
Bit 7	R/W	INV_DATA	0
Bit 6	R	DOOLV	X
Bit 5	R	ROOLV	X
Bit 4	R	TRAIN	X
Bit 3	R/W	Reserved	1
Bit 2	R/W	Reserved	1
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

TRAIN

The CRU reference training status indicates if the CRU is locking to the reference clock or the locking to the receive data. TRAIN is a logic zero if the CRU is locking or locked to the reference clock. TRAIN is a logic one if the CRU is locking or locked to the receive data. TRAIN is invalid if the CRU is not used.

When the optical signal is lost, the SD[1] input pin is expected to be deasserted. In this state, the CRU will be forced into training mode and will lock to REFCLK155. However, the state-machine which controls the TRAIN register bit will continue looking at the data and will occasionally change states. However, the CRU will remain locked to REFCLK155 until SD[1] is once again asserted.

ROOLV

The recovered reference out of lock status indicates that the clock recovery phase locked loop is unable to lock to the reference clock on REFCLK155. At startup, ROOLV may remain at logic 1 for several hundred milliseconds while the PLL obtains lock.

DOOLV

The recovered data out of lock status indicates that the clock recovery phase locked loop is unable to recover and lock to the input data stream. DOOLV is logic one if the divided down recovered clock frequency is not within approximately 488ppm of the REFCLK155 frequency or if LOS_I interrupt has been triggered.

Note: The DOOL detection accuracy is affected by jitter on the recovered clock. As a result, the clock skew needed to declare DOOL could exceed +/- 999 ppm.

INV_DATA

The Serial Data Inversion INV_DATA controls the polarity of the received data. When INV_DATA is set to '1', the polarity of the RXD_P/RXD_N input pins invert. When INV_DATA is set to '0', the RXD_P/RXD_N inputs operate normally.

SDI_INV_2488

The Signal Detect Inversion SDI_INV_2488 controls the polarity of the SD[1] input pin in 2488 mode. When SDI_INV_2488 is set to '1' the polarity of the SD[1] input pin is inverted. When SDI_INV_2488 is set to '0' the polarity of the SD[1] input remains unchanged.

LINE_LOOP_BACK

The line loop back bit selects the source of the timing for the parallel data output of the receive FIFO. When the LINE_LOOP_BACK is set to logic one, the output data of this FIFO is timed to the clock of the S/UNI MULTI-48 transmitter. Either the S/UNI MULTI-48 or the upstream device must be in loop-timed mode for the line-loopback mode to work properly. When reset to logic zero, the receive FIFO output data is timed using either the receive-side-CSU clock or the CRU clock depending on the state of the FIFO_CLOCK Register bit.

For chip-level line loopback in 2488 mode, this LINE_LOOP_BACK bit and the SLLE2488 register bit in the Tx2488 Analog Control/Status register (register 1020H) must be set to logic 1. As well, the LOOPTIMEB and CSU_MODE[3] register bits in the Tx2488 ABC Control register (register 1021H) must be set to logic 0.

LOSEN

The loss of signal enable bit controls the signal detection logic. The CRU uses the LOS detector along with the clock difference detector to determine if the CRU is locked to data. When LOSEN is set to logic one, the incoming signal is monitored for 1/0 transitions as determined by LOS_COUNT[4:0] register bits. If LOSEN is reset to logic zero, the 1/0 transition detector is disabled. Note: recall that LOS_COUNT is specified as the upper 5 bits of an 11 bit number and has an accuracy of ±15.

LOS_COUNT[4:0]

The Loss of Signal 1's/0's transition detector count field sets the value for the number of consecutive all-zeros or all-ones pattern that will force the CRU out of the LOCK TO DATA state. Each bit in the binary count represents sixteen ones or zeros in the pattern. (i.e. LOS_COUNT has an accuracy of ±15). For example, to set the consecutive all-ones or all-zeros pattern to 128 the LOS_COUNT should be set to "01000"b. The default value for this field is 128.

Register 0024H: Rx2488 Analog PRBS Control

Bit	Type	Function	Default
Bit 15	R	PRBS_ERR_CNT[7]	X
Bit 14	R	PRBS_ERR_CNT[6]	X
Bit 13	R	PRBS_ERR_CNT[5]	X
Bit 12	R	PRBS_ERR_CNT[4]	X
Bit 11	R	PRBS_ERR_CNT[3]	X
Bit 10	R	PRBS_ERR_CNT[2]	X
Bit 9	R	PRBS_ERR_CNT[1]	X
Bit 8	R	PRBS_ERR_CNT[0]	X
Bit 7	R/W	CLEAR_ERR_CNT	0
Bit 6	—	Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R	SYNC_STAT	X
Bit 2	R/W	Reserved	0
Bit 1	R/W	PRBS_ENABLE	0
Bit 0	—	Unused	X

PRBS_ENABLE

This bit enables the PRBS monitor of the RX2488 block. When low, the PRBS monitor is disabled. When high, the PRBS monitor is enabled and will check the incoming data stream for errors.

SYNC_STAT

The Monitor Synchronization Status bit reflects the state of the monitor's state machine. When SYNC_STAT is set low, the monitor has lost synchronization. When SYNC_STAT is high, the monitor is in synchronization.

CLEAR_ERR_CNT

The Clear Error Count bit clears the PRBS word error count value. When a logic 1 is written to this bit, the PRBS word error count register is reset to zero. When set to logic 0, the counter operates normally. This bit should be written to 1 then written 0 to perform the clear counter operation.

PRBS_ERR_CNT[7:0]

The ERR_CNT[7:0] register is the number of errors in the PRBS bytes detected during the monitoring. Errors are accumulated only when the monitor is in the synchronized state. Even if there are multiple errors within one PRBS byte, only one error is counted. The transfer of the error counter to this holding register is triggered by writing any value in the CLEAR_ERR_CNT bit. Note that it is not triggered when writing to register 0002H, the Global Performance Monitor Update Register, nor does it assert the global TIP bit in the same register. PRBS_ERR_CNT[7:0] is cleared by the CLEAR_ERR_CNT bit in this register. The actual PRBS error counter is cleared immediately after and during the whole time a logic 1 is written to the CLEAR_ERR_CNT bit. The error counter will not wrap around after reaching FFh. The error counter will saturate to FFh.

Register 0030H: Quad 622 Rx MABC General Control Register

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	Reserved	1
Bit 4	R/W	Reserved	1
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	MABC_ENB	0

MABC_ENB

The global enable control register bit MABC_ENB disables the entire 4x622MABC into low-power mode when set to '1'. When MABC_ENB set to '0', and device is in quad 622/155 mode, the MABC will be in normal operation. There is not need to set MABC_ENB to logic 1 when the device is in 2488 mode in order to save power since it is done automatically.

Register 0031H: Quad 622 Rx MABC Control Register

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	1
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	1
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	1
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	1
Bit 3	R/W	Reserved	1
Bit 2	R/W	Reserved	1
Bit 1	R/W	Reserved0	1
Bit 0	R/W	CSUR_ARSTB	1

CSUR_ARSTB

The register bit CSUR_ARSTB provides a reset to the entire CSUR (Master and Slave PLL). When asserted (= '0'), it resets the entire CSUR. CSUR_ARSTB has to be asserted for at least 106 us to reset the CSUR. When deasserted (= '1'), the CSUR is set to normal operation.

Reserved0

The Reserved0 bits must be set to logic 0 for proper operation.

Reserved

The Reserved bits must be set to their default value for proper operation.

Register 0033H: Quad 622 Rx MABC Interrupt Enable Register

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	R	CSUR_MRAV	X
Bit 9	R	CSUR_SRAV	X
Bit 8	R	Reserved	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	CSUR_MRAI_EN	0
Bit 1	R/W	CSUR_SRAI_EN	0
Bit 0	R/W	CSUR_LDI_EN	0

CSUR_LDI_EN

Register bit CSUR_LDI_EN is used as interrupt enable for CSUR_LDI register bit. It connects the CSUR_LDI status bit to the INT pin of the LAS4x622 block. When CSUR_LDI_EN is set to logic one, an interrupt on the INT is generated upon assertion of the CSUR_LDI register bit. When CSUR_LDI_EN is set low, a change in the CSUR_LDI status does not generate an interrupt.

CSUR_SRAI_EN

Register bit CSUR_SRAI_EN is used as interrupt enable for CSUR_SRAI register bit. It connects the CSUR_SRAI status bit to the INT pin of the LAS4x622 block. When CSUR_SRAI_EN is set to logic one, an interrupt on the INT is generated upon assertion of the CSUR_SRAI register bit. When CSUR_SRAI_EN is set low, a change in the CSUR_SRAI status does not generate an interrupt.

CSUR_MRAI_EN

Register bit CSUR_MRAI_EN is used as interrupt enable for CSUR_MRAI register bit. It connects the CSUR_MRAI status bit to the INT pin of the LAS4x622 block. When CSUR_MRAI_EN is set to logic one, an interrupt on the INT is generated upon assertion of the CSUR_MRAI register bit. When CSUR_MRAI_EN is set low, a change in the CSUR_MRAI status does not generate an interrupt.

CSUR_MRAV

This status register bit indicates a runaway condition for the CSUR Master PLL. A runaway condition is defined as when the CSUR Master PLL control voltage > 1.6V. When CSUR_MRAV goes high, the entire CSUR is reset automatically.

‘0’ = CSUR Master PLL is in a normal operating condition
‘1’ = CSUR Master PLL is in a runaway condition

CSUR_SRAV

This status register bit indicates a runaway condition for the CSUR Slave PLL. A runaway condition is defined as when the CSUR Slave PLL control voltage > 1.6V. When CSUR_SRAV goes high, the CSUR Slave PLL is reset automatically.

‘0’ = CSUR Slave PLL is in a normal operating condition
‘1’ = CSUR Slave PLL is in a runaway condition

Register 0034H: Quad 622 Rx MABC Interrupt Status Register

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R	REFCLK_DET	X
Bit 3	R	Reserved	X
Bit 2	R	CSUR_MRAI	X
Bit 1	R	CSUR_SRAI	X
Bit 0	R	CSUR_LDI	X

CSUR_LDI

This interrupt status register bit indicates the lock status of the CSUR Slave PLL to the reference clock. Any transition of the status of CSUR slave PLL being locked to the reference clock to the status of CSUR slave PLL being out of lock, it will be set to '1'. If WCIMODE is set to logic 1 only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0 than a read of this register automatically clears the bit. The transition from '0' to '1' of this bit can generate an interrupt if the CSUR_LDI_EN is asserted (= '1').

CSUR_MRAI

This interrupt register bit indicates a runaway condition for the CSUR master PLL. Any transition from a normal operation to a runaway condition of the CSUR master PLL will set this bit to '1'. If WCIMODE is set to logic '1' only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0 than a read of this register automatically clears the bit. The transition from '0' to '1' of this bit can generate an interrupt if the CSUR_MRAI_EN is asserted (= '1').

CSUR_SRAI

This interrupt register bit indicates a runaway condition for the CSUR slave PLL. Any transition from a normal operation to a runaway condition of the CSUR slave PLL will set this bit to '1'. If WCIMODE is set to logic '1' only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0 than a read of this register automatically clears the bit. The transition from '0' to '1' of this bit can generate an interrupt if the CSUR_SRAI_EN is asserted (= '1').

REFCLK_DET

This register bit is used for a sanity detection of the reference clock REFCLK77. REFCLK77 is set to '1' if any rising edge of the reference clock is detected since the last clearance of the register bit. If WCIMODE pin is set to logic 1 only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0 than a read of this register automatically clears the bit.

Note that rising edges can often be detected even when no clock is provided on REFCLK77 if REFCLK77_P/N pins are left floating or if their voltage levels are close to each other (differential PECL inputs). This bit is only valid in quad 622/155 mode.

Register 0035H 0435H 0835H 0C35H: Quad 622 Rx MABC Channel Control Register

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	1
Bit 13	R/W	Reserved	1
Bit 12	R/W	Reserved	1
Bit 11	R/W	Reserved	1
Bit 10	R/W	Reserved	1
Bit 9	R/W	Reserved	1
Bit 8	R/W	Reserved	1
Bit 7	R/W	Reserved	1
Bit 6	R/W	Reserved	1
Bit 5	R/W	Reserved	1
Bit 4	R/W	Reserved	1
Bit 3	R/W	Reserved	0
Bit 2	R/W	SDLE622	0
Bit 1	R/W	CDRU_RSTB	1
Bit 0	R/W	CHAN_ENB	0

CHAN_ENB

The channel enable control register bit CHAN_ENB enables the corresponding channel in the 4x622 MABC to normal operation mode when asserted (= ‘0’). When deasserted (= ‘1’) the channel is disabled and placed into low-power mode.

CDRU_RSTB

The CDRU reset register bit CDRU_RSTB applies a reset to the CDRU of respective channel in the 4x622 MABC when asserted (= ‘0’) . The reset should be applied for at least 100us. A reset signal should be applied after any mode/control pin changes to ensure proper start-up states. When deasserted (=’1’), the corresponding channel is out of reset.

SDLE622

The Serial Diagnostic Loopback Enable (SDLE622) bit, when set to ‘1’, loops the data from the transmit side JAT622 to the receive side Rx. In the loopback mode, the Rx locks to the loopback data.

Register 0036H 0436H 0836H 0C36H: Quad 622 Rx Channel Data Path Control Register

Bit	Type	Function	Default
Bit 15	R/W	LOS_COUNT[5]	0
Bit 14	R/W	LOS_COUNT[4]	1
Bit 13	R/W	LOS_COUNT[3]	0
Bit 12	R/W	LOS_COUNT[2]	0
Bit 11	R/W	LOS_COUNT[1]	0
Bit 10	R/W	LOS_COUNT[0]	0
Bit 9	—	Unused	X
Bit 8	R/W	Reserved	0
Bit 7	R/W	INV_SDI_EN_622	0
Bit 6	R/W	SDI_MASK_622	0
Bit 5	R/W	LOS_EN	1
Bit 4	R/W	RX_INV_DATA_ENB	1
Bit 3	R/W	PRBS_SYNCI_EN	0
Bit 2	R/W	PRBS_ERRI_EN	0
Bit 1	R/W	LOSI_EN	0
Bit 0	R/W	DOOLI_EN	0

DOOLI_EN

Register bit DOOLI_EN is used as interrupt enable for DOOLI register bit. It connects the DOOLI status bit to the INT pin of the LAS4x622 block. When DOOLI_EN is set to logic one, an interrupt on the INT is generated upon assertion of the DOOLI register bit. When DOOLI_EN is set low, a change in the DOOLI status does not generate an interrupt.

Note: The DOOL detection accuracy is affected by jitter on the recovered clock. As a result, the clock skew needed to declare DOOL could exceed +/- 999 ppm.

LOSI_EN

Register bit LOSI_EN is used as interrupt enable for LOSI register bit. It connects the LOSI status bit to the INT pin of the LAS4x622 block. When LOSI_EN is set to logic one, an interrupt on the INT is generated upon assertion of the LOSI register bit. When LOSI_EN is set low, a change in the LOSI status does not generate an interrupt.

PRBS_ERRI_EN

Register bit PRBS_ERRI_EN is used as interrupt enable for PRBS_ERRI register bit. It connects the PRBS_ERRI status bit to the INT pin of the LAS4x622 block. When PRBS_ERRI_EN is set to logic one, an interrupt on the INT is generated upon assertion of the PRBS_ERRI register bit. When PRBS_ERRI_EN is set low, a change in the PRBS_ERRI status does not generate an interrupt.

PRBS_SYNCI_EN

Register bit PRBS_SYNCI_EN is used as interrupt enable for PRBS_SYNCI register bit. It connects the PRBS_SYNCI status bit to the INT pin of the LAS4x622 block. When PRBS_SYNCI_EN is set to logic one, an interrupt on the INT is generated upon assertion of the PRBS_SYNCI register bit. When PRBS_SYNCI_EN is set low, a change in the PRBS_SYNCI status does not generate an interrupt.

RX_INV_DATA_ENB

The Rx Serial Data Inversion Enable RX_INV_DATA_ENB controls the polarity of the received data. When RX_INV_DATA_ENB is set to '0' the polarity of the Rx data is invert. When RX_INV_DATA_ENB is set to '1' the Rx data operates normally.

LOS_EN

The loss of signal enable bit LOS_EN controls the signal detection logic. The LAS4x622 block uses the LOS detector along with the clock difference detector to determine if the CDRU is locked to data. When LOS_EN is set to logic one the incoming signal is monitor for 1/0 transitions has determined by LOS_COUNT[5:0] register bits. If LOS_EN is reset to logic zero the 1/0 transition detector is disabled.

SDI_MASK_622

The Signal Detect Mask bit controls the state of the SD[x] signal in 622 mode. When SDI_MASK_622 is set to a logic one the internal SD signal will be forced to the active high state and all downstream blocks will operate normally. When SDI_MASK_622 is set to logic zero the internal SD signal to downstream blocks follows the state of the SD[x] input pin and the state of the INV_SDI_EN_622 bit.

Note: When the SDI_MASK_622 bit is enabled, it is possible for LOS not to be detected in the absence of an optical input signal. Enabling the SDI_MASK_622 bit masks the SD[x] input and forces the S/UNI MULTI-48 to declare LOS only based on an all '0' or all '1' input pattern. However, noise on AC coupled RXD[1-4] inputs can cause transitions preventing detection of an all '0' or all '1' pattern. To avoid this, disable the SDI_MASK_622 bit and connect the SD[x] input signal to the optical module's SD or LOS output. This will allow LOS to be detected when the optical input signal is lost.

INV_SDI_EN_622

The Signal Detect Inversion INV_SDI_EN_622 controls the polarity of the SD[x] input pin in 622 mode. When INV_SDI_EN_622 is set to '1' the polarity of the SD[x] input pin is inverted. When INV_SDI_EN_622 is set to '0' the polarity of the SD[x] input remains unchanged.

LOS_COUNT[5:0]

The Loss of signal 1's/0's transition detector counts. This field sets the value for the number of consecutive all-zeros or all-ones pattern that will set the loss of signal register bit LOSI to '1'. Each bit in the binary count represents eight ones or zeros in the pattern. I.e. to set the consecutive all-ones or all-zeros pattern to 128 the LOS_COUNT should be set to "010000"b. The default value for this field is 128.

Register 0037H 0437H 0837H 0C37H: Quad 622 Rx Channel Data Path PRBS Control Register

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	PRBS_ERR_CNT_CLR	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	RX_PRBS_EN	0

RX_PRBS_EN

This bit enables the PRBS or fixed pattern monitor of the LAS4x622 block. When low, the monitor is disabled. When high, the monitor is enabled and will check the incoming data stream for errors.

PRBS_ERR_CNT_CLR

The Clear Error Count bit clears the PRBS word error count value. When logic '1' is written to this bit the PRBS word error count register is reset to zero. When set to logic '0' the counter operates normally. This bit should be set to logic '1' than immediately set logic '0' to perform the clear counter operation.

Register 0038H 0438H 0838H 0C38H: Quad 622 Rx Channel Data Interrupt Status Register

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R	Reserved	X
Bit 3	R	PRBS_SYNCI	X
Bit 2	R	PRBS_ERRI	X
Bit 1	R	LOSI	X
Bit 0	R	DOOLI	X

DOOLI

The data out of lock interrupt status indicates the recovered data out of lock assertion event, which happens when the difference between the reference clock and the recovered clock goes within or beyond the 488 to 976 ppm range. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0 than a read of this register automatically clears the bit.

Note: The DOOL detection accuracy is affected by jitter on the recovered clock. As a result, the clock skew needed to declare DOOL could exceed +/- 999 ppm.

LOSI

The loss of signal interrupt status indicates the receive signal is lost or at least LOS_COUNT[5:0] consecutive ones or zeros have been received. LOSI is only asserted when the SD input is deasserted or LOS_COUNT[5:0] consecutive ones or zeros have been received (when LOSV transitions from logic 0 to logic 1). This event indicator is not asserted upon LOSV transitions from logic 1 to logic 0. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0 than a read of this register automatically clears the bit.

PRBS_ERRI

The PRBS Bit Error bit provides an event indication that a bit error has been detected in the comparison between the incoming data and the locally generated data. The PRBS_ERRI is set high when the monitor is in the synchronized state and when an error in a PRBS word is detected. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0 than a read of this register automatically clears the bit.

PRBS_SYNCI

The PRBS Synchronization bit indicates that a change in the status of PRBS Monitor has occurred. The comparison is made between the incoming data and the PRBS pattern generated locally. The PRBS_SYNCI is set high when the monitor is in the synchronized state and has received two consecutive corrupted words forcing the PRBS monitor to resynchronize. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0 than a read of this register automatically clears the bit.

Register 0039H 0439H 0839H 0C39H: Quad 622 Rx Channel Data Path PRBS Status Register

Bit	Type	Function	Default
Bit 15	R	PRBS_ERR_CNT[8]	X
Bit 14	R	PRBS_ERR_CNT[7]	X
Bit 13	R	PRBS_ERR_CNT[6]	X
Bit 12	R	PRBS_ERR_CNT[5]	X
Bit 11	R	PRBS_ERR_CNT[4]	X
Bit 10	R	PRBS_ERR_CNT[3]	X
Bit 9	R	PRBS_ERR_CNT[2]	X
Bit 8	R	PRBS_ERR_CNT[1]	X
Bit 7	R	PRBS_ERR_CNT[0]	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R	PRBS_SYNCV	X
Bit 2	R	PRBS_ERRV	X
Bit 1	R	LOSV	X
Bit 0	R	DOOLV	X

DOOLV

The status register bit DOOLV indicates the recovered data out of lock status, which is defined as the difference between the reference clock and the recovered clock beyond a certain ppm level . DOOLV is asserted when the ppm level goes within or beyond the 488 to 976 ppm range, and is deasserted when the ppm level lowers within or below the 488 to 976 ppm range.

DOOLV = ‘0’, normal operation.

DOOLV = ‘1’, recovered data out of lock

Note: The DOOL detection accuracy is affected by jitter on the recovered clock. As a result, the clock skew needed to declare DOOL could exceed +/- 999 ppm.

LOSV

The status register bit LOSV indicates the receive signal is lost or at least LOS_COUNT[4:0] consecutive ones or zeros have been received. LOSV is a logic zero if the SD input is high or less than LOS_COUNT[5:0] consecutive ones or zeros have been received. LOSV is a logic one if the SD input is low or LOS_COUNT[5:0] consecutive ones or zeros have been received.

PRBS_ERRV

The PRBS Bit Error bit PRBS_ERRV provides a status indication that a bit error has been detected in the comparison between the incoming data and the locally generated data. The PRBS_ERRV is set high when the monitor is in the synchronized state and when an error in a PRBS word is detected. PRBS_ERRV is set low in normal operation.

PRBS_SYNCV

The PRBS Synchronization bit PRBS_SYNCV indicates that a change in the status of PRBS Monitor has occurred. The comparison is made between the incoming data and the PRBS pattern generated locally. The PRBS_SYNCV is set high when the monitor is in the synchronized state and has received two consecutive corrupted words forcing the PRBS monitor to resynchronize.

PRBS_ERR_CNT[8:0]

The ERR_CNT[8:0] register, is the number of errors in the PRBS words detected during the monitoring. Errors are accumulated only when the monitor is in the synchronized state. Even if there are multiple errors within one PRBS word, only one error is counted. The PRBS_ERR_CNT[8:0] register is cleared by writing to the PRBS_ERR_CNT_CLR bit in Register 04H. The error counter will not wrap around after reaching 1FFh, it will saturate to this value.

Register 0040H: SRLI Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	1
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	DISFRM	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	—	Unused	X

All Reserved bits must be set to their default values for proper operation.

DISFRM

The disable framing (DISFRM) bit disables the framing algorithm and resets the bit alignment on the RD[15:0] input bus to none. When DISFRM is set to logic 1, the framing algorithm is disabled and the bit alignment is reset to none. When DISFRM is set to logic 0, the framing algorithm is enable and the bit alignment is done when out of frame is declared.

Register 0060H 0460H 0860H 0C60H: SBER Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	SFBERTEN	0
Bit 4	R/W	SFSMODE	0
Bit 3	R/W	SFCMODE	0
Bit 2	R/W	SDBERTEN	0
Bit 1	R/W	SDSMODE	0
Bit 0	R/W	SDCMODE	0

SDCMODE

The SDCMODE alarm bit selects the Signal Degrade BERM window size to use for clearing alarms. When SDCMODE is a logic 0, the SD BERM will clear an alarm using the same window size used for declaration. When SDCMODE is a logic 1, the SD BERM will clear an alarm using a window size that is 8 times longer than alarm declaration window size. The declaration window size is defined by the SBER SD BERM Accumulation Period register.

SDSMODE

The SDSMODE bit selects the Signal Degrade BERM saturation mode. When SDSMODE is a logic 0, the SD BERM will saturate the BIP count on a per frame basis using the SBER SD Saturation Threshold register value. When SDSMODE is a logic 1, the SD BERM will saturate the BIP count on a per window subtotals accumulation period basis using the SBER SD Saturation Threshold register value.

SDBERTEN

The SDBERTEN bit enables automatic monitoring of line bit error rate threshold events by the Signal Degrade BERM. When SDBERTEN is a logic one, the SD BERM continuously monitors line BIP errors over a period defined in the BERM configuration registers. When SDBERTEN is a logic zero, the SD BERM BIP accumulation logic is disabled and the BERM logic is reset to restart in the declaration monitoring state.

All SD BERM configuration registers should be set up before the monitoring is enabled.

SFCMODE

The SFCMODE alarm bit selects the Signal Failure BERM window size to use for clearing alarms. When SFCMODE is a logic 0, the SF BERM will clear an alarm using the same window size used for declaration. When SFCMODE is a logic 1, the SF BERM will clear an alarm using a window size that is 8 times longer than alarm declaration window size. The declaration window size is defined by the SBER SF BERM Accumulation Period register.

SFSMODE

The SFSMODE bit selects the Signal Failure BERM saturation mode. When SFSMODE is a logic 0, the SF BERM will saturate the BIP count on a per frame basis using the SBER SF Saturation Threshold register value. When SFSMODE is a logic 1, the SF BERM will saturate the BIP count on a per window subtotals accumulation period basis using the SBER SD Saturation Threshold register value.

SFBERTEN

The SFBERTEN bit enables automatic monitoring of line bit error rate threshold events by the Signal Failure BERM. When SFBERTEN is a logic one, the SF BERM continuously monitors line BIP errors over a period defined in the BERM configuration registers. When SFBERTEN is a logic zero, the SF BERM BIP accumulation logic is disabled, and the BERM logic is reset to restart in the declaration monitoring state.

All SF BERM configuration registers should be set up before the monitoring is enabled.

Register 0061H 0461H 0861H 0C61H: SBER Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R	SFBERV	X
Bit 0	R	SDBERV	X

SDBERV

The SDBERV bit indicates the Signal Failure BERM alarm state. The alarm is declared (SDBERV is a logic one) when the declaring threshold has been exceeded. The alarm is removed (SDBERV is a logic zero) when the clearing threshold has been reached.

SFBERV

The SFBERV bit indicates the Signal Failure BERM alarm state. The alarm is declared (SFBERV is a logic one) when the declaring threshold has been exceeded. The alarm is removed (SFBERV is a logic zero) when the clearing threshold has been reached.

Register 0062H 0462H 0862H 0C62H: SBER Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R/W	SFBERE	0
Bit 0	R/W	SDBERE	0

SDBERE

The SDBERE bit is the interrupt enable for the SDBER alarm. When SDBERE set to logic 1, the pending interrupt in the SBER Interrupt Status register, SDBERI, will assert the interrupt (INTB) output. When SDBERE is set to logic 0, the pending interrupt will not assert the interrupt (INTB) output.

SFBERE

The SFBERE bit is the interrupt enable for the SFBER alarm. When SFBERE set to logic 1, the pending interrupt in the SBER Interrupt Status Register, SFBERI, will assert the interrupt (INTB) output. When SFBERE is set to logic 0, the pending interrupt will not assert the interrupt (INTB) output.

Register 0063H 0463H 0863H 0C63H: SBER Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R	SFBERI	X
Bit 0	R	SDBERI	X

SDBERI

The SDBERI bit is an event indicator set to logic 1 to indicate any changes in the status of SDBERV. This interrupt status bit is independent of the SDBERE interrupt enable bits. If WCIMODE is set to logic 1, only over-writing with a logic 1 clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

SFBERI

The SFBERI bit is an event indicator set to logic 1 to indicate any changes in the status of SFBERV. This interrupt status bit is independent of the SFBERE interrupt enable bits. If WCIMODE is set to logic 1, only over-writing with a logic 1 clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

Register 0064H 0464H 0864H 0C64H: SBER SF BERM Accumulation Period (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFSAP[15:0]	0000

Register 0065H 0465H 0865H 0C65H: SBER SF BERM Accumulation Period (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFSAP[31:16]	0000

SFSAP[31:0]

The SFSAP[31:0] bits represent the number of STS-N frames to be used to accumulate a BIP error subtotal. The total evaluation window to declare an alarm is broken into 8 subtotals, so this register value represents 1/8 of the total sliding window size. Refer to Operation Section for the recommended settings.

Register 0066H 0466H 0866H 0C66H: SBER SF BERM Saturation Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFSATH[15:0]	FFFF

Register 0067H 0467H 0867H 0C67H: SBER SF BERM Saturation Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFSATH[23:16]	XXFF

SFSATH[23:0]

The SFSTH[23:0] bits represent the allowable number of BIP errors that can be accumulated during a BIP accumulation period before a BER threshold event is asserted. Setting this threshold to 0xFFFFFF disables the saturation functionality. Refer to Operation Section for the recommended settings.

Register 0068H 0468H 0868H 0C68H: SBER SF BERM Declaring Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFDECTH[15:0]	0000

Register 0069H 0469H 0869H 0C69H: SBER SF BERM Declaring Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFDECTH[23:16]	XX00

SFDECTH[23:0]

The SFDECTH[23:0] register represents the number of BIP errors that must be accumulated during a full evaluation window in order to declare a BER alarm. Refer to Operation Section for the recommended settings.

Register 006AH 046AH 086AH 0C6AH: SBER SF BERM Clearing Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFCLRTH[15:0]	0000

Register 006BH 046BH 086BH 0C6BH: SBER SF BERM Clearing Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFCLRTH[23:16]	XX00

SFCLRTH[23:0]

The SFCLRTH[23:0] register represents the number of BIP errors that can be accumulated but not exceeded during a full evaluation window in order to clear a BER alarm. Refer to Operation Section for the recommended settings.

Register 006CH 046CH 086CH 0C6CH: SBER SD BERM Accumulation Period (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDSAP[15:0]	0000

Register 006DH 046DH 086DH 0C6DH: SBER SD BERM Accumulation Period (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDSAP[31:16]	0000

SDSAP[31:0]

The SDSAP[31:0] bits represent the number of STS-N frames to be used to accumulate a BIP error subtotal. The total evaluation window to declare an alarm is broken into 8 subtotals, so this register value represents 1/8 of the total sliding window size. Refer to Operation Section for the recommended settings.

Register 006EH 046EH 086EH 0C6EH: SBER SD BERM Saturation Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDSATH[15:0]	FFFF

Register 006FH 046FH 086FH 0C6FH: SBER SD BERM Saturation Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDSATH[23:16]	XXFF

SDSATH[23:0]

The SDSATH[23:0] bits represent the allowable number of BIP errors that can be accumulated during a BIP accumulation period before a BER threshold event is asserted. Setting this threshold to 0xFFFFFFFF disables the saturation functionality. Refer to Operation Section for the recommended settings.

Register 0070H 0470H 0870H 0C70H: SBER SD BERM Declaring Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDDECTH[15:0]	0000

Register 0071H 0471H 0871H 0C71H: SBER SD BERM Declaring Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDDECTH[23:16]	XX00

SDDECTH[23:0]

The SDDECTH[23:0] register represents the number of BIP errors that must be accumulated during a full evaluation window in order to declare a BER alarm. Refer to Operation Section for the recommended settings.

Register 0072H 0472H 0872H 0C72H: SBER SD BERM Clearing Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDCLRTH[15:0]	0000

Register 0073H 0473H 0873H 0C73H: SBER SD BERM Clearing Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDCLRTH[23:16]	XX00

SDCLRTH[23:0]

The SDCLRTH[23:0] register represents the number of BIP errors that can be accumulated but not exceeded during a full evaluation window in order to clear a BER alarm. Refer to Operation Section for the recommended settings.

Register 0080H 0480H 0880H 0C80H: RRMP Configuration

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	—	Unused	X
Bit 13	R/W	Reserved	0
Bit 12	R/W	LREIBLK	0
Bit 11	R/W	LBIPEREIBLK	0
Bit 10	R/W	LBIPEBERBLK	0
Bit 9	R/W	LBIPEACCBLK	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	SBIPEACCBLK	0
Bit 6	R/W	Reserved	1
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	1
Bit 3	R/W	LRDI3	0
Bit 2	R/W	LAIS3	0
Bit 1	R/W	ALGO2	0
Bit 0	W	FOOF	X

All Reserved bits must be set to their default values for proper operation.

FOOF

The force out of frame (FOOF) bit forces out of frame condition. When a logic 1 is written to FOOF, the framer block is forced out of frame at the next frame boundary regardless of the framing pattern value. The OOF event initiates re-framing in an upstream frame detector. FOOF must be written to logic 0 to remove the force out of frame condition.

ALGO2

The ALGO2 bit selects the framing pattern used to determine and maintain the frame alignment. When ALGO2 is set to logic 1, the framing pattern consist of the 8 bits of the first A1 framing bytes and the first 4 bits of the last A2 framing bytes (12 bits total). This algorithm examines only 12 framing bits; all other framing bits are ignored. When ALGO2 is set to logic 0, the framing patterns consist of 12 A1 framing bytes and 12 A2 framing bytes.

LAIS3

The line alarm indication signal detection (LAIS3) bit selects the Line AIS detection algorithm. When LAIS3 is set to logic 1, Line AIS is declared when a 111 pattern is detected in bits 6,7,8 of the K2 byte for three consecutive frames. When LAIS3 is set to logic 0, Line AIS is declared when a 111 pattern is detected in bits 6,7,8 of the K2 byte for five consecutive frames.

LRDI3

The line remote defect indication detection (LRDI3) bit selects the Line RDI detection algorithm. When LRDI3 is set to logic 1, Line RDI is declared when a 110 pattern is detected in bits 6,7,8 of the K2 byte for three consecutive frames. When LRDI3 is set to logic 0, Line RDI is declared when a 110 pattern is detected in bits 6,7,8 of the K2 byte for five consecutive frames.

SBIPEACCBLK

The section BIP error accumulation block (SBIPEACCBLK) bit controls the accumulation of section BIP errors. When SBIPEACCBLK is set to logic 1, the section BIP accumulation represents BIP-8 block errors (a maximum of 1 error per frame). When SBIPEACCBLK is set to logic 0, the section BIP accumulation represents BIP-8 errors (a maximum of 8 errors per frame).

LBIPEACCBLK

The line BIP error accumulation block (LBIPEACCBLK) bit controls the accumulation of line BIP errors. When LBIPEACCBLK is set to logic 1, the line BIP accumulation represents BIP-24 block errors (a maximum of 1 error per STS-3/STM-1 per frame). When LBIPEACCBLK is set to logic 0, the line BIP accumulation represents BIP-8 errors (a maximum of 8 errors per STS-1/STM-0 per frame).

LBIPEBERBLK

The line BIP error BER block (LBIPEBERBLK) bit controls the indication of line BIP errors for the BER monitoring. When LBIPEBERBLK is set to logic 1, the line BIP count used for BER monitoring represents BIP-24 block errors (a maximum of 1 error per STS-3/STM-1 per frame). When LBIPEBERBLK is set to logic 0, the line BIP count used for BER monitoring represents BIP-8 errors (a maximum of 8 errors per STS-1/STM-0 per frame).

LBIPEREIBLK

The line BIP error REI block (LBIPEREIBLK) bit controls the indication of line BIP errors for the REI-L insertion. When LBIPEREIBLK is set to logic 1, the line BIP count used for REI-L insertion represents BIP-24 block errors (a maximum of 1 error per STS-3/STM-1 per frame saturated to 255). When LBIPEREIBLK is set to logic 0, the line BIP count used for REI-L insertion represents BIP-8 errors (a maximum of 8 errors per STS-1/STM-0 per frame saturated to 255).

LREIBLK

The line REI block (LREIBLK) bit controls the extraction of line REI errors from the M1 byte. When LREIBLK is set to logic 1, the extracted line REI are interpreted as block BIP-24 errors (a maximum of 1 error per STS-3/STM-1 per frame). When LREIBLK is set to logic 0, the extracted line REI are interpreted as BIP-8 errors (a maximum of 8 errors per STS-1/STM-0 per frame).

BUSY

The BUSY (BUSY) bit reports the status of the transfer of section BIP, line BIP and line REI error counters to the holding registers. BUSY is set to logic 1 upon writing to the holding register addresses or by a low to high transition on LCK. BUSY is set to logic 0 upon completion of the transfer. This bit should be polled to determine when new data is available in the holding registers.

Register 0081H 0481H 0881H 0C81H: RRMP Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R	APSBFV	X
Bit 4	R	LRDIV	X
Bit 3	R	LAISV	X
Bit 2	R	LOSV	X
Bit 1	R	LOFV	X
Bit 0	R	OOFV	X

OOFV

The OOFV bit reflects the current status of the out of frame defect. The OOF defect is declared when four consecutive frames have one or more bit errors in their framing pattern. The OOF defect is cleared when two error free framing pattern are found.

LOFV

The LOFV bit reflects the current status of the loss of frame defect. The LOF defect is declared when an out of frame condition exists for a total period of 3 ms during which there is no continuous in frame period of 3 ms. The LOF defect is cleared when an in frame condition exists for a continuous period of 3 ms.

LOSV

The LOSV bit reflects the current status of the loss of signal defect. The LOS defect is declared when 20 µs of consecutive all zeros pattern is detected. The LOS defect is cleared when two consecutive error free framing patterns are found and during the intervening time (one frame) there is no violating period of consecutive all zeros pattern.

LAISV

The LAISV bit reflects the current status of the line alarm indication signal defect. The AIS-L defect is declared when the 111 pattern is detected in bits 6,7 and 8 of the K2 byte for three or five consecutive frames. The AIS-L defect is cleared when any pattern other than 111 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames.

Note for STS-3/STM-1 mode only: During a LOS condition, the all zeros pattern from the receive line interface, when descrambled by the RRMP, can cause a continous 0x77 byte sequence in the K2 byte position. In that case, RRMP will report AIS-L along with LOS.

LRDIV

The LRDIV bit reflects the current status of the line remote defect indication signal defect. The RDI-L defect is declared when the 110 pattern is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. The RDI-L defect is cleared when any pattern other than 110 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames.

APSBFV

The APSBF bit reflects the current status of the APS byte failure defect. The APS byte failure defect is declared when no three consecutive identical K1 bytes are received in the last twelve consecutive frames starting with the last frame containing a previously consistent byte. The APS byte failure defect is cleared when three consecutive identical K1 bytes are received.

Register 0082H 0482H 0882H 0C82H: RRMP Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	R/W	LREIEE	0
Bit 9	R/W	LBIPEE	0
Bit 8	R/W	SBIPEE	0
Bit 7	R/W	COSSME	0
Bit 6	R/W	COAPSE	0
Bit 5	R/W	APSBFE	0
Bit 4	R/W	LRDIE	0
Bit 3	R/W	LAISE	0
Bit 2	R/W	LOSE	0
Bit 1	R/W	LOFE	0
Bit 0	R/W	OOFE	0

OOFE, LOFE, LOSE, LAISE, LRDIE, APSBFE, COAPSE, COSSME, SBIPEE, LBIPEE, LREIEE

The interrupt enable bits control the activation of the interrupt (INTB) output. When the interrupt enable bit is set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When the interrupt enable bit is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

Register 0083H 0483H 0883H 0C83H: RRMP Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	R	LREIEI	X
Bit 9	R	LBIPEI	X
Bit 8	R	SBIPEI	X
Bit 7	R	COSSMI	X
Bit 6	R	COAPSI	X
Bit 5	R	APSBFI	X
Bit 4	R	LRDII	X
Bit 3	R	LAISI	X
Bit 2	R	LOSI	X
Bit 1	R	LOFI	X
Bit 0	R	OOFI	X

OOFI

The out of frame interrupt status (OOFI) bit is an event indicator. OOFI is set to logic 1 to indicate any change in the status of OOFV. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

LOFI

The loss of frame interrupt status (LOFI) bit is an event indicator. LOFI is set to logic 1 to indicate any change in the status of LOFV. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

LOSI

The loss of signal interrupt status (LOSI) bit is an event indicator. LOSI is set to logic 1 to indicate any change in the status of LOSV. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

LAISI

The line alarm indication signal interrupt status (LAISI) bit is an event indicator. LAISI is set to logic 1 to indicate any change in the status of LAISV. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a ‘1’ clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

LRDII

The line remote defect indication interrupt status (LRDII) bit is an event indicator. LRDII is set to logic 1 to indicate any change in the status of LRDIV. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a ‘1’ clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

APSBFI

The APS byte failure interrupt status (APSBFI) bit is an event indicator. APSBFI is set to logic 1 to indicate any change in the status of APSBFV. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a ‘1’ clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

COAPSI

The change of APS bytes interrupt status (COAPSI) bit is an event indicator. COAPSI is set to logic 1 to indicate new APS bytes. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a ‘1’ clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

COSSMI

The change of SSM message interrupt status (COSSMI) bit is an event indicator. COSSMI is set to logic 1 to indicate a new SSM message. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a ‘1’ clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

SBIPEI

The section BIP error interrupt status (SBIPEI) bit is an event indicator. SBIPEI is set to logic 1 to indicate a section BIP error. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a ‘1’ clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

LBIPEI

The line BIP error interrupt status (LBIPEI) bit is an event indicator. LBIPEI is set to logic 1 to indicate a line BIP error. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

LREIEI

The line REI error interrupt status (LREIEI) bit is an event indicator. LREIEI is set to logic 1 to indicate a line REI error. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

Register 0084H 0484H 0884H 0C84H: RRMP Receive APS

Bit	Type	Function	Default
Bit 15	R	K1V[7]	X
Bit 14	R	K1V[6]	X
Bit 13	R	K1V[5]	X
Bit 12	R	K1V[4]	X
Bit 11	R	K1V[3]	X
Bit 10	R	K1V[2]	X
Bit 9	R	K1V[1]	X
Bit 8	R	K1V[0]	X
Bit 7	R	K2V[7]	X
Bit 6	R	K2V[6]	X
Bit 5	R	K2V[5]	X
Bit 4	R	K2V[4]	X
Bit 3	R	K2V[3]	X
Bit 2	R	K2V[2]	X
Bit 1	R	K2V[1]	X
Bit 0	R	K2V[0]	X

K1V[7:0]/K2V[7:0]

The APS K1/K2 bytes value (K1V[7:0]/K2V[7:0]) bits represent the extracted K1/K2 APS bytes. K1V/K2V is updated when the same K1 and K2 bytes (forming a single entity) are received for three consecutive frames.

Register 0085H 0485H 0885H 0C85H: RRMP Receive SSM

Bit	Type	Function	Default
Bit 15	R/W	BYTESSM	0
Bit 14	R/W	FLTRSSM	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	SSMV[7]	X
Bit 6	R	SSMV[6]	X
Bit 5	R	SSMV[5]	X
Bit 4	R	SSMV[4]	X
Bit 3	R	SSMV[3]	X
Bit 2	R	SSMV[2]	X
Bit 1	R	SSMV[1]	X
Bit 0	R	SSMV[0]	X

SSMV[7:0]

The synchronization status message value (SSMV[7:0]) bits represent the extracted S1 nibble (or byte). When filtering is enabled via the FLTRSSM register bit, SSMV is updated when the same S1 nibble (or byte) is received for eight consecutive frames. When filtering is disabled, SSMV is updated every frame.

FLTRSSM

The filter synchronization status message (FLTRSSM) bit enables the filtering of the SSM nibble (or byte). When FLTRSSM is set to logic 1, the SSM value is updated when the same SSM is received for eight consecutive frames. When FLTRSSM is set to logic 0, the SSM value is updated every frame.

BYTESSM

The byte synchronization status message (BYTESSM) bit extends the SSM from a nibble to a byte. When BYTESSM is set to logic 1, the SSM is a byte and bits 1 to 8 of the S1 byte are considered. When BYTESSM is set to logic 0, the SSM is a nibble and only bits 5 to 8 of the S1 byte are considered.

Register 0086H 0486H 0886H 0C86H: RRMP AIS Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	RLAISINS	0
Bit 2	R/W	RLAISEN	0
Bit 1	R/W	RLOHAISEN	0
Bit 0	R/W	RSOHAISEN	0

RSOHAISEN

The receive section overhead AIS enable (RSOHAISEN) bit enables AIS insertion on RTOH when carrying section overhead bytes. When RSOHAISEN is set to logic 1, all ones are forced on the section overhead bytes when a line defect condition exists and this defect is enabled in SARC Section Downstream AIS-L Enbale register (register 0264H 0664H 0A64H 0E64H). When RSOHAISEN is set to logic 0, no AIS are forced on the section overhead bytes regardless of the alarm condition.

RLOHAISEN

The receive line overhead AIS enable (RLOHAISEN) bit enables AIS insertion on RTOH, when carrying line overhead bytes. When RLOHAISEN is set to logic 1, all ones are forced on the line overhead bytes when a line defect condition exists and this defect is enabled in SARC Section Downstream AIS-L Enable register (register 0264H 0664H 0A64H 0E64H). When RLOHAISEN is set to logic 0, no AIS are forced on the line overhead bytes regardless of the alarm condition.

RLAISEN

The receive line AIS enable (RLAISEN) bit enables line AIS insertion in the outgoing data stream. When RLAISEN is set to logic 1, line AIS is inserted in the outgoing data stream when a line defect condition exists and when the SARC block is configured for this alarm consequential action (Register 0264H 0664H 0A64H 0E64H: SARC Section RLAISINS Enable). When RLAISEN is set to logic 0, no line AIS is inserted regardless of the alarm condition.

This bit should be set to logic 1 for normal operation.

RLAISINS

The receive line AIS insertion (RLAISIN) bit forces line AIS insertion in the receive SONET data stream. When RLAISINS is set to logic 1, all ones are inserted in the line overhead bytes and in the payload bytes (all the bytes of the frame except the section overhead bytes) to force a line AIS condition. When RLAISINS is set to logic 0, the line AIS condition is removed.

Register 0087H 0487H 0887H 0C87H: RRMP Section BIP Error Counter

Bit	Type	Function	Default
Bit 15	R	SBIPE[15]	X
Bit 14	R	SBIPE[14]	X
Bit 13	R	SBIPE[13]	X
Bit 12	R	SBIPE[12]	X
Bit 11	R	SBIPE[11]	X
Bit 10	R	SBIPE[10]	X
Bit 9	R	SBIPE[9]	X
Bit 8	R	SBIPE[8]	X
Bit 7	R	SBIPE[7]	X
Bit 6	R	SBIPE[6]	X
Bit 5	R	SBIPE[5]	X
Bit 4	R	SBIPE[4]	X
Bit 3	R	SBIPE[3]	X
Bit 2	R	SBIPE[2]	X
Bit 1	R	SBIPE[1]	X
Bit 0	R	SBIPE[0]	X

SBIPE[15:0]

The section BIP error (SBIPE[15:0]) bits represent the number of section BIP errors that have been detected since the last accumulation interval. The error counter is transferred to the holding registers by a microprocessor write to any of the local RRMP counter registers or the S/UNI MULTI-48 Global Performance Monitor Update register (0002H).

Register 0088H 0488H 0888H 0C88H: RRMP Line BIP Error Counter (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	LBIPE[15:0]	XXXX

Register 0089H 0489H 0889H 0C89H: RRMP Line BIP Error Counter (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 8	—	Unused	X
Bit 7 to Bit 0	R	LBIPE[23:16]	XX

LBIPE[23:0]

The line BIP error (LBIPE[23:0]) bits represent the number of line BIP errors that have been detected since the last accumulation interval. The error counter is transferred to the holding registers by a microprocessor write to any of the local RRMP counter registers or the S/UNI MULTI-48 Global Performance Monitor Update register (0002H).

Register 008AH 048AH 088AH 0C8AH: RRMP Line REI Error Counter (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	LREIE[15:0]	XXXX

Register 008BH 048BH 088BH 0C8BH: RRMP Line REI Error Counter (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 8	—	Unused	X
Bit 7 to Bit 0	R	LREIE[23:16]	XX

LREIE[23:0]

The line REI error (LREIE[23:0]) bits represent the number of line REI errors that have been detected since the last accumulation interval. The error counter is transferred to the holding registers by a microprocessor write to any of the local RRMP counter registers or the S/UNI MULTI-48 Global Performance Monitor Update register (0002H).

Register 00A0H 04A0H 08A0H 0CA0H: RTTP SECTION Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	R/W	IADDR[7]	0
Bit 12	R/W	IADDR[6]	0
Bit 11	R/W	IADDR[5]	0
Bit 10	R/W	IADDR[4]	0
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	SECTION[3]	0
Bit 2	R/W	SECTION[2]	0
Bit 1	R/W	SECTION[1]	0
Bit 0	R/W	SECTION[0]	0

SECTION[3:0]

The STS-1/STM-0 section (SECTION[3:0]) bits select which STS-1/STM-0 timeslot is accessed by the current indirect transfer. This register should be set to 0001.

IADDR[7:0]

The indirect address location (IADDR[7:0]) bits select which indirect address location is accessed by the current indirect transfer.

Indirect Address IADDR[7:0]	Indirect Data
0000 0000	Configuration
0000 0001 to 0011 1111	Invalid address
0100 0000	First byte of the 1/16/64 byte captured trace
0100 0001 to 0111 1111	Other bytes of the 16/64 byte captured trace
1000 0000	First byte of the 1/16/64 byte accepted trace
1000 0001 to 1011 1111	Other bytes of the 16/64 byte accepted trace
1100 0000	First byte of the 16/64 byte expected trace
1100 0001 to 1111 1111	Other bytes of the 16/64 byte expected trace

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0 upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

Register 00A1H 04A1H 08A1H 0CA1H: RTTP SECTION Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Register 00A2H 04A2H 08A2H 0CA2H: RTTP SECTION Trace Unstable Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	TIUV	X

All Reserved bits must be set to their default values for proper operation.

TIUV

The trace identifier unstable status (TIUV) bit indicates the current status of the TIU defect.

Algorithm 1: TIUV is set to logic 0.

Algorithm 2: TIUV is set to logic 1 when one or more erroneous bytes are detected between the current message and the previous message in a total of 8 trail trace messages without any persistent message in between. TIUV is set to logic 0 when a persistent message is found. A persistent message is found when the same message is received for 3 or 5 consecutive multi-frames.

Algorithm 3: TIUV is set to logic 1 when one or more erroneous bytes are detected in three consecutive sixteen byte windows. The first window starts on the first erroneous trail trace byte. BYTE_TIUV is set to logic 0 when the same trail trace byte is received for 48 consecutive frames.

Register 00A3H 004A3H 08A3H 0CA3H: RTTP SECTION Trace Unstable Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	TIUE	0

All Reserved bits must be set to their default values for proper operation.

TIUE

The trace identifier unstable interrupt enable (TIUE) bit controls the activation of the interrupt (INTB) output. When the bit is set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When the bit is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

Register 00A4H 04A4H 08A4H 0CA4H: RTTP SECTION Trace Unstable Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	TIUI	X

All Reserved bits must be set to their default values for proper operation.

TIUI

The trace identifier unstable interrupt status (TIUI) bit is an event indicator. TIUI is set to logic 1 to indicate any changes in the status of TIUV (stable to unstable, unstable to stable). If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

Register 00A5H 04A5H 08A5H 0CA5H: RTTP SECTION Trace Mismatch Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	TIMV	X

TIMV

The trace identifier mismatch status (TIMV) bit indicates the current status of the TIM defect.

Algorithm 1: TIMV is set to logic 1 when none of the last 20 messages matches the expected message. TIMV is set to logic 0 when 16 of the last 20 messages match the expected message.

Algorithm 2: TIMV is set to logic 1 when the accepted message does not match the expected message. TIMV is set to logic 0 when the accepted message matches the expected message.

Algorithm 3: TIMV is set to logic 0.

Register 00A6H 04A6H 08A6H 0CA6H: RTTP SECTION Trace Mismatch Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	TIME	0

All Reserved bits must be set to their default values for proper operation.

TIME

The trace identifier mismatch interrupt enable (TIME) bit controls the activation of the interrupt (INTB) output. When set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

Register 00A7H 04A7H 08A7H 0CA7H: RTTP SECTION Trace Mismatch Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	TIMI	X

All Reserved bits must be set to their default values for proper operation.

TIMI

The trace identifier mismatch interrupt status (TIMI) bit is an event indicator. TIMI is set to logic 1 to indicate any changes in the status of TIMV (match to mismatch, mismatch to match). This interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

Indirect Register 00H: RTTP SECTION Trace Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R/W	SYNC_CRLF	0
Bit 5	R/W	ZEROEN	0
Bit 4	R/W	PER5	0
Bit 3	R/W	NOSYNC	0
Bit 2	R/W	LENGTH16	0
Bit 1	R/W	ALGO[1]	0
Bit 0	R/W	ALGO[0]	0

ALGO[1:0]

The trail trace algorithm select (ALGO[1:0]) bits select the algorithm used to process the trail trace message.

ALGO[1:0]	Trail Trace Algorithm
00	Algorithm disable
01	Algorithm 1
10	Algorithm 2
11	Algorithm 3

When ALGO[1:0] is set to logic 00b, the trail trace algorithms are disabled. The corresponding TIUV, TIMV register bits and the corresponding TIU, TIM output signal time slots are set to logic 0.

LENGTH16

The message length (LENGTH16) bit selects the length of the trail trace message used by algorithm 1 and algorithm 2. When LENGTH16 is set to logic 1, the length of the trail trace message is 16 bytes. When LENGTH16 is set to logic 0, the length of the trail trace message is 64 bytes.

NOSYNC

The synchronization disable (NOSYNC) bit disables the synchronization of the trail trace message in algorithm 1 and algorithm 2. When NOSYNC is set to logic 1, no synchronization is done on the trail trace message. The bytes of the trail trace message are written in the captured page as in a circular buffer. When NOSYNC is set to logic 0, synchronization is done on the trail trace message. See SYNC_CRLF to determine how synchronization is handled when NOSYNC = 0.

PER5

The message persistency (PER5) bit selects the number of multi-frames a trail trace message must be received in order to be declared persistent in algorithm 2. When PER5 is set to logic 1, the same trail trace message must be receive for 5 consecutive multi-frames to be declared persistent. When PER5 is set to logic 0, the same trail trace message must be received for 3 consecutive multi frame to be declared persistent.

ZEROEN

The all zero message enable (ZEROEN) bit selects if the all zero message are validated or not against the expected message in algorithm 1 and algorithm 2. When ZEROEN is set to logic 1, an all zero captured message in algorithm 1 and an all zero accepted message in algorithm 2 are validated against the expected message. A match is declared when both the captured/accepted message and the expected message are all zero. When ZEROEN is set to logic 0, an all zero captured message in algorithm 1 and an all zero accepted message in algorithm 2 are not validated against the expected message but are considered to match. A match is declared when the captured/accepted message is all zero regardless of the expected message.

SYNC_CRLF

The synchronization on CR/LF characters (SYNC_CRLF) bit selects if the current algorithm (except algo3) synchronizes on the CR/LF ASCII characters or on the byte with its MSB set high. When SYNC_CRLF is set to logic 1, the current algorithm synchronizes when it receives the ASCII character “CR” (carriage return) followed by “LF” (line feed) and the current active byte becomes the last byte of the message. When SYNC_CRLF is set to 0, the current algorithm synchronizes when receiving a byte with its MSB set to logic 1. The current active byte then becomes the first byte of the message.

Indirect Register 40H to 7FH: RTTP SECTION Captured Trace

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	CTRACE[7]	X
Bit 6	R/W	CTRACE[6]	X
Bit 5	R/W	CTRACE[5]	X
Bit 4	R/W	CTRACE[4]	X
Bit 3	R/W	CTRACE[3]	X
Bit 2	R/W	CTRACE[2]	X
Bit 1	R/W	CTRACE[1]	X
Bit 0	R/W	CTRACE[0]	X

The RTTP SECTION Captured Trace Indirect Register is provided at RTTP r/w indirect address 40H to 7FH.

CTRACE[7:0]

The captured trail trace message (CTRACE[7:0]) bits contain the currently received trail trace message. When algorithm 1 or 2 is selected and LENGTH16 is set to logic 1, the captured message is stored between address 40h and 4Fh. When algorithm 1 or 2 is selected and LENGTH16 is set to logic 0, the captured message is stored between address 40h and 7Fh. When NOSYNC is set to logic 1, the captured message is not synchronize. When NOSYNC is set to logic 0, the captured message is synchronized and the first byte of the message is stored at address 40h. When algorithm 3 is selected, the captured byte is stored at address 40h.

Indirect Register 80H to BFH: RTTP SECTION Accepted Trace

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	ATRACE[7]	X
Bit 6	R/W	ATRACE[6]	X
Bit 5	R/W	ATRACE[5]	X
Bit 4	R/W	ATRACE[4]	X
Bit 3	R/W	ATRACE[3]	X
Bit 2	R/W	ATRACE[2]	X
Bit 1	R/W	ATRACE[1]	X
Bit 0	R/W	ATRACE[0]	X

The RTTP SECTION Accepted Trace Indirect Register is provided at RTTP r/w indirect address 80H to BFH.

ATRACE[7:0]

The accepted trail trace message (ATRACE[7:0]) bits contain the persistent trail trace message. When algorithm 2 is selected and PER5 is set to logic 1, the accepted message is the same trail trace message received for 5 consecutive multi-frames. When algorithm 2 is selected and PER5 is set to logic 0, the accepted message is the same trail trace message received for 3 consecutive multi-frames. When algorithm 2 is selected and LENGTH16 is set to logic 1, the accepted message is stored between address 80h and 8Fh. When algorithm 2 is selected and LENGTH16 is set to logic 0, the accepted message is stored between address 80h and BFh. When algorithm 3 is selected, the accepted byte is the same trail trace byte received for 48 frames. When algorithm 3 is selected, the accepted byte is stored at address 80h.

Indirect Register C0H to FFH: RTTP SECTION Expected Trace

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	ETRACE[7]	X
Bit 6	R/W	ETRACE[6]	X
Bit 5	R/W	ETRACE[5]	X
Bit 4	R/W	ETRACE[4]	X
Bit 3	R/W	ETRACE[3]	X
Bit 2	R/W	ETRACE[2]	X
Bit 1	R/W	ETRACE[1]	X
Bit 0	R/W	ETRACE[0]	X

The RTTP SECTION Expected Trace Indirect Register is provided at RTTP r/w indirect address C0H to FFH.

ETRACE[7:0]

The expected trail trace message (ETRACE[7:0]) bits contain a static message written by an external microprocessor. In algorithm 1 the expected message is used to validate the captured message. In algorithm 2 the expected message is used to validate the accepted message. When LENGTH16 is set to logic 1, the expected message must be written between address C0h and CFh. When LENGTH16 is set to logic 0, the accepted message must be written between address C0h and FFh.

Register 00C0H 04C0H 08C0H 0CC0H: RTTP PATH Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	R/W	IADDR[7]	0
Bit 12	R/W	IADDR[6]	0
Bit 11	R/W	IADDR[5]	0
Bit 10	R/W	IADDR[4]	0
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 timeslot/path is accessed by the current indirect transfer. PATH[3:0] should only be set to master timeslots values, ranging from 1 (0001) to 4 (0100).

IADDR[7:0]

The indirect address location (IADDR[7:0]) bits select which indirect address location is accessed by the current indirect transfer.

Indirect Address IADDR[7:0]	Indirect Data
0000 0000	Configuration
0000 0001 to 0011 1111	Invalid address
0100 0000	First byte of the 1/16/64 byte captured trace
0100 0001 to 0111 1111	Other bytes of the 16/64 byte captured trace
1000 0000	First byte of the 1/16/64 byte accepted trace
1000 0001 to 1011 1111	Other bytes of the 16/64 byte accepted trace
1100 0000	First byte of the 16/64 byte expected trace
1100 0001 to 1111 1111	Other bytes of the 16/64 byte expected trace

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0 upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

Register 00C1H 04C1H 08C1H 0CC1H: RTTP PATH Indirect Data

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[7:0]

The indirect access data (DATA[7:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transferred to DATA[7:0]. BUSY should be polled to determine when the new data is available in DATA[7:0]. When RWB is set to logic 0 (indirect write), the data from DATA[7:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[7:0] has a different meaning depending on which address of the internal RAM is being accessed.

Register 00C2H 04C2H 08C2H 0CC2H: RTTP PATH Trace Unstable Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	TIUV[4]	X
Bit 2	R	TIUV[3]	X
Bit 1	R	TIUV[2]	X
Bit 0	R	TIUV[1]	X

TIUV[4:1]

The trace identifier unstable status (TIUV[x]) bit indicates the current status of the TIU defect over timeslot x.

Algorithm 1: TIUV is set to logic 0.

Algorithm 2: TIUV is set to logic 1 when one or more erroneous bytes are detected between the current message and the previous message in a total of 8 trail trace messages without any persistent message in between. TIUV is set to logic 0 when a persistent message is found. A persistent message is found when the same message is received for 3 or 5 consecutive multi-frames.

Algorithm 3: TIUV is set to logic 1 when one or more erroneous bytes are detected in three consecutive sixteen byte windows. The first window starts on the first erroneous trail trace byte. BYTE_TIUV is set to logic 0 when the same trail trace byte is received for 48 consecutive frames.

Register 00C3H 04C3H 08C3H 0CC3H: RTTP PATH Trace Unstable Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	TIUE[4]	0
Bit 2	R/W	TIUE[3]	0
Bit 1	R/W	TIUE[2]	0
Bit 0	R/W	TIUE[1]	0

TIUE[4:1]

The trace identifier unstable interrupt enable (TIUE[x]) bit controls the activation of the interrupt (INTB) output. When TIUE[x] is set to logic 1, the corresponding pending interrupt on timeslot x will assert the interrupt (INTB) output. When TIUE[x] is set to logic 0, the corresponding pending interrupt on timeslot x will not assert the interrupt (INTB) output.

Register 00C4H 04C4H 08C4H 0CC4H: RTTP PATH Trace Unstable Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	TIUI[4]	X
Bit 2	R	TIUI[3]	X
Bit 1	R	TIUI[2]	X
Bit 0	R	TIUI[1]	X

TIUI[4:1]

The trace identifier unstable interrupt status (TIUI[x]) bit is an event indicator. TIUI[x] is set to logic 1 to indicate any changes in the status of TIUV[x] (stable to unstable, unstable to stable). This interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

Register 00C5H 04C5H 08C5H 0CC5H: RTTP PATH Trace Mismatch Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	TIMV[4]	X
Bit 2	R	TIMV[3]	X
Bit 1	R	TIMV[2]	X
Bit 0	R	TIMV[1]	X

TIMV[4:1]

The trace identifier mismatch status (TIMV[x]) bit indicates the current status of the TIM defect over timeslot x.

Algorithm 1: TIMV is set to logic 1 when none of the last 20 messages matches the expected message. TIMV is set to logic 0 when 16 of the last 20 messages match the expected message.

Algorithm 2: TIMV is set to logic 1 when the accepted message does not match the expected message. TIMV is set to logic 0 when the accepted message matches the expected message.

Algorithm 3: TIMV is set to logic 0.

Register 00C6H 04C6H 08C6H 0CC6H: RTTP PATH Trace Mismatch Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	TIME[4]	0
Bit 2	R/W	TIME[3]	0
Bit 1	R/W	TIME[2]	0
Bit 0	R/W	TIME[1]	0

TIME[4:1]

The trace identifier mismatch interrupt enable (TIME[x]) bit controls the activation of the interrupt (INTB) output. When TIME[x] is set to logic 1, the corresponding pending interrupt one timeslot x will assert the interrupt (INTB) output. When TIME[x] is set to logic 0, the corresponding pending interrupt on timeslot x will not assert the interrupt (INTB) output.

Register 00C7H 04C7H 08C7H 0CC7H: RTTP PATH Trace Mismatch Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	TIMI[4]	X
Bit 2	R	TIMI[3]	X
Bit 1	R	TIMI[2]	X
Bit 0	R	TIMI[1]	X

TIMI[4:1]

The trace identifier mismatch interrupt status (TIMI[x]) bit is an event indicator. TIMI[x] is set to logic 1 to indicate any changes in the status of TIMV[x] (match to mismatch, mismatch to match). This interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

Indirect Register 00H: RTTP PATH Trace Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R/W	SYNC_CRLF	0
Bit 5	R/W	ZEROEN	0
Bit 4	R/W	PER5	0
Bit 3	R/W	NOSYNC	0
Bit 2	R/W	LENGTH16	0
Bit 1	R/W	ALGO[1]	0
Bit 0	R/W	ALGO[0]	0

ALGO[1:0]

The trail trace algorithm select (ALGO[1:0]) bits select the algorithm used to process the trail trace message.

ALGO[1:0]	Trail Trace Algorithm
00	Algorithm disable
01	Algorithm 1
10	Algorithm 2
11	Algorithm 3

When ALGO[1:0] is set to logic 00b, the trail trace algorithms are disabled. The corresponding TIUV, TIMV register bits and the corresponding TIU, TIM output signal time slots are set to logic 0.

LENGTH16

The message length (LENGTH16) bit selects the length of the trail trace message used by algorithm 1 and algorithm 2. When LENGTH16 is set to logic 1, the length of the trail trace message is 16 bytes. When LENGTH16 is set to logic 0, the length of the trail trace message is 64 bytes.

NOSYNC

The synchronization disable (NOSYNC) bit disables the synchronization of the trail trace message in algorithm 1 and algorithm 2. When NOSYNC is set to logic 1, no synchronization is done on the trail trace message. The bytes of the trail trace message are written in the captured page as in a circular buffer. When NOSYNC is set to logic 0, synchronization is done on the trail trace message. When LENGTH16 is set to logic 1, the trail trace message is synchronized on the MSB of the trail trace message. The byte with its MSB set high is placed in the first byte location of the captured page. When LENGTH16 is set to logic 0, the trail trace message is synchronize on the CR/LF (CR = 0Dh, LF = 0Ah) characters of the trail trace message. The byte following the CR/LF bytes is placed in the first byte location of the captured page.

PER5

The message persistency (PER5) bit selects the number of multi-frames a trail trace message must receive in order to be declared persistent in algorithm 2. When PER5 is set to logic 1, the same trail trace message must be receive for 5 consecutive multi-frames to be declared persistent. When PER5 is set to logic 0, the same trail trace message must be received for 3 consecutive multi-frames to be declared persistent.

ZEROEN

The all zero message enable (ZEROEN) bit selects if the all zero message is validated or not against the expected message in algorithm 1 and algorithm 2. When ZEROEN is set to logic 1, an all zero captured message in algorithm 1 and an all zero accepted message in algorithm 2 are validated against the expected message. A match is declared when both the captured/accepted message and the expected message are all zero. When ZEROEN is set to logic 0, an all zero captured message in algorithm 1 and an all zero accepted message in algorithm 2 are not validated against the expected message but are considered to match. A match is declared when the captured/accepted message is all zero regardless of the expected message.

SYNC_CRLF

The synchronization on CR/LF characters (SYNC_CRLF) bit selects if the current algorithm (except algo3) synchronizes on the CR/LF ASCII characters or on the byte with its MSB set high. When SYNC_CRLF is set to logic 1, the current algorithm synchronizes when it receives the ASCII character “CR” (carriage return) followed by “LF” (line feed) and the current active byte becomes the last byte of the message. When SYNC_CRLF is set to 0, the current algorithm synchronizes when receiving a byte with its MSB set to logic 1. The current active byte then becomes the first byte of the message.

Indirect Register 40H to 7FH: RTTP PATH Captured Trace

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	CTRACE[7]	X
Bit 6	R/W	CTRACE[6]	X
Bit 5	R/W	CTRACE[5]	X
Bit 4	R/W	CTRACE[4]	X
Bit 3	R/W	CTRACE[3]	X
Bit 2	R/W	CTRACE[2]	X
Bit 1	R/W	CTRACE[1]	X
Bit 0	R/W	CTRACE[0]	X

The RTTP PATH Captured Trace Indirect Register is provided at RTTP r/w indirect address 40H to 7FH.

CTRACE[7:0]

The captured trail trace message (CTRACE[7:0]) bits contain the currently received trail trace message. When algorithm 1 or 2 is selected and LENGTH16 is set to logic 1, the captured message is stored between address 40h and 4Fh. When algorithm 1 or 2 is selected and LENGTH16 is set to logic 0, the captured message is stored between address 40h and 7Fh. When NOSYNC is set to logic 1, the captured message is not synchronized. When NOSYNC is set to logic 0, the captured message is synchronized and the first byte of the message is stored at address 40h. When algorithm 3 is selected, the captured byte is stored at address 40h.

Indirect Register 80H to BFH: RTTP PATH Accepted Trace

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	ATRACE[7]	X
Bit 6	R/W	ATRACE[6]	X
Bit 5	R/W	ATRACE[5]	X
Bit 4	R/W	ATRACE[4]	X
Bit 3	R/W	ATRACE[3]	X
Bit 2	R/W	ATRACE[2]	X
Bit 1	R/W	ATRACE[1]	X
Bit 0	R/W	ATRACE[0]	X

The RTTP PATH Accepted Trace Indirect Register is provided at RTTP r/w indirect address 80H to BFH.

ATRACE[7:0]

The accepted trail trace message (ATRACE[7:0]) bits contain the persistent trail trace message. When algorithm 2 is selected and PER5 is set to logic 1, the accepted message is the same trail trace message received for 5 consecutive multi-frames. When algorithm 2 is selected and PER5 is set to logic 0, the accepted message is the same trail trace message received for 3 consecutive multi-frames. When algorithm 2 is selected and LENGTH16 is set to logic 1, the accepted message is stored between address 80h and 8Fh. When algorithm 2 is selected and LENGTH16 is set to logic 0, the accepted message is stored between address 80h and BFh. When algorithm 3 is selected, the accepted byte is the same trail trace byte received for 48 frames. When algorithm 3 is selected, the accepted byte is stored at address 80h.

Indirect Register C0H to FFH: RTTP PATH Expected Trace

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	ETRACE[7]	X
Bit 6	R/W	ETRACE[6]	X
Bit 5	R/W	ETRACE[5]	X
Bit 4	R/W	ETRACE[4]	X
Bit 3	R/W	ETRACE[3]	X
Bit 2	R/W	ETRACE[2]	X
Bit 1	R/W	ETRACE[1]	X
Bit 0	R/W	ETRACE[0]	X

The RTTP PATH Expected Trace Indirect Register is provided at RTTP r/w indirect address C0H to FFH.

ETRACE[7:0]

The expected trail trace message (ETRACE[7:0]) bits contain a static message written by an external microprocessor. In algorithm 1 the expected message is used to validate the captured message. In algorithm 2 the expected message is used to validate the accepted message. When LENGTH16 is set to logic 1, the expected message must be written between address C0h and CFh. When LENGTH16 is set to logic 0, the accepted message must be written between address C0h and FFh.

Register 0100H 0500H 0900H 0D00H: RHPP Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path/timeslot is accessed by the current indirect transfer.

PATH[3:0]	STS-1/STM-0 Path #
0000	Invalid path
0001	Path/timeslot #1
0010	Path/timeslot #2
0011	Path/timeslot #3
0100	Path/timeslot #4
0101	Path/timeslot #5
0110	Path/timeslot #6
0111	Path/timeslot #7
1000	Path/timeslot #8
1001	Path/timeslot #9
1010	Path/timeslot #10
1011	Path/timeslot #11
1100	Path/timeslot #12
1101-1111	Invalid path

IADDR[2:0]

The address location (IADDR[2:0]) bits select which address location is accessed by the current indirect transfer.

Indirect Address IADDR[3:0]	Indirect Data
0000	Pointer Interpreter Configuration
0001	Error Monitor Configuration
0010	Pointer Value and ERDI
0011	Captured and Accepted PSL
0100	Expected PSL and PDI
0101	RHPP Pointer Interpreter status
0110	RHPP Path BIP Error Counter
0111	RHPP Path REI Error Counter
1000	RHPP Path Negative Justification Event Counter
1001	RHPP Path Positive Justification Event Counter
1010 to 1111	Unused

RWB

The active high read and active low write (RWB) bit selects if the current access to an internal register is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to a register. When RWB is set to logic 1, an indirect read access to a register is initiated. The data from the addressed location as indicated using the IADDR field will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to a register is initiated. The data from the Indirect Data Register will be transferred to the addressed register.

BUSY

The active high busy (BUSY) bit reports if a previously initiated indirect access to an internal register has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0 upon completion of the access. This register should be polled to determine when new data is available in the Indirect Data Register.

Register 0101H 0501H 0901H 0D01H: RHPP Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from an indirect register during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the register will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the register. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

Indirect Register 00H: RHPP Pointer Interpreter Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	NDFCNT	0
Bit 4	R/W	INVCNT	0
Bit 3	R/W	RELAYPAIS	0
Bit 2	R/W	JUST3DIS	0
Bit 1	R/W	SSEN	0
Bit 0	—	Unused	X

All Reserved bits must be set to their default values for proper operation.

SSEN

The SS bits enable (SSEN) bit selects whether or not the SS bits are taken into account in the pointer interpreter state machine. When SSEN is set to logic 1, the SS bits must be set to 10 for a valid NORM_POINT, NDF_ENABLE, INC_IND, DEC_IND or NEW_POINT indication. When SSEN is set to logic 0, the SS bits are ignored.

JUST3DIS

The "justification more than 3 frames ago disable" (JUST3DIS) bit selects whether or not the INC_IND or DEC_IND pointer justifications must be more than 3 frames apart to be considered valid. When JUST3DIS is set to logic 0, the previous NDF_ENABLE, INC_IND or DEC_IND indication must be more than 3 frames ago or the present INC_IND or DEC_IND indication is considered an INV_POINT indication. NDF_ENABLE indications can happen every frame regardless of the JUST3DIS bit. When JUST3DIS is set to logic 1, NDF_ENABLE, INC_IND or DEC_IND indication can happen every frame.

RELAYPAIS

The relay path AIS (RELAYPAIS) bit selects the condition to enter the path AIS state in the pointer interpreter state machine. When RELAYPAIS is set to logic 1, the path AIS state is entered with 1 X AIS_ind indication. When RELAYPAIS is set to logic 0, the path AIS state is entered with 3 X AIS_ind indications. This configuration bit also affects the concatenation pointer interpreter state machine.

INVCNT

The invalid counter (INVCNT) bit selects the behavior of the consecutive INV_POINT event counter in the pointer interpreter state machine. When INVCNT is set to logic 1, the consecutive INV_POINT event counter is reset by 3 EQ_NEW_POINT indications. When INVCNT is set to logic 0, the counter is not reset by 3 EQ_NEW_POINT indications. INVCNT must be set to logic 1 to enable behaviour compliant to GR-253 CORE.

NDFCNT

The new data flag counter (NDFCNT) bit selects the behavior of the consecutive NDF_ENABLE event counter in the pointer interpreter state machine. When NDFCNT is set to logic 1, the NDF_ENABLE definition is enabled NDF + ss. When NDFCNT is set to logic 0, the NDF_ENABLE definition is enabled NDF + ss + offset value in the range 0 to 782. This configuration bit only changes the NDF_ENABLE definition for the consecutive NDF_ENABLE event counter to count towards LOP-P defect when the pointer is out of range. This configuration bit does not change the NDF_ENABLE definition for pointer justification.

Indirect Register 01H: RHPP Error Monitor Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	IPREIBLK	0
Bit 9	R/W	IBER	0
Bit 8	R/W	PREIBLKACC	0
Bit 7	R/W	B3EBLK	0
Bit 6	R/W	PBIPECNTBLK	0
Bit 5	R/W	PBIPEBLKACC	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	PRDI10	0
Bit 2	R/W	PLMEND	0
Bit 1	R/W	PSL5	0
Bit 0	R/W	ALGO2	0

The Error Monitor Configuration Indirect Register is provided at RHPP r/w indirect address 01H.

ALGO2

The payload signal label algorithm 2 (ALGO2) bit selects the algorithm for the PSL monitoring. When ALGO2 is set to logic 1, the ITU compliant algorithm (algorithm 2) is used to monitor the PSL. When ALGO2 is set to logic 0, the TELCORDIA compliant algorithm (algorithm 1) is used to monitor the PSL. ALGO2 changes the PLU-P, PLM-P and PDI-P defect definitions but has no effect on UNEQ-P defect, accepted PSL and change of PSL definitions

PSL5

The payload signal label detection (PSL5) bit selects the path PSL persistence. When PSL5 is set to logic 1, a new PSL is accepted when the same PSL value is detected in the C2 byte for five consecutive frames. When PSL5 is set to logic 0, a new PSL is accepted when the same PSL value is detected in the C2 byte for three consecutive frames.

PLMEND

The payload label mismatch removal (PLMEND) bit controls the removal of a PLM-P defect when an UNEQ-P defect is declared. When PLMEND is set to logic 1, a PLM-P defect is terminated when an UNEQ-P defect is declared. When PLMEND is set to logic 0, a PLM-P defect is not terminated when an UNEQ-P defect is declared.

PRDI10

The path remote defect indication detection (PRDI10) bit selects the path RDI and path ERDI persistence. When PRDI10 is set to logic 1, path RDI and path ERDI are accepted when the same pattern is detected in bits 5,6,7 of the G1 byte for ten consecutive frames. When PRDI10 is set to logic 0, path RDI and path ERDI are accepted when the same pattern is detected in bits 5,6,7 of the G1 byte for five consecutive frames.

PBIPEBLKACC

The path block BIP-8 errors accumulation (PBIPEBLKACC) bit controls the accumulation of path BIP-8 errors. When PBIPEBLKACC is set to logic 1, the path BIP-8 error accumulation represents block BIP-8 errors (a maximum of 1 error per frame). When PBIPEBLKACC is set to logic 0, the path BIP-8 error accumulation represents BIP-8 errors (a maximum of 8 errors per frame).

PBIPECNTBLK

The path block BIP-8 errors count (PBIPECNTBLK) bit controls the way path BIP-8 errors are reported to the SARC. If PBIPECNTBLK is set to logic 1, BIP-8 errors are counted on a block basis, incremented only once for one or more BIP-8 errors. When PBIPECNTBLK is set to logic 0, the number of incorrect bits in the BIP-8 are reported (maximum of 8).

B3EBLK

The serial path block BIP-8 errors count (B3EBLK) bit controls the way path BIP-8 errors are reported via the B3E output stream. If B3EBLK is set to logic 1, BIP-8 errors are counted on a block basis, incremented only once for one or more BIP-8 errors. When B3EBLK is set to logic 0, the number of incorrect bits in the BIP-8 are reported (maximum of 8).

PREIBLKACC

The path block REI errors accumulation (PREIBLKACC) bit controls the accumulation of path REI errors from the path status (G1) byte. When PREIBLKACC is set to logic 1, the extracted path REI errors are interpreted as block BIP-8 errors (a maximum of 1 error per frame). When PREIBLKACC is set to logic 0, the extracted path REI errors are interpreted as BIP-8 errors (a maximum of 8 errors per frame).

IBER

The inband error reporting (IBER) bit controls the inband regeneration of the path status (G1) byte. When IBER is set to logic 1, the path status byte is updated with the REI-P and the ERDI-P defects that must be returned to the far end. This application is normally used along with APS ports usage. When IBER is set to logic 0, the path status byte is not altered.

IPREIBLK

The inband path REI block errors (IPREIBLK) bit controls the regeneration of the path REI errors in the path status (G1) byte. When IPREIBLK is set to logic 1, the path REI is updated with block BIP-8 errors (a maximum of 1 error per frame). When IPREIBLK is set to logic 0, the path REI is updated with BIP-8 errors (a maximum of 8 errors per frame).

Indirect Register 02H: RHPP Pointer Value and ERDI

Bit	Type	Function	Default
Bit 15	R	PERDIV[2]	X
Bit 14	R	PERDIV[1]	X
Bit 13	R	PERDIV[0]	X
Bit 12	—	Unused	X
Bit 11	R	SSV[1]	X
Bit 10	R	SSV[0]	X
Bit 9	R	PTRV[9]	X
Bit 8	R	PTRV[8]	X
Bit 7	R	PTRV[7]	X
Bit 6	R	PTRV[6]	X
Bit 5	R	PTRV[5]	X
Bit 4	R	PTRV[4]	X
Bit 3	R	PTRV[3]	X
Bit 2	R	PTRV[2]	X
Bit 1	R	PTRV[1]	X
Bit 0	R	PTRV[0]	X

The Pointer Value Indirect Register is provided at RHPP r/w address 02H.

PTRV[9:0]

The path pointer value (PTRV[9:0]) bits represent the current STS pointer being processed by the pointer interpreter state machine or by the concatenation pointer interpreter state machine.

SSV[1:0]

The SS value (SSV[1:0]) bits represent the current SS (DD) bits being processed by the pointer interpreter state machine or by the concatenation pointer interpreter state machine.

PERDIV[2:0]

The path enhanced remote defect indication value (PERDIV[2:0]) bits represent the filtered path enhanced remote defect indication value. PERDIV[2:0] is updated when the same ERDI pattern is detected in bits 5,6,7 of the G1 byte for five or ten consecutive frames (selectable with the PRDI10 register bit).

Indirect Register 03H: RHPP Captured and Accepted PSL

Bit	Type	Function	Default
Bit 15	R	CPSLV[7]	X
Bit 14	R	CPSLV[6]	X
Bit 13	R	CPSLV[5]	X
Bit 12	R	CPSLV[4]	X
Bit 11	R	CPSLV[3]	X
Bit 10	R	CPSLV[2]	X
Bit 9	R	CPSLV[1]	X
Bit 8	R	CPSLV[0]	X
Bit 7	R	APSLV[7]	X
Bit 6	R	APSLV[6]	X
Bit 5	R	APSLV[5]	X
Bit 4	R	APSLV[4]	X
Bit 3	R	APSLV[3]	X
Bit 2	R	APSLV[2]	X
Bit 1	R	APSLV[1]	X
Bit 0	R	APSLV[0]	X

The Accepted PSL and ERDI Indirect Register is provided at RHPP r/w address 03H.

APSLV[7:0]

The accepted path signal label value (APSLV[7:0]) bits represent the last accepted path signal label value. APSLV is updated differently depending on how the ALGO2 bit in RHPP indirect register 01H is set. When ALGO2 is logic 1, a new PSL is accepted when the same PSL value is detected in the C2 byte for three or five consecutive frames. (selectable with the PSL5 register bit). When ALGO2 is logic 0, APSLV is updated every time a new PSL is received. Note that there is no concept of "accepted" path signal label in Algorithm 1, so this register should only be used when ALGO2 is logic 1.

CPSLV[7:0]

The captured path signal label value (CPSLV[7:0]) bits represent the last captured path signal label value. A new PSL is captured every frame from the C2 byte.

Indirect Register 04H: RHPP Expected PSL and PDI

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R/W	PDIRANGE	0
Bit 12	R/W	PDI[4]	0
Bit 11	R/W	PDI[3]	0
Bit 10	R/W	PDI[2]	0
Bit 9	R/W	PDI[1]	0
Bit 8	R/W	PDI[0]	0
Bit 7	R/W	EPSL[7]	0
Bit 6	R/W	EPSL[6]	0
Bit 5	R/W	EPSL[5]	0
Bit 4	R/W	EPSL[4]	0
Bit 3	R/W	EPSL[3]	0
Bit 2	R/W	EPSL[2]	0
Bit 1	R/W	EPSL[1]	0
Bit 0	R/W	EPSL[0]	0

The Expected PSL and PDI Indirect Register is provided at RHPP r/w indirect address 04H.

EPSL[7:0]

The expected path signal label (EPSL[7:0]) bits represent the expected path signal label. The expected PSL and the expected PDI validate the received or the accepted PSL to declare PLM-P, UNEQ-P and PDI-P defects according to Table 4.

PDI[4:0], PDIRANGE

The payload defect indication (PDI[4:0]) bits and the payload defect indication range (PDIRANGE) bit determine the expected payload defect indication according to Table 5 When PDIRANGE is set to logic 1, the PDI range is enabled and the expected PDI range is from E1H to E0H+PDI[4:0]. When PDIRANGE is set to logic 0, the PDI range is disabled and the expected PDI value is E0H+PDI[4:0]. The expected PSL and the expected PDI validate the received or the accepted PSL to declare PLM-P, UNEQ-P and PDI-P defects according to Table 4.

Indirect Register 05H: RHPP Pointer Interpreter Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R	NDF	X
Bit 5	—	Unused	X
Bit 4	R	INVNDF	X
Bit 3	R	DISCOPA	X
Bit 2	R	CONCAT	X
Bit 1	R	ILLJREQ	X
Bit 0	—	Unused	X

The Pointer Interpreter Status Indirect Register is provided at RHPP r/w indirect address 05H.

ILLJREQ

The illegal pointer justification request (ILLJREQ) signal is set high when a positive and/or negative pointer adjustment is received within three frames of a pointer justification event (inc_ind, dec_ind) or an NDF triggered active offset adjustment (NDF_enable). This bit is only valid for master timeslots. It is not valid for slave (concatenated) timeslots.

CONCAT

The CONCAT bit is set high if the H1 and H2 pointer bytes received matches the concatenation indication (one of the five NDF_enable patterns in the NDF field, don't care in the size field, and all-ones in the pointer offset field).

DISCOPA

The discontinuous change of pointer alignment (DISCOPA) signal is set high when there is a pointer adjustment due to receiving a pointer repeated three times. This bit is only valid for master timeslots. It is not valid for slave (concatenated) timeslots.

INVNDF

The invalid new data flag (INVNDF) signal is set high when an invalid NDF code is received. This bit is only valid for master timeslots. It is not valid for slave (concatenated) timeslots.NDF

The new data flag (NDF) signal is set high when an enabled New Data Flag is received indicating a pointer adjustment (NDF_enabled indication). This bit is only valid for master timeslots. It is not valid for slave (concatenated) timeslots.

Indirect Register 06H: RHPP Path BIP Error Counter

Bit	Type	Function	Default
Bit 15	R	PBIPE[15]	X
Bit 14	R	PBIPE[14]	X
Bit 13	R	PBIPE[13]	X
Bit 12	R	PBIPE[12]	X
Bit 11	R	PBIPE[11]	X
Bit 10	R	PBIPE[10]	X
Bit 9	R	PBIPE[9]	X
Bit 8	R	PBIPE[8]	X
Bit 7	R	PBIPE[7]	X
Bit 6	R	PBIPE[6]	X
Bit 5	R	PBIPE[5]	X
Bit 4	R	PBIPE[4]	X
Bit 3	R	PBIPE[3]	X
Bit 2	R	PBIPE[2]	X
Bit 1	R	PBIPE[1]	X
Bit 0	R	PBIPE[0]	X

The RHPP Path BIP Error Counter register is provided at RHPP r/w indirect address 06H.

PBIPE[15:0]

The path BIP error (PBIPE[15:0]) bits represent the number of path BIP errors that have been detected in the B3 byte since the last accumulation interval. The error counters are transferred to the holding registers by a microprocessor write to the RHPP Counters Update register (Address 203H, 283H, 303H, 383H). The TIP output indicates the transfer status.

Indirect Register 07H: RHPP Path REI Error Counter

Bit	Type	Function	Default
Bit 15	R	PREIE[15]	X
Bit 14	R	PREIE[14]	X
Bit 13	R	PREIE[13]	X
Bit 12	R	PREIE[12]	X
Bit 11	R	PREIE[11]	X
Bit 10	R	PREIE[10]	X
Bit 9	R	PREIE[9]	X
Bit 8	R	PREIE[8]	X
Bit 7	R	PREIE[7]	X
Bit 6	R	PREIE[6]	X
Bit 5	R	PREIE[5]	X
Bit 4	R	PREIE[4]	X
Bit 3	R	PREIE[3]	X
Bit 2	R	PREIE[2]	X
Bit 1	R	PREIE[1]	X
Bit 0	R	PREIE[0]	X

The RHPP Path REI Error Counter register is provided at RHPP r/w indirect address 07H.

PREIE[15:0]

The path REI error (PREIE[15:0]) bits represent the number of path REI errors that have been extracted from the G1 byte since the last accumulation interval. The error counters are transferred to the holding registers by a microprocessor write to the RHPP Counters Update register (Address 203H, 283H, 303H, 383H). The TIP output indicates the transfer status.

Indirect Register 08H: RHPP Path Negative Justification Event Counter

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	R	PNJE[12]	X
Bit 11	R	PNJE[11]	X
Bit 10	R	PNJE[10]	X
Bit 9	R	PNJE[9]	X
Bit 8	R	PNJE[8]	X
Bit 7	R	PNJE[7]	X
Bit 6	R	PNJE[6]	X
Bit 5	R	PNJE[5]	X
Bit 4	R	PNJE[4]	X
Bit 3	R	PNJE[3]	X
Bit 2	R	PNJE[2]	X
Bit 1	R	PNJE[1]	X
Bit 0	R	PNJE[0]	X

The RHPP Path Negative Justification Event Counter register is provided at RHPP r/w indirect address 08H.

PNJE[12:0]

The Path Negative Justification Event (PNJE[12:0]) bits represent the number of Path Negative Justification Events that have occurred since the last accumulation interval. The event counters are transferred to the holding registers by a microprocessor write to RHPP Counters Update register (address 203H, 283H, 303H, 383H). The TIP output indicates the transfer status.

Indirect Register 09H: RHPP Path Positive Justification Event Counter

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	R	PPJE[12]	X
Bit 11	R	PPJE[11]	X
Bit 10	R	PPJE[10]	X
Bit 9	R	PPJE[9]	X
Bit 8	R	PPJE[8]	X
Bit 7	R	PPJE[7]	X
Bit 6	R	PPJE[6]	X
Bit 5	R	PPJE[5]	X
Bit 4	R	PPJE[4]	X
Bit 3	R	PPJE[3]	X
Bit 2	R	PPJE[2]	X
Bit 1	R	PPJE[1]	X
Bit 0	R	PPJE[0]	X

The RHPP Path Positive Justification Event Counter register is provided at RHPP r/w indirect address 09H.

PPJE[12:0]

The Path Positive Justification Event (PPJE[12:0]) bits represent the number of Path Positive Justification Events that have occurred since the last accumulation interval. The event counters are transferred to the holding registers by a microprocessor write to RHPP Counters Update register (address 203H, 283H, 303H, 383H). The TIP output indicates the transfer status.

Register 0102H 0502H 0902H 0D02H: RHPP Reserved

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved1	0
Bit 2	R/W	Reserved1	0
Bit 1	R/W	Reserved1	0
Bit 0	R/W	Reserved1	0

The RHPP Reserved Register is provided at RHPP r/w address 02H.

Reserved1

The Reserved1 bits must be set to logic 1 for proper operation.

Reserved

The Reserved bits must be set to logic 0 for proper operation.

Register 0103H 0503H 0903H 0D03H: RHPP Counters Update

Bit	Type	Function	Default
Bit 15	W	Unused	X
Bit 14	W	Unused	X
Bit 13	W	Unused	X
Bit 12	W	Unused	X
Bit 11	W	Unused	X
Bit 10	W	Unused	X
Bit 9	W	Unused	X
Bit 8	W	Unused	X
Bit 7	W	Unused	X
Bit 6	W	Unused	X
Bit 5	W	Unused	X
Bit 4	W	Unused	X
Bit 3	W	Unused	X
Bit 2	W	Unused	X
Bit 1	W	Unused	X
Bit 0	W	Unused	X

Any write to an RHPP Counters Update Register (address 0103H, 0503H, 0903H, 0D03H) will trigger the transfer of all counter values, for that particular STS-12 slice, to their holding registers. To update all counters in this manner, all four slices registers must be written. This is equivalent to writing to register 0002H, the Global Performance Monitor Update register. The TIP register bit (register 0002H) indicates the transfer status.

Register 0104H 0504H 0904H 0D04H: RHPP Path Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	P_INT[12]	X
Bit 10	R	P_INT[11]	X
Bit 9	R	P_INT[10]	X
Bit 8	R	P_INT[9]	X
Bit 7	R	P_INT[8]	X
Bit 6	R	P_INT[7]	X
Bit 5	R	P_INT[6]	X
Bit 4	R	P_INT[5]	X
Bit 3	R	P_INT[4]	X
Bit 2	R	P_INT[3]	X
Bit 1	R	P_INT[2]	X
Bit 0	R	P_INT[1]	X

The RHPP Path Interrupt Status Register is provided at RHPP read address 04H.

P_INT[1:12]

The Path Interrupt Status bit (P_INT[1:12]) indicates which path(s) have interrupts that are still active. Reading from this register will not clear any of the interrupts. P_INT[1:12] has been added to reduce the average number of accesses required to service interrupts.

Register 0105H 0505H 0905H 0D05H: RHPP Pointer Concatenation Processing Disable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	PTRCDIS[12]	0
Bit 10	R/W	PTRCDIS[11]	0
Bit 9	R/W	PTRCDIS[10]	0
Bit 8	R/W	PTRCDIS[9]	0
Bit 7	R/W	PTRCDIS[8]	0
Bit 6	R/W	PTRCDIS[7]	0
Bit 5	R/W	PTRCDIS[6]	0
Bit 4	R/W	PTRCDIS[5]	0
Bit 3	R/W	PTRCDIS[4]	0
Bit 2	R/W	PTRCDIS[3]	0
Bit 1	R/W	PTRCDIS[2]	0
Bit 0	R/W	PTRCDIS[1]	0

The Pointer Concatenation Processing Disable Register is provided at RHPP r/w address 05H.

PTRCDIS[1:12]

The concatenation pointer processing disable (PTRCDIS[1:12]) bits disable the path concatenation pointer interpreter state machine. When PTRCDIS[n] is set to logic 1, the path concatenation pointer interpreter state machine (for the path n) is disabled and excluded from the LOPC-P, AISC-P and ALLAISC-P defect declaration. When PTRCDIS is set to logic 0, the path concatenation pointer interpreter state machine is enabled and included in the LOPC-P, AISC-P and ALLAISC-P defect declaration.

Register 0108H 0110H 0118H 0120H 0128H 0130H 0138H 0140H 0148H 0150H 0158H 0160H 0508H 0510H 0518H 0520H 0528H 0530H 0538H 0540H 0548H 0550H 0558H 0560H 0908H 0910H 0918H 0920H 0928H 0930H 0938H 0940H 0948H 0950H 0958H 0960H 0D08H 0D10H 0D18H 0D20H 0D28H 0D30H 0D38H 0D40H 0D48H 0D50H 0D58H 0D60H: RHPP STS-1/STM-0 #N (Where N=1 to 48) Pointer Interpreter Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R	PAISCV	X
Bit 4	R	PLOPCV	X
Bit 3	R	PAISV	X
Bit 2	R	PLOPV	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

Each address location is linked to one given timeslot in the RHPP blocks. Addresses starting with 01XXH represent timeslots from RHPP #1, 05XXH represent timeslots from RHPP #2, 09XXH represent timeslots from RHPP #3, 0DXXH represent timeslots from RHPP #4. Address locations internal to one given RHPP block are enumerated in their natural order (address XX08H is timeslot 1, XX10H is timeslot 2, XX18H is timeslot 3…).

PLOPV

The path lost of pointer state (PLOPV) bit indicates the current status of the pointer interpreter state machine. PLOPV is set to logic 1 when the state machine is in the LOP_state. PLOPV is set to logic 0 when the state machine is not in the LOP_state.

This bit is only valid for master timeslots.

PAISV

The path alarm indication signal state (PAISV) bit indicates the current status of the pointer interpreter state machine. PAISV is set to logic 1 when the state machine is in the AIS_state. PAISV is set to logic 0 when the state machine is not in the AIS_state.

This bit is only valid for master timeslots.

PLOPCV

The path lost of pointer concatenation state (PLOPCV) bit indicates the current status of the concatenation pointer interpreter state machine. PLOPCV is set to logic 1 when the state machine is in the LOPC_state. PLOPCV is set to logic 0 when the state machine is not in the LOPC_state.

This bit is only valid for slave (concatenated) timeslots.

PAISCV

The path concatenation alarm indication signal state (PAISCV) bit indicates the current status of the concatenation pointer interpreter state machine. PAISCV is set to logic 1 when the state machine is in the AISC_state. PAISCV is set to logic 0 when the state machine is not in the LOPC_state.

This bit is only valid for slave (concatenated) timeslots.

Register 0109H 0111H 0119H 0121H 0129H 0131H 0139H 0141H 0149H 0151H 0159H 0161H 0509H 0511H 0519H 0521H 0529H 0531H 0539H 0541H 0549H 0551H 0559H 0561H 0909H 0911H 0919H 0921H 0929H 0931H 0939H 0941H 0949H 0951H 0959H 0961H 0D09H 0D11H 0D19H 0D21H 0D29H 0D31H 0D39H 0D41H 0D49H 0D51H 0D59H 0D61H: RHPP STS-1/STM-0 #N (where N=1 to 48) Pointer Interpreter Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	PAISCE	0
Bit 4	R/W	PLOPCE	0
Bit 3	R/W	PAISE	0
Bit 2	R/W	PLOPE	0
Bit 1	—	Unused	X
Bit 0	R/W	PTRJEE	0

Each address location is linked to one given timeslot in the RHPP blocks. Addresses starting with 01XXH represent timeslots from RHPP #1, 05XXH represent timeslots from RHPP #2, 09XXH represent timeslots from RHPP #3, 0DXXH represent timeslots from RHPP #4. Address locations internal to one given RHPP block are enumerated in their natural order (address XX08H is timeslot 1, XX10H is timeslot 2, XX18H is timeslot 3…).

PTRJEE

The pointer justification event interrupt enable (PTRJEE) bit controls the activation of the interrupt (INTB) output. When PTRJEE is set to logic 1, the NJEI and PJEI pending interrupt will assert the interrupt (INTB) output. When PTRJEE is set to logic 0, the NJEI and PJEI pending interrupt will not assert the interrupt (INTB) output.

This bit is only valid for master timeslots. In STS-48c/VC-4-16c mode, this bit is only valid for STS-1/STM0 #1 of RHPP #1.

PLOPE

The path loss of pointer interrupt enable (PLOPE) bit controls the activation of the interrupt (INTB) output. When PLOPE is set to logic 1, the PLOPI pending interrupt will assert the interrupt (INTB) output. When PLOPE is set to logic 0, the PLOPI pending interrupt will not assert the interrupt (INTB) output.

This bit is only valid for master timeslots. In STS-48c/VC-4-16c mode, this bit is only valid for STS-1/STM0 #1 of RHPP #1.

PAISE

The path alarm indication signal interrupt enable (PAISE) bit controls the activation of the interrupt (INTB) output. When PAISE is set to logic 1, the PAISI pending interrupt will assert the interrupt (INTB) output. When PAISE is set to logic 0, the PAISI pending interrupt will not assert the interrupt (INTB) output.

This bit is only valid for master timeslots. In STS-48c/VC-4-16c mode, this bit is only valid for STS-1/STM0 #1 of RHPP #1.

PLOPCE

The path loss of pointer concatenation interrupt enable (PLOPCE) bit controls the activation of the interrupt (INTB) output. When PLOPCE is set to logic 1, the PLOPCI pending interrupt will assert the interrupt (INTB) output. When PLOPCE is set to logic 0, the PLOPCI pending interrupt will not assert the interrupt (INTB) output.

This bit is only valid for slave (concatenated) timeslots. In STS-48c/VC-4-16c mode, this bit is valid for all timeslots except STS-1/STM0 #1 of RHPP #1.

PAISCE

The path concatenation alarm indication signal interrupt enable (PAISCE) bit controls the activation of the interrupt (INTB) output. When PAISCE is set to logic 1, the PAISCI pending interrupt will assert the interrupt (INTB) output. When PAISCE is set to logic 0, the PAISCI pending interrupt will not assert the interrupt (INTB) output.

This bit is only valid for slave (concatenated) timeslots. In STS-48c/VC-4-16c mode, this bit is valid for all timeslots except STS-1/STM0 #1 of RHPP #1.

Register 010AH 0112H 011AH 0122H 012AH 0132H 013AH 0142H 014AH 0152H 015AH 0162H 050AH 0512H 051AH 0522H 052AH 0532H 053AH 0542H 054AH 0552H 055AH 0562H 090AH 0912H 091AH 0922H 092AH 0932H 093AH 0942H 094AH 0952H 095AH 0962H 0D0AH 0D12H 0D1AH 0D22H 0D2AH 0D32H 0D3AH 0D42H 0D4AH 0D52H 0D5AH 0D62H: RHPP STS-1/STM-0 #N (where N=1 to 48) Pointer Interpreter Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R	PAISCI	X
Bit 4	R	PLOPCI	X
Bit 3	R	PAISI	X
Bit 2	R	PLOPI	X
Bit 1	R	PJEI	X
Bit 0	R	NJEI	X

Each address location is linked to one given timeslot in the RHPP blocks. Addresses starting with 01XXH represent timeslots from RHPP #1, 05XXH represent timeslots from RHPP #2, 09XXH represent timeslots from RHPP #3, 0DXXH represent timeslots from RHPP #4. Address locations internal to one given RHPP block are enumerated in their natural order (address XX08H is timeslot 1, XX10H is timeslot 2, XX18H is timeslot 3…).

NJEI

The negative pointer justification event interrupt status (NJEI) bit is an event indicator. NJEI is set to logic 1 to indicate a negative pointer justification event. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

This bit is only valid for master timeslots. In STS-48c/VC-4-16c mode, this bit is only valid for STS-1/STM0 #1 of RHPP #1.

PJEI

The positive pointer justification event interrupt status (PJEI) bit is an event indicator. PJEI is set to logic 1 to indicate a positive pointer justification event. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

This bit is only valid for master timeslots. In STS-48c/VC-4-16c mode, this bit is only valid for STS-1/STM0 #1 of RHPP #1.

PLOPI

The path loss of pointer interrupt status (PLOPI) bit is an event indicator. PLOPI is set to logic 1 to indicate any change in the status of PLOPV (entry to the LOP_state or exit from the LOP_state). The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

This bit is only valid for master timeslots. In STS-48c/VC-4-16c mode, this bit is only valid for STS-1/STM0 #1 of RHPP #1.

PAISI

The path alarm indication signal interrupt status (PAISI) bit is an event indicator. PAISI is set to logic 1 to indicate any change in the status of PAISV (entry to the AIS_state or exit from the AIS_state). The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

This bit is only valid for master timeslots. In STS-48c/VC-4-16c mode, this bit is only valid for STS-1/STM0 #1 of RHPP #1.

PLOPCI

The path loss of pointer concatenation interrupt status (PLOPCI) bit is an event indicator. PLOPCI is set to logic 1 to indicate any change in the status of PLOPCV (entry to the LOPC_state or exit from the LOPC_state). The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

This bit is only valid for slave (concatenated) timeslots. In STS-48c/VC-4-16c mode, this bit is valid for all timeslots except STS-1/STM0 #1 of RHPP #1.

PAISCI

The path concatenation alarm indication signal interrupt status (PAISCI) bit is an event indicator. PAISCI is set to logic 1 to indicate any change in the status of PAISCV (entry to the AISC_state or exit from the AISC_state). The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

This bit is only valid for slave (concatenated) timeslots. In STS-48c/VC-4-16c mode, this bit is valid for all timeslots except STS-1/STM0 #1 of RHPP #1.

Register 010BH 0113H 011BH 0123H 012BH 0133H 013BH 0143H 014BH 0153H 015BH 0163H 050BH 0513H 051BH 0523H 052BH 0533H 053BH 0543H 054BH 0553H 055BH 0563H 090BH 0913H 091BH 0923H 092BH 0933H 093BH 0943H 094BH 0953H 095BH 0963H 0D0BH 0D13H 0D1BH 0D23H 0D2BH 0D33H 0D3BH 0D43H 0D4BH 0D53H 0D5BH 0D63H: RHPP STS-1/STM-0 #N (where N=1 to 48) Error Monitor Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R	PERDIV	X
Bit 5	R	PRDIV	X
Bit 4	R	PPDIV	X
Bit 3	R	PUNEQV	X
Bit 2	R	PPLMV	X
Bit 1	R	PPLUV	X
Bit 0	—	Unused	X

Each address location is linked to one given timeslot in the RHPP blocks. Addresses starting with 01XXH represent timeslots from RHPP #1, 05XXH represent timeslots from RHPP #2, 09XXH represent timeslots from RHPP #3, 0DXXH represent timeslots from RHPP #4. Address locations internal to one given RHPP block are enumerated in their natural order (address XX08H is timeslot 1, XX10H is timeslot 2, XX18H is timeslot 3…).

The bits in this register should only be used for master timeslots.

PPLUV

The path payload label unstable status (PPLUV) bit indicates the current status of the PLU-P defect.

Algorithm 1: PPLUV is set to logic 0.

Algorithm 2: PPLUV is set to logic 1 when a total of 5 received PSL differs from the previously accepted PSL without any persistent PSL in between. PPLUV is set to logic 0 when a persistent PSL is found. A persistent PSL is found when the same PSL is received for 3 or 5 consecutive frames.

PPLMV

The path payload label mismatch status (PPLMV) bit indicates the current status of the PLM-P defect.

Algorithm 1: PPLMV is set to logic 1 when the received PSL does not match, according to Table 4, the expected PSL for 3 or 5 consecutive frames (selectable with the PSL5 register bit). PPLMV is set to logic 0 when the received PSL matches, according to , the expected PSL for 3 or 5 consecutive frames.

Algorithm 2: PPLMV is set to logic 1 when the accepted PSL does not match, according to Table 4, the expected PSL. PPLMV is set to logic 0 when the accepted PSL matches, according to Table 4, the expected PSL.

PUNEQV

The path unequipped status (PUNEQV) bit indicates the current status of the UNEQ-P defect. PUNEQV is set to logic 1 when the received PSL indicates unequipped, according to Table 4, for 3 or 5 consecutive frames (selectable with the PSL5 register bit). A PUNEQV is set to logic 0 when the received PSL indicates not unequipped, according to Table 4, for 3 or 5 consecutive frames.

PPDIV

The path payload defect indication status (PPDIV) bit indicates the current status of the PPDI-P defect.

Algorithm 1: PPDIV is set to logic one when the received PSL is a defect, according to Table 4, 3 or 5 consecutive frames (selectable with the PSL5 register bit). PPDIV is set to logic 0 when the received PSL is not a defect, according to Table 4, for 3 or 5 consecutive frames.

Algorithm 2: PPDIV is set to logic 1 when the accepted PSL is a defect according to Table 4. PPDI is set to logic 0 when the accepted PSL is not a defect according to Table 4.

PRDIV

The path remote defect indication status (PRDIV) bit indicates the current status of the RDI-P defect. PRDIV is set to logic 1 when bit 5 of the G1 byte is set high for five or ten consecutive frames (selectable with the PRDI10 register bit). PRDIV is set to logic 0 when bit 5 of the G1 byte is set low for five or ten consecutive frames.

PERDIV

The path enhanced remote defect indication status (PERDIV) bit indicates the current status of the ERDI-P defect. PERDIV is set to logic 1 when the same 010, 100, 101, 110 or 111 pattern is detected in bits 5, 6 and 7 of the G1 byte for five or ten consecutive frames (selectable with the PRDI10 register bit). PERDIV is set to logic 0 when the same 000, 001 or 011 pattern is detected in bits 5, 6 and 7 of the G1 byte for five or ten consecutive frames.

Register 010CH 0114H 011CH 0124H 012CH 0134H 013CH 0144H 014CH 0154H 015CH 0164H 050CH 0514H 051CH 0524H 052CH 0534H 053CH 0544H 054CH 0554H 055CH 0564H 090CH 0914H 091CH 0924H 092CH 0934H 093CH 0944H 094CH 0954H 095CH 0964H 0D0CH 0D14H 0D1CH 0D24H 0D2CH 0D34H 0D3CH 0D44H 0D4CH 0D54H 0D5CH 0D64H: RHPP STS-1/STM-0 #N (where N=1 to 48) Error Monitor Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R/W	PREIEE	0
Bit 8	R/W	PBIPEE	0
Bit 7	R/W	COPERDIE	0
Bit 6	R/W	PERDIE	0
Bit 5	R/W	PRDIE	0
Bit 4	R/W	PPDIE	0
Bit 3	R/W	PUNEQE	0
Bit 2	R/W	PPLME	0
Bit 1	R/W	PPLUE	0
Bit 0	R/W	COPSLE	0

Each address location is linked to one given timeslot in the RHPP blocks. Addresses starting with 01XXH represent timeslots from RHPP #1, 05XXH represent timeslots from RHPP #2, 09XXH represent timeslots from RHPP #3, 0DXXH represent timeslots from RHPP #4. Address locations internal to one given RHPP block are enumerated in their natural order (address XX08H is timeslot 1, XX10H is timeslot 2, XX18H is timeslot 3…).

The bits in this register should only be used for master timeslots.

COPSLE

The change of path payload signal label interrupt enable (COPSLE) bit controls the activation of the interrupt (INTB) output. When COPSLE is set to logic 1, the COPSLI pending interrupt will assert the interrupt (INTB) output. When COPSLE is set to logic 0, the COPSLI pending interrupt will not assert the interrupt (INTB) output.

PPLUE

The path payload label unstable interrupt enable (PPLUE) bit controls the activation of the interrupt (INTB) output. When PPLUE is set to logic 1, the PPLUI pending interrupt will assert the interrupt (INTB) output. When PPLUE is set to logic 0, the PPLUI pending interrupt will not assert the interrupt (INTB) output.

PPLME

The path payload label mismatch interrupt enable (PPLME) bit controls the activation of the interrupt (INTB) output. When PPLME is set to logic 1, the PPLMI pending interrupt will assert the interrupt (INTB) output. When PPLME is set to logic 0, the PPLMI pending interrupt will not assert the interrupt (INTB) output.

PUNEQE

The path payload unequipped interrupt enable (PUNEQE) bit controls the activation of the interrupt (INTB) output. When PUNEQE is set to logic 1, the PUNEQI pending interrupt will assert the interrupt (INTB) output. When PUNEQE is set to logic 0, the PUNEQI pending interrupt will not assert the interrupt (INTB) output.

PPDIE

The path payload defect indication interrupt enable (PPDIE) bit controls the activation of the interrupt (INTB) output. When PPDIE is set to logic 1, the PPDI pending interrupt will assert the interrupt (INTB) output. When PPDIE is set to logic 0, the PPDI pending interrupt will not assert the interrupt (INTB) output.

PRDIE

The path remote defect indication interrupt enable (PRDIE) bit controls the activation of the interrupt (INTB) output. When PRDIE is set to logic 1, the PRDII pending interrupt will assert the interrupt (INTB) output. When PRDIE is set to logic 0, the PRDII pending interrupt will not assert the interrupt (INTB) output.

PERDIE

The path enhanced remote defect indication interrupt enable (PERDIE) bit controls the activation of the interrupt (INTB) output. When PERDIE is set to logic 1, the PERDII pending interrupt will assert the interrupt (INTB) output. When PERDIE is set to logic 0, the PERDII pending interrupt will not assert the interrupt (INTB) output.

COPERDIE

The change of path enhanced remote defect indication interrupt enable (COPERDIE) bit controls the activation of the interrupt (INTB) output. When COPERDIE is set to logic 1, the COPERDII pending interrupt will assert the interrupt (INTB) output. When COPERDIE is set to logic 0, the COPERDII pending interrupt will not assert the interrupt (INTB) output.

PBIPEE

The path BIP-8 error interrupt enable (PBIPEE) bit controls the activation of the interrupt (INTB) output. When PBIPEE is set to logic 1, the PBIPEI pending interrupt will assert the interrupt (INTB) output. When PBIPEE is set to logic 0, the PBIPEI pending interrupt will not assert the interrupt (INTB) output.

PREIEE

The path REI error interrupt enable (PREIEE) bit controls the activation of the interrupt (INTB) output. When PREIEE is set to logic 1, the PREIEI pending interrupt will assert the interrupt (INTB) output. When PREIEE is set to logic 0, the PREIEI pending interrupt will not assert the interrupt (INTB) output.

Register 010DH 0115H 011DH 0125H 012DH 0135H 013DH 0145H 014DH 0155H 015DH 0165H 050DH 0515H 051DH 0525H 052DH 0535H 053DH 0545H 054DH 0555H 055DH 0565H 090DH 0915H 091DH 0925H 092DH 0935H 093DH 0945H 094DH 0955H 095DH 0965H 0D0DH 0D15H 0D1DH 0D25H 0D2DH 0D35H 0D3DH 0D45H 0D4DH 0D55H 0D5DH 0D65H: RHPP STS-1/STM-0 #N (where N=1 to 48) Error Monitor Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R	PREIEI	X
Bit 8	R	PBIPEI	X
Bit 7	R	COPERDII	X
Bit 6	R	PERDII	X
Bit 5	R	PRDII	X
Bit 4	R	PPDII	X
Bit 3	R	PUNEQI	X
Bit 2	R	PPLMI	X
Bit 1	R	PPLUI	X
Bit 0	R	COPSLI	X

Each address location is linked to one given timeslot in the RHPP blocks. Addresses starting with 01XXH represent timeslots from RHPP #1, 05XXH represent timeslots from RHPP #2, 09XXH represent timeslots from RHPP #3, 0DXXH represent timeslots from RHPP #4. Address locations internal to one given RHPP block are enumerated in their natural order (address XX08H is timeslot 1, XX10H is timeslot 2, XX18H is timeslot 3…).

The bits in this register should only be used for master timeslots.

COPSLI

The change of path payload signal label interrupt status (COPSLI) bit is an event indicator. COPSLI is set to logic 1 to indicate a new PSL-P value. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

ALGO2 register bit has no effect on COPSLI.

PPLUI

The path payload label unstable interrupt status (PPLUI) bit is an event indicator. PPLUI is set to logic 1 to indicate any change in the status of PPLUV (stable to unstable or unstable to stable). The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

PPLMI

The path payload label mismatch interrupt status (PPLMI) bit is an event indicator. PPLMI is set to logic 1 to indicate any change in the status of PPLMV (match to mismatch or mismatch to match). The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

PUNEQI

The path payload unequipped interrupt status (PUNEQI) bit is an event indicator. PUNEQI is set to logic 1 to indicate any change in the status of PUNEQV (equipped to unequipped or unequipped to equipped). The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

PPDII

The path payload defect indication interrupt status (PPDII) bit is an event indicator. PPDII is set to logic 1 to indicate any change in the status of PPDIV (no defect to payload defect or payload defect to no defect). The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

PRDII

The path remote defect indication interrupt status (PRDII) bit is an event indicator. PRDII is set to logic 1 to indicate any change in the status of PRDIV (no defect to RDI defect or RDI defect to no defect). The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

PERDII

The path enhanced remote defect indication interrupt status (PERDII) bit is an event indicator. PERDII is set to logic 1 to indicate any change in the status of PERDIV (no defect to ERDI defect or ERDI defect to no defect). The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

COPERDII

The change of path enhanced remote defect indication interrupt status (COPERDII) bit is an event indicator. COPERDII is set to logic 1 to indicate a new ERDI-P value. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

PBIPEI

The path BIP-8 error interrupt status (PBIPEI) bit is an event indicator. PBIPEI is set to logic 1 to indicate a path BIP-8 error. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

PREIEI

The path REI error interrupt status (PREIEI) bit is an event indicator. PREIEI is set to logic 1 to indicate a path REI error. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

Register 0200H 0600H 0A00H 0E00H: RSVCA Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer. Refer to Section 13.8 for details on RSVCA indirect register access.

Path[3:0]	STS-1/STM-0 Path #
0000	Invalid path
0001-1100	Path #1 to Path #12
1101-1110	Invalid path
1111	Invalid path

IADDR[1:0]

The address location (IADDR[1:0]) bits select which address location is accessed by the current indirect transfer. Refer to Section 13.8 for details on RSVCA indirect register access

IADDR[1:0]	Indirect Register
00	SVCA Outgoing Pointer Justification Performance Monitor
01	SVCA Outgoing Negative Justification Performance Monitor
10	SVCA Diagnostic/Configuration Register
11	Unused

RWB

The active high read and active low write (RWB) bit selects if the current access to an internal register is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to a register. When RWB is set to logic 1, an indirect read access to a register is initiated. The data from the addressed location as indicated using the IADDR field will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to a register is initiated. The data from the Indirect Data Register will be transferred to the addressed register.

BUSY

The active high busy (BUSY) bit reports if a previously initiated indirect access to an internal register has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0 upon completion of the access. This register should be polled to determine when new data is available in the Indirect Data Register.

Register 0201H 0601H 0A01H 0E01H: RSVCA Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from an indirect register during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the register will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the register. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

Register 0202H 0602H 0A02H 0E02H: RSVCA Reserved #1

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved1	0
Bit 2	R/W	Reserved1	0
Bit 1	R/W	Reserved1	0
Bit 0	R/W	Reserved1	0

The RSVCA Reserved #1 Register is provided at RSVCA r/w address 02H.

Reserved1

The Reserved1 bits must be set to logic 1 for proper operation.

Reserved

The Reserved bits must be set to logic 0 for proper operation.

Register 0203H 0603H 0A03H 0E03H: RSVCA Positive Justification Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	PPJI[4]	X
Bit 2	R	PPJI[3]	X
Bit 1	R	PPJI[2]	X
Bit 0	R	PPJI[1]	X

PPJI[4:1]

The positive pointer justification interrupt status (PPJI[4:1]) bits are event indicators for STS-1/STM-0 paths/timeslots #1 to #4. PPJI[4:1] are set to logic 1 to indicate a positive pointer justification event in the outgoing data stream. These interrupt status bits are independent of the interrupt enable bits. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears this bit.

Register 0204H 0604H 0A04H 0E04H: RSVCA Negative Justification Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	NPJI[4]	X
Bit 2	R	NPJI[3]	X
Bit 1	R	NPJI[2]	X
Bit 0	R	NPJI[1]	X

NPJI[4:1]

The negative pointer justification interrupt status (NPJI[4:1]) bits are event indicators for STS-1/STM-0 paths/timeslots #1 to #4. NPJI[4:1] are set to logic 1 to indicate a negative pointer justification event in the outgoing data stream. These interrupt status bits are independent of the interrupt enable bits. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears this bit.

Register 0205H 0605H 0A05H 0E05H: RSVCA FIFO Overflow Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	FOVRI[4]	X
Bit 2	R	FOVRI[3]	X
Bit 1	R	FOVRI[2]	X
Bit 0	R	FOVRI[1]	X

FOVRI[4:1]

The FIFO overflow event interrupt status (FOVRI[4:1]) bits are event indicators for STS-1/STM-0 paths/timeslots #1 to #4. FOVRI[4:1] are set to logic 1 to indicate a FIFO overflow event. These interrupt status bits are independent of the interrupt enable bits. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears this bit.

Register 0206H 0606H 0A06H 0E06H: RSVCA FIFO Underflow Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	FUDRI[4]	X
Bit 2	R	FUDRI[3]	X
Bit 1	R	FUDRI[2]	X
Bit 0	R	FUDRI[1]	X

FUDRI[4:1]

The FIFO underflow event interrupt status (FUDR[4:1]) bits are event indicators for STS-1/STM-0 paths/timeslots #1 to #4. FUDRI[4:1] are set to logic 1 to indicate a FIFO underflow event. These interrupt status bits are independent of the interrupt enable bits. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears this bit.

Register 0207H 0607H 0A07H 0E07H: RSVCA Pointer Justification Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	PJIEN[4]	0
Bit 2	R/W	PJIEN[3]	0
Bit 1	R/W	PJIEN[2]	0
Bit 0	R/W	PJIEN[1]	0

PJIEN[4:1]

The pointer justification event interrupt enable (PJIEN[4:1]) bits control the activation of the interrupt (INT) output for STS-1/STM-0 paths/timeslots #1 to #4. When any of these bit locations is set to logic 1, the corresponding pending interrupt will assert the interrupt (INT) output. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INT) output. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears this bit.

Register 0208H 0608H 0A08H 0E08H: RSVCA FIFO Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	FIEN[4]	0
Bit 2	R/W	FIEN[3]	0
Bit 1	R/W	FIEN[2]	0
Bit 0	R/W	FIEN[1]	0

FIEN[4:1]

The FIFO event interrupt enable (FIEN[4:1]) bits control the activation of the interrupt (INT) output for STS-1/STM-0 paths/timeslots #1 to #4 caused by a FIFO overflow or a FIFO underflow. When any of these bit locations is set to logic 1, the corresponding pending interrupt will assert the interrupt (INT) output. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INT) output. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears this bit.

Register 0209H 0609H 0A09H 0E09H: RSVCA Reserved #2

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	1
Bit 13	R/W	Reserved	1
Bit 12	R/W	Reserved	1
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	1
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

Reserved

All Reserved bits must be set to their default value for proper operation.

Register 020AH 060AH 0A0AH 0E0AH: RSVCA Reserved #3

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Register 020BH 060BH 0A0BH 0E0BH: RSVCA Performance Monitor Trigger

Any write to this register triggers a transfer of all local RSVCA performance monitor counters to holding registers that can be read by the microprocessor interface. This is a write only register.

Indirect Register 00H: RSVCA Positive Justifications Performance Monitor

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	R	PJPMON[12]	0
Bit 11	R	PJPMON[11]	0
Bit 10	R	PJPMON[10]	0
Bit 9	R	PJPMON[9]	0
Bit 8	R	PJPMON[8]	0
Bit 7	R	PJPMON[7]	0
Bit 6	R	PJPMON[6]	0
Bit 5	R	PJPMON[5]	0
Bit 4	R	PJPMON[4]	0
Bit 3	R	PJPMON[3]	0
Bit 2	R	PJPMON[2]	0
Bit 1	R	PJPMON[1]	0
Bit 0	R	PJPMON[0]	0

PJPMON[12:0]

This register reports the number of positive pointer justification events that occurred on the outgoing side in the previous accumulation interval. The content of this register becomes valid after a transfer is triggered by writing to the RSVCA Performance Monitor Trigger register (0x020B, 0x060B, 0x0A0B, 0x0E0B) or the S/UNI MULTI-48 Global Performance Monitor Update register (0002H).

Note that the PJPMON[12:0] count value is only valid for STS-N master timeslots.

Indirect Register 01H: RSVCA Negative Justifications Performance Monitor

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	R	NJPMON[12]	0
Bit 11	R	NJPMON[11]	0
Bit 10	R	NJPMON[10]	0
Bit 9	R	NJPMON[9]	0
Bit 8	R	NJPMON[8]	0
Bit 7	R	NJPMON[7]	0
Bit 6	R	NJPMON[6]	0
Bit 5	R	NJPMON[5]	0
Bit 4	R	NJPMON[4]	0
Bit 3	R	NJPMON[3]	0
Bit 2	R	NJPMON[2]	0
Bit 1	R	NJPMON[1]	0
Bit 0	R	NJPMON[0]	0

NJPMON[12:0]

This register reports the number of negative pointer justification events that occurred on the outgoing side in the previous accumulation interval. The content of this register becomes valid after a transfer is triggered by writing to the RSVCA Performance Monitor Trigger register (0x020B, 0x060B, 0x0A0B, 0x0E0B) or the S/UNI MULTI-48 Global Performance Monitor Update register (0002H).

Note that the NJPMON[12:0] count value is only valid for STS-N master timeslots.

Indirect Register 02H: RSVCA Diagnostic/Configuration

Bit	Type	Function	Default
Bit 15	R/W	PTRRST	0
Bit 14	R/W	PTRSS[1]	0
Bit 13	R/W	PTRSS[0]	0
Bit 12	R/W	JUST3DIS	0
Bit 11	R/W	PTRDD[1]	0
Bit 10	R/W	PTRDD[0]	0
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R/W	Reserved	0
Bit 5	R/W	Diag_NDFREQ	0
Bit 4	R/W	Diag_FifoAISDis	0
Bit 3	R/W	Diag_PAIS	0
Bit 2	R/W	Diag_LOP	0
Bit 1	R/W	Diag_NegJust	0
Bit 0	R/W	Diag_PosJust	0

The RSVCA Diagnostic/Configuration Register is provided at RSVCA read/write indirect address 02H. These bits should be set to their default values during normal operation of the RSVCA. When configured for concatenated payloads, the value written to the master timeslot is automatically propagated to all the slave timeslots.

Diag_PosJust

The Diag_PosJust bit forces the RSVCA to generate outgoing positive justification events. When set to 1, the RSVCA generates positive justification events at the rate of one every four frames regardless of the current level of the internal FIFO. Note that the RSVCA will follow up with an automatic negative pointer justification if it needs to do so in order to keep its FIFO fill levels under control. The diagnostic feature has a lower priority than the FIFO monitor

Diag_PosJust and Diag_NegJust must not be set to one at the same time. If that occurs, their operation is disabled.

Diag_NegJust

The Diag_NegJust bit forces the RSVCA to generate outgoing negative justification events. When set to 1, the RSVCA generates negative justification events at the rate of one every four frames regardless of the current level of the internal FIFO. Note that the RSVCA will follow up with an automatic negative pointer justification if it needs to do so in order to keep its FIFO fill levels under control. The diagnostic feature has a lower priority than the FIFO monitor

Diag_PosJust and Diag_NegJust must not be set to one at the same time. If that occurs, their operation is disabled.

Diag_LOP

When set high, the Diag_LOP bit forces the RSVCA to invert the outgoing NDF field of the payload (selected path(s)) pointer causing downstream pointer processing elements to enter a loss of pointer (LOP) state.

Diag_PAIS

When set high, the Diag_PAIS bit forces the RSVCA to insert path AIS in the selected outgoing stream for at least three consecutive frames. AIS is inserted by writing an all ones pattern in the transport overhead bytes H1, H2, and H3, as well as in the entire STS synchronous payload envelope. The first frame after PAIS negates will contain a new data flag in the transport overhead H1 byte.

Diag_FifoAISDis

When set high, the Diag_FifoAISDis bit forces the RSVCA not to insert path AIS upon FIFO overflow/underflow detection. When set low (normal operation), detection of FIFO overflow/underflow causes path AIS to be inserted in the outgoing stream for at least three consecutive frames.

Note: When Diag_FifoAISDis is enabled, any overflow or underflow will cause the RSVCA to declare both FUDR and FOVR interrupts.

Diag_NDFREQ

When set high, the Diag_NDFREQ bit forces the RSVCA to insert a NEW DATA FLAG indication in the frame regardless of the state of the pointer generation state machine. This bit should be set for less than one frame as multiple NDF will otherwise cause the downstream pointer processor to declare LOP.

After any timeslot is reconfigured, the corresponding Diag_NDFREQ bit must be toggled.

PTRDD[1:0]

The PTRDD[1:0] defines the SS bits for the STS-N/AU-N concatenation pointer (may also be known as DD). ITU requirement for DD bits is unspecified when processing AU-4. Note, TELCORDIA does not specify these two bits.

JUST3DIS

When set high, JUST3DIS allows the RSVCA to perform up to 1 justification per frame when necessary. When set to zero, pointer justifications are allowed only every 4 frames.

PTRSS[1:0]

The PTRSS[1:0] defines the STS-N/AU-N pointer bits SS. ITU requires that SS be set to 10 when processing AU-4. Note, TELCORDIA does not specify these two bits. The SS bits are set to 00 when processing a slave STS-1 timeslot.

PTRRST

When set high, incoming and outgoing pointers are reset to their default values. This bit is level sensitive.

Register 0260H 0660H 0A60H 0E60H: SARC Indirect Path Register

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	PATH [3]	0
Bit 2	R/W	PATH [2]	0
Bit 1	R/W	PATH [1]	0
Bit 0	R/W	PATH [0]	0

PATH[3:0]

The STS-1/STM-0 indirect address path (PATH[3:0]) bits select which STS-1/STM-0 path/timeslot is accessed by the next transfer(s) to SARC registers 0268H, 0269H and 026AH. SARC indirect address path (PATH[3:0]) bits must be written to a valid path value before a write access actually transfers data into indirect registers at address 0268H (0668H, 0A68H, 0E68H), 0269H (0669H, 0A69H, 0E69H) and 026AH (066AH, 0A6AH, 0E6AH). Same applies for read accesses to these registers.

When payload type is STS-48c (VC-4-16c), STS-12c (VC-4-4c) or 1xSTS-3c (1xVC-4), only path/timeslot #1 (0001) is valid. When payload type is 4xSTS-3c (4xVC-4), valid path/timeslot range is 1 (0001) to 4 (0100).

PATH[3:0]	STS-1/STM-0 path #
0000	Invalid path
0001	Path #1
0010-0100	Path #2 to Path #4: valid only in 4xSTS-3c mode
0101-1111	Invalid path

Register 0262H 0662H 0A62H 0E62H: SARC Section Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R/W	LRDI22	0
Bit 0	R/W	Reserved	0

The reserved bit in this register should be set to the default value.

LRDI22

The line remote defect indication (LRDI22) bit selects the line RDI persistence when line RDI is asserted as a result of received defects. When LRDI22 is set to logic 1, a new line RDI-L indication is transmitted for at least 22 frames. When LRDI22 is set to logic 0, a new line RDI indication is transmitted for at least 12 frames.

Register 0263H 0663H 0A63H 0E63H: SARC Section SALM Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	SD/LOS/DOOLEN	0
Bit 9	R/W	SFBEREN	0
Bit 8	R/W	SDBEREN	0
Bit 7	R/W	STIMEN	0
Bit 6	R/W	STIUEN	0
Bit 5	R/W	APSBFEN	0
Bit 4	R/W	LRDIEN	0
Bit 3	R/W	LAISEN	0
Bit 2	R/W	LOSEN	0
Bit 1	R/W	LOFEN	0
Bit 0	R/W	OOFEN	0

OOFEN

The OOF enable bit allows the out of frame defect to be OR'ed into the SALM output. When the OOFEN bit is set high, the corresponding defect indication is OR'ed with other defect indications and output on SALM. When the OOFEN bit is set low, the corresponding defect indication does not affect the SALM output.

LOFEN

The LOF enable bit allows the loss of frame defect to be OR'ed into the SALM output. When the LOFEN bit is set high, the corresponding defect indication is OR'ed with other defect indications and output on SALM. When the LOFEN bit is set low, the corresponding defect indication does not affect the SALM output.

LOSEN

The LOS enable bit allows the loss of signal defect to be OR'ed into the SALM output. When the LOSEN bit is set high, the corresponding defect indication is OR'ed with other defect indications and output on SALM. When the LOSEN bit is set low, the corresponding defect indication does not affect the SALM output.

LAISEN

The LAIS enable bit allows the line alarm indication signal defect to be OR'ed into the SALM output. When the LAISEN bit is set high, the corresponding defect indication is ORed with other defect indications and output on SALM. When the LAISEN bit is set low, the corresponding defect indication does not affect the SALM output.

LRDIEN

The LRDI enable bit allows the line remote defect indication defect to be OR'ed into the SALM output. When the LRDIEN bit is set high, the corresponding defect indication is OR'ed with other defect indications and output on SALM. When the LRDIEN bit is set low, the corresponding defect indication does not affect the SALM output.

APSBFEN

The APSBF enable bit allows the APS byte failure defect to be OR'ed into the SALM output. When the APSBFEN bit is set high, the corresponding defect indication is OR'ed with other defect indications and output on SALM. When the APSBFEN bit is set low, the corresponding defect indication does not affect the SALM output.

STIUEN

The STIU enable bit allows the section trace identifier unstable defect to be OR'ed into the SALM output. When the STIUEN bit is set high, the corresponding defect indication is OR'ed with other defect indications and output on SALM. When the STIUEN bit is set low, the corresponding defect indication does not affect the SALM output.

STIMEN

The STIM enable bit allows the section trace identifier mismatch defect to be OR'ed into the SALM output. When the STIMEN bit is set high, the corresponding defect indication is OR'ed with other defect indications and output on SALM. When the STIMEN bit is set low, the corresponding defect indication does not affect the SALM output.

SDBEREN

The SDBER enable bit allows the signal degrade BER defect to be OR'ed into the SALM output. When the SDBEREN bit is set high, the corresponding defect indication is OR'ed with other defect indications and output on SALM. When the SDBEREN bit is set low, the corresponding defect indication does not affect the SALM output.

SFBEREN

The SFBER enable bit allows the signal failure BER defect to be OR'ed into the SALM output. When the SFBEREN bit is set high, the corresponding defect indication is OR'ed with other defect indications and output on SALM. When the SFBEREN bit is set low, the corresponding defect indication does not affect the SALM output.

SD/LOS/DOOLEN

The SD/LOS/DOOL enable bit allows the deassertion of the SD pin or the assertion of LOS or DOOL to be OR'ed into the SALM output. When SD/LOS/DOOLEN is set high, the corresponding defect indication is OR'ed with other defect indications and output on SALM. When the SD/LOS/DOOLEN bit is set low, the corresponding defect indication does not affect the SALM output.

Reserved

The Reserved bit must be set to logic 0 for proper operation.

Register 0264H 0664H 0A64H 0E64H: SARC Section RLAISINS Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	SD/LOS/DOOLEN	0
Bit 9	R/W	SFBEREN	0
Bit 8	R/W	SDBEREN	0
Bit 7	R/W	STIMEN	0
Bit 6	R/W	STIUEN	0
Bit 5	R/W	APSBFEN	0
Bit 4	R/W	LRDIEN	0
Bit 3	R/W	LAISEN	0
Bit 2	R/W	LOSEN	0
Bit 1	R/W	LOFEN	0
Bit 0	R/W	OOFEN	0

OOFEN, LOFEN, LOSEN, LAISEN, LRDIEN, APSBFEN, STIUEN, STIMEN, SDBEREN, SFBEREN, SD/LOS/DOOLEN

The above enable bits allows for the auto insertion of downstream AIS-P based on any or all of the Receive Line defects listed below. A defect is a candidate for the generation if the associated enable bit is set to logic '1'. If it is set to logic '0', it will not be considered. If any bits in this register are set, bit 0, "RLAISINSEN", of register 026AH, "SARC Path RPAISINS Enable," must also be set.

- Out Of Frame (OOF) defect.
- Loss Of Frame (LOF) defect.
- Loss Of Signal (LOS) defect.
- Line Alarm Indication Signal (AIS-L) defect.
- Line Remote Defect Indication (RDI-L) defect.
- APS Byte Failure (APSBF) defect.
- Section Trace Identifier Unstable (STIU) defect.
- Section Trace Identifier Mismatch (STIM) defect.
- Signal Degrade BER (SDBER) defect.
- Signal Failure BER (SFBER) defect.
- SD input pin deassertion, Loss of Signal (LOS) or Receive Data Out of Lock (DOOL) defect assertion.

Reserved

The Reserved bit must be set to logic 0 for proper operation.

Register 0265H 0665H 0A65H 0E65H: SARC Section TLRDIINS Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	SD/LOS/DOOLEN	0
Bit 9	R/W	SFBEREN	0
Bit 8	R/W	SDBEREN	0
Bit 7	R/W	STIMEN	0
Bit 6	R/W	STIUEN	0
Bit 5	R/W	APSBFEN	0
Bit 4	R/W	LRDIEN	0
Bit 3	R/W	LAISEN	0
Bit 2	R/W	LOSEN	0
Bit 1	R/W	LOFEN	0
Bit 0	R/W	OOFEN	0

OOFEN, LOFEN, LOSEN, LAISEN, LRDIEN, APSBFEN, STIUEN, STIMEN, SDBEREN, SFBEREN

The above enable bits allows for the auto assertion of transmit RDI-L based on the following conditions:

- Out Of Frame (OOF) defect.
- Loss Of Frame (LOF) defect.
- Loss Of Signal (LOS) defect.
- Line Alarm Indication Signal (AIS-L) defect.
- Line Remote Defect Indication (RDI-L) defect.
- APS Byte Failure (APSBF) defect.
- Section Trace Identifier Unstable (STIU) defect.
- Section Trace Identifier Mismatch (STIM) defect.
- Signal Degrade BER (SDBER) defect.
- Signal Failure BER (SFBER) defect.
- SD input pin deassertion, Loss of Signal (LOS) or Receive Data Out of Lock (DOOL) defect assertion.

When a given defect enable bit is set high, the corresponding defect indication is OR'ed with other defect indications and the result forces transmission of Line RDI.

Reserved

The Reserved bit must be set to logic 0 for proper operation.

Register 0268H 0668H 0A68H 0E68H: SARC Path Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	PRDIEN	0
Bit 6	R/W	PERDI22	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	PLOPTREND	0
Bit 3	R/W	PAISPTRCFG[1]	0
Bit 2	R/W	PAISPTRCFG[0]	0
Bit 1	R/W	PLOPTRCFG[1]	0
Bit 0	R/W	PLOPTRCFG[0]	0

This register is considered an indirect register. The proper PATH[3:0] bits values must be set in SARC Indirect Path Register prior to accessing this register.

The reserved bit in this register should be set to the default value.

PLOPTRCFG[1:0]

The path loss of pointer configuration (PLOPTRCFG[1:0]) bits define the LOP-P defect. When PLOPTRCFG[1:0] is set to 00b, a LOP-P defect is declared when the pointer is in the LOP state and a LOP-P defect is removed when the pointer is not in the LOP state. When PLOPTRCFG[1:0] is set to 01b, a LOP-P defect is declared when the pointer or any of the concatenated pointers is in the LOP state and a LOP-P defect is removed when the pointer and all the concatenation pointers are not in the LOP state. When PLOPTRCFG[1:0] is set to 10b, a LOP-P defect is declared when the pointer or any of the concatenated pointers is in the LOP state or in the AIS state and a LOP-P defect is removed when the pointer and all the concatenation pointers are not in the LOP state or in the AIS state.

PAISPTRCFG[1:0]

The path AIS pointer configuration (PAISPTRCFG[1:0]) bits define the AIS-P defect. When PAISPTRCFG[1:0] is set to 00b, an AIS-P defect is declared when the pointer is in the AIS state and an AIS-P defect is removed when the pointer is not in the AIS state. When PAISPTRCFG[1:0] is set to 01b, an AIS-P defect is declared when the pointer or any of the concatenated pointers is in the AIS state and an AIS-P defect is removed when the pointer and all the concatenation pointers are not in the AIS state. When PAISPTRCFG[1:0] is set to 10b, an AIS-P defect is declared when the pointer and all the concatenated pointers are in the AIS state and an AIS-P defect is removed when the pointer or any of the concatenation pointers is not in the AIS state.

PLOPTREND

The path loss of pointer removal (PLOPTREND) bit controls the removal of a LOP-P defect when an AIS-P defect is declared. When PLOPTREND is set to logic 1, a LOP-P defect is terminated when an AIS-P defect is declared. When PLOPTREND is set to logic 0, a LOP-P defect is not terminated when an AIS-P defect is declared.

PERDI22

The path enhance remote defect indication (PERDI22) bit selects the path ERDI persistence. When PERDI22 is set to logic 1, a new path ERDI indication is transmitted by the THPP for at least 22 frames. When PERDI22 is set to logic 0, a new path ERDI indication is transmitted by the THPP for at least 12 frames.

PRDIEN

The path remote defect indication enable (PRDIEN) bit selects between the 1 bit RDI code and the 3 bits ERDI code. When PRDIEN is set to logic 1, the 1 bit RDI code is transmitted by the THPP. When PRDIEN is set to logic 0, the 3 bit ERDI code is transmitted by the THPP.

Register 0269H 0669H 0A69H 0E69H: SARC Path RALM Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R/W	PPLMEN	0
Bit 12	R/W	PPLUEN	0
Bit 11	R/W	PTIMEN	0
Bit 10	R/W	PTIUEN	0
Bit 9	R/W	PERDIEN	0
Bit 8	R/W	PRDIEN	0
Bit 7	R/W	PPDIEN	0
Bit 6	R/W	PUNEQEN	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	LCDEN	0
Bit 3	R/W	PAISPTREN	0
Bit 2	R/W	PLOPTREN	0
Bit 1	R/W	MSSALMEN	0
Bit 0	R/W	SALMEN	0

This register is considered an indirect register. The proper PATH[3:0] bits values must be set in SARC Indirect Path Register prior to accessing this register.

The reserved bit in this register should be set to the default value.

SALMEN, MSSALMEN, PLOPTREN, PAISPTREN, LCDEN, PUNEQEN, PPDIEN, PRDIEN, PERDIEN, PTIUEN, PTIMEN, PPLUEN, PPLMEN

The above enable bits allows for the generation of the RALM output based on the following conditions:

- local section alarm (result of register 0263H/0663H/0A63H/0E63H)
- master slice section alarm (result of register 0263H, valid only over slices 2 to 4, in STS-48/STM-16 mode)
- path loss of pointer defect
- path AIS pointer defect
- path payload label unstable defect
- path payload label mismatch defect
- path payload defect indication defect
- path remote defect indication defect
- path enhanced remote defect indication defect
- path trace identifier unstable defect
- path trace identifier mismatch defect
- loss of cell delineation

When the bit is set high, the corresponding defect indication is ORed with other defect indications to generate RALM. When the bit is set low, the corresponding defect indication does not affect RALM.

Register 026AH 066AH 0A6AH 0E6AH: SARC Path RPAISINS Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R/W	PPLMEN	0
Bit 12	R/W	PPLUEN	0
Bit 11	R/W	PTIMEN	0
Bit 10	R/W	PTIUEN	0
Bit 9	R/W	PERDIEN	0
Bit 8	R/W	PRDIEN	0
Bit 7	R/W	PPDIEN	0
Bit 6	R/W	PUNEQEN	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	PAISPTREN	0
Bit 2	R/W	PLOPTREN	0
Bit 1	R/W	MSRLAISINSEN	0
Bit 0	R/W	RLAISINSEN	0

This register is considered an indirect register. The proper PATH[3:0] bits values must be set in SARC Indirect Path Register prior to accessing this register.

All Reserved bits must be set to their default values for proper operation.

RLAISINSEN, MSRLAISINSEN, PLOPTREN, PAISPTREN, PUNEQEN, PPDIEN, PRDIEN, PERDIEN, PTIUEN, PTIMEN, PPLUEN, PPLMEN

The above enable bits allows for the generation of receive path AIS (AIS-P) based on the following conditions:

- local receive LAIS (result of register 0264H/0664H/0A64H/0E64H)
- master slice receive LAIS (result of register 0264H, valid only over slices 2 to 4, in STS-48/STM-16 mode)
- path loss of pointer defect
- path AIS pointer defect
- path payload label unstable defect
- path payload label mismatch defect
- path payload defect indication defect
- path remote defect indication defect
- path enhanced remote defect indication defect
- path trace identifier unstable defect
- path trace identifier mismatch defect

When the bit is set high, the corresponding defect indication is OR'ed with other defect indications to generate receive AIS-P. When under receive AIS-P, an all ones pattern is

inserted into the receive SPE bytes. When the bit is set low, the corresponding defect indication does not affect the assertion of AIS-P.

Register 0270H 0670H 0A70H 0E70H: SARC LOP Pointer Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	PLOPTRV[4]	X
Bit 2	R	PLOPTRV[3]	X
Bit 1	R	PLOPTRV[2]	X
Bit 0	R	PLOPTRV[1]	X

PLOPTRV[4:1]

The path loss of pointer status (PLOPTRV[N]) bits indicate the current status of the LOP-P defect for STS-1/STM-0 timeslot #N. When PLOPTRCFG register bits are set to 00b, PLOPTRV is asserted when the pointer is in the LOP state and PLOPTRV[N] is negated when the pointer is not in the LOP state. When PLOPTRCFG register bits are set to 01b, PLOPTRV is asserted when the pointer or any of the concatenated pointers is in the LOP state and PLOPTRV[N] is negated when the pointer and all the concatenation pointers are not in the LOP state. When PLOPTRCFG register bits are set to 10b, PLOPTRV[N] is asserted when the pointer or any of the concatenated pointers is in the LOP state or in the AIS state and PLOPTRV is negated when the pointer and all the concatenation pointers are not in the LOP state or in the AIS state. When the PLOPTREND register bit is set to one, PLOPPTRV[N] is negated when an AIS-P defect is detected.

Register 0271H 0670H 0A71H 0E71H: SARC LOP Pointer Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	PLOPTRE[4]	0
Bit 2	R/W	PLOPTRE[3]	0
Bit 1	R/W	PLOPTRE[2]	0
Bit 0	R/W	PLOPTRE[1]	0

PLOPTRE[4:1]

The path loss of pointer interrupt enable (PLOPTRE[N]) bits control the activation of the interrupt (INTB) output. When PLOPTRE[N] is set to logic 1, a pending PLOPTRI interrupt in STS-1/STM-0 timeslot #N will assert the interrupt (INTB) output. When PLOPTRE[N] is set to logic 0, a pending PLOPTRI interrupt in STS-1/STM-0 timeslot #N will not assert the interrupt (INTB) output.

Register 0272H 0672H 0A72H 0E72H: SARC LOP Pointer Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	PLOPTRI[4]	X
Bit 2	R	PLOPTRI[3]	X
Bit 1	R	PLOPTRI[2]	X
Bit 0	R	PLOPTRI[1]	X

PLOPTRI[4:1]

The path loss of pointer interrupt status (PLOPTRI[N]) bits are event indicator for the STS-1/STM-0 path/timeslot #N. PLOPTRI[N] is set to logic 1 to indicate any changes in the status of PLOPTRV[N]. This interrupt status bit is independent of the interrupt enable bit. PLOPTRI[N] is cleared to logic 0 when this register is read. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

Register 0273H 0673H 0A73H 0E73H: SARC AIS Pointer Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	PAISPTRV[4]	X
Bit 2	R	PAISPTRV[3]	X
Bit 1	R	PAISPTRV[2]	X
Bit 0	R	PAISPTRV[1]	X

PAISPTRV[4:1]

The path AIS pointer status (PAISPTRV[N]) bit indicates the current status of the AIS-P defect for path/timeslot STS-1/STM-0 #N. When PAISPTRCFG register bits are set to 00b, PAISPTRV[N] is asserted when the pointer is in the AIS state and PAISPTRV[N] is negated when the pointer is not in the AIS state. When PAISPTRCFG register bits are set to 01b, PAISPTRV[N] is asserted when the pointer or any of the concatenated pointers is in the AIS state and PAISPTRV[N] is negated when the pointer and all the concatenation pointers are not in the AIS state. When PAISPTRCFG register bits are set to 10b, PAISPTRV[N] is asserted when the pointer and all the concatenated pointers are in the AIS state and PAISPTRV[N] is negated when the pointer or any of the concatenation pointers are not in the AIS state.

Register 0274H 0674H 0A74H 0E74H: SARC AIS Pointer Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	PAISPTRE[4]	0
Bit 2	R/W	PAISPTRE[3]	0
Bit 1	R/W	PAISPTRE[2]	0
Bit 0	R/W	PAISPTRE[1]	0

PAISPTRE[4:1]

The path AIS signal pointer interrupt enable (PAISPTRE[N]) bit controls the activation of the interrupt (INTB) output. When PAISPTRE[N] is set to logic 1, a pending PAISPTRI interrupt in STS-1/STM-0 timeslot #N will assert the interrupt (INTB) output. When PAISPTRE[N] is set to logic 0, a pending PAISPTRI interrupt in STS-1/STM-0 timeslot #N will not assert the interrupt (INTB) output.

Register 0275H 0675H 0A75H 0E75H: SARC AIS Pointer Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	PAISPTRI[4]	X
Bit 2	R	PAISPTRI[3]	X
Bit 1	R	PAISPTRI[2]	X
Bit 0	R	PAISPTRI[1]	X

PAISPTRI[4:1]

The path AIS pointer interrupt status (PAISPTRI[N]) bit is an event indicator for STS-1/STM-0 path/timeslot #N. PAISPTRI[N] is set to logic 1 to indicate any changes in the status of PAISPTRV[N]. These interrupt status bits are independent of the interrupt enable bits. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

Register 0280H 0680H 0A80H 0E80H: R8TD APS Control and Status

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R/W	Reserved	0
Bit 8	R/W	OFAAIS	0
Bit 7	R/W	FUOE	0
Bit 6	R/W	LCVE	0
Bit 5	R/W	OFAE	0
Bit 4	R/W	OCAE	0
Bit 3	R	OFAV	X
Bit 2	R	OCAV	X
Bit 1	R/W	FOFA	0
Bit 0	R/W	FOCA	0

FOCA

The force out-of-character-alignment bit (FOCA) controls the operation of the character alignment circuit on a serial link. A transition from logic zero to logic one in this bit forces the receiver to the out-of-character-alignment state where it will search for the transport frame alignment character (K28.5). This bit must be manually set to logic zero before it can be used again.

FOFA

The force out-of-frame-alignment bit (FOFA) controls the operation of the frame alignment circuit. A transition from logic zero to logic one in this bit forces the receiver to the out-of-frame-alignment state where it will search for the transport frame alignment character (K28.5). This bit must be manually set to logic zero before it can be used again.

OCAV

The out-of-character-alignment status bit (OCAV) reports the state of the character alignment circuit. OCAV is set high when the receiver is in the out-of-character-alignment state. OCAV is set low when the receiver is in the in-character-alignment state.

OFAV

The out-of-frame-alignment status bit (OFAV) reports the state of the frame alignment circuit. OFAV is set high when the receiver is in the out-of-frame-alignment state. OFAV is set low when the receiver is in the in-frame-alignment state.

OCAE

The out-of-character-alignment interrupt enable bit (OCAE) controls the change of character alignment state interrupts. Interrupts may be generated when the character alignment circuit changes state to the out-of-character-alignment state or to the in-character-alignment state. When OCAE is set high, an interrupt is generated when a change of state occurs. Interrupts due to changes of character alignment state are masked when OCAE is set low.

OFAE

The out-of-frame-alignment interrupt enable bit (OFAE) controls the change of frame alignment state interrupts. Interrupts may be generated when the frame alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. When OFAE is set high, an interrupt is generated when a change of state occurs. Interrupts due to changes of frame alignment state are masked when OFAE is set low.

LCVE

The line code violation interrupt enable bit (LCVE) controls the line code violation event interrupts. Interrupts may be generated when a line code violation is detected. When LCVE is set high, an interrupt is generated when an LCV is detected. Interrupts due to LCVs are masked when LCVE is set low.

FUOE

The FIFO underrun/overrun status interrupt enable (FUOE) controls the underrun/overrun event interrupts. Interrupts may be generated when the underrun/overrun event is detected. When FUOE is set high, an interrupt is generated when a FIFO underrun or overrun condition is detected. Interrupts due to FIFO underrun of overrun conditions are masked when FUEO is set low.

OFAAIS

The out of frame alignment alarm indication signal (OFAAIS) is set high to force high-order AIS signals in the R8TD egress data stream if the R8TD is in the out-of-frame-alignment state. The R8TD egress data stream is left unaffected in the out-of-frame alignment state when the OFFAIS is set low.

Reserved

The Reserved bits must be set to their default value for proper operation.

Register 0281H 0681H 0A81H 0E81H: R8TD APS Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	FUOI	X
Bit 6	R	LCVI	X
Bit 5	R	OFAI	X
Bit 4	R	OCAI	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

OCAI

The out-of-character-alignment interrupt status bit (OCAI) reports and acknowledges change of character alignment state interrupts. Interrupts are generated when the character alignment block changes state to the out-of-character-alignment state or to the in-character-alignment state. OCAI is set high when change of state occurs. When the interrupt is masked by the OCAE bit, the OCAI remains valid and may be polled to detect change of frame alignment events. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

OFAI

The out-of-frame-alignment interrupt status bit (OFAI) reports and acknowledges change of frame alignment state interrupts. Interrupts are generated when the frame alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. OFAI is set high when change of state occurs. When the interrupt is masked by the OFAE bit, the OFAI remains valid and may be polled to detect change of frame alignment events. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

LCVI

The line code violation event interrupt status bit (LCVI) reports and acknowledges line code violation interrupts. Interrupts are generated when the character alignment block detects a line code violation in the incoming data stream. LCVI is set high when a line code violation event is detected. When the interrupt is masked by the LCVE bit, the LCVI remains valid and may be polled to detect change of frame alignment events. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

FUOI

The FIFO underrun/overrun event interrupt status bit (FUOI) reports and acknowledges the FIFO underrun/overrun interrupts. Interrupts are generated when the character alignment block detects a that the read and write pointers are within one of each other. FUOI is set high when this event is detected. When the interrupt is masked by the FUOE bit, the FUOI remains valid and may be polled to detect underrun/overrun events. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

Register 0282H 0682H 0A82H 0E82H: R8TD APS Line Code Violation Count

Bit	Type	Function	Default
Bit 15	R	LCV[15]	X
Bit 14	R	LCV[14]	X
Bit 13	R	LCV[13]	X
Bit 12	R	LCV[12]	X
Bit 11	R	LCV[11]	X
Bit 10	R	LCV[10]	X
Bit 9	R	LCV[9]	X
Bit 8	R	LCV[8]	X
Bit 7	R	LCV[7]	X
Bit 6	R	LCV[6]	X
Bit 5	R	LCV[5]	X
Bit 4	R	LCV[4]	X
Bit 3	R	LCV[3]	X
Bit 2	R	LCV[2]	X
Bit 1	R	LCV[1]	X
Bit 0	R	LCV[0]	X

LCV[15:0]

The LCV[15:0] bits report the number of line code violations that have been detected since the last time the LCV registers were polled. The LCV registers are polled by writing to this register or to register 0002H, the S/UNI MULTI-48 Global Performance Monitor Update. This action transfers the internally accumulated error count to the LCV registers and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register 0283H 0683H 0A83H 0E83H: R8TD APS Analog Control 1

Bit	Type	Function	Default
Bit 15	R/W	Reserved	1
Bit 14	R/W	Reserved	1
Bit 13	R/W	DRU_ENB	0
Bit 12	R/W	RX_ENB	0
Bit 11	R/W	Reserved1	0
Bit 10	R/W	A_RSTB	1
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved1	0
Bit 4	R/W	Reserved1	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved1	0
Bit 1	R/W	Reserved	0
Bit 0	—	Unused	X

This register controls internal analog functions. This register should be written to 0xcc34 for normal operation.

Reserved

The Reserved bits must be set to their default value for proper operation.

Reserved1

The Reserved1 bits must be set to logic 1 for proper operation.

A_RSTB

The A_RSTB bit is a soft-reset for the Data Recovery Unit Analog block. Setting A_RSTB to logic 0 will reset the block. When used, A_RSTB should be asserted for at least 100 ns to reset circuitry properly.

RX_ENB

The RXLV enable bit (RX_ENB) bit controls the operation of RXLV block #X. Setting RX_ENB to logic 0 enables the block. Setting RX_ENB to logic 1 disables the block.

DRU_ENB

The TXLV enable bit (DRU_ENB) bit controls the operation of Data Recovery Unit Analog block #X. Setting DRU_ENB to logic 0 enables the block. Setting DRU_ENB to logic 1 disables the block.

Register 0284H 0684H 0A84H 0E84H: R8TD APS Analog Control 2

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

This register controls internal analog functions. This register should not be used and should be left in its default state.

Register 0290H: CSTR Control

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	1
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	CSU_ENB	0
Bit 3	R/W	Reserved	1
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R/W	Reserved	1

Except for the CSU_ENB register bit, the other register bits are used for manufacturing test purposes only. They are not required for normal operations.

The Reserved bits should be set to their default values for normal operation.

CSU_ENB

The active low APS CSU enable control signal (CSU_ENB) bit forces the APS CSU into low power configuration. The APS CSU is disabled when CSU_ENB is logic 1. The APS CSU is enabled when CSU_ENB is logic 0. This bit must be set to logic 0 for normal operation.

Register 0291H: CSTR Interrupt Enable and APS CSU Lock Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R	CSU_LOCKV	X
Bit 0	R/W	CSU_LOCKE	0

CSU_LOCKE

The APS CSU lock interrupt enable bit (CSU_LOCKE) enables the assertion of a hardware interrupt on INTB when the APS CSU lock status changes. When CSU_LOCKE is logic 1, the hardware interrupt is enabled. When CSU_LOCKE is logic 0, the hardware interrupt is disabled.

CSU_LOCKV

The APS CSU lock status (CSU_LOCKV) indicates the current state of the APS CSU. When CSU_LOCKV is logic 1, the APS CSU has locked on to the reference clock and is operating normally. When CSU_LOCKV is logic 0, the CSU has not locked onto the reference clock and is not in normal operating mode.

Register 0292H: CSTR APS CSU Lock Interrupt Indication

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 1	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R	CSU_LOCKI	X

CSU_LOCKI

The APS CSU lock interrupt indication bit (CSU_LOCKI) reports changes in the APS CSU lock status. CSU_LOCKI is logic 1 when the APS CSU transitions into or out of lock state. CSU_LOCKI is cleared when this register is read when WCIMODE is set to logic 0. When WCIMODE is set to logic 1, CSU_LOCKI is cleared when the bit is written to logic 1.

Register 02A0H: RDLL Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	—	Unused	X
Bit 2	R/W	ERRORE	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

The RDLL Configuration Register controls the basic operation of the Receive UL3/PL3 DLL. It is not necessary to setup this register for normal operation.

ERRORE

The ERROR interrupt enable (ERRORE) bit enables the error indication interrupt. When ERRORE is set high, an interrupt is generated upon assertion event of the ERR output and ERROR register. When ERRORE is set low, changes in the ERROR and ERR status do not generate an interrupt.

Register 02A1H: RDLL Reserved #1

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

This register controls internal functions. This register should not be used and should be left in its default state.

Register 02A2H: RDLL Reserved #2

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

This register controls internal functions. This register should not be used and should be left in its default state.

Register 02A3H: RDLL Control Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	RFCLKI	X
Bit 6	R	Reserved	X
Bit 5	R	ERRORI	X
Bit 4	R	Reserved	X
Bit 3	—	Unused	X
Bit 2	R	ERROR	X
Bit 1	R	Reserved	0
Bit 0	R	RUN	X

The RDLL Control Status Register provides information of the DLL operation.

RUN

The DLL lock status register bit (RUN) indicates the DLL found a delay line tap in which the phase difference between the rising edge of the feedback clock and the rising edge of RFCLK is zero. After system reset, RUN is logic zero until the phase detector indicates an initial lock condition. When the phase detector indicates lock, RUN is set to logic 1.

The RUN register bit is cleared only by a system reset or a software reset.

ERROR

The delay line error register bit (ERROR) indicates the DLL has run out of dynamic range. When the DLL attempts to move beyond the end of the delay line, ERROR is set high. When ERROR is high, the DLL cannot generate a DLLCLK phase which causes the rising edge of the feedback clock to be aligned to the rising edge of RFCLK. ERROR is set low, when the DLL captures lock again.

ERRORI

The delay line error event register bit (ERRORI) indicates the ERROR register bit has gone high. When the ERROR register changes from a logic zero to a logic one, the ERRORI register bit is set to logic one. If the ERRORE interrupt enable is high, the INT output is also asserted when ERRORI asserts.

When WCIMODE is low, the ERRORI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded. When WCIMODE is high, the ERRORI register bit is cleared immediately after a logic one is written to the ERRORI register, thus acknowledging the event has been recorded.

RFCLKI

The system clock event register bit RFLCKI provides a method to monitor activity on the system clock. When the RFCLK primary input changes from a logic zero to a logic one, the RFCLKI register bit is set to logic one. The RFCLKI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

When WCIMODE is low, the RFCLKI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded. When WCIMODE is high, the RFCLKI register bit is cleared immediately after a logic one is written to the RFCLKI register, thus acknowledging the event has been recorded.

Register 0300H: RSTSI Control Page Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	R/W	PAGE	0
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	TSOUT[3]	0
Bit 6	R/W	TSOUT[2]	0
Bit 5	R/W	TSOUT[1]	0
Bit 4	R/W	TSOUT[0]	0
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R/W	DOUTSEL[1]	0
Bit 0	R/W	DOUTSEL[0]	0

This register provides the data stream number; the time-slot number and the control page select used to access the control pages. Writing to this register triggers an indirect register access. This register cannot be written to when an indirect register access is in progress.

DOUTSEL[1:0]

The Data Output Select (DOUTSEL[1:0]) bits select the output data stream accessed by the current indirect transfer.

DOUTSEL[1:0]	DOUT
00	DOUT #1
01	DOUT #2
10	DOUT #3
11	DOUT #4

TSOUT[3:0]

The indirect STS-1/STM-0 output time slot (TSOUT[3:0]) bits indicate the STS-1/STM-0 output time slot accessed in the current indirect access.

TSOUT[3:0]	STS-1/STM-0 time slot #
0000	Invalid time slot
0001-1100	Time slot #1 to time slot #12
1101-1111	Invalid time slot

PAGE

The page (PAGE) bit selects which control page is accessed in the current indirect transfer. Two pages are defined: page 0 and page 1.

PAGE	Control Page
0	Page 0
1	Page 1

RWB

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the control pages. Writing logic 0 to RWB triggers an indirect write operation. Data to be written is taken for the RSTSI Indirect Data register. Writing logic 1 to RWB triggers an indirect read operation. The data read from the control pages is stored in the RSTSI Indirect Data register after the BUSY bit has cleared.

BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set to logic 1 when this register is written, triggering an access. It remains logic 1 until the access is complete at which time it is set to logic 0. This register should be polled to determine when new data is available in the Indirect Data Register or when another write access can be initiated.

Register 0301H: RSTSI Control Page Indirect Data

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R/W	COC	0
Bit 12	R/W	COD	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	CO[10]	0
Bit 9	R/W	CO[9]	0
Bit 8	R/W	CO[8]	0
Bit 7	R/W	TSIN[3]/CO[7]	0
Bit 6	R/W	TSIN[2]/CO[6]	0
Bit 5	R/W	TSIN[1]/CO[5]	0
Bit 4	R/W	TSIN[0]/CO[4]	0 (see Note)
Bit 3	R/W	CO[3]	0
Bit 2	R/W	CO[2]	0
Bit 1	R/W	DINSEL[1]/CO[1]	0
Bit 0	R/W	DINSEL[0]/CO[0]	0

This register contains the data read from the control pages after an indirect read operation or the data to be written to the control pages in an indirect write operation. The data to be written to the control pages must be set up in this register before triggering a write. The RSTSI Indirect Data register reflects the last value read or written until the completion of a subsequent indirect read operation. This register cannot be written to while an indirect register access is in progress.

Note: Default value is logic 0 when reading this register directly, and logic 1 when reading this register using an indirect access.

DINSEL[1:0]

The Data Input Select (DINSEL[1:0]) field reports the data stream number read from or written to an indirect register location. DINSEL[1:0] also doubles as CO[1:0]

DINSEL[1:0]	Data Stream
00	DIN1
01	DIN2
10	DIN3
11	DIN4

TSIN[3:0]

The STS-1/STM-0 Input Time Slot (TSIN[3:0]) field reports the time-slot number read from or written to an indirect register location. TSIN[3:0] also doubles as CO[7:4].

TSIN[3:0]	STS-1/STM-0 time slot #
0000	Invalid time slot
0001-1100	Time slot #1 to time slot #12
1101-1111	Invalid time slot

COD

The Character Overwrite Data (COD) bit reports the value of the COD bit read from or written to an indirect register location. The value of the COD bit controls the source of the data bits (DOUT[7:0]) that the muxing block outputs. When it is set to logic 0 the muxing block samples and reorders the holding buffers. When it is set to logic 1 then muxing block directly outputs the character overwrite data (CO[7:0]).

COC

The Character Overwrite Control (COC) bit reports the value of the COC bit read from or written to an indirect register location. The value of the COC bit controls the source of the control bits (DOUT[10:8]) that the muxing block outputs. When it is set to logic 0 the muxing block samples and reorders the holding buffers. When it is set to logic 1 then muxing block directly outputs the character overwrite control bits (CO[10:8]).

CO[10:0]

The Character Overwrite (CO[10:0]) bits reports the character overwrite data read from or written to an indirect register location. The interpretation of the character overwrite data bits is altered depending on the value of the COC and COD bits.

Register 0302H: RSTSI Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R	ACTIVE	X
Bit 2	R/W	PSEL	0
Bit 1	R/W	J0RORDR	0
Bit 0	R/W	COAPE	0

COAPE

The change of active page interrupt enable (COAPE) bit enables/disables the change of active page interrupt output (INT). When the COAPE bit is set to logic 1, an interrupt is generated when the active page changes from page 0 to page 1 or from page 1 to page 0. These interrupts are masked when COAPE is set to logic 0.

J0RORDR

The J0 Reorder (J0RORDR) bit enables/disables the reordering of the J0/Z0 bytes. This configuration bit only has an effect when the RSTSI is in the dynamic switching mode – if the RSTSI is in any of the static switching modes then the value of this bit is ignored. When this bit is set to logic 0 the J0/Z0 bytes are not reordered by the muxing block. When this bit is set to logic 1, normal reordering of the J0/Z0 bytes is enabled.

PSEL

The page select (PSEL) bit is used in the selection of the current active page. This bit is logically XORed with the value of the external CPS signal to determine which control page is currently active.

ACTIVE

The active page indication (ACTIVE) bit indicates which control page is currently active. When this bit is logic 0 then page 0 is controlling the dynamic mux. When this bit is logic 1 then page 1 is controlling the dynamic mux.

Register 0303H: RSTSI Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R	COAPI	X

COAPI

The change of active page interrupt statue bit (COAPI) reports the status of the change of active page interrupt. COAPI is set to logic 1 when the active control page changes from page 0 to page 1 or from page 1 to page 0. COAPI is cleared immediately following a read to this register when WCIMODE is logic 0. When WCIMODE is logic 1, COAPI is cleared immediately following a **write** (regardless of value) to this register. COAPI remains valid when the interrupt is not enabled (COAPE set to logic 0) and may be polled to detect change of active control page events.

Register 0310H 0710H 0B10H 0F10H: RCFP Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	POS_SEL	0
Bit 9	R/W	INVERT	0
Bit 8	R/W	STRIP_SEL	0
Bit 7	R/W	DELINDIS	0
Bit 6	R/W	IDLEPASS	0
Bit 5	R/W	CRCPASS	0
Bit 4	R/W	CRC_SEL[1]	1
Bit 3	R/W	CRC_SEL[0]	1
Bit 2	R/W	RXOTYPB	0
Bit 1	R/W	DESCRMBL	1
Bit 0	R/W	PROV	0

PROV

The processor provision bit (PROV) is used to enable the RCFP. When PROV is logic 0, the RCFP ATM and packet processors are disabled and will not transfer any valid data to the Receive FIFO interface. When PROV is logic 1, the RCFP ATM or packet processor is enabled and will process data presented to it and transfer data to the Receive FIFO (RXSDQ).

DESCRMBL

The DESCRMBL bit controls the descrambling of the packet or ATM cell payload with the polynomial $x^{43} + 1$. When DESCRMBL is set to logic 0, frame or cell payload descrambling is disabled. When DESCRMBL is set to logic 1, payload descrambling is enabled.

RXOTYPB

The RXOTYPB bit determines if an incoming alarm signal (AIS-P) will stop a packet by simply asserting EOP, (RXOTYPB set to logic 0), or by asserting both EOP and ERR, (RXOTYPB set to logic 1). When RXOTYPB is set to logic 1, premature termination of the packet will result in that packet failing a FCS check.

This bit is only valid when in POS mode. In ATM mode the RCFP will finish processing any cell in progress and then stop until the alarm signal is cleared.

Note that the packet transfer may be paused until the alarm is removed before being terminated (either with just REOP or with REOP and RERR depending on the RXOTYPB setting).

CRC_SEL[1:0]

The CRC select (CRC_SEL[1:0]) bits allow the control of the CRC calculation according to the table below. For ATM cells, the CRC is calculated over the first four ATM header bytes. For packet applications, the CRC is calculated over the whole packet data, after byte destuffing and descrambling.

Table 15 Functionality of the CRC_SEL[1 0] Register Bits

CRC_SEL[1:0]	HCS Operation	FCS Operation
00	Reserved	No FCS verification
01	Reserved	Reserved
10	CRC-8 without coset polynomial	CRC-CCITT (2 bytes)
11	CRC-8 with coset polynomial added	CRC-32 (4 bytes)

CRCPASS

The CRCPASS bit controls the dropping of cells and packets based on the detection of an CRC error.

When in ATM mode and when CRCPASS is a logic 0, cells containing an HCS error are dropped and the HCS verification state machine transitions to the 'Detection Mode'.

When CRCPASS is logic 1, cells are passed to the external FIFO interface regardless of errors detected in the HCS. Additionally, the HCS verification finite state machine will never lose cell delineation.

Regardless of the programming of this bit, ATM cells are always dropped while the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states unless the DELINDIS bit in this register is set to logic 1.

When in POS mode and CRCPASS is logic 1, then packets with FCS errors are not marked as such and are passed to the external FIFO interface as if no FCS error occurred. When CRCPASS is logic 0, then packets with FCS errors are marked with ERR.

IDLEPASS

The IDLEPASS bit controls the function of the ATM Idle Cell filter. It is only valid when in ATM mode. When IDLEPASS is written with logic 0, all cells that match the Idle Cell Header Pattern and Idle Cell Header Mask are filtered out. When IDLEPASS is enabled, the Idle Cell Header Pattern and Mask register bits are ignored. The default state of this bit and the bits in the RCFP Idle Cell Header and Mask Register enable the dropping of Idle cells.

DELINDIS

The DELINDIS bit can be used to disable HDLC flag alignment and byte de-stuffing. DELINDIS is only valid in POS mode with a POS-PHY Level 3 Interface.

This bit should only be set when Transparent Data Mode is desired. In this mode, data is passed directly from the TelecomBus payload to the POS-PHY Level 3 Bus without flag delineation, byte de-stuffing or CRC checking. Use of Transparent mode requires the use of 64 byte packets, and the CRC_SEL bits must be set to “00”. Note: If byte counting is desired, RBY_MODE must also be set to a logic 1.

STRIP_SEL

The frame check sequence stripping bit (STRIP_SEL) selects the CRC stripping mode of the RCFP. When STRIP_SEL is logic 1, CRC stripping is enabled. When STRIP_SEL is logic 0, CRC stripping is disabled. Note that CRC_SEL[1:0] must not equal "00", (no CRC) for stripping to be enabled. When stripping is enabled the received packet FCS or ATM cell HCS byte(s) are not passed to the RXSDQ FIFO. When STRIP is disabled the received packet FCS are transferred over the FIFO interface. When DELINDIS is enabled, packets and cells are not delineated therefore the value of STRIP_SEL is ignored. **The STRIP_SEL bit must be set to logic 1 if working in ATM mode.**

INVERT

The data inversion bit (INVERT) configures the processor to logically invert the incoming stream before processing it. When INVERT is set to logic 1, the stream is logically inverted before processing. When INVERT is set to logic 0, the stream is not inverted before processing.

POS_SEL

The Packet Over SONET (POS_SEL) bit selects the data type mode of the RCFP. When POS_SEL is logic 1, POS mode is selected. When POS_SEL is logic 0, ATM mode is selected.

Register 0311H 0711H 0B11H 0F11H: RCFP Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R	OOFV	X
Bit 8	R	LOFV	X
Bit 7	R/W	MINLE	0
Bit 6	R/W	MAXLE	0
Bit 5	R/W	ABRTE	0
Bit 4	R/W	XFERE	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	CRCE	0
Bit 1	R/W	OOFE	0
Bit 0	R/W	LOFE	0

LOFE

The LOFE bit enables the generation of an interrupt due to a change in the ATM LCD state. When LOFE is set to logic 1, the interrupt is enabled.

OOFE

The OOFE bit enables the generation of an interrupt due to a change in ATM cell delineation state or packet Idle state. When OOFE is set to logic 1, the interrupt is enabled.

CRCE

The CRCE bit enables the generation of an interrupt due to the detection of an ATM HCS or packet FCS error. When CRCE is set to logic 1, the interrupt is enabled.

XFERE

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the RCFP performance monitor counter holding registers. When XFERE is set to logic 1, the interrupt is enabled.

ABRTE

The Abort Packet Enable bit enables the generation of an interrupt due to the reception of an aborted packet. When ABRTE is set to logic 1, the interrupt is enabled.

MAXLE

The Maximum Length Packet Enable bit enables the generation of an interrupt due to the reception of a packet exceeding the programmable maximum packet length. When MAXLE is set to logic 1, the interrupt is enabled.

MINLE

The Minimum Length Packet Enable bit enables the generation of an interrupt due to the reception of a packet that is smaller than the programmable minimum packet length. When MINLE is set to logic 1, the interrupt is enabled.

LOFV

The LOFV bit gives the ATM Loss of Cell Delineation state. When LOFV is logic 1, an out of cell delineation (LOF) defect has persisted for the number of cells specified in the LCD Count Threshold register. When LOFV is logic 0, the RCFP has been in cell delineation for the number of cells specified in the LCD Count Threshold register. The cell time period can be varied by using the LCDC[10:0] register bits in the RCFP LCD Count Threshold register.

OOFV

The OOFV bit indicates the ATM cell delineation or packet out of frame alignment state. When OOFV is logic 1, the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states and is hunting for the cell boundaries or the packet processor is in Idle state. When OOFV is logic 0, the cell delineation state machine is in the 'SYNC' state and cells are passed through the receive FIFO or the packet processor is not in Idle state.

Register 0312H 0712H 0B12H 0F12H: RCFP Interrupt Indication and Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	MINLI	X
Bit 6	R	MAXLI	X
Bit 5	R	ABRTI	X
Bit 4	R	XFERI	X
Bit 3	R	Reserved	X
Bit 2	R	CRCI	X
Bit 1	R	OOFI	X
Bit 0	R	LOFI	X

LOFI

The LOFI bit is set to logic 1 when there is a change in the loss of cell delineation (LCD) state. The current value of the LCD state is available through the LOFV bit in the RCFP Interrupt Enable register. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read. This interrupt can be masked using LOFE.

OOFI

The OOFI bit is set to logic 1 when the RCFP ATM cell processor enters or exits the SYNC state or the packet processor enters or exits the frame alignment state. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read. This interrupt can be masked using OOFE.

CRCI

The CRCI bit is set to logic 1 when an ATM HCS or packet FCS error is detected. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read. This interrupt can be masked using CRCE.

XFERI

The XFERI bit indicates that a transfer of accumulated counter data has occurred. Logic 1 in this bit position indicates that the RCFP performance monitor counter holding registers have been updated. This update is initiated by writing to one of the counter register locations, or by writing to register 0002H for global performance monitor update. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read. This interrupt can be masked using XFERE.

ABRTI

The ABRTI bit indicates the generation of an interrupt due to the reception of an aborted packet. This interrupt can be masked using ABRTE. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read.

MAXLI

The MAXLI bit indicates an interrupt due to the reception of a packet exceeding the programmable maximum packet length. This interrupt can be masked using MAXLE. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read.

MINLI

The MINLI bit indicates an interrupt due to the reception of a packet that is smaller than the programmable minimum packet length. This interrupt can be masked using MINLE. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read.

Register 0313H 0713H 0B13H 0F13H: RCFP Minimum Packet Length

Bit	Type	Function	Default
Bit 15	R/W	MINPL[7]	0
Bit 14	R/W	MINPL[6]	0
Bit 13	R/W	MINPL[5]	0
Bit 12	R/W	MINPL[4]	0
Bit 11	R/W	MINPL[3]	0
Bit 10	R/W	MINPL[2]	1
Bit 9	R/W	MINPL[1]	0
Bit 8	R/W	MINPL[0]	0
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	RBY_MODE	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	0

Reserved

The Reserved bits should be set to their default values for proper operation.

RBY_MODE

The receive byte counter mode (RBY_MODE) bit is used to select the mode in which the RBY_IC[39:0] counters work. When RBY_MODE is logic 0, RBY_IC[39:0] will count all bytes in received packets (including FCS and Abort bytes) after the byte destuffing operation. When RBY_MODE is logic 1, RBY_IC[39:0] will count all bytes in received packets (including FCS, Abort, and stuff bytes) before the byte destuffing operation. Flag bytes will not be counted in either case. The RBY_MODE bit is only valid when working in POS mode. Note that in transparent mode (DELINDIS=1), RBY_MODE must be set to logic 1.

MINPL[7:0]

The Minimum Packet Length (MINPL[7:0]) bits are used to set the minimum packet length. Packets smaller than this length are marked with an error. The packet length used here is defined as the number of bytes encapsulated into the POS frame after destuffing but including the FCS. The default minimum packet length is 4 octets. If STRIP_SEL in register RCFP configuration is set to logic 1, then MINPL should be set to at least 4 plus the number of CRC bytes – i.e. either 6 or 8. If STRIP_SEL is logic 0, then MINPL should be set to a value greater than or equal to 5.

Register 0314H 0714H 0B14H 0F14H: RCFP Maximum Packet Length

Bit	Type	Function	Default
Bit 15	R/W	MAXPL[16]	0
Bit 14	R/W	MAXPL[15]	0
Bit 13	R/W	MAXPL[14]	0
Bit 12	R/W	MAXPL[13]	0
Bit 11	R/W	MAXPL[12]	0
Bit 10	R/W	MAXPL[11]	0
Bit 9	R/W	MAXPL[10]	1
Bit 8	R/W	MAXPL[9]	1
Bit 7	R/W	MAXPL[8]	0
Bit 6	R/W	MAXPL[7]	0
Bit 5	R/W	MAXPL[6]	0
Bit 4	R/W	MAXPL[5]	0
Bit 3	R/W	MAXPL[4]	0
Bit 2	R/W	MAXPL[3]	0
Bit 1	R/W	MAXPL[2]	0
Bit 0	R/W	MAXPL[1]	0

MAXPL[16:1]

The Maximum Packet Length (MAXPL[16:0]) bits are used to set the maximum packet length. MAXPL[0] is automatically set to logic 0. Packets larger than this length are marked with an error. This Maximum Packet Length defaults to 1.5 Kbytes. The packet length used here is defined as the number of bytes encapsulated into the POS frame excluding byte stuffing but including the FCS. The default maximum packet length is 1536 octets. The maximum packet length allowed is 128 Kbytes. MAXPL[16:1] should not be set higher than 0xFFFA or lower than 0x0003 to guarantee correct behavior.

Register 0315H 0715H 0B15H 0F15H: RCFP LCD Count Threshold

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	R/W	LCDC[10]	0
Bit 9	R/W	LCDC[9]	0
Bit 8	R/W	LCDC[8]	1
Bit 7	R/W	LCDC[7]	0
Bit 6	R/W	LCDC[6]	1
Bit 5	R/W	LCDC[5]	1
Bit 4	R/W	LCDC[4]	0
Bit 3	R/W	LCDC[3]	1
Bit 2	R/W	LCDC[2]	0
Bit 1	R/W	LCDC[1]	0
Bit 0	R/W	LCDC[0]	0

LCDC[10:0]

The LCDC[10:0] bits represent the number of consecutive cell periods the receive cell processor must be out of cell delineation before loss of cell delineation (LCD) is declared. Likewise, LCD is not deasserted until the receive cell processor is in cell delineation for the number of cell periods specified by LCDC[10:0]. Note that this value forms a lower bound for the assertion of LCD. In the presence of random data, false headers could be discovered, which would reset the counter and delay the declaration of LCD.

The default value of LCD[10:0] is 360, which translates to the following:

Table 16 Average STS-x Cell Period Versus LCD Integration Period

Format	Average Cell Period	Default LCD Integration Period
STS-48c	176.9 ns	63.8 μs
STS-12c	707.5 ns	254.7 μs

Register 0316H 0716H 0B16H 0F16H: RCFP Receive Idle Cell Header and Mask

Bit	Type	Function	Default
Bit 15	R/W	GFC[3]	0
Bit 14	R/W	GFC[2]	0
Bit 13	R/W	GFC[1]	0
Bit 12	R/W	GFC[0]	0
Bit 11	R/W	PTI[3]	0
Bit 10	R/W	PTI[2]	0
Bit 9	R/W	PTI[1]	0
Bit 8	R/W	CLP	1
Bit 7	R/W	MGFC[3]	1
Bit 6	R/W	MGFC[2]	1
Bit 5	R/W	MGFC[1]	1
Bit 4	R/W	MGFC[0]	1
Bit 3	R/W	MPTI[3]	1
Bit 2	R/W	MPTI[2]	1
Bit 1	R/W	MPTI[1]	1
Bit 0	R/W	MCLP	1

MCLP

The CLP bit contains the mask pattern for the eighth bit of the fourth octet of the 53-octet cell. This mask is applied to this register to select the bits included in the cell filter. Logic 1 in this bit position enables the CLP bit in the pattern register to be compared. Logic 0 causes the masking of the CLP bit. The default enables the register bit comparison.

MPTI[3:0]

The MPTI[3:0] bits contain the mask pattern for the fifth, sixth, and seventh bits of the fourth octet of the 53-octet cell. This mask is applied to the Idle Cell Header field to select the bits included in the cell filter. A logic 1 in any bit position enables the corresponding bit in the pattern register to be compared. A logic 0 causes the masking of the corresponding bit. The default enables the register bit comparison.

MGFC[3:0]

The MGFC[3:0] bits contain the mask pattern for the first, second, third, and fourth bits of the first octet of the 53-octet cell. This mask is applied to the Idle Cell Header field to select the bits included in the cell filter. Logic 1 in any bit position enables the corresponding bit in the pattern register to be compared. Logic 0 causes the masking of the corresponding bit. The default enables the register bit comparison.

CLP

The CLP bit contains the pattern to match in the eighth bit of the fourth octet of the 53-octet cell, in conjunction with the Idle Cell Header and Mask register bit. The IDLEPASS bit in the Configuration Register must be set to logic 0 to enable dropping of cells matching this pattern.

PTI[2:0]

The PTI[2:0] bits contain the pattern to match in the fifth, sixth, and seventh bits of the fourth octet of the 53-octet cell, in conjunction with the Idle Cell Header and Mask register bits. The IDLEPASS bit in the Configuration Register must be set to logic 0 to enable dropping of cells matching this pattern.

GFC[3:0]

The GFC[3:0] bits contain the pattern to match in the first, second, third, and fourth bits of the first octet of the 53-octet cell, in conjunction with the Idle Cell Header and Mask register bits. The IDLEPASS bit in the Configuration Register must be set to logic 0 to enable dropping of cells matching this pattern.

Note that an all-zeros pattern must be present in the VPI and VCI fields of the Idle cell.

Register 0317H 0717H 0B17H 0F17H: RCFP Receive Byte/Idle Cell Counter (LSB)

Bit	Type	Function	Default
Bit 15	R	RBY_IC[15]	X
Bit 14	R	RBY_IC[14]	X
Bit 13	R	RBY_IC[13]	X
Bit 12	R	RBY_IC[12]	X
Bit 11	R	RBY_IC[11]	X
Bit 10	R	RBY_IC[10]	X
Bit 9	R	RBY_IC[9]	X
Bit 8	R	RBY_IC[8]	X
Bit 7	R	RBY_IC[7]	X
Bit 6	R	RBY_IC[6]	X
Bit 5	R	RBY_IC[5]	X
Bit 4	R	RBY_IC[4]	X
Bit 3	R	RBY_IC[3]	X
Bit 2	R	RBY_IC[2]	X
Bit 1	R	RBY_IC[1]	X
Bit 0	R	RBY_IC[0]	X

Register 0318H 0718H 0B18H 0F18H: RCFP Receive Byte/Idle Cell Counter

Bit	Type	Function	Default
Bit 15	R	RBY_IC[31]	X
Bit 14	R	RBY_IC[30]	X
Bit 13	R	RBY_IC[29]	X
Bit 12	R	RBY_IC[28]	X
Bit 11	R	RBY_IC[27]	X
Bit 10	R	RBY_IC[26]	X
Bit 9	R	RBY_IC[25]	X
Bit 8	R	RBY_IC[24]	X
Bit 7	R	RBY_IC[23]	X
Bit 6	R	RBY_IC[22]	X
Bit 5	R	RBY_IC[21]	X
Bit 4	R	RBY_IC[20]	X
Bit 3	R	RBY_IC[19]	X
Bit 2	R	RBY_IC[18]	X
Bit 1	R	RBY_IC[17]	X
Bit 0	R	RBY_IC[16]	X

Register 0319H 0719H 0B19H 0F19H: RCFP Receive Byte/Idle Cell Counter (MSB)

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	RBY_IC[39]	X
Bit 6	R	RBY_IC[38]	X
Bit 5	R	RBY_IC[37]	X
Bit 4	R	RBY_IC[36]	X
Bit 3	R	RBY_IC[35]	X
Bit 2	R	RBY_IC[34]	X
Bit 1	R	RBY_IC[33]	X
Bit 0	R	RBY_IC[32]	X

RBY_IC[39:0]

When POS mode is selected, the RBY_IC[39:0] bits indicate the number of bytes received within POS frames during the last accumulation interval. The byte counts include all user payload bytes, FCS bytes, and abort bytes. Inclusion of stuffed bytes in the count is controlled by the RBY_MODE register bit. HDLC flags are not counted.

When ATM mode is selected, the RBY_IC[39:0] bits indicate the number of Idle cells received and passed to the FIFO interface in the last accumulation interval.

A write to any one of the RCFP counter registers loads all the corresponding RCFP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0002H can be written to initiate a global performance counter update across the S/UNI MULTI-48.

Register 031AH 071AH 0B1AH 0F1AH: RCFP Receive Packet/Cell Counter (LSB)

Bit	Type	Function	Default
Bit 15	R	RP_RC[15]	X
Bit 14	R	RP_RC[14]	X
Bit 13	R	RP_RC[13]	X
Bit 12	R	RP_RC[12]	X
Bit 11	R	RP_RC[11]	X
Bit 10	R	RP_RC[10]	X
Bit 9	R	RP_RC[9]	X
Bit 8	R	RP_RC[8]	X
Bit 7	R	RP_RC[7]	X
Bit 6	R	RP_RC[6]	X
Bit 5	R	RP_RC[5]	X
Bit 4	R	RP_RC[4]	X
Bit 3	R	RP_RC[3]	X
Bit 2	R	RP_RC[2]	X
Bit 1	R	RP_RC[1]	X
Bit 0	R	RP_RC[0]	X

Register 031BH 071BH 0B1BH 0F1B: RCFP Receive Packet/Cell Counter (MSB)

Bit	Type	Function	Default
Bit 15	R	RP_RC[31]	X
Bit 14	R	RP_RC[30]	X
Bit 13	R	RP_RC[29]	X
Bit 12	R	RP_RC[28]	X
Bit 11	R	RP_RC[27]	X
Bit 10	R	RP_RC[26]	X
Bit 9	R	RP_RC[25]	X
Bit 8	R	RP_RC[24]	X
Bit 7	R	RP_RC[23]	X
Bit 6	R	RP_RC[22]	X
Bit 5	R	RP_RC[21]	X
Bit 4	R	RP_RC[20]	X
Bit 3	R	RP_RC[19]	X
Bit 2	R	RP_RC[18]	X
Bit 1	R	RP_RC[17]	X
Bit 0	R	RP_RC[16]	X

RP_RC[31:0]

When POS mode is selected, the RP_RC[31:0] bits indicate the number of received good packets passed to the FIFO interface during the last accumulation interval.

When ATM mode is selected, the RP_RC[31:0] bits indicate the number of received ATM cells and passed to the FIFO interface in the last accumulation interval.

A write to any one of the RCFP counter registers loads all the corresponding RCFP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0002H can be written to initiate a global performance counter update across the S/UNI MULTI-48.

Register 031CH 071CH 0B1CH 0F1CH: RCFP Receive Erroneous FCS/HCS Counter

Bit	Type	Function	Default
Bit 15	R	EFCS[15]	X
Bit 14	R	EFCS[14]	X
Bit 13	R	EFCS[13]	X
Bit 12	R	EFCS[12]	X
Bit 11	R	EFCS[11]	X
Bit 10	R	EFCS[10]	X
Bit 9	R	EFCS[9]	X
Bit 8	R	EFCS[8]	X
Bit 7	R	EFCS[7]/UHCS[7]	X
Bit 6	R	EFCS[6]/UHCS[6]	X
Bit 5	R	EFCS[5]/UHCS[5]	X
Bit 4	R	EFCS[4]/UHCS[4]	X
Bit 3	R	EFCS[3]/UHCS[3]	X
Bit 2	R	EFCS[2]/UHCS[2]	X
Bit 1	R	EFCS[1]/UHCS[1]	X
Bit 0	R	EFCS[0]/UHCS[0]	X

EFCS[15:0]

When POS mode is selected, the EFCS[15:0] bits indicate the number of received FCS errors during the last accumulation interval.

UHCS[7:0]

When ATM mode is selected, the UHCS[7:0] bits indicate the number of HCS errors received in the last accumulation interval.

A write to any one of the RCFP counter registers loads all the corresponding RCFP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0002H can be written to initiate a global performance counter update across the S/UNI MULTI-48.

Register 031DH 071DH 0B1DH 0F1DH: RCFP Receive Aborted Packet Counter

Bit	Type	Function	Default
Bit 15	R	RABR[15]	X
Bit 14	R	RABR[14]	X
Bit 13	R	RABR[13]	X
Bit 12	R	RABR[12]	X
Bit 11	R	RABR[11]	X
Bit 10	R	RABR[10]	X
Bit 9	R	RABR[9]	X
Bit 8	R	RABR[8]	X
Bit 7	R	RABR[7]	X
Bit 6	R	RABR[6]	X
Bit 5	R	RABR[5]	X
Bit 4	R	RABR[4]	X
Bit 3	R	RABR[3]	X
Bit 2	R	RABR[2]	X
Bit 1	R	RABR[1]	X
Bit 0	R	RABR[0]	X

RABR[15:0]

When POS mode is selected, the RABR[15:0] bits indicate the number of aborted packets received during the last accumulation interval. This counter is held at value 0 when ATM mode is selected.

A write to any one of the RCFP counter registers loads all the corresponding RCFP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0002H can be written to initiate a global performance counter update across the S/UNI MULTI-48.

Register 031EH 071EH 0B1EH 0F1EH: RCFP Receive Minimum Length Packet Error Counter

Bit	Type	Function	Default
Bit 15	R	RMINL[15]	X
Bit 14	R	RMINL[14]	X
Bit 13	R	RMINL[13]	X
Bit 12	R	RMINL[12]	X
Bit 11	R	RMINL[11]	X
Bit 10	R	RMINL[10]	X
Bit 9	R	RMINL[9]	X
Bit 8	R	RMINL[8]	X
Bit 7	R	RMINL[7]	X
Bit 6	R	RMINL[6]	X
Bit 5	R	RMINL[5]	X
Bit 4	R	RMINL[4]	X
Bit 3	R	RMINL[3]	X
Bit 2	R	RMINL[2]	X
Bit 1	R	RMINL[1]	X
Bit 0	R	RMINL[0]	X

RMINL[15:0]

When POS mode is selected, the RMINL[15:0] bits indicate the number of minimum length packet errors received during the last accumulation interval. This counter is held at value 0 when ATM mode is selected. Note that all minimum packet violations are counted in this register.

A write to any one of the RCFP counter registers loads all the corresponding RCFP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0002H can be written to initiate a global performance counter update across the S/UNI MULTI-48.

Register 031FH 071FH 0B1FH 0F1FH: RCFP Receive Maximum Length Packet Error Counter

Bit	Type	Function	Default
Bit 15	R	RMAXL[15]	X
Bit 14	R	RMAXL[14]	X
Bit 13	R	RMAXL[13]	X
Bit 12	R	RMAXL[12]	X
Bit 11	R	RMAXL[11]	X
Bit 10	R	RMAXL[10]	X
Bit 9	R	RMAXL[9]	X
Bit 8	R	RMAXL[8]	X
Bit 7	R	RMAXL[7]	X
Bit 6	R	RMAXL[6]	X
Bit 5	R	RMAXL[5]	X
Bit 4	R	RMAXL[4]	X
Bit 3	R	RMAXL[3]	X
Bit 2	R	RMAXL[2]	X
Bit 1	R	RMAXL[1]	X
Bit 0	R	RMAXL[0]	X

RMAXL[15:0]

When POS mode is selected, the RMAXL[15:0] bits indicate the number of maximum length packet errors received during the last accumulation interval. This counter is held at value 0 when ATM mode is selected.

A write to any one of the RCFP counter registers loads all the corresponding RCFP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0002H can be written to initiate a global performance counter update across the S/UNI MULTI-48.

Register 0320H: RXSDQ FIFO Reset

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R	RXSDQTIP	X
Bit 0	R/W	SDQRST	1

SDQRST

This bit is used to reset the RXSDQ. The RXSDQ comes up in reset. It should be taken out of reset by writing a 0 to this bit. The user can reset the RXSDQ at any time by writing a 1 to this bit, and then writing a 0. Reset flushes all the data in the FIFOs, resets the read and write pointers and resets all counters. The configuration information is not changed by Reset.

RXSDQTIP

The RXSDQTIP bit indicates that the RXSDQ counters are in the process of being transferred to their holding registers. A transfer is initialized by writing to the S/UNI MULTI-48 Global Performance Monitor Update register (0002H). RXSDQTIP is logic 1 while a transfer is in progress. It returns to logic 0 when the transfer is completed.

Register 0321H: RXSDQ FIFO Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	SOPE	0
Bit 1	R/W	EOPE	0
Bit 0	R/W	OFLE	0

OFLE

When this bit is set to 1, FIFO overflows cause the INTB output to be asserted. If this bit is set to 0, FIFO overflows do not cause INTB to be asserted.

EOPE

When this bit is set to 1, bad EOP signals cause the INTB output to be asserted. If this bit is set to 0, bad EOP signals do not cause INTB to be asserted.

SOPE

When this bit is set to 1, bad SOP signals cause the INTB output to be asserted. If this bit is set to 0, bad SOP signals do not cause INTB to be asserted.

Reserved

This bit should be set to logic 0 for proper operation.

Register 0323H: RXSDQ FIFO Overflow Port and Interrupt Indication

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R	OFL_FIFO[5]	X
Bit 12	R	OFL_FIFO[4]	X
Bit 11	R	OFL_FIFO[3]	X
Bit 10	R	OFL_FIFO[2]	X
Bit 9	R	OFL_FIFO[1]	X
Bit 8	R	OFL_FIFO[0]	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R	OFLI	X

OFLI

This bit is set when any of the configured FIFOs overflows. The FIFO number that caused this interrupt is available in OFL_FIFO[5:0]. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read. This overflow indication can be set by each byte of a cell or packet that is being written into a full FIFO, so multiple interrupts can be generated for the same cell or packet if the interrupt indication is read too quickly.

OFL_FIFO[5:0]

These bits are used to indicate the FIFO number which overflowed and set the OFLI indication. These bits are valid only when OFLI is logic 1. If multiple FIFOs overflow before this interrupt is serviced, OFL_FIFO[5:0] will indicate the FIFO that first overflowed (see section 13.28 on how FIFO number and PL3/UL3 channels are mapped).

Register 0324H: RXSDQ FIFO EOP Error Port and Interrupt Indication

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R	EOP_FIFO[5]	X
Bit 12	R	EOP_FIFO[4]	X
Bit 11	R	EOP_FIFO[3]	X
Bit 10	R	EOP_FIFO[2]	X
Bit 9	R	EOP_FIFO[1]	X
Bit 8	R	EOP_FIFO[0]	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R	EOPI	X

EOPI

This bit is set when two EOPs arrive consecutively on the same FIFO without being separated by a SOP. The FIFO number that caused the interrupt is available in EOP_FIFO[5:0]. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read.

EOP_FIFO[5:0]

These bits are used to indicate the FIFO which received a bad EOP and set the EOPI indication. These bits are valid only when EOPI is logic 1. If multiple bad EOP sequences occur before this interrupt is serviced, EOP_FIFO[5:0] will indicate the FIFO that first observed the bad EOP sequence.

Register 0325H: RXSDQ FIFO SOP Error Port and Interrupt Indication

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R	SOP_FIFO[5]	X
Bit 12	R	SOP_FIFO[4]	X
Bit 11	R	SOP_FIFO[3]	X
Bit 10	R	SOP_FIFO[2]	X
Bit 9	R	SOP_FIFO[1]	X
Bit 8	R	SOP_FIFO[0]	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R	SOPI	X

SOPI

This bit is set when two SOPs arrive consecutively on the same FIFO without being separated by a EOP. The FIFO number that caused the interrupt is available in SOP_FIFO[5:0]. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read.

SOP_FIFO[5:0]

These bits are used to indicate the FIFO which received a bad SOP and set the SOPI indication. These bits are valid only when SOPI is logic 1. If multiple bad SOP sequences occur before this interrupt is serviced, SOP_FIFO[5:0] will indicate the FIFO that first observed the bad SOP sequence.

Register 0328H: RXSDQ FIFO Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	W	FLUSH	X
Bit 12	R	EMPTY	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	PHYID[5]	0
Bit 4	R/W	PHYID[4]	0
Bit 3	R/W	PHYID[3]	0
Bit 2	R/W	PHYID[2]	0
Bit 1	R/W	PHYID[1]	0
Bit 0	R/W	PHYID[0]	0

This is an indirect register that is used to specify the address of the FIFO that the user is setting up or reading the setup for. This register is the common address used for the four registers including this one: RXSDQ FIFO Indirect Configuration, RXSDQ FIFO Indirect Buffer Available and Data Available Thresholds, and RXSDQ FIFO Indirect Cells and Packets Count. In order to change the current setup of a FIFO, it is recommended that the user reads the existing setup information first, makes any modifications as required, and writes back the information. Note that this read and write-back procedure must be performed for each of the above registers, even if its contents are not changing.

PHYID[5:0]

This is a 6-bit number that is used to describe the current FIFO being addressed by the rest of the FIFO setup registers – the FIFO Indirect Configuration, FIFO Buffer Available Threshold, FIFO Data Available Threshold and FIFO Cells and Packets Count. The range of FIFO numbers that can be used is 0 to 2FH (see section 13.28 on how FIFO number and PL3/UL3 channels are mapped).

EMPTY

This read-only bit indicates if the **requested FIFO** is empty. When this bit is read as 1, the FIFO number specified in PHYID[5:0] in this register is empty. Before reconfiguring a disabled FIFO, this bit needs to be sampled at logic 1 indicating that the FIFO is empty.

FLUSH

This is a write-only bit used to discard all the current data in a specified FIFO. This should typically be used if a non-empty FIFO needs to be reconfigured. If this bit is manually set, it must also be manually cleared before enabling the specified FIFO. Note that this bit can only be set or cleared when RWB = 0 and PHYID is used to select the correct PHY since it is an indirect access bit.

RWB

This bit is used to indicate whether the user is writing the setup of a FIFO, or reading all setup information of a FIFO. This bit is used in conjunction with the BUSY bit. When this bit is set to 1, all the available setup information of the FIFO requested in PHYID[5:0] is available in the registers FIFO Indirect Configuration, FIFO Indirect Buffer Available Threshold, FIFO Indirect Data Available Threshold, and FIFO Indirect Cells and Packets Count. When this bit is set to 0, the user is writing the configuration of a FIFO. The RXSDQ latches in the data in the FIFO Indirect Configuration, FIFO Indirect Buffer Available Threshold, FIFO Indirect Data Available Threshold, and FIFO Indirect Cells and Packets Count registers.

BUSY

This is a read-only bit is used to indicate to the user that the information requested for the FIFO specified in bits PHYID[5:0] is in the process of being updated. If this bit is sampled to be 1, the update is still in progress. If this bit is sampled 0, the information for the FIFO is now available in the FIFO Indirect Configuration, FIFO Indirect Buffer Available Threshold, FIFO Indirect Data Available Threshold, and FIFO Indirect Cells and Packets Count registers.

Register 0329H: RXSDQ FIFO Indirect Configuration

Bit	Type	Function	Default
Bit 15	R/W	ENABLE	0
Bit 14	R/W	POS_SEL	0
Bit 13	R/W	FIFO_NUMBER[5]	0
Bit 12	R/W	FIFO_NUMBER[4]	0
Bit 11	R/W	FIFO_NUMBER[3]	0
Bit 10	R/W	FIFO_NUMBER[2]	0
Bit 9	R/W	FIFO_NUMBER[1]	0
Bit 8	R/W	FIFO_NUMBER[0]	0
Bit 7	R/W	FIFO_BS[1]	0
Bit 6	R/W	FIFO_BS[0]	0
Bit 5	—	Unused	X
Bit 4	R/W	BLOCK_PTR[4]	0
Bit 3	R/W	BLOCK_PTR[3]	0
Bit 2	R/W	BLOCK_PTR[2]	0
Bit 1	R/W	BLOCK_PTR[1]	0
Bit 0	R/W	BLOCK_PTR[0]	0

BLOCK_PTR[4:0]

This is a 5-bit number that is calculated and programmed by the user based on the number of PHYs, the size of each FIFO, and total number of FIFOs required by the system.

FIFO_BS[1:0]

This 2-bit number denotes the size in Blocks of FIFO for the PHYID specified in the FIFO Indirect Address register. The bandwidth is related to the size of the FIFO that will be allocated to the PHY.

FIFO_NUMBER[5:0]

This is a 6-bit internal FIFO number that is used to associate a given PHY ID with a FIFO. This number can be in one of 4 ranges, and is unique for each PHY (see section 13.28 on how FIFO number and PL3/UL3 channels are mapped).

POS_SEL

This bit is set to 1 if the FIFO needs to be configured as a packet FIFO. By default, the FIFOs are configured as ATM cell FIFOs. Note that a packet FIFO can process ATM cell traffic, but without enforcing cell size. When POS_SEL=0, there are 5 dead cycles between cell transfers, resulting in a 98.2% bandwidth for a 100 MHz clock (102 MHz clock is sufficient for 100% bandwidth). When POS_SEL=1, there are only 2 dead cycles between transfers, so full ATM bandwidth is possible with a 91 MHz clock. Thus, it is recommended that POS_SEL be set to logic 0 only for UL3 applications.

ENABLE

This bit enables individual FIFOs. Writing a 0 to this bit disables a FIFO. If previously enabled, a disabled FIFO does not accept any new data into it, but continues to assert Data Available internally until it is drained completely. In order to reconfigure FIFOs during operation, they need to be disabled first.

Register 032AH: RXSDQ FIFO Indirect Data Available Threshold

Bit	Type	Function	Default
Bit 15	R/W	DT[7]	0
Bit 14	R/W	DT[6]	0
Bit 13	R/W	DT[5]	0
Bit 12	R/W	DT[4]	0
Bit 11	R/W	DT[3]	0
Bit 10	R/W	DT[2]	0
Bit 9	R/W	DT[1]	1
Bit 8	R/W	DT[0]	1
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

This register is used to set the Data Available Threshold for each of the FIFOs. This threshold is explained in Section 13.31. The FIFOs need not be enabled to set this threshold. In order to change this value for a FIFO, the user should first disable it, write in the new value, and enable it again.

Reserved

The Reserved bits should be set to their default values for proper operation.

DT[7:0]

These bits specify the Data Available threshold for the FIFO selected by the FIFO Indirect Address register PHYID[5:0] bits. When this threshold is being set, these bits are written to by the user, and when this threshold is being read, these bits hold the previously configured data. The threshold is equal to DT[7:0] + 1. This threshold is set in 16 byte Blocks. This threshold can never be greater than the size of the FIFO being configured, and the absolute maximum value is DT[7:0] +1 = 16. This number should be a standard fraction of the FIFO size in blocks. In the case of UL3 ATM FIFOs, this number must be set to a value of DT[7:0] = 3 (ATM cells are 4 Blocks long).

For PL3 interfaces, RVAL will be asserted for the channel (PHYID[5:0]) when the FIFO depth is equal to or greater than DT[7:0] + 1 or when an EOP is in the FIFO.

For UL3 ATM interfaces, RCA will be asserted for the channel (PHYID[5:0]) when the FIFO depth is equal to or greater than one cell (DT[7:0] + 1 = 4 blocks = 1 cell).

Register 032BH: RXSDQ FIFO Indirect Cell and Packet Count

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R	COUNT[3]	X
Bit 2	R	COUNT[2]	X
Bit 1	R	COUNT[1]	X
Bit 0	R	COUNT[0]	X

This register is used to read the 4-bit non-saturating FIFO counters for the enabled FIFOs, which count the number of ATM cells or packets accepted by the FIFO. The counts are latched when the register 0002H of the S/UNI MULTI-48 is written to. These counters are then reset, and the latched values can be read individually through this register.

The counters provided by the RXSDQ are purely for diagnostic purposes. They should be ignored in normal operations.

COUNT[3:0]

These read-only bits hold the last sampled count for the FIFO requested for in FIFO Indirect Address register PHYID[5:0] bits. This register is latched when register 0002H is written to for a global performance monitor update. After the count is latched into the register, the internal counter is reset to 0, and starts counting again. When this counter reaches its maximum count, it rolls over.

Register 032CH: RXSDQ FIFO Cells and Packets Accepted Aggregate Count (LSB)

Bit	Type	Function	Default
Bit 15	R	ACOUNT[15]	X
Bit 14	R	ACOUNT[14]	X
Bit 13	R	ACOUNT[13]	X
Bit 12	R	ACOUNT[12]	X
Bit 11	R	ACOUNT[11]	X
Bit 10	R	ACOUNT[10]	X
Bit 9	R	ACOUNT[9]	X
Bit 8	R	ACOUNT[8]	X
Bit 7	R	ACOUNT[7]	X
Bit 6	R	ACOUNT[6]	X
Bit 5	R	ACOUNT[5]	X
Bit 4	R	ACOUNT[4]	X
Bit 3	R	ACOUNT[3]	X
Bit 2	R	ACOUNT[2]	X
Bit 1	R	ACOUNT[1]	X
Bit 0	R	ACOUNT[0]	X

Register 032DH: RXSDQ FIFO Cells and Packets Accepted Aggregate Count (MSB)

Bit	Type	Function	Default
Bit 15	R	ACOUNT[31]	X
Bit 14	R	ACOUNT[30]	X
Bit 13	R	ACOUNT[29]	X
Bit 12	R	ACOUNT[28]	X
Bit 11	R	ACOUNT[27]	X
Bit 10	R	ACOUNT[26]	X
Bit 9	R	ACOUNT[25]	X
Bit 8	R	ACOUNT[24]	X
Bit 7	R	ACOUNT[23]	X
Bit 6	R	ACOUNT[22]	X
Bit 5	R	ACOUNT[21]	X
Bit 4	R	ACOUNT[20]	X
Bit 3	R	ACOUNT[19]	X
Bit 2	R	ACOUNT[18]	X
Bit 1	R	ACOUNT[17]	X
Bit 0	R	ACOUNT[16]	X

ACOUNT[31:0]

These bits display the aggregate count of all the POS packets and ATM cells that are accepted by the RXSDQ. This register is latched when register 0002H is written to for a global performance monitor update. After the count is latched into the register, the internal counter is reset to 0, and starts counting again. When this counter reaches its maximum count, it rolls over and starts counting again from 0.

Register 032EH: RXSDQ FIFO Cells and Packets Dropped Aggregate Count

Bit	Type	Function	Default
Bit 15	R	DCOUNT[15]	X
Bit 14	R	DCOUNT[14]	X
Bit 13	R	DCOUNT[13]	X
Bit 12	R	DCOUNT[12]	X
Bit 11	R	DCOUNT[11]	X
Bit 10	R	DCOUNT[10]	X
Bit 9	R	DCOUNT[9]	X
Bit 8	R	DCOUNT[8]	X
Bit 7	R	DCOUNT[7]	X
Bit 6	R	DCOUNT[6]	X
Bit 5	R	DCOUNT[5]	X
Bit 4	R	DCOUNT[4]	X
Bit 3	R	DCOUNT[3]	X
Bit 2	R	DCOUNT[2]	X
Bit 1	R	DCOUNT[1]	X
Bit 0	R	DCOUNT[0]	X

DCOUNT[15:0]

These bits display the aggregate count of all the POS packets and ATM cells that are dropped by the RXSDQ due to FIFO overflows. This register is latched when register 0002H is written to for a global performance monitor update. After the count is latched into the register, the internal counter is reset to 0, and starts counting again. When this counter reaches its maximum count, it rolls over and starts counting again from 0.

Register 0330H: RXPHY Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R/W	RSXPAUSE[1]	0
Bit 12	R/W	RSXPAUSE[0]	0
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	W	Reserved1	0
Bit 4	W	Reserved	0
Bit 3	W	Reserved1	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	ODDPARITY	0
Bit 0	R/W	RXPRST	1

RXPRST

The RXPRST bit is used to reset the RXPHY circuitry. When RXPRST is set to logic zero, the RXPHY operates normally. When RXPRST is set to logic one, the RXPHY ignores all pin inputs but the register bits may be accessed for purposes of initialization. The RXPHY deasserts all outputs until a logic zero is written to RXPRST.

ODDPARITY

The ODDPARITY bit is used to set the type of parity that is generated by the RXPHY for the UL3 or POS L3 interface. When set to logic 1, odd parity is generated. When set to logic 0, even parity is generated. This bit is global and affects all PHY channels.

Reserved

The Reserved bits must be set to logic 0 for proper operation.

Reserved1

The Reserved1 bits must be set to logic 1 for proper operation.

RSXPAUSE[1:0]

RSXPAUSE bits control the number of additional clocks to pause between transfers as per POS-PHY Level 3 specification. These bits are effective in PL3 mode only. The default setting is '00' meaning the minimal pause of 2 dead cycles and one RSX cycle will occur between transfers resulting in maximum bandwidth usage. As setting of '01' indicates 1 additional clock between transfers and a setting of '10' indicates 2 additional clocks between transfers. The setting of '11' is reserved. Note that the additional clock cycles are inserted in the RSX pulse, effectively widening the pulse. These bits cannot be changed during operation and can only be changed when RXPRST is logic one.

Register 0331H: RXPHY Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R	RUNTCELLI	X

RUNTCELLI

In UTOPIA, the RENB was detected as being deasserted before appropriate time at end of the cell transfer. The cell will continue to be transferred as per the Utopia Level 3 specification, but this indicates that there may be a configuration mismatch between the RXPHY and the downstream device. A possible cause is the incorrect setting of the size of the cell expected by this interface. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read.

Register 0332H: RXPHY Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R/W	RUNTCELLE	0

RUNTCELLE

The RUNTCELLE bit is used to enable RUNTCELLI signal to assert a hardware interrupt on the INTB pin. When set to logic 0, the hardware interrupt is masked. When set to logic 1, the hardware interrupt is enabled.

Register 0333H: RXPHY Indirect Burst Size

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	CONFIG_RWB	0
Bit 13	R/W	PHY_ADDR[5]	0
Bit 12	R/W	PHY_ADDR[4]	0
Bit 11	R/W	PHY_ADDR[3]	0
Bit 10	R/W	PHY_ADDR[2]	0
Bit 9	R/W	PHY_ADDR[1]	0
Bit 8	R/W	PHY_ADDR[0]	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	BURST_SIZE[3]	0
Bit 2	R/W	BURST_SIZE[2]	0
Bit 1	R/W	BURST_SIZE[1]	1
Bit 0	R/W	BURST_SIZE[0]	1

The RXPHY Indirect Burst Size register is an indirect address and data register. The register is used only in POS-PHY mode of operation.

BURST_SIZE[3:0]

The BURST_SIZE data register is provided to program the allowable burst size for the PHY. The size of a burst is BURST_SIZE + 1. For example, a BURST_SIZE[3:0] = "0000" indicates a burst size of one block. A block is equal to 16 bytes and takes 4 clocks to transfer. The 4 bits of Burst Size allow the maximum burst to be 16 blocks (256 bytes), per PHY. This register is used only in POS-PHY L3 mode. BURST_SIZE[3:0] defaults to "0011", but this default value is only observable if RFCLK is toggling (else it returns "0000").

PHY_ADDR[5:0]

The PHY_ADDR bits are an indirect address that is used with BURST_SIZE data. The two allow indirect address reads and writes using a small amount of external address space. The PHY_ADDR is used with CONFIG_RWB and BUSY to command reads and writes. Valid values for PHY_ADDR[5:0] are from 0 to 2FH (see section 13.28 on how FIFO number and PL3/UL3 channels are mapped).

CONFIG_RWB

The CONFIG_RWB register allows the indirect addressing method to specify whether a read or write is being performed. A value of '1' means that a read is to be performed on the data for PHY_ADDR and will be placed in the BURST_SIZE register. A value of '0' means that a write of the information in BURST_SIZE will be performed for PHY channel address PHY_ADDR.

BUSY

The BUSY bit is used in indirect addressing to indicate the operation of read or write is currently being executed. A value of '1' means the operation is currently in progress and the microprocessor should wait. A value of '0' means the operation is finished and the microprocessor may proceed with further access.

Register 0334H: RXPHY Calendar Length

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R/W	CALENDAR_LENGTH[6]	0
Bit 5	R/W	CALENDAR_LENGTH[5]	0
Bit 4	R/W	CALENDAR_LENGTH[4]	0
Bit 3	R/W	CALENDAR_LENGTH[3]	0
Bit 2	R/W	CALENDAR_LENGTH[2]	0
Bit 1	R/W	CALENDAR_LENGTH[1]	0
Bit 0	R/W	CALENDAR_LENGTH[0]	0

CALENDAR_LENGTH[6:0]

The CALENDAR_LENGTH register is provided to program the length of calendar used for servicing up to a maximum of 128 entries. (See Register 0335H RXPHY Calendar Indirect Address Data). The number of entries is equal to CALENDAR_LENGTH + 1.

Register 0335H: RXPHY Calendar Indirect Address Data

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	CALENDAR_ADDR[6]	0
Bit 13	R/W	CALENDAR_ADDR[5]	0
Bit 12	R/W	CALENDAR_ADDR[4]	0
Bit 11	R/W	CALENDAR_ADDR[3]	0
Bit 10	R/W	CALENDAR_ADDR[2]	0
Bit 9	R/W	CALENDAR_ADDR[1]	0
Bit 8	R/W	CALENDAR_ADDR[0]	0
Bit 7	R/W	CONFIG_RWB	0
Bit 6	—	Unused	X
Bit 5	R/W	CALENDAR_DATA[5]	X
Bit 4	R/W	CALENDAR_DATA[4]	X
Bit 3	R/W	CALENDAR_DATA[3]	X
Bit 2	R/W	CALENDAR_DATA[2]	X
Bit 1	R/W	CALENDAR_DATA[1]	X
Bit 0	R/W	CALENDAR_DATA[0]	X

The RXPHY Calendar Indirect Address Data register is an indirect address and data register. The register is used in POS mode of operation.

CALENDAR_DATA[5:0]

The CALENDAR_DATA register is provided to program the PHY address number to be serviced in the calendar sequence. The calendar consists of a maximum of 128 entries where the CALENDAR_ADDR is used to access one of the 128 (or less) entries to either write or read CALENDAR_DATA. CALENDAR_DATA is the PHY address to be serviced during the sequence associated with CALENDAR_ADDR. The length of the calendar is set in the RXPHY Calendar Length register. CALENDAR_DATA[5:0] defaults to “000000”, but this default value is only observable if RFCLK is toggling.

CALENDAR_ADDR[6:0]

The CALENDAR_ADDR register is an indirect address register that is used with CALENDAR_DATA register. The two registers together allow indirect address reads and writes using a small amount of external address space. The CALENDAR_ADDR is used with CONFIG_RWB and BUSY to command reads and writes.

CONFIG_RWB

The CONFIG_RWB register allows the indirect addressing method to specify whether a read or write is being performed. A value of '1' means that a read is to be performed on the data at CALENDAR_ADDR and will be placed in the CALENDAR_DATA register. A value of '0' means that a write of the information in CALENDAR_DATA will be performed at address CALENDAR_ADDR.

BUSY

The BUSY bit is used in indirect addressing to indicate the operation of read or write is currently being executed. A value of '1' means the operation is currently in progress and the microprocessor should wait. A value of '0' means the operation is finished and the microprocessor may proceed with further access.

Register 0336H: RXPHY Data Type Field

Bit	Type	Function	Default
Bit 15	R/W	POS_FIELD[7]	0
Bit 14	R/W	POS_FIELD[6]	0
Bit 13	R/W	POS_FIELD[5]	0
Bit 12	R/W	POS_FIELD[4]	0
Bit 11	R/W	POS_FIELD[3]	0
Bit 10	R/W	POS_FIELD[2]	0
Bit 9	R/W	POS_FIELD[1]	0
Bit 8	R/W	POS_FIELD[0]	1
Bit 7	R/W	ATM_FIELD[7]	0
Bit 6	R/W	ATM_FIELD[6]	0
Bit 5	R/W	ATM_FIELD[5]	0
Bit 4	R/W	ATM_FIELD[4]	0
Bit 3	R/W	ATM_FIELD[3]	0
Bit 2	R/W	ATM_FIELD[2]	0
Bit 1	R/W	ATM_FIELD[1]	0
Bit 0	R/W	ATM_FIELD[0]	0

The RXPHY Data Type Field is used in POS-PHY L3 mode of operation only and is provided as a means to identify the type of traffic, ATM or packet, being sent over the POS-PHY L3 interface. Selection of ATM and packet PHYs is done using the POS_SEL bits in the RXSDQ FIFO Indirect Configuration register.

ATM_FIELD[7:0]

The ATM_FIELD register is provided to identify ATM cell transfers over the POS-PHY L3 interface. When the outgoing data is an ATM cell, then the ATM_FIELD[7:0] is inserted in RDAT[31:24] at the cycle in which the in-band address is inserted in RDAT[5:0] (ie. when RSX is logic 1).

POS_FIELD[7:0]

The POS_FIELD register is provided to identify packet data transfers over the POS-PHY L3 interface. When the outgoing data is of type packet, then the POS_FIELD[7:0] is inserted in RDAT[31:24] at the cycle in which the in-band address is inserted in RDAT[5:0] (ie. when RSX is logic 1).

Register 0340H 0740H 0B40H 0F40H: RTDP Indirect Channel Select

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	R/W	Reserved	0
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	CHAN[1]	0
Bit 0	R/W	CHAN[0]	0

CHAN[1:0]

The indirect channel number bits (CHAN[1:0]) indicate the channel to be updated or queried in the indirect access.

Reserved

The Reserved bit should be set to its default value for proper operation.

RWB

The read/write bar (RWB) bit selects between an update operation (write) or a query operation (read). Writing a logic 0 to RWB triggers the update operation of the channel specified by CHAN[1:0] with the information in the RTDP Indirect registers. Writing a logic 1 to RWB triggers a query of the channel specified by CHAN[1:0] and the information is placed in all of the RTDP Indirect Registers.

Note that any write access to RDTP indirect registers during cell/packet flow will momentarily corrupt the outgoing cell or packet.

BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is logic 1 when a write to the Indirect Channel Select register triggers an indirect access and will stay logic 1 until the access is complete. This register should be polled to determine when data from an indirect read operation is available in all the Indirect Data registers or to determine when a new indirect write operation may commence. (Note – BUSY is also logic 1 after reset while the channel provision RAM is being initialized and is cleared when the RAM has completed initialization and the RTDP is ready to accept an indirect access operation to the RAM.)

Register 0341H 0741H 0B41 0F41H: RTDP Indirect Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	POS_SEL	0
Bit 9	R/W	INVERT	0
Bit 8	R/W	STRIP_SEL	0
Bit 7	R/W	DELINDIS	0
Bit 6	R/W	IDLEPASS	0
Bit 5	R/W	CRCPASS	0
Bit 4	R/W	CRC_SEL[1]	1
Bit 3	R/W	CRC_SEL[0]	1
Bit 2	R/W	RXOTYP	0
Bit 1	R/W	DESCRMBL	1
Bit 0	R/W	PROV	0

This register must be initialized before triggering an indirect write, and reflects the value written until the completion of a subsequent indirect channel read operation.

PROV

The processor provision bit (PROV) configures the RTDP to process ATM cells and packets as configured. When PROV is logic 1, the selected channel's processor is enabled. When PROV is logic 0, the selected channel's processor is disabled.

DESCRMBL

The DESCRMBL bit controls the descrambling of the packet or ATM cell payload with the polynomial $x^{43} + 1$. When DESCRMBL is set to logic 0, frame or cell payload descrambling is disabled. When DESCRMBL is set to logic 1, payload descrambling is enabled.

RXOTYP

The RXOTYP determines if an incoming AIS-P alarm signal (from APS or Rx Line, depending on data path configuration) will stop a packet by simply asserting EOP or by asserting EOP and ERR. When RXOTYP is set to logic zero, the abort sequence is inserted generating a user abort error. When the RXOTYP is set to logic one, the frame processor performs a simple flag insertion and thus the packet will be flagged as an FCS error.

This bit is only valid when processing packets. When processing ATM cells, the RTDP will finish processing any cell in progress and then stop until the alarm is cleared.

Note that the packet transfer may be paused until the alarm is removed before being terminated (either with just REOP or with REOP and RERR depending on the RXOTYP setting).

CRC_SEL[1:0]

The CRC select (CRC_SEL[1:0]) bits allow the control of the CRC calculation according to the table below. For ATM cells, the CRC is calculated over the first four ATM header bytes. For packet applications, the CRC is calculated over the whole packet data, after bit/byte destuffing and descrambling.

Table 17 Functionality of the CRC_SEL[1 0] Register Bits

CRC_SEL[1:0]	HCS Operation	FCS Operation
00	Reserved	No FCS verification
01	Reserved	Reserved
10	CRC-8 without coset polynomial	CRC-CCITT (2 bytes)
11	CRC-8 with coset polynomial added	CRC-32 (4 bytes)

CRCPASS

The CRCPASS bit controls the dropping of cells and packets based on the detection of an CRC error.

When processing ATM cells and when CRCPASS is a logic 0, cells containing an HCS error are dropped and the HCS verification state machine transitions to the 'Detection Mode'. When CRCPASS is a logic 1, cells are passed to the external FIFO interface regardless of errors detected in the HCS. Additionally, the HCS verification finite state machine will never lose cell delineation.

When processing packets and when CRCPASS is logic 1, then packets with FCS errors are not marked as such and are passed to the external FIFO interface as if no FCS error occurred. When CRCPASS is logic 0, then packets with FCS errors are marked using ERR.

Note that ATM idle cells which contain HCS errors will cause the state machine to change state regardless of the setting of the IDLEPASS register bit.

Regardless of the programming of this bit, ATM cells are always dropped while the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states unless the DELINDIS bit in this register is set to logic 1.

IDLEPASS

The IDLEPASS bit controls the function of the ATM Idle Cell filter. It is only valid when processing ATM cells. When IDLEPASS is written with a logic 0, all cells that match the Idle Cell Header Pattern and Idle Cell Header Mask are filtered out. When IDLEPASS is a logic 1, the Idle Cell Header Pattern and Mask register bits are ignored. The default state of this bit and the bits in the RTDP Idle Cell Header and Mask Register enable the dropping of idle cells.

DELINDIS

The DELINDIS bit can be used to disable all HDLC flag alignment. All payload data read by the RTDP is passed to the FIFO interface without the requirement of having to find packet delineation first. DELINDIS is only valid in POS mode.

This bit should only be set when Transparent Data Mode is desired. In this mode, data is passed directly from the TelecomBus payload to the POS-PHY Level 3 Bus without flag delineation, byte or bit de-stuffing or CRC checking. Use of Transparent mode requires the use of 64 byte packets, and the CRC_SEL bits must be set to “00”.

STRIP_SEL

The indirect frame check sequence stripping bit (STRIP_SEL) configures the RTDP to remove the CRC from the outgoing packet. When STRIP_SEL is logic 1 and CRC_SEL[1:0] is not equal to "00" (no CRC), the received packet FCS byte(s) or ATM cell HCS byte(s) are not transferred over the FIFO interface. When STRIP_SEL is set to logic 0, the received packet FCS are transferred over the FIFO interface. **The STRIP_SEL bit must be set to logic 1 if working in ATM mode.**

INVERT

The data inversion bit (INVERT) configures the processor to logically invert the incoming stream before processing it. When INVERT is set to logic 1, the stream is logically inverted before processing. When INVERT is set to logic 0, the stream is not inverted before processing.

POS_SEL

The ATM/POS selection bit (POS_SEL) configures the RTDP for operation in ATM or packet mode. When POS_SEL is logic 1, then packet mode is selected. When POS_SEL is logic 0, then ATM mode is selected.

Reserved

The Reserved bits should be set to logic 0 for proper operation.

Register 0342H 0742H 0B42 0F42H: RTDP Indirect Minimum Packet Length and Bit Order

Bit	Type	Function	Default
Bit 15	R/W	MINPL[7]	0
Bit 14	R/W	MINPL[6]	0
Bit 13	R/W	MINPL[5]	0
Bit 12	R/W	MINPL[4]	0
Bit 11	R/W	MINPL[3]	0
Bit 10	R/W	MINPL[2]	1
Bit 9	R/W	MINPL[1]	0
Bit 8	R/W	MINPL[0]	0
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	BIT_ABRTE	0
Bit 3	R/W	RBY_MODE	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	0

This register must be initialized before triggering an indirect write, and reflects the value written until the completion of a subsequent indirect channel read operation.

Reserved

The Reserved bits should be set to their default value for proper operation.

RBY_MODE

The receive byte counter mode (RBY_MODE) bit is used to select the mode in which the RBY_IC[31:0] counters work. When RBY_MODE is logic 0, RBY_IC[31:0] will count all bytes in received packets (including FCS and Abort bytes) after the byte destuffing operation. When RBY_MODE is logic 1, RBY_IC[31:0] will count all bytes in received packets (including FCS, Abort, and stuff bytes) before the byte destuffing operation. Flag bytes will not be counted in either case. The RBY_MODE bit is only valid when working in byte-stuffed POS mode. RBY_MODE must be set to logic 0 for bit-stuffed HDLC mode and is invalid for the ATM mode.

BIT_ABRTE

The Bit Abort Sequence Abort Enable (BIT_ABRTE) is used to enable counts of errors caused by a one byte packet consisting only of an bit-stuffed abort sequence (at least seven ones) when in bit de-stuffed packet mode. When BIT_ABRTE = 0, a flag followed by an abort sequence will generate a set of error conditions which will be counted as erroneous FCS, Min Packet length and Aborted packet counters. When BIT_ABRTE = 1, the same sequence will not cause the error counters to increment. When the all-ones sequence is being used as idle space between packets, enabling this bit prevents spurious error counts from being generated. Note that this bit does not block associated error interrupts (MINLI, UCRCI, ABRTI) which should be disabled on a channel by channel basis when all-ones sequences are used as idle.

MINPL[7:0]

The Minimum Packet Length (MINPL[7:0]) bits are used to set the minimum packet length. Packets smaller than this length are marked with an error. The packet length used here is defined as the number of bytes encapsulated into the frame after destuffing but including the FCS. The default minimum packet length is 4 octets. Values smaller than 4 should not be used.

Register 0343H 0743H 0B43H 0F43H: RTDP Indirect Maximum Packet Length

Bit	Type	Function	Default
Bit 15	R/W	MAXPL[16]	0
Bit 14	R/W	MAXPL[15]	0
Bit 13	R/W	MAXPL[14]	0
Bit 12	R/W	MAXPL[13]	0
Bit 11	R/W	MAXPL[12]	0
Bit 10	R/W	MAXPL[11]	0
Bit 9	R/W	MAXPL[10]	1
Bit 8	R/W	MAXPL[9]	1
Bit 7	R/W	MAXPL[8]	0
Bit 6	R/W	MAXPL[7]	0
Bit 5	R/W	MAXPL[6]	0
Bit 4	R/W	MAXPL[5]	0
Bit 3	R/W	MAXPL[4]	0
Bit 2	R/W	MAXPL[3]	0
Bit 1	R/W	MAXPL[2]	0
Bit 0	R/W	MAXPL[1]	0

This register must be initialized before triggering an indirect write, and reflects the value written until the completion of a subsequent indirect channel read operation.

MAXPL[16:0]

The Maximum Packet Length (MAXPL[16:0]) bits are used to set the maximum packet length. MAXPL[0] is set equal to 0. Packets larger than this length are marked with an error. The packet length used here is defined as the number of bytes encapsulated into the POS frame after destuffing but including the FCS bytes. The default maximum packet length is 1536 octets.

Register 0344H 0744H 0B44 0F44H: RTDP Indirect LCD Count Threshold

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	R/W	LCDC[10]	0
Bit 9	R/W	LCDC[9]	0
Bit 8	R/W	LCDC[8]	1
Bit 7	R/W	LCDC[7]	0
Bit 6	R/W	LCDC[6]	1
Bit 5	R/W	LCDC[5]	1
Bit 4	R/W	LCDC[4]	0
Bit 3	R/W	LCDC[3]	1
Bit 2	R/W	LCDC[2]	0
Bit 1	R/W	LCDC[1]	0
Bit 0	R/W	LCDC[0]	0

This register must be initialized before triggering an indirect write, and reflects the value written until the completion of a subsequent indirect channel read operation.

LCDC[10:0]

The LCDC[10:0] bits represent the number of consecutive cell periods the receive cell processor must be out of cell delineation before loss of cell delineation (LCD) is declared. Likewise, LCD is not deasserted until the receive cell processor is in cell delineation for the number of cell periods specified by LCDC[10:0].

The default value of LCD[10:0] is 360, which translates to the following:

Format	Average Cell Period	Default LCD Integration Period
STS-3c	2.83 μs	1018.8 μs

Register 0345H 0745H 0B45H 0F45H: RTDP Indirect Idle Cell Header and Mask

Bit	Type	Function	Default
Bit 15	R/W	GFC[3]	0
Bit 14	R/W	GFC[2]	0
Bit 13	R/W	GFC[1]	0
Bit 12	R/W	GFC[0]	0
Bit 11	R/W	PTI[3]	0
Bit 10	R/W	PTI[2]	0
Bit 9	R/W	PTI[1]	0
Bit 8	R/W	CLP	1
Bit 7	R/W	MGFC[3]	1
Bit 6	R/W	MGFC[2]	1
Bit 5	R/W	MGFC[1]	1
Bit 4	R/W	MGFC[0]	1
Bit 3	R/W	MPTI[3]	1
Bit 2	R/W	MPTI[2]	1
Bit 1	R/W	MPTI[1]	1
Bit 0	R/W	MCLP	1

This register must be initialized before triggering an indirect write, and reflects the value written until the completion of a subsequent indirect channel read operation.

MCLP

The CLP bit contains the mask pattern for the eighth bit of the fourth octet of the 53-octet cell. This mask is applied to this register to select the bits included in the cell filter. A logic 1 in this bit position enables the CLP bit in the pattern register to be compared. A logic zero causes the masking of the CLP bit.

MPTI[3:0]

The MPTI[3:0] bits contain the mask pattern for the fifth, sixth, and seventh bits of the fourth octet of the 53-octet cell. This mask is applied to the Idle Cell Header Pattern Register to select the bits included in the cell filter. A logic 1 in any bit position enables the corresponding bit in the pattern register to be compared. A logic zero causes the masking of the corresponding bit.

MGFC[3:0]

The MGFC[3:0] bits contain the mask pattern for the first, second, third, and fourth bits of the first octet of the 53-octet cell. This mask is applied to the Idle Cell Header Pattern Register to select the bits included in the cell filter. A logic 1 in any bit position enables the corresponding bit in the pattern register to be compared. A logic zero causes the masking of the corresponding bit.

GFC[3:0]

The GFC[3:0] bits contain the pattern to match in the first, second, third, and fourth bits of the first octet of the 53-octet cell, in conjunction with the Idle Cell Header Mask Register. The IDLEPASS bit in the Configuration Register must be set to logic zero to enable dropping of cells matching this pattern. Note that an all-zeros pattern must be present in the VPI and VCI fields of the idle or unassigned cell.

PTI[2:0]

The PTI[2:0] bits contain the pattern to match in the fifth, sixth, and seventh bits of the fourth octet of the 53-octet cell, in conjunction with the Idle Cell Header Mask Register. The IDLEPASS bit in the Configuration Register must be set to logic zero to enable dropping of cells matching this pattern.

CLP

The CLP bit contains the pattern to match in the eighth bit of the fourth octet of the 53-octet cell, in conjunction with the Match Header Mask Register. The IDLEPASS bit in the Configuration Register must be set to logic zero to enable dropping of cells matching this pattern.

Register 0346H 0746H 0B46H 0F46H: RTDP Indirect Receive Byte/Idle Cell Counter (LSB)

Bit	Type	Function	Default
Bit 15	R	RBY_IC[15]	X
Bit 14	R	RBY_IC[14]	X
Bit 13	R	RBY_IC[13]	X
Bit 12	R	RBY_IC[12]	X
Bit 11	R	RBY_IC[11]	X
Bit 10	R	RBY_IC[10]	X
Bit 9	R	RBY_IC[9]	X
Bit 8	R	RBY_IC[8]	X
Bit 7	R	RBY_IC[7]	X
Bit 6	R	RBY_IC[6]	X
Bit 5	R	RBY_IC[5]	X
Bit 4	R	RBY_IC[4]	X
Bit 3	R	RBY_IC[3]	X
Bit 2	R	RBY_IC[2]	X
Bit 1	R	RBY_IC[1]	X
Bit 0	R	RBY_IC[0]	X

Register 0347H 0747H 0B47H 0F47H: RTDP Indirect Receive Byte/Idle Cell Counter (MSB)

Bit	Type	Function	Default
Bit 15	R	RBY_IC[31]	X
Bit 14	R	RBY_IC[30]	X
Bit 13	R	RBY_IC[29]	X
Bit 12	R	RBY_IC[28]	X
Bit 11	R	RBY_IC[27]	X
Bit 10	R	RBY_IC[26]	X
Bit 9	R	RBY_IC[25]	X
Bit 8	R	RBY_IC[24]	X
Bit 7	R	RBY_IC[23]	X
Bit 6	R	RBY_IC[22]	X
Bit 5	R	RBY_IC[21]	X
Bit 4	R	RBY_IC[20]	X
Bit 3	R	RBY_IC[19]	X
Bit 2	R	RBY_IC[18]	X
Bit 1	R	RBY_IC[17]	X
Bit 0	R	RBY_IC[16]	X

RBY_IC[31:0]

When packet mode is selected, the RBY_IC[31:0] bits indicate the number of bytes received within frames during the last accumulation interval. The byte counts include all user payload bytes, FCS bytes, and abort bytes. Inclusion of stuffed bytes in the count is controlled by the RBY_MODE register bit. HDLC flags are not counted.

When ATM mode is selected, the RBY_IC[31:0] bits indicate the number of Idle cells received and passed to the FIFO interface in the last accumulation interval.

A direct write to any one of the RTDP counter registers loads all the corresponding RTDP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0002H can be written to initiate a global performance counter update across the S/UNI MULTI-48. Note that only counters for channels that are provisioned and enabled in the RTDP and RCAS12 will be updated.

Register 0348H 0748H 0B48H 0F48H: RTDP Indirect Packet/Cell Counter (LSB)

Bit	Type	Function	Default
Bit 15	R	RP_RC[15]	X
Bit 14	R	RP_RC[14]	X
Bit 13	R	RP_RC[13]	X
Bit 12	R	RP_RC[12]	X
Bit 11	R	RP_RC[11]	X
Bit 10	R	RP_RC[10]	X
Bit 9	R	RP_RC[9]	X
Bit 8	R	RP_RC[8]	X
Bit 7	R	RP_RC[7]	X
Bit 6	R	RP_RC[6]	X
Bit 5	R	RP_RC[5]	X
Bit 4	R	RP_RC[4]	X
Bit 3	R	RP_RC[3]	X
Bit 2	R	RP_RC[2]	X
Bit 1	R	RP_RC[1]	X
Bit 0	R	RP_RC[0]	X

Register 0349H 0749H 0B49H 0F49H: RTDP Indirect Packet/Cell Counter (MSB)

Bit	Type	Function	Default
Bit 15	R	RP_RC[31]	X
Bit 14	R	RP_RC[30]	X
Bit 13	R	RP_RC[29]	X
Bit 12	R	RP_RC[28]	X
Bit 11	R	RP_RC[27]	X
Bit 10	R	RP_RC[26]	X
Bit 9	R	RP_RC[25]	X
Bit 8	R	RP_RC[24]	X
Bit 7	R	RP_RC[23]	X
Bit 6	R	RP_RC[22]	X
Bit 5	R	RP_RC[21]	X
Bit 4	R	RP_RC[20]	X
Bit 3	R	RP_RC[19]	X
Bit 2	R	RP_RC[18]	X
Bit 1	R	RP_RC[17]	X
Bit 0	R	RP_RC[16]	X

RP_RC[31:0]

When packet mode is selected, the RP_RC[31:0] bits indicate the number of good packets received and passed to the FIFO interface during the last accumulation interval.

When ATM mode is selected, the RP_RC[31:0] bits indicate the number of received ATM cells received and passed to the FIFO interface in the last accumulation interval.

A direct write to any one of the RTDP counter registers loads all the corresponding RTDP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0002H can be written to initiate a global performance counter update across the S/UNI MULTI-48. Note that only counters for channels that are provisioned and enabled in the RTDP and RCAS12 will be updated.

Register 034AH 074AH 0B4AH 0F4AH: RTDP Indirect Receive Erroneous FCS/HCS Counter

Bit	Type	Function	Default
Bit 15	R	EFCS[15]	X
Bit 14	R	EFCS[14]	X
Bit 13	R	EFCS[13]	X
Bit 12	R	EFCS[12]	X
Bit 11	R	EFCS[11]	X
Bit 10	R	EFCS[10]	X
Bit 9	R	EFCS[9]	X
Bit 8	R	EFCS[8]	X
Bit 7	R	EFCS[7]/UHCS[7]	X
Bit 6	R	EFCS[6]/UHCS[6]	X
Bit 5	R	EFCS[5]/UHCS[5]	X
Bit 4	R	EFCS[4]/UHCS[4]	X
Bit 3	R	EFCS[3]/UHCS[3]	X
Bit 2	R	EFCS[2]/UHCS[2]	X
Bit 1	R	EFCS[1]/UHCS[1]	X
Bit 0	R	EFCS[0]/UHCS[0]	X

EFCS[15:0]

When packet mode is selected, the EFCS[15:0] bits indicate the number of received FCS errors during the last accumulation interval.

UHCS[7:0]

When ATM mode is selected, the UHCS[7:0] bits indicate the number of uncorrectable HCS errors received in the last accumulation interval. Note that the last HCS error that causes the cell processor to enter the HUNT state will not be reflected in the count. This differs from the operation of the RCFP.

A direct write to any one of the RTDP counter registers loads all the corresponding RTDP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0002H can be written to initiate a global performance counter update across the S/UNI MULTI-48. Note that only counters for channels that are provisioned and enabled in the RTDP and RCAS12 will be updated.

Register 034BH 074BH 0B4BH 0F4BH: RTDP Indirect Receive Aborted Packet Counter

Bit	Type	Function	Default
Bit 15	R	RABR[15]	X
Bit 14	R	RABR[14]	X
Bit 13	R	RABR[13]	X
Bit 12	R	RABR[12]	X
Bit 11	R	RABR[11]	X
Bit 10	R	RABR[10]	X
Bit 9	R	RABR[9]	X
Bit 8	R	RABR[8]	X
Bit 7	R	RABR[7]	X
Bit 6	R	RABR[6]	X
Bit 5	R	RABR[5]	X
Bit 4	R	RABR[4]	X
Bit 3	R	RABR[3]	X
Bit 2	R	RABR[2]	X
Bit 1	R	RABR[1]	X
Bit 0	R	RABR[0]	X

RABR[15:0]

When packet mode is selected, the RABR[15:0] bits indicate the number of aborted packets received during the last accumulation interval. This counter is held at value 0 when ATM mode is selected.

A direct write to any one of the RTDP counter registers loads all the corresponding RTDP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0002H can be written to initiate a global performance counter update across the S/UNI MULTI-48. Note that only counters for channels that are provisioned and enabled in the RTDP and RCAS12 will be updated.

Register 034CH 074CH 0B4CH 0F4CH: RTDP Indirect Receive Minimum Length Packet Error Counter

Bit	Type	Function	Default
Bit 15	R	RMINL[15]	X
Bit 14	R	RMINL[14]	X
Bit 13	R	RMINL[13]	X
Bit 12	R	RMINL[12]	X
Bit 11	R	RMINL[11]	X
Bit 10	R	RMINL[10]	X
Bit 9	R	RMINL[9]	X
Bit 8	R	RMINL[8]	X
Bit 7	R	RMINL[7]	X
Bit 6	R	RMINL[6]	X
Bit 5	R	RMINL[5]	X
Bit 4	R	RMINL[4]	X
Bit 3	R	RMINL[3]	X
Bit 2	R	RMINL[2]	X
Bit 1	R	RMINL[1]	X
Bit 0	R	RMINL[0]	X

This register must be initialized before triggering an indirect write, and reflects the value written until the completion of a subsequent indirect channel read operation.

RMINL[15:0]

When packet mode is selected, the RMINL[15:0] bits indicate the number of minimum length packet errors received during the last accumulation interval. This counter is held at value 0 when ATM mode is selected. Note that malformed packets smaller than 4 bytes will not be counted in this register.

A direct write to any one of the RTDP counter registers loads all the corresponding RTDP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0002H can be written to initiate a global performance counter update across the S/UNI MULTI-48. Note that only counters for channels that are provisioned and enabled in the RTDP and RCAS12 will be updated.

Register 034DH 074DH 0B4DH 0F4DH: RTDP Indirect Receive Maximum Length Packet Error Counter

Bit	Type	Function	Default
Bit 15	R	RMAXL[15]	X
Bit 14	R	RMAXL[14]	X
Bit 13	R	RMAXL[13]	X
Bit 12	R	RMAXL[12]	X
Bit 11	R	RMAXL[11]	X
Bit 10	R	RMAXL[10]	X
Bit 9	R	RMAXL[9]	X
Bit 8	R	RMAXL[8]	X
Bit 7	R	RMAXL[7]	X
Bit 6	R	RMAXL[6]	X
Bit 5	R	RMAXL[5]	X
Bit 4	R	RMAXL[4]	X
Bit 3	R	RMAXL[3]	X
Bit 2	R	RMAXL[2]	X
Bit 1	R	RMAXL[1]	X
Bit 0	R	RMAXL[0]	X

This register must be initialized before triggering an indirect write, and reflects the value written until the completion of a subsequent indirect channel read operation.

RMAXL[15:0]

When packet mode is selected, the RMAXL[15:0] bits indicate the number of maximum length packet errors received during the last accumulation interval. This counter is held at value 0 when ATM mode is selected.

A direct write to any one of the RTDP counter registers loads all the corresponding RTDP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0002H can be written to initiate a global performance counter update across the S/UNI MULTI-48. Note that only counters for channels that are provisioned and enabled in the RTDP and RCAS12 will be updated.

Register 0350H 0750H 0B50H 0F50H + *n*: RTDP Interrupt Enable (*n* = 0, 1)

Bit	Type	Function	Default
Bit 15	R/W	XFERE	0
Bit 14	R/W	MINLE_***2n+1***	0
Bit 13	R/W	MAXLE_***2n+1***	0
Bit 12	R/W	ABRTE_***2n+1***	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	UCRCE_***2n+1***	0
Bit 9	R/W	OOFE_***2n+1***	0
Bit 8	R/W	LOFE_***2n+1***	0
Bit 7	—	Unused	X
Bit 6	R/W	MINLE_***2n***	0
Bit 5	R/W	MAXLE_***2n***	0
Bit 4	R/W	ABRTE_***2n***	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	UCRCE_***2n***	0
Bit 1	R/W	OOFE_***2n***	0
Bit 0	R/W	LOFE_***2n***	0

The channel mapping for these registers is as follows:

n	RTDP Register	Channel Number for 2n	Channel Number for 2n+1
0	0350H 0750H 0B50H 0F50H	0	1
1	0351H 0751H 0B51H 0F51H	2	3

LOFE

The LOFE bit enables the generation of an interrupt due to a change in the ATM LCD state. When LOFE is set to logic 1, the interrupt is enabled.

OOFE

The OOFE bit enables the generation of an interrupt due to a change in ATM cell delineation state or packet alignment state. When OOFE is set to logic 1, the interrupt is enabled.

CRCE

The CRCE bit enables the generation of an interrupt due to the detection of an ATM HCS or packet FCS error. When CRCE is set to logic 1, the interrupt is enabled.

ABRTE

The Abort Packet Enable bit enables the generation of an interrupt due to the reception of an aborted packet. When ABRTE is set to logic 1, the interrupt is enabled.

MAXLE

The Maximum Length Packet Enable bit enables the generation of an interrupt due to the reception of a packet exceeding the programmable maximum packet length. When MAXLE is set to logic 1, the interrupt is enabled.

MINLE

The Minimum Length Packet Enable bit enables the generation of an interrupt due to the reception of a packet that is smaller than the programmable minimum packet length. When MINLE is set to logic 1, the interrupt is enabled.

XFERE

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the RTDP performance monitor counter holding registers. When XFERE is set to logic 1, the interrupt is enabled. XFERE is only available at registers 0350H, 0750H, 0B50H and 0F50H.

Register 0356H 0756H 0B56H 0F56H + *n*: RTDP Interrupt Indication (*n* = 0, 1)

Bit	Type	Function	Default
Bit 15	R	XFERI	X
Bit 14	R	MINLI_***2n+1***	X
Bit 13	R	MAXLI_***2n+1***	X
Bit 12	R	ABRTI_***2n+1***	X
Bit 11	R	Reserved	X
Bit 10	R	CRCI_***2n+1***	X
Bit 9	R	OOFI_***2n+1***	X
Bit 8	R	LOFI_***2n+1***	X
Bit 7	—	Unused	X
Bit 6	R	MINLI_***2n***	X
Bit 5	R	MAXLI_***2n***	X
Bit 4	R	ABRTI_***2n***	X
Bit 3	R	Reserved	X
Bit 2	R	CRCI_***2n***	X
Bit 1	R	OOFI_***2n***	X
Bit 0	R	LOFI_***2n***	X

The channel mapping for these registers is as follows:

n	RTDP Register	Channel Number for 2n	Channel Number for 2n+1
0	0356H 0756H 0B56H 0F56H	0	1
1	0357H 0757H 0B57H 0F57H	2	3

LOFI

The LOFI bit is logic 1 when there is a change in the loss of cell delineation (LCD) state for the channel. The current value of the LCD is available in the LOFV bits in the RTDP LOF Status register. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read.

OOFI

The OOFI bit is logic 1 when the RTDP ATM cell processor for the channel enters or exits the SYNC state or the packet processor finds a new flag alignment. The current value of the out-of-delineation state is available in the OOFV bits in the RTDP OOF Status register. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read.

CRCI

The CRCI bit is logic 1 when an ATM HCS or packet FCS error is detected on the channel. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read.

ABRTI

The ABRTI bit indicates bit enables the generation of an interrupt due to the reception of an aborted packet. This interrupt can be masked using ABRTE for the channel. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read.

MAXLI

The MAXLI bit indicates an interrupt due to the reception of a packet exceeding the programmable maximum packet length. This interrupt can be masked using MAXLE for the channel. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read.

MINLI

The MINLI bit indicates an interrupt due to the reception of a packet that is smaller than the programmable minimum packet length. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read. Note that although packets smaller than 4 bytes will not increment the RMINL counter, they will cause the MINLI interrupt.

XFERI

The XFERI bit indicates that a transfer of accumulated counter data has occurred on the channel. A logic 1 in this bit position indicates that the RTDP performance monitor counter holding registers have been updated. This update is initiated by writing to one of the counter register locations, or by writing to register 0002H for global performance monitor update. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read. XFERI is only available at registers 0356H 0756H 0B56H 0F56H.

Register 035CH 075CH 0B5CH 0F5CH: RTDP OOF Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	OOFV_3	X
Bit 2	R	OOFV_2	X
Bit 1	R	OOFV_1	X
Bit 0	R	OOFV_0	X

OOFV_***x***

The OOFV_***x*** bit indicates the ATM cell delineation or packet Idle state for channel ***x***. When OOFV_***x*** is logic 1, the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states and is hunting for the cell boundaries or the packet processor has not found a flag alignment. When OOFV_***x*** is logic 0, the cell delineation state machine is in the 'SYNC' state or the packet processor is frame aligned.

Register 035DH 075DH 0B5DH 0F5DH: RTDP LOF Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	LOFV_3	X
Bit 2	R	LOFV_2	X
Bit 1	R	LOFV_1	X
Bit 0	R	LOFV_0	X

LOFV_***x***

The LOFV_***x*** bit gives the ATM Loss of Cell Delineation state for channel ***x***. When LOF is logic 1, an out of cell delineation (OOF) defect has persisted for the number of cells specified in the LCD Count Threshold register. When LOFV_***x*** is logic 0, the RTDP has been in cell delineation for the number of cells specified in the LCD Count Threshold register. The cell time period can be varied by using the LCDC[10:0] register bits in the RTDP LCD Count Threshold register.

When in bit-stuffed HDLC mode, LOFV_***x*** shows the Idle status of the channel. If LOFV_***x*** is logic 1, then the channel is currently in Idle state.

Register 0360H 0760H 0B60H 0F60H: RCAS12 Channel Disable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	1
Bit 10	R/W	Reserved	1
Bit 9	R/W	Reserved	1
Bit 8	R/W	Reserved	1
Bit 7	R/W	Reserved	1
Bit 6	R/W	Reserved	1
Bit 5	R/W	Reserved	1
Bit 4	R/W	Reserved	1
Bit 3	R/W	CH3_DIS	1
Bit 2	R/W	CH2_DIS	1
Bit 1	R/W	CH1_DIS	1
Bit 0	R/W	CH0_DIS	1

CH***x***_DIS

The Channel ***x*** disable bit (CH***x***_DIS) controls the squelching of data directed to Channel ***x***. When CH***x***_DIS is logic 1, the RCAS12 will disable transfer of any data to Channel ***x***. When CH***x***_DIS is logic 0, data is transferred to Channel ***x*** normally.

Register 0361H 0761H 0B61H 0F61H: RCAS12 Channel Loopback Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	R/W	STS12C_LBEN	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	CH3_LBEN	0
Bit 2	R/W	CH2_LBEN	0
Bit 1	R/W	CH1_LBEN	0
Bit 0	R/W	CH0_LBEN	0

CH***x***_LBEN

The Channel ***x*** diagnostic loopback enable bit (CH***x***_LBEN) is used to enable a diagnostic loopback from the transmit Channel ***x*** data stream to the receive Channel ***x*** data stream. When CH***x***_LBEN is logic 1, the receive data directed to Channel ***x*** is to be over-written by data retrieved from the loopback FIFO of Channel ***x***. When CH***x***_LBEN is logic 0, the loopback is disabled.

STS12C_LBEN

The STS12C_LBEN bit should be set to logic 1 (along with the corresponding CH**x**_LBEN bit) for per-channel diagnostic loopback when the RCAS12 is processing one STS-12c channel or part of one STS-48c channel. It should be set to logic 0 if the RCAS12 is not enabled for per-channel diagnostic loopback with an STS-12c or STS-48c channel.

Register 0362H 0762H 0B62H 0F62H + *x*: RCAS12 Timeslot *x* Configuration (*x* = 0H to BH)

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	R/W	Reserved	0
Bit 7	R/W	TS***x***_MODE[2]	0
Bit 6	R/W	TS***x***_MODE[1]	0
Bit 5	R/W	TS***x***_MODE[0]	0
Bit 4	R/W	TS***x***_PROV	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	TS***x***_CHAN[1]	0
Bit 0	R/W	TS***x***_CHAN[0]	0

TSx_CHAN[1:0]

The TS***x***_CHAN[1:0] bits give the channel number to which the input data stream in timeslot ***x*** is directed to.

TSx_PROV

The TS***x***_PROV bit provisions and unprovisions the timeslot. When TS***x***_PROV is logic 1, the receive data stream on timeslot ***x*** is processed as part of the channel as indicated by TS***x***_CHAN. When TS***x***_PROV is logic 0, the receive data stream on timeslot ***x*** does not belong to any channel and is ignored.

TS*x*_MODE[2:0]

The TS*x*_MODE[2:0] bits identify the type of traffic carried on timeslot ***x***. All timeslots associated with a concatenated payload channel must be set up appropriately as shown in Table 18.

Table 18 RCAS12 Timeslot Mode Selection

TS*x*_MODE[2:0]	Line Traffic Type
000	STS-48c/VC-4-16c or STS-12c/VC-4-4c
001	STS-3c/VC-4
010	Reserved
011	Reserved
100	Reserved
101	Reserved
110	Reserved
111	Reserved

Register 0370H 0770H 0B70H 0F70H: SFBA Configuration and Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R	LOTV	X
Bit 2	R/W	LOT_SEL	0
Bit 1	R/W	SD_EN	1
Bit 0	R/W	SD_INV	0

LOTV

The loss of transition status indicates the receive power is lost or a bit sequence of 97 or more consecutive ones or zeros have been received. LOTV is a logic zero if valid receive power is detected on the SD input and no bit sequence of 97 or more consecutive ones or zeros have been received. LOTV is logic one if a loss of power is detected on the SD input or a bit sequence of 97 or more consecutive ones or zeros has been received.

LOT_SEL

The loss of transition selector (LOT_SEL) bit selects if the declaration of loss of transition (LOT) is triggered by the data and SD signal or only the SD signal. When LOT_SEL is a logic zero, a loss of transition is declared when a bit sequence of 97 or more consecutive ones or zeros occurs in the receive data or when a loss of power is detected on the SD input. When LOT_SEL is logic one, a loss of signal is declared only when a loss of power is detected on the SD input.

Note that when the Signal Detect Enable (SD_EN) bit is set to logic zero (i.e. the SD input is ignored) and the LOT_SEL is a logic one, no loss of transition can be declared.

SD_EN

The Signal Detect Enable (SD_EN) bit enables the SD input signal. When SD_EN is set to logic 1, the SD input is enabled. When SD_EN is set to logic 0, the SD input is ignored. This bit must be set to logic 0 when S/UNI MULTI-48 is in Serial Diagnostic Loopback mode (SDLE622) and DCRU155_622 is enabled (DCRU155_622EN[x]).

Note: When the SD_EN bit is set to logic 0, it is possible for LOT not to be detected in the absence of an optical input signal. Disabling the SD_EN bit masks the SD[x] input and forces the S/UNI MULTI-48 to declare LOT only based on an all '0' or all '1' input pattern (if LOT_SEL is set to logic 0). However, noise on AC coupled RXD[1-4] inputs can cause transitions preventing detection of an all '0' or all '1' pattern. To avoid this, enable the SD_EN bit and connect the SD[x] input signal to the optical module's SD or LOS output. This will allow LOT to be detected when the optical input signal is lost.

SD_INV

The signal detect input invert (SD_INV) controls the polarity of the SD input. The value of the SD input is logically XOR'ed with the value of the SD_INV register. Therefore, when SD_INV is a logic zero, valid signal power is indicated by the SD input high. When SD_INV is logic one, the SD input low indicates valid signal power.

Register 0371H 0771H 0B71H 0F71H: SFBA Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R/W	LOTE	0

LOTE

The LOTE bit enables the loss of transition indication interrupt. When LOTE is set high, an interrupt is generated upon assertion events of the LOTV register. When LOTE is set low, changes in the LOTV status does not generate an interrupt.

Register 0372H 0772H 0B72H 0F72H: SFBA Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R	LOTI	X

Clear mode of interrupts depends on the WCIMODE input value. When WCIMODE is zero, all the interrupts are cleared when they are read. When WCIMODE is one, a given interrupt is cleared only if logic one is being written in its corresponding bit.

LOTI

The LOTI bit is the loss of transition interrupt status bit. LOTI is set high when a loss of transition event occurs. A Loss Of Transition is defined as either a loss of power detected on the SD input or a bit sequence of 97 or more consecutive ones or zeros received on RDATA [7:0]. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read. If the LOTE interrupt enable is logic one, the INT output is also asserted with LOTI asserted.

Register 0380H 0780H 0B80H 0F80H: DCRU155_622 Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved Reserved	0
Bit 5	R/W	Reserved	1
Bit 4	R/W	DCC_ENB	1
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved1	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Reserved

The Reserved bits must be set to their default value for proper operation.

Reserved1

The Reserved1 bits must be set to logic 1 for proper operation.

DCC_ENB

The Duty Cycle Correction Enable (DCC_ENB) control enables the duty cycle correction circuit in the phase detector. When DCC_ENB is low, the duty cycle correction circuit is enabled. When DCC_ENB is high, the duty cycle correction circuit is disabled. This bit should be set to logic 0 when the serial diagnostic loopback is enabled and DCRU155_622 is enabled. This bit should be set to logic 1 in all other cases.

Register 0381H 0781H 0B81H 0F81H: DCRU155_622 Status and Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	1
Bit 5	—	Unused	X
Bit 4	R	RUN	X
Bit 3	R	Reserved	X
Bit 2	R	ERROR	X
Bit 1	R/W	Reserved	0
Bit 0	R/W	ERRORE	0

Reserved

The Reserved bits must be set to their default value for proper operation.

ERRORE

The ERROR interrupt enable (ERRORE) bit enables the error indication interrupt. When ERRORE is set high, an interrupt is generated upon assertion event ERROR register bit. When ERRORE is set low, changes in the ERROR status do not generate an interrupt.

ERROR

The delay line error register bit (ERROR) indicates the DLL has run out of dynamic range. When the DLL attempts to move beyond the end of the delay line, ERROR is set high. When ERROR is high, the DLL cannot generate a recovered clock locked to the serial data stream. ERROR is set low when the DCRU may again try to recover the data stream.

RUN

The DLL lock status register bit (RUN) indicates the DLL found a delay line tap in which the phase difference between the rising edge of the reference clock and the rising edge of the generated clock is zero. After system reset, RUN is logic zero until the phase detector indicates an initial lock condition. When the phase detector indicates lock, RUN is set to logic 1.

The RUN register bit is cleared only by a system reset or software reset.

LIMIT[1:0]	Rollover Value
“00”	20
“01”	24
“10”	28
“11”	30

Register 0382H 0782H 0B82H 0F82H: DCRU155_622 Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	1
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	—	Unused	X
Bit 3	R/W	Reserved	0
Bit 2	—	Unused	X
Bit 1	R	Reserved	X
Bit 0	R	ERRORI	X

Reserved

The Reserved bits must be set to their default value for proper operation.

ERRORI

The delay line error interrupt status register bit (ERRORI) indicates the ERROR register bit has gone high. When the ERROR register bit changes from a logic zero to logic one, the ERRORI register bit is set to logic one. If the ERRORE interrupt enable is high, the INT output is also asserted when ERRORI asserts. When WCIMODE is low, the ERRORI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded. When WCIMODE is high, the ERRORI register bit is cleared immediately after a logic one is written to the ERRORI register, thus acknowledging the event has been recorded.

Register 0383H 0783H 0B83H 0F83H: DCRU155_622 Powerdown

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	PWRDN	1
Bit 6	R	Reserved	X
Bit 5	—	Unused	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

Writing to this register performs a software reset of the DCRU DLL. A software reset requires a maximum of 2*12*32 SYSCLK cycles for the DLL to regain lock. During this time the DLLCLK phase is adjusting from its current position to delay tap 0, back to a whip position and then will attempt to lock to the incoming serial data stream phase.

PWRDN

The DCRU power down (PWRDN) controls the generation of the recovered clock. When PWRDN is set high, the DCRU reduces power consumption by killing clocks internally as well as the recovered clock. When PWRDN is set low, the DCRU operates normally.

Register 1020H: Tx2488 Analog Control/Status

Bit	Type	Function	Default
Bit 15	R	ROOL_I	X
Bit 14	R	REFCLK_MON	X
Bit 13	—	Unused	X
Bit 12	R	Reserved	X
Bit 11	R/W	Reserved	1
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	R/W	TX2488_MODE[2]	0
Bit 7	R/W	TX2488_MODE[1]	0
Bit 6	R/W	TX2488_MODE[0]	0
Bit 5	R/W	PRBS_FPATT	0
Bit 4	R/W	PRBS_ENABLE	0
Bit 3	R/W	SLLE2488	0
Bit 2	R/W	INV_DATA	0
Bit 1	R	ROOL_V	X
Bit 0	R/W	ROOL_EN	0

ROOL_EN

The Reference Out Of Lock Enable bit enables the ROOL_I interrupt to assert the INTB pin. When ROOL_EN is set to logic one, an interrupt on the INTB is generated upon assertion of the ROOL_I register bit. When ROOL_EN is set low, a change in the ROOL_I status does not generate an interrupt.

ROOL_V

The Reference Out Of Lock status bit indicates the current status of the ROOL detector. The ROOL_V is only latched during a read operation and therefore will change to reflect the current status the ROOL compare logic. The reference out of lock status bit indicates whether the clock synthesis unit (CSU) phase locked loop is able to lock to the reference clock or the recovered clock depending on the state of the LOOPTIMEB bit in register 1021H. ROOL_V is a logic zero if the divided down synthesized clock frequency is within +/-1000 ppm of the reference frequency.

INV_DATA

The Serial Data Inversion INV_DATA controls the polarity of the transmitter data. When INV_DATA is set to ‘1’, the polarity of the TXD_P/TXD_N input pins are inverted. When INV_DATA is set to ‘0’, the TXD_P/TXD_N inputs operate normally.

SLLE2488

The serial line loop-back enable (SLLE2488) bit loops the recovered data and clock to the transmit output. When this bit is set to logic 1, data from the 2488 receiver is input into the PISO and data from the SONET transmit processor is ignored.

For chip-level line loopback, the LINE_LOOP_BACK bit in the Rx2488 Analog CRU Clock Training Configuration and Status register (register 0023H) and the SLLE2488 register bit in the Tx2488 Analog Control/Status register (register 1020H) must be set to logic 1. As well, the LOOPTIMEB and CSU_MODE[3] register bits in the Tx2488 ABC Control register (register 1021H) must be set to logic 0.

PRBS_ENABLE

This bit enables the generation of a PRBS sequence or a fixed pattern in place of the normal transmit data. When low, the data into the PISO-2488 contains data from the SONET transmit processor. When PRBS_ENABLE is set to logic 1, the data into the PISO-2488 contains PRBS words or a fixed pattern, depending on the value of the PRBS_FPATT bit. The generated PRBS is based on the $X^{23}+X^{18}+1$ polynomial (PRBS^23) implemented by a Linear Feedback Shift Register (LFSR).

PRBS_FPATT

This bit enables the generation of a PRBS or a fixed pattern in place of the normal transmit data. When low, the PISO input data contains PRBS words and when high, the fixed pattern written into the FPATT[15:0] in TX2488 Fixed Pattern Register (Reg. 0022H) is used.

TX2488_MODE[2:0]

The TX2488 Mode control bits are used to place the TX2488-CML in one of the following operating modes:

Table 19 TX2488 Mode Control

TX2488_MODE [2:0] Value	Description
111	Reserved
1XX	When the MODE[2] is set high, the data from Channel 1 of the quad mode analog blocks is used as the input to the transmitter.
0XX	When MODE[2] is set low, the data from PISO-2488 is used as the input to the Transmitter. The default is to use the PISO-2488 as the input.
X11	Reserved
X10	Reserved
X01	When the configuration bits MODE0 and MODE1 are set respectively high and low, limited-swing AC coupling suitable for CML compatible Optical data link devices are used. In this mode a 16mA bias current is generated in the differential CML transmitter that is based on an internal reference resistor matched with the output stage load. The generated current produces a reduced-swing differential CML output amplitude. This configuration sets the output amplitude to 533mVppd nominal.
X00	When the configuration bits MODE1 and MODE0 are set low, AC coupling suitable for CML or most PECL compliant ODL transmitters is used. In this mode a 30.5mA bias current is generated in the differential CML transmitter that is based on an internal reference resistor matched with the output stage load. The generated current produces the standard differential amplitude on 50-Ohm single-ended, or 100 Ohm differential, output terminations. This configuration sets the output amplitude to 1Vppd nominal.

Note: TX2488_MODE[1:0] also controls the Tx swing for Channel 1 in quad 622/155 mode.

REFCLK_MON

The reference clock monitor indicates the status of the REFCLK155_P/N pin. A logic high on REFCLK_MONI indicates that at least one low to high transition has occurred on the REFCLK155_P/N pin since the last read of this register. Reading the REFCLK_MON bit clears the setting. REFCLK_MON will be set to logic high after the first transition on REFCLK155_P/N. Software must read this register twice to determine if the REFCLK155_P/N is toggling. If on the second read REFCLK_MON is set to logic low it indicates that REFCLK155_P/N is not toggling.

Note that rising edges can often be detected even when no clock is provided on REFCLK155 if REFCLK155_P/N pins are left floating or if their voltage levels are close to each other (differential PECL inputs). This bit is only valid when RX_REF_ENABLE (register 1021H) is set to logic 1.

ROOL_I

The reference out of lock interrupt status bit is asserted when the clock synthesis unit (CSU) phase locked loop is unable to lock to the reference clock or the recovered clock depending on the state of the LOOPTIMEB bit in register 1021H. The ROOL_I signal is a latched value of the frequency compare logic and only indicates that the synthesized clock has failed to lock at some point and does not reflect the current state. The ROOL_V bit indicates the current ROOL value. At startup, ROOL_I may be latched to logic 1 for several hundred milliseconds while the PLL obtains lock. To insure that the synthesized clock has locked this bit should be read twice separated by at least 500 uSec. If WCIMODE is logic 1, only over-writing with a '1' clears this bit. If WCIMODE is a logic 0, then a read of this register automatically clears the bit.

Note: When ROOL_I is set and indicates that the CSU has lost lock to the reference clock, then once the reference is restored, the CSU must be reset (using CSU_RESET in register 1021H) before normal operation can begin.

Register 1021H: TX2488 ABC Control

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	PISO_RESET	0
Bit 13	R/W	CSU_RESET	0
Bit 12	R/W	RX_REF_ENABLE	1
Bit 11	R/W	TX2488_ENABLE	1
Bit 10	R/W	C2C_ENABLE	1
Bit 9	R/W	CSU_ENABLE	1
Bit 8	R/W	Reserved	0
Bit 7	R/W	LOOPTIMEB	1
Bit 6	R/W	CSU_MODE[6]	1
Bit 5	R/W	CSU_MODE[5]	1
Bit 4	R/W	CSU_MODE[4]	0
Bit 3	R/W	CSU_MODE[3]	1
Bit 2	R/W	CSU_MODE[2]	0
Bit 1	R/W	CSU_MODE[1]	0
Bit 0	R/W	CSU_MODE[0]	0

CSU_MODE[6:0]

The CSU Mode control bits are used to place the CSU in one of the following operating modes:

CSU Mode Control

Mode Bits	Description
6:5	Loop filter resistor select. They allow selection of various loop filter parameters that affect bandwidth. Selection modes are: Bits 6:5 Resistor Value 11 2 x 10KΩ (Default) 10 2 x 9KΩ 01 Invalid Mode 00 2 x 2.5KΩ (for loop-time mode) Note: The optimum setting for Hogge-II and PFD mode is 10K ohms. The optimum setting for loop-timed operation is 2.5K ohms. See CSU_MODE[2] register bit description also.
4	This bit should be set to '0'. Reset levels are (AVDH / 2) ± 100mV. (DEFAULT).
3	Sets the divide ratio for the feedback signal to be used in Hogge-II Phase detector. 0 – divide by 8 1 - divide by 1 (DEFAULT) Note: In non-loop time operation (LOOPTIMEB set to logic one) this

Mode Bits	Description
	bit must be set to logic one (divide by 1) to insure proper operation. In loop-time mode (LOOPTIMEB set to logic zero) this bit must be set to logic 0 (divide by 8).
2	Selects the type of phase detector used in the PLL after the frequency lock is achieved. Note that AUTO_PD Register bit has to be set to '0', so that the phase detector can be set manually. 0 - Phase & Frequency Detector (a.k.a. PFD) (Default) 1 - Hogge-II Phase Detector. NOTE: PFD is the default mode for start-up. Once the frequency lock is achieved, switching to Hogge mode will reduce the intrinsic jitter by about 10%. In Hogge mode the resistor value must be 10KΩ. If after frequency lock, the PFD mode is continued to be used for normal operation (10% more jitter). For resistor value selections, see Bits 6:5.
1:0	This field should be set to '00' for normal operation and '01' for loop-timed operation.

LOOPTIMEB

Used to select the input reference clock for the CSU2488. When set to logic zero the transmitter timing is derived from the recovered clock (loop-time mode). When this bit is set to logic one the transmitter timing is derived from the external refrence clock (lock-to-reference). Note: In loop-time mode (LOOPTIMEB set to logic zero) the CSU_MODE[6:3] and CSU_MODE[1] bits must be set to logic 0, while CSU_MODE[0] must be set to logic 1. The S/UNI MULTI-48 cannot be configured for loop time operation if operating with a mate device unless both received clocks are frequency locked.

CSU_ENABLE

The Clock Source Unit Enable provides a global power down of the CSU Analog Block Circuit. When set to '0', this bit forces the CSU to a low power state and functionality is disabled. When set to '1', the CSU operates in the normal mode of operation.

C2C_ENABLE

The CML to CMOS Interface Module Enable provides a global power down of the CML2CMOS-RX2488 Analog Block Circuit. When set to '0', this bit forces the CML to CMOS Interface Module to a low power state and functionality is disabled. When set to '1', the CML to CMOS Interface Module operates in the normal mode of operation.

TX2488_ENABLE

The 2.488GHz Transmitter Enable provides a global power down of the TX2488 Analog Block Circuit. When set to '0', this bit forces the TX2488 to a low power state and functionality is disabled. When set to '1', the TX2488 operates in the normal mode of operation.

RX_REF_ENABLE

The PECL Reference Clock Receiver Enable provides a global power down of the RX2488-PECL Analog Block Circuitry used for reference clock input. When set to '0', this bit forces the block to a low power state and functionality is disabled. When set to '1', the block operates in the normal mode of operation.

CSU_RESET

The Clock Source Unit Reset provides a complete reset of the CSU2488 Analog Block Circuit. When set to '1', this bit forces the CSU to a known initial state. While the bit is set to '1', the functionality of the block is disabled. When set to '0', the CSU operates in the normal mode of operation. This bit is not self-clearing. Therefore a '0' must be written to the bit to remove the reset condition. When used, CSU_RESET should be asserted for at least 2 ms to reset circuitry properly.

PISO_RESET

The PISO Reset provides a complete reset of the PISO-2488 Analog Block Circuit. When set to '1', this bit forces the PISO to a known initial state. While the bit is set to '1', the functionality of the block is disabled. When set to '0', the PISO operates in the normal mode of operation. This bit is not self-clearing. Therefore a '0' must written to the bit to remove the reset condition. When used, PISO_RESET should be asserted for at least 100 ns to reset circuitry properly.

Register 1022H: TX2488 Fixed Pattern Register

Bit	Type	Function	Default
Bit 15	R/W	FPATT[15]	0
Bit 14	R/W	FPATT[14]	0
Bit 13	R/W	FPATT[13]	0
Bit 12	R/W	FPATT[12]	0
Bit 11	R/W	FPATT[11]	0
Bit 10	R/W	FPATT[10]	0
Bit 9	R/W	FPATT[9]	0
Bit 8	R/W	FPATT[8]	0
Bit 7	R/W	FPATT[7]	0
Bit 6	R/W	FPATT[6]	0
Bit 5	R/W	FPATT[5]	0
Bit 4	R/W	FPATT[4]	0
Bit 3	R/W	FPATT[3]	0
Bit 2	R/W	FPATT[2]	0
Bit 1	R/W	FPATT[1]	0
Bit 0	R/W	FPATT[0]	0

FPATT[15:0]

The FPATT[15:0] provides the fixed pattern that will be generated when the PRBS_FPATT bit is set to logic 1. If PRBS_FPATT is set to logic 0, this register is not used. When fixed-pattern is used, the word's most significant bit (MSB), namely FPATT[15], is transmitted first over the serial output link.

Note that the transition density of the transmit data stream must be considered when sending fixed patterns.

Register 1030H: Quad 622 Tx MABC CSUT Control Register

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	1
Bit 9	R/W	Reserved	1
Bit 8	R/W	Reserved	1
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	CSUT_ARSTB	1

CSUT_ARSTB

The CSUT analog reset bit CSUT_ARSTB provides a reset to the CSUT. To reset the CSUT properly, CSUT_ARSTB should be held low for at least 100 ns. The CSUT requires 5 ms to regain lock when CSUT_ARSTB is brought back to high.

'0' = Reset applied to entire CSUT , asserted for at least 100 ns
'1' = Normal operation (default)

Register 1031H: Quad 622 Tx CSUT Clock Detector Control Register

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	1
Bit 13	R/W	Reserved	1
Bit 12	R/W	Reserved	1
Bit 11	R/W	Reserved	1
Bit 10	R/W	Reserved	1
Bit 9	R/W	Reserved	1
Bit 8	R/W	Reserved	1
Bit 7	R/W	Reserved	1
Bit 6	R/W	Reserved	1
Bit 5	R/W	Reserved	1
Bit 4	R/W	Reserved	1
Bit 3	R	ROOLV	X
Bit 2	R	Reserved	X
Bit 1	R/W	Reserved	0
Bit 0	R/W	ROOLI_EN	0

ROOLI_EN

Register bit ROOLI_EN is used as interrupt enable for ROOLI register bit. It connects the ROOLI status bit to the INT pin of the LAS4x622 block. When ROOLI_EN is set to logic one, an interrupt on the INT is generated upon assertion of the ROOLI register bit. When ROOLI_EN is set low, a change in the ROOLI status does not generate an interrupt.

ROOLV

The Transmit reference out of lock status bit indicates the clock synthesis phase locked loop is unable to lock to the reference clock on REFCLK77. ROOLV is a logic one if difference between the divided down synthesized clock CSUT_DIVCLK frequency and the reference clock RECLK frequency is not within certain ppm. At startup, ROOLV may remain at logic 1 for several hundred mil-seconds while the PLL obtains lock.

Register 1032H: Quad 622 Tx CSUT Interrupt Status Register

Bit	Type	Function	Default
Bit 15	R	Reserved	X
Bit 14	R	Reserved	X
Bit 13	R	Reserved	X
Bit 12	R	Reserved	X
Bit 11	R	Reserved	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R	ROOLI	X

ROOLI

The Transmit reference out of lock status indicates the clock synthesis phase locked loop is unable to lock to the reference clock on REFCLK77. ROOLI is a logic one if the divided down synthesized clock frequency is not within 488 ppm of the REFCLK77 frequency. At startup, ROOLI may remain at logic 1 for several hundred mil-seconds while the PLL obtains lock. If WCIMODE is set to logic 1 only over-writing with a '1' clears this bit. If WCIMODE is set to a logic 0 then a read of this register automatically clears the bit.

Register 1033H 1433H 1833H 1C33H: Quad 622 Tx MABC and JAT622 Channel Control and Status Register

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	JAT_ERR	X
Bit 6	R	JAT_RUN	X
Bit 5	R/W	JAT_RATE[1]	0
Bit 4	R/W	JAT_RATE[0]	0
Bit 3	R/W	LOOPT	0
Bit 2	R/W	SLLE622	0
Bit 1	R/W	TX_MODE[1]	1
Bit 0	R/W	TX_MODE[0]	0

TX_MODE[1:0]

The Tx mode selection register field TX_MODE[1:0] selects the output swing levels for the TX.

'00' = Low swing levels
'01' = Large swing levels
'1X' = XAUI levels (default)

Note: TX_MODE[1:0] only applies to Channel 2-4, Channel 1 is controlled by TX2488_MODE[1:0] in register 0x1020H.

SLLE622

The serial line loopback enable register bit SLLE622 controls the source data used to generate the outgoing transmit line serial data stream in the JAT622. When SLLE622 is low, the transmit data is transmitted by the JAT622. When SLLE622 is high, the receive data is transmitted by the JAT622. When SLLE622 is high, LOOPT must also be set high for proper operation.

LOOPT

The JAT622 looptime enable bit LOOPT controls the source clock used to generate the outgoing serial data stream for the JAT622. When LOOPT is low, the JAT622 uses the clock from CSUT which is synced to REFCLK77 to control the phase of the outgoing serial stream output. When LOOPT is high, the JAT622 uses the receive clock to control the phase of the outgoing serial stream outputs (jitter attenuation mode). When SLLE622 is high, LOOPT must also be set high for proper operation.

JAT_RATE[1:0]

The JAT622 data rate control register field JAT_RATE[1:0] configures the JAT622 to perform serialization and jitter attenuation for different line rates. The resulting configuration value determines the JAT_RATE line rate.

"00"	622Mbit/s NRZ line rate
"01"	155Mbit/s NRZ line rate
"10"	Reserved
"11"	Reserved

JAT_RUN

The JAT622 DLL run status register bit JAT_RUN indicates the DLL of the JAT622 has locked to the incoming reference clock. When RUN is low, the DLL is searching for the proper delay tap (initialization). When RUN is high, the DLL has initialized and is attempting to track the incoming serial stream. This register bit is a read-only register bit.

JAT_ERR

The JAT622 DLL error status register bit JAT_ERR indicates the DLL of JAT622 has run out of delay line. When JAT_ERR is high, the DLL is trying to move beyond the end of the delay line losing the phase lock. When JAT_ERR is low, the DLL is operating normally. This register bit is a read-only register bit.

Register 1034H 1434H 1834H 1C34H: Quad 622 Tx Channel Data Path and PRBS Control Register

Bit	Type	Function	Default
Bit 15	R/W	TX_PRBS_FPATT[7]	0
Bit 14	R/W	TX_PRBS_FPATT[6]	0
Bit 13	R/W	TX_PRBS_FPATT[5]	0
Bit 12	R/W	TX_PRBS_FPATT[4]	0
Bit 11	R/W	TX_PRBS_FPATT[3]	0
Bit 10	R/W	TX_PRBS_FPATT[2]	0
Bit 9	R/W	TX_PRBS_FPATT[1]	0
Bit 8	R/W	TX_PRBS_FPATT[0]	0
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R/W	TX_PRBS_FPATT_EN	0
Bit 1	R/W	TX_PRBS_EN	0
Bit 0	R/W	TX_INV_DATA_EN	0

TX_INV_DATA_EN

The Tx Serial Data Inversion TX_INV_DATA_EN controls the polarity of the transmitter data. When TX_INV_DATA_EN is set to '1' the polarity of the transmit stream is inverted. When TX_INV_DATA_EN is set to '0' the transmit stream operates normally.

TX_PRBS_EN

This bit enables the generation of a PRBS or a fixed pattern in place of the normal transmit data. When low, the data into the JAT622 contains data from the SONET transmit processor. When TX_PRBS_EN is set to a logic '1', the data into the JAT622 contains PRBS words or a fixed pattern depending on the value of the TX_PRBS_FPATT_EN bit.

TX_PRBS_FPATT_EN

This bit enables the generation of a PRBS or a fixed pattern in place of the normal transmit data. When low, the PISO input data contains PRBS words, and when high the fixed pattern written into the FPATT[7:0] Register is input.

TX_PRBS_FPATT[7:0]

The FPATT[7:0] provides the fixed pattern that will be monitored for when the TX_PRBS_FPATT_EN bit is set to a logic 1. If PRBS_FPATT is set to logic 0 this register is not used.

Register 1040H: STLI Clock Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	1
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	TDCLK48EN	0

TDCLK48EN

The transmit STS-48/STM-16 mode clock enable (TDCLK48EN) bit controls the gating of the internal parallel transmit clock. When TDCLK48EN is set to logic 1, the transmit clock for STS-48/STM-16 mode operates normally. When TDCLK48EN is set to logic 0, the transmit clock needed for STS-48/STM-16 mode is held low. This register bit must be set to logic 1 for normal operation in STS-48/STM-16 mode. This register bit must be set to logic 0 for normal operation in STS-12/STM-4 or STS-3/STM-1 modes.

Reserved

The Reserved bits must be left in their default values for proper operation.

Register 1060H 1460H 1860H 1C60H: JAT622 Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	—	Unused	X
Bit 4	R/W	TX55	0
Bit 3	R/W	TXDINV	0
Bit 2	—	Unused	X
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

The Configuration Register controls the basic operation of the JAT.

Reserved

These bits are reserved and should be written with their default value.

TXDINV

The transmit data invert (TXDINV) controls the polarity of the serial transmit outputs. When TXDINV is high, the polarity of the transmit data outputs is inverted. When TXDINV is low, the polarity of the transmit data outputs is normal.

TX55

The transmit 55h bit (TX55) forces the serial transmit outputs to send a repeated 1010 pattern at the line rate. When TX55 is high, a 1010 pattern is transmitted on line transmit output ports. When TX55 is low, data is sent normally on line transmit output ports.

Register 1061H 1461H 1861H 1C61H: JAT622 Configuration and Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	FRST	0
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R	RUN	X
Bit 3	R	FERR	X
Bit 2	R	ERROR	X
Bit 1	R/W	FERRE	0
Bit 0	R/W	ERRORE	0

The Configuration and Interrupt Enable Register controls the basic operation of the JAT.

ERRORE

The ERROR interrupt enable (ERRORE) bit enables the error indication interrupt. When ERRORE is set high, an interrupt is generated upon assertion event of the ERR output and ERROR register. When ERRORE is set low, changes in the ERROR and ERR status do not generate an interrupt.

FERRE

The FIFO error interrupt enable (FERRE) bit enables the FIFO error indication interrupt. When FERRE is set high, an interrupt is generated upon assertion event of the FERR register. When FERRE is set low, changes in the FERR status does not generate an interrupt. This interrupt should only be enabled in line loopback mode.

ERROR

The delay line error register bit (ERROR) indicates the DLL has run out of dynamic range. When the DLL attempts to move beyond the end of the delay line, ERROR is set high. When ERROR is high, the DLL cannot generate a recovered clock locked to the serial data stream. ERROR is set low, when the JAT may again try to recover the data stream.

FERR

The loopback FIFO error register bit (FERR) indicates the line loopback FIFO has underrun or overrun. The loopback FIFO handles the phase difference between the incoming byte serial data stream on RDATA[7:0] and the outgoing serial stream. When the FIFO error occurs, the FERR is set high. When the FIFO is operating normally, FERR is low. This status bit should not be considered unless in line loopback mode (STS-12/STM-4 or STS-3/STM-1 mode).

RUN

The DLL lock status register bit (RUN) indicates the DLL found a delay line tap to lock to the incoming reference clock. After system reset, RUN is logic zero until the phase detector indicates an initial lock condition. When the phase detector indicates lock, the DLL has initialized and is attempting to tracking the incoming serial stream.

The RUN register bit is cleared only by a system reset or a software reset.

FRST

The FIFO reset control (FRST) bit allows the loopback FIFO to be set to a known state. When FRST is set high, the loopback FIFO fill level is set to 4 bytes (half full) and the outgoing stream line interface is held constant. When FRST is set low, the loopback FIFO operates normally.

The FRST does not affect the serial line interface when SLLE622 is not enabled.

Register 1062H 1462H 1862H 1C62H: JAT622 Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	1
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R	FERRI	X
Bit 0	R	ERRORI	X

The Status Register reports the basic operation of the JAT.

ERRORI

The delay line error event register bit (ERRORI) indicates the ERROR register bit has gone high. When the ERROR register changes from a logic zero to a logic one, the ERRORI register bit is set to logic one. If the ERRORE interrupt enable is high, the INT output is also asserted when ERRORI asserts.

When WCIMODE is low, the ERRORI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded. When WCIMODE is high, the ERRORI register bit is cleared immediately after a logic one is written to the ERRORI register, thus acknowledging the event has been recorded.

FERRI

The FIFO error event register bit (FERRI) indicates the FERR register bit has gone high. When the FERR register changes from a logic zero to a logic one, the FERRI register bit is set to logic one. If the FERRE interrupt enable is high, the INT output is also asserted when FERRI asserts. This interrupt should not be considered unless in line loopback mode (STS-12/STM-4 or STS-3/STM-1 mode).

When WCIMODE is low, the FERRI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded. When WCIMODE is high, the FERRI register bit is cleared immediately after a logic one is written to the FERRI register, thus acknowledging the event has been recorded.

Register 1063H 1463H 1863H 1C63H: JAT622 Powerdown

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	PWRDN	1
Bit 6	R	Reserved	X
Bit 5	—	Unused	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

The Powerdown Register enables the power down of the JAT.

Writing to this register performs a software reset of the DLL. A software reset requires a maximum of 2*12*32 SYSCLK cycles for the DLL to regain lock. PWRDN

The JAT power down bit (PWRDN) controls the generation of the line rate clock . When PWRDN is set high, the JAT reduces power consumption by killing clocks internally as well as the line transmit clock. When PWRDN is set low, the JAT operates normally.

Register 1080H 1480H 1880H 1C80H: TRMP Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	LREIBLK	0
Bit 10	R/W	LREIEN	1
Bit 9	R/W	APSEN	1
Bit 8	R/W	Reserved	1
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	1
Bit 4	R/W	Reserved	0
Bit 3	R/W	TRACEEN	0
Bit 2	R/W	J0Z0INCEN	0
Bit 1	R/W	Z0DEF	0
Bit 0	R/W	A1A2EN	1

All Reserved bits must be set to their default values for proper operation.

A1A2EN

The A1A2 framing enable (A1A2EN) bit controls the insertion of the framing bytes in the data stream. When A1A2EN is set to logic 1, F6h and 28h are inserted in the A1 and A2 bytes according to the priority of Table 7. When A1A2EN is set to logic 0, the framing bytes are not inserted.

For STS-48/STM-16 operation, the A1A2EN bit in the TRMP Configuration register from all 4 slices must be set to the same value.

Z0DEF

The Z0 definition (Z0DEF) bit defines the Z0 growth bytes. When Z0DEF is set to logic 1, the Z0 bytes are defined according to ITU. There is no Z0 byte in STS-3/STM-1 mode. The Z0 bytes are located in STS-1/STM-0 #2 to #4 in STS-12/STM-4 master mode and are located in STS-1/STM-0 #1 to #4 in STS-12/STM-4 slave mode. When Z0DEF is set to logic 0, The Z0 bytes are defined according to TELCORDIA. The Z0 bytes are located in STS-1/STM-0 #2 to #3 in STS-3/STM-1 mode, are located in STS-1/STM-0 #2 to #12 in STS-12/STM-4 master mode and are located in STS-1/STM-0 #1 to #12 in STS-12/STM-4 slave mode.

When Z0DEF = 1, the user must ensure that remaining unused bytes (non-Z0 bytes) are inserted via TTOH ports to ensure proper transition density in these non-scrambled byte locations.

For STS-48/STM-16 operation, the Z0DEF bit in the TRMP Configuration register from all 4 slices must be set to the same value.

J0Z0INCEN

The J0 and Z0 increment enable (J0Z0INCEN) bit controls the insertion of an incremental pattern in the section trace and Z0 growth bytes. When J0ZOINCEN is set to logic 1, the corresponding STS-1/STM-0 path # is inserted in the J0 and Z0 bytes according to the priority of Table 7. When J0Z0INCEN is set to logic 0, no incremental pattern is inserted.

For STS-48/STM-16 operation, the J0Z0INCEN bit in the TRMP Configuration register from all 4 slices must be set to the same value.

TRACEEN

The section trace enable (TRACEEN) bit controls the insertion of section trace in the data stream. When TRACEEN is set to logic 1, the section trace from the Section TTTP block is inserted in the J0 byte of STS-1/STM-0 #1 according to the priority of Table 7. When TRACEEN is set to logic 0, the section trace from the J0[7:0] input port is not inserted.

APSEN

The APS enable (APSEN) bit controls the insertion of automatic protection switching in the data stream. When APSEN is set to logic 1, the APS bytes from the RRMP are inserted in the K1/K2 bytes of STS-1/STM-0 #1 according to the priority of Table 7. When APSEN is set to logic 0, the APS bytes from the RRMP are not inserted.

LREIEN

The line REI enable (LREIEN) bit controls the insertion of line remote error indication in the data stream. When LREIEN is set to logic 1, the line REI from the RRMP is inserted in the M1 byte of STS-1/STM-0 #3 according to the priority of Table 7. When LREIEN is set to logic 0, the line REI from the RRMP is not inserted.

LREIBLK

The line REI block error (LREIBLK) bit controls the generation of line remote error indication. When LREIBLK is set to logic 1, the line REI inserted in the M1 byte represents BIP-24 block errors (a maximum of 1 error per STS-3/STM-1 per frame). When LREIBLK is set to logic 0, the line REI inserted in the M1 byte represents BIP-8 errors (a maximum of 8 error per STS-1/STM-0 per frame).

Register 1081H 1481H 1881H 1C81H: TRMP Register Insertion

Bit	Type	Function	Default
Bit 15	R/W	UNUSEDV	0
Bit 14	R/W	UNUSEDEN	0
Bit 13	R/W	NATIONALV	0
Bit 12	R/W	NATIONALEN	0
Bit 11	—	Unused	X
Bit 10	R/W	E2REGEN	0
Bit 9	R/W	Z2REGEN	0
Bit 8	R/W	Z1REGEN	0
Bit 7	R/W	S1REGEN	0
Bit 6	R/W	D4D12REGEN	0
Bit 5	R/W	K1K2REGEN	0
Bit 4	R/W	D1D3REGEN	0
Bit 3	R/W	F1REGEN	0
Bit 2	R/W	E1REGEN	0
Bit 1	R/W	Z0REGEN	1
Bit 0	R/W	J0REGEN	1

J0REGEN

The J0 register enable (J0REGEN) bit controls the insertion of section trace in the data stream. When J0REGEN is set to logic 1, the section trace from the TRMP Transmit J0 and Z0 register is inserted in the J0 byte of STS-1/STM-0 #1 according to the priority of Table 7. When J0REGEN is set to logic 0, the section trace from the TRMP Transmit J0 and Z0 register is not inserted.

Z0REGEN

The Z0 register enable (Z0REGEN) bit controls the insertion of Z0 growth bytes in the data stream. When Z0REGEN is set to logic 1, the Z0 growth byte from the TRMP Transmit J0 and Z0 register is inserted in the Z0 bytes according to the priority of Table 7. When Z0REGEN is set to logic 0, the Z0 growth byte from the TRMP Transmit J0 and Z0 register is not inserted. The Z0DEF bit in the TRMP Configuration register defines the Z0 bytes.

E1REGEN

The E1 register enable (E1REGEN) bit controls the insertion of section order wire in the data stream. When E1REGEN is set to logic 1, the section order wire from the TRMP Transmit E1 and F1 register is inserted in the E1 byte of STS-1/STM-0 #1 according to the priority of Table 7. When E1REGEN is set to logic 0, the section order wire from the TRMP Transmit E1 and F1 register is not inserted.

F1REGEN

The F1 register enable (F1REGEN) bit controls the insertion of section user channel in the data stream. When F1REGEN is set to logic 1, the section user channel from the TRMP Transmit E1 and F1 register is inserted in the F1 byte of STS-1/STM-0 #1 according to the priority of Table 7. When F1REGEN is set to logic 0, the section user channel from the TRMP Transmit E1 and F1 register is not inserted.

D1D3REGEN

The D1 to D3 register enable (D1D3REGEN) bit controls the insertion of section data communication channel in the data stream. When D1D3REGEN is set to logic 1, the section DCC from the TRMP Transmit D1D3 and D4D12 register is inserted in the D1 to D3 bytes of STS-1/STM-0 #1 according to the priority of Table 7. When D1D3REGEN is set to logic 0, the section DCC from the TRMP Transmit D1D3 and D4D12 register is not inserted.

K1K2REGEN

The K1K2 register enable (K1K2REGEN) bit controls the insertion of automatic protection switching in the data stream. When K1K2REGEN is set to logic 1, the APS bytes from the TRMP Transmit K1 and K2 register are inserted in the K1, K2 bytes of STS-1/STM-0 #1 according to the priority of Table 7. When K1K2REGEN is set to logic 0, the APS bytes from the TRMP Transmit K1 and K2 register are not inserted.

D4D12REGEN

The D4 to D12 register enable (D4D12REGEN) bit controls the insertion of line data communication channel in the data stream. When D4D12REGEN is set to logic 1, the line DCC from the TRMP Transmit D1D3 and D4D12 register is inserted in the D4 to D12 bytes of STS-1/STM-0 #1 according to the priority of Table 7. When D4D12REGEN is set to logic 0, the line DCC from the TRMP Transmit D1D3 and D4D12 register is not inserted.

S1REGEN

The S1 register enable (S1REGEN) bit controls the insertion of the synchronization status message in the data stream. When S1REGEN is set to logic 1, the SSM from the TRMP Transmit S1 and Z1 register is inserted in the S1 byte of STS-1/STM-0 #1 according to the priority of Table 7. When S1REGEN is set to logic 0, the SSM from the TRMP Transmit S1 and Z1 register is not inserted.

Z1REGEN

The Z1 register enable (Z1REGEN) bit controls the insertion of Z1 growth bytes in the data stream. When Z1REGEN is set to logic 1, the Z1 byte from the TRMP Transmit S1 and Z1 register is inserted in the Z1 bytes according to the priority of Table 7. When Z1REGEN is set to logic 0, the Z1 byte from the TRMP Transmit S1 and Z1 register is not inserted.

Z2REGEN

The Z2 register enable (Z2REGEN) bit controls the insertion of Z2 growth bytes in the data stream. When Z2REGEN is set to logic 1, the Z2 byte from the TRMP Transmit Z2 and E2 register is inserted in the Z2 bytes according to the priority of Table 7. When Z2REGEN is set to logic 0, the Z2 byte from the TRMP Transmit Z2 and E2 register is not inserted.

E2REGEN

The E2 register enable (E2REGEN) bit controls the insertion of line order wire in the data stream. When E2REGEN is set to logic 1, the line order wire from the TRMP Transmit Z2 and E2 register is inserted in the E2 byte of STS-1/STM-0 #1 according to the priority of Table 7. When E2REGEN is set to logic 0, the line order wire from the TRMP Transmit Z2 and E2 register is not inserted.

NATIONALEN

The national enable (NATIONALEN) bit controls the insertion of national bytes in the data stream. When NATIONALEN is set to logic 1, an all one or an all zero pattern is inserted in the national bytes according to the priority of Table 7. When NATIONALEN is set to logic 0, no pattern is inserted. The Z0DEF bit in the TRMP Configuration register defines the national bytes of ROW #1.

NATIONALV

The national value (NATIONALV) bit controls the value inserted in the national bytes. When NATIONALV is set to logic 1, an all one pattern is inserted in the national bytes if enabled via the NATIONALEN register bit. When NATIONALV is set to logic 0, an all zero pattern is inserted in the national bytes if enabled via the NATIONALEN register bit.

UNUSEDEN

The unused enable (UNUSEDEN) bit controls the insertion of unused bytes in the data stream. When UNUSEDEN is set to logic 1, an all one or an all zero pattern is inserted in the unused bytes according to the priority of Table 7. When UNUSEDEN is set to logic 0, no pattern is inserted.

UNUSEDV

The unused value (UNUSEDV) bit controls the value inserted in the unused bytes. When UNUSEDV is set to logic 1, an all one pattern is inserted in the unused bytes if enabled via the UNUSEDEN register bit. When UNUSEDV is set to logic 0, an all zero pattern is inserted in the unused bytes if enabled via the UNUSEDEN register bit.

Register 1082H 1482H 1882H 1C82H: TRMP Error Insertion

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	R/W	B2DISABLE	0
Bit 7	R/W	B1DISABLE	0
Bit 6	R/W	LOSINS	0
Bit 5	R/W	LAISINS	0
Bit 4	R/W	LRDIINS	0
Bit 3	R/W	A1ERR	0
Bit 2	R/W	HMASKEN	1
Bit 1	R/W	B2MASKEN	1
Bit 0	R/W	B1MASKEN	1

B1MASKEN

The B1 mask enable (B1MASKEN) bit selects the use of the B1 byte extracted from the TTOH port. When B1MASKEN is set to logic 1, the B1 byte extracted from the TTOH port is used as a mask to toggle bits in the calculated B1 byte (the B1 byte extracted from the TTOH port is XOR with the calculated B1 byte). When B1MASKEN is set to logic 0, the B1 byte extracted from the TTOH port is inserted instead of the calculated B1 byte.

B2MASKEN

The B2 mask enable (B2MASKEN) bit selects the use of the B2 bytes extracted from the TTOH port. When B2MASKEN is set to logic 1, the B2 bytes extracted from the TTOH port are used as a mask to toggle bits in the calculated B2 bytes (the B2 bytes extracted from the TTOH port are XOR with the calculated B2 bytes). When B2MASKEN is set to logic 0, the B2 bytes extracted from the TTOH port are inserted instead of the calculated B2 bytes.

HMASKEN

The H1/H2 mask enable (HMASKEN) bit selects the use of the H1/H2 bytes extracted from the TTOH port. When HMASKEN is set to logic 1, the H1/H2 bytes extracted from the TTOH port are used as a mask to toggle bits in the H1/H2 path payload pointer bytes (the H1/H2 bytes extracted from the TTOH port are XOR with the path payload pointer bytes). When HMASKEN is set to logic 0, the H1/H2 bytes extracted from the TTOH port are inserted instead of the path payload pointer bytes.

A1ERR

The A1 error insertion (A1ERR) bit is used to introduce framing errors in the A1 bytes. When A1ERR is set to logic 1, 76h instead of F6h is inserted in all of the A1 bytes according to the priority of Table 7. When A1ERR is set to logic 0, no framing errors are introduced.

LRDIINS

The line RDI insertion (LRDIINS) bit is used to force a line remote defect indication in the data stream. When LRDIINS is set to logic 1, the 110 pattern is inserted in bits 6, 7 and 8 of the K2 byte of STS-1/STM-0 #1 to force a line RDI condition. When LRDIINS is set to logic 0, the line RDI condition is removed.

LAISINS

The line AIS insertion (LAISINS) bit is used to force a line alarm indication signal in the data stream. When LAISINS is set to logic 1, all ones are inserted in the line overhead and in the payload (all the bytes of the frame except the section overhead bytes) to force a line AIS condition. When LAISINS is set to logic 0, the line AIS condition is removed. Line AIS is inserted/removed on frame boundary before scrambling.

Note, for STS-48/STM-16 operation, this bit must be set to the same value as the other LAISINS bits in the TRMP #2 Error Insertion, TRMP #3 Error Insertion and TRMP #4 Error Insertion registers.

LOSINS

The LOS insertion (LOSINS) bit is used to force a loss of signal condition in the data stream. When LOSINS is set to logic 1, the data steam is set to all zeros (after scrambling) to force a loss of signal condition. When LOSINS is set to logic 0, the loss of signal condition is removed.

Note, for STS-48/STM-16 operation, this bit must be set to the same value as the other LOSINS bits in the TRMP #2 Error Insertion, TRMP #3 Error Insertion and TRMP #4 Error Insertion registers.

B1DISABLE

The B1 disable insertion (B1DISABLE) bit is used to set the B1 byte in a pass through mode. When B1DISABLE is set to logic one, the B1 byte value is passed through transparently without being overwritten. When B1DISABLE is set to logic zero, a valid B1 byte is inserted into the SOH.

B2DISABLE

The B2 disable insertion (B2DISABLE) bit is used to set the B2 byte in a pass through mode. When B2DISABLE is set to logic one, the B2 byte value is passed through transparently without being overwritten. When B2DISABLE is set to logic zero, a valid B2 byte is inserted into the TOH.

Register 1083H 1483H 1883H 1C83H: TRMP Transmit J0 and Z0

Bit	Type	Function	Default
Bit 15	R/W	J0V[7]	0
Bit 14	R/W	J0V[6]	0
Bit 13	R/W	J0V[5]	0
Bit 12	R/W	J0V[4]	0
Bit 11	R/W	J0V[3]	0
Bit 10	R/W	J0V[2]	0
Bit 9	R/W	J0V[1]	0
Bit 8	R/W	J0V[0]	1
Bit 7	R/W	Z0V[7]	1
Bit 6	R/W	Z0V[6]	1
Bit 5	R/W	Z0V[5]	0
Bit 4	R/W	Z0V[4]	0
Bit 3	R/W	Z0V[3]	1
Bit 2	R/W	Z0V[2]	1
Bit 1	R/W	Z0V[1]	0
Bit 0	R/W	Z0V[0]	0

This register is only valid once written. The default value is not transferred.

Z0V[7:0]

The Z0 byte value (Z0V[7:0]) bits hold the Z0 growth byte to be inserted in the data stream. The Z0V[7:0] value is inserted in the Z0 bytes if the insertion is enabled via the Z0REGEN bit in the TRMP Register Insertion register. The Z0DEF bit in the TRMP Configuration register defines the Z0 bytes.

J0V[7:0]

The J0 byte value (J0V[7:0]) bits hold the section trace to be inserted in the data stream. The J0V[7:0] value is inserted in the J0 byte of STS-1/STM-0 #1 if the insertion is enabled via the J0REGEN bit in the TRMP Register Insertion register.

Register 1084H 1484H 1884H 1C84H: TRMP Transmit E1 and F1

Bit	Type	Function	Default
Bit 15	R/W	E1V[7]	0
Bit 14	R/W	E1V[6]	0
Bit 13	R/W	E1V[5]	0
Bit 12	R/W	E1V[4]	0
Bit 11	R/W	E1V[3]	0
Bit 10	R/W	E1V[2]	0
Bit 9	R/W	E1V[1]	0
Bit 8	R/W	E1V[0]	0
Bit 7	R/W	F1V[7]	0
Bit 6	R/W	F1V[6]	0
Bit 5	R/W	F1V[5]	0
Bit 4	R/W	F1V[4]	0
Bit 3	R/W	F1V[3]	0
Bit 2	R/W	F1V[2]	0
Bit 1	R/W	F1V[1]	0
Bit 0	R/W	F1V[0]	0

F1V[7:0]

The F1 byte value (F1V[7:0]) bits hold the section user channel to be inserted in the data stream. The F1V[7:0] value is inserted in the F1 byte of STS-1/STM-0 #1 if the insertion is enabled via the F1REGEN bit in the TRMP Register Insertion register.

E1V[7:0]

The E1 byte value (E1V[7:0]) bits hold the section order wire to be inserted in the data stream. The E1V[7:0] value is inserted in the E1 byte of STS-1/STM-0 #1 if the insertion is enabled via the E1REGEN bit in the TRMP Register Insertion register.

Register 1085H 1485H 1885H 1C85H: TRMP Transmit D1D3 and D4D12

Bit	Type	Function	Default
Bit 15	R/W	D1D3V[7]	0
Bit 14	R/W	D1D3V[6]	0
Bit 13	R/W	D1D3V[5]	0
Bit 12	R/W	D1D3V[4]	0
Bit 11	R/W	D1D3V[3]	0
Bit 10	R/W	D1D3V[2]	0
Bit 9	R/W	D1D3V[1]	0
Bit 8	R/W	D1D3V[0]	0
Bit 7	R/W	D4D12V[7]	0
Bit 6	R/W	D4D12V[6]	0
Bit 5	R/W	D4D12V[5]	0
Bit 4	R/W	D4D12V[4]	0
Bit 3	R/W	D4D12V[3]	0
Bit 2	R/W	D4D12V[2]	0
Bit 1	R/W	D4D12V[1]	0
Bit 0	R/W	D4D12V[0]	0

D4D12V[7:0]

The D4D12 byte value (D4D12V[7:0]) bits hold the line data communication channel to be inserted in the data stream. The D4D12V[7:0] value is inserted in the D4 to D12 bytes of STS-1/STM-0 #1 if the insertion is enabled via the D4D12REGEN bit in the TRMP Register Insertion register.

D1D3V[7:0]

The D1D3 byte value (D1D3V[7:0]) bits hold the section data communication channel to be inserted in the data stream. The D1D3V[7:0] value is inserted in the D1 to D3 bytes of STS-1/STM-0 #1 if the insertion is enabled via the D1D3REGEN bit in the TRMP Register Insertion register.

Register 1086H 1486H 1886H 1C86H: TRMP Transmit K1 and K2

Bit	Type	Function	Default
Bit 15	R/W	K1V[7]	0
Bit 14	R/W	K1V[6]	0
Bit 13	R/W	K1V[5]	0
Bit 12	R/W	K1V[4]	0
Bit 11	R/W	K1V[3]	0
Bit 10	R/W	K1V[2]	0
Bit 9	R/W	K1V[1]	0
Bit 8	R/W	K1V[0]	0
Bit 7	R/W	K2V[7]	0
Bit 6	R/W	K2V[6]	0
Bit 5	R/W	K2V[5]	0
Bit 4	R/W	K2V[4]	0
Bit 3	R/W	K2V[3]	0
Bit 2	R/W	K2V[2]	0
Bit 1	R/W	K2V[1]	0
Bit 0	R/W	K2V[0]	0

K1V[7:0], K2V[7:0]

The K1, K2 bytes value (K1V[7:0], K2V[7:0]) bits hold the APS bytes to be inserted in the data stream. The K1V[7:0], K2V[7:0] values are inserted in the K1, K2 bytes of STS-1/STM-0 #1 if the insertion is enabled via the K1K2REGEN bit in the TRMP Register Insertion register.

Register 1087H 1487H 1887H 1C87H: TRMP Transmit S1 and Z1

Bit	Type	Function	Default
Bit 15	R/W	S1V[7]	0
Bit 14	R/W	S1V[6]	0
Bit 13	R/W	S1V[5]	0
Bit 12	R/W	S1V[4]	0
Bit 11	R/W	S1V[3]	0
Bit 10	R/W	S1V[2]	0
Bit 9	R/W	S1V[1]	0
Bit 8	R/W	S1V[0]	0
Bit 7	R/W	Z1V[7]	0
Bit 6	R/W	Z1V[6]	0
Bit 5	R/W	Z1V[5]	0
Bit 4	R/W	Z1V[4]	0
Bit 3	R/W	Z1V[3]	0
Bit 2	R/W	Z1V[2]	0
Bit 1	R/W	Z1V[1]	0
Bit 0	R/W	Z1V[0]	0

Z1V[7:0]

The Z1 byte value (Z1V[7:0]) bits hold the Z1 growth byte to be inserted in the data stream. The Z1V[7:0] value is inserted in the Z1 byte if the insertion is enabled via the Z1REGEN bit in the TRMP Register Insertion register.

S1V[7:0]

The S1 byte value (S1V[7:0]) bits hold the synchronization status message to be inserted in the data stream. The S1V[7:0] value is inserted in the S1 byte of STS-1/STM-0 #1 if the insertion is enabled via the S1REGEN bit in the TRMP Register Insertion register.

Register 1088H 1488H 1888H 1C88H: TRMP Transmit Z2 and E2

Bit	Type	Function	Default
Bit 15	R/W	Z2V[7]	0
Bit 14	R/W	Z2V[6]	0
Bit 13	R/W	Z2V[5]	0
Bit 12	R/W	Z2V[4]	0
Bit 11	R/W	Z2V[3]	0
Bit 10	R/W	Z2V[2]	0
Bit 9	R/W	Z2V[1]	0
Bit 8	R/W	Z2V[0]	0
Bit 7	R/W	E2V[7]	0
Bit 6	R/W	E2V[6]	0
Bit 5	R/W	E2V[5]	0
Bit 4	R/W	E2V[4]	0
Bit 3	R/W	E2V[3]	0
Bit 2	R/W	E2V[2]	0
Bit 1	R/W	E2V[1]	0
Bit 0	R/W	E2V[0]	0

E2V[7:0]

The E2 byte value (E2[7:0]) bits hold the line order wire to be inserted in the data stream. The E2V[7:0] value is inserted in the E2 byte of STS-1/STM-0 #1 if the insertion is enabled via the E2REGEN bit in the TRMP Register Insertion register.

Z2V[7:0]

The Z2 byte value (Z2V[7:0]) bits hold the Z2 growth byte to be inserted in the data stream. The Z2V[7:0] value is inserted in the Z2 byte if the insertion is enabled via the Z2REGEN bit in the TRMP Register Insertion register.

Register 1089H 1489H 1889H 1C89H: TRMP Transmit H1 and H2 Mask

Bit	Type	Function	Default
Bit 15	R/W	H1MASK[7]	0
Bit 14	R/W	H1MASK[6]	0
Bit 13	R/W	H1MASK[5]	0
Bit 12	R/W	H1MASK[4]	0
Bit 11	R/W	H1MASK[3]	0
Bit 10	R/W	H1MASK[2]	0
Bit 9	R/W	H1MASK[1]	0
Bit 8	R/W	H1MASK[0]	0
Bit 7	R/W	H2MASK[7]	0
Bit 6	R/W	H2MASK[6]	0
Bit 5	R/W	H2MASK[5]	0
Bit 4	R/W	H2MASK[4]	0
Bit 3	R/W	H2MASK[3]	0
Bit 2	R/W	H2MASK[2]	0
Bit 1	R/W	H2MASK[1]	0
Bit 0	R/W	H2MASK[0]	0

H2MASK[7:0]

The H2 mask (H2MASK[7:0]) bits hold the H2 path payload pointer errors to be inserted in the data stream. The H2MASK[7:0] is XOR'ed with the path payload pointer already in the data stream.

H1MASK[7:0]

The H1 mask (H1MASK[7:0]) bits hold the H1 path payload pointer errors to be inserted in the data stream. The H1MASK[7:0] is XOR'ed with the path payload pointer already in the data stream.

Register 108AH 148AH 188AH 1C8AH: TRMP Transmit B1 and B2 Mask

Bit	Type	Function	Default
Bit 15	R/W	B1MASK[7]	0
Bit 14	R/W	B1MASK[6]	0
Bit 13	R/W	B1MASK[5]	0
Bit 12	R/W	B1MASK[4]	0
Bit 11	R/W	B1MASK[3]	0
Bit 10	R/W	B1MASK[2]	0
Bit 9	R/W	B1MASK[1]	0
Bit 8	R/W	B1MASK[0]	0
Bit 7	R/W	B2MASK[7]	0
Bit 6	R/W	B2MASK[6]	0
Bit 5	R/W	B2MASK[5]	0
Bit 4	R/W	B2MASK[4]	0
Bit 3	R/W	B2MASK[3]	0
Bit 2	R/W	B2MASK[2]	0
Bit 1	R/W	B2MASK[1]	0
Bit 0	R/W	B2MASK[0]	0

B2MASK[7:0]

The B2 mask (B2MASK[7:0]) bits hold the B2 BIP-8 errors to be inserted in the data stream. The B2MASK[7:0] is XOR'ed with the calculated B2 before insertion in the B2 byte.

B1MASK[7:0]

The B1 mask (B1MASK[7:0]) bits hold the B1 BIP-8 errors to be inserted in the data stream. The B1MASK[7:0] is XOR'ed with the calculated B1 before insertion in the B1 byte.

Register 10A0H 14A0H 18A0H 1CA0H: TTTP SECTION Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	—	Unused	X
Bit 12	R/W	IADDR[6]	0
Bit 11	R/W	IADDR[5]	0
Bit 10	R/W	IADDR[4]	0
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	SECTION[3]	0
Bit 2	R/W	SECTION[2]	0
Bit 1	R/W	SECTION[1]	0
Bit 0	R/W	SECTION[0]	0

SECTION[3:0]

The STS-1/STM-0 section (SECTION[3:0]) bits select which STS-1/STM-0 timeslot is accessed by the current indirect transfer. SECTION[3:0] should be set to 0001.

IADDR[6:0]

The indirect address location (IADDR[6:0]) bits select which indirect address location is accessed by the current indirect transfer.

Indirect Address IADDR[6:0]	Indirect Data
000 0000	Configuration
000 0001 to 011 1111	Invalid address
100 0000	First byte of the 1/16/64 byte trace
100 0001 to 111 1111	Other bytes of the 16/64 byte trace

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0 upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

Register 10A1H 14A1H 18A1H 1CA1H: TTTP SECTION Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Indirect Register 00H: TTTP SECTION Trace Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R/W	ZEROEN	0
Bit 1	R/W	BYTEEN	0
Bit 0	R/W	LENGTH16	0

LENGTH16

The message length (LENGTH16) bit selects the length of the trail trace message to be transmitted. When LENGTH16 is set to logic 1, the length of the trail trace message is 16 bytes. When LENGTH16 is set to logic 0, the length of the trail trace message is 64 bytes.

BYTEEN

The single byte message enable (BYTEEN) bit enables the single byte trail trace message. When BYTEEN is set to logic 1, the length of the trail trace message is 1 byte. When BYTEEN is set to logic 0, the length of the trail trace message is determined by LENGTH16. BYTEEN has precedence over LENGTH16.

ZEROEN

The all zero message enable (ZEROEN) bit enables the transmission of an all zero trail trace message. When ZEROEN is set to logic 1, an all zero message is transmitted. When ZEROEN is set to logic 0, the RAM message is transmitted. The enabling and disabling of the all zero trail trace message is not done on message boundary since the receiver is required to perform filtering on the message.

Indirect Register 40H to 7FH: TTTP SECTION Trace

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	TRACE[7]	X
Bit 6	R/W	TRACE[6]	X
Bit 5	R/W	TRACE[5]	X
Bit 4	R/W	TRACE[4]	X
Bit 3	R/W	TRACE[3]	X
Bit 2	R/W	TRACE[2]	X
Bit 1	R/W	TRACE[1]	X
Bit 0	R/W	TRACE[0]	X

TRACE[7:0]

The trail trace message (TRACE[7:0]) bits contain the trail trace message to be transmitted. When BYTEEN is set to logic 1, the message is stored at indirect register address 40h. When BYTEEN is set to logic 0 and LENGTH16 is set to logic 1, the message is stored between indirect register address 40h and 4Fh. When BYTEEN is set to logic 0 and LENGTH16 is set to logic 0, the message is stored between indirect register address 40h and 7Fh.

Register 10C0H 14C0H 18C0H 1CC0H: TTTP PATH Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	—	Unused	X
Bit 12	R/W	IADDR[6]	0
Bit 11	R/W	IADDR[5]	0
Bit 10	R/W	IADDR[4]	0
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 timeslot/path is accessed by the current indirect transfer. PATH[3:0] should only be set to master timeslot values, ranging from 1 (0001) to 4 (0100).

IADDR[6:0]

The indirect address location (IADDR[6:0]) bits select which indirect address location is accessed by the current indirect transfer.

Indirect Address IADDR[6:0]	Indirect Data
000 0000	Configuration
000 0001 to 011 1111	Invalid address
100 0000	First byte of the 1/16/64 byte trace
100 0001 to 111 1111	Other bytes of the 16/64 byte trace

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0 upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

Register 10C1H 14C1H 18C1H 1CC1H: TTTP PATH Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Indirect Register 00H: TTTP PATH Trace Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R/W	ZEROEN	0
Bit 1	R/W	BYTEEN	0
Bit 0	R/W	LENGTH16	0

LENGTH16

The message length (LENGTH16) bit selects the length of the trail trace message to be transmitted. When LENGTH16 is set to logic 1, the length of the trail trace message is 16 bytes. When LENGTH16 is set to logic 0, the length of the trail trace message is 64 bytes.

BYTEEN

The single byte message enable (BYTEEN) bit enables the single byte trail trace message. When BYTEEN is set to logic 1, the length of the trail trace message is 1 byte. When BYTEEN is set to logic 0, the length of the trail trace message is determined by LENGTH16. BYTEEN has precedence over LENGTH16.

ZEROEN

The all zero message enable (ZEROEN) bit enables the transmission of an all zero trail trace message. When ZEROEN is set to logic 1, an all zero message is transmitted. When ZEROEN is set to logic 0, the RAM message is transmitted. The enabling and disabling of the all zero trail trace message is not done on message boundary since the receiver is required to perform filtering on the message.

Indirect Register 40H to 7FH: TTTP PATH Trace

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	TRACE[7]	X
Bit 6	R/W	TRACE[6]	X
Bit 5	R/W	TRACE[5]	X
Bit 4	R/W	TRACE[4]	X
Bit 3	R/W	TRACE[3]	X
Bit 2	R/W	TRACE[2]	X
Bit 1	R/W	TRACE[1]	X
Bit 0	R/W	TRACE[0]	X

TRACE[7:0]

The trail trace message (TRACE[7:0]) bits contain the trail trace message to be transmitted. When BYTEEN is set to logic 1, the message is stored at indirect register address 40h. When BYTEEN is set to logic 0 and LENGTH16 is set to logic 1, the message is stored between indirect register address 40h and 4Fh. When BYTEEN is set to logic 0 and LENGTH16 is set to logic 0, the message is stored between indirect register address 40h and 7Fh.

Register 1100H 1500H 1900H 1D00H: THPP Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path/timeslot is accessed by the current indirect transfer.

Path[3:0]	STS-1/STM-0 Path #
0000	Invalid path
0001	Path/timeslot #1
0010	Path/timeslot #2
0011	Path/timeslot #3
0100	Path/timeslot #4
0101-1111	Invalid path

IADDR[3:0]

The address location (IADDR[3:0]) bits select which address location is accessed by the current indirect transfer.

IADDR[3:0]	Indirect Register
0000	THPP Control Register
0001	THPP Source and Pointer Control
0010	Reserved
0011	Reserved
0100	THPP B3 Mask and Fixed stuff byte
0101	THPP Transmit C2 and J1
0110	THPP Transmit H4 Mask and G1

0111	THPP Transmit F2 and Z3
1000	THPP Transmit Z4 and Z5
1001 to 1111	Unused

RWB

The active high read and active low write (RWB) bit selects if the current access to an internal register is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to a register. When RWB is set to logic 1, an indirect read access to a register is initiated. The data from the addressed location as indicated using the IADDR field will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to a register is initiated. The data from the Indirect Data Register will be transferred to the addressed register.

BUSY

The active high busy (BUSY) bit reports if a previously initiated indirect access to an internal register has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0 upon completion of the access. This register should be polled to determine when new data is available in the Indirect Data Register.

Register 1101H 1501H 1901H 1D01H: THPP Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from an indirect register during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the register will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the register. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

Register 1102H 1502H 1902H 1D02H: THPP Reserved

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved1	0
Bit 2	R/W	Reserved1	0
Bit 1	R/W	Reserved1	0
Bit 0	R/W	Reserved1	0

Reserved1

The Reserved1 bits must be set to logic 1 for proper operation.

Reserved

The Reserved bits must be set to logic 0 for proper operation.

Indirect Register 00H: THPP Control Register

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	TDIS	0
Bit 4	—	Unused	X
Bit 3	R/W	FSBEN	0
Bit 2	R/W	PREIEBLK	0
Bit 1	R/W	Reserved	0
Bit 0	—	Unused	X

All Reserved bits must be set to their default values for proper operation.

PREIEBLK

The path REI block error (PREIEBLK) bit controls the extraction of path REI errors in the PREI monitoring block of the STS/AU pointer. When PREIEBLK is set to logic 1, the path REI extracted represents BIP-8 block errors (a maximum of 1 error per frame). When PREIEBLK is set to logic 0, the path REI extracted represents BIP-8 errors (a maximum of 8 errors per frame).

This bit is only valid for THPP master timeslots.

FSBEN

When the FSBEN register bit is logic one, THPP overwrites the fixed stuff bytes. The value used is that programmed in the FSB field of THPP Indirect Register 04H.

Note that fixed stuff bytes can't be overwritten when the source of the data to the THPP block is the APS input port. Fixed stuff bytes can only be overwritten when the data comes from the transmit PL3/UL3 sub-system (when register 0005H THPP_MUX[n] bit is set to logic 0).

This bit is valid for and should be consistent for all STS-1 timeslots containing fixed stuff bytes.

TDIS

When TDIS is set to logic one, the path overhead bytes are passed through transparently without being overwritten by the THPP. When TDIS is set to logic zero, the THPP inserts path overhead.

In a working/protect environment (using APS ports) using 2 S/UNI MULTI-48 devices, this bit should be set to logic 1 in all master timeslots of the "working" device to disable THPP since the "protect" THPP will be used for POH insertion.

This bit is only valid for THPP master timeslots.

Indirect Register 01H: THPP Source and Pointer Control Register

Bit	Type	Function	Default
Bit 15	R/W	UNEQV	0
Bit 14	R/W	UNEQ	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	ENG1REC	1
Bit 10	R/W	ENH4MASK	0
Bit 9	R/W	PTBJ1	0
Bit 8	R/W	SRCZ5	0
Bit 7	R/W	SRCZ4	0
Bit 6	R/W	SRCZ3	0
Bit 5	R/W	SRCF2	0
Bit 4	R/W	SRCG1	0
Bit 3	R/W	SRCH4	0
Bit 2	R/W	SRCC2	0
Bit 1	R/W	SRCJ1	0
Bit 0	R/W	IBER	0

IBER

When the IBER register bit is set to logic one, the G1 byte is passed through the THPP. It can then be generated by the SIRP block rather than THPP, or simply pass through the G1 value coming from the APS port. When IBER is set to logic zero, the G1 byte can be modified by one of the THPP POH sources.

This bit is only valid for THPP master timeslots.

SRCJ1, SRCC2, SRCH4, SRCG1, SRCF2, SRCZ3, SRCZ4, SRCZ5

The SRCnn bits are used to determine the source for the path overhead bytes. SRCnn bits are the lowest priority POH insertion control bits. They are only considered when all higher priority bits are disabled (see Table 9). When all applicable higher priority POH insertion control bits are disabled and a given SRCnn bit is set to logic 0, POH byte “nn” (nn = J1, C2, H4, G1, F2, Z3, Z4 or Z5) will be passed through untouched by the THPP. When all applicable higher priority POH insertion control bits are disabled and a given SRCnn bit is set to logic 1, POH byte “nn” will be overwritten with the value found in the applicable THPP POH value indirect register (see THPP indirect registers 05H to 08H).

This bit is only valid for THPP master timeslots.

PTBJ1

The PTBJ1 or Path Trace Buffer J1 byte register bit is used to determine the origin of the path trace byte to be inserted. When PTBJ1 is high, the J1 byte is sourced from the TTTP PATH block; otherwise, the J1 byte is not inserted at all as it is controlled using the SRCJ1 bit.

This bit is only valid for THPP master timeslots.

ENH4MASK

When ENH4MASK is logic high, the H4[7:0] byte in THPP Transmit H4 Mask and G1 register is used as an error mask on the H4 byte. When ENH4MASK is logic low, the H4[7:0] byte in THPP Transmit H4 Mask and G1 register is inserted as the H4 byte.

This bit is only valid for THPP master timeslots.

ENG1REC

The valid high ENG1REC register bit enables the insertion of the PRDI[2:0] and PREI[3:0] of the G1 byte from the SARC block. When ENG1REC is set to logic low, the G1 byte source is other than the SARC block.

UNEQ

The unequipped bit (UNEQ) controls the insertion of an all-one or an all-zero pattern in the payload, including path overhead and fixed stuff bytes.

The B3 value will be calculated and inserted such that the unequipped frame has a valid BIP.

When UNEQ is set to logic one, an all-one or an all-zero pattern is inserted in the payload (including path overhead and fixed stuff bytes). The UNEQV bit in this register determines the pattern. When UNEQ is set logic 0, no pattern is inserted.

UNEQV

The unequipped value (UNEQV) bit controls the value inserted in the payload. When UNEQV is set to logic 1, an all-one pattern is inserted in the payload if enabled via the UNEQ register bit. When UNEQV is set to logic 0, an all-zero pattern is inserted in the payload if enabled via the UNEQ register bit.

Indirect Register 04H: THPP Fixed Stuff Byte and B3 Mask (TFSB)

Bit	Type	Function	Default
Bit 15	R/W	B3MASK[7]	0
Bit 14	R/W	B3MASK[6]	0
Bit 13	R/W	B3MASK[5]	0
Bit 12	R/W	B3MASK[4]	0
Bit 11	R/W	B3MASK[3]	0
Bit 10	R/W	B3MASK[2]	0
Bit 9	R/W	B3MASK[1]	0
Bit 8	R/W	B3MASK[0]	0
Bit 7	R/W	FSB[7]	0
Bit 6	R/W	FSB[6]	0
Bit 5	R/W	FSB[5]	0
Bit 4	R/W	FSB[4]	0
Bit 3	R/W	FSB[3]	0
Bit 2	R/W	FSB[2]	0
Bit 1	R/W	FSB[1]	0
Bit 0	R/W	FSB[0]	0

FSB[7:0]

When the FSBEN bit in the THPP Control register is logic one, the THPP replaces the fixed stuff bytes with the byte from this register. Note that if the channel is unequipped, this field may be set to the same value that is indicated by UNEQV to insert FSB that is consistent with the rest of the payload.

Note that fixed stuff bytes can't be overwritten when the source of the data to the THPP block is the APS input port. Fixed stuff bytes can only be overwritten when the data comes from the transmit PL3/UL3 sub-system (when register 0005H THPP_MUX[n] bit is set to logic 0).

FSB[7:0] should be consistent for all THPP timeslots within a given concatenated payload.

B3MASK[7:0]

The calculated B3 parity byte is always XOR'ed with this register bit to allow the user to insert errors in B3.

B3MASK[7:0] is only valid for THPP master timeslots.

Indirect Register 05H: THPP Transmit J1 and C2

Bit	Type	Function	Default
Bit 15	R/W	C2[7]	0
Bit 14	R/W	C2[6]	0
Bit 13	R/W	C2[5]	0
Bit 12	R/W	C2[4]	0
Bit 11	R/W	C2[3]	0
Bit 10	R/W	C2[2]	0
Bit 9	R/W	C2[1]	0
Bit 8	R/W	C2[0]	0
Bit 7	R/W	J1[7]	0
Bit 6	R/W	J1[6]	0
Bit 5	R/W	J1[5]	0
Bit 4	R/W	J1[4]	0
Bit 3	R/W	J1[3]	0
Bit 2	R/W	J1[2]	0
Bit 1	R/W	J1[1]	0
Bit 0	R/W	J1[0]	0

J1[7:0]

The J1[7:0] bits are inserted in the J1 byte position when the SRCJ1 bit of the THPP Source & Pointer Control Register is logic 0. J1[7:0] is inserted into the J1 position of the POH when register insertion is enabled. See Table 9 Path Overhead Byte Source Priority for details.

This field is only valid for THPP master timeslots.

C2[7:0]

The C2[7:0] bits are inserted in the C2 byte position when the SRCC2 bit of the THPP Source & Pointer Control Register is logic 0. C2[7:0] is inserted into the C2 position of the POH when register insertion is enabled. See Table 9 Path Overhead Byte Source Priority for details.

This field is only valid for THPP master timeslots.

Indirect Register 06H: THPP Transmit G1 POH and H4 Mask (TG1H4POH)

Bit	Type	Function	Default
Bit 15	R/W	H4[7]	0
Bit 14	R/W	H4[6]	0
Bit 13	R/W	H4[5]	0
Bit 12	R/W	H4[4]	0
Bit 11	R/W	H4[3]	0
Bit 10	R/W	H4[2]	0
Bit 9	R/W	H4[1]	0
Bit 8	R/W	H4[0]	0
Bit 7	R/W	G1[7]	0
Bit 6	R/W	G1[6]	0
Bit 5	R/W	G1[5]	0
Bit 4	R/W	G1[4]	0
Bit 3	R/W	G1[3]	0
Bit 2	R/W	G1[2]	0
Bit 1	R/W	G1[1]	0
Bit 0	R/W	G1[0]	0

G1[7:0]

The G1[7:0] bits are inserted in the G1 byte position when the SRCG1 bit of the Source and Pointer Control Register is high. G1[7:0] is inserted into the G1 position of the POH when register insertion is enabled. See Table 9 Path Overhead Byte Source Priority for details.

This field is only valid for THPP master timeslots.

H4[7:0]

The H4[7:0] bits are inserted in the H1 byte position when the ENH4MASK bit of the Source and Pointer Control Register is high. H4[7:0] is inserted into the H4 position of the POH when register insertion is enabled. See Table 9 Path Overhead Byte Source Priority for details.

This field is only valid for THPP master timeslots.

Indirect Register 07H: THPP Transmit F2 and Z3 POH (TF2Z3POH)

Bit	Type	Function	Default
Bit 15	R/W	F2[7]	0
Bit 14	R/W	F2[6]	0
Bit 13	R/W	F2[5]	0
Bit 12	R/W	F2[4]	0
Bit 11	R/W	F2[3]	0
Bit 10	R/W	F2[2]	0
Bit 9	R/W	F2[1]	0
Bit 8	R/W	F2[0]	0
Bit 7	R/W	Z3[7]	0
Bit 6	R/W	Z3[6]	0
Bit 5	R/W	Z3[5]	0
Bit 4	R/W	Z3[4]	0
Bit 3	R/W	Z3[3]	0
Bit 2	R/W	Z3[2]	0
Bit 1	R/W	Z3[1]	0
Bit 0	R/W	Z3[0]	0

Z3[7:0]

The Z3[7:0] bits are inserted in the Z3 byte position when the SRCZ3 bit of the THPP Source and Pointer Control Register is logic 0. Z3[7:0] is inserted into the Z3 position of the POH when register insertion is enabled. See Table 9 Path Overhead Byte Source Priority for details.

This field is only valid for THPP master timeslots.

F2[7:0]

The F2[7:0] bits are inserted in the F2 byte position when the SRCF2 bit of the THPP Source and Pointer Control Register is logic 0. F2[7:0] is inserted into the F2 position of the POH when register insertion is enabled. See Table 9 Path Overhead Byte Source Priority for details.

This field is only valid for THPP master timeslots.

Indirect Register 08H: THPP Transmit Z4 and Z5 Overhead (TZ4Z5POH)

Bit	Type	Function	Default
Bit 15	R/W	Z4[7]	0
Bit 14	R/W	Z4[6]	0
Bit 13	R/W	Z4[5]	0
Bit 12	R/W	Z4[4]	0
Bit 11	R/W	Z4[3]	0
Bit 10	R/W	Z4[2]	0
Bit 9	R/W	Z4[1]	0
Bit 8	R/W	Z4[0]	0
Bit 7	R/W	Z5[7]	0
Bit 6	R/W	Z5[6]	0
Bit 5	R/W	Z5[5]	0
Bit 4	R/W	Z5[4]	0
Bit 3	R/W	Z5[3]	0
Bit 2	R/W	Z5[2]	0
Bit 1	R/W	Z5[1]	0
Bit 0	R/W	Z5[0]	0

Z5[7:0]

The Z5[7:0] bits are inserted in the Z5 byte position when the SRCZ5 bit of the THPP Source and Pointer Control Register is logic 0. Z5[7:0] is inserted into the Z5 position of the POH when register insertion is enabled. See Table 9 Path Overhead Byte Source Priority for details.

This field is only valid for THPP master timeslots.

Z4[7:0]

The Z4[7:0] bits are inserted in the Z4 byte position when the SRCZ4 bit of the THPP Source and Pointer Control Register is logic 0. Z4[7:0] is inserted into the Z4 position of the POH when register insertion is enabled. See Table 9 Path Overhead Byte Source Priority for details.

This field is only valid for THPP master timeslots.

Register 1200H 1600H 1A00H 1E00H: TSVCA Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer. Refer to Section 13.8 for details on TSVCA indirect register access.

Path[3:0]	STS-1/STM-0 Path #
0000	Invalid path
0001-1100	Path #1 to Path #12
1101-1110	Invalid path
1111	Invalid path

IADDR[1:0]

The address location (IADDR[1:0]) bits select which address location is accessed by the current indirect transfer. Refer to Section 13.8 for details on TSVCA indirect register access

IADDR[1:0]	Indirect Register
00	SVCA Outgoing Pointer Justification Performance Monitor
01	SVCA Outgoing Negative Justification Performance Monitor
10	SVCA Diagnostic/Configuration Register
11	Unused

RWB

The active high read and active low write (RWB) bit selects if the current access to an internal register is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to a register. When RWB is set to logic 1, an indirect read access to a register is initiated. The data from the addressed location as indicated using the IADDR field will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to a register is initiated. The data from the Indirect Data Register will be transferred to the addressed register.

BUSY

The active high busy (BUSY) bit reports if a previously initiated indirect access to an internal register has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0 upon completion of the access. This register should be polled to determine when new data is available in the Indirect Data Register.

Register 1201H 1601H 1A01H 1E01H: TSVCA Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from an indirect register during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the register will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the register. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

Register 1202H 1602H 1A02H 1E02H: TSVCA Reserved #1

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved1	0
Bit 2	R/W	Reserved1	0
Bit 1	R/W	Reserved1	0
Bit 0	R/W	Reserved1	0

Reserved1

The Reserved1 bits must be set to logic 1 for proper operation.

Reserved

The Reserved bits must be set to logic 0 for proper operation.

Register 1203H 1603H 1A03H 1E03H: TSVCA Positive Justification Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	PPJI[4]	X
Bit 2	R	PPJI[3]	X
Bit 1	R	PPJI[2]	X
Bit 0	R	PPJI[1]	X

PPJI[4:1]

The positive pointer justification interrupt status (PPJI[4:1]) bits are event indicators for STS-1/STM-0 paths/timeslots #1 to #4. PPJI[4:1] are set to logic 1 to indicate a positive pointer justification event in the outgoing data stream. These interrupt status bits are independent of the interrupt enable bits. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears this bit.

Register 1204H 1604H 1A04H 1E04H: TSVCA Negative Justification Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	NPJI[4]	X
Bit 2	R	NPJI[3]	X
Bit 1	R	NPJI[2]	X
Bit 0	R	NPJI[1]	X

NPJI[4:1]

The negative pointer justification interrupt status (NPJI[4:1]) bits are event indicators for STS-1/STM-0 paths/timeslots #1 to #4. NPJI[4:1] are set to logic 1 to indicate a negative pointer justification event in the outgoing data stream. These interrupt status bits are independent of the interrupt enable bits. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears this bit.

Register 1205H 1605H 1A05H 1E05H: TSVCA FIFO Overflow Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	FOVRI[4]	X
Bit 2	R	FOVRI[3]	X
Bit 1	R	FOVRI[2]	X
Bit 0	R	FOVRI[1]	X

FOVRI[4:1]

The FIFO overflow event interrupt status (FOVRI[4:1]) bits are event indicators for STS-1/STM-0 paths/timeslots #1 to #4. FOVRI[4:1] are set to logic 1 to indicate a FIFO overflow event. These interrupt status bits are independent of the interrupt enable bits. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears this bit.

Register 1206H 1606H 1A06H 1E06H: TSVCA FIFO Underflow Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	FUDRI[4]	X
Bit 2	R	FUDRI[3]	X
Bit 1	R	FUDRI[2]	X
Bit 0	R	FUDRI[1]	X

FUDRI[4:1]

The FIFO underflow event interrupt status (FUDR[4:1]) bits are event indicators for STS-1/STM-0 paths/timeslots #1 to #4. FUDRI[4:1] are set to logic 1 to indicate a FIFO underflow event. These interrupt status bits are independent of the interrupt enable bits. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears this bit.

Register 1207H 1607H 1A07H 1E07H: TSVCA Pointer Justification Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	PJIEN[4]	0
Bit 2	R/W	PJIEN[3]	0
Bit 1	R/W	PJIEN[2]	0
Bit 0	R/W	PJIEN[1]	0

PJIEN[4:1]

The pointer justification event interrupt enable (PJIEN[4:1]) bits control the activation of the interrupt (INT) output for STS-1/STM-0 paths/timeslots #1 to #4. When any of these bit locations is set to logic 1, the corresponding pending interrupt will assert the interrupt (INT) output. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INT) output. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears this bit.

Register 1208H 1608H 1A08H 1E08H: TSVCA FIFO Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	FIEN[4]	0
Bit 2	R/W	FIEN[3]	0
Bit 1	R/W	FIEN[2]	0
Bit 0	R/W	FIEN[1]	0

FIEN[4:1]

The FIFO event interrupt enable (FIEN[4:1]) bits control the activation of the interrupt (INT) output for STS-1/STM-0 paths/timeslots #1 to #4 caused by a FIFO overflow or a FIFO underflow. When any of these bit locations is set to logic 1, the corresponding pending interrupt will assert the interrupt (INT) output. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INT) output. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears this bit.

Register 1209H 1609H 1A09H 1E09H: TSVCA Reserved #2

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	1
Bit 13	R/W	Reserved	1
Bit 12	R/W	Reserved	1
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	1
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

Reserved

All Reserved bits must be set to their default value for proper operation.

Register 120AH 160AH 1A0AH 1E0AH: TSVCA Reserved #3

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Register 120BH 160BH 1A0BH 1E0BH: TSVCA Performance Monitor Trigger

Any write to this register triggers a transfer of all local TSVCA performance monitor counters to holding registers that can be read by the microprocessor interface. This is a write only register.

Indirect Register 00H: TSVCA Positive Justifications Performance Monitor

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	R	PJPMON[12]	0
Bit 11	R	PJPMON[11]	0
Bit 10	R	PJPMON[10]	0
Bit 9	R	PJPMON[9]	0
Bit 8	R	PJPMON[8]	0
Bit 7	R	PJPMON[7]	0
Bit 6	R	PJPMON[6]	0
Bit 5	R	PJPMON[5]	0
Bit 4	R	PJPMON[4]	0
Bit 3	R	PJPMON[3]	0
Bit 2	R	PJPMON[2]	0
Bit 1	R	PJPMON[1]	0
Bit 0	R	PJPMON[0]	0

PJPMON[12:0]

This register reports the number of positive pointer justification events that occurred on the outgoing side in the previous accumulation interval. The content of this register becomes valid after a transfer is triggered by writing to the TSVCA Performance Monitor Trigger register (0x120B, 0x160B, 0x1A0B, 0x1E0B) or the S/UNI MULTI-48 Global Performance Monitor Update register (0002H).

Note that the PJPMON[12:0] count value is only valid for STS-N master timeslots.

Indirect Register 01H: TSVCA Negative Justifications Performance Monitor

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	R	NJPMON[12]	0
Bit 11	R	NJPMON[11]	0
Bit 10	R	NJPMON[10]	0
Bit 9	R	NJPMON[9]	0
Bit 8	R	NJPMON[8]	0
Bit 7	R	NJPMON[7]	0
Bit 6	R	NJPMON[6]	0
Bit 5	R	NJPMON[5]	0
Bit 4	R	NJPMON[4]	0
Bit 3	R	NJPMON[3]	0
Bit 2	R	NJPMON[2]	0
Bit 1	R	NJPMON[1]	0
Bit 0	R	NJPMON[0]	0

NJPMON[12:0]

This register reports the number of negative pointer justification events that occurred on the outgoing side in the previous accumulation interval. The content of this register becomes valid after a transfer is triggered by writing to the TSVCA Performance Monitor Trigger register (0x120B, 0x160B, 0x1A0B, 0x1E0B) or the S/UNI MULTI-48 Global Performance Monitor Update register (0002H).

Note that the NJPMON[12:0] count value is only valid for STS-N master timeslots.

Indirect Register 02H: TSVCA Diagnostic/Configuration

Bit	Type	Function	Default
Bit 15	R/W	PTRRST	0
Bit 14	R/W	PTRSS[1]	0
Bit 13	R/W	PTRSS[0]	0
Bit 12	R/W	JUST3DIS	0
Bit 11	R/W	PTRDD[1]	0
Bit 10	R/W	PTRDD[2]	0
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R/W	Reserved	0
Bit 5	R/W	Diag_NDFREQ	0
Bit 4	R/W	Diag_FifoAISDis	0
Bit 3	R/W	Diag_PAIS	0
Bit 2	R/W	Diag_LOP	0
Bit 1	R/W	Diag_NegJust	0
Bit 0	R/W	Diag_PosJust	0

Diag_PosJust

The Diag_PosJust bit forces the TSVCA to generate outgoing positive justification events. When set to 1, the TSVCA generates positive justification events at the rate of one every four frames regardless of the current level of the internal FIFO. Note that the TSVCA will follow up with an automatic negative pointer justification if it needs to do so in order to keep its FIFO fill levels under control. The diagnostic feature has a lower priority than the FIFO monitor.

Diag_PosJust and Diag_NegJust must not be set to one at the same time. If that occurs, their operation is disabled.

Diag_NegJust

The Diag_NegJust bit forces the TSVCA to generate outgoing negative justification events. When set to 1, the TSVCA generates negative justification events at the rate of one every four frames regardless of the current level of the internal FIFO. Note that the TSVCA will follow up with an automatic negative pointer justification if it needs to do so in order to keep its FIFO fill levels under control. The diagnostic feature has a lower priority than the FIFO monitor.

Diag_PosJust and Diag_NegJust must not be set to one at the same time. If that occurs, their operation is disabled.

Diag_LOP

When set high, the Diag_LOP bit forces the TSVCA to invert the outgoing NDF field of the payload (selected path(s)) pointer causing downstream pointer processing elements to enter a loss of pointer (LOP) state.

Diag_PAIS

When set high, the Diag_PAIS bit forces the TSVCA to insert path AIS in the selected outgoing stream for at least three consecutive frames. AIS is inserted by writing an all ones pattern in the transport overhead bytes H1, H2, and H3, as well as in the entire STS synchronous payload envelope. The first frame after PAIS negates will contain a new data flag in the transport overhead H1 byte.

Diag_FifoAISDis

When set high, the Diag_FifoAISDis bit forces the TSVCA not to insert path AIS upon FIFO overflow/underflow detection. When set low (normal operation), detection of FIFO overflow/underflow causes path AIS to be inserted in the outgoing stream for at least three consecutive frames.

Note: When Diag_FifoAISDis is enabled, any overflow or underflow will cause the TSVCA to declare both FUDR and FOVR interrupts.

Diag_NDFREQ

When set high, the Diag_NDFREQ bit forces the TSVCA to insert a NEW DATA FLAG indication in the frame regardless of the state of the pointer generation state machine. This bit should be set for less than one frame as multiple NDF will otherwise cause the downstream pointer processor to declare LOP.

After any timeslot is reconfigured, the corresponding Diag_NDFREQ bit must be toggled.

PTRDD[1:0]

The PTRDD[1:0] defines the SS bits for the STS-N/AU-N concatenation pointer (may also be known as DD). ITU requires that DD be set to 10 when processing AU-4. Note, TELCORDIA does not specify these two bits.

JUST3DIS

When set high, JUST3DIS allows the TSVCA to perform up to 1 justification per frame when necessary. When set to zero, pointer justifications are allowed only every 4 frames.

PTRSS[1:0]

The PTRSS[1:0] defines the STS-N/AU-N pointer bits SS. ITU requires that SS be set to 10 when processing AU-4. Note, TELCORDIA does not specify these two bits. The SS bits are set to 00 when processing a slave STS-1 timeslot.

PTRRST

When set high, incoming and outgoing pointers are reset to their default values. This bit is level sensitive.

Register 1240H 1640H 1A40H 1E40H: PRGM Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path/timeslot is accessed by the current indirect transfer. For the S/UNI MULTI-48, PATH[3:0] is normally set to range 1H to 4H except when accessing the monitor error counter, interrupts and status registers for all timeslots, including slave timeslots. In this clast case, the range is 1H to CH.

IADDR[3:0]

The internal address bits select which internal register is accessed by the current indirect transfer.

IADDR[3:0]	Register
0000	Monitor – Timeslot Configuration page
0001	Monitor – PRBS[22:7] page
0010	Monitor – PRBS[6:0] page
0011	Reserved
0100	Monitor – Monitor error count page
0101	Reserved
1000	Generator – Timeslot Configuration page
1001	Generator – PRBS[22:7] page
1010	Generator – PRBS[6:0] page
1011	Reserved

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal register is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal register. When RWB is set to logic 1, an indirect read access to the register is initiated. The data from the addressed location in the internal register will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the register is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal register. Do not write to indirect registers 04H to 07H.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal register has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0 upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

Register 1241H 1641H 1A41H 1E41H: PRGM Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from an internal register during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal register will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal register. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which internal register is being accessed.

Register 1242H 1642H 1A42H 1E42H: PRGM Generator Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	GEN_STS12CSL	0
Bit 14	R/W	GEN_STS12C	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	R/W	GEN_MSSLEN[2]	0
Bit 9	R/W	GEN_MSSLEN[1]	0
Bit 8	R/W	GEN_MSSLEN[0]	0
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	Reserved1	0
Bit 2	R/W	Reserved1	0
Bit 1	R/W	Reserved1	0
Bit 0	R/W	Reserved1	0

Reserved1

The Reserved1 bits must be set to logic 1 for proper operation.

Reserved

All Reserved bits must be set to their default values for proper operation.

GEN_MSSLEN[2:0], GEN_STS12C, GEN_STS12CSL

These bits control the operating mode of the PRGM generators. The bits should be set according to the table below.

PRGM	GEN_STS12C	GEN_STS12CSL	GEN_MSSLEN[2:0]
Master	1	0	011
Slave	1	1	011

GEN_MSSLEN[2:0]

The Master/Slave Configuration Enable enables the master/slave configuration of the PRGM's generator.

GEN_MSSLEN[2:0]	Configuration
000	ms/sl configuration disable (STS-12c/VC-4-4c or STS-3c/VC-4)
011	ms/sl configuration enable

GEN_MSSLEN[2:0]	Configuration
	4 PRGMs (STS-48c/VC-4-16c)
others	Invalid configuration

GEN_MSSLEN[2:0] must be set to “000” for payload rates STS-12c and below.

GEN_STS12C

The STS-12c/VC-4-4c payload configuration (GEN_STS12C) bit selects the payload configuration. When GEN_STS12C is set to logic 1, the timeslots #1 to #12 are part of the same concatenated payload defined by GEN_MSSLEN. When GEN_STS12C is set to logic 0, the STS-1/STM-0 paths are defined as STS-3c (VC-4) payloads.

GEN_STS12CSL

The slave STS-12c/VC-4-4c payload configuration (GEN_STS12CSL) bit selects the slave payload configuration. When GEN_STS12CSL is set to logic 1, the timeslots #1 to #12 are part of a slave payload. When GEN_STS12CSL is set to logic 0, the timeslots #1 to # 12 are part of a concatenate master payload.

Registers Configuration To Select Payload Type

Mode	Payload	STS12C	STS12CSL	MSSLEN[2:0]
Master	Rates lower than STS-12c/VC-4-4c	0	0	000
Master	STS-12c/VC-4-4c	1	0	000
Master				
	STS-48c/VC-4-16c, slice 1	1	0	011
Slave				
	STS-48c/VC-4-16c, slices 2-4	1	1	011

Register 1243H 1643H 1A43H 1E43H: PRGM Monitor Payload Configuration Register

Bit	Type	Function	Default
Bit 15	R/W	MON_STS12CSL	0
Bit 14	R/W	MON_STS12C	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	R/W	MON_MSSLEN[2]	0
Bit 9	R/W	MON_MSSLEN[1]	0
Bit 8	R/W	MON_MSSLEN[0]	0
Bit 7	—	Unused	X
Bit 6	R/W	Reserved	0
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	Reserved1	0
Bit 2	R/W	Reserved1	0
Bit 1	R/W	Reserved1	0
Bit 0	R/W	Reserved1	0

Reserved1

The Reserved1 bits must be set to logic 1 for proper operation.

Reserved

All Reserved bits must be set to their default values for proper operation.

MON_MSSLEN[2:0], MON_STS12C, MON_STS12CSL

These bits control the operating mode of the PRGM monitors. The bits should be set according to the table below.

PRGM	MON_STS12C	MON_STS12CSL	MON_MSSLEN[2:0]
Master	1	0	011
Slave	1	1	011

MON_MSSLEN[2:0]

The Master/Slave Configuration Enable enables the master/slave configuration of the PRGM's monitor.

GEN_MSSLEN[2:0]	Configuration
000	ms/sl configuration disable (STS-12c/VC-4-4c or STS-3c/VC-4)
011	ms/sl configuration enable

GEN_MSSLEN[2:0]	Configuration
	4 PRGMs (STS-48c/VC-4-16c)
others	Invalid configuration

MON_MSSLEN[2:0] must be set to "000" for payload rates STS-12c and below.

MON_STS12C

The STS-12c/VC-4-4c payload configuration (MON_STS12C) bit selects the payload configuration. When MON_STS12C is set to logic 1, the timeslots #1 to #12 are part of the same concatenated payload defined by MON_MSSLEN. When MON_STS12C is set to logic 0, the STS-1/STM-0 paths are defined as STS-3c (VC-4) payloads.

MON_STS12CSL

The slave STS-12c/VC-4-4c payload configuration (MON_STS12CSL) bit selects the slave payload configuration. When MON_STS12CSL is set to logic 1, the timeslots #1 to #12 are part of a slave payload. When MON_STS12CSL is set to logic 0, the timeslots #1 to # 12 are part of a concatenate master payload.

Register 1244H 1644H 1A44H 1E44H: PRGM Monitor Byte Error Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	MON[12]_ERRI	X
Bit 10	R	MON[11]_ERRI	X
Bit 9	R	MON[10]_ERRI	X
Bit 8	R	MON[9]_ERRI	X
Bit 7	R	MON[8]_ERRI	X
Bit 6	R	MON[7]_ERRI	X
Bit 5	R	MON[6]_ERRI	X
Bit 4	R	MON[5]_ERRI	X
Bit 3	R	MON[4]_ERRI	X
Bit 2	R	MON[3]_ERRI	X
Bit 1	R	MON[2]_ERRI	X
Bit 0	R	MON[1]_ERRI	X

MON**x**_ERRI

The Monitor Byte Error Interrupt Status registers contain the status of the interrupt generated by each of the 48 STS-1 timeslots when an error has been detected.

The MON**x**_ERRI bit is set high when the monitor is in the synchronized state and when an error in a PRBS byte is detected in the STS-1 timeslot **x**. This bit is independent of MON**x**_ERRE, and is cleared after it has been read. MONx_ERRI is cleared to logic 0 when this register is read if WCIMODE is set to logic 0. MONx_ERRI is cleared only when it is written to logic 1 if WCIMODE is set to logic 1.

Register 1245H 1645H 1A45H 1E45H: PRGM Monitor Byte Error Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	MON[12]_ERRE	0
Bit 10	R/W	MON[11]_ERRE	0
Bit 9	R/W	MON[10]_ERRE	0
Bit 8	R/W	MON[9]_ERRE	0
Bit 7	R/W	MON[8]_ERRE	0
Bit 6	R/W	MON[7]_ERRE	0
Bit 5	R/W	MON[6]_ERRE	0
Bit 4	R/W	MON[5]_ERRE	0
Bit 3	R/W	MON[4]_ERRE	0
Bit 2	R/W	MON[3]_ERRE	0
Bit 1	R/W	MON[2]_ERRE	0
Bit 0	R/W	MON[1]_ERRE	0

MON**x**_ERRE

The Monitor Byte Error Interrupt Enable registers enable the interrupt for each of the 48 STS-1 timeslots.

When MON**x**_ERRE is set high, the Byte Error Interrupt is allowed to generate an interrupt on INTB.

Register 1249H 1649H 1A49H 1E49H: PRGM Monitor Synchronization Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	MON[12]_SYNCI	X
Bit 10	R	MON[11]_SYNCI	X
Bit 9	R	MON[10]_SYNCI	X
Bit 8	R	MON[9]_SYNCI	X
Bit 7	R	MON[8]_SYNCI	X
Bit 6	R	MON[7]_SYNCI	X
Bit 5	R	MON[6]_SYNCI	X
Bit 4	R	MON[5]_SYNCI	X
Bit 3	R	MON[4]_SYNCI	X
Bit 2	R	MON[3]_SYNCI	X
Bit 1	R	MON[2]_SYNCI	X
Bit 0	R	MON[1]_SYNCI	X

MON**x**_SYNCI

The Monitor Synchronization Interrupt Status registers indicate synchronization interrupts for each of the 48 STS-1 timeslots.

The Monitor Synchronization Interrupt Status Interrupt (MON**x**_SYNCI) bit is set high when a change occurs in the monitor's synchronization status. Whenever a state machine of the **x** STS-1 timeslot goes from Synchronized to Out Of Synchronization state or vice-versa, the MON**x**_SYNCI is set high. For concatenated payloads, only the STS-1 timeslot state machine that first detects the change in Synchronization Status in this PRBS monitor will set MONx_SYNCI high. This bit is independent of MONx_SYNCE. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

Note that the PRGM will synchronize on an all zeros or all ones pattern. To verify that a valid PRBS pattern is the signal the PRGM is locked to, check the PRBS[22:0] bits in the PRGM Monitor PRBS Accumulator Page. If the bits are not all zeroes or all ones, then the synchronization is due to locking on a valid PRBS pattern.

Register 124AH 164AH 1A4AH 1E4AH: PRGM Monitor Synchronization Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	MON[12]_SYNCE	0
Bit 10	R/W	MON[11]_SYNCE	0
Bit 9	R/W	MON[10]_SYNCE	0
Bit 8	R/W	MON[9]_SYNCE	0
Bit 7	R/W	MON[8]_SYNCE	0
Bit 6	R/W	MON[7]_SYNCE	0
Bit 5	R/W	MON[6]_SYNCE	0
Bit 4	R/W	MON[5]_SYNCE	0
Bit 3	R/W	MON[4]_SYNCE	0
Bit 2	R/W	MON[3]_SYNCE	0
Bit 1	R/W	MON[2]_SYNCE	0
Bit 0	R/W	MON[1]_SYNCE	0

MON**x**_SYNCE

The Monitor Synchronization Interrupt Enable registers enables the synchronization interrupts for each of the 48 STS-1 timeslots.

The Monitor Synchronization Interrupt Enable register allows each individual STS-1 timeslost to generate an external interrupt on INTB. When MON**x**_SYNCE is set high, a change in the synchronization state of the monitor in STS-1 timeslot **x** generates an interrupt on INTB.

Register 124BH 164BH 1A4BH 1E4BH: PRGM Monitor Synchronization Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	MON[12]_SYNCV	X
Bit 10	R	MON[11]_SYNCV	X
Bit 9	R	MON[10]_SYNCV	X
Bit 8	R	MON[9]_SYNCV	X
Bit 7	R	MON[8]_SYNCV	X
Bit 6	R	MON[7]_SYNCV	X
Bit 5	R	MON[6]_SYNCV	X
Bit 4	R	MON[5]_SYNCV	X
Bit 3	R	MON[4]_SYNCV	X
Bit 2	R	MON[3]_SYNCV	X
Bit 1	R	MON[2]_SYNCV	X
Bit 0	R	MON[1]_SYNCV	X

MON**x**_SYNCV

The Monitor Synchronization Status registers reflects the synchronization state of each STS-1 timeslot.

The Monitor Synchronization Status registers reflect the state of the monitor's state machine. When MON**x**_SYNCV is set high, the monitor's state machine is in synchronization for the STS-1 timeslot **x**. When MON**x**_SYNCV is low, the monitor is out of sync for the STS-1 timeslot **x**. The Synchronization Status is only valid when the corresponding monitor is enabled.

Note that the PRGM will synchronize on an all zeros or all ones pattern. To verify that a valid PRBS pattern is the signal the PRGM is locked to, check the PRBS[22:0] bits in the PRGM Monitor PRBS Accumulator Page. If the bits are not all zeroes or all ones, then the synchronization is due to locking on a valid PRBS pattern.

Register 124CH 164CH 1A4CH 1E4CH: PRGM Performance Counters Transfer Trigger

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R	TIP	X

A write in this register will trigger the transfer of the error counters for that slice to holding registers from which they can be read. The value written in the register is not important. Once the transfer is initiated, the TIP bit is set high, and when the holding registers contain the value of the error counters, TIP is set low.

TIP

The Transfer In Progress bit reflects the state of the TIP output signal. When TIP is high, an error counter transfer has been initiated, but the counters are not transferred to the holding register yet. When TIP is low, the value of the error counters are available to be read in the holding registers. This bit can be polled after an error counters transfer request to determine if the counters are ready to be read.

Indirect Register 00H: PRGM Monitor Timeslot Configuration Page

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R/W	SEQ_PRBSB	0
Bit 5	R/W	Reserved	0
Bit 4	—	Unused	X
Bit 3	W	RESYNC	0
Bit 2	R/W	INV_PRBS	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	MON_ENA	0

All Reserved bits must be set to their default values for proper operation.

MON_ENA

The Monitor Enable register bit enables the PRBS monitors for the PRGM blocks (all timeslots). If MON_ENA is set high, a PRBS sequence is generated and compared to the incoming PRBS sequence inserted in the payload of the SONET/SDH frame. If MON_ENA is low, the input monitor data is ignored.

INV_PRBS

INV_PRBS sets the monitor to invert the PRBS before comparing it to the internally generated payload. When set high, the PRBS bytes will be inverted. When set low, the PRBS bytes will be compared unmodified.

RESYNC

RESYNC sets the monitor to re-initialize the PRBS sequence. When set high, the monitor's state machines will be forced in the Out Of Sync state and will automatically try to resynchronize to the incoming stream. To force another resynchronization, the bit needs to be set low again before it is set high.

SEQ_PRBSB

SEQ_PRBSB enables the monitoring of a PRBS or sequential pattern inserted in the payload. When low, the payload is expected to contain PRBS bytes. When high, the payload is expected to contain a sequential pattern.

Indirect Register 01H: PRGM Monitor PRBS[22:7] Accumulator Page

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	PRBS[22:7]	0000

Indirect Register 02H: PRGM Monitor PRBS[6:0] Accumulator Page

Bit	Type	Function	Default
Bit 15 to Bit 7	—	Unused	00
Bit 6 to Bit 0	R/W	PRBS[6:0]	00

PRBS[22:0]

The PRBS[22:0] register contains the state of the LFSR monitor. It is possible to write to this register to change the initial state of the monitor.

Indirect Register 04H: PRGM Monitor Error Count Page

Bit	Type	Function	Default
Bit 15	R	ERR_CNT[15]	X
Bit 14	R	ERR_CNT[14]	X
Bit 13	R	ERR_CNT[13]	X
Bit 12	R	ERR_CNT[12]	X
Bit 11	R	ERR_CNT[11]	X
Bit 10	R	ERR_CNT[10]	X
Bit 9	R	ERR_CNT[9]	X
Bit 8	R	ERR_CNT[8]	X
Bit 7	R	ERR_CNT[7]	X
Bit 6	R	ERR_CNT[6]	X
Bit 5	R	ERR_CNT[5]	X
Bit 4	R	ERR_CNT[4]	X
Bit 3	R	ERR_CNT[3]	X
Bit 2	R	ERR_CNT[2]	X
Bit 1	R	ERR_CNT[1]	X
Bit 0	R	ERR_CNT[0]	X

ERR_CNT[15:0]

The ERR_CNT[15:0] register is the number of errors in the PRBS bytes detected during monitoring. Errors are generally accumulated only when the monitor is in the synchronized state. Even if there are multiple errors within one PRBS byte, only one error is counted. The transfer of the error counter to this holding register is triggered by an indirect write to the PRGM Performance Counters Transfer Trigger register for the particular STS-12 slice (register 124CH, 164CH, 1A4CH or 1E4CH respectively) or by writing to register 0002H for a global performance monitor update. Do not write to this register. The error counter will not wrap around after reaching FFFFH. It will saturate to this value.

Note that the 3 errors which cause the PRGM to lose synchronization may be counted as 3, 4, or 5 errors.

Indirect Register 08H: PRGM Generator Timeslot Configuration Page

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R/W	Reserved	0
Bit 12	R/W	PRBS_ENA	0
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	S[1]	0
Bit 6	R/W	S[0]	0
Bit 5	R/W	SEQ_PRBSB	0
Bit 4	R/W	Reserved	0
Bit 3	W	FORCE_ERR	0
Bit 2	—	Unused	X
Bit 1	R/W	INV_PRBS	0
Bit 0	R/W	Reserved	0

All Reserved bits must be set to their default values for proper operation.

INV_PRBS

INV_PRBS sets the generator to invert the PRBS before inserting it in the payload. When set high, the PRBS bytes will be inverted. When set low, the PRBS bytes will be inserted unmodified.

FORCE_ERR

The Force Error bit is used to force bit errors in the inserted pattern. When set high, the MSB of the next byte will be inverted, inducing a single bit error. The register will clear itself when the operation is complete. A read operation will always result in a logic '0'.

SEQ_PRBSB

SEQ_PRBSB enables the insertion of a X23+X18+1 PRBS sequence or a sequential pattern in the payload. When low, the payload is filled with PRBS bytes. When high, a sequential pattern is inserted.

S[1:0]

The S[1:0] bits contain the value inserted in the S[1:0] bit positions in the payload pointer.

PRBS_ENA

This bit specifies if PRBS overwriting is enabled. If PRBS_ENA is high, X23+X18+1 PRBS patterns are generated and are used to overwrite the data stream. If PRBS_ENA is low, no pattern is generated and the data stream is not overwritten.

Indirect Register 09H : PRGM Generator PRBS[22:7] Accumulator Page

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	PRBS[22:7]	0000

Indirect Register 0AH: PRGM Generator PRBS[6:0] Accumulator Page

Bit	Type	Function	Default
Bit 15 to Bit 7	—	Unused	00
Bit 6 to Bit 0	R/W	PRBS[6:0]	00

PRBS[22:0]

The PRBS[22:0] register contains the state of the LFSR generator. It is possible to write in this register to change the initial state of the generator.

Register 1260H 1261H 1262H 1263H 1660H 1661H 1662H 1663H 1A60H 1A61H 1A62H 1A63H 1E60H 1E61H 1E62H 1E63H: SIRP Timeslot Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	TSx_RDI20F	0
Bit 3	R/W	TSx_ERDI	0
Bit 2	R/W	Reserved	1
Bit 1	R/W	Reserved	1
Bit 0	R/W	TSx_PROV	0

Register 1260H is used to configure timeslot 1 (TS1), register 1261H is used to configure timeslot 2 (TS2), register 1262H is used to configure timeslot 3 (TS3), register 1263H is used to configure timeslot 4 (TS4).

All Reserved bits must be set to their default values for proper operation.

TSx_PROV

TSx_PROV suppresses the flow of data through the SIRP for timeslot X. For proper operation of the S/UNI-MULTI-48, TSx_PROV must be set to 1 for all master timeslots. TSx_PROV should be set to logic 0 for slave timeslots. See Operation Section for more details on how to define which timeslots to provision.

TSx_ERDI

The TSx_ERDI bit selects between normal and extended RDI encoding. When TSx_ERDI is set high, extended RDI (ERDI-P) is selected. When TSx_ERDI is set low, normal RDI-P is selected. These selections are summarized in Table 20.

Table 20 SIRP RDI Settings

	ERDI Code	ERDI Interpretation
TSx_ERDI = 1	001	No ERDI-P defect
	010	ERDI-P payload defect
	101	ERDI-P server defect
	110	ERDI-P connectivity defect
TSx_ERDI = 0	000	No RDI-P defect
	000	No RDI-P defect
	100	RDI-P defect
	100	RDI-P defect

TSx_RDI20F

The TSx_RDI20F bits specify the configuration of RDI maintenance duration. The standard required duration is 10 frames. The GR-253 objective duration is 20 frames. The two options are specified by the TSx_RDI20F bit are selected as shown in Table 21.

Table 21 SIRP RDI Maintenance

TSx_RDI20F	Configuration
0	A particular RDI value for will be maintained for the required 10 frames before changing to a lower priority RDI code.
1	A particular RDI value for will be maintained for the GR-253 objective 20 frames before changing to a lower priority RDI code.

Register 126CH 166CH 1A6CH 1E6CH: SIRP Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	RDIPRIHI[1]	0
Bit 4	R/W	RDIPRIHI[0]	0
Bit 3	R/W	RDIPRIMID[1]	0
Bit 2	R/W	RDIPRIMID[0]	0
Bit 1	R/W	LCD[1]	1
Bit 0	R/W	LCD[0]	0

LCD[1:0]

The LCD[1:0] bits represent the top two bits of the RDI code generated when a Loss of ATM Cell Delineation (LCD) event is detected. The third bit (LSB) is the inverse of the second (LCD[0]). **To conform to Telcordia and ITU SONET/SDH standards, this register field must be set to 01 (note the default is 10).**

RDIPRIMID[1:0]

The RDIPRIMID[1:0] bits specify which two-bit alarm code point (RDI) will be treated as the second highest priority code. These bits combined with the RDIPRIHI bits determine the priority scheme. The bits are interpreted as shown in RDIPRIHI[1:0]. **To comply with Telcordia and ITU SONET/SDH standards this register field must be set to 11**.

RDIPRIHI[1:0]

The RDIPRIHI[1:0] bits specify which two-bit alarm code point (RDI) will be treated as the highest priority code. High priority codes will replace low priority codes at the next transmit G1 byte, instead of allowing 10/20 copies to be sent. The highest priority alarm is sent 10/20 times before replacement is allowed. **To comply with Telcordia and ITU SONET/SDH standards this register field must be set to 10**.

Table 22 SIRP RDI Priority Schemes

RDIPRIHI[1:0]	RDIPRIMID[1:0]	Priority of Codes (3 = Highest)	
		Code	Priority

RDIPRIHI[1:0]	RDIPRIMID[1:0]	Priority of Codes (3 = Highest)	
		Code	Priority
11	01	110	3
		010	2
		101	1
		001	0
11	10	110	3
		101	2
		010	1
		001	0
10	11	101	3
		110	2
		010	1
		001	0
10	01	101	3
		010	2
		110	1
		001	0
01	11	010	3
		110	2
		101	1
		001	0
01	10	010	3
		101	2
		110	1
		001	0
00	00	110	1
		101	1
		010	1
		001	0
Other codes	other codes	Reserved	

Notes:

- When RDIPRIHI[1:0] and RDIPRIMID[1:0] are both equal to b'00, all RDI codes have equal priority except RDI[1:0] = b'00 which always has lowest priority.
- The above table only affects the relationship between the configured LCD value and whatever in-band RDI is provided by the SARC/RHPP in the Protect device. For example, the priority of any Server Defect cannot be made lower than a Connectivity Defect by changing these register values.

Register 1280H 1680H 1A80H 1E80H: T8TE APS Control and Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	FIFOERRE	0
Bit 3	R/W	TPINS	0
Bit 2	R/W	Reserved	0
Bit 1	W	CENTER	0
Bit 0	R/W	DLCV	0

The Reserved bit must be set to its default value for proper operation.

DLCV

The diagnose line code violation bit (DLCV) controls the insertion of line code violation in the APS outgoing serial data. When DLCV is set high, the encoded data is continuously inverted to generate line code violations. The inverted data will represent both valid and invalid 8B/10B characters as not all 8B/10B characters have positive running disparity and negative running disparity characters simply the inverse of each other. Note that Serial-TelecomBus control characters are not affected by the DLCV bit and are passed unaltered.

CENTER

The FIFO centering control bit (CENTER) controls the separation of the FIFO read and write pointers. CENTER is a self-clearing write only bit. When a logic high is written to CENTER, and the current FIFO depth is not in the range of 3, 4 or 5 characters, the FIFO depth is forced to be four 8B/10B characters deep with a momentary data corruption. Writing to the CENTER bit when the FIFO depth is in the 3, 4 or 5 character range produces no effect. CENTER always returns a logic low when read.

The FIFO should be centered whenever any of the following actions are taken: (1) the chip is reset/powered on, (2) APS CSU is reset, (3) APS is reset or (4) the position of APSIFP (or its internal delay towards APSOFP) changes.

For proper operation, the T8TEs' CENTER bit must be set to logic 1 after the APS CSU is locked. This is the only way to guarantee that all transmit FIFO depths are within 1 or 2 clock cycles of each other. This is required for J0 alignment at the far end.

Note that, when using the APSOFP output of the S/UNI MULTI-48 externally, all 4 T8TE FIFOs should be centered, regardless of the usage of their associated link.

TPINS

The Test Pattern Insertion (TPINS) controls the insertion of test pattern in the outgoing data stream for jitter testing purpose. When this bit is set high, the test pattern stored in the registers (TP[9:0]) is used to replace all the overhead and payload bytes of the output data stream. When TPINS is set low, no test patterns are generated.

FIFOERRE

The FIFO overrun/underrun error interrupt enable bit (FIFOERRE) controls the FIFO overrun interrupt event. An interrupt is generated on a FIFO error event if the FIFOERRE is set to logic 1. No interrupt is generated if FIFOERRE if is set to logic 0.

Reserved

Reserved should be kept at its default value.

Register 1281H 1681H 1A81H 1E81H: T8TE APS Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R	FIFOERRI	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

FIFOERRI

The FIFO overrun/underrun error interrupt indication bit (FIFOERRI) reports a FIFO overrun/underrun error event. FIFO overrun/underrun errors occur when FIFO logic detects FIFO read and write pointers in close proximity to each other. FIFOERRI is set to logic 1 on a FIFO overrun/underrun error. This bit does not cause a hardware interrupt on INTB unless the FIFOERRE bit is set high. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

Register 1282H 1682H 1A82H 1E82H: T8TE APS TelecomBus Mode #1

Bit	Type	Function	Default
Bit 15	R/W	TMODE7[1]	0
Bit 14	R/W	TMODE7[0]	0
Bit 13	R/W	TMODE6[1]	0
Bit 12	R/W	TMODE6[0]	0
Bit 11	R/W	TMODE5[1]	0
Bit 10	R/W	TMODE5[0]	0
Bit 9	R/W	TMODE4[1]	0
Bit 8	R/W	TMODE4[0]	0
Bit 7	R/W	TMODE3[1]	0
Bit 6	R/W	TMODE3[0]	0
Bit 5	R/W	TMODE2[1]	0
Bit 4	R/W	TMODE2[0]	0
Bit 3	R/W	TMODE1[1]	0
Bit 2	R/W	TMODE1[0]	0
Bit 1	R/W	TMODE0[1]	0
Bit 0	R/W	TMODE0[0]	0

Register 1283H 1683H 1A83H 1E83H: T8TE APS TelecomBus Mode #2

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	TMODE11[1]	0
Bit 6	R/W	TMODE11[0]	0
Bit 5	R/W	TMODE10[1]	0
Bit 4	R/W	TMODE10[0]	0
Bit 3	R/W	TMODE9[1]	0
Bit 2	R/W	TMODE9[0]	0
Bit 1	R/W	TMODE8[1]	0
Bit 0	R/W	TMODE8[0]	0

TMODE0[1:0]-TMODE11[1:0]

The TelecomBus mode registers (TMODE0[1:0]-TMODE11[1:0]) contain TelecomBus mode settings for each STS-1 timeslot in the STS-12 stream. **All STS-1 timeslots in all streams must work in the same mode**. A S/UNI MULTI-48 configured to use its APS ports **must** have HPT mode enabled.

The setting stored in TMODE**x**[1:0] (**x** can be 0-11) determines which set of TelecomBus control signals are to be encoded in 8B/10B characters. Table 23 defines the values for setting each mode.

Table 23 TelecomBus Mode

TMODEx[1:0]	Functional Description
00	MST Mode
01	HPT Mode
10, 11	Reserved

Register 1284H 1684H 1A84H 1E84H: T8TE APS Test Pattern

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R/W	TP[9]	1
Bit 8	R/W	TP[8]	0
Bit 7	R/W	TP[7]	1
Bit 6	R/W	TP[6]	0
Bit 5	R/W	TP[5]	1
Bit 4	R/W	TP[4]	0
Bit 3	R/W	TP[3]	1
Bit 2	R/W	TP[2]	0
Bit 1	R/W	TP[1]	1
Bit 0	R/W	TP[0]	0

TP[9:0]

The Test Pattern registers (TP[9:0]) contain the test pattern that is used to insert into the outgoing data stream for jitter test purpose. When the TPINS bit is set high, the test pattern stored in TP[9:0] is used to replace all the overhead and payload bytes of the output data stream.

Register 1285H 1685H 1A85H 1E85H: T8TE APS Analog Control

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	TXLV_ENB	0
Bit 7	R/W	APISO_ENB	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	1
Bit 1	R/W	Reserved	1
Bit 0	R/W	ARSTB	1

All Reserved bits must be set to their default values for proper operation.

ARSTB

The analog reset bit (ARSTB) controls the TXLV and APISO operation. When ARSTB is set low, the TXLV and APISO are reset. This bit must be set to logic 1 for normal operation. When used, ARSTB should be asserted for at least 100 ns to reset circuitry properly.

APISO_ENB

The APISO enable bit (APISO_ENB) controls the APISO operation. When set to logic 1, APISO_ENB disables the APISO. When set to logic 0, APISO_ENB enables the APISO.

TXLV_ENB

The TXLV enable bit (TXLV_ENB) controls the TXLV operation. When set to logic 1, TXLV_ENB disables the TXLV. When set to logic 0, TXLV_ENB enables the TXLV.

Register 1286H 1686H 1A86H 1E86H: T8TE APS DTB Bus

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

This register controls internal analog functions. This register should not be used and should be left in its default state.

Register 12A0H: TDLL Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	—	Unused	X
Bit 2	R/W	ERRORE	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

The TDLL Configuration Register controls the basic operation of the Transmit UL3/PL3 DLL. It is not necessary to setup this register for normal operation.

ERRORE

The ERROR interrupt enable (ERRORE) bit enables the error indication interrupt. When ERRORE is set high, an interrupt is generated upon assertion event of the ERR output and ERROR register. When ERRORE is set low, changes in the ERROR and ERR status do not generate an interrupt.

Register 12A1H: TDLL Reserved #1

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

This register controls internal functions. This register should not be used and should be left in its default state.

Register 12A2H: TDLL Reserved #2

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

This register controls internal functions. This register should not be used and should be left in its default state.

Register 12A3H: TDLL Control Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	TFCLKI	X
Bit 6	R	Reserved	X
Bit 5	R	ERRORI	X
Bit 4	R	Reserved	X
Bit 3	—	Unused	X
Bit 2	R	ERROR	X
Bit 1	R	Reserved	0
Bit 0	R	RUN	0

The TDLL Control Status Register provides information of the DLL operation.

RUN

The DLL lock status register bit (RUN) indicates the DLL found a delay line tap in which the phase difference between the rising edge of the feedback clock and the rising edge of TFCLK is zero. After system reset, RUN is logic zero until the phase detector indicates an initial lock condition. When the phase detector indicates lock, RUN is set to logic 1.

The RUN register bit is cleared only by a system reset or a software reset.

ERROR

The delay line error register bit (ERROR) indicates the DLL has run out of dynamic range. When the DLL attempts to move beyond the end of the delay line, ERROR is set high. When ERROR is high, the DLL cannot generate a DLLCLK phase which causes the rising edge of the feedback clock to be aligned to the rising edge of TFCLK. ERROR is set low, when the DLL captures lock again.

ERRORI

The delay line error event register bit (ERRORI) indicates the ERROR register bit has gone high. When the ERROR register changes from a logic zero to a logic one, the ERRORI register bit is set to logic one. If the ERRORE interrupt enable is high, the INT output is also asserted when ERRORI asserts.

When WCIMODE is low, the ERRORI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded. When WCIMODE is high, the ERRORI register bit is cleared immediately after a logic one is written to the ERRORI register, thus acknowledging the event has been recorded.

TFCLKI

The system clock event register bit TFLCKI provides a method to monitor activity on the system clock. When the TFCLK primary input changes from a logic zero to a logic one, the TFCLKI register bit is set to logic one.

When WCIMODE is low, the TFCLKI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded. When WCIMODE is high, the TFCLKI register bit is cleared immediately after a logic one is written to the TFCLKI register, thus acknowledging the event has been recorded.

Register 1300H: TSTSI Control Page Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	R/W	PAGE	0
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	TSOUT[3]	0
Bit 6	R/W	TSOUT[2]	0
Bit 5	R/W	TSOUT[1]	0
Bit 4	R/W	TSOUT[0]	0
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R/W	DOUTSEL[1]	0
Bit 0	R/W	DOUTSEL[0]	0

This register provides the data stream number; the time-slot number and the control page select used to access the control pages. Writing to this register triggers an indirect register access. This register cannot be written to when an indirect register access is in progress.

DOUTSEL[1:0]

The Data Output Select (DOUTSEL[1:0]) bits select the output data stream accessed by the current indirect transfer.

DOUTSEL[1:0]	DOUT
00	DOUT #1
01	DOUT #2
10	DOUT #3
11	DOUT #4

TSOUT[3:0]

The indirect STS-1/STM-0 output time slot (TSOUT[3:0]) bits indicate the STS-1/STM-0 output time slot accessed in the current indirect access.

TSOUT[3:0]	STS-1/STM-0 time slot #
0000	Invalid time slot
0001-1100	Time slot #1 to time slot #12
1101-1111	Invalid time slot

PAGE

The page (PAGE) bit selects which control page is accessed in the current indirect transfer. Two pages are defined: page 0 and page 1.

PAGE	Control Page
0	Page 0
1	Page 1

RWB

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the control pages. Writing logic 0 to RWB triggers an indirect write operation. Data to be written is taken for the TSTSI Indirect Data register. Writing logic 1 to RWB triggers an indirect read operation. The data read from the control pages is stored in the TSTSI Indirect Data register after the BUSY bit has cleared.

BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set to logic 1 when this register is written, triggering an access. It remains logic 1 until the access is complete at which time it is set to logic 0. This register should be polled to determine when new data is available in the Indirect Data Register or when another write access can be initiated.

Register 1301H: TSTSI Control Page Indirect Data

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R/W	COC	0
Bit 12	R/W	COD	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	CO[10]	0
Bit 9	R/W	CO[9]	0
Bit 8	R/W	CO[8]	0
Bit 7	R/W	TSIN[3]/CO[7]	0
Bit 6	R/W	TSIN[2]/CO[6]	0
Bit 5	R/W	TSIN[1]/CO[5]	0
Bit 4	R/W	TSIN[0]/CO[4]	0 (see Note)
Bit 3	R/W	CO[3]	0
Bit 2	R/W	CO[2]	0
Bit 1	R/W	DINSEL[1]/CO[1]	0
Bit 0	R/W	DINSEL[0]/CO[0]	0

This register contains the data read from the control pages after an indirect read operation or the data to be written to the control pages in an indirect write operation. The data to be written to the control pages must be set up in this register before triggering a write. The TSTSI Indirect Data register reflects the last value read or written until the completion of a subsequent indirect read operation. This register cannot be written to while an indirect register access is in progress.

Note: Default value is logic 0 when reading this register directly, and logic 1 when reading this register using an indirect access.

DINSEL[1:0]

The Data Input Select (DINSEL[1:0]) field reports the data stream number read from or written to an indirect register location. DINSEL[1:0] also doubles as CO[1:0]

DINSEL[1:0]	Data Stream
00	DIN1
01	DIN2
10	DIN3
11	DIN4

TSIN[3:0]

The STS-1/STM-0 Input Time Slot (TSIN[3:0]) field reports the time-slot number read from or written to an indirect register location. TSIN[3:0] also doubles as CO[7:4].

TSIN[3:0]	STS-1/STM-0 time slot #
0000	Invalid time slot
0001-1100	Time slot #1 to time slot #12
1101-1111	Invalid time slot

COD

The Character Overwrite Data (COD) bit reports the value of the COD bit read from or written to an indirect register location. The value of the COD bit controls the source of the data bits (DOUT[7:0]) that the muxing block outputs. When it is set to logic 0 the muxing block samples and reorders the holding buffers. When it is set to logic 1 then muxing block directly outputs the character overwrite data (CO[7:0].

COC

The Character Overwrite Control (COC) bit reports the value of the COC bit read from or written to an indirect register location. The value of the COC bit controls the source of the control bits (DOUT[10:8]) that the muxing block outputs. When it is set to logic 0 the muxing block samples and reorders the holding buffers. When it is set to logic 1 then muxing block directly outputs the character overwrite control bits (CO[10:8]).

CO[10:0]

The Character Overwrite (CO[10:0]) bits reports the character overwrite data read from or written to an indirect register location. The interpretation of the character overwrite data bits is altered depending on the value of the COC and COD bits.

Register 1302H: TSTSI Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R	ACTIVE	X
Bit 2	R/W	PSEL	0
Bit 1	R/W	J0RORDR	0
Bit 0	R/W	COAPE	0

COAPE

The change of active page interrupt enable (COAPE) bit enables/disables the change of active page interrupt output (INT). When the COAPE bit is set to logic 1, an interrupt is generated when the active page changes from page 0 to page 1 or from page 1 to page 0. These interrupts are masked when COAPE is set to logic 0.

J0RORDR

The J0 Reorder (J0RORDR) bit enables/disables the reordering of the J0/Z0 bytes. This configuration bit only has an effect when the TSTSI is in the dynamic switching mode – if the TSTSI is in any of the static switching modes then the value of this bit is ignored. When this bit is set to logic 0 the J0/Z0 bytes are not reordered by the muxing block. When this bit is set to logic 1, normal reordering of the J0/Z0 bytes is enabled.

PSEL

The page select (PSEL) bit is used in the selection of the current active page. This bit is logically XORed with the value of the external CPS signal to determine which control page is currently active.

ACTIVE

The active page indication (ACTIVE) bit indicates which control page is currently active. When this bit is logic 0 then page 0 is controlling the dynamic mux. When this bit is logic 1 then page 1 is controlling the dynamic mux.

Register 1303H: TSTSI Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R	COAPI	X

COAPI

The change of active page interrupt statue bit (COAPI) reports the status of the change of active page interrupt. COAPI is set to logic 1 when the active control page changes from page 0 to page 1 or from page 1 to page 0. COAPI is cleared immediately following a read to this register when WCIMODE is logic 0. When WCIMODE is logic 1, COAPI is cleared immediately following a write (regardless of value) to this register. COAPI remains valid when the interrupt is not enabled (COAPE set to logic 0) and may be polled to detect change of active control page events.

Register 1310H 1710H 1B10H 1F10H: TCFP Configuration

Bit	Type	Function	Default
Bit 15	R/W	FIFO_ERRE	0
Bit 14	R/W	FIFO_UDRE	0
Bit 13	R/W	XFERE	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	DELINDIS	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	POS_SEL	0
Bit 7	R/W	CRC_SEL[1]	1
Bit 6	R/W	CRC_SEL[0]	1
Bit 5	R/W	FLAG[3]	0
Bit 4	R/W	FLAG[2]	0
Bit 3	R/W	FLAG[1]	0
Bit 2	R/W	FLAG[0]	0
Bit 1	R/W	SCRMBL	1
Bit 0	R/W	PROV	0

PROV

The processor provision bit (PROV) is used to enable the TCFP. When PROV is logic 0, the TCFP ATM and packet processors are disabled and will not request data from the TXSDQ FIFO interface and will respond to data requests with all 1's data. When PROV is logic 1, the TCFP ATM or packet processor is enabled and will respond to data requests with valid data after requesting and processing data from the TXSDQ FIFO interface.

SCRMBL

The SCRMBL bit controls the scrambling of the packet data stream or ATM cell payload. When SCRMBL is a logic 1, scrambling is enabled. When SCRMBL is a logic 0, scrambling is disabled.

FLAG[3:0]

The flag insertion control (FLAG[3:0]) configures the minimum number of flag bytes the packet processor inserts between packets. The minimum number of flags (01111110) inserted between packets is shown in the table below. FLAG[3:0] are used only in POS mode.

Table 24 Selection of the number of Flag Bytes

FLAG[3:0]	Minimum Number of FLAG Bytes
0000	1 flag
0001	2 flags

FLAG[3:0]	Minimum Number of FLAG Bytes
0010	4 flags
0011	8 flags
0100	16 flags
0101	32 flags
0110	64 flags
0111	128 flags
1000	256 flags
1001	512 flags
1010	1024 flags
1011	2048 flags
1100	4096 flags
1101	8192 flags
1110	16384 flags
1111	32768 flags

CRC_SEL[1:0]

The CRC select (CRC_SEL[1:0]) bits allow the control of the CRC calculation according to the table below. For ATM cells, the CRC is calculated over the first four ATM header bytes. For packet applications, the CRC is calculated over the whole packet data, before byte stuffing and scrambling.

Table 25 CRC Mode Selection

CRC_SEL[1:0]	HCS Operation	FCS Operation
00	Reserved	No FCS inserted
01	Reserved	No FCS inserted
10	CRC-8 without coset polynomial	CRC-CCITT (2 bytes)
11	CRC-8 with coset polynomial added	CRC-32 (4 bytes)

POS_SEL

The POS_SEL bit enables the POS HDLC frame processing mode. When POS_SEL is set to logic 1, POS processing will occur. When POS_SEL is set to logic 0, ATM mode is selected.

Reserved

The Reserved bits should be set to logic 0 for proper operation.

DELINDIS

The DELINDIS bit can be used to disable HDLC flag alignment and byte stuffing. All payload data written to the POS-PHY Level 3 interface is passed directly to the TelecomBus Interface. DELINDIS is only valid in POS mode.

This bit should only be set when Transparent Data Mode is desired. In this mode, data is passed directly from the POS-PHY Level 3 Bus to the TelecomBus payload without flag insertion, byte stuffing or CRC generation. Use of Transparent mode requires the use of 64 byte packets, and the FIFO must not be allowed to under-run since no flags are available to fill excess bandwidth. In addition, the CRC_SEL bits must be set to "00".

XFERE

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the transmitted packet/cell counter, transmitted byte counter, and aborted packet counter holding registers. When XFERE is set to logic 1, the interrupt is enabled.

FIFO_UDRE

The FIFO_UDRE bit enables the generation of an interrupt due to a FIFO underrun. When FIFO_UDRE is set to logic 1, the interrupt is enabled the signal INT will be set to logic 1 whenever FIFO_UNRI is set to logic 1.

FIFO_ERRE

The FIFO_ERRE bit enables the generation of an interrupt due to a FIFO error. When FIFO_ERRE is set to logic 1, the interrupt is enabled and the signal INT will be set to logic 1 whenever FIFO_ERRI is set to logic 1.

Register 1311H 1711H 1B11H 1F11H: TCFP Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	FIFO_ERRI	X
Bit 14	R	FIFO_UDRI	X
Bit 13	R	XFERI	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

XFERI

The XFERI bit indicates that a transfer of accumulated counter data has occurred. A logic 1 in this bit position indicates that the transmitted cell/packet counter, transmitted byte counter, and aborted packet counter holding registers have been updated. This update is initiated by writing to one of the TCFP counter register locations, or initiating a global performance monitor update by writing to register 0002H. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read.

FIFO_UDRI

The FIFO_UDRI bit is logic 1 when an attempt is made to read from the FIFO while it is empty. This is considered a system error.

When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read.

FIFO_ERRI

This bit is set to one when an error is detected on the read side of the FIFO. This error can be caused by an abnormal sequence of TSOP and TEOP signals or the assertion of FIFO_ERR. This assertion can normally be caused by a previous FIFO overrun condition or a user asserted error from the POS-PHY L3 interface.

When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read.

Register 1312H 1712H 1B12H 1F12H: TCFP Idle/Unassigned ATM Cell Header

Bit	Type	Function	Default
Bit 15	R/W	GFC[3]	0
Bit 14	R/W	GFC[2]	0
Bit 13	R/W	GFC[1]	0
Bit 12	R/W	GFC[0]	0
Bit 11	R/W	PTI[2]	0
Bit 10	R/W	PTI[1]	0
Bit 9	R/W	PTI[0]	0
Bit 8	R/W	CLP	1
Bit 7	R/W	PAYLD[7]	0
Bit 6	R/W	PAYLD[6]	1
Bit 5	R/W	PAYLD[5]	1
Bit 4	R/W	PAYLD[4]	0
Bit 3	R/W	PAYLD[3]	1
Bit 2	R/W	PAYLD[2]	0
Bit 1	R/W	PAYLD[1]	1
Bit 0	R/W	PAYLD[0]	0

PAYLD[7:0]

The PAYLD[7:0] (Idle Cell Payload) value reflects the payload bytes which will be inserted into the ATM Idle cell generated by the TCFP.

CLP

The CLP (Cell Loss Priority) bit contains the eighth bit position of the fourth octet of the idle/unassigned cell pattern. Cell rate decoupling is accomplished by transmitting idle cells when the TCFP detects that no outstanding cells are available from the external FIFO and data is requested on the TCFP egress interface. Additionally, XOFF can be used to force the transmission of Idle/Unassigned cells in ATM mode.

PTI[2:0]

The PTI[2:0] (Payload Type) bits contain the fifth, sixth, and seventh bit positions of the fourth octet of the idle/unassigned cell pattern. Idle cells are transmitted when the TCFP detects that no outstanding cells are available from the external FIFO and data is requested on the TCFP egress interface. Additionally, XOFF can be used to force the transmission of Idle/Unassigned cells in ATM mode.

GFC[3:0]

The GFC[3:0] (Generic Flow Control) bits contain the first, second, third, and fourth bit positions of the first octet of the idle/unassigned cell pattern. Idle/unassigned cells are transmitted when the TCFP detects that no outstanding cells are available from the external FIFO and data is requested on the TCFP egress interface. Additionally, XOFF can be used to force the transmission of Idle/Unassigned cells in ATM mode. The all zeros pattern is transmitted in the VCI and VPI fields of the idle/unassigned cell.

Register 1313H 1713H 1B13H 1F13H: TCFP Diagnostics

Bit	Type	Function	Default
Bit 15	R/W	DCRC[7]	0
Bit 14	R/W	DCRC[6]	0
Bit 13	R/W	DCRC[5]	0
Bit 12	R/W	DCRC[4]	0
Bit 11	R/W	DCRC[3]	0
Bit 10	R/W	DCRC[2]	0
Bit 9	R/W	DCRC[1]	0
Bit 8	R/W	DCRC[0]	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	TX_BYTE_MODE	0
Bit 4	R/W	XOFF	0
Bit 3	R/W	INVERT	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

Reserved

The Reserved bits should be set to their default values for proper operation.

INVERT

The data inversion bit (INVERT) configures the ATM or packet processor to logically invert the outgoing data stream. When INVERT is set to logic 1, the outgoing data stream is logically inverted. The outgoing data stream is not inverted when INVERT is set to logic 0.

XOFF

The XOFF serves as a transmission enable bit. When XOFF is set to logic 0, ATM cells or packets are transmitted normally. When XOFF is set to logic 1, the cell or packet currently being transmitted is completed and then transmission is suspended. When XOFF is set to logic 1, the TCFP will stop requesting data from the TXSDQ and ATM Idle cells or HDLC flags will be sent on the TCFP egress interface. Note that while XOFF is set to logic 1, byte and packet counters may reflect bytes held in the TCFP's internal FIFO that have not yet been transmitted

TX_BYTE_MODE

The transmit byte counter mode (TX_BYTE_MODE) bit is used to select the mode in which the TX_BYTE[39:0] counters work. When TX_BYTE_MODE is logic 0, TX_BYTE[39:0] will count all bytes in transmitted packets (including FCS and Abort bytes) before the byte stuffing operation. When TX_BYTE_MODE is logic 1, TX_BYTE[39:0] will count all bytes in transmitted packets (including FCS, Abort, and stuff bytes) after the byte stuffing operation. Flag bytes will not be counted in either case. The TX_BYTE_MODE bit is only valid when working in POS mode.

DCRC[7:0]

The diagnostic CRC word (DCRC[7:0]) configures the ATM or packet processor to logically invert bits in the inserted CRC on the outgoing data stream for diagnostic purposes. When any bit in DCRC[7:0] is set to logic 1, the corresponding bit in the FCS value inserted by the POS processor or the HCS value inserted by the ATM processor is logically inverted. DCRC[7:0] is ignored when no FCS is inserted. Each DCRC[x] bit will cause a bit error in each byte of the 2 byte or 4 byte FCS.

Register 1314H 1714H 1B14H 1F14H: TCFP Transmit Cell/Packet Counter (LSB)

Bit	Type	Function	Default
Bit 15	R	TX_CELL[15]	X
Bit 14	R	TX_CELL[14]	X
Bit 13	R	TX_CELL[13]	X
Bit 12	R	TX_CELL[12]	X
Bit 11	R	TX_CELL[11]	X
Bit 10	R	TX_CELL[10]	X
Bit 9	R	TX_CELL[9]	X
Bit 8	R	TX_CELL[8]	X
Bit 7	R	TX_CELL[7]	X
Bit 6	R	TX_CELL[6]	X
Bit 5	R	TX_CELL[5]	X
Bit 4	R	TX_CELL[4]	X
Bit 3	R	TX_CELL[3]	X
Bit 2	R	TX_CELL[2]	X
Bit 1	R	TX_CELL[1]	X
Bit 0	R	TX_CELL[0]	X

Register 1315H 1715H 1B15H 1F15H: TCFP Transmit Cell/Packet Counter (MSB)

Bit	Type	Function	Default
Bit 15	R	TX_CELL[31]	X
Bit 14	R	TX_CELL[30]	X
Bit 13	R	TX_CELL[29]	X
Bit 12	R	TX_CELL[28]	X
Bit 11	R	TX_CELL[27]	X
Bit 10	R	TX_CELL[26]	X
Bit 9	R	TX_CELL[25]	X
Bit 8	R	TX_CELL[24]	X
Bit 7	R	TX_CELL[23]	X
Bit 6	R	TX_CELL[22]	X
Bit 5	R	TX_CELL[21]	X
Bit 4	R	TX_CELL[20]	X
Bit 3	R	TX_CELL[19]	X
Bit 2	R	TX_CELL[18]	X
Bit 1	R	TX_CELL[17]	X
Bit 0	R	TX_CELL[16]	X

TX_CELL[31:0]

The TX_CELL[31:0] bits indicate the number of cells or **non-aborted** packets transmitted to the TCFP egress stream during the last accumulation interval. ATM Idle cells, HDLC flags, and HDLC Abort bytes inserted into the transmission stream are not counted.

A write to any one of the TCFP counter registers loads all the corresponding TCFP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0002H can be written to initiate a global performance counter update across the S/UNI MULTI-48.

Register 1316H 1716H 1B16H 1F16H: TCFP Transmit Byte Counter (LSB)

Bit	Type	Function	Default
Bit 15	R	TX_BYTE[15]	X
Bit 14	R	TX_BYTE [14]	X
Bit 13	R	TX_BYTE [13]	X
Bit 12	R	TX_BYTE [12]	X
Bit 11	R	TX_BYTE [11]	X
Bit 10	R	TX_BYTE [10]	X
Bit 9	R	TX_BYTE [9]	X
Bit 8	R	TX_BYTE [8]	X
Bit 7	R	TX_BYTE [7]	X
Bit 6	R	TX_BYTE [6]	X
Bit 5	R	TX_BYTE [5]	X
Bit 4	R	TX_BYTE [4]	X
Bit 3	R	TX_BYTE [3]	X
Bit 2	R	TX_BYTE [2]	X
Bit 1	R	TX_BYTE [1]	X
Bit 0	R	TX_BYTE [0]	X

Register 1317H 1717H 1B17H 1F17H: TCFP Transmit Byte Counter

Bit	Type	Function	Default
Bit 15	R	TX_ BYTE [31]	X
Bit 14	R	TX_ BYTE [30]	X
Bit 13	R	TX_ BYTE [29]	X
Bit 12	R	TX_ BYTE [28]	X
Bit 11	R	TX_ BYTE [27]	X
Bit 10	R	TX_ BYTE [26]	X
Bit 9	R	TX_ BYTE [25]	X
Bit 8	R	TX_ BYTE [24]	X
Bit 7	R	TX_ BYTE [23]	X
Bit 6	R	TX_ BYTE [22]	X
Bit 5	R	TX_ BYTE [21]	X
Bit 4	R	TX_ BYTE [20]	X
Bit 3	R	TX_ BYTE [19]	X
Bit 2	R	TX_ BYTE [18]	X
Bit 1	R	TX_ BYTE [17]	X
Bit 0	R	TX_ BYTE [16]	X

Register 1318H 1718H 1B18H 1F18H: TCFP Transmit Byte Counter (MSB)

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	TX_ BYTE [39]	X
Bit 6	R	TX_ BYTE [38]	X
Bit 5	R	TX_ BYTE [37]	X
Bit 4	R	TX_ BYTE [36]	X
Bit 3	R	TX_ BYTE [35]	X
Bit 2	R	TX_ BYTE [34]	X
Bit 1	R	TX_ BYTE [33]	X
Bit 0	R	TX_ BYTE [32]	X

TX_BYTE[39:0]

The TX_ BYTE[39:0] bits indicate the number of bytes in packets transmitted to the TCFP egress stream during the last accumulation interval. The byte counts include all user payload bytes, FCS bytes, and abort bytes. Inclusion of stuffed bytes is controlled by the TX_BYTE_MODE register bit. HDLC flags and Idle characters are not counted. The TX_BYTE[39:0] counters are only valid when processing packets.

A direct write to any one of the TCFP counter registers loads all the corresponding TCFP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0002H can be written to initiate a global performance counter update across the S/UNI®-MULTI-48.

Register 1319H 1719H 1B19H 1F19H: TCFP Aborted Packet Counter

Bit	Type	Function	Default
Bit 15	R	TX_ABT[15]	X
Bit 14	R	TX_ABT[14]	X
Bit 13	R	TX_ABT[13]	X
Bit 12	R	TX_ABT[12]	X
Bit 11	R	TX_ABT[11]	X
Bit 10	R	TX_ABT[10]	X
Bit 9	R	TX_ABT[9]	X
Bit 8	R	TX_ABT[8]	X
Bit 7	R	TX_ABT[7]	X
Bit 6	R	TX_ABT[6]	X
Bit 5	R	TX_ABT[5]	X
Bit 4	R	TX_ABT[4]	X
Bit 3	R	TX_ABT[3]	X
Bit 2	R	TX_ABT[2]	X
Bit 1	R	TX_ABT[1]	X
Bit 0	R	TX_ABT[0]	X

TX_ABT[15:0]

The TX_ ABT[15:0] bits indicate the number aborted packets transmitted to the TCFP egress stream during the last accumulation interval. These counters are only valid when processing packets.

A write to any one of the TCFP counter registers loads all the corresponding TCFP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0002H can be written to initiate a global performance counter update across the S/UNI MULTI-48.

Register 1320H: TXSDQ FIFO Reset

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R	TXSDQTIP	X
Bit 0	R/W	SDQRST	1

SDQRST

This bit is used to reset the TXSDQ. The TXSDQ comes up in reset. It should be taken out of reset by writing a 0 to this bit. The user can reset the TXSDQ at any time by writing a 1 to this bit, and then writing a 0. Reset flushes all the data in the FIFOs, resets the read and write pointers and resets all counters. The configuration information is not changed by Reset.

TXSDQTIP

The TXSDQTIP bit indicates that the TXSDQ counters are in the process of being transferred to their holding registers. A transfer is initialized by writing to the S/UNI MULTI-48 Global Performance Monitor Update register (0002H). TXSDQTIP is logic 1 while a transfer is in progress. It returns to logic 0 when the transfer is completed.

Register 1321H: TXSDQ FIFO Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	SOPE	0
Bit 1	R/W	EOPE	0
Bit 0	R/W	OFLE	0

OFLE

When this bit is set to 1, FIFO overflows cause the INTB output to be asserted. If this bit is set to 0, FIFO overflows do not cause INTB to be asserted.

EOPE

When this bit is set to 1, bad EOP signals cause the INTB output to be asserted. If this bit is set to 0, bad EOP signals do not cause INTB to be asserted.

SOPE

When this bit is set to 1, bad SOP signals cause the INTB output to be asserted. If this bit is set to 0, bad SOP signals do not cause INTB to be asserted.

Reserved

This bit should be set to logic 0 for proper operation.

Register 1323H: TXSDQ FIFO Overflow Port and Interrupt Indication

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R	OFL_FIFO[5]	X
Bit 12	R	OFL_FIFO[4]	X
Bit 11	R	OFL_FIFO[3]	X
Bit 10	R	OFL_FIFO[2]	X
Bit 9	R	OFL_FIFO[1]	X
Bit 8	R	OFL_FIFO[0]	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R	OFLI	X

OFLI

This bit is set when any of the configured FIFOs overflows. The FIFO number that caused this interrupt is available in OFL_FIFO[5:0]. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read. This overflow indication can be set by each byte of a cell or packet that is being written into a full FIFO, so multiple interrupts can be generated for the same cell or packet if the interrupt indication is read too quickly.

OFL_FIFO[5:0]

These bits are used to indicate the FIFO number which overflowed and set the OFLI indication. These bits are valid only when OFLI is logic 1. If multiple FIFOs overflow before this interrupt is serviced, OFL_FIFO[5:0] will indicate the FIFO that first overflowed (see section 13.28 on how FIFO number and PL3/UL3 channels are mapped).

Register 1324H: TXSDQ FIFO EOP Error Port and Interrupt Indication

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R	EOP_FIFO[5]	X
Bit 12	R	EOP_FIFO[4]	X
Bit 11	R	EOP_FIFO[3]	X
Bit 10	R	EOP_FIFO[2]	X
Bit 9	R	EOP_FIFO[1]	X
Bit 8	R	EOP_FIFO[0]	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R	EOPI	X

EOPI

This bit is set when two EOPs arrive consecutively on the same FIFO without being separated by a SOP. The FIFO number that caused the interrupt is available in EOP_FIFO[5:0]. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read.

EOP_FIFO[5:0]

These bits are used to indicate the FIFO which observed a bad EOP sequence and set the EOPI indication. These bits are valid only when EOPI is logic 1. If multiple bad EOP sequences occur before this interrupt is serviced, EOP_FIFO[5:0] will indicate the FIFO that first observed the bad EOP sequence (see section 13.28 on how FIFO number and PL3/UL3 channels are mapped).

Register 1325H: TXSDQ FIFO SOP Error Port and Interrupt Indication

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R	SOP_FIFO[5]	X
Bit 12	R	SOP_FIFO[4]	X
Bit 11	R	SOP_FIFO[3]	X
Bit 10	R	SOP_FIFO[2]	X
Bit 9	R	SOP_FIFO[1]	X
Bit 8	R	SOP_FIFO[0]	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R	SOPI	X

SOPI

This bit is set when two SOPs arrive consecutively on the same FIFO without being separated by a EOP. The FIFO number that caused the interrupt is available in SOP_FIFO[5:0]. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read.

SOP_FIFO[5:0]

These bits are used to indicate the FIFO which observed a bad SOP sequence and set the SOPI indication. These bits are valid only when SOPI is logic 1. If multiple bad SOP sequences occur before this interrupt is serviced, SOP_FIFO[5:0] will indicate the FIFO that first observed the bad SOP sequence (see section 13.28 on how FIFO number and PL3/UL3 channels are mapped).

Register 1328H: TXSDQ FIFO Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	W	FLUSH	0
Bit 12	R	EMPTY	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	PHYID[5]	0
Bit 4	R/W	PHYID[4]	0
Bit 3	R/W	PHYID[3]	0
Bit 2	R/W	PHYID[2]	0
Bit 1	R/W	PHYID[1]	0
Bit 0	R/W	PHYID[0]	0

This is an indirect register that is used to specify the address of the FIFO that the user is setting up or reading the setup for. This register is the common address used for the four registers including this one: TXSDQ FIFO Indirect Configuration, TXSDQ FIFO Indirect Buffer Available and Data Available Thresholds, and TXSDQ FIFO Indirect Cells and Packets Count. In order to change the current setup of a FIFO, it is recommended that the user reads the existing setup information first, makes any modifications as required, and writes back the information. Note that this read and write-back procedure must be performed for each of the above configuration registers, even if its contents are not changing.

PHYID[5:0]

This is a 6-bit number that is used to describe the current FIFO being addressed by the rest of the FIFO setup registers – the FIFO Indirect Configuration, FIFO Buffer Available Threshold, FIFO Data Available Threshold and FIFO Cells and Packets Count. The range of FIFO numbers that can be used is 0 to 2FH (see section 13.28 on how FIFO number and PL3/UL3 channels are mapped).

EMPTY

This read-only bit indicates if the **requested FIFO** is empty. When this bit is read as 1, the FIFO number specified in PHYID[5:0] in this register is empty. Before reconfiguring a disabled FIFO, this bit needs to be sampled at logic 1 indicating that the FIFO is empty.

FLUSH

This is a write-only bit used to discard all the current data in a specified FIFO. This should typically be used if a non-empty FIFO needs to be reconfigured. If this bit is manually set, it must also be manually cleared before enabling the specified FIFO. Note that this bit can only be set or cleared when RWB = 0 and PHYID is used to select the correct PHY since it is an indirect access bit.

RWB

This bit is used to indicate whether the user is writing the setup of a FIFO, or reading all setup information of a FIFO. This bit is used in conjunction with the BUSY bit. When this bit is set to 1, all the available setup information of the FIFO requested in PHYID[5:0] is available in the registers FIFO Indirect Configuration, FIFO Buffer Available Threshold, FIFO Data Available Threshold and FIFO Cells and Packets Count. When this bit is set to 0, the user is writing the configuration of a FIFO. The TXSDQ latches in the data in the FIFO Indirect Configuration, FIFO Buffer Available Threshold, FIFO Data Available Threshold and FIFO Cells and Packets Count registers.

BUSY

This is a read-only bit is used to indicate to the user that the information requested for the FIFO specified in bits PHYID[5:0] is in the process of being updated. If this bit is sampled to be 1, the update is still in progress. If this bit is sampled 0, the information for the FIFO is now available in the FIFO Indirect Configuration, FIFO Buffer Available Threshold, FIFO Data Available Threshold and FIFO Cells and Packets Count registers.

Register 1329H: TXSDQ FIFO Indirect Configuration

Bit	Type	Function	Default
Bit 15	R/W	ENABLE	0
Bit 14	R/W	POS_SEL	0
Bit 13	R/W	FIFO_NUMBER[5]	0
Bit 12	R/W	FIFO_NUMBER[4]	0
Bit 11	R/W	FIFO_NUMBER[3]	0
Bit 10	R/W	FIFO_NUMBER[2]	0
Bit 9	R/W	FIFO_NUMBER[1]	0
Bit 8	R/W	FIFO_NUMBER[0]	0
Bit 7	R/W	FIFO_BS[1]	0
Bit 6	R/W	FIFO_BS[0]	0
Bit 5	—	Unused	X
Bit 4	R/W	BLOCK_PTR[4]	0
Bit 3	R/W	BLOCK_PTR[3]	0
Bit 2	R/W	BLOCK_PTR[2]	0
Bit 1	R/W	BLOCK_PTR[1]	0
Bit 0	R/W	BLOCK_PTR[0]	0

BLOCK_PTR[4:0]

This is a 5-bit number that is calculated and programmed by the user based on the number of PHYs, the size of each FIFO, and total number of FIFOs required by the system.

FIFO_BS[1:0]

This 2-bit number denotes the size in Blocks of FIFO for the PHYID specified in the FIFO Indirect Address register. The bandwidth is related to the size of the FIFO that will be allocated to the PHY.

FIFO_NUMBER[5:0]

This is a 6-bit internal FIFO number that is used to associate a given PHY ID with a FIFO. This number can be in one of 4 ranges, and is unique for each PHY (see section 13.28 on how FIFO number and PL3/UL3 channels are mapped).

POS_SEL

This bit is set to 1 if the FIFO needs to be configured as a packet FIFO. By default, the FIFOs are configured as ATM cell FIFOs

ENABLE

This bit enables individual FIFOs. Writing a 0 to this bit disables a FIFO. If previously enabled, a disabled FIFO does not accept any new data into it, but continues to assert Data Available internally until it is drained completely. In order to reconfigure FIFOs during operation, they need to be disabled first.

Register 132AH: TXSDQ FIFO Indirect Data and Buffer Available Thresholds

Bit	Type	Function	Default
Bit 15	R/W	DT[7]	0
Bit 14	R/W	DT[6]	0
Bit 13	R/W	DT[5]	0
Bit 12	R/W	DT[4]	0
Bit 11	R/W	DT[3]	0
Bit 10	R/W	DT[2]	0
Bit 9	R/W	DT[1]	1
Bit 8	R/W	DT[0]	1
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R/W	BT[4]	0
Bit 3	R/W	BT[3]	0
Bit 2	R/W	BT[2]	0
Bit 1	R/W	BT[1]	1
Bit 0	R/W	BT[0]	1

This register is used to set the Data and Buffer Available Thresholds for each of the FIFOs.

The Buffer Available Threshold is explained in Section 13.30. The FIFOs need not be enabled to set this threshold. In order to change this value for a FIFO, the user should first disable it, write in the new value, and enable it again.

The Data Available threshold is explained in Section 13.31. The FIFOs need not be enabled to set this threshold. In order to change this value for a FIFO, the user should first disable it, write in the new value, and enable it again.

BT[4:0]

These bits specify the Buffer Available threshold for the FIFO specified in PHYID[5:0] bits in the FIFO Indirect Address register. When this threshold is being set, these bits are written to by the user, and when this threshold is being read, these bits hold the previously configured data. The threshold is equal to BT[4:0] + 1.

This threshold is set in 16 byte Blocks. This threshold can never be greater than the size of the FIFO being configured, and the absolute maximum value is BT[4:0] +1 = 32. This number should be a standard fraction of the FIFO size in blocks. In the case of UL3 ATM FIFOs, this number must be set to a value of BT[4:0] = 3 since ATM cells are 4 blocks in size. PL3 FIFOs may follow the guidelines described in section 13.31.

DT[7:0]

These bits specify the Data Available threshold for the FIFO selected by the FIFO Indirect Address register PHYID[5:0] bits. When this threshold is being set, these bits are written to by the user, and when this threshold is being read, these bits hold the previously configured data. The threshold is equal to DT[7:0] + 1.

This threshold is set in 16 byte Blocks. This threshold can never be greater than the size of the FIFO being configured, and the absolute maximum value is DT[7:0] +1 = 192. This number should be a standard fraction of the FIFO size in blocks. In the case of ATM FIFOs, this number must be set to a value of DT[7:0] = 3 (ATM cells are 4 Blocks long).

The DT[7:0] threshold sets the level at which the cell/packet processors (TCFP s) blocks can begin transmission of a cell or packet. Once transmission of a cell or packet begins, it cannot be stopped so this threshold should be set to a value which guarantees that the Utopia/POS-PHY interface can write to the FIFO in due time to prevent FIFO underruns. For packet data, it is recommended that DT[7:0] be set to a larger value about equal to 1/2 or 2/3 the size of the FIFO.

Register 132BH: TXSDQ FIFO Indirect Cells and Packets Count

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R	COUNT[3]	X
Bit 2	R	COUNT[2]	X
Bit 1	R	COUNT[1]	X
Bit 0	R	COUNT[0]	X

This register is used to read the 4-bit non-saturating FIFO counters for the enabled FIFOs, which count the number of ATM cells or packets accepted by the FIFO. The counts are latched when the register 0002H of the S/UNI MULTI-48 is written to. These counters are then reset, and the latched values can be read individually through this register.

The counters provided by the TXSDQ are purely for diagnostic purposes. They should be ignored in normal operations.

COUNT[3:0]

These read-only bits hold the last sampled count for the FIFO requested for in FIFO Indirect Address register PHYID[5:0] bits. This register is latched when register 0002H is written to for a global performance monitor update. After the count is latched into the register, the internal counter is reset to 0, and starts counting again. When this counter reaches its maximum count, it rolls over.

Register 132CH: TXSDQ FIFO Cells and Packets Accepted Aggregate Count (LSB)

Bit	Type	Function	Default
Bit 15	R	ACOUNT[15]	X
Bit 14	R	ACOUNT[14]	X
Bit 13	R	ACOUNT[13]	X
Bit 12	R	ACOUNT[12]	X
Bit 11	R	ACOUNT[11]	X
Bit 10	R	ACOUNT[10]	X
Bit 9	R	ACOUNT[9]	X
Bit 8	R	ACOUNT[8]	X
Bit 7	R	ACOUNT[7]	X
Bit 6	R	ACOUNT[6]	X
Bit 5	R	ACOUNT[5]	X
Bit 4	R	ACOUNT[4]	X
Bit 3	R	ACOUNT[3]	X
Bit 2	R	ACOUNT[2]	X
Bit 1	R	ACOUNT[1]	X
Bit 0	R	ACOUNT[0]	X

Register 132DH: TXSDQ FIFO Cells and Packets Accepted Aggregate Count (MSB)

Bit	Type	Function	Default
Bit 15	R	ACOUNT[31]	X
Bit 14	R	ACOUNT[30]	X
Bit 13	R	ACOUNT[29]	X
Bit 12	R	ACOUNT[28]	X
Bit 11	R	ACOUNT[27]	X
Bit 10	R	ACOUNT[26]	X
Bit 9	R	ACOUNT[25]	X
Bit 8	R	ACOUNT[24]	X
Bit 7	R	ACOUNT[23]	X
Bit 6	R	ACOUNT[22]	X
Bit 5	R	ACOUNT[21]	X
Bit 4	R	ACOUNT[20]	X
Bit 3	R	ACOUNT[19]	X
Bit 2	R	ACOUNT[18]	X
Bit 1	R	ACOUNT[17]	X
Bit 0	R	ACOUNT[16]	X

ACOUNT[31:0]

These bits display the aggregate count of all the POS packets and ATM cells that are accepted by the TXSDQ. This register is latched when register 0002H is written to for a global performance monitor update. After the count is latched into the register, the internal counter is reset to 0, and starts counting again. When this counter reaches its maximum count, it rolls over and starts counting again from 0.

Register 132EH: TXSDQ FIFO Cells and Packets Dropped Aggregate Count

Bit	Type	Function	Default
Bit 15	R	DCOUNT[15]	X
Bit 14	R	DCOUNT[14]	X
Bit 13	R	DCOUNT[13]	X
Bit 12	R	DCOUNT[12]	X
Bit 11	R	DCOUNT[11]	X
Bit 10	R	DCOUNT[10]	X
Bit 9	R	DCOUNT[9]	X
Bit 8	R	DCOUNT[8]	X
Bit 7	R	DCOUNT[7]	X
Bit 6	R	DCOUNT[6]	X
Bit 5	R	DCOUNT[5]	X
Bit 4	R	DCOUNT[4]	X
Bit 3	R	DCOUNT[3]	X
Bit 2	R	DCOUNT[2]	X
Bit 1	R	DCOUNT[1]	X
Bit 0	R	DCOUNT[0]	X

DCOUNT[15:0]

These bits display the aggregate count of all the POS packets and ATM cells that are dropped by the TXSDQ due to FIFO overflows. This register is latched when register 0002H is written to for a global performance monitor update. After the count is latched into the register, the internal counter is reset to 0, and starts counting again. When this counter reaches its maximum count, it rolls over and starts counting again from 0.

Register 1330H: TXPHY Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R/W	Reserved	0
Bit 8	W	Reserved1	0
Bit 7	R/W	TPAHOLD	0
Bit 6	R/W	INBANDADDR	1
Bit 5	W	Reserved0	0
Bit 4	W	Reserved0	0
Bit 3	R/W	PARERREN	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	ODDPARITY	0
Bit 0	R/W	TXPRST	1

TXPRST

The TXPRST bit is used to reset the TXPHY circuitry. When TXPRST is set to logic zero, the TXPHY operates normally. When TXPRST is set to logic one, the TXPHY ignores all pin inputs but the registers may be accessed for purposes of initialization. The TXPHY deasserts all outputs until a logic zero is written to TXPRST.

ODDPARITY

The ODDPARITY bit is used to set the type of parity that is generated by the TXPHY. When set to logic 1, odd parity is expected. When set to logic 0, even parity is expected. This bit is global and affects all PHY channels.

PARERREN

When set to logic 1, PARERREN will enable the TXPHY to pass an error signal to the TXSDQ upon detection of a parity error. This will cause the packet to be aborted by the cell processor. This bit has no effect on ATM cells with parity errors. If PARERREN is set to logic 0, parity errors will not disrupt the transmission of a packet. They will only cause an interrupt (if enabled).

INBANDADDR

The INBANDADDR bit is used only in POS-PHY L3 mode to indicate whether the in-band address is expected (INBANDADDR set to logic 1) or not (INBANDADDR set to logic 0) on the TX PL3 interface. This bit is useful in single PHY applications where the in-band addressing is optional (address 0 is assumed) and the Link Layer device does not send an address in band since there is only one PHY. This bit can only be changed when TXPRST is logic 1. Note that regardless of the value of INBANDADDR, PTPA will reflect the address value on the TADR pins. Also note that, when INBANDADDR is set to logic 0, the TSX pin can still be used as in multi PHY applications, or tied to logic 0.

TPAHOLD

The TPAHOLD bit is used only in POS-PHY mode to control the STPA and PTPA signal response time.

TPAHOLD can only be set to logic 1 if the upstream device is working in burst-transfer mode (TENB is deasserted between each burst). In this mode FIFO status at the beginning of a transfer will be used throughout the transfer to make the PTPA response to a poll. PTPA (for a given PHY) will be asserted within one clock cycle of the write which causes the FIFO fill level to cross its buffer available threshold, but PTPA can't be deasserted (for a given PHY) during a transfer. STPA should not be used when TPAHOLD is set to logic 1.

When TPAHOLD is set to logic 0, STPA/PTPA for a channel will deassert 5 clock cycles after the write which causes the FIFO fill level to cross its buffer available threshold. This mode is not recommended for Multi-PHY applications if the external transmit PL3 master is designed to simply hold the on-going transfer when STPA is deasserted. In such a case, an important amount of bandwidth can be lost during the time the PL3 interface is waiting for STPA to reassert. In standard transmit PL3 systems, this mode is only suitable for a Single-PHY application (one channel).

This bit cannot be changed during operation and can only be changed when TXPRST is logic one.

Reserved0

The Reserved0 bits must be set to logic 0 for proper operation.

Reserved1

The Reserved1 bit must be set to logic 1 for proper operation.

Register 1331H: TXPHY Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R	TDTFERRI	X
Bit 1	R	TPARERRI	X
Bit 0	R	RUNTCELLI	X

RUNTCELLI

The RUNTCELLI bit indicates that TENB was detected as being deasserted before the end of the cell transfer when operating in Utopia L3 mode. This will result in a partial cell transfer and an erroneous cell will passed to the TXSDQ. Possible causes are incorrect setting in the size of the cell expected by this interface. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read.

TPARERRI

The TPARERR bit is used to indicate that a Parity Error was observed on the incoming TDAT bus since the last time the interrupt was read. The packet will be marked erroneous and sent on to the TXSDQ. ATM cell transmission is not affected by parity errors. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read.

TDTFERRI

The TDTFERR bit is used to indicate that a Data Field mismatch was observed on the incoming TDAT[31:24] bus compared to the ATM/packet selection for that PHY configuration (selection done using the POS_SEL bits in the TXSDQ FIFO Indirect Configuration register). When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read.

Register 1332H: TXPHY Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R/W	TDTFERRE	0
Bit 1	R/W	TPARERRE	0
Bit 0	R/W	RUNTCELLE	0

RUNTCELLE

The RUNTCELLE bit is used to enable the detection of the runt cell condition (RUNTCELLI) to assert a hardware interrupt on the INTB pin. When set to logic 0, the hardware interrupt is masked. When set to logic 1, the hardware interrupt is enabled.

TPARERRE

The TPARERRE bit is used to enable the detection of a parity error (TPARERRI) to assert a hardware interrupt on the INTB pin. When set to logic 0, the hardware interrupt is masked. When set to logic 1, the hardware interrupt is enabled.

TDTFERRE

The TDTFERRE bit is used to enable the TDFTERRI interrupt status bit to assert a hardware interrupt on the INTB pin. When set to logic 0, the hardware interrupt is masked. When set to logic 1, the hardware interrupt is enabled.

Register 1333H: TXPHY Data Type Field

Bit	Type	Function	Default
Bit 15	R/W	POS_FIELD[7]	0
Bit 14	R/W	POS_FIELD[6]	0
Bit 13	R/W	POS_FIELD[5]	0
Bit 12	R/W	POS_FIELD[4]	0
Bit 11	R/W	POS_FIELD[3]	0
Bit 10	R/W	POS_FIELD[2]	0
Bit 9	R/W	POS_FIELD[1]	0
Bit 8	R/W	POS_FIELD[0]	1
Bit 7	R/W	ATM_FIELD[7]	0
Bit 6	R/W	ATM_FIELD[6]	0
Bit 5	R/W	ATM_FIELD[5]	0
Bit 4	R/W	ATM_FIELD[4]	0
Bit 3	R/W	ATM_FIELD[3]	0
Bit 2	R/W	ATM_FIELD[2]	0
Bit 1	R/W	ATM_FIELD[1]	0
Bit 0	R/W	ATM_FIELD[0]	0

The TXPHY Data Type Field is used in POS-PHY L3 mode of operation only and is provided as a means to identify the type of traffic, ATM or packet, being sent over the POS-PHY L3 interface. Selection of ATM and packet PHYs is done using the POS_SEL bit in the TXSDQ FIFO Indirect Configuration register.

ATM_FIELD[7:0]

The ATM_FIELD register is provided to identify an ATM cell being transferred over the POS-PHY L3 interface. When the incoming data is of type ATM cell, then the value of TDAT[31:24] at the cycle in which the in-band address is inserted on TDAT[5:0] (ie. when TSX = 1) should match ATM_FIELD[7:0]. Otherwise, an interrupt is signaled to indicate a data type mismatch.

POS_FIELD[7:0]

The POS_FIELD register is provided to identify packet data being transferred over the POS-PHY L3 interface. When the incoming data is of type packet, then the value of TDAT[31:24] at the cycle in which the in-band address is inserted on TDAT[5:0] (ie. When TSX = 1) should match POS_FIELD[7:0]. Otherwise, an interrupt is signaled to indicate a data type mismatch.

Register 1340H 1740H 1B40H 1F40H: TTDP Indirect Channel Select

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	R/W	Reserved	0
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	CHAN[1]	0
Bit 0	R/W	CHAN[0]	0

Note that when configuring a channel in the TTDP, that channel must be diasbled in the downstream TCAS12 block (using CHx_DIS bits from register 1360H) or the configuration write may not be properly executed.

CHAN[1:0]

The indirect channel number bits (CHAN[1:0]) indicate the channel to be updated or queried in the indirect access.

Reserved

The Reserved bit should be set to logic 0 for proper operation.

RWB

The read/write bar (RWB) bit selects between an update operation (write) and a query operation (read). Writing logic 0 to RWB triggers the update operation of the channel specified by CHAN[1:0] with the information in TTDP Registers 1, 2, and 3. Writing a logic 1 to RWB triggers a query of the channel specified by CHAN[1:0] and the information is placed in all of the Indirect Registers.

BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is logic 1 when a write to the Indirect Channel Select register triggers an indirect access and will stay logic 1 until the access is complete. This register should be polled to determine when data from an indirect read operation is available in all the Indirect Data registers or to determine when a new indirect write operation may commence. (Note – BUSY is also logic 1 after reset while the channel provision RAM is being initialized and is cleared when the RAM has completed initialization and the TTDP is ready to accept an indirect access operation to the RAM.)

Register 1341H 1741H 1B41H 1F41H: TTDP Indirect Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R/W	Reserved	0
Bit 12	R/W	DELINDIS	0
Bit 11	R/W	HCSDQDB	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	POS_SEL	0
Bit 8	R/W	CRC_SEL[1]	1
Bit 7	R/W	CRC_SEL[0]	1
Bit 6	R/W	FLAG[3]	0
Bit 5	R/W	FLAG[2]	0
Bit 4	R/W	FLAG[1]	0
Bit 3	R/W	FLAG[0]	0
Bit 2	R/W	SCRMBL	1
Bit 1	R/W	IDLE	0
Bit 0	R/W	PROV	0

This register must be initialized before triggering an indirect write, and reflects the value written until the completion of a subsequent indirect channel read operation.

PROV

The processor provision bit (PROV) is used to enable the TTDP. When PROV is logic 0, the TTDP ATM and POS processors are disabled and will not request data from the FIFO interface and will respond to data requests with idle data (all 1's). When PROV is logic 1, the TCFP ATM or POS processor is enabled and will respond to data requests with valid data after requesting and processing data from the TXSDQ FIFO interface.

IDLE

The inter-frame time fill bit (IDLE) configures the packet processor to use flag bytes or HDLC idle as the inter-frame time fill between packets. When IDLE is set to logic 0, the packet processor uses flag bytes as the inter-frame time fill. When IDLE is set to logic 1, the packet processor uses HDLC idle (all one's byte with no byte or bit stuffing pattern) as the inter-frame time fill. IDLE is only valid when POS_SEL is set to logic 1.

SCRMBL

The scramble enable bit (SCRMBL) controls the scrambling of the packet data stream or ATM cell payload. When SCRMBL is set to logic 1, scrambling is enabled. When SCRMBL is set to logic 0, scrambling is disabled.

FLAG[3:0]

The flag insertion control (FLAG[3:0]) configures the minimum number of flags or idle bytes the packet processor inserts between packets. The minimum number of flags (01111110) or bytes of idle (11111111) between two flags inserted between packets is shown in the table below. Idle bytes are inserted between flags only if the IDLE bit is set to logic 1. FLAG[3:0] are valid only when POS_SEL is set to logic 1.

Table 26 Selection of the number of Flag Bytes

FLAG[3:0]	Minimum Number of Flag/Idle Bytes
0000	1 flag/0 bytes of idle
0001	2 flags/0 bytes of idle
0010	4 flags/2 bytes of idle
0011	8 flags/6 bytes of idle
0100	16 flags/14 bytes of idle
0101	32 flags/30 bytes of idle
0110	64 flags/62 bytes of idle
0111	128 flags/126 bytes of idle
1000	256 flag/254 bytes of idle
1001	512 flags/510 bytes of idle
1010	1024 flags/1022 bytes of idle
1011	2048 flags/2046 bytes of idle
1100	4096 flags/4094 bytes of idle
1101	8192 flags/8190 bytes of idle
1110	16384 flags/16382 bytes of idle
1111	32768 flags/32766 bytes of idle

CRC_SEL[1:0]

The CRC select (CRC_SEL[1:0]) bits allow the control of the CRC calculation according to the table below. For ATM cells, when HCSDQDB is logic 0, the CRC is calculated over the first four ATM header octets, and when HCSDQDB is logic 1, the CRC is calculated over octets 2, 3, and 4. For packet applications, the CRC is calculated over the whole packet data, before byte stuffing and scrambling.

Table 27 CRC Mode Selection

CRC_SEL[1:0]	HCS Operation	FCS Operation
00	Reserved	No FCS inserted
01	Reserved	No FCS inserted
10	CRC-8 without coset polynomial	CRC-CCITT (2 bytes)
11	CRC-8 with coset polynomial added	CRC-32 (4 bytes)

POS_SEL

The ATM/POS selection bit (POS_SEL) configures the TTDP for operation in ATM or POS mode. When POS_SEL is logic 1, then POS mode is selected. When POS_SEL is logic 0, then ATM mode is selected.

HCSDQDB

The HCSDQDB bit controls the cell header octets included in the HCS calculation. When a logic 1 is written to HCSDQDB, header octets, 2, 3, and 4 are included in the HCS calculation as required by IEEE-802.6 DQDB specification. When a logic 0 is written to HCSDQDB, all four header octets are included in the HCS calculation as required by the ATM Forum UNI specification and ITU-T Recommendation I.432.

DELINDIS

The DELINDIS bit controls the disabling of bit/byte stuffing and flag insertion. When a logic 1 is written to DELINDIS, flags are not inserted unless a FIFO underrun occurs, and data is not stuffed. When a logic 0 is written to DELINDIS, packets are delimited by flags, and stuffed according to the IDLE, FLAG, and BIT_STUFF configuration bits. CRC insertion and scrambling are not affected by DELINDIS. DELINDIS is only valid when POS_SEL is logic 1. This bit should only be set when Transparent Mode operation is desired. In Transparent Mode, data must be written to the POS-PHY Level 3 Bus in 64 byte blocks, and the FIFO must not be allowed to underflow. In addition for Transparent Mode, the CRC_SEL bits should be set to “00” to disable CRC generation.

Reserved

The Reserved register bits must be set to logic 0 for proper operation.

Register 1342H 1742H 1B42H 1F42H: TTDP Indirect Idle/Unassigned ATM Cell Header

Bit	Type	Function	Default
Bit 15	R/W	GFC[3]	0
Bit 14	R/W	GFC[2]	0
Bit 13	R/W	GFC[1]	0
Bit 12	R/W	GFC[0]	0
Bit 11	R/W	PTI[2]	0
Bit 10	R/W	PTI[1]	0
Bit 9	R/W	PTI[0]	0
Bit 8	R/W	CLP	1
Bit 7	R/W	PAYLD[7]	0
Bit 6	R/W	PAYLD[6]	1
Bit 5	R/W	PAYLD[5]	1
Bit 4	R/W	PAYLD[4]	0
Bit 3	R/W	PAYLD[3]	1
Bit 2	R/W	PAYLD[2]	0
Bit 1	R/W	PAYLD[1]	1
Bit 0	R/W	PAYLD[0]	0

The Indirect Idle/Unassigned ATM Cell Header Register must be initialized before triggering an indirect write, and reflects the value written until the completion of a subsequent indirect channel read operation.

PAYLD[7:0]

The PAYLD[7:0] (Idle Cell Payload) value reflects the payload bytes which will be inserted into the ATM Idle cell generated by the TTDP.

CLP

The Cell Loss Priority bit (CLP) contains the eighth bit position of the fourth octet of the idle/unassigned cell pattern. Cell rate decoupling is accomplished by transmitting idle cells when the TTDP detects that no outstanding cells are available from the external FIFO and data is requested on the TTDP egress interface. Additionally, XOFF can be used to force the transmission of Idle/Unassigned cells in ATM mode.

PTI[2:0]

The Payload Type bits (PTI[2:0]) contain the fifth, sixth, and seventh bit positions of the fourth octet of the idle/unassigned cell pattern. Idle cells are transmitted when the TTDP detects that no outstanding cells are available for transmission. Additionally, XOFF can be used to force the transmission of Idle/Unassigned cells in ATM mode.

GFC[3:0]

The Generic Flow Control bits (GFC[3:0]) contain the first, second, third, and fourth bit positions of the first octet of the idle/unassigned cell pattern. Idle/unassigned cells are transmitted when the TTDP detects that no outstanding cells are available from the external FIFO for transmission. Additionally, XOFF can be used to force the transmission of Idle/Unassigned cells in ATM mode. The all zeros pattern is transmitted in the VCI and VPI fields of the idle/unassigned cell.

Register 1343H 1743H 1B43H 1F43H: TTDP Indirect Diagnostics

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	TX_BYTE_MODE	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	DCRC	0
Bit 3	R/W	INVERT	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

This register must be initialized before triggering an indirect write, and reflects the value written until the completion of a subsequent indirect channel read operation.

Reserved

The Reserved bits must be set to their default value for proper operation.

INVERT

The data inversion bit (INVERT) configures the ATM or packet processor to logically invert the outgoing data stream from the TTDP. When INVERT is set to logic 1, the outgoing data stream is logically inverted. The outgoing data stream is not inverted when INVERT is set to logic 0.

DCRC

The diagnostic CRC bit (DCRC) configures the ATM or packet processor to err the CRC on the outgoing data stream for diagnostic purposes. When DCRC is set to logic 1, the FCS value inserted by the POS/HDLC processor or the HCS value inserted by the ATM processor is logically XORed with CRC_XOR[7:0]. The inserted FCS or HCS is not logically XORed when DCRC is set to logic 0. DCRC is ignored when PROV is logic 0.

TX_BYTE_MODE

The transmit byte counter mode (TX_BYTE_MODE) bit is used to select the mode in which the TX_BYTE[31:0] counters work. When TX_BYTE_MODE is logic 0, TX_BYTE[31:0] will count all bytes in transmitted packets (including FCS and Abort bytes) before the bit/byte stuffing operation. When TX_BYTE_MODE is logic 1, TX_BYTE[31:0] will count all bytes in transmitted packets (including FCS, Abort, and stuff bytes) after the byte stuffing operation. Flag bytes will not be counted in either case. The TX_BYTE_MODE bit is only valid when working in byte-stuffed POS mode. In bit-stuffed HDLC mode, TX_BYTE_MODE must be set to logic 0. TX_BYTE[31:0] is not used in ATM mode.

Register 1344H 1744H 1B44H 1F44H: TTDP Indirect Transmit Cell/Packet Counter (LSB)

Bit	Type	Function	Default
Bit 15	R	TX_CELL[15]	X
Bit 14	R	TX_CELL[14]	X
Bit 13	R	TX_CELL[13]	X
Bit 12	R	TX_CELL[12]	X
Bit 11	R	TX_CELL[11]	X
Bit 10	R	TX_CELL[10]	X
Bit 9	R	TX_CELL[9]	X
Bit 8	R	TX_CELL[8]	X
Bit 7	R	TX_CELL[7]	X
Bit 6	R	TX_CELL[6]	X
Bit 5	R	TX_CELL[5]	X
Bit 4	R	TX_CELL[4]	X
Bit 3	R	TX_CELL[3]	X
Bit 2	R	TX_CELL[2]	X
Bit 1	R	TX_CELL[1]	X
Bit 0	R	TX_CELL[0]	X

Register 1345H 1745H 1B45H 1F45H: TTDP Indirect Transmit Cell/Packet Counter (MSB)

Bit	Type	Function	Default
Bit 15	R	TX_CELL[31]	X
Bit 14	R	TX_CELL[30]	X
Bit 13	R	TX_CELL[29]	X
Bit 12	R	TX_CELL[28]	X
Bit 11	R	TX_CELL[27]	X
Bit 10	R	TX_CELL[26]	X
Bit 9	R	TX_CELL[25]	X
Bit 8	R	TX_CELL[24]	X
Bit 7	R	TX_CELL[23]	X
Bit 6	R	TX_CELL[22]	X
Bit 5	R	TX_CELL[21]	X
Bit 4	R	TX_CELL[20]	X
Bit 3	R	TX_CELL[19]	X
Bit 2	R	TX_CELL[18]	X
Bit 1	R	TX_CELL[17]	X
Bit 0	R	TX_CELL[16]	X

TX_CELL[31:0]

The transmit cell/packet count bits (TX_CELL[31:0]) indicate the number of cells or **non-aborted** packets transmitted during the last accumulation interval. ATM Idle cells, HDLC flags, and HDLC Idle bytes inserted into the transmission stream are not counted.

A direct write to any one of the TTDP counter registers loads all the corresponding TTDP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0002H can be written to initiate a global performance counter update across the S/UNI MULTI-48. Note that only counters for channels that are provisioned and enabled in the TTDP and TCAS12 will be updated.

Register 1346H 1746H 1B46H 1F46H: TTDP Indirect Transmit Byte Counter (LSB)

Bit	Type	Function	Default
Bit 15	R	TX_BYTE[15]	X
Bit 14	R	TX_BYTE [14]	X
Bit 13	R	TX_BYTE [13]	X
Bit 12	R	TX_BYTE [12]	X
Bit 11	R	TX_BYTE [11]	X
Bit 10	R	TX_BYTE [10]	X
Bit 9	R	TX_BYTE [9]	X
Bit 8	R	TX_BYTE [8]	X
Bit 7	R	TX_BYTE [7]	X
Bit 6	R	TX_BYTE [6]	X
Bit 5	R	TX_BYTE [5]	X
Bit 4	R	TX_BYTE [4]	X
Bit 3	R	TX_BYTE [3]	X
Bit 2	R	TX_BYTE [2]	X
Bit 1	R	TX_BYTE [1]	X
Bit 0	R	TX_BYTE [0]	X

Register 1347H 1747H 1B47H 1F47H: TTDP Indirect Transmit Byte Counter (MSB)

Bit	Type	Function	Default
Bit 15	R	TX_BYTE [31]	X
Bit 14	R	TX_BYTE [30]	X
Bit 13	R	TX_BYTE [29]	X
Bit 12	R	TX_BYTE [28]	X
Bit 11	R	TX_BYTE [27]	X
Bit 10	R	TX_BYTE [26]	X
Bit 9	R	TX_BYTE [25]	X
Bit 8	R	TX_BYTE [24]	X
Bit 7	R	TX_BYTE [23]	X
Bit 6	R	TX_BYTE [22]	X
Bit 5	R	TX_BYTE [21]	X
Bit 4	R	TX_BYTE [20]	X
Bit 3	R	TX_BYTE [19]	X
Bit 2	R	TX_BYTE [18]	X
Bit 1	R	TX_BYTE [17]	X
Bit 0	R	TX_BYTE [16]	X

TX_BYTE[31:0]

The TX_BYTE[31:0] bits indicate the number of bytes in packets transmitted to the TTDP egress stream during the last accumulation interval. The byte counts include all user payload bytes, FCS bytes, and abort bytes. Inclusion of stuffed bytes is controlled by the TX_BYTE_MODE register bit. HDLC flags and Idle characters are not counted. The TX_BYTE[31:0] counters are only valid when processing packets.

A direct write to any one of the TTDP counter registers loads all the corresponding TTDP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0002H can be written to initiate a global performance counter update across the S/UNI MULTI-48. Note that only counters for channels that are provisioned and enabled in the TTDP and TCAS12 will be updated.

Register 1348H 1748H 1B48H 1F48H: TTDP Indirect Aborted Packet Counter

Bit	Type	Function	Default
Bit 15	R	TX_ABT[15]	X
Bit 14	R	TX_ABT[14]	X
Bit 13	R	TX_ABT[13]	X
Bit 12	R	TX_ABT[12]	X
Bit 11	R	TX_ABT[11]	X
Bit 10	R	TX_ABT[10]	X
Bit 9	R	TX_ABT[9]	X
Bit 8	R	TX_ABT[8]	X
Bit 7	R	TX_ABT[7]	X
Bit 6	R	TX_ABT[6]	X
Bit 5	R	TX_ABT[5]	X
Bit 4	R	TX_ABT[4]	X
Bit 3	R	TX_ABT[3]	X
Bit 2	R	TX_ABT[2]	X
Bit 1	R	TX_ABT[1]	X
Bit 0	R	TX_ABT[0]	X

TX_ABT[15:0]

The transmit aborted packet count bits (TX_ ABT[15:0]) indicate the number aborted packets transmitted to the TTDP egress stream during the last accumulation interval. These counters are only valid when packet mode is selected.

A direct write to any one of the TTDP counter registers loads all the corresponding TTDP's counter registers with the current counter value and resets the internal counters. The counter should be polled regularly to avoid saturating.

Register 0002H can be written to initiate a global performance counter update across the S/UNI MULTI-48. Note that only counters for channels that are provisioned and enabled in the TTDP and TCAS12 will be updated.

Register 1349H 1749H 1B49H 1F49H: TTDP CRC Error Mask

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	CRC_XOR[7]	0
Bit 6	R/W	CRC_XOR[6]	0
Bit 5	R/W	CRC_XOR[5]	0
Bit 4	R/W	CRC_XOR[4]	0
Bit 3	R/W	CRC_XOR[3]	0
Bit 2	R/W	CRC_XOR[2]	0
Bit 1	R/W	CRC_XOR[1]	0
Bit 0	R/W	CRC_XOR[0]	0

CRC_XOR[7:0]

The error mask CRC XOR bits (CRC_XOR[7:0]) is used in conjunction with DCRC to generate CRC errors. When DCRC is set to logic 1, the FCS byte values inserted by the POS/HDLC processor or the HCS value inserted by the ATM processor is logically XORed with CRC_XOR[7:0]. The inserted FCS or HCS is not logically XORed when DCRC is set to logic 0. DCRC is ignored when PROV is logic 0.

Register 134AH 174AH 1B4AH 1F4AH: TTDP Interrupt Enable 1

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	R/W	XFERE	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	FIFO_ERRE_3	0
Bit 2	R/W	FIFO_ERRE_2	0
Bit 1	R/W	FIFO_ERRE_1	0
Bit 0	R/W	FIFO_ERRE_0	0

FIFO_ERRE_**x**

The FIFO error interrupt enable bit (FIFO_ERRE_**x**) enables the generation of a hardware interrupt due to a FIFO error condition (TERR is asserted at the POS-PHY L3 interface or SOP and EOP are at unexpected locations) for channel **x**H. When FIFO_ERRE_**x** is set to logic one, the interrupt is enabled and causes FIFO_ERRI_**x** and the output INTB to be asserted. When set to logic zero, FIFO_ERRI_**x** will be asserted but not INTB.

XFERE

The transfer interrupt enable bit (XFERE) enables the generation of a hardware interrupt when an accumulation interval is completed and new values are stored in the transmitted packet/cell counter, transmitted byte counter, and aborted packet counter holding registers. When XFERE is set to logic 1, the interrupt is enabled and causes XFERI and the output INTB to be asserted. When XFERE is set to logic 0, XFERI will be asserted, but not INTB. XFERI is the transfer interrupt associated with all provisioned channels.

Register 134BH 174BH 1B4BH 1F4BH: TTDP Interrupt Enable 2

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	FIFO_UDRE_3	0
Bit 2	R/W	FIFO_UDRE_2	0
Bit 1	R/W	FIFO_UDRE_1	0
Bit 0	R/W	FIFO_UDRE_0	0

FIFO_UDRE_**x**

The FIFO underrun interrupt enable bit (FIFO_UDRE_**x**) enables the generation of an interrupt due to a FIFO underrun for channel **x**H. When FIFO_UDRE_**x** is set to logic 1, the interrupt is enabled and causes FIFO_UDRI_**x** and the output INTB to be asserted. When FIFO_UDRE is set to logic 0, FIFO_UDRI_**x** will be asserted but not INTB.

Register 134CH 174CH 1B4CH 1F4CH: TTDP Interrupt 1

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	R	XFERI	X
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	FIFO_ERRI_3	X
Bit 2	R	FIFO_ERRI_2	X
Bit 1	R	FIFO_ERRI_1	X
Bit 0	R	FIFO_ERRI_0	X

FIFO_ERRI_**x**

The FIFO error interrupt bit (FIFO_ERRI_**x**) bit is set to one when an ERROR is detected on the read side of the FIFO for channel **x**H. An abnormal sequence of TSOP and TEOP signals or the assertion of TERR from the POS-PHY interface can cause this error. This can normally be caused by a previous FIFO overrun or underrun condition. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read

XFERI

The transfer counter complete interrupt bit (XFERI) indicates that a transfer of accumulated counter data has occurred for all provisioned channels. A logic 1 in this bit position indicates that the transmitted cell/packet counter, transmitted byte counter, and aborted packet counter holding registers have been updated. This update is initiated by writing to one of the counter register locations, or writing to register 0002H for a global performance monitor update. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read.

Register 134DH 174DH 1B4DH 1F4DH: TTDP Interrupt 2

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	FIFO_UDRI_3	X
Bit 2	R	FIFO_UDRI_2	X
Bit 1	R	FIFO_UDRI_1	X
Bit 0	R	FIFO_UDRI_0	X

FIFO_UDRI_**x**

The FIFO underrun interrupt bit (FIFO_UDRI_**x**) bit is logic 1 when an attempt is made to read from the TXSDQ FIFO while it is empty for channel **x**H. This is considered a system error. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read.

Register 134EH 174EH 1B4EH 1F4EH: TTDP Transmit Off

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	XOFF _3	0
Bit 2	R/W	XOFF _2	0
Bit 1	R/W	XOFF _1	0
Bit 0	R/W	XOFF _0	0

XOFF_**x**

The transmission off bit (XOFF_**x**) serves as a transmission enable bit for channel **x**. When channel x is provisioned and XOFF_**x** is set to logic 0, ATM cells or packets are transmitted normally. When channel **x** is provisioned and XOFF_**x** is set to logic 1, the cell or packet being transmitted is completed and then transmission is suspended. When XOFF_**x** is asserted, the TTDP will not request data from the external FIFO. ATM Idle cells or POS flags will be sent on the TTDP egress interface.

Register 1360H 1760H 1B60H 1F60H: TCAS12 Channel Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	Reserved	1
Bit 10	R/W	Reserved	1
Bit 9	R/W	Reserved	1
Bit 8	R/W	Reserved	1
Bit 7	R/W	Reserved	1
Bit 6	R/W	Reserved	1
Bit 5	R/W	Reserved	1
Bit 4	R/W	Reserved	1
Bit 3	R/W	CH3_DIS	1
Bit 2	R/W	CH2_DIS	1
Bit 1	R/W	CH1_DIS	1
Bit 0	R/W	CH0_DIS	1

CH***x***_DIS

The Channel ***x*** disable bit (CH***x***_DIS) disables Channel ***x***. When CH***x***_DIS is logic 1, the TCAS12 will cease requesting data from the upstream block and FDATA[7:0] is inserted onto the timeslot. When CH***x***_DIS is logic 0, the TCAS12 will request data from the upstream block for Channel ***x*** normally.

Register 1362H 1762H 1B62H 1F62H + *x*: TCAS12 Timeslot *x* Configuration (*x* = 0H to BH)

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R/W	Reserved	0
Bit 8	R/W	LOCK0	0
Bit 7	R/W	TS***x*** _MODE[2]	0
Bit 6	R/W	TS***x*** _MODE[1]	0
Bit 5	R/W	TS***x*** _MODE[0]	0
Bit 4	R/W	TS***x*** _PROV	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	TS***x*** _CHAN[1]	0
Bit 0	R/W	TS***x*** _CHAN[0]	0

TS***x***_CHAN[1:0]

The TS***x***_CHAN[1:0] bits give the channel number from which the data stream in timeslot ***x*** is taken from.

TS***x***_PROV

The TS***x***_PROV bit provisions and unprovisions the timeslot. When TS***x***_PROV is logic 1, data to timeslot ***x*** is processed as part of the channel as indicated by TS***x***_CHAN. When TS***x***_PROV is logic 0, the data transmitted on timeslot ***x*** is taken from the TCAS12's FDATA[7:0] register bit settings instead of from the upstream block.

TS***x***_MODE[2:0]

The TS***x***_MODE[2:0] bits identify the type of traffic carried on timeslot ***x***. All timeslots associated with a concatenated payload channel must be set up appropriately as shown in Table 28.

Table 28 TCAS12 Timeslot Mode Selection

TS*x*_MODE[2:0]	Line Traffic Type
000	STS-48c/VC-4-16c or STS-12c/VC-4-4c
001	STS-3c/VC-4
010	Reserved
011	Reserved
100	Reserved
101	Reserved
110	Reserved
111	Reserved

LOCK0

The LOCK0 bit controls the payload offset of the TCAS12 outgoing data stream in the locked mode. When LOCK0 is set to logic 1, the J1 byte in the outgoing data stream is forced to the byte immediately following the H3 bytes (pointer offset = 0). When LOCK0 is logic 0, the J1 byte is forced to the byte immediately following the J0 byte (pointer offset = 522). For either setting of LOCK0, the outgoing H1 and H2 bytes will be valid.

Note that the pointer value will be modified by the TSVCA towards the transmit line interface. Thus, the actual 0/522 locked pointer value will only apply when the data is output on the Transmit APS port. The Transmit Line pointer value is not deterministic.

Reserved

The Reserved bits should be set to logic 0 for proper operation.

Register 136EH 176EH 1B6EH 1F6EH: TCAS12 Idle Timeslot Fill Data

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	R/W	Reserved	0
Bit 7	R/W	FDATA[7]	1
Bit 6	R/W	FDATA[6]	1
Bit 5	R/W	FDATA[5]	1
Bit 4	R/W	FDATA[4]	1
Bit 3	R/W	FDATA[3]	1
Bit 2	R/W	FDATA[2]	1
Bit 1	R/W	FDATA[1]	1
Bit 0	R/W	FDATA[0]	1

This register contains the data to be written to disabled timeslots.

FDATA[7:0]

The fill data bits (FDATA[7:0]) are transmitted during unprovisioned timeslots (TS***x***_PROV) or timeslots connected to disabled channels (CH***x***_DIS) or serial links.

Reserved

The Reserved bits should be set to logic 0 for proper operation.

12 Test Features Description

Simultaneously asserting (low) the CSB, RDB, and WRB inputs causes all digital output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the S/UNI MULTI-48 device. Test mode registers (as opposed to normal mode registers) are selected when TRS (A[13]) is high.

Test mode registers may also be used for board testing. When all of the functional blocks within the S/UNI MULTI-48 device are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface (refer to the section "Test Mode 0" for details).

In addition, the S/UNI MULTI-48 device also supports a standard IEEE 1149.1 five-signal JTAG boundary scan test port for use in board testing. All digital device inputs may be read and all digital device outputs may be forced via the JTAG test port.

Table 29 Test Mode Register Memory Map

Address	Register
0000H-1FFFH	Normal Mode Registers
2000H	Master Test Register
2001H	Test Mode Address Force Enable
2002H	Test Mode Address Force Value
2003H	Receive Analog Test Mode enable #1
2004H	Receive Analog Test Mode enable #2
2005H	Transmit Analog Test Mode enable #1
2006H	Transmit Analog Test Mode enable #2
2007H	TM0 Smart Framing Block frame pulses
2008H	TM0 Smart Framing Block APSFP2J0DLY
2009H	Characterization #1
200AH	Characterization #2
200BH	Characterization #3
200CH	Characterization #4
200DH-3FFFH	Reserved For Test

Note that test registers in address range 2000H-201FH are mirrored in 2400H-241FH, 2800H-281FH, and 2C00H-2C1FH.

12.1 Master Test and Test Configuration Registers

Notes on Test Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.

2. Writeable test mode register bits are not initialized upon reset unless otherwise noted.

Register 2000H: S/UNI MULTI-48 Master Test

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	FORCE_LASVCLK	0
Bit 6	R/W	PMCATST_2488	X
Bit 5	R/W	PMCATST	X
Bit 4	R/W	PMCTST	X
Bit 3	R/W	DBCTRL	0
Bit 2	R/W	IOTST	0
Bit 1	R/W	HIZDATA	0
Bit 0	R/W	HIZIO	0

This register is used to enable S/UNI MULTI-48 test features. All bits, except PMCATST_2488, PMCTST and PMCATST are reset to zero by a reset of the S/UNI MULTI-48 using the RSTB input. PMCATST_2488, PMCTST and PMCATST are reset when CSB is logic 1. PMCATST_2488, PMCTST and PMCATST can also be reset by writing a logic 0 to the corresponding register bit.

Both PMCATST and PMCATST_2488 (bit 5 and 6) in this register must be set to high for 2488 line side analog test.

Access to this register is not affected by the Test Mode Address Force functions in registers 2001H and 2002H.

HIZIO, HIZDATA

The HIZIO and HIZDATA bits control the tri-state modes of the S/UNI MULTI-48 . While the HIZIO bit is a logic one, all output pins of the S/UNI MULTI-48 except the data bus and output TDO are held tri-state. The microprocessor interface is still active. While the HIZDATA bit is a logic one, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles. The HIZDATA bit is overridden by the DBCTRL bit.

IOTST

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each block in the S/UNI MULTI-48 for board level testing. When IOTST is a logic 1, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequently the device outputs.

DBCTRL

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic 1 and PMCTST is set to logic 1, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the S/UNI MULTI-48 to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

PMCTST

The PMCTST bit is used to configure the S/UNI MULTI-48 for PMC-Sierra's manufacturing tests. When PMCTST is set to logic one, the S/UNI MULTI-48 microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors. The PMCTST can be cleared by setting CSB to logic one or by writing logic zero to the bit.

PMCATST

The PMCATST bit is used to configure the analog portion of the S/UNI MULTI-48 for PMC-Sierra's manufacturing tests. The PMCATST can be cleared by setting CSB to logic one or by writing logic zero to the bit. Both PMCATST and PMCATST_2488 (bit 5 and 6) in this register must be set to high for 2488 line side analog test. Only PMCATST needs to be set high for APS analog test.

PMCATST_2488

The PMCATST_2488 bit is used to configure the 2488 Mbit/s analog portion of the S/UNI MULTI-48 for PMC-Sierra's manufacturing tests. The PMCATST_2488 can be cleared by setting CSB to logic one or by writing logic zero to the bit. Both PMCATST and PMCATST_2488 (bit 5 and 6) in this register must be set to high for 2488 line side analog test.

FORCE_LASVCLK

The FORCE_LASVCLK bit is used to configure the test clock of the LAS4x622 block for PMC-Sierra's manufacturing tests. When FORCE_LASVCLK is logic 1, SD_TEST input pin is used as a test clock. FORCE_LASVCLK cannot be reset in normal mode. It is cleared to 0 in test mode when RSTB is low or when PMCTST is low.

Register 2001H: S/UNI MULTI-48 Test Mode Address Force Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	Reserved	X
Bit 2	R/W	Reserved	X
Bit 1	R/W	SFBA_SCAN	X
Bit 0	R/W	TM_A_EN	X

This register is used to force the address pins to a certain value. These bits are valid when either PMCTST or PMCATST is set to logic 1.

Access to this register is not affected by the Test Mode Address Force functions in registers 2001H and 2002H.

TM_A_EN

When TM_A_EN is logic 1 and either PMCTST or PMCATST is logic 1, the TM_A[1:0] register bits replace the input pins A[12:11]. Like PMCTST and PMCATST, the TM_A_EN bit is cleared only when CSB is logic 1 or when it is written to logic 0.

SFBA_SCAN

When SFBA_SCAN is logic 1, the SFBA blocks are configured in scan mode. SFBA_SCAN is cleared when CSB is logic 1 or when it is written to logic 0.

Register 2002H: S/UNI MULTI-48 Test Mode Address Force Value

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R/W	TM_SLICE	X
Bit 1	R/W	TM_A[1]	X
Bit 0	R/W	TM_A[0]	X

This register is used to force the address pins to a certain value. These bits are valid when either PMCTST or PMCATST is set to logic 1. The TM_A[1:0] bits are forced on A[12:11] when TM_A_EN is logic 1. Otherwise, the A[12:11] pin signals are used.

Access to this register is not affected by the Test Mode Address Force functions in registers 2001H and 2002H.

TM_A[1:0]

When TM_A_EN is logic 1 and either PMCTST or PMCATST is logic 1, the TM_A[1:0] bits replace the input pins A[12:11]. The TM_A[1:0] bits are not cleared on reset. These bits can be cleared by setting CSB to logic one or by writing logic zero to these bits.

TM_SLICE

When TM_A_EN is logic 1 and either PMCTST or IOTST is logic 1, the TM_SLICE bit high will force the S/UNI MULTI-48 to ignore the input pin A[12:11] and select all 4 slices. Like PMCTST and PMCATST, TM_SLICE bits are cleared only when CSB is logic 1 or when they are written to logic 0.

Register 2003H: S/UNI MULTI-48 Receive Analog Test Mode Enable Test Register #1

Bit	Type	Function	Default
Bit 15	R/W	ARXTSTBUS[15]	X
Bit 14	R/W	ARXTSTBUS[14]	X
Bit 13	R/W	ARXTSTBUS[13]	X
Bit 12	R/W	ARXTSTBUS[12]	X
Bit 11	R/W	ARXTSTBUS[11]	X
Bit 10	R/W	ARXTSTBUS[10]	X
Bit 9	R/W	ARXTSTBUS[9]	X
Bit 8	R/W	ARXTSTBUS[8]	X
Bit 7	R/W	ARXTSTBUS[7]	X
Bit 6	R/W	ARXTSTBUS[6]	X
Bit 5	R/W	ARXTSTBUS[5]	X
Bit 4	R/W	ARXTSTBUS[4]	X
Bit 3	R/W	ARXTSTBUS[3]	X
Bit 2	R/W	ARXTSTBUS[2]	X
Bit 1	R/W	ARXTSTBUS[1]	X
Bit 0	R/W	ARXTSTBUS[0]	X

This register can be accessed when either PMCTST or PMCATST is set to logic 1.

Register 2004H: S/UNI MULTI-48 Receive Analog Test Mode Enable Test Register #2

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	ARXTSTBUS[19]	X
Bit 2	R/W	ARXTSTBUS[18]	X
Bit 1	R/W	ARXTSTBUS[17]	X
Bit 0	R/W	ARXTSTBUS[16]	X

This register can be accessed when either PMCTST or PMCATST is set to logic 1.

ARXTSTBUS[19:0]

When ARXTSTBUS[19:0] and PMCATST are logic 1, the analog PECL receiver is configured for its manufacturing test mode. Like PMCTST and PMCATST, ARXTSTBUS bits are cleared only when CSB is logic 1 or when they are written to logic 0.

Register 2005H: S/UNI MULTI-48 Transmit Analog Test Mode Enable Test Register #1

Bit	Type	Function	Default
Bit 15	R/W	ATXTSTBUS[15]	X
Bit 14	R/W	ATXTSTBUS[14]	X
Bit 13	R/W	ATXTSTBUS[13]	X
Bit 12	R/W	ATXTSTBUS[12]	X
Bit 11	R/W	ATXTSTBUS[11]	X
Bit 10	R/W	ATXTSTBUS[10]	X
Bit 9	R/W	ATXTSTBUS[9]	X
Bit 8	R/W	ATXTSTBUS[8]	X
Bit 7	R/W	ATXTSTBUS[7]	X
Bit 6	R/W	ATXTSTBUS[6]	X
Bit 5	R/W	ATXTSTBUS[5]	X
Bit 4	R/W	ATXTSTBUS[4]	X
Bit 3	R/W	ATXTSTBUS[3]	X
Bit 2	R/W	ATXTSTBUS[2]	X
Bit 1	R/W	ATXTSTBUS[1]	X
Bit 0	R/W	ATXTSTBUS[0]	X

This register can be accessed when either PMCTST or PMCATST is set to logic 1.

Register 2006H: S/UNI MULTI-48 Transmit Analog Test Mode Enable Test Register #2

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R/W	ATXTSTBUS[18]	X
Bit 1	R/W	ATXTSTBUS[17]	X
Bit 0	R/W	ATXTSTBUS[16]	X

This register can be accessed when either PMCTST or PMCATST is set to logic 1.

ATXTSTBUS[18:0]

When ATXTSTBUS[18:0] and PMCATST are logic 1, the analog PECL transmitter is configured for its manufacturing test mode. Like PMCTST and PMCATST, ATXTSTBUS bits are cleared only when CSB is logic 1 or when they are written to logic 0.

Register 2007H: S/UNI MULTI-48 TM0 Smartframing block frame pulses

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R/W	TM0_TSTSI_J0P	X
Bit 3	R/W	TM0_TCAS_OFP	X
Bit 2	R/W	TM0_RSVCA_OFP	X
Bit 1	R/W	TM0_RXAPS_J0P	X
Bit 0	R/W	TM0_TXAPS_J0P	X

This register can be accessed when either PMCTST or PMCATST is set to logic 1.

TM0_TXAPS_J0P

TM0_TXAPS_J0P controls the J0 pulse between the smart framing block and the transmit APS sub-system, and between the smart framing block and the receive PL3/UL3 subsystem. This bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

TM0_RXAPS_J0P

TM0_RXAPS_J0P controls the J0 pulse between the smart framing block and the transmit SONET subsystem. This bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

TM0_RSVCA_OFP

TM0_RSVCA_OFP controls the frame pulse between the smart framing block and the RSVCA blocks. This bit can be cleared by setting CSB to logic one or by writing logic zero to the bit. This bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

TM0_TCAS_OFP

TM0_TCAS_OFP controls the frame pulse between the smart framing block and the TCAS12 block. This bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

TM0_TSTSI_J0P

TM0_TSTSI_J0P controls the J0 pulse between the smart framing block and the TSTSI block. This bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

Register 2008H: S/UNI MULTI-48 TM0 Smartframing block APSFP2J0DLY

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R/W	TM0_APSFP2J0DLY[13]	X
Bit 12	R/W	TM0_APSFP2J0DLY[12]	X
Bit 11	R/W	TM0_APSFP2J0DLY[11]	X
Bit 10	R/W	TM0_APSFP2J0DLY[10]	X
Bit 9	R/W	TM0_APSFP2J0DLY[9]	X
Bit 8	R/W	TM0_APSFP2J0DLY[8]	X
Bit 7	R/W	TM0_APSFP2J0DLY[7]	X
Bit 6	R/W	TM0_APSFP2J0DLY[6]	X
Bit 5	R/W	TM0_APSFP2J0DLY[5]	X
Bit 4	R/W	TM0_APSFP2J0DLY[4]	X
Bit 3	R/W	TM0_APSFP2J0DLY[3]	X
Bit 2	R/W	TM0_APSFP2J0DLY[2]	X
Bit 1	R/W	TM0_APSFP2J0DLY[1]	X
Bit 0	R/W	TM0_APSFP2J0DLY[0]	X

This register can be accessed when either PMCTST or PMCATST is set to logic 1.

TM0_APSFP2J0DLY[13:0]

TM0_APSFP2J0DLY[13:0] controls the APSFP2J0DLY[13:0] bus from the smart framing block to the S/UNI MULTI-48 normal registers. These bits can be cleared by setting CSB to logic one or by writing logic zero to these bits.

Register 2009H: S/UNI MULTI-48 Characterization #1

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	CHAR_APSIFP	X
Bit 6	R/W	IOCHAREN	X
Bit 5	R/W	CHAR_APSOFP	X
Bit 4	R/W	CHAR_RTOH[1]	X
Bit 3	R/W	CHAR_RTOHFP[1]	X
Bit 2	R/W	CHAR_RTOHCLK[1]	X
Bit 1	R/W	CHAR_B3E[1]	X
Bit 0	R/W	CHAR_RALM[1]	X

This register can be accessed when either PMCTST or PMCATST is set to logic 1. To be active, the IOCHAREN bit must be logic 1.

CHAR_RALM[1]

CHAR_RALM[1] controls the input of the last flop before the RALM[1] output. This bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

CHAR_B3E[1]

CHAR_B3E[1] controls the input of the last flop before the B3E[1] output. This bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

CHAR_RTOHCLK[1]

CHAR_RTOHCLK[1] controls the input of the last flop before the RTOHCLK[1] output. This bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

CHAR_RTOHFP[1]

CHAR_RTOHFP[1] controls the input of the last flop before the RTOHFP[1] output. This bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

CHAR_RTOH[1]

CHAR_RTOH[1] controls the input of the last flop before the RTOH[1] output. This bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

CHAR_APSOFP

CHAR_APSOFP controls the input of the last flop before the APSOFP output. This bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

IOCHAREN

IOCHAREN enables the use of the test registers 2009H, 200AH, 200BH and 200CH. This bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

CHAR_APSIFP

CHAR_APSIFP is used to read the APSIFP sampled input.

Register 200AH: S/UNI MULTI-48 Characterization #2

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	Reserved	X
Bit 4	R/W	CHAR_RTOH[2]	X
Bit 3	R/W	CHAR_RTOHFP[2]	X
Bit 2	R/W	CHAR_RTOHCLK[2]	X
Bit 1	R/W	CHAR_B3E[2]	X
Bit 0	R/W	CHAR_RALM[2]	X

This register can be accessed when either PMCTST or PMCATST is set to logic 1. To be active, the IOCHAREN bit must be logic 1.

CHAR_RALM[2]

CHAR_RALM[2] controls the input of the last flop before the RALM[2] output. This bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

CHAR_B3E[2]

CHAR_B3E[2] controls the input of the last flop before the B3E[2] output. This bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

CHAR_RTOHCLK[2]

CHAR_RTOHCLK[2] controls the input of the last flop before the RTOHCLK[2] output. This bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

CHAR_RTOHFP[2]

CHAR_RTOHFP[2] controls the input of the last flop before the RTOHFP[2] output. This bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

CHAR_RTOH[2]

CHAR_RTOH[2] controls the input of the last flop before the RTOH[2] output. This bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

Register 200BH: S/UNI MULTI-48 Characterization #3

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	Reserved	X
Bit 4	R/W	CHAR_RTOH[3]	X
Bit 3	R/W	CHAR_RTOHFP[3]	X
Bit 2	R/W	CHAR_RTOHCLK[3]	X
Bit 1	R/W	CHAR_B3E[3]	X
Bit 0	R/W	CHAR_RALM[3]	X

This register can be accessed when either PMCTST or PMCATST is set to logic 1. To be active, the IOCHAREN bit must be logic 1.

CHAR_RALM[3]

CHAR_RALM[3] controls the input of the last flop before the RALM[3] output. This bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

CHAR_B3E[3]

CHAR_B3E[3] controls the input of the last flop before the B3E[3] output. This bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

CHAR_RTOHCLK[3]

CHAR_RTOHCLK[3] controls the input of the last flop before the RTOHCLK[3] output. This bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

CHAR_RTOHFP[3]

CHAR_RTOHFP[3] controls the input of the last flop before the RTOHFP[3] output. This bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

CHAR_RTOH[3]

CHAR_RTOH[3] controls the input of the last flop before the RTOH[3] output. This bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

Register 200CH: S/UNI MULTI-48 Characterization #4

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	Reserved	X
Bit 4	R/W	CHAR_RTOH[4]	X
Bit 3	R/W	CHAR_RTOHFP[4]	X
Bit 2	R/W	CHAR_RTOHCLK[4]	X
Bit 1	R/W	CHAR_B3E[4]	X
Bit 0	R/W	CHAR_RALM[4]	X

This register can be accessed when either PMCTST or PMCATST is set to logic 1. To be active, the IOCHAREN bit must be logic 1.

CHAR_RALM[4]

CHAR_RALM[4] controls the input of the last flop before the RALM[4] output. This bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

CHAR_B3E[4]

CHAR_B3E[4] controls the input of the last flop before the B3E[4] output. This bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

CHAR_RTOHCLK[4]

CHAR_RTOHCLK[4] controls the input of the last flop before the RTOHCLK[4] output. This bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

CHAR_RTOHFP[4]

CHAR_RTOHFP[4] controls the input of the last flop before the RTOHFP[4] output. This bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

CHAR_RTOH[4]

CHAR_RTOH[4] controls the input of the last flop before the RTOH[4] output. This bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

12.2 JTAG Test Port

The S/UNI MULTI-48 JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operation section.

Table 30 Instruction Register (Length - 3 bits)

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Table 31 Identification Register

Length	32 bits
Version Number	1H (revision B)
Part Number	5360H
Manufacturer's Identification Code	0CDH
Device Identification	053600CDH

12.3 Boundary Scan Cells

In the following diagrams, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the center of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the Boundary Scan Register table located above.

Figure 29 Input Observation Cell (IN_CELL)

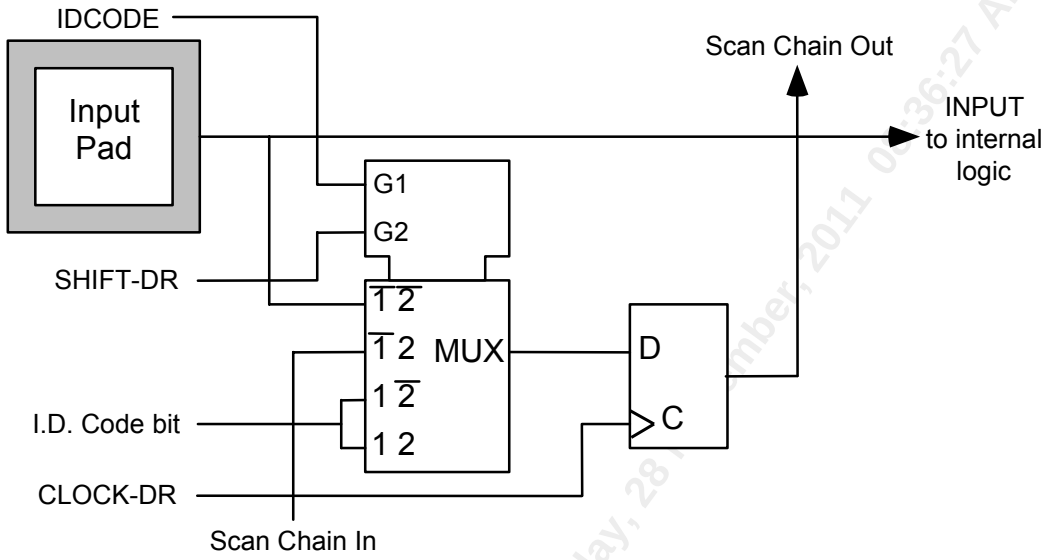


Figure 30 Output Cell (OUT_CELL)

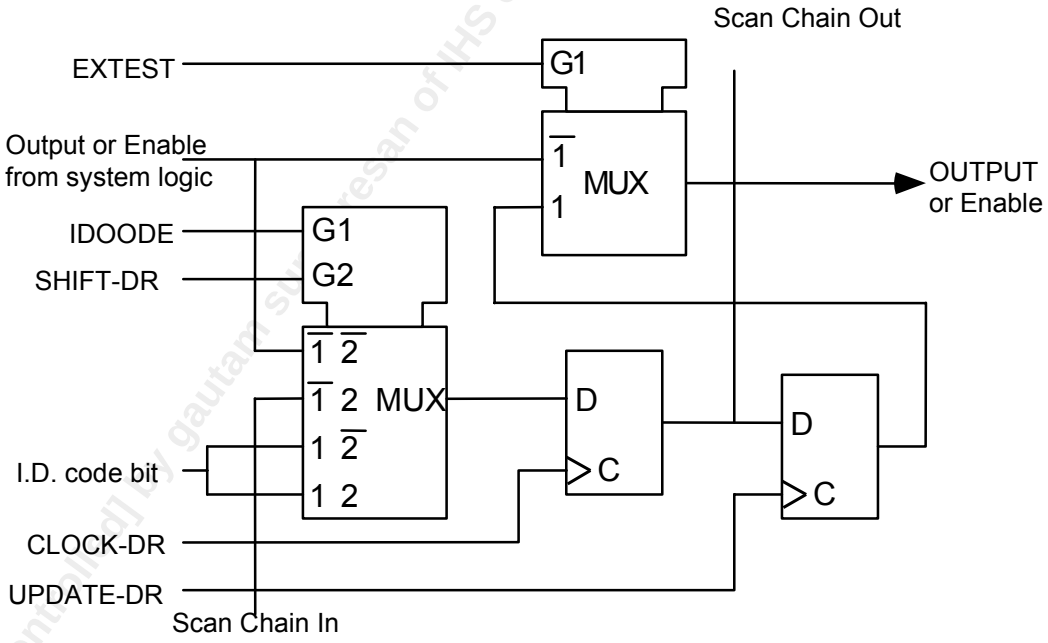


Figure 31 Bidirectional Cell (IO_CELL)

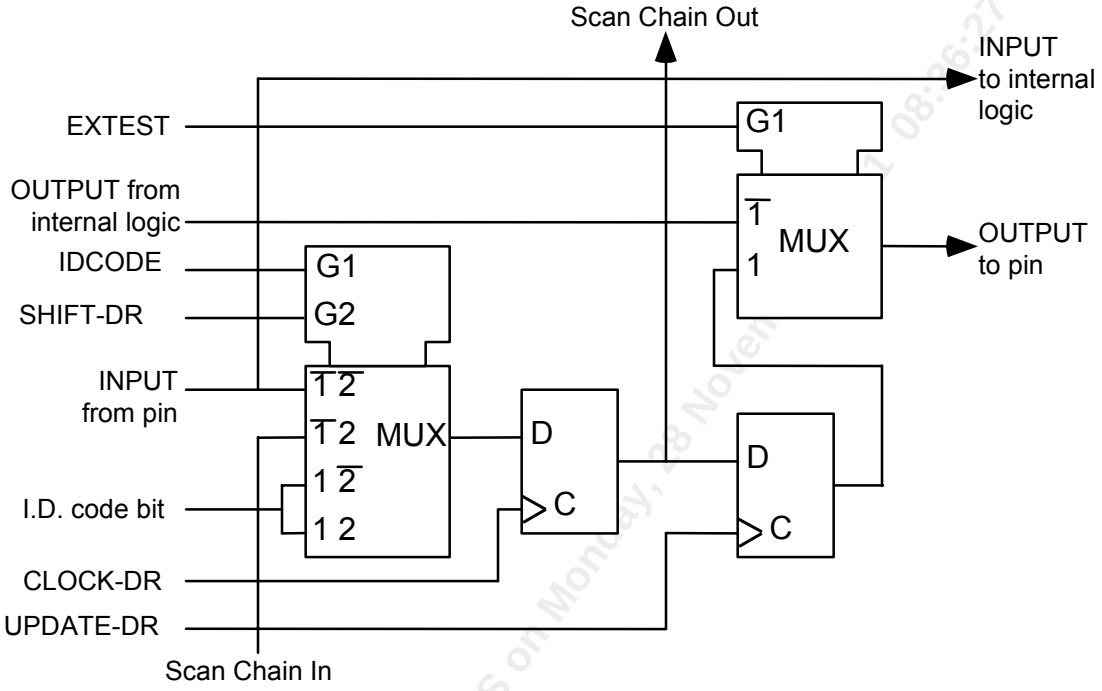
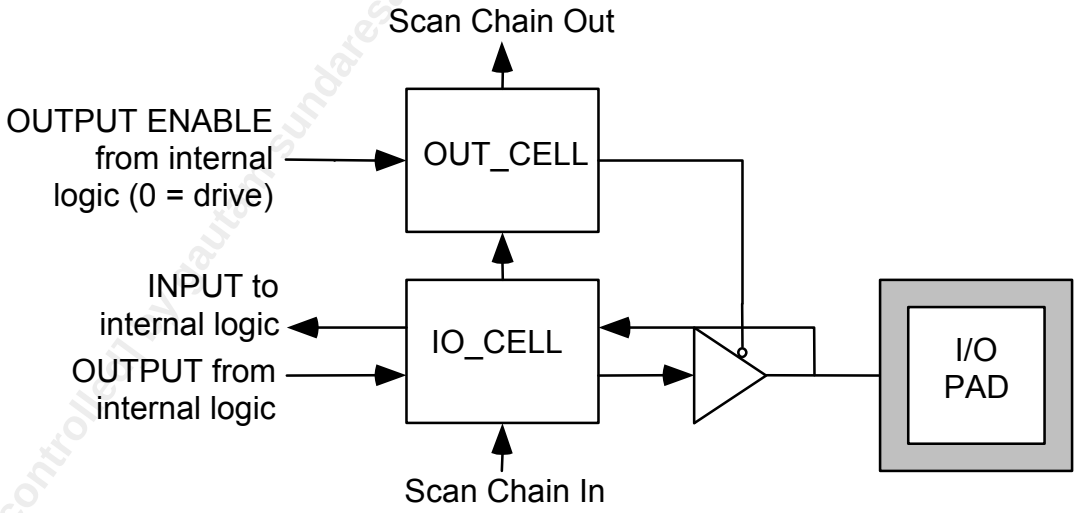


Figure 32 Layout of Output Enable and Bidirectional Cells



13 Operation

The S/UNI MULTI-48 device supports a rich set of line, path, APS, and packet/cell configuration options. This section provides details about operating the device.

13.1 Board Design Recommendations

Environmental noise and signal integrity are often the limiting factors in system performance. The following board design guidelines must be followed to ensure proper operation:

1 Use a single plane for grounds.

2 Provide separate +3.3 volt analog transmit, +3.3 volt analog receive, and +3.3 volt digital supplies, but otherwise connect the supply voltages together at one point close to the connector where +3.3 volt supply is brought to the card.

3 Provide separate +1.8 volt analog transmit, +1.8 volt analog receive, and +1.8 volt digital supplies, but otherwise connect the supply voltages together at one point close to the connector where +1.8 volt supply is brought to the card.

4 Ferrite beads are not advisable in digital switching circuits because inductive spiking (di/dt noise) is introduced into the power rail. Simple RC filtering is the best approach, provided care is taken to ensure the IR drop in the resistance does not lower the supply voltage below the recommended operating voltage.

5 High-frequency decoupling capacitors are recommended for the analog power pins and they should be as close to the package pin as possible. Separate decoupling is required to prevent the transmitter from coupling noise into the receiver and to prevent transients from coupling into some reference circuitry. See the section on Power Supplies for more details.

6 The high speed signals must be routed with 50 ohm controlled impedance circuit board traces and must be terminated with a matched load. Normal TTL-type design rules are not recommended and will reduce the performance of the device.

13.2 Power Supplies filtering

Figure 33 Line Analog Power Supply Filtering

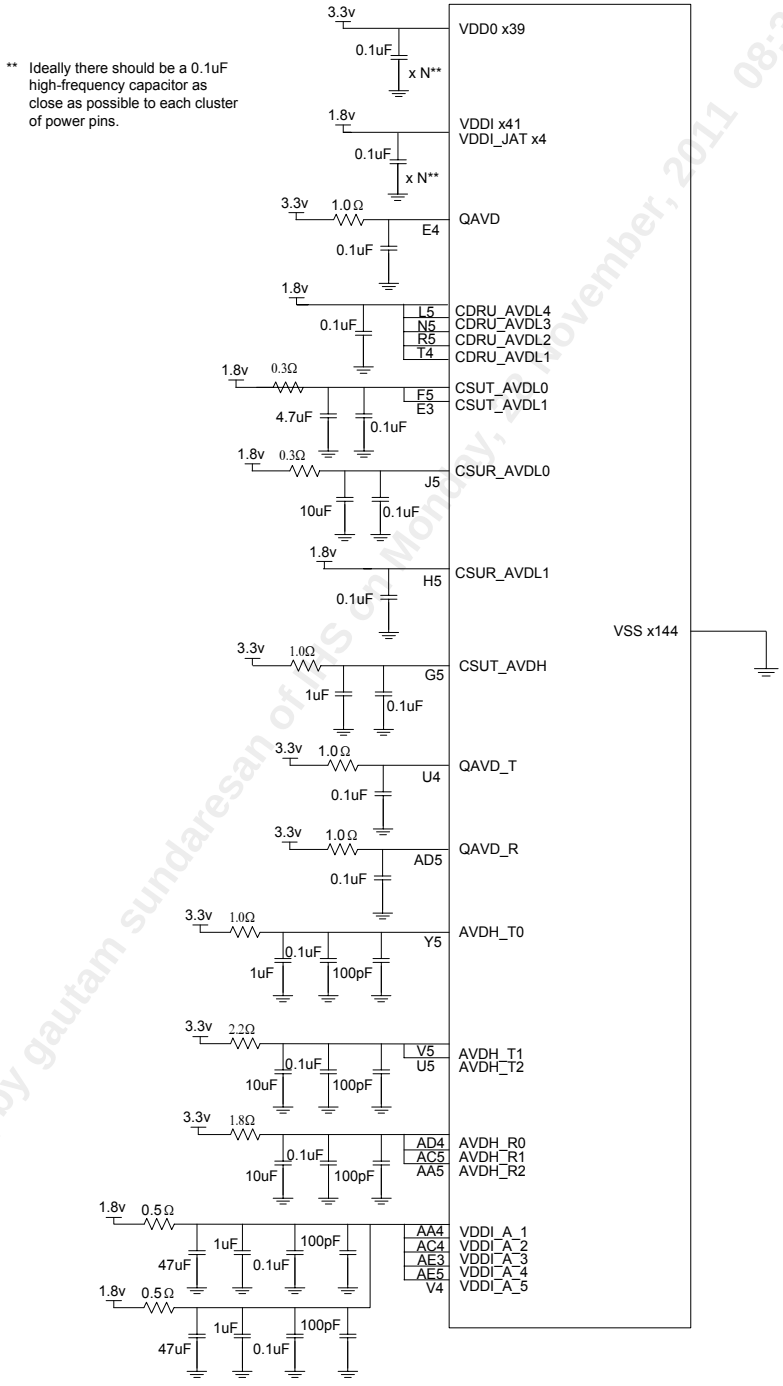
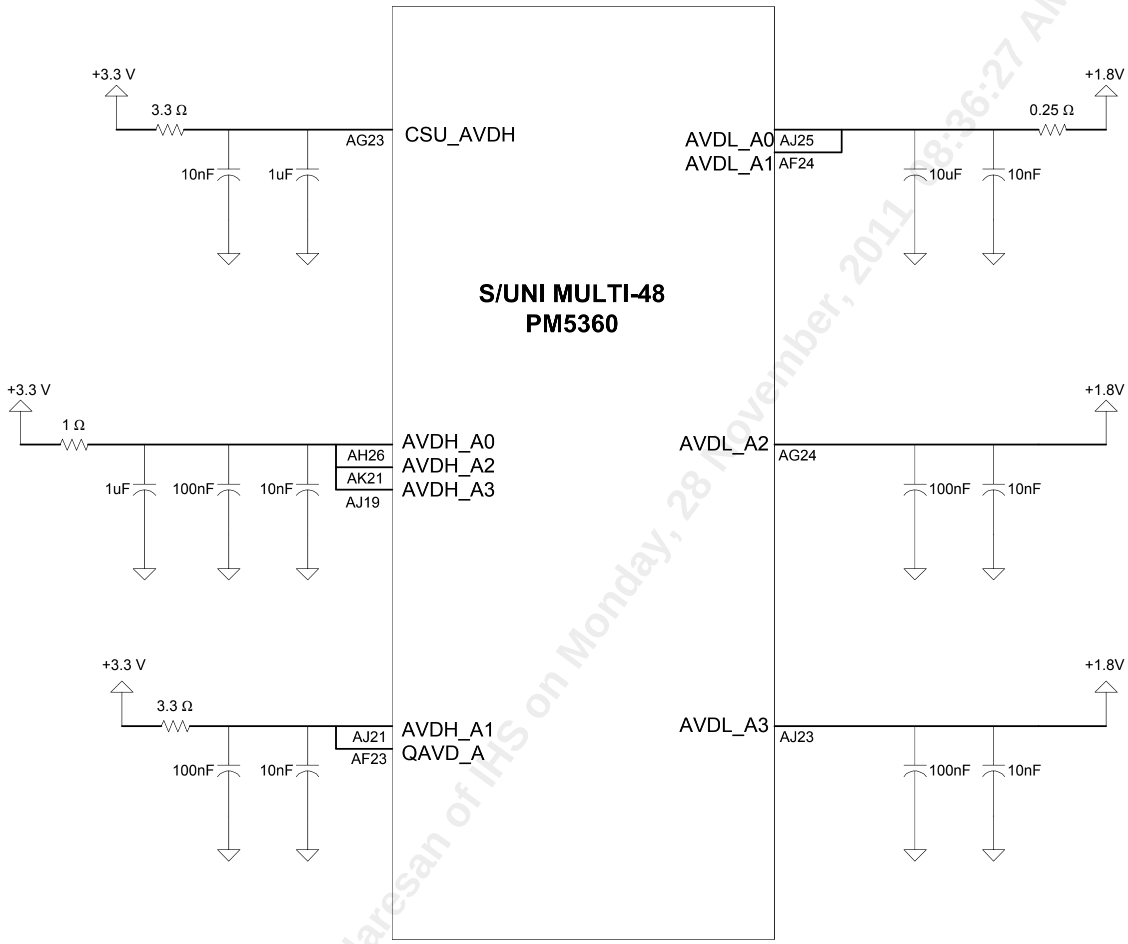


Figure 34 APS Analog Power Supply Filtering



Note that the APS analog power supply filtering can be dropped if the APS port is not used. When the APS port is not used, APS analog blocks should be powered down appropriately. APS analog blocks can be powered down using their individual enable bits. These bits are located in the R8TD APS Analog Control 1 register (0283H), CSTR Control register (0290H) and T8TE APS Analog Control register (1285H).

13.3 Power Up/Down Sequence

Due to ESD protection structures in the pads, it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions, it is possible to blow these ESD protection devices or trigger latch up.

The recommended power supply sequencing is as follows:

1. Supply 3.3V power either before 1.8V power or simultaneously with 1.8V power.

2. Drive I/Os after all the supplies have been powered.

3. Power down the device in the reverse sequence.

Notes:

- Analog is very tolerant of noise - no regulator required.
- On any board, there is always a delay between different devices activating. Therefore, the S/UNI MULTI-48 device can sustain +/-100 ma drive on its input pins for up to 100 ms while powering up.

13.4 Device Initialization

13.4.1 Device Reset

The reset pin of the S/UNI MULTI-48 device (RSTB – active low) should be asserted for at least 2 ms to initiate a complete initialization or re-initialization of the device. While RSTB is held low (logic 0), both the digital and the analog portions of the chip are reset. During active hardware reset, the CSB input pin must be high.

Users may elect to reset the S/UNI MULTI-48 device using register bits. This is accomplished by writing to the S/UNI MULTI-48 Master Software Resets Register (register 0003H).

After digital reset, and before starting any software routines to capture performance monitor count values, a write to register 0002H should be executed to initiate a global performance monitor count update. Then, the TIP bit in register 0002H should be monitored after approximately 105ns. If it is logic 1, a software reset (done by setting and then clearing DRESET in register 0003H) should be done to clear a TIP lock-up condition. Repeat this sequence until TIP is read to be logic 0.

13.4.2 Register Initialization

There are several registers in the S/UNI MULTI-48 whose initial values must be overwritten for proper device functioning. All “Reserved0” bits must be set to logic 0. All “Reserved1” bits must be set to logic 1. Other bits also state the needed value in their description. Refer to the different register descriptions for details.

13.5 Programming the Line Side Configuration Registers

When the S/UNI MULTI-48 is reset, when its line side analog blocks are reset or whenever the line side mode changes, the proper line side analog initilization sequence must be used to configure the line side analog blocks correctly. The following section describe the needed configuration sequences based on line side mode.

13.5.1 STS-48/STM-16 Line Side Mode of Operation

To configure the device into 1x2488 mode, the user needs to configure the 1x2488 line side SERDES blocks in normal operation mode and the 4x622/155 line side SERDES blocks in power down mode. The device STS48EN pin (XORed with STS48ENB register bit) determines which SERDES is active. As long as the STS48EN XOR result is logic 1, the SERDES 4x622/155 blocks will be automatically powered down to save power and the SERDES 1x2488 will be powered up in normal mode. STS-48/STM-16 line side mode of operation must be configured using the following steps:

1. Set the STS48EN pin (XOR'ed with STS48ENB register bit) to logic 1.

2. Reset the device. If the STS48ENB register bit is used to invert the value of the STS48EN pin (or if software reset is preferred), complete device reset must be replaced, minimally, by the following step:

   - Use the ARST_1X2488 bit from register 0003H to reset the SERDES 1x2488 analog blocks.

3. Set all "Reserved0" and "Reserved1" bits to their intended values.

4. Set TDCLK48EN register bit of STLI Clock Configuration register (1040H) to logic 1.

Notes:

- Other settings can keep their default values.
- When line configuration is over, wait for at least 5 ms before configuring the device registers.
- Note that whenever the 2488 link is unused, it should always have its analog blocks powered down, following the procedure described in step 5, Section 13.5.2.

13.5.2 Quad STS-12/STM-4 or STS-3/STM-1 Line Side Mode of Operation

To configure the device into quad 622/155 mode, the user needs to configure both the 1x2488 line side SERDES blocks and the 4x622/155 line side SERDES blocks in normal mode to use the 1x2488 analog receiver and transmitter for quad mode channel 1. To save power, the rest of the Rx and Tx 1x2488 analog sections need to be powered down. Quad STS-12/STM-4 or STS-3/STM-1 line side mode of operation must be configured using the following steps:

1. Set the STS48EN pin (XOR'ed with STS48ENB register bit) to logic 0.

2. Reset the device. If the STS48ENB register bit is used to invert the value of the STS48EN pin (or if software resets are preferred), complete device reset must be replaced, minimally, by the following step: Use the ARST_4x622, RST_LAS4x622, RST_JAT622 and DRST_DCRU155_622 bits from register 0003H to manually reset the SERDES 4x622/155 blocks.

3. Set all "Reserved0" and "Reserved1" bits to their intended values.

4. Select the proper setting between STS-12/STM-4 or STS-3/STM-1 mode for each of the links using RSTS12EN[4:1] and TSTS12EN[4:1] fields in register 0004H, S/UNI MULTI-48 Master Configuration Register #1. These bits must be set to logic 1 for each STS-12/STM-4 link, and to logic 0 for each link configured in STS-3/STM-1 mode.

5. Power down the unused Rx and Tx 2488 analog blocks:
   - Write a logic 0 in the CRU_ENABLE register bit of the RX2488 Analog CRU Control register (0022H). RX2488_ENABLE bit must keep its logic 1 value unless receive line link 1 is unused. If line link 1 is unused, RX2488_ENABLE must also be set to logic 0.
   - Write a logic 0 in the CSU_ENABLE, C2C_ENABLE and RX_REF_ENABLE register bits of the TX2488 ABC Control register (1021H). TX2488_ENABLE bit must keep its logic 1 value unless transmit line link 1 is unused. If line link 1 is unused, TX2488_ENABLE must also be set to logic 0.
6. Power down the unused 155/622 links. Write a logic 1 in the CHAN_ENB bit of the unused links Quad 622 Rx MABC Channel Control Register (0035H 0435H 0835H 0C35H).
7. If receive line link 1 is used, write a logic 1 in the SLICE1_RX622_EN bit of register 0022H (Rx2488 Analog CRU Control).
8. If transmit line link 1 is used, write TX2488_MODE[2] bit in register 1020H (Tx2488 Analog Control/Status) to logic 1.
9. Wait for 7ms.
10. Clear the PWRDN bit in the JAT622 Powerdown registers (1063H 1463H 1863H 1C63H) for all slices except for the unused line links, which should keep their powered down value.

This procedure for quad STS-12/STM-4 mode ends here. If one or more line links are STS-3/STM-1, add the following steps:

11. Write the proper value to the DCRU155_622EN[4:1] field of register 001DH (S/UNI MULTI-48 Miscellaneous Defect Configuration #4). These bits must be set to logic 1 for each link configured in STS-3/STM-1 mode.
12. Set the JAT_RATE[1:0] field of the Quad 622 Tx MABC and JAT622 Channel Control and Status Register (1033H 1433H 1833H 1C33H) to “01” for all STS-3/STM-1 links.
13. Remove the DCRU power down by writing a logic 0 in the PWRDN bit of the DCRU155_622 Powerdown register (0383H 0783H 0B83H 0F83H) for all STS-3/STM-1 links.

Notes:

- Other settings can keep their default values.
- When line configuration is over, wait for at least 5 ms before configuring the device registers.
- Any unused link should always have its analog blocks powered down using the description of the power down bits as stated in steps 5, 6, 10 and 13.

13.6 Preventing Errors Due to Unstable Clocks

Clock glitches and out-of-specification clocks can cause corruption of data and control bits due to timing violations. Two cases can produce unstable clocks and require software intervention: SYSCLK_EN value change and line side initialization.

13.6.1 SYSCLK_EN value change

Whenever the SYSCLK_EN bit value is changed (register 0016H), software must do the following:

- Reset SONET blocks (SBER, RRMP, RTTPs, RHPP, RSVCA, TSVCA, SARC, TTTPs, THPP, TRMP, PRGM, SIRP) using RESETSL[4:1] (register 0003H);
- Reset the SYSTEM side blocks (RSTSI, RCAS12, RCFP, RTDP, RXSDQ, RXPHY, TSTSI, TCAS12, TCFP, TTDP, TXSDQ, TXPHY) using SYS_RESET (register 001CH);
- Re-configure the affected SONET and system blocks with the proper settings.

13.6.2 Line Side Initialization

Line side initialization (or re-initialization) must occur any time the S/UNI MULTI-48 is reset, its line side analog blocks are reset or its line side mode changes. After the line side analog blocks initialization sequence is run, software must do the following:

- Reset SONET blocks (SBER, RRMP, RTTPs, RHPP, RSVCA, TSVCA, SARC, TTTPs, THPP, TRMP, PRGM, SIRP) using RESETSL[4:1] (register 0003H);
- Re-configure the affected SONET blocks with the proper settings.

13.7 Interrupt Service Routine

The S/UNI MULTI-48 device will assert INTB to logic 0 when a condition which is configured to produce an interrupt occurs. To find which condition caused this interrupt, follow the procedure outlined below:

1. Read the S/UNI MULTI-48 Master Interrupt Status #1-#8 registers (000BH – 0012H). The bits point to the functional block(s) which caused the hardware interrupt. For instance, if the RXSDQ block caused the interrupt, the RXSDQI bit will be logic 1 in register 000FH. These bits get cleared when the interrupt is cleared.
2. Find the register address of the corresponding block which caused the interrupt and read its Interrupt Status registers. The interrupt functional block and interrupt source identification register bits from steps 1 and 2 are cleared once this register has been read (or written with a logic 1 when WCIMODE is set to logic 1) and the interrupt(s) identified.
3. Service the interrupt(s).
4. If the INTB pin is still logic 0, then there are still interrupts to be serviced and steps 1 to 3 need to be repeated. Otherwise, all interrupts have been serviced. Wait for the next assertion of INTB.

13.8 Accessing Indirect Registers

Indirect registers are used to conserve address space in the S/UNI MULTI-48 device. Indirect registers are accessed by writing to the indirect address register. Use the following steps when writing to indirect registers:

1. Read the BUSY bit. If it is equal to logic 0, continue to step 2. Otherwise, continue polling the BUSY bit.

2. Write the desired configurations for the channel into the indirect data register(s).

3. Write the channel number (indirect address) to the indirect address register with RWB set to logic 0.

4. Read BUSY. Once it equals 0, the indirect write has been completed.

The following steps should be followed for reading indirect registers:

1. Read the BUSY bit. If it is equal to logic 0, continue to step 2. Otherwise, continue polling the BUSY bit.

2. Write the channel number (indirect address) to the indirect address register with RWB set to logic 1.

3. Read the BUSY bit. If it is equal to logic 0, continue to 4. Otherwise, continue polling the BUSY bit.

4. Read the indirect data register(s) to find the state of the register bits for the selected channel number.

Note: the TXSDQ and RXSDQ are handled somewhat differently than most functional blocks with indirect registers. The TXSDQ and RXSDQ have several Indirect Data Registers – though only one Indirect Address register that controls them all. See the TXSDQ and RXSDQ register description for more information.

The SARC's indirect registers are also programmed in a slightly different manner. See Section 10.7 for more details.

A particular idiosyncracy should be noted for the SVCA's indirect registers. When configured for concatenated payloads, the value written to SVCA indirect register 2 (diagnostics reg) of a master timeslot gets propagated to (overwrites) the indirect register 2 values of all slave timeslots associated to the master timeslot (within the SVCA where the indirect write was performed). Similarly, when the payload is changed to a higher concat level (eg. 4xSTS-3c to STS-12c), the value previously present in the master timeslot is propagated to (overwrites) the values in the slave timeslots without any indirect write actions being performed. When the payload is changed back to a lower concatenation level, the new SVCA indirect register 2 values remain and the old ones are lost. The same behavior is observed when writing to indirect register 2 of timeslot 1 (the de-facto master) of an SVCA configured as a STS-12 slave of an STS-48c payload.

13.9 Using the Performance Monitoring Features

The performance monitor counters within the different blocks are provided for performance monitoring purposes. The TCFP, TTDP, RCFP, RTDP, R8TD, RXSDQ, TXSDQ, RHPP, RRMP, RSVCA, TSVCA and PRGM blocks all contain performance monitor registers. The counters have been sized to not saturate if polled every second.

Each block's counters can be accumulated independently if one of the registers which contain the latched counter values is written to. A device update of all the counters can be done by writing to the S/UNI MULTI-48 Global Performance Monitor Update register (register 0002H). After this register is written to, the TIP bit in this register can be polled to determine when all the counter values have been transferred and are ready to be read.

13.10 Configuring SONET/SDH Payload from a Concatenated Stream to a Channelized Stream

When configuring SONET/SDH payload from a concatenated stream to a channelized stream (previously slave timeslots becoming master timeslots), the following procedure must be applied. After payload configuration:

1. Set the Diag_NDFREQ (bit 5) to logic 1 in R/TSVCA Diagnostic/Configuration indirect register 02H for all new master timeslots.

2. Clear the Diag_NDFREQ (bit 5) to logic 0 in R/TSVCA Diagnostic/Configuration indirect register 02H for all new master timeslots.

13.11 Loopback Operation

The S/UNI MULTI-48 provides four loopback modes : line side line loopback, serial diagnostic loopback, parallel diagnostic loopback and cell/packet loopback. Note that, in all loopback configurations, the data is also propagated towards its standard path.

Line Side Loopback

The Line Side Line Loopback connects the receive data stream to transmit data stream in the SerDes blocks. The loopback datapath includes the internal clock recovery and clock synthesis but excludes all of the SONET frame processing. In this mode, the entire receive path is operating normally. To have the line side line loopback operate properly, the user has to enable the LOOPTIME mode or guarantee the reference clock frequency is locked to the receive data frequency.

In 2488 mode, the loopback is enabled by setting LINE_LOOP_BACK bit in register 0023H and the SLLE2488 register bit in register 1020H to logic 1. The 2488 looptime mode is enabled by configuring the LOOPTIMEB, CSU_MODE[6:3] and CSU_MODE[1] bits to logic 0, and CSU_MODE[0] to logic 1, in register 1021H.

In quad 622/155 mode, it is enabled by setting SLLE622 and LOOPT to logic 1 in registers 1033H, 1433H, 1833H, 1C33H for quadrants 1, 2, 3, and 4 respectively. Once the line loopback mode is enabled, the loopback FIFO should be reset by toggling the FRST bit in register 1061H, 1461H, 1861H, 1C61H for quadrants 1, 2, 3, and 4 respectively. This FRST bit should also be toggled whenever there's a FERRI interrupt (register 1062H 1462H 1862H 1C62H) under normal receive line conditions (no SD, LOS/LOT nor DOOL defect). Note that the corresponding SONET_EN[X] bit(s) from register 001CH (S/UNI MULTI-48 Miscellaneous Defect Configuration #3) must be set to logic 1 when line loopback is enabled in 622 mode.

Serial Diagnostic Loopback

Serial Diagnostic Loopback enables a loopback from the transmit 2.488 Gbit/s serial line to the receive 2.488 Gbit/s serial line in 2488 mode or from each transmit 622/155 Mbit/s serial line to the corresponding receive 622/155 Mbit/s serial line. In 2488 mode, it is enabled by setting the SDLE2488 bit high in register 0022H. In quad 622/155 mode, it is enabled by setting the SDLE622 bit high in registers 0035H 0435H 0835H 0C35H. **Note** that both SD_EN bit in SFBA Configuration and Status register and DCC_ENB bit in DCRU155_622 Configuration register must be set to logic 0 when in Serial Diagnostic Loopback mode for slices where DCRU155_622 is enabled (DCRU155_622EN[x]).

Parallel Diagnostic Loopback

Parallel Diagnostic Loopback enables a digital loopback from the transmit line to the receive line before the SerDes analog circuitry. In 2488 mode, it is enabled by setting the PDLB bit high in register 0008H. In quad 622/155 mode, it is enabled independently for each quadrant by setting the proper PDLB[4:1] bits in register 0008H.

Cell/Packet Loopback

Cell/Packet Loopback enables a digital loopback from the Transmit Channel Assigner block (TCAS12) to the Receive Channel Assigner block (RCAS12) on a per cell/packet channel basis. Up to 16 cell/packet channels can be independently looped from the transmit UL3/PL3 cell/packet streams to the receive UL3/PL3 interface. Cell/packet loopback is enabled using the CHx_LBEN and STS12C_LBEN register bits from register 0361H (RCAS12 Channel Loopback Enable). When looping an STS-12c (VC-4-4c) channel or part of an STS-48c (VC-4-16c) channel, only CH0_LBEN and STS12C_LBEN should be set to logic 1. When looping sub-STS-12c (VC-4-4c) channels, only the individual CHx_LBEN bits should be set to logic 1, depending on what channels are in loopback mode.

13.12 Invalid Receive Line Timing Recovery

Under certain loss of signal (SD, LOS/LOT) or excessive incoming frequency drift (DOOL) conditions, the receive line clock recovery unit can output a line rate clock that is not locked to any external reference (REFCLK155 or REFCLK77) for keep-alive purposes. In these cases, the recovered clock frequency can drift out of the +/- 20 PPM frequency range. The transmit line data rate in loop-time mode and the RCLKO output frequency will thus be directly affected depending on the following conditions:

STS-48/STM-16 mode:

- SD, LOS defects: Both RCLKO and loop-timed transmit line data rate will automatically switch to external timing (locked on REFCLK155). No action required.

- DOOL defect: Loop-timed transmit line data rate will automatically switch to external timing (locked on REFCLK155). No action required.
  RCLKO can drift out of the +/- 20 PPM frequency range. Manual timing reference switch could be required for applications needing RCLKO to be within the +/- 20 PPM frequency range.

STS-12/STM-4 mode:

- SD/LOS/DOOL defects: Both RCLKO and loop-timed transmit line data rate can drift out of the +/- 20 PPM frequency range. Manual timing reference switch (such as getting out of loop-time mode) could be required for applications needing RCLKO or transmit line data rate to be within the +/- 20 PPM frequency range.

STS-3/STM-1 mode:

- LOT defect: Both RCLKO and loop-timed transmit line data rate can drift out of the +/- 20 PPM frequency range. Manual timing reference switch (such as getting out of loop-time mode) could be required for applications needing RCLKO or transmit line data rate to be within the +/- 20 PPM frequency range.
  Note: There is no DOOL defect equivalent in STS-3/STM-1 mode. LOF monitoring could thus be used, along with LOT, to trigger manual timing reference switching due to high incoming frequency drift.

13.13 Using The Section/Line Bit Error Rate Monitoring Features

The Bit Error Rate Monitor (SBER) block counts and monitors line BIP errors over programmable periods of time (window size). It can declare an alarm or clear an alarm if the alarm is already set. A different threshold must be used to declare or clear the alarm, whether or not those two operations are performed at the same BER. Table 32 and Table 33 list the recommended content of the SBER registers for different line rates (STS-N) and error rates (BER). Both BER monitors in the SBER are equivalent and are programmed similarly. In a normal application, they will be set to monitor different BER.

When the SF/SD CMODE bit is 1, this indicates that the monitor will use an alarm clearing window size that is eight times longer than the declaration window size. When the SF/SD CMODE bit is 0, this indicates that the monitor will use an alarm clearing window size that is equal to the declaration window size. In both cases, the clearing threshold is calculated for a BER that is 10 times lower than the declaration BER, as required in the references. Table 32 and Table 33 indicate the declare BER, the evaluation period, and the recommended CMODE and associated thresholds.

The saturation threshold is not listed in the tables. It is programmed with the value 0xFFFFFF by default, deactivating saturation. Saturation capabilities are provided to allow the user to address issues associated with error bursts. It enables the user to determine a ceiling value at which the error counters will saturate, letting error bursts pass through within a frame or sub window period.

Since the monitoring algorithm is based on a pseudo-sliding window containing eight sub intervals, the time required to declare or clear an alarm can take up to nine sub-accumulation periods (SAP). Table 32 and Table 33 thus consider that each SAP must take a value lower or equal to $1/9^{th}$ of the timing constraint, in frames.

Table 32 Recommended SBER Settings for Different Data and BER Rates Using Telcordia Objectives

OC	Monitored Declare BER	Objective met for Switching Time (s)	SF/SD CMODE	SF/SD SAP (hex)	SF/SD DECTH (hex)	SF/SD CLRTH (hex)
3	10^{-3}	0.008	0	00000007	0001FB	000074
3	10^{-4}	0.013	0	0000000B	000088	000018
3	10^{-5}	0.100	0	00000058	000073	000014
3	10^{-6}	1.000	0	00000378	000075	000014
3	10^{-7}	10.000	0	000022B8	000075	000014
3	10^{-8}	83.000	0	00012031	00005F	000011
3	10^{-9}	667.000	0	00090BF8	00004B	00000F
12	10^{-3}	0.008	0	00000007	000828	0001AE
12	10^{-4}	0.008	0	00000007	00016E	000036
12	10^{-5}	0.025	0	00000016	000073	000014
12	10^{-6}	0.250	0	000000DE	000075	000014
12	10^{-7}	2.500	0	000008AE	000075	000014
12	10^{-8}	21.000	0	000048EA	000061	000012
12	10^{-9}	167.000	0	000243DC	00004B	00000F
48	10^{-3}	0.008	0	00000007	002116	000677
48	10^{-4}	0.008	0	00000007	0005F8	0000C1
48	10^{-5}	0.008	0	00000007	000095	000019
48	10^{-6}	0.063	0	00000037	000074	000014
48	10^{-7}	0.625	0	0000022B	000075	000014
48	10^{-8}	5.200	0	0000120E	000060	000011
48	10^{-9}	42.000	0	000091D5	00004C	00000F

Table 33 Recommended SBER Settings for Different Data and BER Rates Using Telcordia and ITU Requirements

OC	Monitored Declare BER	Requirement met for Switching Time (s)	SF/SD CMODE	SF/SD SAP (hex)	SF/SD DECTH (hex)	SF/SD CLRTH (hex)
3	10^{-3}	0.01	0	00000008	000238	00008A
3	10^{-4}	0.10	0	0000002B	00022B	000055
3	10^{-5}	1.00	0	00000192	00022B	000051
3	10^{-6}	10.00	0	00000F98	00022B	000050
3	10^{-7}	100.00	0	00009BD6	00022B	000050
3	10^{-8}	1,000.00	0	00061647	00022B	000050
3	10^{-9}	10,000.00	0	003CDEAD	00022B	000050
12	10^{-3}	0.01	0	00000008	00093C	0001F7
12	10^{-4}	0.10	0	0000002B	00091D	00012C
12	10^{-5}	1.00	0	00000192	000922	00011C
12	10^{-6}	10.00	0	00000F98	000922	00011B
12	10^{-7}	100.00	0	00009BD6	000922	00011A
12	10^{-8}	1,000.00	0	00061647	000922	00011A
12	10^{-9}	10,000.00	0	003CDEAD	000922	00011A
48	10^{-3}	0.01	0	00000008	0025A5	00077B
48	10^{-4}	0.10	0	0000002B	002554	000465
48	10^{-5}	1.00	0	00000192	00256F	000426
48	10^{-6}	10.00	0	00000F98	002570	000420
48	10^{-7}	100.00	0	00009BD6	002571	00041F
48	10^{-8}	1,000.00	0	00061647	002571	00041F
48	10^{-9}	10,000.00	0	003CDEAD	002571	00041F

Important Note:

The user should NOT use CMODE = 1 mode when working with Telcordia or ITU requirements for the evaluation periods. In that case, the clearing time (eight times declare time) would not conform to the requirements (where clearing time requirement = declare time requirement). For the same reason, the user should also avoid using CMODE = 1 with Telcordia objectives when the detection threshold = 10^{-3}.

The user should note that a probability of 99% was assumed as the probability that the switch initiation time (declaring) is below the Telcordia requirement. Since the Telcordia specification is vague regarding this issue ("must be very close to 1.0"), the approximation with 0.99 is sufficient and lets the Telcordia requirements be identical to the ITU requirements.

The user should also note that the Telcordia objectives are stricter than Telcordia and ITU requirements upon detection and clearing times. But Telcordia and ITU requirements are stricter than Telcordia objectives upon detection and clearing probability for a given BER (99% vs 95% for Telcordia objectives).

13.14 Using The Receive Trail Trace Processor Features

The RTTP monitors a one-byte, 16-byte, or 64-byte trail trace message. To monitor a one-byte message, the ALGO register bits must be set to 11 (algo3). The trail trace byte is captured at address 40H. To monitor a 16-byte message, the ALGO register bits must be set to 01/10 (algo1/2) and the LENGTH16 register bit must be set to logic one. The trail trace message is captured between the 40H and 4FH addresses. To monitor a 64-byte message, the ALGO register bits must be set to 01/10 (algo1/2) and LENGTH16 register bit must be set to logic zero. The trail trace message is captured between the 40H and 7FH addresses.

When SYNC_CRLF is low, the synchronization is based on the MSB of the trail trace byte. Only one of the bytes has its MSB set high. The byte with its MSB set high is the first byte of the message. When SYNC_CRLF is high, the synchronization is based on the CR/LF (CR = 0Dh, LF = 0Ah) characters of the trail trace message. The byte following the CR/LF bytes is the first byte of the message.

Figure 35 1-Byte Trail trace Message

ALGO = 11

1st BYTE		40H, 80H, C0H

Figure 36 16-Byte Trail trace Message, sync on MSB

ALGO = 01/10 , LENGTH16 = 1 , SYNC_CRLF = 0

1st BYTE	MSB SET HIGH	40H, 80H, C0H
2nd BYTE		41H, 81H, C1H
...		...
15th BYTE		4EH, 8EH, CEH
16th BYTE		4FH, 8FH, CFH

Figure 37 16-byte Trail trace Message, sync on CR/LF

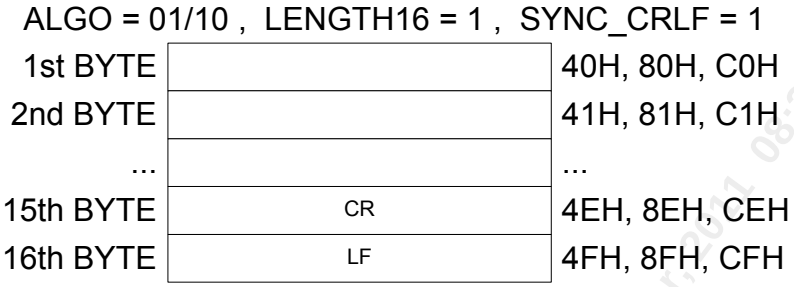


Figure 38 64-Byte Trail trace Message, sync on MSB

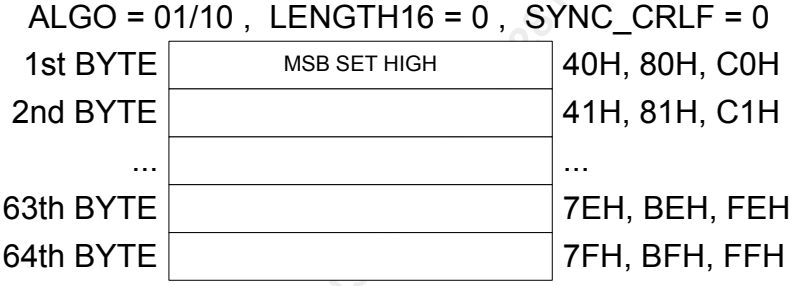
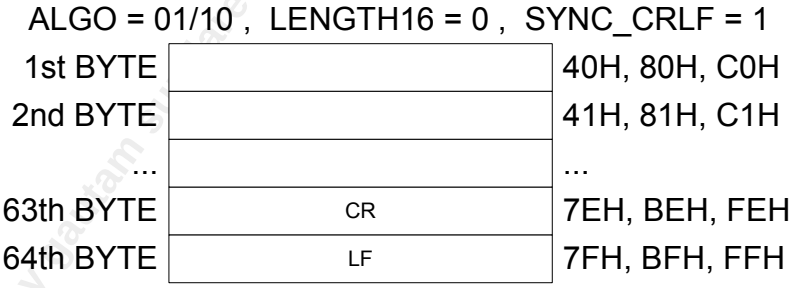


Figure 39 64-Byte Trail trace Message, sync on CR/LF



To avoid declaring an unstable/mismatch defect when the transmitter updates the trail trace message, the RTTP considers an all zeros message to be matched. An all-zeros captured message in algorithm 1 and an all-zeros accepted message in algorithm 2 are not validated against the expected message but are considered match. That is, a match is declared when the captured or accepted message is all zeros regardless of the expected message. This feature can be turned off by setting the ZEROEN register bit to logic one.

Note: The transmitter is required to force an all zeros trail trace message when the trail trace message is updated.

13.15 Using the Transmit Trail trace Processor

The TTTP generates a one-byte, 16-byte, or 64-byte trail trace message. To generate a one-byte message, the BYTEEN register bit must be set to logic one. The trail trace byte is placed at address 40H. To generate a 16-byte message, the BYTEEN register bit must be set to logic zero and the LENGTH16 register bit must be set to logic one. The trail trace message is placed between the 40H and 4FH addresses. To generate a 64-byte message, both the BYTEEN and the LENGTH16 register bits must be set to logic zero. The trail trace message is placed between the 40H and 7FH addresses.

The trail trace message must include synchronization because the TTTP does not add synchronization to the message. The synchronization mechanism is different for a 16-byte message and for a 64-byte message. When the message is 16 bytes, the synchronization is based on the MSB of the trail trace byte. Only one of the 16 bytes has its MSB set high. The byte with its MSB set high is the first byte of the message. When the message is 64 bytes, the synchronization is based on the CR/LF (CR = 0Dh, LF = 0Ah) characters of the trail trace message. The byte following the CR/LF bytes is the first byte of the message.

Figure 40 1-Byte Trail trace Message

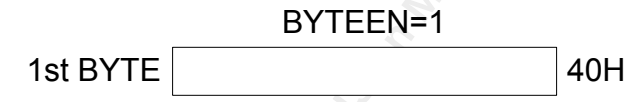
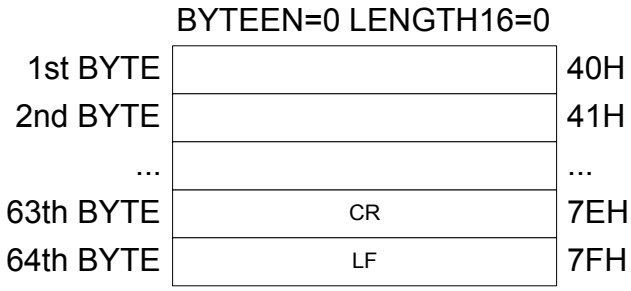


Figure 41 16-Byte Trail trace Message

Figure 42 64-Bytes Trail trace Message



To avoid generating an unstable/mismatch message, the TTTP can be configured (with the ZEROEN register bit) to generate an all-zeros trail trace message while the microprocessor updates the internal message. The enabling and disabling of the all-zeros message is not done on message boundary since the receiver is required to perform filtering on the message.

13.16 LCD Defect Processing and ERDI-P/REI-P Insertion

The Loss of Cell Delineation defect (LCD) is reported by the receive cell processors (RCFP/RTDP), in ATM mode only. The way this defect is handled towards proper transmit line ERDI-P insertion varies depending on the usage of the APS port. Transmit line REI-P and ERDI-P insertion in the G1 byte requires the use of many different blocks when dealing with LCD defects: RCFP, RTDP, RSTSI, TSTSI, RHPP, RTTP PATH, SARC, THPP and SIRP.

How these blocks interact depends on the datapath. There are two cases:

- Standard datapath: from/to the line side to/from the PL3/UL3 side, within a single device;
- APS datapath: from/to the line side of one device to/from the PL3/UL3 side of a second device, via the APS port.

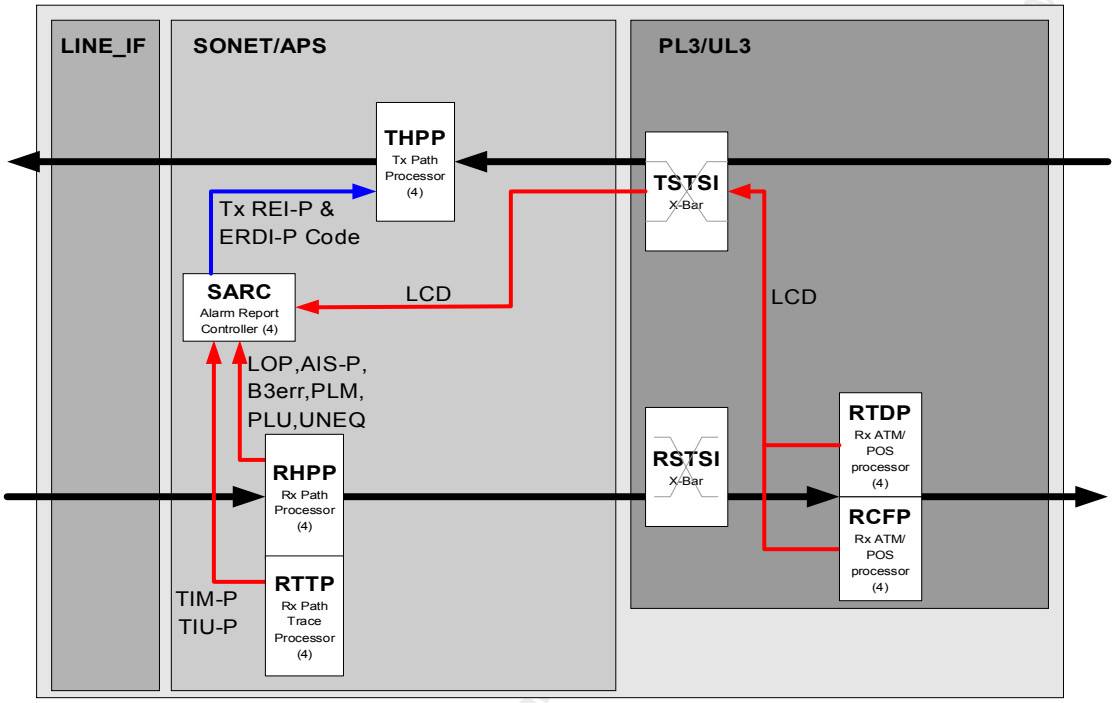
13.16.1 Standard Datapath LCD Defect Processing

When all ERDI-P related defects are monitored within the same device, here are the needed blocks and their role in the insertion of valid transmit line ERDI-P and REI-P codes:

- RCFP/RTDP: Report LCD defects based on the received ATM stream (after any RSTSI timeslot remapping).
- TSTSI: Optionally remaps LCD defects to the proper timeslots.
- RHPP: Reports LOP, AIS-P, PLU, PLM and UNEQ defects and B3 errors.
- RTTP PATH: Reports TIM-P and TIU-P defects.
- SARC: Processes defects and generates the proper (E)RDI-P and REI-P codes towards the THPP block.
- THPP: Inserts the (E)RDI-P and REI-P codes in the transmit line G1 byte.

Figure 43 illustrates how the defects are handled towards proper transmit line REI-P and (E)RDI-P insertion in a standard datapath ATM configuration.

Figure 43 LCD defect processing: standard datapath



For this configuration to behave properly, the following register settings should be applied:

- THPP POH insertion must be enabled. THPP indirect register 00H, bit 5 (TDIS) should be set to logic 0 for all master timeslots.
- (E)RDI-P and REI-P codes insertion in the G1 byte should be enabled in the THPP. THPP indirect register 01H, bit 0 (IBER) must be set to logic 0 and bit 11 (ENG1REC) should be set to logic 1 for all master timeslots.

Note: The LCD defect is declared in the RCFP/RTDP after data passed through the RSTSI X-BAR, thus it must always pass through a symmetrical TSTSI X-BAR.

This standard way of inserting the (E)RDI-P and REI-P codes in the transmit G1 byte using the THPP block should be used whenever one of the following conditions apply:

- APS port is not used (all defects are declared in the same device).
- Cell processors are configured in packet mode (no possible LCD).
- One does not want to include LCD defects in the ERDI-P code calculation.
- RDI-P encoding is enabled (PRDIEN is set to logic 1, register 0268H: SARC Path Configuration; TSx_ERDI is set to logic 0, register 1260H: SIRP Timeslot Configuration). As opposed to ERDI-P encoding, LCD is not considered for RDI-P.

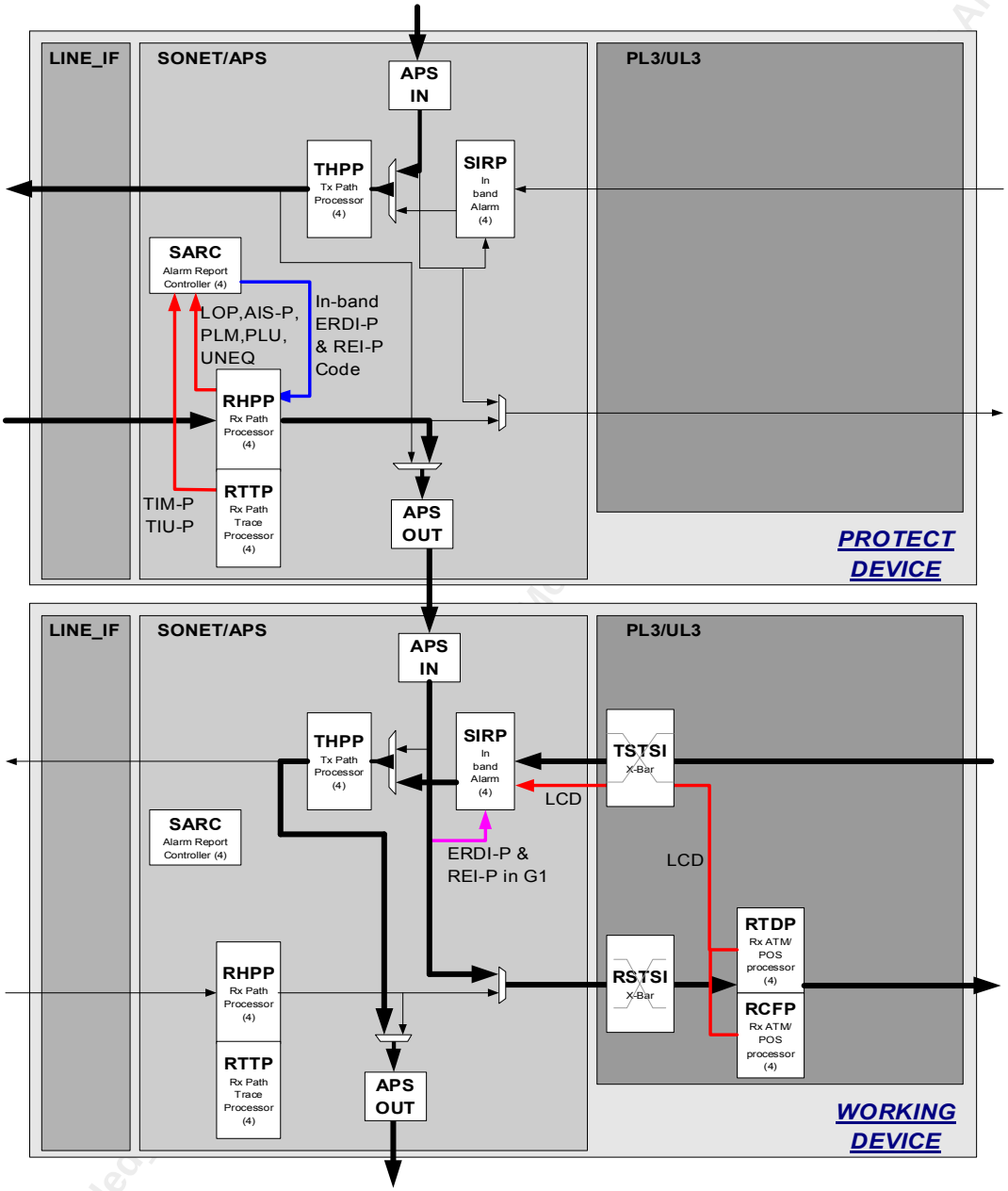
13.16.2 APS Datapath LCD Defect Processing

When LCD is not monitored within the same device as the SONET/SDH related defects (such as in a working/protect configuration using APS), here are the needed blocks and their role in the insertion of valid transmit line ERDI-P and REI-P codes:

- RCFP/RTDP (working): Report LCD defects based on the received ATM stream (after any RSTSI timeslot remapping).
- TSTSI (working): Optionally remaps LCD defects to the proper timeslots.
- RHPP (protect): Reports LOP, AIS-P, PLU, PLM and UNEQ defects and B3 errors; inserts inband ERDI-P and REI-P codes.
- RTTP PATH (protect): Reports TIM-P and TIU-P defects.
- SARC (protect): Processes defects and generates the proper ERDI-P and REI-P codes towards the RHPP block.
- SIRP (working): Snoops the APS In data to recover the ERDI-P and REI-P codes inserted by the protect RHPP. Modifies the ERDI-P code depending on comparisions with the received LCD defects status. Inserts the final ERDI-P and REI-P codes in the transmit line G1 byte.

Figure 44 illustrates how the defects are handled towards proper transmit line REI-P and ERDI-P insertion in an APS datapath ATM configuration.

Figure 44 LCD defect processing: APS datapath



For this configuration to behave properly, the following register settings should be applied:

- RHPP inband ERDI-P insertion must be enabled in the protect device. Protect RHPP indirect register 01H, bit 9 (IBER) should be set to logic 1 for all master timeslots.
- THPP POH insertion should be disabled (pass through mode) in the working device because its functionality is duplicated by the downstream protect THPP. Working THPP indirect register 00H, bit 5 (TDIS) should be set to logic 1 for all master timeslots.
- THPP G1 byte insertion should be disabled (G1 passed through) in the protect device. Protect THPP indirect register 01H, bit 0 (IBER) must be set to logic 1 for all master timeslots.

Note: The LCD defect is declared in the working RCFP/RTDP after data passed through the working RSTSI X-BAR, thus it must always pass through a symmetrical working TSTSI X-BAR.

This defect processing scheme implying SIRP usage and inband ERDI-P and REI-P insertion in the RHPP block is only required if all the following conditions apply:

- APS port is used (all defects are not declared in the same device).
- Cell processors are configured in ATM mode.
- One does want to include LCD defects in the ERDI-P code calculation.
- ERDI-P encoding is enabled (PRDIEN is set to logic 0, register 0268H: SARC Path Configuration; TSx_ERDI is set to logic 1, register 1260H: SIRP Timeslot Configuration). As opposed to RDI-P encoding, LCD is considered for ERDI-P.

Note: When all these conditions apply and SIRP must be used to insert proper transmit line ERDI-P and REI-P codes, downstream AIS-P insertion must be disabled in order not to overwrite the inband ERDI-P and REI-P codes inserted by the protect RHPP. Register 026AH (SARC Path RPAISINS Enable) should be set to 0000H for all master timeslots.

13.17 APS Interface Operation

The LVDS APS Ports implement the 777.6 Mbit/s LVDS links. A reference clock of 77.76 MHz is sourced from the SYSCLK pin or is derived from the REFCLKx pins. When connecting two devices via the APS ports, the clock feeding both APS ports must be frequency locked.

For the APS interface to work properly, the 8B/10B encoder (T8TE) must be set in HPT mode.

There are 3 possible APSIFP pin usage schemes:

- When both SYSCLK_EN (register 0016H) and APSIFP_EN (register 0015H) register bits are logic 1, the APSIFP pin signal is considered synchronous to SYSCLK and sampled accordingly.

- When SYSCLK_EN (register 0016H) is logic 1 and APSIFP_EN (register 0015H) is logic 0, the APSIFP pin signal has no relation with the SYSCLK pin signal so the S/UNI MULTI-48 device detects its rising edges in order to align APS data.
- Whenever APSIFP_EN (register 0015H) is logic 0, the APSIFP pin is not used and S/UNI MULTI-48 device will rely on an internally generated frame pulse.

The S/UNI MULTI-48 supports two APS port synchronization mechanisms. The first mechanism uses a common distributed 8 KHz frame pulse and the second relies on a software algorithm to achieve synchronization between mate APS ports.

13.17.1 Receive APS Port Synchronization

This APS synchronization method can only be used when the APSIFP pin is used (APSIFP_EN is logic 1). This method uses knowledge of the inter-links skew to calculate the needed setting for APS port syncronization.

A timing pulse (APSIFP pin) for SONET frames must be generated and fed to each device. This timing pulse can be synchronous to the SYSCLK pin signal (when SYSCLK_EN is logic 1) or rising edge detected (when SYSCLK_EN is logic 0). Each S/UNI MULTI-48 device has an input frame delay register field (AIJ0DLY), which contains the number of 77.76 MHz clock cycles that a device should use to align the timing pulse with the APS framing character K28.5 of the STS-12 frame. This signal is used to instruct the ingress load devices to start emitting an STS-12 frame (with its special “J0” control character) at that time. The ingress FIFOs permit a variable latency in K28.5 arrival of up to 16 clock cycles. That is, the largest tolerable delay between the slowest and fastest LVDS link is 16 8B/10B characters. Consequently, the external system must ensure that the relative delays between all four receive LVDS links be less than 16 8B/10B characters. The minimum value for the internal programmable delay (AIJ0DLY[13:0]) is the delay to the last (slowest) J0 character (including the delay inside the S/UNI MULTI-48 APS framing logic). The maximum value is the delay to the first (fastest) J0 character (including the delay inside the S/UNI MULTI-48 APS framing logic) plus 16 bytes. The actual programmed delay should be based on the delay of the “slowest” of the four links – the link in which J0 arrives last plus a small safety margin of 1 or 2 words. When this APS framing method is used, the needed AIJ0DLY value must be found using a trial and error routine. The magnitude of the clock cycle delay is bounded by two parameters. First, the programmed delay register AIJ0DLY is 14 bits. This implies that a clock cycle delay of $2^{14}-1$ or 16,383 clock cycles can be programmed. However, the second parameter, the frame rate (125 µs), bounds the delay to nearly one STS-12 frame or 9718 (9719 unique values but 0 is the value for no delay) clock cycles (125 µs x 77.76 MHz), after which the next SONET frame begins.

13.17.2 Receive APS Port SMART Framing

The receive APS smart framing must be used when no APSIFP is provided to the S/UNI MULTI-48 device, but can also be used in any APS configuration scheme. This procedure is the recommended method in all possible cases, regardless of the usage of the external SYSCLK or APSIFP pins. The receive APS smart framing method is a software based algorithm of synchronizing APS ports.

In a working/protect environment using two S/UNI MULTI-48 devices, software must start its smart framing routine by synchronizing the "working" device, and then the "protect" device, since the protect device configuration is dependant on the working device alignment. Note that, in a working/protect configuration, the working and protect AOJ0DLY_EN bits and protect AOJ0DLY value (register 0016H, S/UNI MULTI-48 APS Output TelecomBus Synchronization Delay) must be configured prior to any smart framing attempt.

To synchronize one S/UNI MULTI-48 APS port, the software driver must execute the following steps:

PART 1: Find used APS links

1. Write a delay of 0 in the AIJ0DLY[13:0] field of the S/UNI MULTI-48 APSIFP Enable and APS Input TelecomBus Synchronization Delay register (register 0015H).
2. Verify which APS links are used by monitoring the Rx APS J0 interrupts in register 0018H (S/UNI MULTI-48 Rx APS J0 FIFO Interrupt Status). To be considered used, an APS link must be receiving receiving sufficient J0 8B/10B codes. A link's corresponding EXJ0 or OKJ0 interrupts (register 0018H) should be asserted once a frame for at least 4 out of 5 consecutive frames. This can be verified using the standard interrupts service routine or by polling the EXJ0 and OKJ0 interrupt status bits once a frame for 5 frames. All links reporting only NOJ0 interrupts are deemed unused and must be eliminated from this procedure.

Because floating APS links could induce fake J0 8B/10B codes, R8TD interrupts must also be used to verify if a link is deemed "used". Using only the links considered "used" after step 1, follow the next steps:

3. Clear all used links R8TD interrupt status bits by either reading the S/UNI MULTI-48 R8TD APS Interrupt Status register (register 0281H 0681H 0A81H 0E81H), when WCIMODE is set to logic 0, or by writing logic 1 values to all R8TD interrupt status bits in the same register, when WCIMODE is set to logic 1.
4. Wait for a few us (10 us should be enough).
5. Read all used links R8TD out-of-character-alignment (OCA) and out-of-frame-alignment (OFA) status bits (OFAV, OCAV, register 0280H 0680H 0A80H 0E80H) and interrupt status bits (register 0281H 0681H 0A81H 0E81H) several (~10) times. Monitor for any asserted OCAV or OFAV status bits and for FUOI, LCVI, OCAI or OFAI interrupts. If no link reports any problem (OCA or OFA asserted states or FUO/LCV/OCA/OFA interrupts), all current "used" links should be considered used and routine should go directly to part 2. If one/some link(s) reported OCA/OFA asserted states or FUO/LCV/OCA/OFA interrupts, these links can't be considered used unless they pass a second test, as stated in the next steps.
6. Add 8 to the current AIJ0DLY field of the S/UNI MULTI-48 APSIFP Enable and APS Input TelecomBus Synchronization Delay register (register 0015H).
7. Wait for at least 5 frames.
8. Repeat steps 3 to 7, monitoring all links that are still considered "used" once again. Links that report OCA/OFA/LCV/FUO errors both times steps 3 to 7 are executed should be deemed unused (most probably floating). Remaining links are considered used.

The following steps must only target used APS links.

9. Find an AIJ0DLY value where no R8TD errors are reported.
   If none of the used links report OCA/OFA/LCV/FUO errors with the current AIJ0DLY value, go to part 2 without changing the current AIJ0DLY value.

   If one/some of the used links report OCA/OFA/LCV/FUO errors with the current AIJ0DLY value:
   Repeat until no more OCA/OFA/LCV/FUO errors are found over used links, then go to part 2:
   * Add 4 to the current AIJ0DLY value;
   * Wait for at least 5 frames;
   * Monitor for any asserted R8TD OCAV or OFAV status bits and for FUOI, LCVI, OCAI or OFAI interrupts over used links. See steps 3 to 7 .

Make sure to disable the interrupts service routine if needed.

PART 2: Sort used APS links and initialize framing

Trigger a:

10. **WAIT_TIP routine**: Write any valid value (one of the “used” links value) to register 0019H (S/UNI MULTI-48 APS SMART framing configuration register). Poll the APS_TIP register bit and wait for its de-assertion in S/UNI MULTI-48 APSIFP Enable and APS Input TelecomBus Synchronization Delay register (register 0015H). In all cases, this routine could be replaced by waiting for at least 5 frames.
11. For each of the used APS links, read their APS frame pulse to J0 delay:
    - Select an APS link with APSLINKSEL[1:0] field, in S/UNI MULTI-48 APS SMART framing configuration register (register 0019H).
    - Poll the APS_TIP register bit and wait for its de-assertion in S/UNI MULTI-48 APSIFP Enable and APS Input TelecomBus Synchronization Delay register (register 0015H).
    - Read the given link delay in the APSFP2J0DLY[13:0] field of the S/UNI MULTI-48 APS SMART framing configuration register (register 0019H).
12. Find which of the used APS links have the shortest delay, and which have the longest delay. The link(s) with the smallest APSFP2J0DLY value will be referenced as the shortest delay group. The link(s) with the largest APSFP2J0DLY value will be referenced as the longest delay group. Make sure to consider the wrap around value of 25F7H and the maximum inter-link delay of 16 cycles (max value of the inter-link APSFP2J0DLY difference is 24 due to FIFO depth) when processing the results to determine which links have the longest/shortest delay. If only one APS link is used or all used links have the same APSFP2J0DLY value, go to next step.
13. To AIJ0DLY[13:0], add the delay value found in the shortest link(s) APSFP2J0DLY[13:0] value. If only one APS link is used or all used links have the same APSFP2J0DLY value, add its/their APSFP2J0DLY[13:0] value in AIJ0DLY[13:0], trigger a WAIT_TIP routine and go to part 4.

PART 3: Place all APS links within the same R8TD FIFO window

14. Write any valid value (one of the used links value) to register 0019H (S/UNI MULTI-48 APS SMART framing configuration register), poll the APS_TIP register bit and wait for its de-assertion in S/UNI MULTI-48 APSIFP Enable and APS Input TelecomBus Synchronization Delay register (register 0015H).
15. Read each of the APSIFP2J0DLY values from the longest delay group:
    - Select one of the longest delay link with the APSLINKSEL[1:0] field, in S/UNI MULTI-48 APS SMART framing configuration register (register 0019H).
    - Poll the APS_TIP register bit and wait for its de-assertion in S/UNI MULTI-48 APSIFP Enable and APS Input TelecomBus Synchronization Delay register (register 0015H).
    - Read the given link delay in the APSFP2J0DLY[13:0] field of the S/UNI MULTI-48 APS SMART framing configuration register (register 0019H).

16. If all longest delay links APSIFP2J0DLY value are 0, go to part 4 of this algorithm. Else, add 8 to the current AIJ0DLY field and repeat part 3. Note: This "+8" step should not be repeated more than twice (maximum of two 8 cycles offsets) since maximum delay difference between two links is 16.

PART 4: Verify R8TD FIFO interrupts

Verify there are no R8TD FIFO underrun/overrun or Line Code Violation interrupts.

17. Clear all used links R8TD interrupt status bits by either reading the S/UNI MULTI-48 R8TD APS Interrupt Status register, when WCIMODE is set to logic 0, or by writing logic 1 values to all R8TD interrupt status bits in the same register, when WCIMODE is set to logic 1.
18. Wait for a few us (10 us should be enough).
19. Read all used links R8TD interrupt status bits several times (~10). Monitor for any new R8TD FIFO underrun/overrun (FUOI) or Line Code Violations (LCVI) interrupts.

    CASE 1: *There is only one APS link used or all used links have the same APSFP2J0DLY value*.
    If there was no R8TD FUOI nor LCVI interrupts, go directly to part 5. If there were FUOI or LCVI interrupts, do the following:
    - Add 4 to the current AIJ0DLY field value.
    - Trigger a WAIT_TIP routine
    - Clear the Rx APS J0 interrupts in register 0018H (S/UNI MULTI-48 Rx APS J0 FIFO Interrupt Status).
    - Monitor the Rx APS J0 interrupts for about 5 frames. If used links all trigger (only) OKJ0 interrupts once a frame for 5 consecutive frames, consider the APS smart framing procedure finished. Else, if there are EXJ0 or NOJ0 interrupts on used links, substract 8 from the current AIJ0DLY count, then consider the APS smart framing procedure finished.

    CASE 2: *There are valid shortest and longest delay groups.*
    If there were no R8TD FUOI nor LCVI interrupts, go directly to part 5. If there were new FUOI or LCVI interrupts, do the following:
    If one of the shortest delay group links had FUOI or LCVI interrupts, substract 4 from the current AIJ0DLY field value. If one of the longest delay links had FUOI or LCVI interrupts, add 4 to the current AIJ0DLY field value. In both cases, this ends the APS smart framing routine. Longest and shortest delay links are not supposed to have interrupts at the same time. If it does happen, it probably is because software didn't wait long enough before clearing the interrupts or because inter-link skew does not respect the specification.

PART 5: Center APS links within R8TD FIFO window

20. Add 1 to the current AIJ0DLY field value.
21. Trigger a WAIT_TIP routine.

Clear top level J0 ints

23- Wait for 2 to 3 frames

22. 24- Monitor for any new NOJ0 or EXJ0 ints. If there are NOJ0 or EXJ0 interrupts, substract 4 from the current AIJ0DLY field value and consider the APS smart framing routine over. If there are no NOJ0 or EXJ0 interrupts, repeat part 5.

These steps should cover all cases. If software wants to double check that the APS port really is synchronized properly, it can do the following:

- Clear device level Rx APS J0 FIFO interrupts (register 0018H) as well as all 4 links R8TD interrupts.
- Read all links APS frame pulse to J0 delay (see step 11). Make sure they all are 0.

- Read all links R8TD interrupts. Make sure there are no FIFO underrun/overrun (FUOI) nor Line Code Violations (LCVI) interrupts.
- Read Rx APS J0 FIFO Interrupt Status register (register 0018H). Make sure there only are OKJ0 interrupts on all links.

Note that software must make sure there is no ongoing interrupt servicing routine that could read the R8TD interrupts while the smart framing routine is going on. An easy way to do so is to disable all R8TD interrupts using the R8TD interrupt enable bits.

Software should wait for at least two frames after device configuration before starting the smart framing algorithm for the S/UNI MULTI-48 internal references to be stable. When two devices are dependant on each other's APS synchronization (as in a working/protect configuartion using APS ports), software should also wait for at least two frames between each device smart framing algorithm.

When doing a substract or add operation over AIJ0DLY, software should always make sure to deal properly with the wrap around value of 25F7H.

In cases where only some of the APS links are used, APS smart framing routine should be called any time a new APS link is added. To avoid having to run the smart framing algorithm and temporarily waste the synchronization over the already synchronized links when adding a new link, the user must minimally verify that the added link is synchronized properly. This can be done using the recommandations stated previously. If the added link is not synchronized properly, the smart framing routine needs to be run. The APS smart framing routine does not have to be reinvoked when a port is removed.

In order to lower complexity of the smart framing procedure, it is possible to replace Part 1 steps by simply providing a "used links" list field when calling the smart framing software routine. The only downside of this method is that it's not self-checking and smart framing could hang or incorrectly synchronize the APS ports if a "used" link is not connected properly or if a link is connected properly but its R8TD FIFO pointers are in over/underflow.

13.17.3 APS Port Error Recovery Guidelines

Everytime an APS input serial data stream is changed, its R8TD character alignement must be forced to out-of-character-alignment, using the FOCA bit in the R8TD Control and Status register (register 0280H).

After APS port synchronization and R8TD frame alignment, if R8TD LCV interrupts occur multiple times (> 1) per frame over 3 consecutive frames, set FOCA to force realignment.

If errors in the internal frame counter occur (alpha particles or some other odd reason), interrupts on the EXJ0 and NOJ0 bits (register 0018H: Rx APS J0 FIFO Interrupt Status), and the R8TD's framing and character alignment interrupts will show misalignment of the J0 characters. The APS synchronization routine will need to be run again to realign everything.

13.18 Interoperability via the 777MHz LVDS Interface

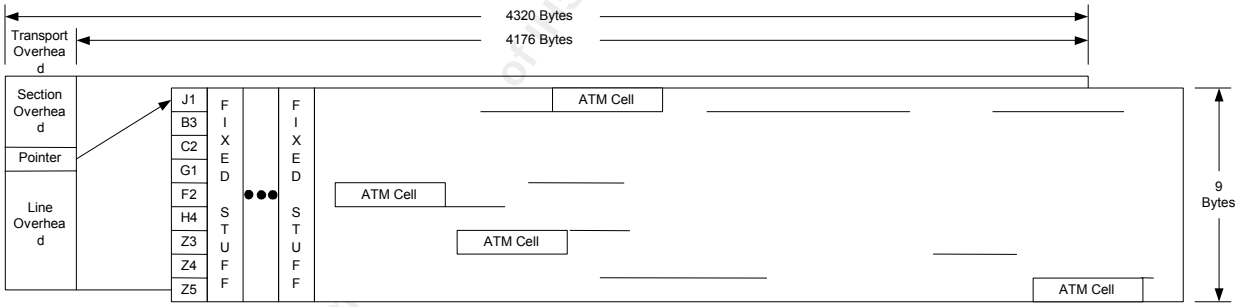
When interconnecting the S/UNI MULTI 48 with other PMC devices via the 777MHz LVDS interface, it is required to operate in HPT mode. For devices that do not support the HPT mode and that only operate in the MST mode, the S/UNI MULTI 48 can be configured for proper interoperability. In this case, the S/UNI MULTI 48 will be set in MST mode and bits RXAPS_PSEUDO_MST[3:0] of Register 0007H Line Side Transmit Configuration will have to be set (please refer to the register section for more details).

13.19 SONET/SDH Frame Mappings and Overhead Byte Usage

13.19.1 ATM Mapping

The S/UNI MULTI-48 device processes the ATM cell mapping for STS-3c/VC-4, STS-12c/VC-4-4c or STS-48c/VC-4-16c. The S/UNI MULTI-48 device processes the transport and path overhead required to support ATM UNIs and NNIs. In addition, it provides support for the APS bytes, the data communication channels and provides full control and observability of the transport and path overhead bytes through register access. In Figure 45, the STS-48c/VC-4-16c mapping is shown. In this mapping, fifteen stuff columns are included in the SPE. No other options are provided.

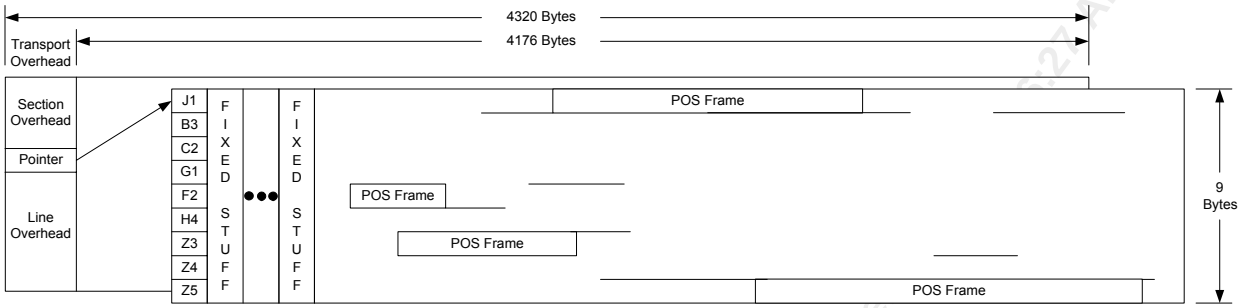
Figure 45 ATM Mapping (STS-48/STM-16 frame)



13.19.2 Packet Over SONET Mapping

The S/UNI MULTI-48 device processes the Packet Over SONET mapping STS-3c/VC-4, STS-12c/VC-4-4c or STS-48c/VC-4-16c. It also processes the transport and path overhead required to support Packet Over SONET applications. In addition, the S/UNI MULTI-48 device provides support for the APS bytes, the data communication channels, and provides full control and observability of the transport and path overhead bytes through register access. In Figure 46, the STS-48c/VC-4-16c mapping is shown. In this mapping, the SPE is used for POS Frames. Again, there is one path overhead and 15 fixed stuff columns.

Figure 46 Packet Over SONET Mapping



13.20 ATM Cell Data Structure

ATM cells may be passed to/from the S/UNI MULTI-48 device using a 52-byte cell structure on a 32-bit UTOPIA level 3 compliant interface.

Figure 47 shows the default ATM cell format for the S/UNI MULTI-48 device at the UTOPIA Level 3 interface. It is the 13 x 32-bit word structure with no HCS or UDF bytes.

Bit 31 of each word is the most significant bit (which corresponds to the first bit transmitted or received). The start of cell indication input and output (TSOC and RSOC) are coincident with Word 1 (containing the first four header octets).

Figure 47 A 52 Byte ATM Data Structure

	Bit 31 Bit 16		Bit 15 Bit 0	
Word 1	H1	H2	H3	H4
Word 2	Payload 1	Payload 2	Payload 3	Payload 4
Word 3	Payload 5	Payload 6	Payload 7	Payload 8
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
Word 12	Payload 41	Payload 42	Payload 43	Payload 44
Word 13	Payload 45	Payload 46	Payload 47	Payload 48

13.21 POS/HDLC Data Structure

Packets may be passed to/from the S/UNI MULTI-48 device using a 32-bit POS-PHY Level 3 compliant interface.

The 32-bit POS-PHY Level 3 data structure is shown in Figure 48. The packet length of 63 bytes was chosen arbitrarily for illustrative purposes. Other lengths are acceptable. Octets are written in the same order they are to be transmitted or they were received on the SONET line. All words are composed of four octets, except the last word of a packet which can have one, two, three, or four octets. If the Transmit Packet Processor (TCFP or TTDP) is configured not to insert the FCS field, then these bytes should be included with the packet passed through the POS-PHY L3 interface. Similarly, if the Receive Packet Processor (RCFP or RTDP) is configured not to strip the FCS field, then these bytes will be included at the end of the packet.

Figure 48 A 63 Byte Packet Data Structure

	Bit 31 Bit 16		Bit 15 Bit 0	
Word 1	Byte 1/SOP	Byte 2	Byte 3	Byte 4
Word 2	Byte 5	Byte 6	Byte 7	Byte 8
Word 3	Byte 9	Byte 10	Byte 11	Byte 12
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
Word 15	Byte 57	Byte 58	Byte 59	Byte 60
Word 16	Byte 61	Byte 62	Byte 63/EOP	Unused

Both the start of the packet and the end of the packet must be identified by the TSOP/RSOP and TEOP/REOP signals. When the first section of a packet is transferred over the interface, the TSOP/RSOP signals will be high for Byte 1 of the packet only. The TMOD[1:0] or RMOD[1:0] pins will indicate how many bytes of the final word are valid.

Bits 31 to 24 form the first transmitted byte and bit 31 is bit which is transmitted first. This is the desired set-up for byte-synchronous POS.

13.21.1 Limitation When Using Externally Generated FCS in STS-48c Mode

When the S/UNI MULTI-48 device is set up in STS-48c POS mode and FCS bytes are passed through the transmit POS-PHY L3 interface, the overall throughput is reduced. The maximum bandwidth throughput will be reduced by a maximum of two bytes per packet. The overall effect will depend on the length of the packets + FCS bytes being transferred through the POS-PHY L3 interface. If the packet + FCS length is evenly divisible by four bytes, no bandwidth is lost for that packet.

13.21.2 Limitations on Small Packets

The S/UNI MULTI-48 device cannot handle packet payloads (excluding FCS) which are smaller than four bytes.

In the receive direction, the RCFP/RTDP should be programmed such that the minimum packet size is at least four bytes + FCS. Packet payloads of three bytes or less are tagged by the RCFP/RTDP packet processor and marked as minimum length violations. For configurations where the FCS is passed through the PL3 bus, the FCS byte count should be treated as payload bytes for these minimum packet size calculations.

In the transmit direction, the minimum packet payload size permitted is four bytes. The exception to this is when the packet is aborted using the TERR pin. Aborted packets can be less than the four byte minimum. The S/UNI MULTI-48 device will extend these packets to four bytes before tagging with the appropriate abort sequence.

13.22 Transport and Path Overhead Bytes

Transport Overhead Bytes

The Transport Overhead Bytes (TOH) consist of the Section Overhead (SOH) and Line Overhead (LOH) bytes. The S/UNI MULTI-48 device can extract these bytes from the received SONET/SDH frame and insert overhead into the transmit stream. This can be done via the RTOH and TTOH ports. See Section 14 for more information on these ports.

Section and Line overhead can also be inserted by the TRMP as illustrated in Table 7 in Section 10.11: Transmit Regenerator and Multiplexer Section Processor (TRMP). The TOH should always be configured either via the TTOH port or by the insertion registers within the TRMP.

The TOH consists of the following bytes:

- **A1, A2:** The frame alignment bytes (A1, A2) locate the SONET frame in the serial stream.
- **J0:** The J0 byte is currently defined as the section trace byte for SONET/SDH. J0 byte is not scrambled by the frame synchronous scrambler.
- **Z0:** The Z0 bytes are currently defined as the section growth bytes for SONET/SDH. Z0 bytes are not scrambled by the frame synchronous scrambler.
- **B1:** The section bit interleaved parity byte provides a section error monitoring function.

In the transmit direction, the S/UNI MULTI-48 device calculates the B1 byte over all bits of the previous frame after scrambling. The calculated code is then placed in the current frame before scrambling.

In the receive direction, the S/UNI MULTI-48 device calculates the B1 code over the current frame and compares this calculation with the B1 byte received in the following frame. B1 errors are accumulated in an error event counter.

- **D1 - D3:** The section data communications channel provides a 192 kbit/s data communications channel for network element to network element communications.
- **H1, H2:** The pointer value bytes locate the path overhead column in the SONET/SDH frame.

In the transmit direction, the S/UNI MULTI-48 device inserts a dynamic pointer value, with a normal new data flag indication in the first or any new H1-H2 pointer value. The concatenation indication is inserted in the remaining slave H1-H2 pairs. Pointer movements can be induced using the TSVCA registers.

In the receive direction, the pointer is interpreted to locate the SPE. The loss of pointer state is entered when a valid pointer cannot be found. Path AIS is detected when H1 and H2 contain an all ones pattern.

- **H3:** The pointer action bytes contain synchronous payload envelope data when a negative stuff event occurs. The all zeros pattern is inserted in the transmit direction. This byte is ignored in the receive direction unless a negative stuff event is detected.
- **B2:** The line bit interleaved parity bytes provide a line error monitoring function.

In the transmit direction, the S/UNI MULTI-48 device calculates the B2 values. The calculated code is then placed in the next frame.

In the receive direction, the S/UNI MULTI-48 device calculates the B2 code over the current frame and compares this calculation with the B2 code receive in the following frame. Receive B2 errors are accumulated in an error event counter.

- **K1, K2:** The K1 and K2 bytes provide the automatic protection switching channel. The K2 byte is also used to identify line layer maintenance signals. Line RDI is indicated when bits 6, 7, and 8 of the K2 byte are set to the pattern '110'. Line AIS is indicated when bits 6, 7, and 8 of the K2 byte are set to the pattern '111'.

In the transmit direction, the S/UNI MULTI-48 device provides register control for the K1 and K2 bytes.

In the receive direction, the S/UNI MULTI-48 device provides register access to the filtered APS channel. Protection switch byte failure alarm detection is provided. The K2 byte is examined to determine the presence of the line AIS, or the line RDI maintenance signals

- **D4 - D12:** The line data communications channel provides a 576 kbit/s data communications channel for network element to network element communications.
- **S1:** The S1 byte provides the synchronization status byte. Bits 5 through 8 of the synchronization status byte identify the synchronization source of the data signal. Bits 1 through 4 are currently undefined.

In the transmit direction, the S/UNI MULTI-48 device provides register control for the synchronization status byte.

In the receive direction, the S/UNI MULTI-48 device provides register access to the synchronization status byte.

- **Z1:** The Z1 bytes are located in the second and third STS-1's locations and are allocated for future growth.
- **M1:** The M1 byte is located in the third STS-1 location and provides a line far end block error function for remote performance monitoring.
- **Z2:** The Z2 bytes are located in the first and second STS-1's locations and are allocated for future growth.

In the transmit direction, Z2 byte is internally generated. The number of B2 errors detected in the previous interval is inserted.

In the receive direction, a legal Z2 byte value is added to the line RFI event counter.

Path Overhead Bytes

The Path Overhead (POH) contains each of the bytes mentioned in this section. POH can be inserted by the THPP via register writes. See the THPP description in the Functional Description chapter.

The POH consists of the following bytes:

- **J1:** The Path Trace byte is used to repetitively transmit a 64-byte CLLI message (for SONET networks), or a 16-byte E.164 address (for SDH networks). When not used, this byte should be set to transmit continuous null characters. Null is defined as the ASCII code, 0x00.

In the transmit direction, characters can be inserted using the TTTP Path Trace register. The register is the default selection and resets to 0x00 to enable the transmission of NULL characters from a reset state.

In the receive direction, the path trace message is optionally extracted into the 16 or 64 byte path trace message buffer.

- **B3:** The path bit interleaved parity byte provides a path error monitoring function.

In the transmit direction, the S/UNI MULTI-48 device calculates the B3 bytes. The calculated code is then placed in the next frame.

In the receive direction, the S/UNI MULTI-48 device calculates the B3 code and compares this calculation with the B3 byte received in the next frame. B3 errors are accumulated in an error event counter.

- **C2:** The path signal label indicator identifies the equipped payload type. For ATM payloads, the identification code is 0x13. For Packet over SONET (including X^{43}+1 payload scrambling), the identification code is 0x16.
- **G1:** The path status byte provides a path RDI function, and a path remote defect indication function. Three bits are allocated for remote defect indications: bit 5 (the path RDI bit), bit 6 (the auxiliary path RDI bit) and bit 7 (Enhanced RDI bit). Taken together these bits provide a eight state path RDI code that can be used to categorize path defect indications.

In the transmit direction, the S/UNI MULTI-48 device provides register bits to control the path RDI (bit 5) and auxiliary path RDI (bit 6) states. For path RDI, the number of B3 errors detected in the previous interval is inserted either automatically or using a register. This path RDI code has nine legal values, namely 0 to 8 errors.

In the receive direction, a legal path RDI value is accumulated in the path RDI event counter. In addition, the path RDI and auxiliary path RDI signal states are available in internal registers.

- **H4:** The multi-frame indicator byte is a payload specific byte, and is not used for ATM payloads. This byte is forced to 0x00 in the transmit direction, and is ignored in the receive direction.
- **Z3 - Z5:** The path growth bytes provide three unused bytes for future use.

In the transmit direction, the growth bytes may be inserted from the three THPP Path Growth byte registers.

13.23 Using the SONET/SDH Inband Error Report Processor (SIRP)

The remote alarm port RDI and REI values are sourced from an upstream module in the S/UNI MULTI-48 device. The SIRP allows these alarm indications to be transmitted back to the remote end via the APS port.

REI and RDI values are sourced from the SIRP remote alarm port. If the extended RDI mode is enabled, the receive cell processor's loss-of-cell delineation state (LCD, in ATM mode), which is mapped to a programmable RDI code if asserted, is compared with the remote port's RDI code. The higher priority RDI will take precedence.

SIRP proper timeslots must be provisioned when using the PL3/UL3 transmit side or the PRBS generator of the PRGM block. To provision the SIRP properly, TSx_PROV register bit must be set to logic 1 for all master timeslots, depending on payload type:

- STS-48c/VC-4-16c: Provision SIRP on slice 1, timeslot 1
- STS-12c/VC-4-4c over slice N: Provision SIRP on slice N, timeslot 1
- 4 x STS-3c/VC-4 over slice N: Provision SIRP on slice N, timeslots 1 to 4
- 1 x STS-3c/VC-4 over slice N: Provision SIRP on slice N, timeslot 1.

13.24 Using the PRBS Generator and Monitor (PRGM)

A pseudo-random (using the $X^{23}+X^{18}+1$ polynomial) or incrementing pattern can be inserted/extracted in the SONET/SDH payload. It cannot be inserted into the ATM cell or packet payload. With PRBS data and incrementing data patterns, the payload envelope is filled with pseudo-random/incrementing bytes with the exception of POH and fixed stuff columns. In the case of the incrementing counts, the count starts at 0 and increments to FFh before the count starts over at 0 once again. The incrementing count is free to float within the payload envelope and therefore the 0 count is not associated with any fixed location within a payload envelope.

13.24.1 Synchronization

Before monitoring the correctness of the PRBS payload, the monitor must synchronize to the incoming PRBS. The process of synchronization involves synchronizing the monitoring LFSR to the transmitting LFSR. Once the two are synchronized, the monitoring LFSR generates the next expected PRBS bytes. When receiving sequential PRBS bytes (STS-12c/VC-4-4c), the LFSR state is determined after receiving three PRBS bytes (24 bits of the sequence). The last 23 of 24 bits (excluding MSB of first received byte) would give the complete LFSR state. The eight newly generated LFSR bits after a shift by 8 (last 8 XOR products) will produce the next expected PRBS byte.

In master/slave configuration of the monitor (STS-48c/VC-4-16c concatenated payloads), more bytes are needed to recover the LFSR state, because the slaves need a few bytes to be synchronized with the J1 byte indicator.

The implemented algorithm requires four PRBS bytes of the same payload to ascertain the LFSR state. From this recovered LFSR state the next expected PRBS byte is calculated.

An Out of Synchronization and Synchronized State is defined for the monitor. While in progress of synchronizing to the incoming PRBS stream, the monitor is out of synchronization and remains in this state until the LFSR state is recovered and the state has been verified by receiving four consecutive PRBS bytes without error. The monitor will then change to the Synchronized State and remains in that state until forced to resynchronize via the RESYNC register bit or upon receiving 3 bytes with errors. When forced to resynchronize, the monitor changes to the Out of Synchronization State and tries to regain synchronization.

It is important to note that the monitor can falsely synchronize to an all zeros pattern or, if the incoming pattern is inverted, an all ones pattern. It is recommended that users poll the PRGM Monitor's LFSR value after synchronization has been declared to confirm that the value is neither all 1's or all 0's.

Upon detecting three consecutive PRBS byte errors, the monitor will enter the Out of Synchronization State and automatically try to resynchronize to the incoming PRBS stream. Once synchronized to the incoming stream, it will take four consecutive non-erroneous PRBS bytes to change back into the Synchronized State. The auto synchronization is useful when the input frame alignment of the monitored stream changes. The realignment will affect the X23+X18+1 PRBS sequence causing all input PRBS bytes to mismatch and forcing the need for a resynchronization of the monitor. The auto resynchronization does this, detecting a burst of errors and automatically re-synchronizing.

13.24.2 Error Detection and Accumulation

By comparing the received PRBS byte with the calculated PRBS byte, the monitor is able to detect byte errors in the payload. A byte error is detected on a comparison mismatch of the two bytes. Only a single byte error is counted regardless of the number of erroneous bits in the byte. All byte errors are accumulated in a 16 bit byte error counter. The error counter will saturate at its maximum value of FFFFh; ie. it will not wrap around to 0000h if further PRBS byte errors are encountered. The counter is readable via the PRGM Monitor Error Count. An indirect read to that register will initiate a transfer of the error counter into the registers for reading. The error counter is cleared when transferred into the registers and the accumulation restarts at zero. All master and slave (concat) STS-1 timeslots error counts belonging to a concatenated stream must be read. The error counts in each associated register must be summed by software.

Bit errors are accumulated only when the monitor is in synchronized state. To enter the synchronized state, the monitor must have synchronized to the incoming PRBS stream and received four consecutive bytes without errors. Once synchronized, the monitor falls out of synchronization when forced by programming high the RESYNC register bit, or once it detects three consecutive PRBS byte errors. When out of synchronization, detected errors are not accumulated. However, it should be noted that when the PRGM goes out of synchronization, 1 or 2 extra errors may be counted. In other words, the 3 errors which cause the PRGM to lose synch may in fact be counted as 3, 4, or 5 errors.

Note that SONET slice #1 must not be in reset state when the PRGM block is configured to monitor any data stream coming from the receive line interface. That is, RESETSL[1] bit (register 0003H: S/UNI MULTI-48 Master Software Resets Register) must be set to logic 0 when any PRGM_MUX[X] bit (register 0005H: S/UNI MULTI-48 Master Configuration Register #2) is set to logic 0 and its corresponding PRGM monitor is enabled (MON_ENA bit set to logic 1, in PRGM Indirect Register 00H: PRGM Monitor Timeslot Configuration Page).

13.24.3 Monitoring and Generating a Single STS-3c/VC-4 PRBS Payload in STS-3/STM-1 Mode

When a single STS-3c/VC-4 stream is monitored in STS-3/STM-1 line mode, the PRGM must be configured to monitor only an STS-3c/VC-4 payload on the first STS-3/STM-1 position because of the pseudo STS-12/STM-4 frame generation. The MON_ENA configuration bit of the "PRGM Monitor Timeslot Configuration" for STS-1/STM-0 timeslots #1, 5 and 9 must be set to logic 1. The MON_ENA configuration bit of the "PRGM Monitor Timeslot Configuration" for other timeslots must be set to logic 0.

To generate a single STS-3c/VC-4 PRBS payload in STS-3/STM-1 line mode, only one STS-3c/VC-4 payload has to be generated at the first STS-3c/VC-4 position because of the pseudo STS-12/STM-4 frame generation. The PRBS_ENA configuration bit of the "PRGM Generator Timeslot Configuration" for the STS-1/STM-0 timeslots #1, 5 and 9 must be set to logic 1. The PRBS_ENA configuration bit of the "PRGM Generator Timeslot Configuration" for other timeslots must be set to logic 0.

13.25 Setting up Timeslot Assignments in the UL3/PL3 X-Bar

The UL3/PL3 X-Bar allows the swapping of any transmit UL3/PL3 channel to any transmit line payload and the swapping of any receive line payload to any receive UL3/PL3 channel. The STSI blocks can be used to rearrange system side and line side SONET/SDH timeslots. Each block buffers 48 timeslots and rearranges them as desired before outputting them. The STSI blocks allow user configuration of timeslot mappings, basic bypass of timeslots and predefined mappings.

13.25.1 Standard Line-Side (SONET sub-system) Timeslot Map

The standard Line-side Timeslot Map at the S/UNI MULTI-48 interface is shown in Table 34. The timeslots of Table 34 represent the timeslot usage in the SONET sub-system, on the line side of the TSTSI and RSTSI, and are presented from left to right. The timeslots of Table 34 are processed from left to right.

Payload bytes from the SONET/SDH stream are labeled by Sx,y. Within Sx,y, the STS-3/STM-1 number is given by 'x' and the column number within the STS-3/STM-1 is given by 'y.' With such a mapping, an STS-12c/VC-4-4c data stream is built out of the first byte of each of the four STS-3 (Sx,1), the second byte of each of the STS-3 (Sx,2) and the third and last byte of each of the STS-3 (Sx,3). STS-12c/VC-4-4c or 4 x STS-3c/VC-4 payloads are transferred across one complete stream. An STS-48c/VC-4-16c payload is built out of all 4 streams.

Table 34 Standard Line-Side Timeslot Map

Line-Side Timeslots

Stream 0	S1,1	S2,1	S3,1	S4,1	S1,2	S2,2	S3,2	S4,2	S1,3	S2,3	S3,3	S4,3
Stream 1	S5,1	S6,1	S7,1	S8,1	S5,2	S6,2	S7,2	S8,2	S5,3	S6,3	S7,3	S8,3
Stream 2	S9,1	S10,1	S11,1	S12,1	S9,2	S10,2	S11,2	S12,2	S9,3	S10,3	S11,3	S12,3
Stream 3	S13,1	S14,1	S15,1	S16,1	S13,2	S14,2	S15,2	S16,2	S13,3	S14,3	S15,3	S16,3

13.25.2 Required System-Side Timeslot Map for Sub-STS-48c/VC-4-16c Data Streams

The required system-side Timeslot Map inside the S/UNI MULTI-48 interface is shown in Table 35 for sub-STS-48c/VC-4-16c data stream. The timeslots of Table 35 are processed from left to right.

With such a mapping, an STS-12c/VC-4-4c data stream will occupy one complete stream. STS-3c/VC-4 data streams within each STS-12/STM-4 data stream must be allocated to a set of Sx,1 and Sx,2 and Sx,3 timeslots shown in Table 35.

Note: The timeslot locations of Table 34 and Table 35 are identical. Thus, if no space or time timeslot interchanges are required for sub-STS-48c/VC-4-16c data streams, the RSTSISW[1:0] and TSTSISW[1:0] bits in the S/UNI MULTI-48 Line Side Receive Configuration register (address 0006H) and in the S/UNI MULTI-48 Line Side Transmit Configuration register (address 0007H) can be programmed in bypass mode (‘b01).

Table 35 Required System-Side Timeslot Map for Sub-STS-48c/VC-4-16c Data Streams

System-Side Timeslots

Stream 0	S1,1	S2,1	S3,1	S4,1	S1,2	S2,2	S3,2	S4,2	S1,3	S2,3	S3,3	S4,3
Stream 1	S5,1	S6,1	S7,1	S8,1	S5,2	S6,2	S7,2	S8,2	S5,3	S6,3	S7,3	S8,3
Stream 2	S9,1	S10,1	S11,1	S12,1	S9,2	S10,2	S11,2	S12,2	S9,3	S10,3	S11,3	S12,3
Stream 3	S13,1	S14,1	S15,1	S16,1	S13,2	S14,2	S15,2	S16,2	S13,3	S14,3	S15,3	S16,3

13.25.3 Required System-Side Timeslot Map for STS-48c/VC-4-16c Data Streams

The required system-side Timeslot Map inside the S/UNI MULTI-48 interface is shown in Table 36 for an STS-48c/VC-4-16c data stream. The timeslots of Table 36 are processed from left to right.

With such a mapping, an STS-48c/VC-4-16c data stream will be carried by the data streams 1 to 4.

Mapping from the standard line-side timeslot mapping shown in Table 34 to the STS-48c/VC-4-16c system-side timeslot mapping shown in Table 36 can be done by setting the RSTSISW[1:0] bits to ‘b10 and the TSTSISW[1:0] bits to ‘b11 in the S/UNI MULTI-48 Line Side Receive Configuration register (address 0006H) and in the S/UNI MULTI-48 Line Side Transmit Configuration register (address 0007H).

Table 36 Required System-Side Timeslot Map for an STS-48c/VC-4-16c Data Steam

	System-Side Timeslots											
Stream 0	S1,1	S5,1	S9,1	S13,1	S1,2	S5,2	S9,2	S13,2	S1,3	S5,3	S9,3	S13,3
Stream 1	S2,1	S6,1	S10,1	S14,1	S2,2	S6,2	S10,2	S14,2	S2,3	S6,3	S10,3	S14,3
Stream 2	S3,1	S7,1	S11,1	S15,1	S3,2	S7,2	S11,2	S15,2	S3,3	S7,3	S11,3	S15,3
Stream 3	S4,1	S8,1	S12,1	S16,1	S4,2	S8,2	S12,2	S16,2	S4,3	S8,3	S12,3	S16,3

13.25.4 Custom Timeslot Mappings and Movement of Timeslots Associated with a Channel

If the RSTSISW[1:0] or TSTSISW[1:0] bits are set to ‘b00, then the corresponding STSI block will be set for custom timeslot mapping. This permits the user to swap the position of STS-3c/VC-4 and STS-12c/VC-4-4c channels or interface with non-standard line-side timeslot maps.

In the custom timeslot mappings mode of operation, the RSTSI timeslot transformation must correspond to the inverse of the TSTSI mapping.

The channels must still fit into the required system-side timeslot map in a manner that is required by a channel of such a rate. For example, an STS-3c channel which occupied line-side timeslots S1,1 and S1,2 and S1,3 in Table 34 can be moved to system-side timeslots S7,1 and S7,2 and S7,3 in Table 35. The analogous mapping can be done from the system-side timeslots to the line-side timeslots.

The following procedure shows how the RSTSI block can be programmed to perform such a remapping of timeslots. Page 0 of the RSTSI block is configured in the example.

1. Set RSTSISW[1:0] equal to ‘b00.

2. For the RSTSI, the base address RSTSI_BASE is 0300H.

3. Read BUSY in the RSTSI Indirect Address register at RSTSI_BASE + 00H. If it is logic 0, proceed to step 4. Otherwise, poll BUSY until it is logic 0.

4. Write 0010H to the RSTSI Indirect Data register at RSTSI_BASE + 01H to set TSIN[3:0] to 1 and DINSEL[1:0] to 0. This selects the RXD_P/N[1][7:0] and line-side timeslot S1,1 as the input bus and timeslot respectively.

5. Write 0031H to the RSTSI Indirect Address register at RSTSI_BASE + 00H to set TSOUT[3:0] to 3 and DOUTSEL[1:0] to 1. This selects the position S7,1 on the output stream and system-side timeslot in the page 0 mapping of the RSTSI.

6. Read BUSY in the RSTSI Indirect Address register at RSTSI_BASE + 00H. If it is logic 0, proceed to step 7. Otherwise, poll BUSY until it is logic 0.

7. Write 0050H to the RSTSI Indirect Data register at RSTSI_BASE + 01H to set TSIN[3:0] to 5 and DINSEL[1:0] to 0. This selects the RXD_P/N[1][7:0] and line-side timeslot S1,2 as the input bus and timeslot respectively.

8. Write 0071H to the RSTSI Indirect Address register at RSTSI_BASE + 00H to set TSOUT[3:0] to 7 and DOUTSEL[1:0] to 1. This selects the position S7,2 on the output stream and system-side timeslot in the page 0 mapping of the RSTSI.

9. Read BUSY in the RSTSI Indirect Address register at RSTSI_BASE + 00H. If it is logic 0, proceed to step 10. Otherwise, poll BUSY until it is logic 0.

10. Write 0090H to the RSTSI Indirect Data register at RSTSI_BASE + 01H to set TSIN[3:0] to 9 and DINSEL[1:0] to 0. This selects the RXD_P/N[1][7:0] and line-side timeslot S1,3 as the input bus and timeslot respectively.

11. Write 00B1H to the RSTSI Indirect Address register at RSTSI_BASE + 00H to set TSOUT[3:0] to BH and DOUTSEL[1:0] to 1. This selects the position S7,3 on the output stream and system-side timeslot in the page 0 mapping of the RSTSI.

12. Return to step 1 to configure more timeslot mappings if needed.

13.25.5 Active and Standby Pages in the STSI Blocks

The STSI blocks contain two configuration pages: an active page and an inactive page. Page selection in the RSTSI is done by its PSEL register bit. Page selection in the TSTSI is also done using its PSEL register bit.

The existence of an active page and an inactive page allows the user to set-up an alternate timeslot mapping on multiple devices or multiple STSI blocks before performing a global switch to the new mapping. The swapping of the page in use is done at transport frame boundaries.

13.26 Setting up Channels for Different Payload Configurations

The S/UNI MULTI-48 device can process ATM, POS, and HDLC traffic for STS-3c/VC-4, STS-12c/VC-4-4c, and STS-48c/VC-4-16c data rates.

System side timeslots and PL3/UL3 channel numbers are integrally linked. The timeslots referred to are those on the system side of the RSTSI and TSTSI blocks, and are those which are directly processed by the RCAS12, TCAS12, TCFP, RCFP, RTDP and TTDP blocks.

System side timeslot locations are illustrated in Table 35 and Table 36.

- STS-48c/VC-4-16c traffic occupies all of the line side timeslots and system-side timeslots of all four data streams. Valid sets are listed in Table 37.
- STS-12c/VC-4-4c traffic occupies twelve line-side timeslots and twelve system-side timeslots of one data stream. A set starts at timeslots S1,1, S5,1, S9,1 or S13,1 as shown in Table 34 and Table 35. Valid sets are listed in Table 37.
- STS-3c/VC-4 traffic occupies three line-side and three system-side timeslots spaced four bytes apart of one data stream as shown in Table 34 and Table 35. Valid sets are listed in Table 37.

Table 37 Valid Receive/Transmit Timeslot Mappings

Rate	Valid Mappings
STS-48c/VC-4-16c	All S***x,y*** (***x*** is from 1 to 16,***y*** is from 1 to 3)
STS-12c/VC-4-4c	S1,1 S2,1 S3,1 S4,1 S1,2 S2,2 S3,2 S4,2 S1,3 S2,3 S3,3 S4,3 S5,1 S6,1 S7,1 S8,1 S5,2 S6,2 S7,2 S8,2 S5,3 S6,3 S7,3 S8,3 S9,1 S10,1 S11,1 S12,1 S9,2 S10,2 S11,2 S12,2 S9,3 S10,3 S11,3 S12,3 S13,1 S14,1 S15,1 S16,1 S13,2 S14,2 S15,2 S16,2 S13,3 S14,3 S15,3 S16,3
STS-3c/VC-4	S1,1 S1,2 S1,3 S2,1 S2,2 S2,3 S3,1 S3,2 S3,3 S4,1 S4,2 S4,3 S5,1 S5,2 S5,3 S6,1 S6,2 S6,3 S7,1 S7,2 S7,3 S8,1 S8,2 S8,3 S9,1 S9,2 S9,3 S10,1 S10,2 S10,3 S11,1 S11,2 S11,3 S12,1 S12,2 S12,3 S13,1 S13,2 S13,3 S14,1 S14,2 S14,3 S15,1 S15,2 S15,3 S16,1 S16,2 S16,3

13.26.1 Receive and Transmit Channel Assigner Configuration

Each SONET/SDH data stream is assigned to a unique receive (or transmit) channel assigner (RCAS12/TCAS12). The RCAS12 (or TCAS12) assigns a configurable channel number to every SONET/SDH payload on the data stream. When processing an STS-48c/VC-4-16c payload, all four RCAS12 (or TCAS12) channel assignments must be configured identically and must be set to channel 0. Once a timeslot is mapped to a channel number by the RCAS12 (or TCAS12), the channel is offset before reaching the UL3/PL3 PHY interface. The offset is a function of the data stream ID and the range of the UL3/PL3 PHY interface (CHAN4SEL register bit).

Table 38 describes correspondence between the SONET/SDH timeslots and the UL3/PL3 channel numbers when payload type is STS-12c/VC-4-4c or STS-3c/VC-4. When payload is STS-48c/VC-4-16c, channel number must be set to 0.

Table 38 SONET/SDH timeslot to UL3/PL3 channel mapping for sub-STS-48c/VC-4-16c payload types

	Configurable RCAS12/TCAS12 channel range		UL3/PL3 PHY channel #	
	CHAN4SEL = 1	**CHAN4SEL = 0**	**CHAN4SEL = 1**	**CHAN4SEL = 0**
Stream 1	0	0 to 3	0	0 to 3
Stream 2	0	0 to 3	1	4 to 7
Stream 3	0	0 to 3	2	8 to 11
Stream 4	0	0 to 3	3	12 to 15

Note 1: The CHAN4SEL register bit is configurable via the S/UNI MULTI-48 Master Configuration Register #1 at address 0004H.

Note 2: The UL3/PL3 channel number corresponds to the S/UNI MULTI-48 RADR[3:0] and TADR[3:0] ports.

Receive and Transmit Channel Assigner Set-up

The following is an example configuration for the RCAS12. The TCAS12 procedure is identical.

1. Write to the RCAS12 # *y* (where *y* is from 1 to 4) Channel Disable register at addresses 0360H 0760H 0B60H 0F60H to disable the desired channels before changing the configuration.

2. Update the channel configuration. Write to the RCAS12 # *y* (where *y* is from 1 to 4) Timeslot Configuration register at 0362H 0762H 0B62H 0F62H + *x* (where *x* is from 0H to BH).

    a. For an STS-48c/VC-4-16c payload, all timeslots (*x* set from 0H to BH) of all RCAS12 # *y* (*y* set from 1 to 4) must be provisioned and assigned to channel 0.

    b. For an STS-12c/VC-4-4c payload on the data stream # *y,* all timeslots (*x* set from 0H to BH) of the RCAS12 # *y* must be provisioned and assigned to the same channel.

    c. For an STS-3c/VC-4 payload on the data stream # *y*, timeslots (*x* set to 0H, 4H and 8H for the first STS-3c/VC-4, *x* set to 1H, 5H and 9H for the second STS-3c/VC-4, *x* set to 2H, 6H and AH for the third STS-3c/VC-4 and *x* set to 3H, 7H and BH for the last STS-3c/VC-4) of the RCAS12 # *y* must be provisioned and assigned to the same channel.

3. Write to the RCAS12 # *y* (where *y* is from 1 to 4) Channel Disable register at addresses 0360H 0760H 0B60H 0F60H to re-enable the desired channels after the configuration change.

Table 39 Example of SONET/SDH timeslot mapping to PHY channel # (CHAN4SEL = 0)

	SONET/SDH payload	SONET/SDH timeslots	RCAS/TCAS # *y* timeslots *x*	RCAS/TCAS # *y* channel map	UL3/PL3 channel #
Stream 1	first STS-3c/VC-4	S1,1 S1,2 S1,3	0H, 4H and 8H	channel 2	channel 2
	second STS-3c/VC-4	S2,1 S2,2 S2,3	1H, 5H and 9H	channel 0	channel 0
	third STS-3c/VC-4	S3,1 S3,2 S3,3	2H, 6H and AH	channel 3	channel 3
	fourth STS-3c/VC-4	S4,1 S4,2 S4,3	3H, 7H and BH	channel 1	channel 1
Stream 2	STS-12c/VC-4-4c	S5,1 to S8,3	0H to BH	channel 0	channel 4
Stream 3	STS-12c/VC-4-4c	S9,1 to S12,3	0H to BH	channel 2	channel 8
Stream 4	first STS-3c/VC-4	S13,1 S13,2 S13,3	0H, 4H and 8H	channel 0	channel 12
	second STS-3c/VC-4	S14,1 S14,2 S14,3	1H, 5H and 9H	channel 2	channel 14
	third STS-3c/VC-4	S15,1 S15,2 S15,3	2H, 6H and AH	channel 1	channel 13

	fourth STS-3c/VC-4	S16,1 S16,2 S16,3	3H, 7H and BH	channel 3	channel 15

Note 1: The RCAS12 (or TCAS12) channel mapping must be unique. No two STS-3c/VC-4 payloads can be assigned the same channel in the same RCAS12 (or TCAS12).

13.27 Receive and Transmit Cell Processors Configuration

The S/UNI MULTI-48 device is composed of four independent transmit cell processors. The cell processor links the transmit PHY interface (TXPHY) and scalable data queue (TXSDQ) to transmit channel assigner (TCAS12). A transmit cell processor is composed of the transmit time-sliced datacom processor (TTDP) and the transmit cell and frame processor (TCFP). The TCFP processes STS-12c/VC-4-4c or STS-48c/VC-4-16c payload, and the TTDP processes STS-3c/VC-4 payload. When the TCFP is active, the TTDP should be disabled (unprovisioned), and when the TTDP is active, the TCFP should be disabled.

The S/UNI MULTI-48 device is also composed of four independent receive cell processors. The cell processor links the channel assigner (RCAS12) to the scalable data queue (RXSDQ) and receive PHY interface (RXPHY). A receive cell processor is composed of the receive time-sliced datacom processor (RTDP) and the receive cell and frame processor (RCFP). The RCFP processes STS-12c/VC-4-4c or STS-48c/VC-4-16c payload, and the RTDP processes STS-3c/VC-4 payload. When the RCFP is active, the RTDP should be disabled (unprovisioned), and when the RTDP is active, the RCFP should be disabled.

The set-up for the STS-12c/VC-4-4c and STS-48c/VC-4-16c receive and transmit cell processors is as follows:

1. Write the bit 0 of the RCFP # *y* (where *y* is from 1 to 4) Configuration register at addresses 0310H 0710H 0B10H 0F10H. For STS-48c/VC-4-16c SONET payload, only RCFP #1 must be provisioned. Other RCFP registers should be configured to fully program the receive cell processor.

2. Write the bit 0 of the TCFP # *y* (where *y* is from 1 to 4) Configuration register at addresses 1310H 1710H 1B10H 1F10H. For STS-48c/VC-4-16c SONET payload, only TCFP #1 must be provisioned. Other TCFP registers should be configured to fully program the transmit cell processor.

The set-up for the STS-3c receive and transmit cell processors is as follows:

1. Write the bit 0 of the RTDP # *y* (where *y* is from 1 to 4) Configuration Indirect register of the channel number # *z* (where *z* is from 0 to 3) at addresses 0341H 0741H 0B41H 0F41H. The channel number # *z* is associated with the RCAS12 channel number assigned for this payload. Other RTDP registers should be configured to fully program the receive cell processor.

2. Write the bit 0 of the TTDP # *y* (where *y* is from 1 to 4) Configuration Indirect register of the channel number # *z* (where *z* is from 0 to 3) at addresses 1341H 1741H 1B41H 1F41H. The channel number # *z* is associated with the TCAS12 channel number assigned for this payload. Other TTDP registers should be configured to fully program the receive cell processor.

Note that when configuring a channel in the TTDP, that channel must be disabled in the downstream TCAS12 block (using CHx_DIS bits from registers 1360H 1740H 1B40H 1F40H) or the configuration write may not be properly executed.

13.28 RXSDQ and TXSDQ Configuration

The SDQ supports 2 different FIFO sizes: 48 Blocks (equal to 12 ATM Cells or 768 bytes) and 192 Blocks (equal to 48 ATM Cells or 3072 bytes). Table 40 shows the recommended FIFO sizes for different data rates.

Table 40 Suggested FIFO Buffer Sizes

FIFO_BS[1:0]	FIFO Size (Blocks)	FIFO Size (ATM Cells)	Suggested BW
00, 01	Reserved	Reserved	Reserved
10	48	12	STS-3c/VC-4
11	192	48	STS-12c/VC-4-4c STS-48c/VC-4-16c

There are 768 Blocks (192 ATM Cells or 12288 bytes) of total storage that can be carved up into a maximum of 16 FIFOs of the sizes mentioned above. The storage is organized in four banks of 192 Blocks each. Block numbers 0 to 191 (000H to 0BFH) are in Bank 0, 192 to 383 (0C0H to 17FH) are in Bank 1, 384 to 575 (180H to 23FH) are in Bank 2, and 576 to 767 (240H to 2FFH) are in Bank 3.

In order to configure the SDQ, the user must determine the size of each FIFO in Blocks and then add them together. The total number of Blocks must be less than 768. The minimum FIFO size is 48 Blocks or 12 ATM Cells. An additional restriction in the SDQ is that each of the four Banks of the SDQ cannot contain more than four FIFOs of 48 blocks or one FIFO of 192 blocks.

The user is required to program three parameters for any given SDQ FIFO:

1. The physical FIFO Number –The value of the FIFO_NUMBER[5:0] register bits (as specified in the FIFO Indirect Configuration Register) must be set to correspond to the channel number (or equivalently, the PHY number) as shown in Table 41 and in Table 42. Refer to the "Setting up Channels for Different Payload Configurations" section for the relation between the SONET/SDH timeslots and the UL3/PL3 Channel number.

Table 41 SDQ FIFO_NUMBER Configuration (When CHAN4SEL = 0)

Bank	UL3/PL3 Channel #	PHYID[5:0]	FIFO_NUMBER[5:0]
0	0 to 3	0 to 3 (0x00 to 0x03)	0 to 3 (0x00 to 0x03)
1	4 to 7	12 to 15 (0x0C to 0x0F)	16 to 19 (0x10 to 0x13)
2	8 to 11	32 to 35 (0x20 to 0x23)	40 to 43 (0x28 to 0x2B)
3	12 to 15	44 to 47 (0x2C to 0x2F)	56 to 59 (0x38 to 0x3B)

Table 42 SDQ FIFO_NUMBER Configuration (When CHAN4SEL = 1)

Bank	UL3/PL3 Channel #	PHYID[5:0]	FIFO_NUMBER[5:0]
0	0	0 (0x00)	0 (0x00)
1	1	12 (0x0C)	16 (0x10)
2	2	32 (0x20)	40 (0x28)
3	3	44 (0x2C)	56 (0x38)

Note that the FIFO_NUMBER value must correspond explicitly to the UL3/PL3 Channel number. For instance, for UL3/PL3 Channel #2, the FIFO_NUMBER must be set to the value 2 (0x02) when CHAN4SEL is set to logic 0 and to 40 (0x28) when CHAN4SEL is set to logic 1.

2. The Block Pointer – this is calculated using the starting Block number, which should be a multiple of the FIFO size. Since there are 192 Blocks in a Bank, the starting Block number is actually an 8 bit number. However, since the smallest FIFO is a multiple of 8 Blocks, only the upper 5 are significant – these 5 bits are called the Block Pointer. The Block Pointer is specified in the FIFO Indirect Configuration register in the BLOCK_PTR[4:0] field. When a bank is processing an STS-48c/VC-4-16c or STS-12c/VC-4-4c payload, the starting block pointer should be set at 00H not to waste buffering area in a bank. When a bank is processing a 4x STS-3c/VC-4 data stream, the starting block pointer should be set at 00H, 06H, 0CH and 12H to evenly distribute all 4 FIFOs in a bank.

3. The FIFO Size – this is a 2 bit number that specifies one of 2 possible sizes for the FIFO. Refer to Table 40 for the values used to specify the FIFO sizes, and a guide to sizing the FIFO based on the bandwidth of the associated PHY. It is up to the discretion of the user to apply this guide to each specific case. This number is specified in the FIFO Indirect Configuration register in the FIFO_BS[1:0] field.

A FIFO occupies the number of Blocks specified by its size starting at the Block Pointer. The user must not configure the Block pointers such that two FIFOs overlap. The user can, however, have gaps between consecutive Blocks, which can potentially be filled by expanding one or the other Block. However, since only 2 FIFO sizes are valid, the user cannot arbitrarily expand a FIFO. Care must be taken to ensure that when expanding from one size to the next, the FIFOs do not overlap. Refer to Section 13.29 for a guide to expanding and contracting configured Blocks in the SDQ.

Table 43 illustrates the configuration for a typical case. This case involves 2 PHYs that have a bandwidth of STS-12, and are allocated 192 Block FIFOs each. There are 8 STS-3c PHYs configured, using a 48 Block FIFO. Bank 0 and Bank 1 have one FIFO each, while Bank 2 and Bank 3 have 4 FIFOs each. The sum of all the Blocks used in this example is 768 which is the maximum number of Blocks available.

Table 43 SDQ Configuration Example (When CHAN4SEL = 0)

UL3/PL3 Channel #	PHYID [5:0]	BW	Size (Blocks/ Cells)	FIFO_BS [1:0]	Bank	FIFO_ NUMBER[5:0]	Starting Block	BLOCK_ PTR[4:0]
0	0x00	STS-12c	192/48	‘b11	0	0x00	0x0	0x0
4	0x0C	STS-12c	192/48	‘b11	1	0x10	0x0	0x0
8	0x20	STS-3c	48/12	‘b10	2	0x28	0x0	0x0
9	0x21	STS-3c	48/12	‘b10	2	0x29	0x30	0x6
10	0x22	STS-3c	48/12	‘b10	2	0x2A	0x60	0xC
11	0x23	STS-3c	48/12	‘b10	2	0x2B	0x90	0x12
12	0x2C	STS-3c	48/12	‘b10	3	0x38	0x0	0x0
13	0x2D	STS-3c	48/12	‘b10	3	0x39	0x30	0x6
14	0x2E	STS-3c	48/12	‘b10	3	0x3A	0x60	0xC
15	0x2F	STS-3c	48/12	‘b10	3	0x3B	0x90	0x12

When configuring/modifying SDQ for a PHY ID, the FIFO number should be set accordingly. Different PHY IDs cannot have the same FIFO number otherwise, the configuration of the other PHY will be overwritten.

The SDQ cannot detect errors due to user misconfiguration. If the user sets up FIFOs that overlap each other, or do not start at a Block number that is a multiple of the size of the FIFO, the results will be unpredictable.

13.29 RXSDQ and TXSDQ Dynamic Reconfiguration

Each PHY connected to a FIFO can have a depth of 48 or 192 Blocks. The SDQ allows the reconfiguration of these PHY to different sizes (for example: the aggregation of four adjacent 48 Block FIFOs into one 192 Block FIFO) without dropping any cells or packets in FIFOs belonging to other PHYs. In order to perform a reconfiguration, the FIFOs being reconfigured should first be disabled (ENABLE = 0) using the FIFO Indirect Configuration register. When disabled, the FIFO will cease to accept any new data, but will continue to drain all existing blocks to the read interface. The user should manually empty the FIFO (by writing a 1 to the FLUSH bit in the FIFO Indirect Address register). Once all the FIFOs that need to be reconfigured are empty, the user must manually clear the FLUSH bit, then write the new configuration by recalculating the FIFO_NUMBER[5:0] and BLOCK_PTR[4:0] bits, changing the FIFO_BS[1:0] bits, and finally in a separate indirect write, setting the appropriate ENABLE bit. This procedure ensures that the FIFOs not being reconfigured are not affected in any way, and allows the ones being reconfigured to not drop any pre-existing data.

As indicated, the user can only aggregate adjacent FIFOs. However, any individual FIFO can be expanded as long as there is no overlap between FIFOs due to this expansion. The user can reduce a FIFO’s size at any time as this will not cause an overlap.

Care should be taken to insure that the ENABLE bit is not set until all other configuration changes have already been written into the FIFO by applying the following procedure:

1. Set indirect data values with ENABLE = 0

2. Write desired indirect address with FLUSH = 1

3. Wait until EMPTY is polled as 1

4. Set indirect data values

5. Write indirect address with FLUSH = 0

6. When ready, set indirect data values with ENABLE = 1

7. Write desired indirect address

Note: For step 4, the user must read all indirect data values for the desired PHY and write them back modifying only the ENABLE bit by setting it to logic 1. Note that this procedure of reading all indirect data values and writing all indirect data values for each indirect write performed is required to maintain the desired configuration for the SDQ FIFOs.

13.30 TXSDQ Buffer Available Operation

For each of the FIFOs configured in the TXSDQ, a Buffer Available (BA[p]) bit indicates whether or not the FIFO p can accept more data. The BA[p] status is given (BA[p] = 1) when the TXSDQ can accommodate at least another injection of BT[4:0] + 1 blocks into its FIFO p. When the number of blocks available in FIFO p is less than (BT[4:0] + 1), then BA[p] is deasserted (BA[p] = 0). At this point, no more new data can be accepted, but the current transaction completes (if BT[p] is not set at the maximum for FIFO p). Eventually, when some of the data in FIFO p is drained by the read interface, the available FIFO space will equal or exceed BT[4:0] + 1. BA[p] is asserted when this condition is reached. The BA[p] state is reflected by the TCA and STPA and PTPA output signals on the Utopia L3 and POS-PHY L3 interfaces when PHY p is selected and/or polled.

In setting the TXSDQ buffer available threshold BT[4:0], the maximum data burst size from the upstream device must be taken into account. Section 13.33 describes how to program BT[4:0] to keep the upstream device from overflowing the TXSDQ FIFO. In general, the following formula applies:

(BT[4:0] + 1) ≥ max burst size from upstream device + system application margin

The values of BT[4:0] and DT[7:0] in the TXSDQ Indirect Data and Buffer Available Thresholds register must be set so that:

(DT[7:0] + 1) + (BT[4:0] + 1) ≤ FIFO size

The FIFO size is set using the FIFO_BS[1:0] register bits in the TXSDQ FIFO Indirect Configuration register and DT[7:0] is the TXSDQ is set in the TXSDQ Indirect Data and Buffer Available Thresholds register. This constraint keeps the FIFO from entering a state where the TXSDQ cannot sustain a new burst from the upstream device and the downstream TCFP or TTDP block does not have enough data to initiate a transfer.

For ATM FIFOs, BT[4:0] and DT[7:0] must be set equal to the value 3. This sets the threshold to be 4 blocks which is the space occupied by an ATM cell. The upstream device should also set its maximum burst size to be equal to one ATM cell. Note that for ATM FIFO's with a POS-PHY bus, if the TPAHOLD bit = 1, BT[4:0] should be set to 7 as described in Section 13.33.

The TXSDQ and RXSDQ FIFOs are divided up into blocks of 16 bytes each which is the smallest granularity of the FIFO. Note that two packets cannot occupy the same FIFO Block. A 17 byte packet will occupy two full blocks, though the second block will be mostly empty, and wasted space. This needs to be considered when attempting to predict the available space in the buffer, and this is the reason why bandwidth tends to be lower for packet sizes that are slightly larger than an integral number of 16-byte blocks.

13.31 RXSDQ and TXSDQ Data Available and Burst-Size Operation

In the RXSDQ and TXSDQ blocks, each FIFO indicates whether or not data is available for reading by asserting the Data Available line (DA[p] for FIFO p). The DA[p] line is asserted by the RXSDQ or TXSDQ under two conditions:

- If the queue depth of FIFO p is greater than a user configured Data Available Threshold (DT[p]), i.e. if there is more data than specified by the threshold.
- If at least one EOP is stored in the FIFO, i.e. the tail end of at least one packet is available in the threshold.

The DA[p] line is de-asserted when the data in the FIFO falls below the threshold and there are no EOPs in the FIFO. For the RXSDQ block, the DA[p] state is reflected by the RCA output signal on the UTOPIA L3 interface. When using the POS-PHY L3 interface, the RXPHY polls the DA[p] signals using its Calendar Sequence to determine if there is any data in the PHY to output.

For the RXSDQ, the BURST_SIZE[3:0] setting in the RXPHY Indirect Burst Size register is closely tied to the DT[7:0] setting in the RXSDQ FIFO Indirect Data Available Threshold register. BURST_SIZE[3:0] must be set to a value less than or equal to (DT[7:0]). This will prevent the RXPHY from initiating a burst until there is sufficient data in the RXSDQ.

For transfer of ATM cells, the BURST_SIZE[3:0] and DT[7:0] register bits must both be set to the value 3. This makes the threshold equal to four blocks, which will contain one ATM cell.

It is also important to note that larger burst sizes may cause the FIFOs in the RXSDQ to reach higher fill levels because more time is needed per PHY to complete a burst. Also, since a burst is terminated when an EOP signal is detected, small packets will cause their associated PHY to be penalized in net throughput across the POS-PHY L3 interface. To maximize fairness, it is recommended that the burst size be kept fairly small – on the order of four blocks (BURST_SIZE[3:0] = 0x3).

In the TXSDQ, once the DA[p] signal indicates that enough data is in the TXSDQ to begin a cell or packet transfer, the downstream TCFP/TTDP blocks will begin pulling data from the corresponding FIFO. The TCFP/TTDP blocks will continue pulling, regardless of the DA[p] state, until the cell or packet is complete. Once complete, the blocks will start the next cell or packet transfer from the TXSDQ, but only after the DA[p] signal is again asserted.

The value of DT[7:0] in the TXSDQ Indirect Data and Buffer Available Thresholds register must be set so that:

$(DT[7:0] + 1) + (BT[4:0] + 1) \leq \text{FIFO size}$

The FIFO size is set using the FIFO_BS[1:0] register bits in the TXSDQ FIFO Indirect Configuration register and BT[4:0] is set in the TXSDQ FIFO Indirect Data and Buffer Available Thresholds register. This constraint keeps the FIFO from entering a state where the TXSDQ cannot sustain a new burst from the upstream device and the downstream TCFP/TTDP block does not have enough data to initiate a transfer.

For packet data streams, it is recommended that DT[7:0] be set to a value close to half or 2/3 of the size of the FIFO. For ATM cell streams, DT[7:0] must be set to the value 0x3.

13.32 RXPHY POS-PHY L3 Servicing

In POS-PHY Level 3, the RXPHY block controls the flow of data across the interface to the Link Layer device and also decides which PHY channel will use the bus. The RXPHY block reads the channel calendar registers and selects a FIFO p that has Data Available (DA[p]) signals asserted. The method of selection is programmed by the user. Servicing is proportional to the number of times a PHY number is entered in the calendar register (see RXPHY Calendar Indirect Address Data register). Once a PHY channel is selected, the POS block controls the RSX signal and passes REOP, RSOP, and RVAL signals from the RXSDQ block to the POS-PHY L3 interface. It also accepts RENB from the Link Layer device and passes it on to the RXSDQ block. The control of transfer size and pause between transfers is accomplished using an internal version of the RENB signal and the BURST_SIZE and RSXPAUSE registers. The burst size is programmable on a per PHY basis.

13.32.1 RXPHY POS-PHY L3 Servicing Algorithm

The calendar servicing algorithm makes choices for service according to the user programmable calendar entered in the RXPHY Calendar Indirect Address Data register.

The calendar algorithm is implemented using a pointer called the servicing pointer. The servicing pointer moves down the calendar, and the first positive packet available assertion the pointer encounters will be the PHYID selected for transfer on the next subsequent opportunity. It is recommended that repeated entries in the calendar be spread in a uniform manner in the calendar. This will help maximize the chances of selection in a proportional manner. The servicing algorithm remembers all assertions for available packets made in the past and advances the servicing pointer through the responses without regard to the age of the response. This algorithm provides flexibility in servicing without starvation as long as the number of entries in the calendar for a PHY is proportional to the bandwidth of that PHY.

Table 44 is an example showing the Calendar with the data available response (DA[p]) from the RXSDQ. In this example, the entire 16 entries are used and PHYIDx and PHYIDz are enabled and PHYIDy is not enabled. The servicing pointer traverses the entries that responded with a positive data available DA[p] assertion. In this example, the selection would be to choose PHYIDx first and then choose PHYIDz.

The number of Calendar entries is programmable and the maximum entry number is 128.

Table 44 RXPHY Calendar Example

RXSDQ Packet available assertion DA[p]	PHY enable	CALENDAR ADDR	CALENDAR DATA
1	1	0	PHYIDx
0	0	1	PHYIDy
1	1	2	PHYIDz
..	..	..	..
..	..	..	..
0	1	15	PHYIDz

For most S/UNI MULTI-48 applications, it is recommended that the calendar length be set to 16 and each STS-3 granule be distributed evenly across the calendar ordering. This will simplify the procedure needed to create concatenated channels or disperse a concatenated channel into individual channels. If dynamic reprovisioning is required, we recommend that the calendar be programmed as shown in Table 45.

Table 45 RXPHY Calendar Recommended Setup for Dynamic Reprovisioning

Calendar Entry	STS-3c PHY Address		STS-12c	STS-48c
	Only 1 STS-3c per bank/slice (155 mode)	Up to 4 STS-3c per bank/slice (2488/622 mode)	PHY Address	PHY Address
0	0	0	0	0
1	12	12	12	0
2	32	32	32	0
3	44	44	44	0
4	0	1	0	0
5	12	13	12	0
6	32	33	32	0
7	44	45	44	0
8	0	2	0	0
9	12	14	12	0
10	32	34	32	0
11	44	46	44	0
12	0	3	0	0
13	12	15	12	0
14	32	35	32	0
15	44	47	44	0

For instance, if an STS-12c/VC-4-4c channel (PHY address #44) occupied entries 3, 7, 11 and 15 in the calendar, it can be broken up into 4 STS-3c/VC-4 channels by simply overwriting those 4 calendar entries with new PHY channel numbers (44, 45, 46 and 47, respectively).

If 4 STS-3c/VC-4 channels are to be combined into an STS-12c/VC-4-4c channel, the 4 calendar entries can simply be written with the STS-12c/VC-4-4c channel number and the calendar will be reprovisioned with each channel receiving the appropriate service bandwidth. The same applies to any transition between any STS-48c/VC-4-16c, STS-12c/VC-4-4c or STS-3c/VC-4 payload configuration.

Note that care must be taken when using mixed 622 and 155 streams. In order for each channel to be proportionally represented in the calendar with regards to its bandwidth, the calendar size of 16 entries might not be the best setup. The calendar size should generally represent the number of STS-3c/VC-4 granules over the receive PL3 sub-system. For instance, if there are two STS-12c/VC-4-4c channels (622 mode), one 4xSTS-3c/VC-4 channel (622 mode) and 1 single STS-3c/VC-4 channel (155 mode), then the 16 calendar entries can't be divided to proportionally represent 13 different STS-3c/VC-4 granules. When using 155 mode channels, the only case where the recommended setup described in Table 45 will really enable smooth dynamic reprovisioning is when all channels are reprovisioned to/from 155 streams. Dynamic reprovisioning to/from single 155 mode channels will otherwise always affect the calendar setting of at least some channels that are not reprovisioned.

Note that when reconfiguring the calendar, the affected calendar entries must be unprovisioned in their upstream blocks first (RXSDQ, RTDP/RCFP, and RCAS12 blocks) to ensure that they are not being serviced while the reconfiguration is taking place. Unprovisioning the channels will make it so the calendar algorithm sees no data available from those channels.

13.33 Transmit PL3 STPA and PTPA Behavior

The STPA signal provides the fill status of the FIFO that is selected by the transmit PL3 interface. The PTPA provides the fill status of the polled transmit FIFO.

When STPA or PTPA is logic 1, it indicates that the FIFO has enough room to absorb a pre-determined number of data transfers. Once the FIFO threshold has been exceeded, meaning that the FIFO can no longer absorb the pre-determined number of data transfers, then STPA will transition to logic 0.

Figure 49 and Figure 50 show the behavior of STPA/PTPA when the FIFO threshold is reached. It is critical that the upstream device responds properly in order to avoid any FIFO overflow in the TXSDQ.

There are two basic methods of transferring data across the PL3 interface: 1) burst-transfer mode and 2) word-transfer mode. Burst-transfer mode is similar to the UL3 interface. Where the UL3 interface will transfer one cell at a time, the PL3 interface will transfer a maximum number of bytes or end at an end-of-packet indication in one burst, whichever comes first. Setting TPAHOLD (TXPHY Configuration register) to logic 1 will configure the S/UNI MULTI-48 to burst-transfer mode.

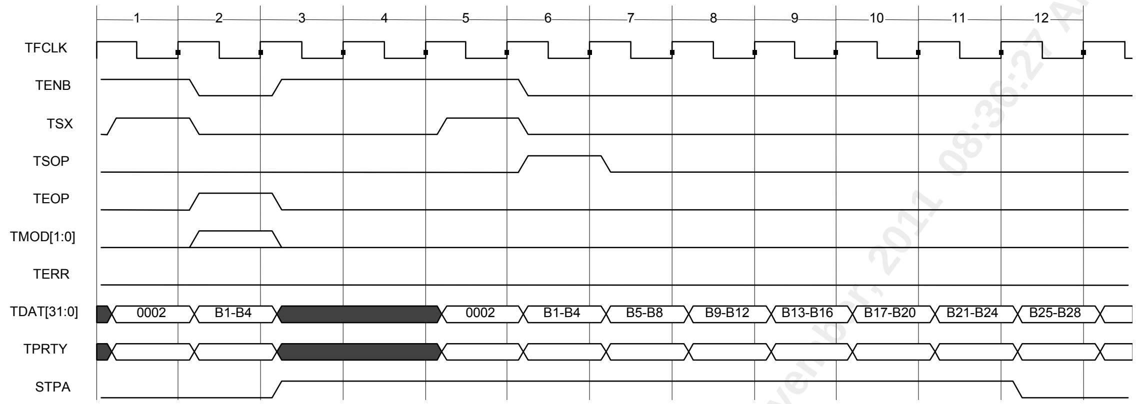
Word-transfer mode has no such limitations. During polling, the upstream device is expected to watch the PTPA signal to find when it can begin a transfer. Once the transfer is started, it must observe the STPA signal and pause when required to prevent overflowing the FIFO. Setting TPAHOLD to logic 0 will configure the S/UNI MULTI-48 device to word-transfer mode or hybrid word/burst-transfer mode. Note that this mode should not be used in standard Multi-PHY applications because an important amount of bandwidth can be lost due to the PL3 interface waiting for STPA to reassert once a transfer is paused. In order for this mode to be suitable for Multi-PHY applications, the transmit PL3 master would require to be able to start transfers on other PHYs once STPA is deasserted for one given PHY, without waiting for STPA to be deasserted. Otherwise, this mode is only suitable for Single-PHY applications (one channel).

13.33.1 TPAHOLD = 0

Figure 49 shows the behavior of STPA when the TPAHOLD register bit (TXPHY Configuration register) is set to logic 0. This is the default operating mode. In this example, the write to the FIFO, which occurs at the start of cycle 7, crosses the TXSDQ block's BT[4:0] threshold. STPA responds on cycle 12. There is a five clock cycle delay between the write and the response on STPA.

Note that it is possible to use PTPA even when TPAHOLD is set to logic 1, but user must be aware that the five clock cycle delay also applies to PTPA.

Figure 49 TPAHOLD Set To 0



This five-cycle delay can be dealt with in two ways.

First, the upstream device can be programmed to wait for the response before sampling the new STPA status. For small transfers, this may affect the net throughput possible on the PL3 bus. In this case, the TXSDQ buffer threshold can be set equal or greater than the PL3 burst-size of the upstream device.

BT[4:0] ≥ burst-size – 1

Where burst-size is in units of blocks (1 block = 16 bytes).

Second, if the upstream device cannot account for the STPA delay or maximum throughput is desired on the PL3 bus, the TXSDQ block's buffer threshold must be set to guarantee that any transfers which occur during the five-cycle delay do not cause any overflows. To do this, the value of the TXSDQ block's buffer threshold may need to be increased. It can be calculated by using the following equation:

BT[4:0] ≥ 1 + (num_min_pack * min_pack_size_in_blocks) + remainder - 1

Where:

Let m = minimum packet size (as a number of transfer cycles)
Let s = upstream device's response time to STPA (# of clocks after STPA for transfer to stop)

Let ovrhd_cycles = number of non-packet payload cycles per transfer (each guaranteed null cycle introduced by the upstream device counts as 1)

num_min_pack = downround ((5 + s - 1) / (m + ovrhd_cycles))

min_pack_size_in_blocks = upround (m / 4)

remainder = upround (((5 + s - 1) mod m) / 4)

Explanation:

The STPA is late by five clocks and the link layer device takes s number of clocks after STPA to stop transfer, resulting in 5 + s words that can be written after the threshold gets exceeded.

- the '1' is to deal with the worst case where the threshold gets exceeded during the write of the final word of a packet whose size is one block greater than a multiple of 4 (eg. the EOP word of a 13 word packet, as this word wastes a whole block by itself).
- num_min_pack is the number of full minimum-sized packets that can be written during the 5 + s - 1 clocks. (The subtraction of 1 refers to the EOP word corresponding to point i)

  eg. if s = 2, m = 5, ovrhd_cycles = 0,

  num_min_pack = downround((5+2-1) / (5+0)) = 1.

  That is, in those 6 clocks, there could be one full min-size packet that can be written
- min_pack_size_in_blocks is the number of blocks occupied by a minimum-sized packet. eg. if m = 5 clocks cycles, then min_pack_size_in_blocks is 2.
- remainder refers to how many blocks of a partial packet gets written after the minimum-sized packets had been written. (5 + s – 1)mod m is a calculation of how many words are contained in the final partial packet. The number of blocks occupied is simply that value divided by 4 rounded up.
- the '-1' at the end of the equation refers to the fact that BT in the TXSDQ is one less than what's required.

Examples:

- s = 2 (7 clock latency for response to STPA)

  m = 1 (min 4-byte packet)
  ovrhd_cycles = 0 (4 byte packet, no null cycles guaranteed between each

  packet/burst)

  num_min_pack = downround ((5+2-1)/(1+0)) = 6

  min_pack_size_in_blocks = upround(1/4) = 1

  remainder = upround (((5+2-1)mod1)/4) = 0

  BT[4:0] ≥ 1 + (6*1) + 0 – 1 = 6

- s = 2 (7 clock latency for response to STPA)

  m = 1 (min 4-byte packet)

  ovrhd_cycles = 1 (4 byte packet, 1 null cycle guaranteed between each packet/burst)

  num_min_pack = downround ((5+2-1)/(1+1)) = 3

  min_pack_size_in_blocks = uproud(1/4) = 1

  remainder = uproud (((5+2-1)mod1)/4) = 0

  BT[4:0] ≥ 1 + (3*1) + 0 – 1 = 3
- s = 2 (7 clock latency for response to STPA)

  m = 13 (atm cell)

  ovrhd_cycles = 0 (no null cycles)

  num_min_pack = downround ((5+2-1)/(13+0)) = 0

  min_pack_size_in_blocks = uproud(13/4) = 4

  remainder = uproud (((5+2-1)mod13)/4) = 2

  BT[4:0] ≥ 1 + (0*4) + 2 – 1 = 2

  For the optional PL3 mode where each burst is not terminated by a TENB transition to logic 1, TPAHOLD must be set to logic 0.

13.33.2 TPAHOLD = 1

Figure 50 shows the behavior of PTPA when the TPAHOLD register bit (TXPHY Configuration register) is set to logic 1. This is the optional operating mode which decreases the TPA response delay from five cycles to one cycle, but holds TPA assertion until the completion of the transfer.

TPA logic 0 to logic 1 transitions are reported one clock cycle after the write access causing the FIFO fill level to cross its buffer available threshold. TPA logic 1 to logic 0 transitions are also based on a single clock cycle delay after FIFO fill level crosses its buffer available threshold, but they can only happen during two precise opportunities:

- one cycle after a transfer is initated;
- two cycles after the transfer completes.

This optional mode is only usable when each burst is terminated by a TENB transition to logic 1. Because the PL3 interface is used in “burst-transfer mode”, the STPA signal should not be used. Once a burst has been allowed by polling PTPA at logic 1, then one full burst is allowed. PTPA must be polled at logic 1 again before another burst can be started.

In this example, the write to the FIFO, which occurs at the start of cycle 7, crosses the desired FIFO fill threshold. PTPA responds on cycle 8. There is a 1 clock cycle delay between the write and the response on PTPA. Cycle 8 is considered “one cycle after transfer is initated” because the first cycle of a transfer is defined as the first clock cycle where TENB is sampled low (cycle 7 in Figure 50).

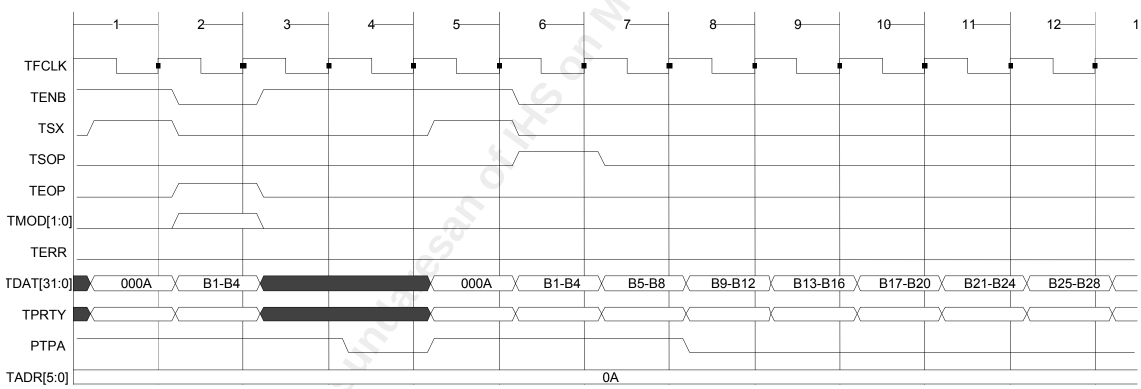
The TXSDQs FIFO threshold must be set-up differently. For this mode to operate correctly:

- BT[4:0] = 2*burst-size – 1
  Where burst-size is in units of blocks (1 block = 16 bytes).

While the TXSDQ’s FIFO threshold is set so it transitions when less than 2 bursts remain available, the TPAHOLD feature will hold PTPA high until there is less than 1 burst available. Thus, the user can still fully utilize the entire FIFO.

Because we usually want the TXSDQ block’s data threshold (DT[7:0]) to be a fairly large value to prevent FIFO underruns, the burst-size must be set to a reasonable value (see Section 13.30 for restrictions on the relationship between TXSDQ’s DT[7:0] and BT[4:0]).

Figure 50 TPAHOLD Set To 1



13.34 Setting ATM Mode of Operation over Utopia L3 or POS-PHY L3

ATM is the default operation mode for the S/UNI MULTI-48 device. The following operational sequence should be used to prepare an ATM channel.

1. Input pin PL3EN (logically XORed with the PL3EN bit of register 0004H) must be tied to logic 1 to enable mixed-ATM/POS operation or to logic 0 for pure ATM operation with UTOPIA Level 3 interface. The POS-PHY L3 interface must be used for dual-mode operation.

2. Unprovision (disable) all line-side timeslots and system side channels that are to be changed. This is to be done in the TCAS12, RCAS12, TCFP, RCFP, TTDP, RTDP, RXSDQ, and TXSDQ blocks. The FIFOs of the corresponding channels will be reset and emptied when they are unprovisioned.

3. Leave the TXSDQ and RXSDQ BT[4:0] and DT[7:0] values equal to their default values of 3. See Sections 13.30 and 13.31 for details.

4. Set the POS_SEL register bits in the TCFP, RCFP, TTDP, and RTDP blocks to logic 0 for the desired ATM channels. Optionally set the POS_SEL register bits RXSDQ and TXSDQ blocks to 0 for the desired ATM channels if runt cell detection is required at the expense of reduced bandwidth. The RXSDQ and TXSDQ will still process cells correctly, though without the size checking if configured for POS traffic.

5. Optionally, reset the performance monitoring counters in all blocks by writing to the S/UNI MULTI-48 Global Performance Monitor Update register. TIP remains high as the performance monitoring registers are loaded, and is set to a logic zero when the transfer is complete.

13.35 Setting Packet Mode of Operation Over POS-PHY L3

The following operational sequence should be used to prepare a channel for Packet operation without affecting other channels.

1. Input pin PL3EN (logically XORed with the PL3EN bit of register 0004H) must be tied to logic 1 to enable the POS-PHY L3 system interface.

2. Unprovision (disable) all line-side timeslots and system side channels that are to be changed. This is to be done in the TCAS12, RCAS12, TCFP, RCFP, TTDP, RTDP, RXSDQ, and TXSDQ blocks. The FIFOs of the corresponding channels will be reset and emptied when they are unprovisioned.

3. Set the POS_SEL register bits in the TCFP, RCFP, TTDP, RTDP, RXSDQ, and TXSDQ blocks to logic 1 for the desired POS/HDLC channels.

4. Program the RXPHY servicing algorithm. See Section 13.32 for details.

5. Set the RXSDQ Data Available threshold (DT[7:0]) values to the desired values. See Section 13.31 for details.

6. Enter the RXPHY BURST_SIZE[3:0]. See Section 13.31 for details.

7. Enter the TXSDQ Buffer Available Threshold (BT[4:0]). See Section 13.30 for details.

8. Enter the TXSDQ Data Available Threshold (DT[7:0]). See Section 13.31 for details.

9. Optionally, reset the performance monitoring counters in all blocks by writing to the S/UNI MULTI-48 Global Performance Monitor Update register. TIP remains high as the performance monitoring registers are loaded, and is set to a logic zero when the transfer is complete.

13.36 Setting Transparent Mode of Operation Over POS-PHY L3

To send transparent data from the POS-PHY L3 bus, configure the S/UNI MULTI-48 device for Packet Over SONET mode as in Section 13.40.1 with the following amendments:

1. Set the DELINDIS bits and clear the CRC_SEL bits of the TCFP and RCFP (for STS-12c or STS-48c channels) or of the TTDP and RTDP (for lower rate channels). Make sure that RBY_MODE is set in the RCFP to insure proper byte counting.

2. Make sure that the FIFO on the transmit side will never underrun. A FIFO underrun in Transparent mode would result in data corruption.

3. Data should be transferred over the POS-PHY Level 3 bus broken up into 64 byte packets.

13.37 Example Set-up

The following is an example configuration for an STS-3c/VC-4 bidirectional channel residing at line-side timeslots S4,1, S4,2, and S4,3 and system-side timeslots S4,1, S4,2, and S4,3 and channel/PHY address 3.

1. Set RSTS12C[1] and RSTS12CSL[1] register bits in the S/UNI MULTI-48 Line Side Receive Configuration register (0006H) to ‘b0.

2. Set TSTS12C[1] and TSTS12CSL[1] register bits in the S/UNI MULTI-48 Line Side Transmit Configuration register (0007H) to ‘b0.

3. Set up the RXSDQ and TXSDQ as follows for PHYID = 3:

    a. Assuming timeslots (S1,1, S1,2, S1,3), (S2,1, S2,2, S2,3) and (S3,1, S3,2, S3,3) consist of STS-3 data streams with FIFO sizes of 48 Blocks, BLOCK_PTR[4:0] for the channel in question can be calculated to be 12H, FIFO_NUMBER[5:0] is set to 03, and FIFO_BS[1:0] is set to 0x2.

    b. Set POS_SEL to logic 1 for POS/HDLC traffic or 0 for ATM traffic.

    c. Set TXSDQ BT[4:0] and DT[7:0] to 0x3 for an ATM channel. Otherwise set them according to the constraints described in Sections 13.30 and 13.31.

    d. Set RXSDQ DT[7:0] to 0x3 for an ATM channel. Otherwise set them according to the constraints described in Section 13.31.

4. Configure the RXPHY as follows:

    a. If using the POS-PHY L3 interface, set the CALENDAR_LENGTH[6:0] value to 0FH to allow 16 calendar entries.

    b. If using the POS-PHY L3 interface, for CALENDAR_ADDR[6:0] values of 03H set CALENDAR_DATA[5:0] equal to 03H. This allows the S/UNI MULTI-48 polling mechanisms to poll channel number 3 one time out of 16. The sequence is spread out evenly amongst the 16 calendar sequences.

    c. Set ODDPARITY to configure the parity to be generated.

    d. Set RSXPAUSE[1:0] to set the pausing between POS-PHY L3 transfers to the desired level.

    e. Set BURST_SIZE[3:0] for PHY_ADDR[5:0] = 0x3 (see Section 13.31). If an ATM PHY, set BURST_SIZE[3:0] to the value 0x3.

5. Configure the TXPHY as follows:

    a. Set ODDPARITY to configure the parity to be generated.

    b. Set PARERREN to select if parity errors are to cause packets to be aborted.

6. Configure the RTDP at RTDP_BASE = 0340H as follows for CHAN[3:0] = 3:

    a. Set the POS_SEL to 1 if processing POS. Set to logic 0 for ATM.

    b. Set CRC_SEL[1:0] for desired CRC type.

7. Configure the TTDP at TTDP_BASE = 1340H as follows for CHAN[3:0] = 3:

    a. Set the POS_SEL to 1 if processing POS. Set to logic 0 for ATM.

    b. Set CRC_SEL[1:0] for desired CRC type.

8. Configure the RCAS12 at RCAS12_BASE = 0360H for Timeslots ***x*** = 3, 7, and 11 as follows:

    a. Set TS***x***_CHAN[3:0] = 3.

    b. Set TSx_MODE[2:0] = ‘b001.

    c. Set TS***x***_PROV = 1.

9. Configure the TCAS12 at TCAS12_BASE = 1360H for Timeslots ***x*** = 3, 7, and 11 as follows:

    a. Set TS***x***_CHAN[3:0] = 3.

    b. Set TSx_MODE[2:0] = ‘b001.

    c. Set TS***x***_PROV = 1.

10. Configure the SIRP at SIRP_BASE = 1260H for Timeslots ***x*** = 3 as follows:

    a. Set PROV = 1.

    b. Set TS3_RDI20F, and TS3_ERDI to the desired alarm reporting mode.

    c. Set the RDIPRIHI[1:0] and RDIPRIMID[1:0] and LCD[1:0] bits for the desired alarm reporting mode.

11. Set SDQRST = 0 in RXSDQ and TXSDQ.

12. Set ENABLE = 1 in RXSDQ and TXSDQ for PHY_ID = 3. Ensure all other information for the indirect write to PHY_ID = 3 is unchanged from the previous SDQ configs.

13. Set RTDP (at RTDP_BASE = 0340H, channel number 3) PROV = 1.

14. Set TTDP (at TTDP_BASE = 1340H, channel number 3) PROV = 1.

15. Set TCAS12 (at TCAS12_BASE = 1360H) CH3_DIS = 0.

16. Set RCAS12 (at RCAS12_BASE = 0360H) CH3_DIS = 0.

17. Set TXPHY TXPRST = 0.

18. Set RXPHY RXPRST = 0.

13.38 Dynamically Reprovisioning Channels to Different Rates

The S/UNI MULTI-48 device allows dynamic modification of channel rates without affecting other channels. For instance, a single STS-12c/VC-4-4 channel can be broken up into 4 separate STS-3c/VC-4 channels. The following are the steps required:

1. Find the system side timeslots associated with the channel to be modified.

2. If the dynamic modification involves a data-rate of STS-3c, disable any independent software process that might counter polling process update counters in the S/UNI MULTI-48.

3. In the RCAS12 and TCAS12 blocks, set CH***x***_DIS to logic 1 for the affected channels.

4. In the RCAS12, TCAS12, and SIRP blocks, set TS***x***_PROV to logic 0 for the affected system timeslots.

5. Reconfigure the affected RSTS12C[x] and RSTS12CSL[x] register bits in the S/UNI MULTI-48 Line Side Receive Configuration register.

6. Reconfigure the affected TSTS12C[x] and TSTS12CSL[x] register bits in the S/UNI MULTI-48 Line Side Transmit Configuration register.

7. Reconfigure the affected SYS_RSTS12C[x] and SYS_RSTS12CSL[x] register bits in the S/UNI MULTI-48 System Side Receive and Transmit Configuration register.

8. Reconfigure the affected SYS_TSTS12C[x] and SYS_TSTS12CSL[x] register bits in the S/UNI MULTI-48 System Side Receive and Transmit Configuration register.

9. Reset the PROV bits in the affected channels in the TCFP, TTDP, RCFP, and RTDP blocks.

10. Reconfigure the RXSDQ and TXSDQ as described in Section 13.29. Use the FLUSH bit for the affected FIFO_PTR addresses to clear the FIFOs. Make sure EMPTY = 1 for each affected FIFO_PTR then write 0 to FLUSH for each affected FIFO_PTR.

11. Reconfigure the RXPHY's calendar to match the new channel rates. See Section 13.32.

12. Reconfigure the RCAS12, TCAS12, and SIRP blocks so the timeslots involved in the modified channel correspond to the proper channel rate using the TS***x***_MODE and TS***x***_CHAN bits. Set the TS***x***_PROV bits for these timeslots. Leave the CH***x***_DIS bits asserted for the new channel(s).

13. Reconfigure the TCFP, TTDP, RCFP, and RTDP for the new channel. Set the PROV bits for the new channel(s).

14. Clear the CH***x***_DIS bits associated with the new channel(s) to enable the new channel(s).

15. Re-enable any suspended software processes that update counters in the S/UNI MULTI-48.

13.39 Cell/packet processors and FIFOs Error Recovery

13.39.1 RXSDQ FIFOs losing ATM cell alignment

In a rare event, upon S/UNI MULTI-48 initialization and configuration or when APSIFP resynchronizations occur, the RXSDQ state machine may not recover to an ATM cell alignment if its FIFO has been set to ATM mode (POS_SEL = 0 in register 0329H). This can be diagnosed when RXSDQ asserts continuous SOP and EOP interrupts for a specific channel.

Workarounds

If using the PL3 interface, this lock-up condition can be avoided by setting the RXSDQ FIFOs to packet mode (POS_SEL = 1 in regiser 0329H) for both ATM and packet channels. Functional behaviour will not be affected by this change from an ATM FIFO to a packet FIFO.

To detect the lock-up state and to implement the workaround when using the UL3 interface with the RXSDQ FIFOs enabled in ATM mode (POS_SEL = 0 in register 0329H), the EOP and SOP interrupts must first be enabled (i.e., EOPE and SOPE bits in register 0321H).

Upon detection of continuous EOP and SOP interrupts (i.e., EOPI bit in register 0324H and SOPI bit in register 0325H) for a specific channel, the following recovery procedure should be used in order to resume normal operation:

14. Disable the affected FIFO (based on EOP/SOP_FIFO fields content) using the ENABLE bit from register 0329H (RXSDQ FIFO Indirect Configuration).

15. Flush the affected FIFO content using the FLUSH bit from register 0328H (RXSDQ FIFO Indirect Address).

16. Enable back the needed FIFO using the ENABLE bit from register 0329H (RXSDQ FIFO Indirect Configuration).

13.40 System Interface Error Recovery

13.40.1 UTOPIA Level 3 Transmit Interface Misalignment Recovery

On the Transmit UL3 interface, cell alignment is done on logic 1-to-0 transition of TENB. That is, TSOC is expected on the same cycle where TENB has just transitioned to logic 0. Thus, if the upstream device has misalignment between its TENB and TSOC, the S/UNI MULTI-48 device will align its cells to the TENB and may give error indications on its RUNTCELLI (TXPHY Interrupt Status register,) and/or SOPI interrupt (TXSDQ SOP Error Port and Interrupt Indication). Once the upstream device has realigned its signals, the S/UNI MULTI-48 device will realign on the next 1-to-0 transition of TENB.

13.40.2 UTOPIA Level 3 Receive Interface Misalignment Recovery

On the Receive UL3 interface, cell transfer is aligned to the RENB signal. Once asserted to logic 0, RENB must not deassert until cycle P11 of a cell. The S/UNI MULTI-48 device will not respond to early deassertions of RENB and will continue transfer of the cell in progress.

To realign the S/UNI MULTI-48 device to the downstream device, the RENB must remain deasserted for more than 13 clock cycles. This will guarantee that the S/UNI MULTI-48 device has completed transfer of any cell and the next cell will be aligned to RENB.

This means that RENB cannot be tied low with the downstream device expecting to align using the RSOC output of the S/UNI MULTI-48 device.

The alternate method to realign cells is to unprovision the RCFP/RTDP and then unprovision and flush the RXSDQ. When the RXSDQ and RCFP/RTDP are restarted, the cells will be properly aligned to RENB.

13.40.3 UTOPIA Level 3 Transmit Clock (TFCLK) Error Recovery

When the TFCLK is taken away and restored or is corrupted by a glitch in UL3 mode, the TxDLL will indicate an error by asserting the ERRORI register bit in the TxDLL Control Status register. The S/UNI MULTI-48 may also generate continuous SOPI interrupts in the TXSDQ block or RUNTCELLI interrupts in the TXPHY block which indicate a misalignment state.

When this condition is detected, the following recovery procedure should be used:

1. Detect TxDLL ERRORI interrupt
2. Reset the TxDLL by writing to the TxDLL Delay Tap Status register
3. Unprovision and flush the TXSDQ to stop the upstream device from transmitting (TXSDQ FIFO Indirect Configuration, bit 15 and TXSDQ FIFO Indirect Address, bit 13)
4. Reset the TXPHY
5. Clear the reset on the TXPHY
6. Clear the flush bit and provision the TXSDQ

13.40.4 UTOPIA Level 3 Receive Clock (RFCLK) Error Recovery

When the RFCLK is taken away and restored or is corrupted by a glitch in UL3 mode, the S/UNI MULTI-48 device's RxDLL will indicate an ERRORI interrupt. The system-side link-layer device may get continuous RSOC errors and the RXPHY block may give continuous RUNTCELLI interrupts.

When this condition is detected, the following recovery procedure should be used:

1. Detect RxDLL ERRORI interrupt
2. Reset the RFCLK_DLL by writing to the RxDLL Delay Tap Status register

3. Unprovision the RCFPs and RTDPs cell/packet processors

4. Unprovision and flush the RXSDQ (RXSDQ FIFO Indirect Configuration, bit 15 and RXSDQ FIFO Indirect Address, bit 13)

5. Reset the RXPHY

6. Clear the reset on the RXPHY

7. Clear the flush bit and provision the RXSDQ

8. Provision the RCFPs and RTDPs

13.40.5 POS Level 3 Transmit (TFCLK) Error Recovery

When the TFCLK is taken away and restored or corrupted by a glitch in PL3 mode, the TxDLL will indicate an ERRORI interrupt. In some cases the S/UNI MULTI-48 TXSDQ also asserts SOPI and EOPI interrupts.

When this condition is detected, the following recovery procedure should be used:

1. Detect ERRORI interrupt in TXDLL Control Status Register

2. Reset the TxDLL (write to register TXDLL Delay Tap Status/DLL Reset)

3. Disable the TXSDQ FIFO (TXSDQ FIFO Indirect Configuration, bit 15)

4. Flush the TXSDQ FIFO (TXSDQ FIFO Indirect Address, bit 13)

5. Reset the TXPHY

6. Clear the reset on the TXPHY

7. Enable the TXSDQ (TXSDQ FIFO Indirect Configuration, bit 15)

13.40.6 POS Level 3 Receive (RFCLK) Error Recovery

When the RFCLK is taken away and restored or corrupted by a glitch in PL3 mode, the system side link-layer device may get continuous RSOP errors. The RxDLL indicates an ERRORI interrupt.

When this condition is detected, the following recovery procedure should be used:

1. Detect RxDLL ERRORI bit asserted [RXDLL Control Status register, bit 5].
   Note: upstream device may get continuous RSOP errors.

2. Reset the RxDLL [write to register RXDLL Delay Tap Status/DLL Reset]

3. Unprovision the upstream cell/packet processor (RCFPs and RTDPs)

4. Disable the RXSDQ FIFO [RXSDQ FIFO Indirect Configuration register, bit 15]

5. Flush the RXSDQ FIFO [RXSDQ FIFO Indirect Address register, bit 13]

6. Reset the RXPHY

7. Clear the reset on the RXPHY

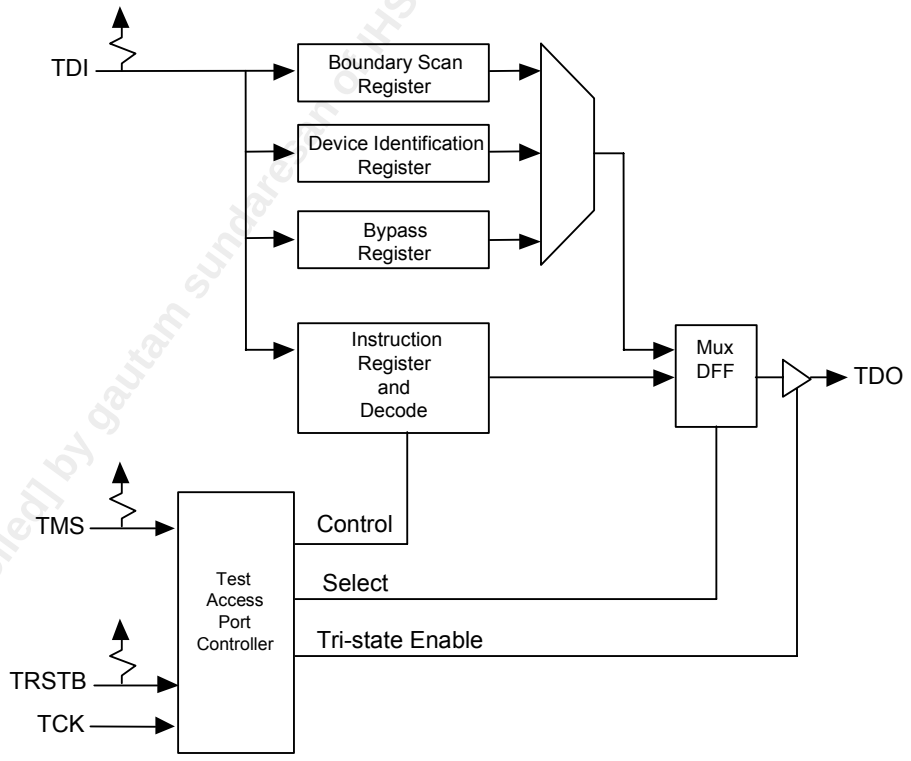
8. Clear the flush bit and enable the RXSDQ FIFO [RXSDQ FIFO Indirect Configuration register, bit 15]

9. Provision the RCFPs and RTDPs

13.41 JTAG Support

The S/UNI MULTI-48 device supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI, and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TRSTB should be tied to RSTB if the JTAG interface is not used. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

Figure 51 Boundary Scan Architecture



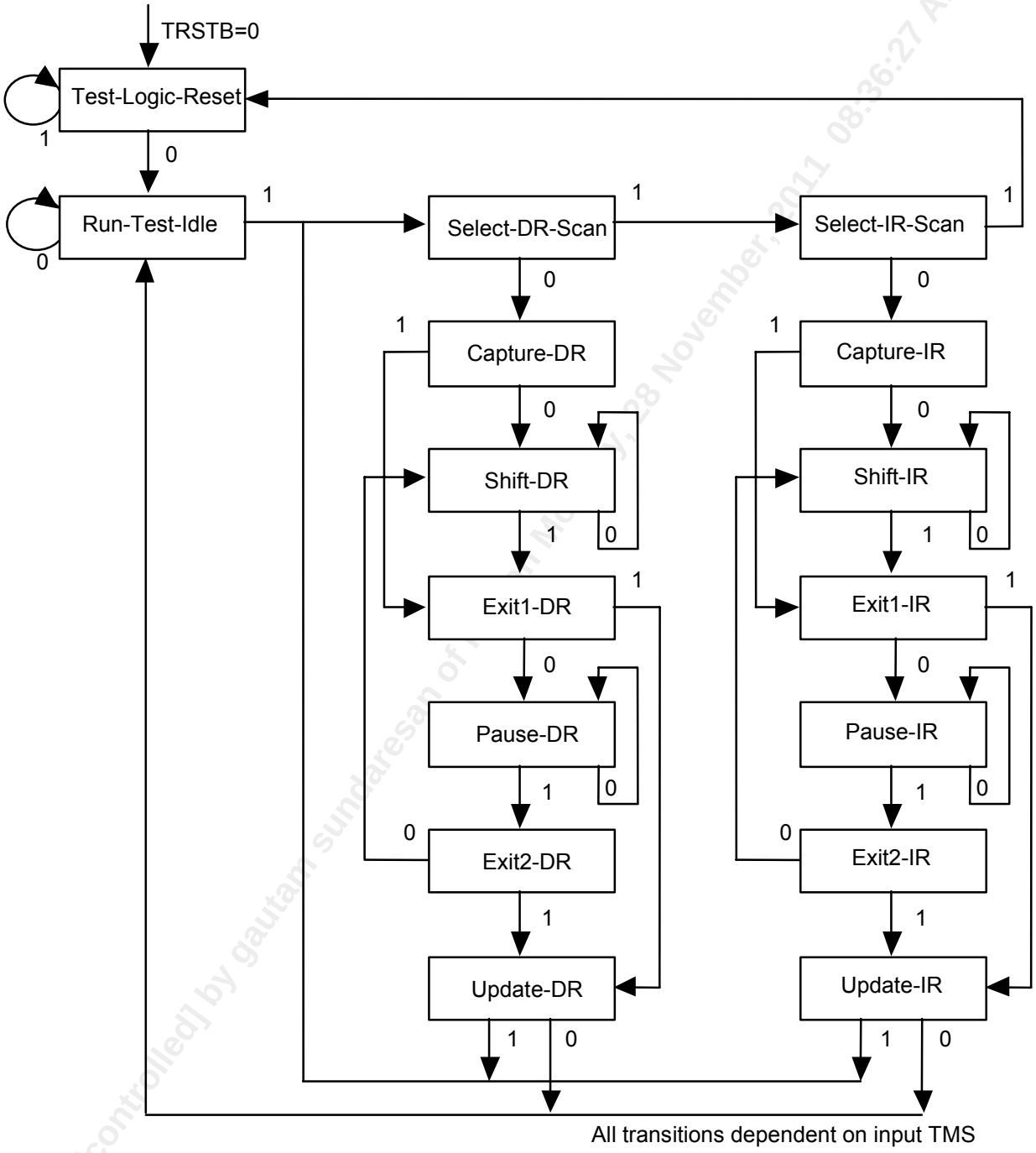
The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register, and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

13.41.1 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

Figure 52 TAP Controller Finite State Machine



13.41.2 States

Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

Boundary Scan Instructions

The following is a description of the standard instructions. Each instruction selects a serial test data register path between input, TDI and output, TDO.

13.41.3 Instructions

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

14 Functional Timing

14.1 Receive Transport Overhead

Figure 53 RTOH Output Timing

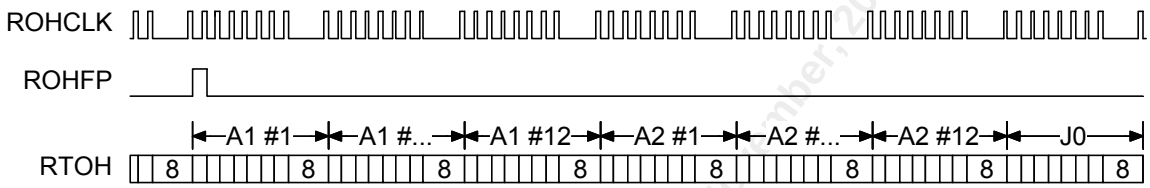


Figure 54 RTOH and RTOHFP Output Timing

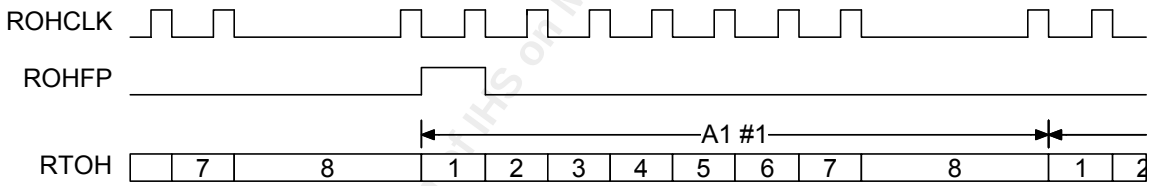


Figure 53 shows the receive transport overhead (RTOH) functional timing for STS-48/STM-16 or STS-12/STM-4 mode. The same figure applies when the S/UNI MULTI-48 is processing STS-3/STM-1 stream(s), only there are only three of each A1 and A2 bytes instead of twelve.

When the device is processing STS-48/STM-16 or STS-12/STM-4 stream(s), RTOHCLK is a 20.736 MHz clock generated by gapping a 25.92 MHz clock (33% high duty cycle). 2592 bits (9x3x12 bytes) are output on RTOH between two RTOHFP assertions. When the device is processing STS-3/STM-1 stream(s), RTOHCLK is a 5.184 MHz clock generated by gapping a 6.48MHz clock (33% high duty cycle).

Figure 54 shows that RTOH and RTOHFP are aligned with the falling edge of RTOHCLK. The rising edge of RTOHCLK should be used to sample RTOH and RTOHFP. Sampling RTOHFP high identifies the MSB of the first A1 byte on RTOH.

14.2 Transmit Transport Overhead

Figure 55 TTOH and TTOHEN Input Timing

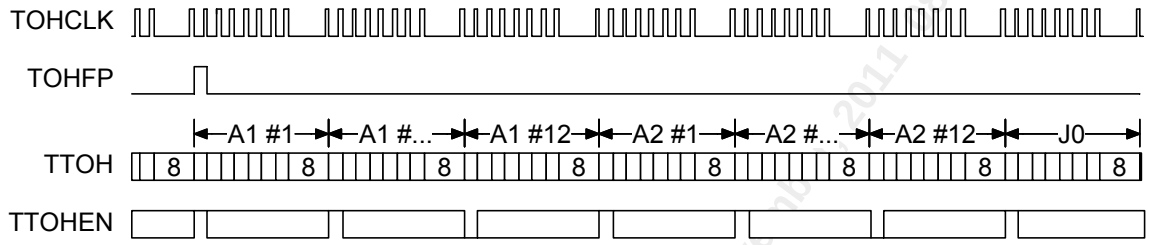


Figure 56 TTOH and TOHFP Input Timing

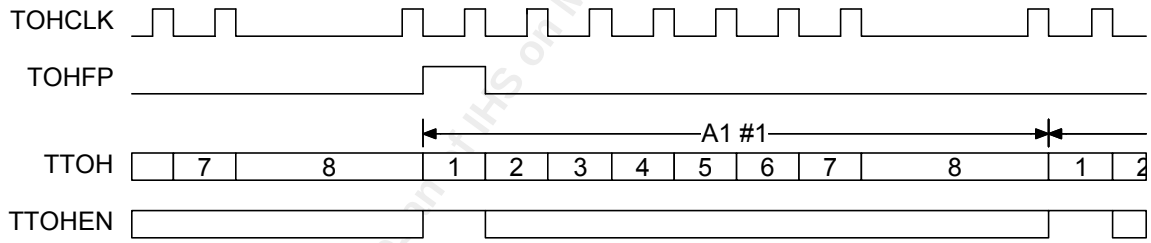


Figure 55 shows the transmit transport overhead (TTOH) functional timing for STS-48/STM-16 or STS-12/STM-4 mode. The same figure applies when the S/UNI MULTI-48 is processing STS-3/STM-1 stream(s), only there are only three of each A1 and A2 bytes instead of twelve.

When the device is processing STS-48/STM-48 or STS-12/STM-4 stream(s), TOHCLK is a 20.736 MHz clock generated by gapping a 25.92 MHz clock (33% high duty cycle). 2592 bits (9x3x12 bytes) are input on TOH between two TOHFP assertions. When the device is processing STS-3/STM-1 stream(s), RTOHCLK is a 5.184 MHz clock generated by gapping a 6.48MHz (33% high duty cycle).

TTOHEN is used to validate the insertion of the corresponding byte on TTOH. When TTOHEN is sampled high on the MSB of the byte, the byte will be inserted in the transport overhead. When TTOHEN is sampled low on the MSB of the byte, the byte is not inserted. TTOH and TTOHEN are sampled with the rising edge of TOHCLK. TOHFP is aligned with the falling edge of TOHCLK. The rising edge of TOHCLK should be used to sample TOHFP. Sampling TOHFP high identifies the MSB of the first A1 byte on TTOH.

14.3 Receive SONET Path Alarms

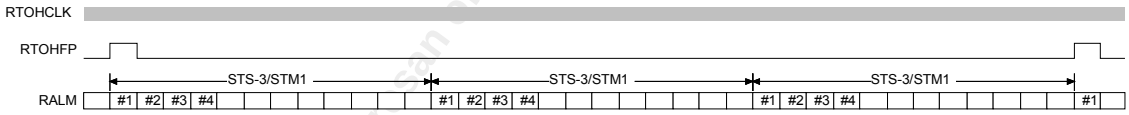
Figure 57 shows the receive path alarm functional timing. RALM is used to output the "ORing" of the enabled path defects. RALM[x] is timed off of RTOHCLK.

RTOHFP high identifies clock cycle 1 of 2592 in single STS-48/STM-16 or in quad STS-12/STM-4 processing modes. RTOHFP high identifies clock cycle 1 of 648 in quad STS-3/STM-1 processing mode.

Only the first 72 cycles (cycles 1 to 72) of RALM[1] contain necessary information in STS-48c/VC-4-16c processing mode. When the SONET processing slice handles an STS-12c/VC-4-4c payload or when the SONET processing slice handles an STS-3/STM-1 data stream, only the first 72 cycles (cycles 1 to 72) of RALM[x] contain necessary information. When the SONET processing slice handles four STS-3c/VC-4 payloads, the cycles 1-72 of RALM[x] contain necessary information for the first STS-3/STM-1, the cycles 73-144 of RALM[x] contain necessary information for the second STS-3/STM-1, the cycles 145-216 of RALM[x] contain necessary information for the third STS-3/STM-1, the cycles 217-288 of RALM[x] contain necessary information for the fourth STS-3/STM-1.

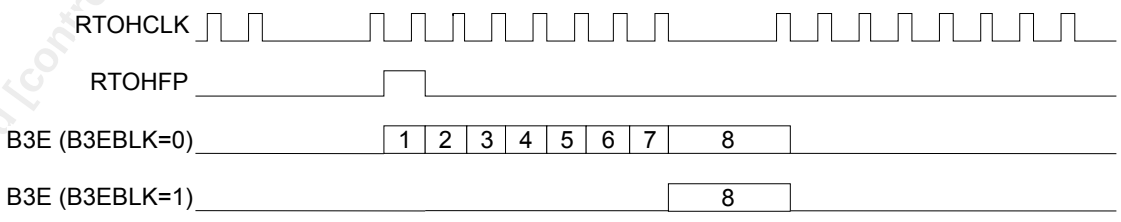
The information is repeated once every 864 cycles in single STS-48/STM-16 or in quad STS-12/STM-4 processing modes. The information is repeated once every 216 cycles in quad STS-3/STM-1 processing mode.

Figure 57 RALM Output Timing (processing 4 STS-3c/VC-4)



The path BIP-8 errors are output on the B3E serial output as shown in Figure 58. The error count is output once every B3 bytes on one of the three opportunities. These opportunities appear on B3E every 864 cycles in single STS-48/STM-16 or in quad STS-12/STM-4 processing modes. These opportunities appear on B3E every 216 cycles in quad STS-3/STM-1 processing mode. The path numbering follows the rules used for the RALM output signal.

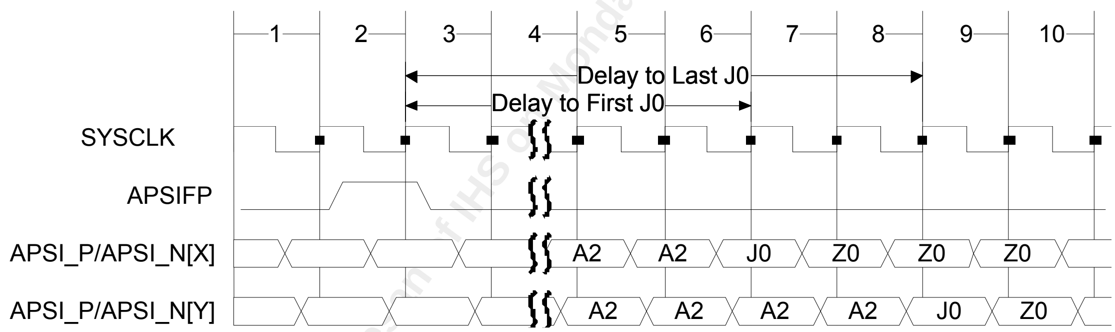
Figure 58 B3E Output Timing



14.4 Incoming APS Serial TelecomBus

Figure 59 shows the relative timing of the incoming APS serial TelecomBus LVDS links. Links carry SONET/SDH frame octets that are encoded in 8B/10B characters. Frame boundaries, justification events, and alarm conditions are encoded in special control characters. The upstream devices sourcing the links share a common clock and have a common transport frame alignment that is synchronized by the APS Input Frame Pulse signal (APSIFP). Due to phase noise of clock multiplication circuits and backplane routing discrepancies, the links will not phase aligned to each other but are frequency locked. The delay from APSIFP being sampled high to the first and last J0 character is shown in Figure 59. In this example, the first J0 is delivered by one of the four APSI links (APSI+/APSI-). The delay to the last J0 represents the time when the all the links have delivered their J0 character. In the example below, one of the links (APSI+[Y]/APSI-[Y]) is shown to be the slowest. The external system must ensure that the relative delays between all the APSI LVDS links be less than 16 bytes (approximately 205ns). The relative phases of the links in Figure 59 are shown for illustrative purposes only.

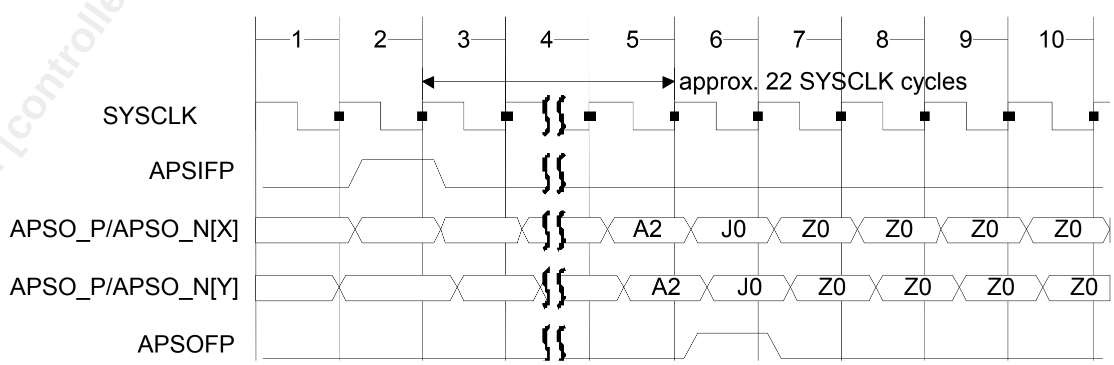
Figure 59 APSI Serial TelecomBus Link Timing



14.5 Outgoing APS Serial TelecomBus

Figure 60 shows the timing relationships around the APSIFP signal. The Outgoing APS J0 Frame Pulse (APSOFP) signal indicates the approximate time at which the J0 byte is available on the output APS LVDS links. Note the default time between APSIFP and APSOFP is approximately 22 SYSCLK (from SYSCLK pin or based on REFCLK155/77_P/N) cycles.

Figure 60 Outgoing APS Serial TelecomBus



14.6 ATM UTOPIA Level 3 System Interface

The ATM UTOPIA Level 3 System Interface is compatible with the UTOPIA Level 3 specification. The S/UNI MULTI-48 device only supports the 32-bit mode of operation and PHY addresses (channels) from 0 to 15.

14.6.1 Transmit UL3 Interface

The Transmit UTOPIA Level 3 System Interface Timing diagrams (Figure 61 and Figure 62) illustrate the operation of the system side transmit UL3 interface. The single PHY case shown in Figure 61 illustrates the behavior of the TCA signal. At the start of cycle 4, there is only enough FIFO buffer space for the cell being transferred so TCA is deasserted. The deassertion occurs on the TFCLK edge **after** TSOC of the cell (cell#1) being written to the FIFO is sampled. This cell will take the last remaining cell buffer space in the FIFO. This TCA behavior is consistent with the Utopia L3 specification which states that TCA is invalid on the TFCLK edge that initiates the transition of TSOC to logic 1.

On cycle 5, a cell has been read out of the FIFO to the S/UNI MULTI-48 core so it now has room to accommodate the cell currently being transferred (cell#1) plus one additional cell (cell#2). At the start of cycle 8, the transfer of cell#1 is completed. TCA remains high because there is still buffer space for one more cell. At the start of cycle 10, transfer of cell#2 starts. TCA is deasserted at cycle 11 because besides the space for holding cell#2, there is no FIFO space for any more cells.

TCA will be deasserted for polling cycles during the first three cycles of a cell transfer for the PHY being transferred. That is, for cycles 3, 4, and 5 the PHY currently transferring a cell will say it has no more room even if it does. This prevents a false positive on TCA before the FIFO fill level can be re-evaluated.

Note that the single-PHY mode is handled exactly like the multi-PHY mode except that the PHY address is held at the value 0. If TENB is held low, back-to-back cell transfers on the same PHY can be performed without a dead cycle.

TSOC must be high during the first byte of the ATM cell structure and must be present for the start of each cell. Thus, TSOC will mark the H1 byte. If TSOC is asserted at the wrong time (not at proper cell boundaries), a corrupted (but complete) cell will be transmitted from the S/UNI MULTI-48 device. This corrupted cell will contain the bytes from the runt cell transferred through the UL3 interface plus some random bytes to fill the remainder of the ATM cell.

The multi-PHY timing diagram of Figure 62 shows the TCA polling mechanism. The buffer available status is given on the next rising TFCLK edge after the address on TADR[3:0] is sampled. Also shown is how different PHYs are selected for data transfer. When TENB is logic 1, the address on TADR[3:0] is selected as the PHY for the next transfer once TENB returns to logic 0.

Figure 61 Transmit UTOPIA Level 3 System Interface Timing for Single PHY

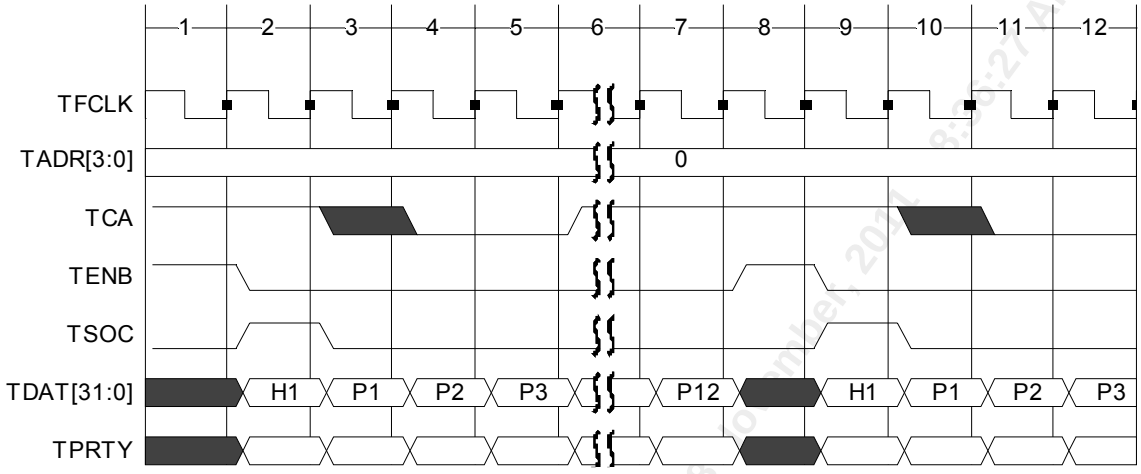
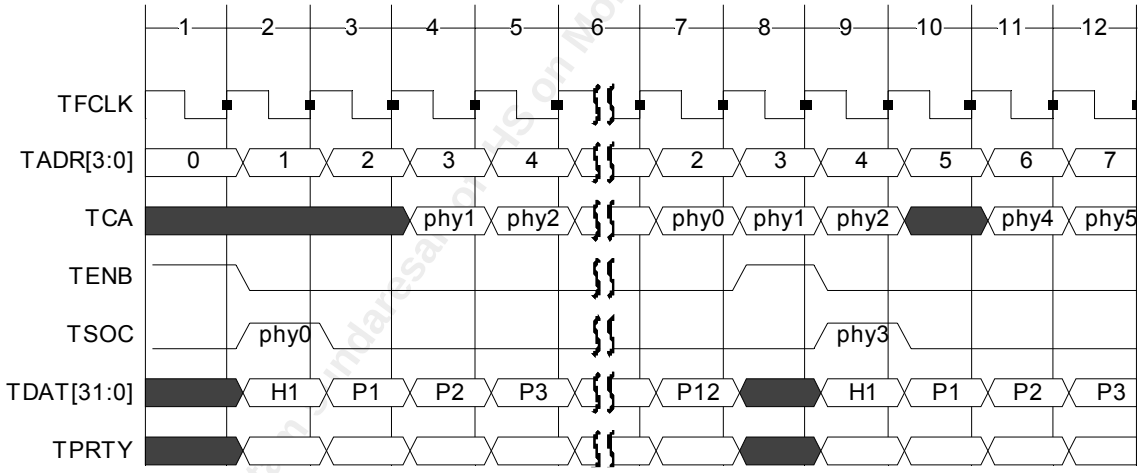


Figure 62 Transmit UTOPIA Level 3 System Interface Timing for Multi-PHY



14.6.2 Receive UL3 Interface

The Receive UTOPIA Level 3 System Interface Timing diagrams (Figure 63 and Figure 64) illustrate the operation of the system side receive interface.

The single PHY case shown in Figure 63 illustrates the behavior of the RCA signal. At the start of cycle 3, RENB is sampled low which initiates a cell transfer from the S/UNI MULTI-48. The transfer begins at cycle 4. The response to RENB always occurs on the rising RFCLK edge following the RFCLK edge which samples RENB. Also note that RENB must remain asserted during a cell transfer as specified by the Utopia L3 standard. In Figure 63, this occurs on the rising edge of RFCLK at the start of cycle 9.

RCA is deasserted in cycle 4 and 11 coincident with the RSOC assertion indicating that the cell transfer which has just started contains the last cell in the FIFO at this time. RCA may be asserted at any time due to the insertion of a complete cell into the FIFO.

RCA will be deasserted for polling cycles during the first two cycles of a cell transfer for the PHY being transferred. That is, for cycles 4 and 5 the PHY currently transferring a cell will say it has no more data even if it does. This prevents a false positive on RCA before the FIFO fill level can be re-evaluated.

Back-to-back cells from the same PHY can be handled by holding RENB asserted at logic 0 during cycle 8. In this case, cycle 10 for RSOC, RDAT[31:0], and RPRTY will be eliminated and the following cycles will be advanced. Otherwise, the single-PHY mode is handled exactly like the multi-PHY mode except that the PHY address is held at the value 0.

The multi-PHY timing diagram of Figure 64 shows the RCA polling mechanism. The data available status is given on the next rising RFCLK edge after the address on RADR[3:0] is sampled. Also shown is how different PHYs are selected for data transfer. When RENB is logic 1, the address on RADR[3:0] is selected as the PHY for the next transfer once RENB returns to logic 0.

Figure 63 Receive UTOPIA Level 3 System Interface Timing for Single PHY

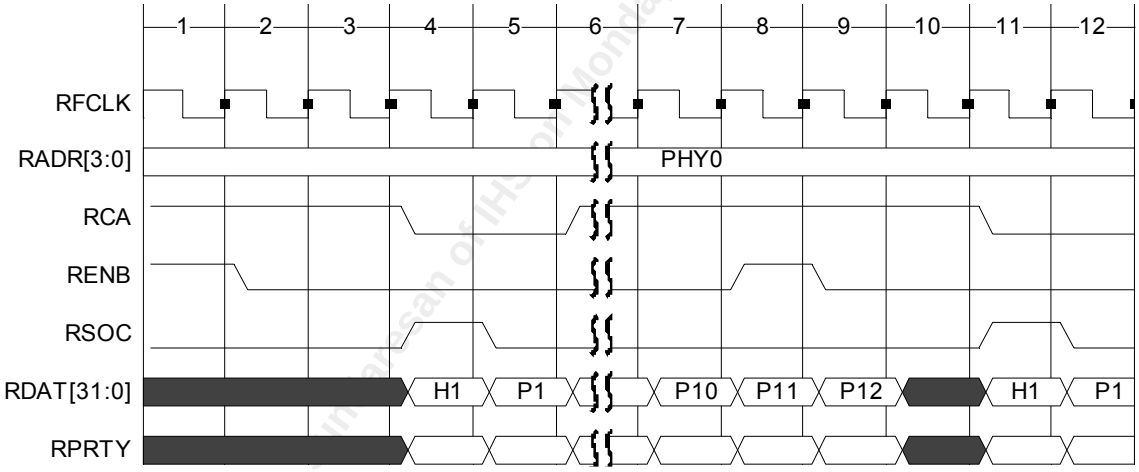
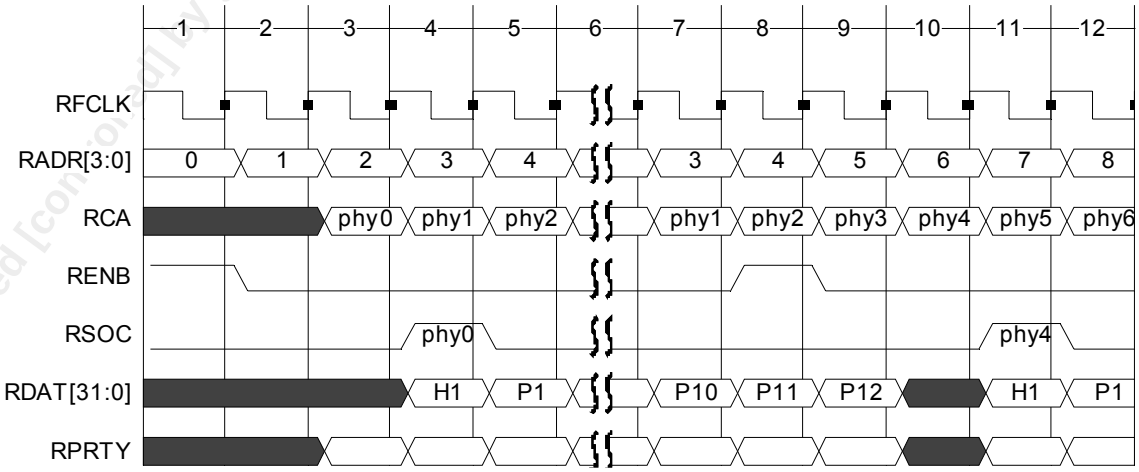


Figure 64 Receive UTOPIA Level 3 System Interface Timing for Multi-PHY



14.7 Packet over SONET (POS) Level 3 System Interface

The Packet over SONET (POS) Level 3 System Interface is compatible with the POS-PHY Level 3 specification. The S/UNI MULTI-48 only supports the 32-bit mode of operation.

14.7.1 Transmit PL3 Interface

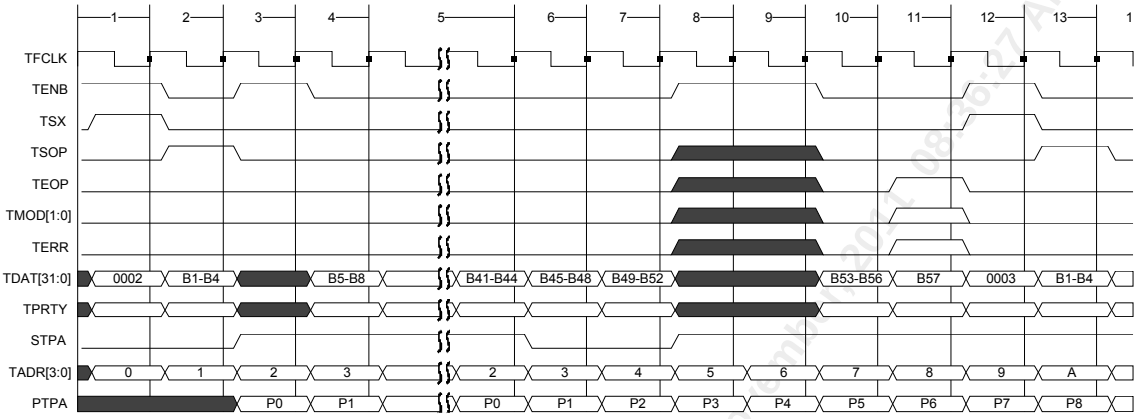
The Transmit POS Level 3 System Interface Timing diagram (Figure 65) illustrates the operation of the system side transmit FIFO interface. TENB, TSX, and TDAT[31:0] (because TSX is logic 1, TDAT[31:24] contains the Data Type Field, TDAT[7:0] contains the in-band PHY address) are asserted in cycle 1 to start the transfer. STPA responds in cycle 3 to show that there is room in the FIFO (the FIFO fill threshold is user programmable) for PHY address 2. The packet data is transferred on TDAT[31:0] starting at the rising TFCLK edge at the start of cycle 3. TSOP is also asserted at this cycle to indicate the data on TDAT[31:24] contains the start-of-packet byte. TENB is deasserted in cycle 3 by the upstream device to pause the transfer. Data transfer continues in cycle 4. In cycle 6, STPA is deasserted indicating that the FIFO for PHY address 0 has fallen below the data available threshold (TXSDQ's BT[4:0] register bits). In the example shown here, the upstream device responds by stopping its transfer immediately at cycle 9 by deasserting TENB. With most set-up configurations, the upstream device does not need to stop immediately. It can complete the transfer of one more burst before stopping.

Because STPA is asserted again on cycle 8, transfers can be conducted again. TENB is asserted again before cycle 11 to continue the transfer. In cycle 11, TEOP is asserted to indicate that TDAT[31:0] contains one byte which is the end of the packet. TMOD[1:0] is valid at the same time to indicate which bytes in TDAT[31:0] contain valid data and thus the last byte of the packet can be inferred. TERR is also valid during this cycle to indicate whether or not this packet should be aborted because of an upstream error. If TERR is logic 1, the packet will be aborted by the S/UNI MULTI-48's packet processor.

In cycle 12, TENB is deasserted and TSX is asserted to select a different PHY to transfer data to.

TSOP must be high during transfers which contain the first byte of a packet. TEOP must be high during transfers which contain the last byte of a packet. It is legal to assert TSOP and TEOP at the same time. This case occurs when TDAT[31:0] contain both the SOP and EOP. When TSOP is asserted and the previous transfer was not marked with TEOP, the system interface realigns itself to the new timing, and both the previous packet and the current packet may be corrupted and aborted.

Figure 65 Transmit POS Level 3 System Interface Timing



14.7.2 Receive PL3 Interface

The Receive POS Level 3 System Interface Timing diagram (Figure 66) illustrates the operation of the system side receive interface. The S/UNI MULTI-48 performs the polling operation internally, selects the PHY for which data is to be transferred, and pushes data to the downstream reader.

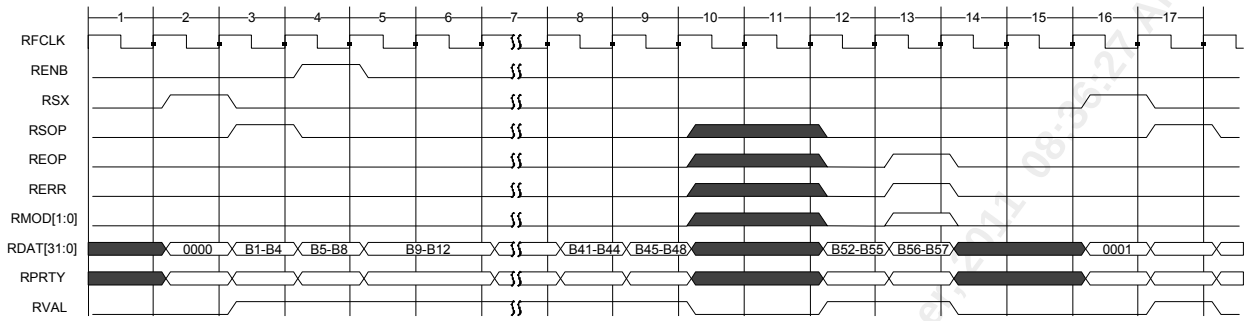
When data is available, the RVAL signal is asserted. RSX is also asserted in cycle 2 to indicate that the PHY address for which data is being transferred is present on RDAT[7:0]. RDAT[31:24] holds the Data Type Field. At cycle 3, RSOP is asserted to indicate that the RDAT[31:24] contains the first byte of a packet. RENB is deasserted in cycle 4 because the downstream device wants to pause the data transfer.

Data transfer continues until cycle 10 when RVAL is deasserted. At cycle 12 and 13, the last two transfers for the packet are performed. In cycle 13, REOP signals the last byte of the packet is contained in RDAT[31:0] and the value of RMOD[1:0] indicates which bytes in RDAT[31:0] contain valid data. RERR is asserted along with REOP if errors were detected in this packet (aborted, length violation, FIFO overrun, FCS errors) so the downstream device may discard the packet. In cycle 16, a new transfer is initiated by reasserting RSX and a new PHY address and data type on RDAT[7:0] and RDAT[31:24] respectively.

The burst length of any transfer can be limited by setting the RXPHY's BURST_SIZE[7:0] register bits. The polling algorithm used for selecting the order in which data from different PHYs are transferred is completely user programmable using the CALENDAR_LENGTH[6:0], CALENDAR_ADDR[6:0] and CALENDAR_DATA[5:0] register bits of the RXPHY.

The FIFO threshold at which data transfer begins is set by the RXSDQ's DT[7:0] register bits. ATM cells can be transferred through the PL3 interface as fixed length packets. The DT[7:0] value should be set so that only complete ATM cells are transferred.

Figure 66 Receive POS Level 3 System Interface Timing



15 Absolute Maximum Ratings

Maximum rating are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

Table 46 Absolute Maximum Ratings

Storage Temperature	-40°C to +125°C
Supply Voltage for 1.8V	-0.3V to +2.5V
Supply Voltage for 3.3V	-0.3V to +4.6V
Voltage on any PECL Compatible Pin	-0.3V to (AVDH + 0.3V)
Voltage on any LVDS Pin	-0.3V to (AVDH + 0.3V)
Voltage on any Digital Pin except for SD	-0.3V to (VDDO + 0.3V)
Voltage on SD Digital TTL input pin	-0.3V to 5.5V
Static Discharge Voltage	±1000 V
Latch-Up Current except RESK pin	±100 mA
Latch-Up Current on RESK pin	±50 mA
DC Input Current	±20 mA
Lead/Ball Temperature	+225°C
Absolute Maximum Junction Temperature	+150°C
Maximum Overshoot on Output pins *	-2V to (VDDO + 2V) for 10ns, 20mA max
Input pad overshoot tolerance	-2V to (VDDO + 2V) for 10ns, 100mA max

Note:

* Most output pins require termination circuitry.

16 Power Information

16.1 Power Requirements

Table 47 Power Requirements

Conditions	Parameter	Typ[1,3]	High[4]	Max[2]	Units
2488 Mbit/s Mode APS Enabled	IDDOP (1.8V)	2.323	—	3.540	A
	IDDOP (3.3 V)	0.392	—	0.549	A
	Total Power	5.475	6.378	—	W
2488 Mbit/s Mode APS Disabled	IDDOP (1.8V)	2.132	—	3.249	A
	IDDOP (3.3 V)	0.332	—	0.465	A
	Total Power	4.933	5.750	—	W
4 x 622 Mbit/s Mode APS Enabled	IDDOP (1.8V)	2.486	—	3.788	A
	IDDOP (3.3 V)	0.376	—	0.527	A
	Total Power	5.716	6.663	—	W
4 x 622 Mbit/s Mode APS Disabled	IDDOP (1.8V)	2.304	—	3.511	A
	IDDOP (3.3 V)	0.318	—	0.446	A
	Total Power	5.197	6.061	—	W
4 x 155 Mbit/s Mode APS Enabled	IDDOP (1.8V)	2.146	—	3.270	A
	IDDOP (3.3 V)	0.212	—	0.297	A
	Total Power	4.562	5.331	—	W
4 x 155 Mbit/s Mode APS Disabled	IDDOP (1.8V)	1.969	—	3.001	A
	IDDOP (3.3 V)	0.154	—	0.216	A
	Total Power	4.052	4.739	—	W

Notes:

1. Typical IDD values are calculated as the mean value of current under the following conditions: typically processed silicon, nominal supply voltage, T_J=60 °C, outputs loaded with 30 pF (if not otherwise specified), and a normal amount of traffic or signal activity. These values are suitable for evaluating typical device performance in a system
2. Max IDD values are currents guaranteed by the production test program and/or characterization over process for operating currents at the maximum operating voltage and operating temperature that yields the highest current (including outputs loaded to 30 pF, unless otherwise specified)
3. Typical power values are calculated using the formula:

   $$\text{Power} = \sum_i (\text{VDDNom}_i \times \text{IDDTyp}_i)$$

   Where i denotes all the various power supplies on the device, VDDNomi is the nominal voltage for supply i, and IDDTypi is the typical current for supply i (as defined in note 1 above). These values are suitable for evaluating typical device performance in a system

4. High power values are a “normal high power” estimate and are calculated using the formula:

   Power = ∑i(VDDMaxi x IDDHighi)

   Where i denotes all the various power supplies on the device, VDDMaxi is the maximum operating voltage for supply i, and IDDHighi is the current for supply i. IDDHigh values are calculated as the mean value plus two sigmas (2σ) of measured current under the following conditions: T_J=105° C, outputs loaded with 30 pF (if not otherwise specified). These values are suitable for evaluating board and device thermal characteristics

17 D.C. Characteristics

T_a = -40°C to T_j = 125°C, V_{DDI} = $VDDI_{typical}$ ± 5%, V_{DDO} = $VDDO_{typical}$ ± 5%, AVDL = AVDL typical ± 5%, AVDH = $AVDH_{typical}$ ± 5%, QAVD = $QAVD_{typical}$ ± 5%

Typical Conditions: T_a = 25°C, VDDI = 1.8V, VDDO = 3.3V, AVDH = 3.3V, AVDL = 1.8V, QAVD = 3.3V

Table 48 D.C. Characteristics

Symbol	Parameter	Min	Typical	Max	Units	Conditions
POWER SUPPLY						
V_{VDDI}	Power Supply	1.71	1.8	1.89	Volts	
V_{VDDO}	Power Supply	3.14	3.3	3.46	Volts	
V_{AVDL}	Power Supply	1.71	1.8	1.89	Volts	
V_{AVDH}	Power Supply	3.14	3.3	3.46	Volts	
V_{QAVD}	Power Supply	3.14	3.3	3.46	Volts	
CMOS/TTL						
V_{IL}	Input Low Voltage	—	—	0.8	Volts	Guaranteed Input Low voltage.
V_{IH}	Input High Voltage	2.0	—	—	Volts	Guaranteed Input High voltage.
V_{OL}	Output or Bi-directional Low Voltage	—	0.1	0.4	Volts	Guaranteed output Low voltage at VDD=2.97V and I_{OL}=maximum rated for pad.
V_{OH}	Output or Bi-directional High Voltage	2.4	VDDO – 0.2	—	Volts	Guaranteed output High voltage at VDD=2.97V and I_{OH}=maximum rated current for pad.
V_{ST-}	Schmitt Trigger Input Low Voltage			0.8	Volts	Refer to Note 4
V_{ST}+	Schmidt Trigger Input High Voltage	2.2			Volts	Refer to Note 4
V_{TH}	Schmidt Trigger Input Hysteresis Voltage		0.5		Volts	Refer to Note 4
I_{ILPU}	Input Low Leakage Current	-200	-50	-10	µA	VIL = GND (Refer to notes 1 and 3)
I_{IHPU}	Input High Leakage Current	-10	0	+10	µA	VIH = VDDO (Refer to notes 1 and 3)
I_{IL}	Input Low Leakage Current	-10	0	+10	µA	VIL = GND (Refer to notes 2 and 3)
I_{IH}	Input High Leakage Current	-10	0	+10	µA	VIH = VDDO (Refer to notes 2 and 3)
C_{IN}	Input Capacitance	—	5	—	pF	t_A=25°C, f = 1 MHz
C_{OUT}	Output Capacitance	—	5	—	pF	t_A=25°C, f = 1 MHz

Symbol	Parameter	Min	Typical	Max	Units	Conditions
C_{IO}	Bi-directional Capacitance	—	5	—	pF	t_A=25°C, f = 1 MHz
V_{ICM}	LVDS Input Common-Mode Range	0	—	1.8	V	
$\|V_{IDM}\|$	LVDS Input Differential Sensitivity	60	—	—	mV	
R_{IN}	LVDS Differential Input Impedance	—	100	—	Ω	
V_{LOH}	LVDS Output voltage high	—	1375	1475	mV	RLOAD=100Ω ±1%
V_{LOL}	LVDS Output voltage low	925	1025	—	mV	RLOAD=100Ω ±1%
V_{ODM}	LVDS Output Differential Voltage	300	350	400	mV	R_{LOAD}=100Ω ±1%
V_{OCM}	LVDS Output Common-Mode Voltage	1125	1200	1275	mV	R_{LOAD}=100Ω ±1%
R_O	LVDS Output Impedance, Differential	—	110	—	Ω	
$\|\Delta V_{ODM}\|$	Change in $\|V_{ODM}\|$ between “0” and “1”	—	—	25	mV	R_{LOAD}=100Ω ±1%
ΔV_{OCM}	Change in V_{OCM} between “0” and “1”	—	—	25	mV	R_{LOAD}=100Ω ±1%
I_{SP}, I_{SN}	LVDS Short-Circuit Output Current	—	—	10	mA	Drivers shorted to ground
ISPN	LVDS Short-Circuit Output Current	—	—	10	mA	Drivers shorted together
AC PECL						
$V_{OA, PECL}$	PECL Output Amplitude TX2488_MODE[1:0] = “00” (default) TX2488_MODE[1:0] = “01” TX_MODE[1:0] = “10” Note: TX2488_MODE: register 1020H TX_MODE: registers 1433H 1833H 1C33H	0.90 0.465 0.90	1.00 0.533 1.24	1.10 0.600 1.68	Vppd Vppd Vppd	TXD_P/N[1] TXD_P/N[1] TXD_P/N[4:2] Differential Peak-to-Peak Voltage (Tx) Min: at -40ºC, V_{AVDH}(min), V_{AVDL}(min) Max: at 125ºC, V_{AVDH}(max),V_{AVDL}(max)
$V_{IA, PECL}$	PECL Input Amplitude	0.40 0.18	— —	2.0 2.5	Vppd Vppd	RXD_P/N[1], REFCLK155_P/N RXD_P/N[4:2] Differential Peak-to-Peak Voltage (Rx)

Symbol	Parameter	Min	Typical	Max	Units	Conditions
$R_{PECL\ GNRL}$	Differential PECL Termination Input and Output	—	100	—	Ω	all PECL ports except TXD_P[1]/TXD_N[1]
$R_{PECL\ TXD1}$	Differential PECL Termination Output	—	50	—	Ω	TXD_P[1]/TXD_N[1] (Refer to note 5)
DC PECL						
$V_{i,\ PECL}$	PECL Input Amplitude (with respect to 2.5 V, 3.3V or 5V DC coupled PECL levels)	-1.16 -1.81	-0.95 -1.70	-0.88 -1.48	VIH VIL	REFCLK77_P/N

Notes on D.C. Characteristics:

1. Input pin or bi-directional pin with internal pull-up resistor.
2. Input pin or bi-directional pin without internal pull-up resistor
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).
4. Schmitt Trigger Input pins: RSTB, TRSTB, CSB and TCK
5. TXD_P[1]/TXD_N[1] still needs to drive 100 Ohms differential

18 A.C. Timing Characteristics

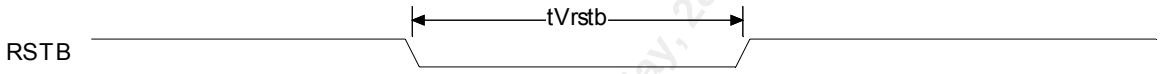
T_a = -40°C to T_j = 125°C, V_{DDI} = $VDDI_{typical}$ ± 5%, V_{DDO} = $VDDO_{typical}$ ± 5%, AVDL = $AVDL_{typical}$ ± 5%, AVDH = $AVDH_{typical}$ ± 5%, QAVD = $QAVD_{typical}$ ± 5%

18.1 Reset Pulse Width Timing Characteristics

Table 49 Reset Pulse Width Timing (Figure 67)

Symbol	Description	Min	Max	Units
tVrstb	RSTB pulse width	2	—	ms

Figure 67 Reset Pulse Width



18.2 SONET/SDH Overhead Interface Timing Characteristics

Table 50 SONET/SDH Overhead Interface Timing (Figure 68 and Figure 69)

Symbol	Description	Min	Max	Units
tP_{rtohfp}	RTOHCLK Low to RTOHFP valid	-7	7	ns
tP_{rtoh}	RTOHCLK Low to RTOH valid	-7	7	ns
tP_{b3e}	RTOHCLK Low to B3E valid	-7	7	ns
tP_{ralm}	RTOHCLK Low to RALM valid	-7	7	ns
tP_{ttohfp}	TOHCLK Low to TOHFP valid	-7	7	ns
tS_{ttoh}	TTOH Set-up time to TTOHCLK	14	—	ns
tH_{ttoh}	TTOH Hold time to TTOHCLK	0	—	ns
tS_{ttohen}	TTOHEN Set-up time to TTOHCLK	14	—	ns
tH_{ttohen}	TTOHEN Hold time to TTOHCLK	0	—	ns

Figure 68 SONET/SDH Receive Overhead Interface Timing

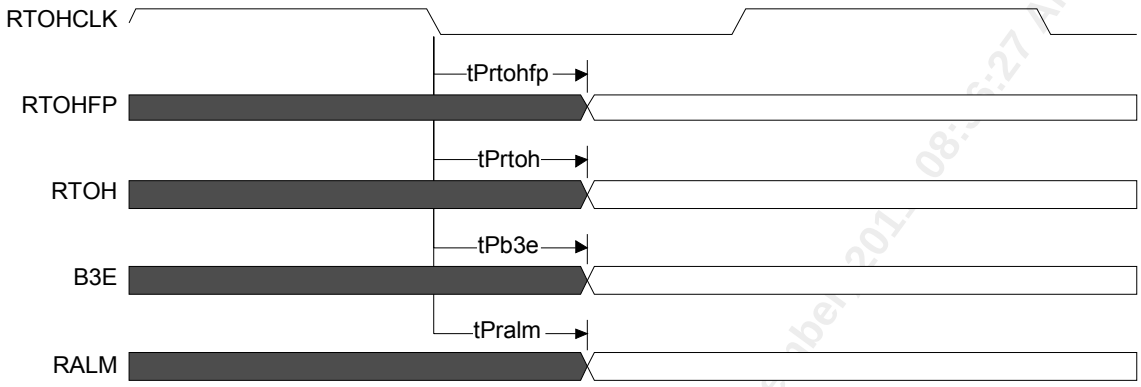
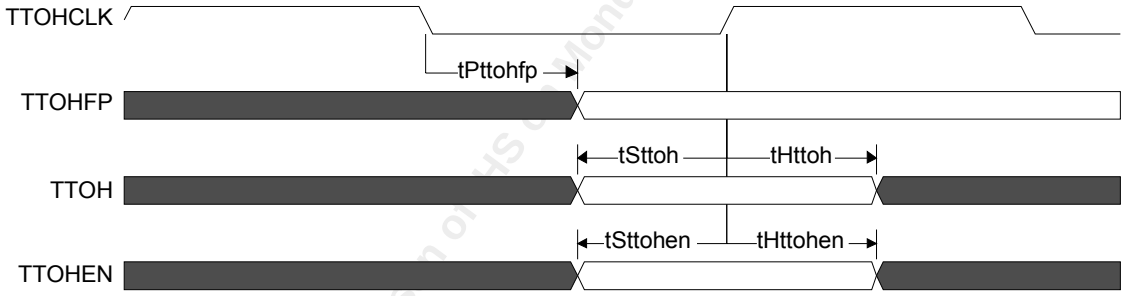


Figure 69 SONET/SDH Transmit Overhead Interface Timing



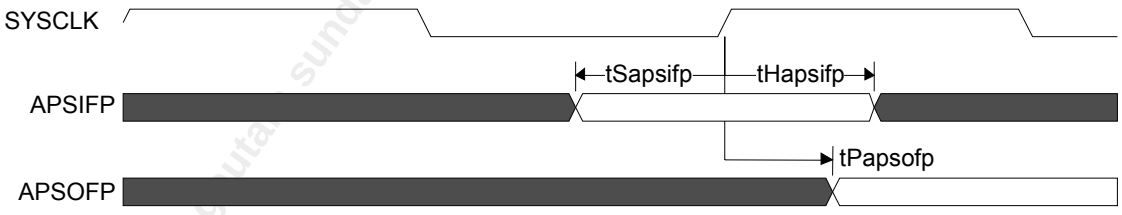
18.3 APS Port Interface Timing Characteristics

Table 51 APS Port Interface Timing (Figure 70)

Symbol	Description	Min	Typical	Max	Units
fSYSCLK	SYSCLK Frequency (nominally 77.76 MHz) (Telcordia spec for +/-20ppm clock sources); all conditions	77.758	77.76	77.762	MHz
tHISYSCLK	SYSCLK High Pulse Width (45/55 duty cycle)	5.79	—	—	ns
tLOSYSCLK	SYSCLK Low Pulse Width (45/55 duty cycle)	5.79	—	—	ns
tSapsifp	APSIFP Set-up time to SYSCLK (when APSIFP is synchronous to SYSCLK)	3	—	—	ns
tHapsifp	APSIFP Hold time to SYSCLK (when APSIFP is synchronous to SYSCLK)	0.3	—	—	ns
tPapsofp	SYSCLK High to APSOFP valid (when SYSCLK pin is used)	—	10	—	ns

Symbol	Description	Min	Typical	Max	Units
tHIAPSIFP	APSIFP High Pulse Width (when APSIFP is used, but SYSCLK is not)	12.8597 (minimum REFCLK 77.76 period)	—	—	ns
tLOAPSIFP	APSIFP Low Pulse Width (when APSIFP is used, but SYSCLK is not)	25.7194 (2 x minimum REFCLK 77.76 period)	—	—	ns
FRlvds	APSI_P/ APSI_N[4:1], APSO_P/ APSO_N[4:1] Bit Rate vs internal SYSCLK (SYSCLK_I) *Note: SYSCLK_I relates to: SYSCLK when SYSCLK pin is used; else REFCLK77_P/N in 622/155 mode or half of REFCLK155_P/N frequency in 2488 mode.*	$10f_{SYSCLK\_I}$ – 100ppm	$10f_{SYSCLK\_I}$	$10f_{SYSCLK\_I}$ + 100ppm	Mbit/s
Taps,jitter	Jitter acceptable on SYSCLK input (RMS, 12kHz to 20MHz)			5.4	ps
Tfall	V_{ODM} fall time, 80%-20%, (R_{LOAD}=100Ω ±1%)	150	300	450	ps
Trise	V_{ODM} rise time, 20%-80%, (R_{LOAD}=100Ω ±1%)	150	300	450	ps
Tskew	Differential Skew			50	ps

Figure 70 APS Port Interface Timing



18.4 OC-48 Interface Timing Characteristics

Table 52 OC-48 Interface Timing

Symbol	Description	Min	Max	Units
fREFCLK155_P/N	REFCLK155_P/N Input Frequency (nominally 155.52MHz) (Telcordia spec for +/-20ppm clock sources); all conditions	155.517	155.523	MHz
tHIREFCLK155_P/N	REFCLK155_P/N Hi Pulse Width (45/55 duty cycle)	2.89	—	ns
tLOREFCLK155_P/N	REFCLK155_P/N Low Pulse Width (45/55 duty cycle)	2.89	—	ns
jRMS48	OC-48 Transmit Line Output RMS jitter (12 kHz to 20 MHz)		0.01	UI
fRCLKO48	RCLKO Output Frequency (nominally 77.76 MHz) (Frequency locked on the receive data rate,Telcordia spec for +/-20ppm data rates); OC-48 mode	77.758	77.762	MHz
tHIRCLKO48	RCLKO Hi Pulse Width; OC-48 mode (45/55 duty cycle)	5.79	—	ns
tLORCLKO48	RCLKO Low Pulse Width; OC-48 mode (45/55 duty cycle)	5.79	—	ns

18.5 OC-12 and OC-3 Interface Timing Characteristics

Table 53 OC-12 and OC-3 Line Interface Timing

Symbol	Description	Min	Max	Units
fREFCLK77±	REFCLK77± Input Frequency (nominally 77.76MHz) (Telcordia spec for +/-20ppm clock sources); all conditions	77.758	77.762	MHz
tHIREFCLK77±	REFCLK77± Hi Pulse Width (45/55 duty cycle)	5.79	—	ns
tLOREFCLK77±	REFCLK77± Low Pulse Width (45/55 duty cycle)	5.79	—	ns
jRMS12	OC-12 Transmit Line Output RMS jitter (12 kHz to 5 MHz)		0.01	UI
jRMS3	OC-3 Transmit Line Output RMS jitter (12 kHz to 1.3 MHz)		0.01	UI
fRCLKO12	RCLKO Output Frequency (nominally 77.76 MHz) (Frequency locked on the receive data rate,Telcordia spec for +/-20ppm data rates); OC-12 mode	77.758	77.762	MHz
tHIRCLKO12	RCLKO Hi Pulse Width; OC-12 mode (45/55 duty cycle)	5.79	—	ns
tLORCLKO12	RCLKO Low Pulse Width; OC-12 mode (45/55 duty cycle)	5.79	—	ns
fRCLKO3	RCLKO Output Frequency (nominally 19.44 MHz) (Frequency locked on the receive data rate,Telcordia spec for +/-20ppm data rates); OC-3 mode	19.4396	19.4404	MHz
tHIRCLKO3	RCLKO Hi Pulse Width; OC-3 mode (45/55 duty cycle)	23.15	—	ns
tLORCLKO3	RCLKO Low Pulse Width; OC-3 mode (45/55 duty cycle)	23.15	—	ns

18.6 System Interface Timing

Table 54 Receive System Interface Timing (Figure 71)

Symbol	Description	Min	Max	Units
Frfclk	RFCLK Frequency	60	104	MHz
tHIrfclk	RFCLK HI Pulse Width	3.85	—	ns
tLOrfclk	RFCLK LO Pulse Width	3.85	—	ns
tS_{radr}	RADR[3:0] Set-up time to RFCLK	2	—	ns
tH_{radr}	RADR[3:0] Hold time to RFCLK	0.5	—	ns
tS_{renb}	RENB Set-up time to RFCLK	2	—	ns
tH_{renb}	RENB Hold time to RFCLK	0.5	—	ns
tPrval	RFCLK High to RCA/RVAL Valid	1.5	6	ns
tPrsop	RFCLK High to RSOC/RSOP Valid	1.5	6	ns
tPreop	RFCLK High to REOP Valid	1.5	6	ns
tPrprty	RFCLK High to RPRTY Valid	1.5	6.6	ns

Symbol	Description	Min	Max	Units
tPrerr	RFCLK High to RERR Valid	1.5	6	ns
tPrsx	RFCLK High to RSX Valid	1.5	6	ns
tPrdat	RFCLK High to RDAT[31:0] Valid	1.5	6.6	ns
tPrmod	RFCLK High to RMOD[1:0] Valid	1.5	6	ns

Figure 71 Receive System Interface Timing Diagram

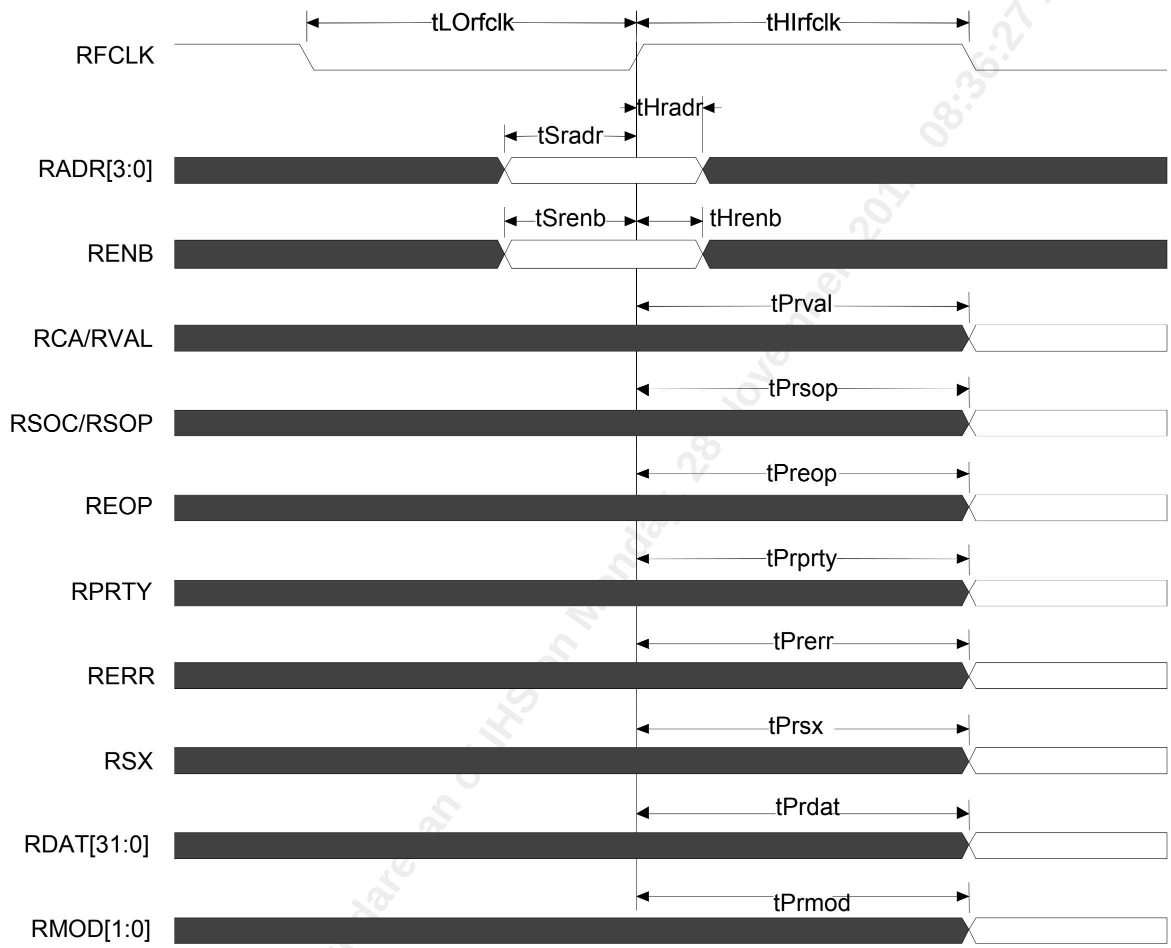
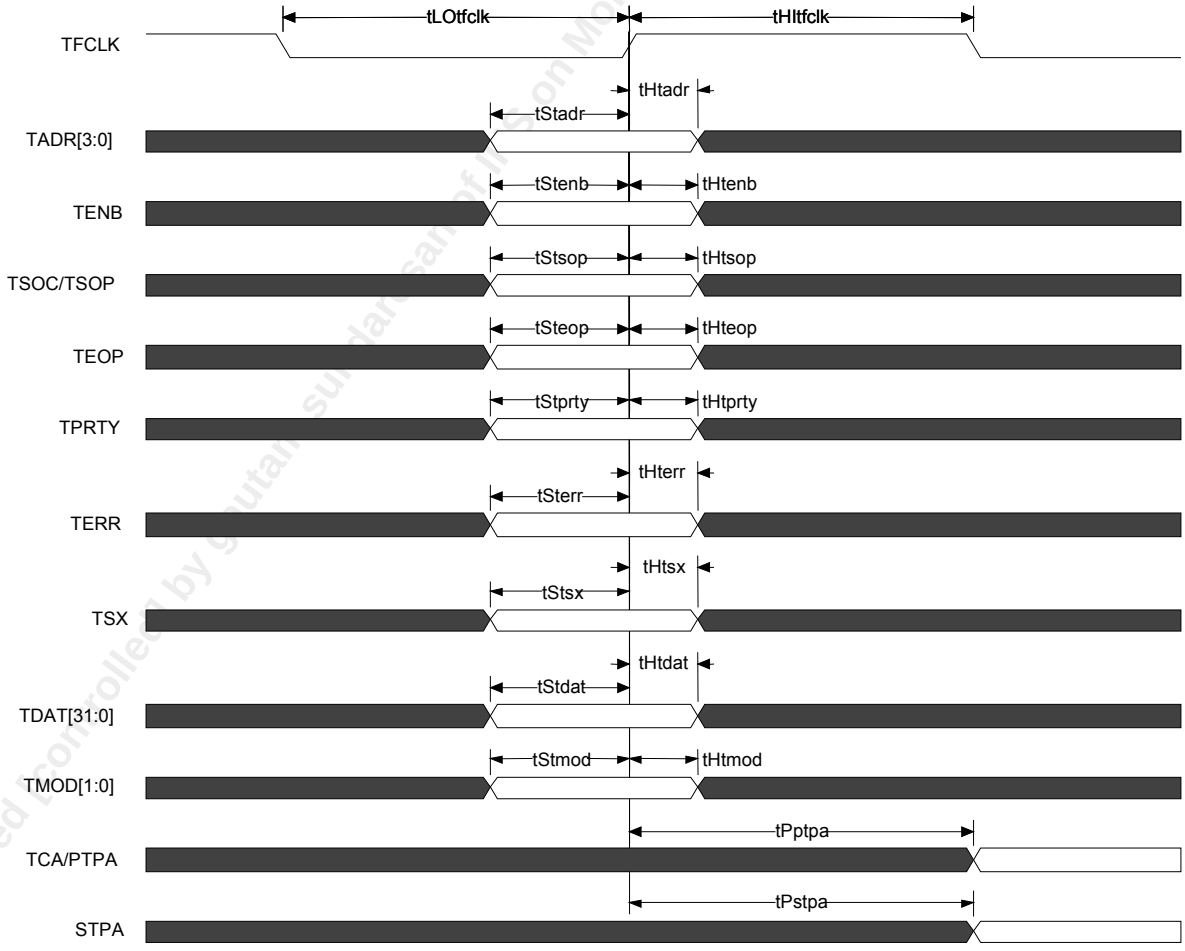


Table 55 Transmit System Interface Timing

Symbol	Description	Min	Max	Units
Ftfclk	TFCLK Frequency	60	104	MHz
tHItfclk	TFCLK HI Pulse Width	3.85	—	ns
tLOtfclk	TFCLK LO pulse Width	3.85	—	ns
tS_{tadr}	TADR[3:0] Set-up time to TFCLK	2	—	ns
tH_{tadr}	TADR[3:0] Hold time to TFCLK	0.5	—	ns
tS_{tenb}	TENB Set-up time to TFCLK	2	—	ns
tH_{tenb}	TENB Hold time to TFCLK	0.5	—	ns
tS_{tsop}	TSOC/TSOP Set-up time to TFCLK	2	—	ns
tHtsop	TSOC/TSOP Hold time to TFCLK	0.5	—	ns
tSteop	TEOP Set-up time to TFCLK	2	—	ns

Symbol	Description	Min	Max	Units
tHteop	TEOP Hold time to TFCLK	0.5	—	ns
tStprty	TPRTY Set-up time to TFCLK	2	—	ns
tHtprty	TPRTY Hold time to TFCLK	0.5	—	ns
tSterr	TERR Set-up time to TFCLK	2	—	ns
tHterr	TERR Hold time to TFCLK	0.5	—	ns
tStsx	TSX Set-up time to TFCLK	2.3	—	ns
tHtsx	TSX Hold time to TFCLK	0.5	—	ns
tStdat	TDAT[31:0] Set-up time to TFCLK	2.3	—	ns
tHtdat	TDAT[31:0] Hold time to TFCLK	0.5	—	ns
tStmod	TMOD[1:0] Set-up time to TFCLK	2	—	ns
tHtmod	TMOD[1:0] Hold time to TFCLK	0.5	—	ns
tP_{ptpa}	TFCLK High to TCA/DTPA Valid	1.5	6	ns
tP_{stpa}	TFCLK High to STPA Valid	1.5	6	ns

Figure 72 Transmit System Interface Timing

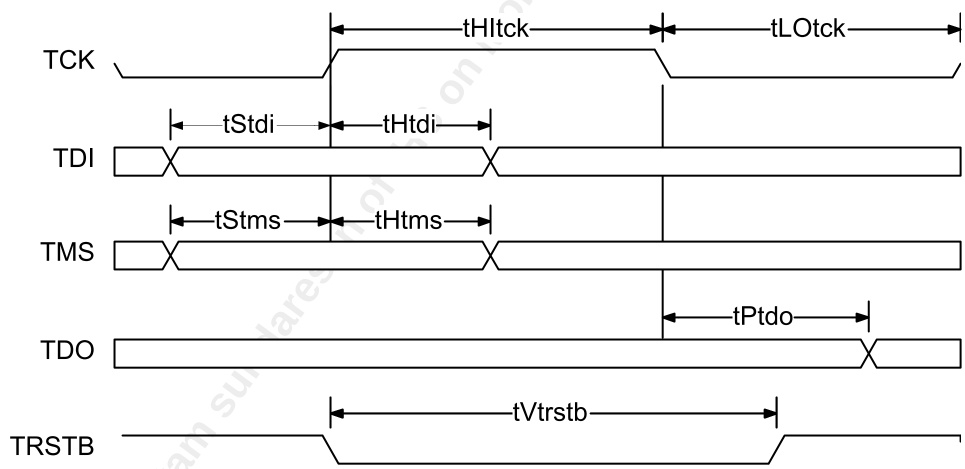


18.7 JTAG Test Port Timing

Table 56 JTAG Port Interface (Figure 73)

Symbol	Description	Min	Max	Units
fTCK	TCK Frequency	—	4	MHz
tHITCK	TCK HI Pulse Width	100	—	ns
tHITCK	TCK LO Pulse Width	100	—	ns
tSTMS	TMS Set-up time to TCK	25	—	ns
tHTMS	TMS Hold time to TCK	25	—	ns
tSTDI	TDI Set-up time to TCK	25	—	ns
tHTDI	TDI Hold time to TCK	25	—	ns
tPTDO	TCK Low to TDO Valid	2	25	ns
tVTRSTB	TRSTB Pulse Width	100	—	ns

Figure 73 JTAG Port Interface Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.
3. All digital clock signals should have 0.5 ns maximum transition time. All digital input signals should have 1.0 ns maximum transition time.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Minimum and maximum output propagation delays are measured with a 30 pF load on the outputs except when otherwise specified.

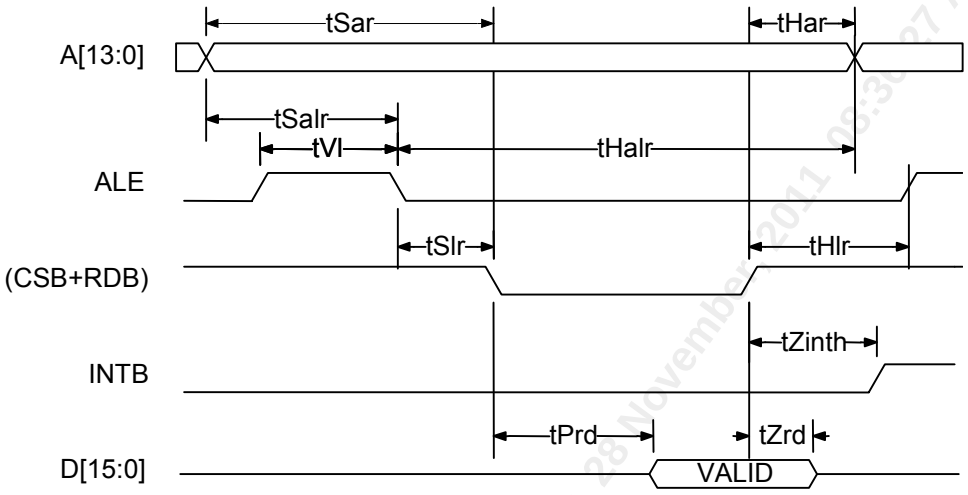
18.8 Microprocessor Interface Timing Characteristics

T_A = -40°C to T_J = +125°C, V_{VDDI} = $V_{VDDItypical}$ ± 5%, V_{VDDO} = $V_{DDOtypical}$ ± 10%
(Typical Conditions: T_C = 25°C, V_{VDDI} = 1.8V, V_{VDDO} = 3.3V)

Table 57 Microprocessor Interface Read Access (Figure 74)

Symbol	Parameter	Min	Typ	Max	Units
TS_{AR}	Address to Valid Read Set-up Time	10	—	—	ns
TH_{AR}	Address to Valid Read Hold Time	5	—	—	ns
TS_{ALR}	Address to Latch Set-up Time	10	—	—	ns
TH_{ALR}	Address to Latch Hold Time	10	—	—	ns
TV_{L}	Valid Latch Pulse Width	—	5	—	ns
TS_{LR}	Latch to Read Set-up	—	0	—	ns
TH_{LR}	Latch to Read Hold	—	5		ns
TP_{RD}	Valid Read to Valid Data Propagation Delay	—	—	70	ns
TZ_{RD}	Valid Read Negated to Output Tri-state	—	—	20	ns
TZ_{INTH}	Valid Read Negated to INTB High (WCIMODE=0)	—	—	50	ns

Figure 74 Intel Microprocessor Interface Read Timing



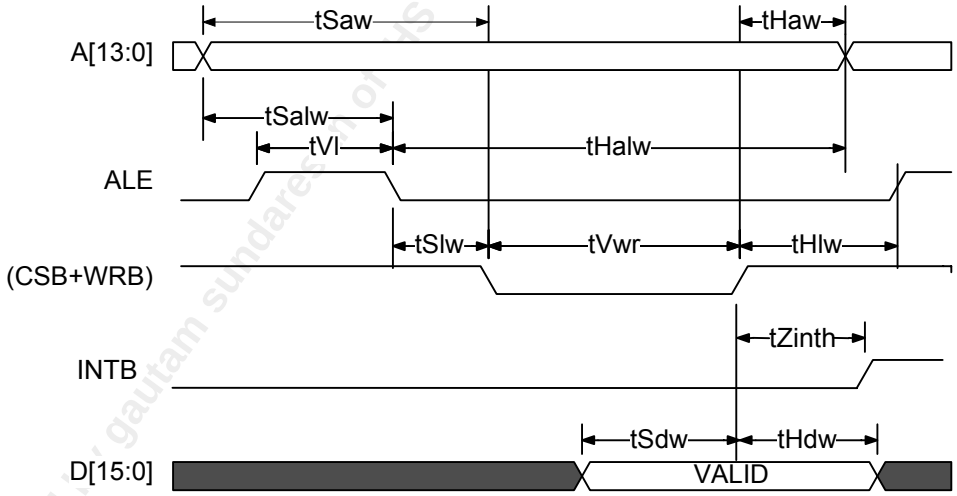
Notes on Microprocessor Interface Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Minimum and maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[15:0]).
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALR}, tH_{ALR}, tV_L, tS_{LR}, and tH_{LR} are not applicable.
5. Parameter tH_{AR} is not applicable if address latching is used.
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Table 58 Microprocessor Interface Write Access (Figure 75)

Symbol	Parameter	Min	Typ	Max	Units
TS_{AW}	Address to Valid Write Set-up Time	10	—	—	ns
TS_{DW}	Data to Valid Write Set-up Time	20	—	—	ns
TS_{ALW}	Address to Latch Set-up Time	10	—	—	ns
TH_{ALW}	Address to Latch Hold Time	10	—	—	ns
TV_{L}	Valid Latch Pulse Width	—	5	—	ns
TS_{LW}	Latch to Write Set-up	—	0	—	ns
TH_{LW}	Latch to Write Hold	—	5	—	ns
TH_{DW}	Data to Valid Write Hold Time	5	—	—	ns
TH_{AW}	Address to Valid Write Hold Time	5	—	—	ns
TV_{WR}	Valid Write Pulse Width	40	—	—	ns
TZ_{INTH}	Valid Write to INTB High (WCIMODE=1)	—	—	50	ns

Figure 75 Intel Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.
2. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALW}, tH_{ALW}, tV_{L}, tS_{LW}, and tH_{LW} are not applicable.
3. Parameter tH_{AW} is not applicable if address latching is used.
4. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
5. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

19 Thermal Information

This product is designed to operate over a wide temperature range and is suited for both central office and outside plant equipment[1].

Table 59 Thermal Information

Maximum long-term operating junction temperature (T_J) to ensure adequate long-term life	105 °C
Maximum junction temperature (T_J) for short-term excursions with guaranteed continued functional performance[2]. This condition will typically be reached when local ambient reaches 85 °C.	125 °C
Minimum ambient temperature (T_A)	-40 °C

Table 60 Device Compact Model[3]

Junction-to-Case Thermal Resistance, θ_{JC}	0.3 °C/W
Junction-to-Board Thermal Resistance, θ_{JB}	5.03 °C/W
Junction-to-Ambiant Thermal Resistance, θ_{JA}	NC = 11.71 °C/W 200 LFM = 10.07 °C/W 400 LFM = 8.95 °C/W

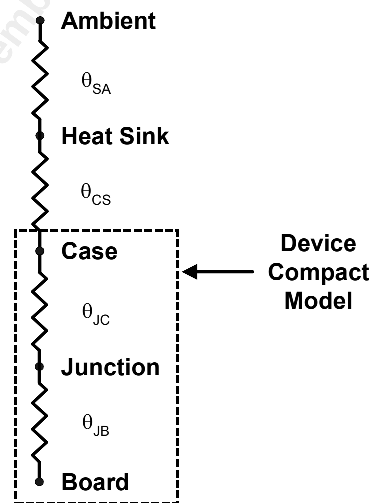


Table 61 Device Compact Model[4]

$\theta_{SA}+\theta_{CS}$[4]	The sum of $\theta_{SA} + \theta_{CS}$ must be less than or equal to: $[(105 - T_A) / P_D] - \theta_{JC}]$ °C/W where: T_A is the ambient temperature at the heat sink location P_D is the operating power dissipated in the package θ_{SA} and θ_{CS} are required for long-term operation

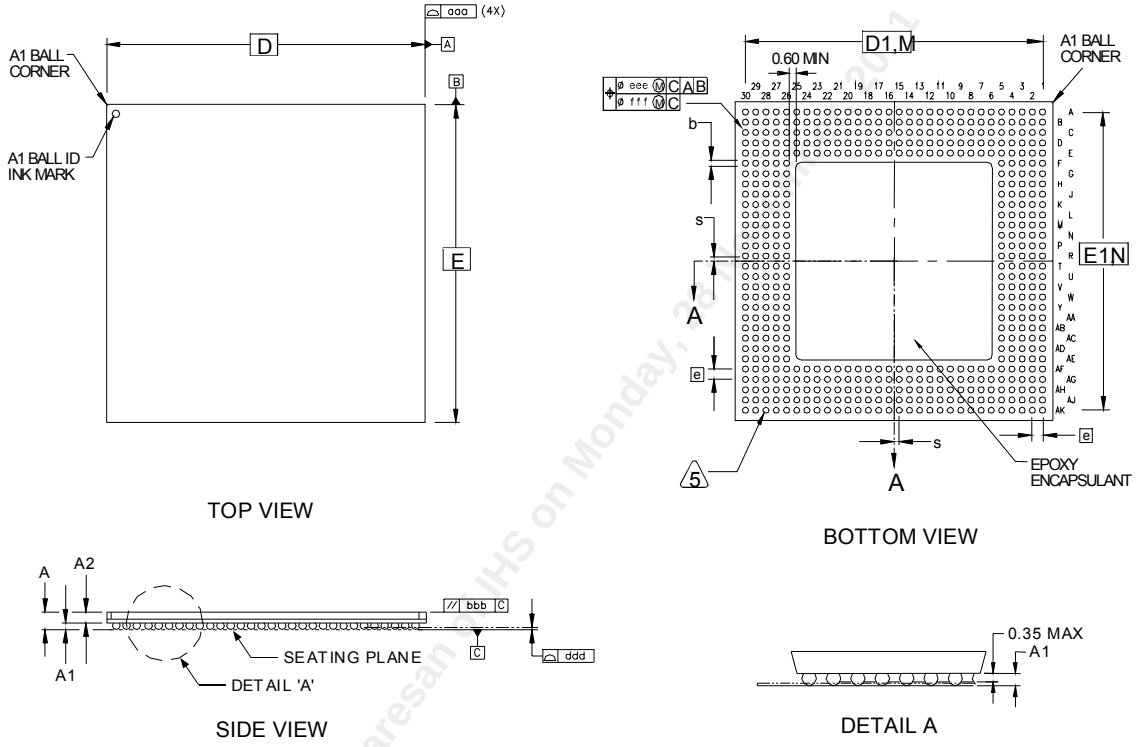
Notes

1. The minimum ambient temperature requirement for meets the minimum ambient temperature requirement for Industrial Equipment
2. Short-term is used as defined in Telcordia Technologies Generic Requirements GR-63-Core; for more information about the GR-63-CORE standard, see [3].
3. θ_{JC}, the junction-to-case thermal resistance, is a measured nominal value plus two sigma. θ_{JB}, the junction-to-board thermal resistance, is obtained by simulating conditions described in JEDEC Standard JESD 51-8; for more information about this standard, see [7].
4. θ_{SA} is the thermal resistance of the heat sink to ambient. θ_{CS} is the thermal resistance of the heat sink attached material. The maximum θ_{SA} required for the airspeed at the location of the device in the system with all components in place.

20 Mechanical Information

The package conforms to JEDEC JESD51 (2S2P).

Figure 76 Mechanical Drawing 500 Pin UBGA 31x31 MM BODY (B SUFFIX)



NOTES: 1) ALL DIMENSIONS IN
2) SION aaa TES PACKAGE Y
3) DIMENSION DENOTES RALLEL
4) NSION ddd DENOTES NARITY
5) OF SOLDER MASK IS 0.53 +/- 0.025 DIAMETER
6) PACKAGE LIANT TO JEDEC ISTERED TLINE 034, TION 1.

PACKAGE TYPE : 500 THERMALLY ENHANCED BALL GRID ARRAY - UBGA																
BODY SIZE : 31 x 31 x 1.47 MM																
Dim.	A	A_1	A_2	D	D_1	E	E_1	M,N	b	e	aaa	bbb	ddd	eee	fff	S
Min.	1.26	0.40	0.86	-	-	-	-	-	0.50	-	-	-	-	-	-	-
Nom.	1.42	0.50	0.92	31.00 BSC	29.00 BSC	31.00 BSC	29.00 BSC	30x30	0.60	1.00 BSC	-	-	-	-	-	-
Max.	1.62	0.60	1.02	-	-	-	-	-	0.70	-	0.20	0.25	0.20	0.25	0.10	0.50

Notes

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