PM5390

S/UNI® 9953

SATURN® USER NETWORK INTERFACE for 9953 MBIT/S

Data Sheet

Proprietary and Confidential

Released

Issue 10 : January, 2007

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Legal Information

Copyright

Copyright 2007 PMC-Sierra, Inc. All rights reserved.

The information in this document is proprietary and confidential to PMC-Sierra, Inc., and for its customers' internal use. In any event, no part of this document may be reproduced or redistributed in any form without the express written consent of PMC-Sierra, Inc.

PMC-2000604 (R10)

Disclaimer

None of the information contained in this document constitutes an express or implied warranty by PMC-Sierra, Inc. as to the sufficiency, fitness or suitability for a particular purpose of any such information or the fitness, or suitability for a particular purpose, merchantability, performance, compatibility with other parts or systems, of any of the products of PMC-Sierra, Inc., or any portion thereof, referred to in this document. PMC-Sierra, Inc. expressly disclaims all representations and warranties of any kind regarding the contents or use of the information, including, but not limited to, express and implied warranties of accuracy, completeness, merchantability, fitness for a particular use, or non-infringement.

In no event will PMC-Sierra, Inc. be liable for any direct, indirect, special, incidental or consequential damages, including, but not limited to, lost profits, lost business or lost data resulting from any use of or reliance upon the information, whether or not PMC-Sierra, Inc. has been advised of the possibility of such damage.

Trademarks

For a complete list of PMC-Sierra's trademarks, see our web site at http://www.pmc-sierra.com/legal/.

Other product and company names mentioned herein may be the trademarks of their respective owners.

Patents

The technology discussed in this document is protected by one or more of the following patent grants:

U.S. Patent No. 5,835,602.

Cdn Patent No. 2,194,919.

Other relevant patent grants may also exist.

Downloaded by Content Team of Partminer Inc. at Wednesday, 07 February, 2007 6:59:32 PM

Contacting PMC-Sierra

PMC-Sierra
100-2700 Production Way
Burnaby, BC Canada V5A 4X1

Tel: +1 (604) 415-6000
Fax: +1 (604) 415-6200

Document Information: document@pmc-sierra.com
Corporate Information: info@pmc-sierra.com
Technical Support: apps@pmc-sierra.com
Web Site: http://www.pmc-sierra.com

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Revision History

Issue No.	Issue Date	Details of Change
10	January 2007	Added Figure 75 1152 PIN FCBGA – 35x35 MM BODY – HDBU Substrate. Updated Table 85 Ordering Information.
9	February 2006	Updated ordering information including RoHS-compliant device details.
8	March, 2003	Minor updates to a few sections for Release to Production.
7	January, 2003	Updates to most sections to include details on new functionality in Revision C of the device. Major updates include GFP descriptions, updated Ethernet descriptions, additional registers for power management, improved DCC port access, path termination over receive APS port, and other smaller improvements.
6	June 2002	Major updates to all sections.
5	October 2001	Updated Pin Description, Top-Level Register Description. Updated Operation, Functional and AC Timing sections. Updated DC Characteristics section for LVDS and PECL I/O requirements. Updated relevant sections to reflect 10 Gigabit Ethernet LAN PHY support. Updated thermal information.
4	April 2001	Updated Pin Description, Top-Level Register and TSB Register Description. Updated Operation, Functional and AC Timing sections.
3	September 2000	Revised Functional Timing and AC Timing sections. Added STM-4 slice architecture in Functional Description and Microprocessor sections. Re-organized register address map and register description for the slice architecture.
2	July 2000	Issue 2 datasheet created
1	April 2000	Preliminary datasheet created

Downloaded by Content Team of Partminer Inc on Wednesday, 10 October 2007 06:59:39 PM

Table of Contents

Downloaded by Content Team on Portmanteau on Wednesday, 07 February, 2007 06:59:32 PM

Downloaded by Content Removed Inc on Wednesday, 07 February, 2007 06:59:32 PM

Downloaded by Conteq Telecom Electronic on Wednesday, 07 February, 2007 06:59:32 PM

Downloaded by Content Premier Inc on Wednesday, 07 February, 2007 06:59:32 PM

Downloaded by Content Server Partner Inc on Wednesday, 07 February, 2007 06:59:32 PM

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

List of Registers

Downloaded by Connect Tech Inc. on Wednesday, 07 February, 2007, 06:59:32 PM

Downloaded by Content Removed Content, LLC on Wednesday, 07 February, 2007 06:59:32 PM

Downloaded by Content Department at Wednesday, 07 February, 2007 06:59:32 PM

Downloaded by Comset - Bath of Harmony Incl Wednesday, 07 February 2007, 06:59:32 PM

Downloaded by Content Removed Pericom Inc on Wednesday, 07 February, 2007 06:59:32 PM

Downloaded by Content Removal Service Inc on Wednesday, 07 February, 2007 06:59:32 PM

Downloaded by Content Nation Patronital IIC currwheedy; 07 February, 2007, 06:59:32 PM

Downloaded by Content Removed Pmc-Sierra, Inc. on Wednesday, 01 February, 2007 06:59:32 PM

Downloaded by Content Removed Private IP on Wednesday, 07 February, 2007 06:59:32 PM

Downloaded by Content Removed Pmc-Sierra, Inc. on Wednesday, 01 February 2007 06:59:32 PM

Downloaded by Content Removal Inc on Wednesday, 01 February 2007 06:59:32 PM

Downloaded by Content Removed from Portal at IHS on Wednesday, 07 February, 2007 06:59:32 PM

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

List of Figures

Downloaded by Content Team Portal Inc on Wednesday, 07 February, 2007 06:59:32 PM

Downloaded by Content Technologies, Inc. on Wednesday, February 21, 2007 06:59:32 PM

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

List of Tables

Downloaded by Central Team (Mantrinet) on Wednesday, 07 February, 2007 06:59:32 PM

Downloaded by Content Technologies Inc on Wednesday, 07 February, 2001 06:59:32 PM

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 06:59:32 PM

1 Definitions

The following table defines the abbreviations for the S/UNI® 9953.

Table 1 Definitions

APISO	Analog Parallel In Serial Out
ATM	Asynchronous Transfer Mode
CSU	Clock Synthesis Unit
DRU	Data Recovery Unit
EFLX	Egress FIFO
FIFO	First In First Out
HDLC	High-Level Data Link Control
IFLX	Ingress FIFO
LVDS	Low Voltage Differential Signaling
PL4IDU	PL4 Input Data Unpacker
PL4ODP	PL4 Output Data Packer
PL4IO	PL4 Input and Output Interface
PL4MOS	PL4 Multi-stream Output Scheduler
POS	Packet Over SONET
R8TD	Receive 8B/10B TelecomBus Decoder
RCFP	Receive Cell Frame Processor (OC-48)
RCFP-9953	Receive Cell Frame Processor (OC-192)
RHPP	Receive High order Path Processor
RRMP	Receive Regenerator Multiplexer Processor
RTTP	Received Trail Trace Processor
RXXG	Receive Ethernet Processor 10 Gigabits
RXLV	Receive LVDS
R64B66B	Receive 64B/66B Processor
SARC	SONET/SDH Alarm Reporting Controller
SBER	SONET/SDH Bit Error Rate
SIRP	SONET/SDH In-band Error Report Processor
STSI	SONET/SDH Time Slot Interchange
SVCA	SONET/SDH Virtual Container Aligner
T8TE	Transmit 8B/10B TelecomBus Encoder
TCFP	Transmit Cell Frame Processor (OC-48)
TCFP-9953	Transmit Cell Frame Processor (OC-192)
THPP	Transmit High order Path Processor
TRMP	Transmit Regenerator Multiplexer Processor
TTTP	Transmit Trail Trace Processor
TXXG	Transmit Ethernet Processor 10 Gigabits
TXLV	Transmit LVDS

Downloaded by Document Team (PMC-Sierra) on Wednesday, 07 February, 2007 06:59:32 PM

TXLVREF	Transmit LVDS Reference
T64B66B	Transmit 64B/66B Processor

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

2 Features

The PM5390 S/UNI 9953 is a SATURN® user network interface (9953 Mbit/s) with the following features.

2.1 General

- Single chip ATM, POS, GFP and 10 Gigabit Ethernet LAN/WAN PHY User-Network Interface. Operates at 9953.28 Mbit/s for WAN PHY mode, and at 10320 Mbit/s for LAN PHY mode.
- Provides ATM, POS, GFP and 10 Gigabit Ethernet WAN PHY payload processing for STS-192c (STM-64-64c).
- Provides ATM and POS payload processing for 4 x STS-48c (4 x STM-16-16c) and STS-192 (STM-64) channelized down to STS-48 (STM-16).
- Implements the ATM Forum User Network Interface Specification and the ATM physical layer for Broadband ISDN according to CCITT Recommendation I.432.
- Implements the Point-to-Point Protocol (PPP) over SONET (SDH) specification according to RFC 2615(1619)/1662 of the PPP Working Group of the Internet Engineering Task Force.
- Implements 10 Gigabit Ethernet LAN/WAN PHY specification according to the IEEE 802.3ae.
- Processes 16 bit, 622 Mbit/s SONET (SDH) STS-192c (STM-64-64c) data streams or four 4 bit, 622 Mbit/s SONET (SDH) STS-48c (STM-16-16c) data streams on the line side.
- Provides termination for SONET Section, Line and Path overhead or SDH Regenerator Section, Multiplexer Section and High Order Path overhead for STS-192c (STM-64-64c), 4 x STS-48c (4 x STM-16-16c) and STS-192 (STM-64) channelized down to STS-48 (STM-16).
- Provides direct connection to optics via a 16-bit 644.53125 MHz IEEE 802.3ae XSBI line-side interface for 10 Gigabit Ethernet LAN PHY operation.
- Provides direct connection to optics via a 16-bit 622.08 MHz SFI-4 Phase-1 line-side interface for STS-192c and 10 Gigabit Ethernet WAN PHY operation.
- Provides SATURN POS-PHY Level 4™ 16-bit LVDS System Interface (622 to 700 Mbit/s) for ATM, POS and 10 Gigabit Ethernet applications.
- Supports diagnostic loop back from the transmit stream to the receive stream system interface.
- Supports line loop back from the receive stream to the transmit stream line interface.
- Provides support for automatic protection switching (APS) via two 16-bit LVDS 777.6 MHz ports.
- MDIO/MDC port for control and monitoring of optic modules.

Downloaded by Conta from Pminc on Wednesday, 06 February 2008 06:59:32 PM

- Provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.
- Provides a generic 16-bit microprocessor bus interface for configuration, control, and status monitoring.
- Low power 1.8V CMOS core logic with 3.3V CMOS/TTL compatible digital inputs and digital outputs.
- Typical power dissipation in the range 6W – 9W, depending on the operating mode, with APS port disabled.
- Industrial temperature range (-40C to +105C).

2.2 SONET Section and Line / SDH Regenerator and Multiplexer Section

- Frames to the SONET (SDH) receive stream and inserts the framing bytes (A1, A2) and the section trace byte (J0) into the transmit stream; descrambles the received stream and scrambles the transmit stream.
- Calculates and compares the bit interleaved parity (BIP) error detection codes (B1, B2) for the receive stream. Calculates and inserts B1 and B2 in the transmit stream. Accumulates near end errors (B1, B2) and far end errors (M1) and inserts line remote error indications (REI) into the M1 byte based on received B2 errors.
- Detects signal degrade (SD) and signal fail (SF) threshold crossing alarms based on received B1 errors.
- Extracts and optionally inserts on dedicated pins the SONET (SDH) transport overhead for an SONET (SDH) frame.
- Extracts and filters the automatic protection switch (APS) channel (K1, K2) bytes into internal registers. Inserts the APS channel into the transmit stream.
- Extracts and filters the synchronization status message (S1) byte into an internal register for the receive stream. Inserts the synchronization status message (S1) byte into the transmit stream.
- Extracts a 64 byte (Telcordia compatible) or 16 byte (ITU compatible) section trace (J0) message using an internal register bank for the receive stream. Detects an unstable message or mismatch message with an expected message. Provides access to the accepted message via the microprocessor port. Inserts a 64 byte or 16 byte section trace (J0) message using an internal register bank for the transmit stream.
- Detects loss-of-signal (LOS), out-of-frame (OOF), loss-of-frame (LOF), line remote defect indication (RDI-L), line alarm indication signal (AIS-L), and protection switching byte failure alarms on the receive stream.
- Provides manual and automatic transmit line RDI insertion following detection of various received alarms (LOS, LOF, LAIS, SD, SF, STIM, STIU).
- Supports Automatic Protection Switching (APS) via a mate protection port.

Downloaded by Components Direct Inc on Wednesday, 07 February, 2007 06:50:32 PM

2.3 SONET Path / SDH High Order Path

- Interprets the received payload pointer (H1, H2) and extracts the SONET (SDH) synchronous payload envelope and path overhead and passes data on to ATM cell/packet or 10 Gigabit Ethernet frame processor.
- Detects loss of pointer (LOP), path alarm indication signal (PAIS) and path (normal and enhanced) remote defect indication (RDI) for the receive stream. Optionally inserts path alarm indication signal (PAIS) and path remote defect indication (RDI) in the transmit stream.
- Extracts and inserts the entire SONET (SDH) path overhead to and from dedicated pins. The path overhead bytes may be sourced from internal registers or from bit serial path overhead input stream. Path overhead insertion may also be disabled.
- Extracts the received path payload label (C2) byte into an internal register and detects for payload label unstable (PLU), payload label mismatch (PLM), payload unequipped (UNEQ) and payload defect indication (PDI). Inserts the path payload label (C2) byte from an internal register for the transmit stream.
- Extracts a 64 byte or 16 byte path trace (J1) message using an internal register bank for the receive stream. Detects an unstable message or mismatch message with an expected message. Provides access to the captured, accepted and expected message via the microprocessor port. Inserts a 64 byte or 16 byte path trace (J1) message using an internal register bank for the transmit stream.
- Detects received path BIP-8 and counts received path BIP-8 errors for performance monitoring purposes. BIP-8 errors are selectable to be treated on a bit basis or block basis. Optionally calculates and inserts path BIP-8 error detection codes for the transmit stream.
- Counts received path remote error indications (REI's) for performance monitoring purposes. Optionally inserts the path REI count into the path status byte (G1) based on bit or block BIP-8 errors detected in the receive path. Reporting of BIP-8 errors is on a bit or block basis independent of the accumulation of BIP-8 errors.
- Provides automatic transmit path RDI and path Enhanced RDI insertion following detection of various received alarms (LAIS, LOP, LOPCON, PAIS, PAISCON, PTIM, PTIU, PLM, PLU, UNEQ, PDI).

2.4 ATM Processors

- Extracts ATM cells from four received STS-48c (STM-16-16c) channel payloads or one STS-192c (STM-64-64c) channel payload using ATM cell delineation.
- In the receive direction, provides ATM cell payload de-scrambling, header check sequence (HCS) error detection, idle/unassigned cell filtering and detects out of cell delineation (OCD) and loss of cell delineation (LCD) alarms.
- In the transmit direction, provides ATM idle/unassigned cell insertion, header check sequence (HCS) generation/insertion, and ATM cell payload scrambling.
- Counts number of transmitted cells, received cells, received idle cells, received erred cells and received dropped cells.

Downloaded by Copyright Document Center, Inc. on Wednesday, 07 February 2007 09:39:36 PM

- Provides a POS-PHY Level 4 16-bit wide LVDS data path interfaces (622 to 700 Mbit/s) to internal cell FIFOs in both the receive and transmit directions.

2.5 POS Processors

- Extracts packets from four received STS-48c (STM-16-16c) channel payloads or one STS-192c (STM-64-64c) channel payload using HDLC frame delineation.
- In the receive direction, performs flag sequence detection, self-synchronous data de-scrambling on payloads using the $x^{43}+1$ polynomial, frame check sequence (FCS) validation for CRC-CCITT (STS-48c/STM-16-16c) and CRC-32 polynomials, control escape de-stuffing or byte de-stuffing, minimum and maximum packet lengths checking and FCS stripping.
- For minimum and maximum received packet lengths, optionally deletes short packets and marks those exceeding the maximum length as erred.
- In the transmit direction, performs flag sequence insertion, POS data scrambling using the $1+x^{43}$ polynomial, byte stuffing for transparency processing, optionally frame check sequence generation using the CRC-CCITT (STS-48c/STM-16-16c) and CRC-32 polynomials, packet aborts under the direction of the host or when the FIFOs underflow.
- Provides a POS-PHY Level 4 16-bit wide LVDS data path interfaces (622 to 700 Mbit/s) to internal FIFOs in both the receive and transmit directions.

2.6 GFP Processors

- Extracts packets from one STS-192c (STM-64-64c) channel payload using Frame Based Generic Framing Procedure (GFP-F) frame delineation.
- In the receive direction, performs GFP frame delineation, cHEC error detection and correction, optional payload plus FCS descrambling, idle frame detection and filtering, frame length checking and optional eHEC/tHEC , OAM sHEC and FCS validation
- In the transmit direction, expects the GFP frame to be pre-formatted in accordance with the GFP frame format, including the PLI field. Then provides rate adaptation via GFP idle frame insertion, optional cHEC, tHEC, eHEC and FCS calculation, and performs GFP Payload area scrambling.
- Provides a POS-PHY Level 4 16-bit wide LVDS data path interfaces (622 to 700 Mbit/s) to internal FIFOs in both the receive and transmit directions.

2.7 10 Gigabit Ethernet Processor (LAN and WAN PHY)

- Provides an IEEE 802.3ae 10 Gigabit MAC for Ethernet frame handling.
- Provides mapping to insert/extract Ethernet frames into/from the IEEE 802.3ae Physical Coding Sub-layer (PCS).
- Provides IEEE 802.3ae standard square wave and pseudo-random test pattern generation and checking.
- PCS layer utilizes an STS-192c (STM-64-64c) channel payload (operating at 9953.28 Mbit/s) for 10 Gigabit Ethernet WAN PHY operation.

Downloaded by Content Team of Pericom Semi. on Wednesday, February, 01 2006 06:50:32 PM

- PCS layer processes all data bytes from the XSBI interface (operating at 10320 Mbit/s) for 10 Gigabit Ethernet LAN PHY operation.
- Supports frame delineation using the 64B/66B method as being proposed by the IEEE 802.3ae.
- Supports Ethernet 2.0, IEEE 802.3 LLC and IEEE 802.3 SNAP/LLC encoding formats including VLAN tagged frames.
- Rate control of MAC provides payload suitable for OC-192c SONET/SDH transport.
- In the receive direction, supports 64B/66B decoding, frame delineation, frame integrity (FCS and length) checks, frame filtering and passing based on erred frames, 64 byte minimum frame size and a 9.6K byte maximum frame size.
- In the transmit direction, supports frame generation (preamble, CRC), minimum frame size padding up to 64 bytes, maximum frame truncation up to 9.6K bytes and 64B/66B encoding.
- Provides statistic counters to support
  - Ethernet MIB IEEE 802.3-1998, Clause 30 and 802.3ae
  - SNMP Interface Group MIB, RFC 1213 MIB II & RFC 2233 SMIv2
  - RMON Statistics Group MIB, RFC 1757
  - Ethernet-like MIB, RFC 2665

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:09:32 PM

3 Applications

- Edge and Core Routers.
- Multi-Service (Multi-Protocol) Switches.
- Internet POP and Transport POP L2 Ethernet Switches.
- SONET/SDH Add/Drop Multiplexers and Optical Cross-Connects.
- WAN and Edge ATM Switches.
- Up-link cards.
- SONET/SDH ATM/POS 10 Gigabit Ethernet test equipment.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

4 References

1. Bell Communications Research - GR-253-CORE “SONET Transport Systems: Common Generic Criteria”, Issue 2 Revision 2, January 1999.

2. Bell Communications Research - GR-436-CORE “Digital Network Synchronization Plan”, Issue 1 Revision 1, June 1996.

3. ANSI T1X1.5/99-204, “T1 105.02 draft text for Mapping IEEE 802.3 Ethernet MAC frames to SONET payload”, July 1999.

4. ANSI - T1.105-1995, “Synchronous Optical Network (SONET) – Basic Description including Multiplex Structure, Rates, and Formats”, 1995.

5. ANSI T1.107 - 1995, "Digital Hierarchy - Formats Specifications".

6. ANSI T1.107a - 1990, "Digital Hierarchy - Supplement to Formats Specifications (DS3 Format Applications)".

7. ANSI T1.627 - 1993, "Broadband ISDN - ATM Layer Functionality and Specification".

8. ETS 300 417-1-1, "Generic Functional Requirements for Synchronous Digital Hierarchy (SDH) Equipment", January, 1996.

9. ITU-T Recommendation G.703 - "Physical/Electrical Characteristics of Hierarchical Digital Interfaces", 1991.

10. ITU-T Recommendation G.704 - "General Aspects of Digital Transmission Systems; Terminal Equipment - Synchronous Frame Structures Used At 1544, 6312, 2048, 8488 and 44 736 Kbit/s Hierarchical Levels", July 1995.

11. ITU, Recommendation G.707 - "Network Node Interface For The Synchronous Digital Hierarchy", 1996.

12. ITU Recommendation G781, “Structure of Recommendations on Equipment for the Synchronous Design Hierarchy (SDH)”, January 1994.

13. ITU, Recommendation G.783 - "Characteristics of Synchronous Digital Hierarchy (SDH) Equipment Functional Blocks", 1996.

14. ITU Recommendation I.432, “ISDN User Network Interfaces”, March 93.

15. ATM Forum, af-uni-0010.02, ATM User-Network Interface Specification, V3.1 September 1994.

16. ATM Forum ATM00-0080 – “Frame Based ATM Interface Level 4”, baseline text.

17. IETF Network Working Group – RFC-1619, “Point to Point Protocol (PPP) over SONET (SDH) Specification”, May 1994.

Downloaded by Content Team Partnership on Wednesday, 01 February, 2007 06:59:32 PM

18. IETF Network Working Group – RFC-1661, “The Point to Point Protocol (PPP)”, July 1994.

19. IETF Network Working Group – RFC-1662, “PPP in HDLC like framing”, July 1994.

20. IETF Network Working Group – RFC-2615, “Point to Point Protocol (PPP) over SONET (SDH)”, June 1999.

21. OIF – OIF99.102, “Proposal for a common electrical interface between SONET framers and SONET serializer/deserializer parts for STS-192/STM-64 interfaces.”, July 1999.

22. OIF – OIF00.026.0, “SPI-4 Phase II,” baseline text.

23. PMC-991635, “POS PHY Level 4, Saturn Interface Specification For Packet and Cell Transfer Between Physical Layer and Link Layer Devices for OC-192 SONET/SDH and 10 Gbit/s Ethernet Applications”, Issue 6, Feb. 2001.

24. IEEE P802.3ae final version 5.0.

25. IEEE 802.3-2000.

26. PMC-2010559, “S/UNI 9953 and S/UNI-1x10GbE Frequently Asked Questions”, Issue 1, May 25, 2001.

27. PMC-2010770, “Power Supply Filtering Recommendations”, Issue 1, June 5, 2001.

28. PMC-2011381, “S/UNI 9953 4XOC-48 Line Card Reference Design”, Issue 1, July 12, 2001.

29. PMC-2010476, “POS-PHY Level 4 Static Alignment Design Considerations Application Note”, Issue 1, Issue 1, March 15, 2001.

30. PMC-2011046, “Interfacing to SFI-4 on PMC-Sierra’s Xenon Chipset”, Issue 1, June 2001.

31. PMC-2021518, “JTAG Test Features Description”

32. ITU-T Recommendation G.7041/Y.1303 Generic Framing Procedure.

33. Electronic Industries Association. *Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device)*: EIA/JESD51. December 1995.

34. Electronic Industries Alliance 1999. *Integrated Circuit Thermal Test Method Environmental Conditions -Junction-to-Board: JESD51-8*. October 1999.

35. Telcordia Technologies. *Network Equipment-Building System (NEBS) Requirements: Physical Protection: Telcordia Technologies Generic Requirements GR-63-CORE*. Issue 1. October 1995.

36. SEMI (Semiconductor Equipment and Materials International). SEMI G30-88 Test Method for Junction-to-Case Thermal Resistance Measurements of Ceramic Packages. 1988.

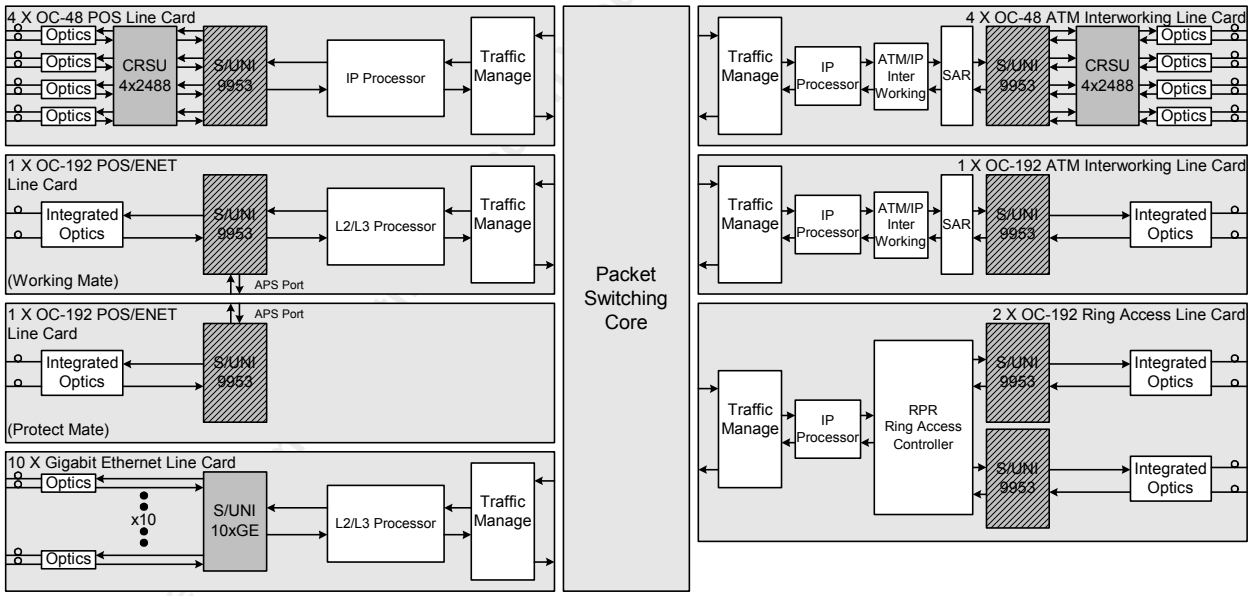
Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:50:32 PM

5 Application Examples

The PM5390 S/UNI 9953 device is applicable to equipment implementing Asynchronous Transfer Mode (ATM), Packet over SONET/SDH (POS) and Data over SONET (SDH) Interfaces. The S/UNI 9953 provides physical layer and data link layer termination for connections between routers, ATM Switches, Multi Service Switches and transport equipment at the OC-192 and OC-48 rates. The S/UNI 9953 is also applicable to equipment implementing 10 Gigabit Ethernet LAN PHY interfaces operating at 10320 Mbit/s.

For routers with 10 Gigabit capable switch ports, the S/UNI 9953 provides solutions for quad OC-48 and OC-192 IP processing cards, 10 Gigabit Ethernet LAN/WAN cards, OC-192 and quad OC-48 ATM inter-working cards and ring based (IPT, DPT) cards. A quad Clock and Data recovery, Clock Synthesis device (CRSU™ 4x2488 device) is required in front of the S/UNI 9953 when it is configured in quad OC-48 mode. Optics supporting the OIF SFI-4 Phase 1 interface are required in the OC-192 or 10GE WAN mode and optics supporting XSBI interface are required in the 10GE LAN modeS/UNI 9953. All S/UNI devices shown below interface to higher layer protocol devices through a standard POS-PHY Level 4™ device. Working and protected versions of the non-ring based cards are also supported. Please refer to Figure 1 below.

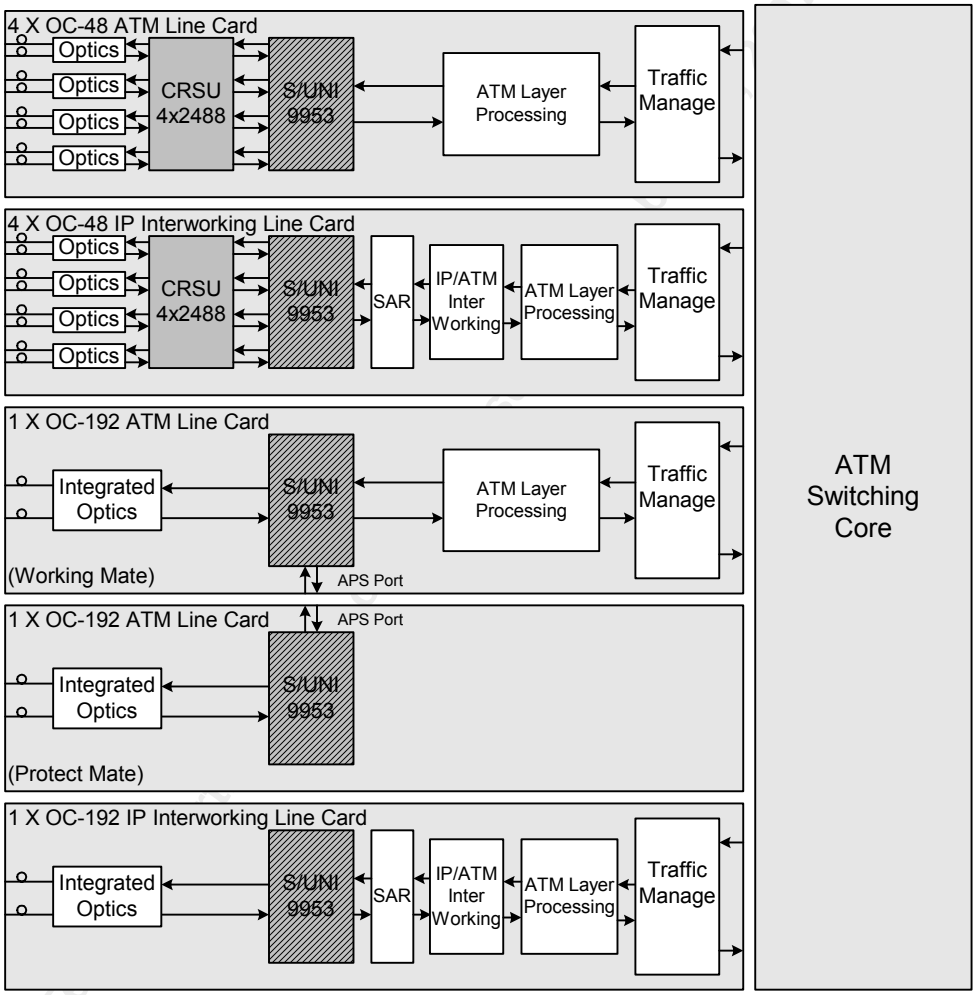
Figure 1 Router - 10G Port Capable



Downloaded by Content Wednesday, [illegible] 2007 6:[illegible] PM

For ATM switches with 10 Gigabit capable switch ports, the S/UNI 9953 provides solutions for OC-192 and quad OC-48 ATM processing cards, and OC-192 and quad OC-48 IP inter-working cards. All S/UNI devices shown below interface to higher layer protocol devices through a standard POS-PHY Level 4 device. Working and protected versions of cards are also supported. Please refer Figure 2 below.

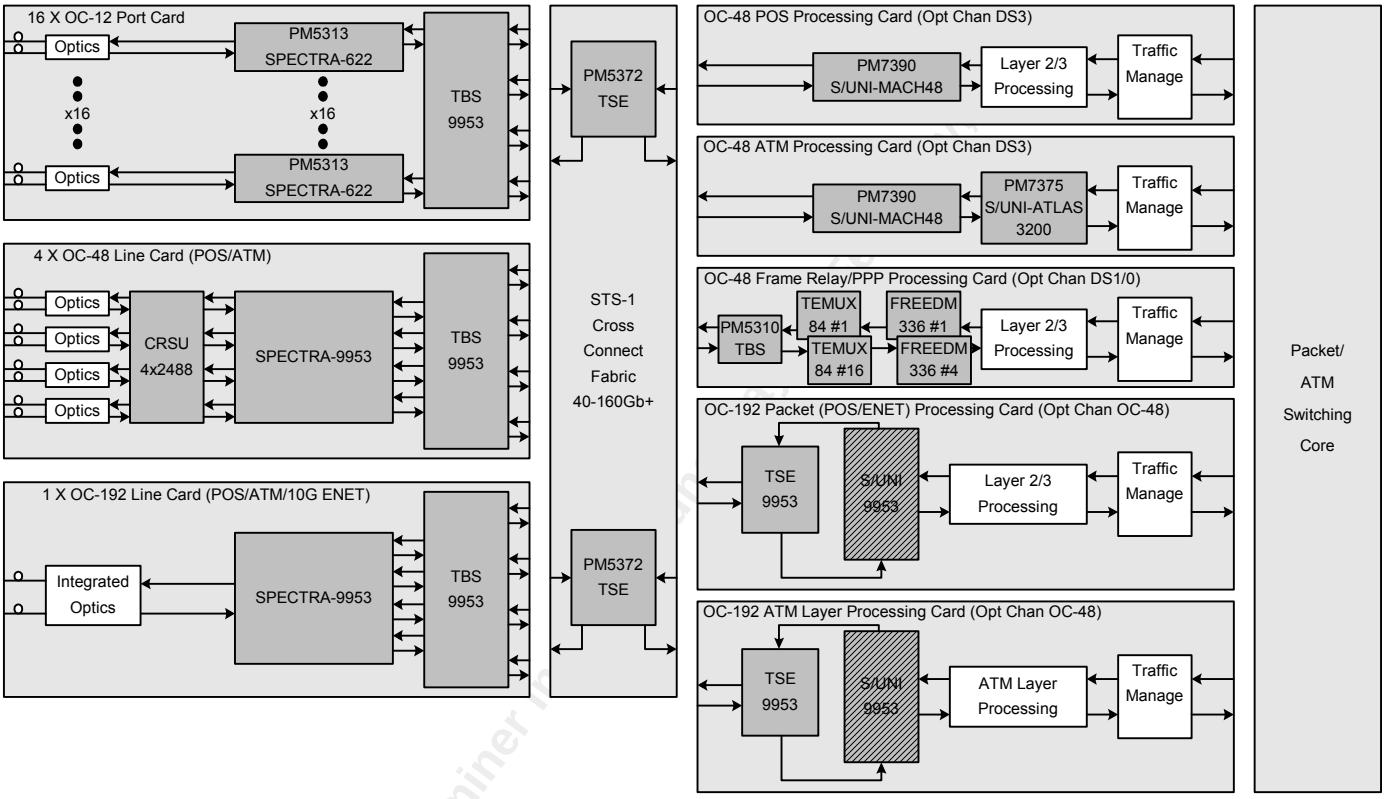
Figure 2 ATM Switch - 10G Port Capable



Downloaded by Content Tu

For Multi-service switches with 10 Gigabit capable switch ports, the S/UNI 9953 provides protocol site termination for ATM, POS, GFP, and 10 Gigabit Ethernet STS-192c (STM-64-64c) payloads and for ATM and POS 4*STS-48c (STM-16-16c) payloads. Please refer Figure 3 below.

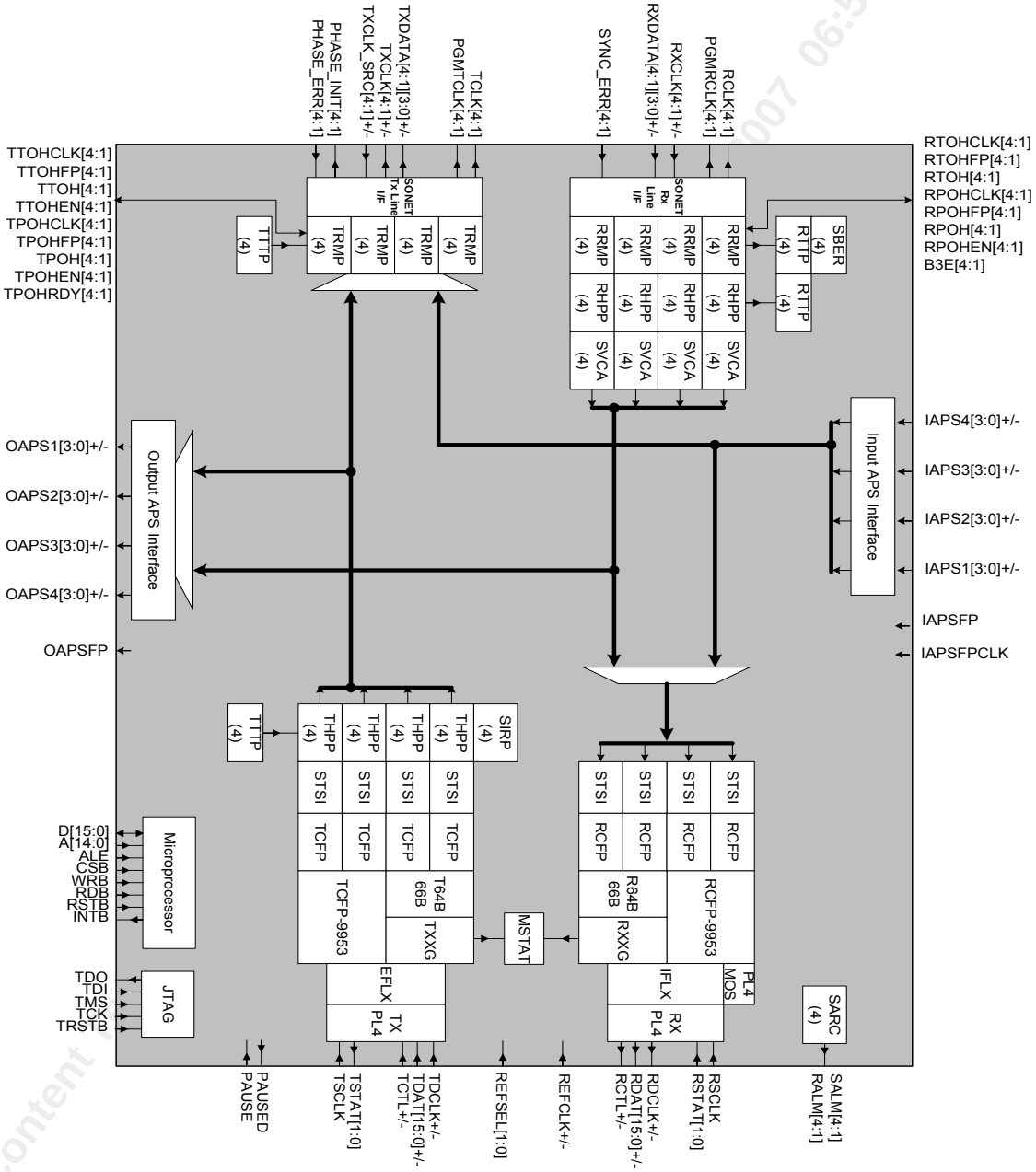
Figure 3 Multi-Service Switch



Downloaded by Content Team of Partminer

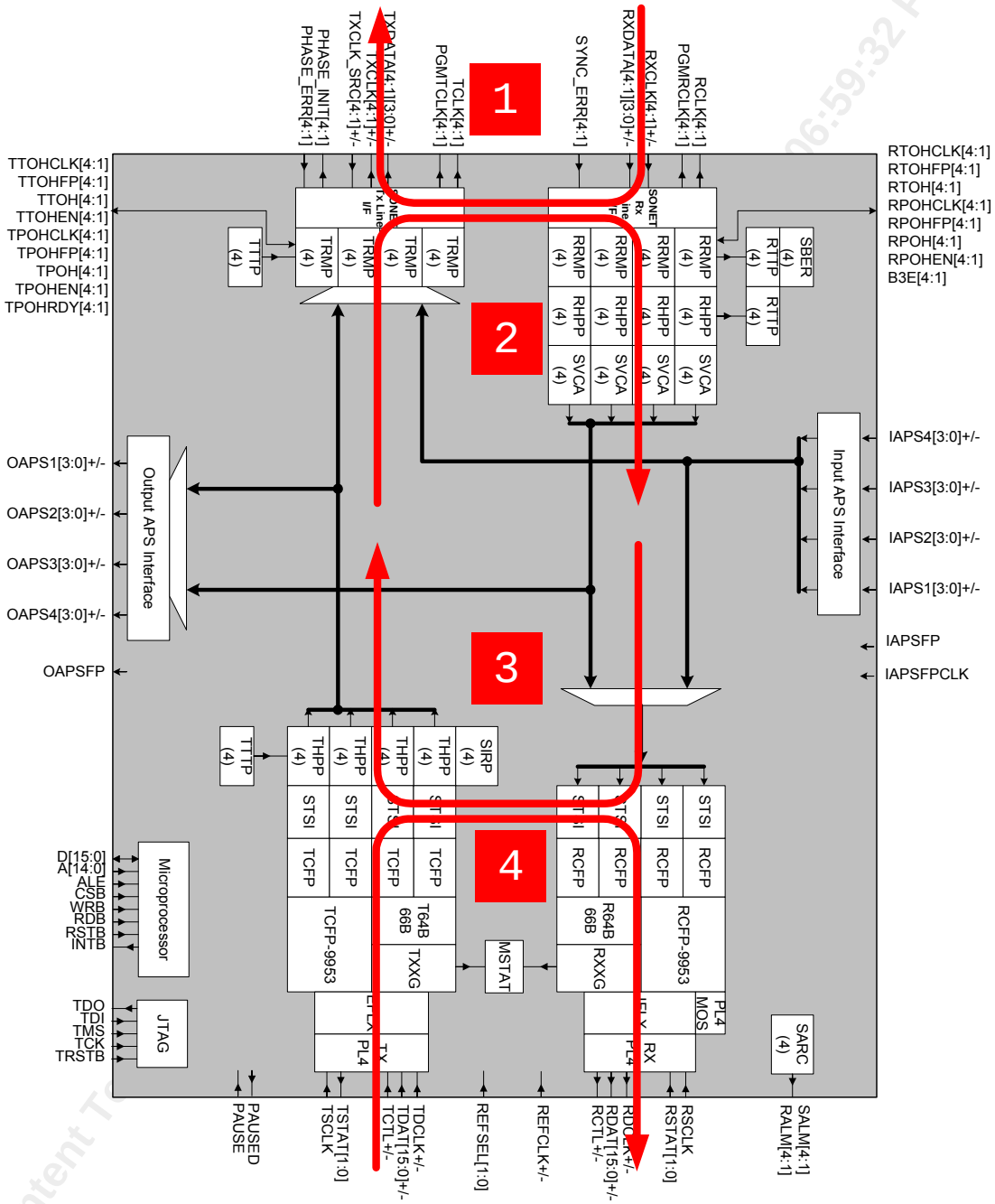
6 Block Diagram

Figure 4 Normal Operation



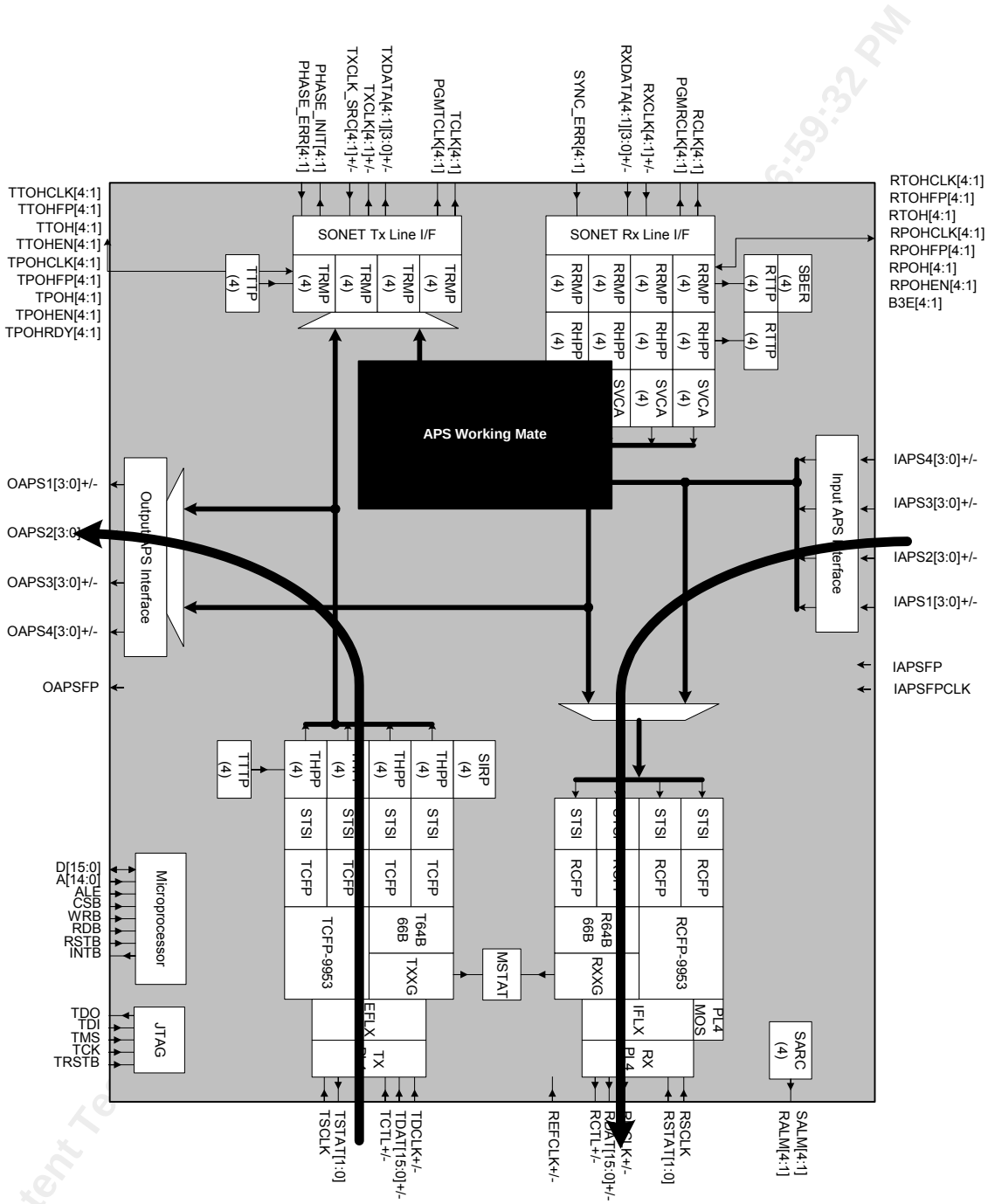
Downloaded by Content ... 007 06:59:32 PM

Figure 5 Loop Back Modes



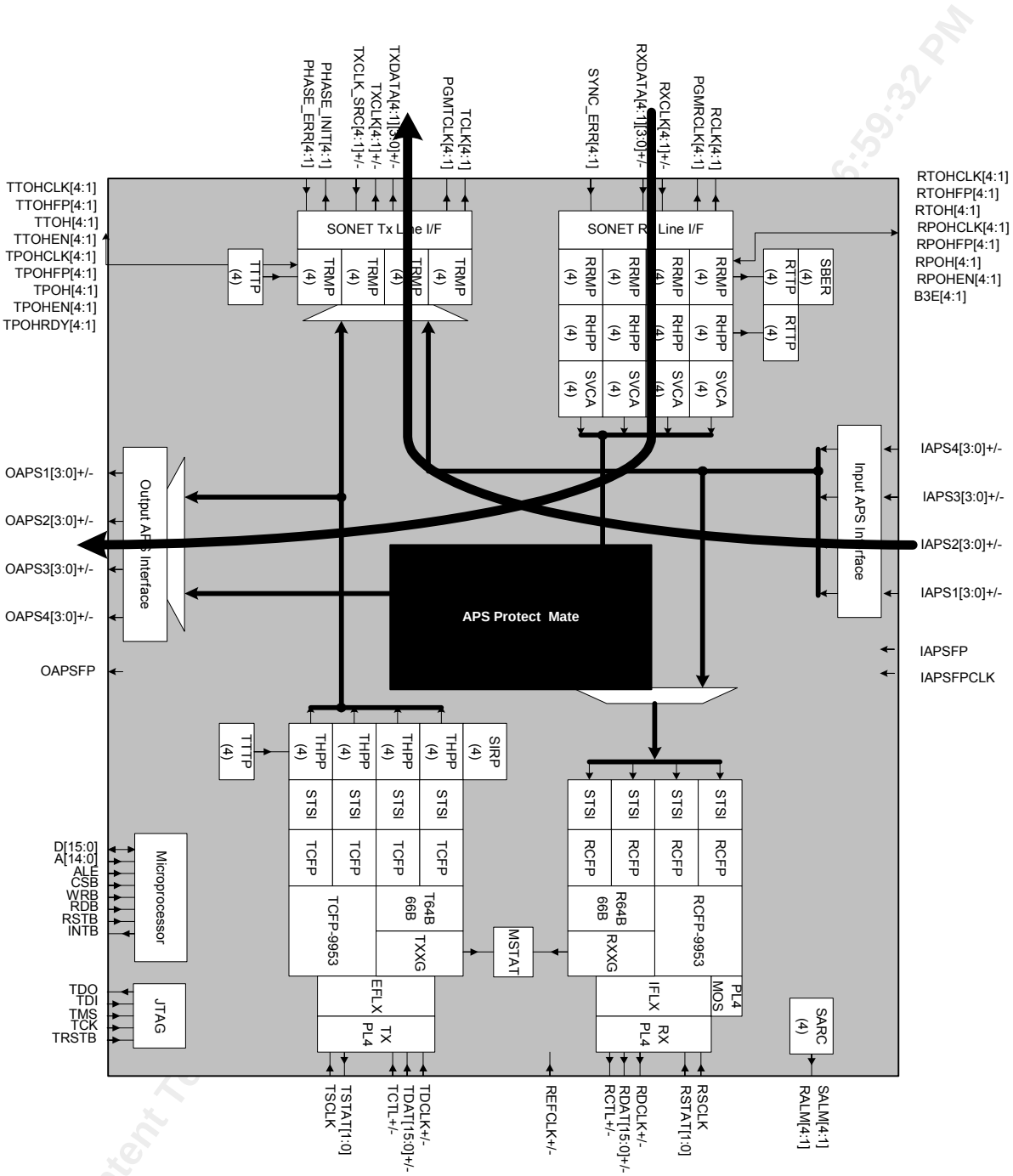
Downloaded by Content To... 06:59:32 PM

Figure 6 APS Working



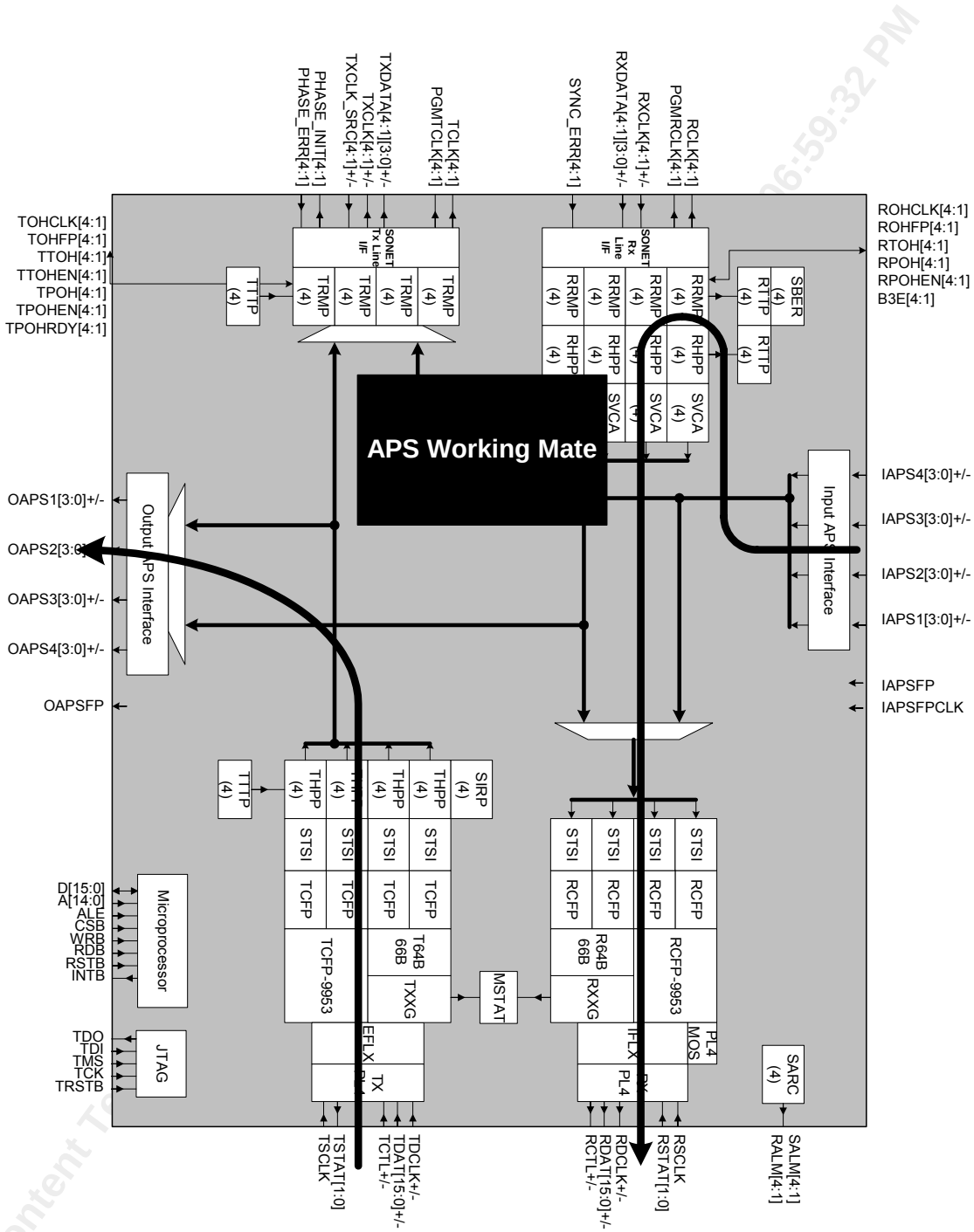
Downloaded by Content Te... 6:59:32 PM

Figure 7 APS Protect



Downloaded by Content Tu... 6:59:32 PM

Figure 8 APS Working (with Path Termination)



Downloaded by Content To

7 Description

The PM5390 S/UNI 9953 SATURN User Network Interface is a monolithic integrated circuit that implements SONET (SDH) processing and payload termination for four OC-48 streams, one OC-192 stream or one 10 Gigabit Ethernet LAN PHY stream. In OC-192 mode of operation, both unchannelized and channelized operation down to STS-48c (STM-16-16c) is supported. In the quad OC-48 and OC-192 modes, the S/UNI 9953 performs ATM and Packet over SONET (POS) mapping. In single unchannelized OC-192 mode, the S/UNI 9953 also performs Generic Framing Procedure (GFP) and IEEE 802.3ae 10 Gigabit Ethernet WAN mapping. In all SONET/SDH modes of operation, the S/UNI 9953 can be configured as an APS working device or as an APS protect device. As either a working or protect device, dedicated APS ports are provided to communicate with an associated mate device under an APS failure condition. In 10 Gigabit Ethernet LAN PHY operation, the S/UNI 9953 performs IEEE 802.3ae 10 Gigabit Ethernet mapping for a 10320 Mbit/s data stream.

The S/UNI 9953 receives SONET (SDH) streams using four 4 bit parallel interfaces for quad OC-48 operation and a sixteen bit parallel interface for OC-192 operation. For both modes of operation, the S/UNI 9953 processes section, line, and path overhead. The S/UNI 9953 performs framing (A1, A2), de-scrambling, detects alarm conditions, and monitors section, line, and path bit interleaved parity (B1, B2, B3), accumulating error counts at each level for performance monitoring purposes. Line and path remote error indications (M1, G1) are also accumulated. The S/UNI 9953 interprets the received payload pointers (H1, H2) and extracts the synchronous payload envelope, which carries the received ATM cells, POS frames, or ten Gigabit Ethernet frames.

The S/UNI 9953 receives a 10 Gigabit Ethernet data stream at 10320 Mbit/s using a sixteen bit parallel XSBI interface derived from the OIF99.102.5 SFI-4 specification.

When used to implement ATM UNI or NNI interfaces, the S/UNI 9953 frames to the ATM payload using cell delineation. Idle/unassigned cells may be optionally dropped. Cells are also dropped upon detection of an uncorrectable header check sequence error. The ATM cell payloads are descrambled and are written to a programmable depth cell FIFO buffer. For quad OC-48 operation, four virtual FIFOs are provided. The received cells are read from the FIFO using a 16-bit wide POS-PHY Level 4 (622 to 700 Mbit/s) data path interface. Counts of received ATM cell, errored and uncorrectable cells and errored and correctable cells are accumulated independently for performance monitoring purposes.

When used to implement POS interfaces, the S/UNI 9953 extracts POS frames from the SONET (SDH) synchronous payload envelope. Frames are verified for correct construction and size. The control escape characters are removed. The frame check sequence is optionally verified for correctness and the extracted packets are placed in a receive FIFO. For quad OC-48 operation, four virtual FIFOs are provided. The received packets are read from the FIFO through a 16-bit wide POS-PHY Level 4 (622 to 700 Mbit/s) data path interface. Valid and FCS errored packet counts are provided for performance monitoring. The S/UNI 9953 POS implementation is flexible enough to support several link layer protocols, including HDLC, PPP and Frame Relay.

Downloaded by [illegible] on Wednesday, February [illegible] 12:[illegible] PM

When used to implement GFP interfaces, the S/UNI 9953 extracts GFP frames from the SONET (SDH) synchronous payload envelope. Frames are verified for correct construction and size. Frame delineation is performed using the cHEC field and are placed in a receive FIFO. Other HEC fields are optionally verified. Extended headers are optionally supported. The received packets are read from the FIFO through a 16-bit wide POS-PHY Level 4 (622 to 700 Mbit/s) data path interface. Valid and erred frame counts are provided for performance monitoring.

When used to implement 10 Gigabit Ethernet WAN PHY interfaces, the S/UNI 9953 extracts Ethernet frames from the SONET (SDH) synchronous payload envelope using frame delineation. When used to implement 10 Gigabit Ethernet LAN PHY interfaces, the S/UNI 9953 extracts Ethernet frames from the XSBI data stream using similar frame delineation. Frames are verified for correct construction and size. The frame check sequence is optionally verified for correctness and the extracted packets are placed in a receive FIFO. The received packets are read from the FIFO through a 16-bit wide POS-PHY Level 4 (622 to 700 Mbit/s) data path interface. The full suite of Ethernet statistics are counted and provided for performance monitoring. The S/UNI 9953 frame delineation implementation is flexible enough to support any packet based link layer frame.

The S/UNI 9953 transmits SONET (SDH) streams using four 4 bit parallel interfaces for quad OC-48 operation and a sixteen bit parallel interface for OC-192 operation. For both modes of operation, the S/UNI 9953 inserts section, line, and path overhead. The S/UNI 9953 performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and creates section, line, and path bit interleaved parity codes (B1, B2, B3) as required to allow performance monitoring at the far end. Line and path remote error indications (M1, G1) are also inserted. The S/UNI 9953 generates the payload pointer (H1, H2) and inserts the synchronous payload envelope that carries the ATM cells, POS frames and 10 Gigabit Ethernet frames. The S/UNI 9953 also supports the insertion of a large variety of errors into the transmit stream such as framing pattern errors, bit interleaved parity errors, and illegal pointers, which are useful for system diagnostics and tester applications.

The S/UNI 9953 transmits a 10 Gigabit Ethernet data stream at 10320 Mbit/s using a sixteen bit parallel XSBI interface derived from the OIF99.102.5 SFI-4 specification.

When used to implement ATM UNI or NNI interfaces, ATM cells are written to an internal programmable FIFO via a 16-bit wide POS-PHY Level 4 (622 to 700 Mbit/s) data path interface. For quad OC-48 and channelized OC-192 operation, four virtual FIFOs are provided. Idle/unassigned cells are automatically inserted when the internal FIFO contains less than one complete cell. The S/UNI 9953 provides generation of the header check sequence and scrambles the payload of the ATM cells. Each of these transmit ATM cell processing functions can be enabled or bypassed.

When used to implement POS interfaces, the S/UNI 9953 inserts POS frames into the SONET (SDH) synchronous payload envelope. Packets to be transmitted are written to an internal programmable FIFO via a 16-bit wide POS-PHY Level 4 (622 to 700 Mbit/s) data path interface. For quad OC-48 and channelized OC-192 operation, four virtual FIFOs are provided. POS frames are built by inserting the flags, control escape characters and the FCS fields. Either the CRC-CCITT (STS-48c/STM-16c) or CRC-32 can be computed and added to the frame.

Downloaded by [illegible] from Document Center Inc on 12-Feb-2007 16:59:24 EST

When used to implement GFP interfaces, the S/UNI 9953 inserts GFP frames into the SONET (SDH) synchronous payload envelope. Packets to be transmitted are written to an internal programmable FIFO via a 16-bit wide POS-PHY Level 4 (622 to 700 Mbit/s) data path interface. Pre-formatted GFP frames, including the PLI field, are read from the FIFO and GFP frames are built by over writing the various HEC fields with calculated data.

When used to implement 10 Gigabit Ethernet WAN PHY interfaces, the S/UNI 9953 inserts Ethernet frames into the SONET (SDH) synchronous payload envelope. When used to implement 10 Gigabit Ethernet LAN PHY interfaces, the S/UNI 9953 inserts Ethernet frames into the XSBI data stream. Packets to be transmitted are written to an internal programmable FIFO via a 16-bit wide POS-PHY Level 4 (622 to 700 Mbit/s) data path interface. Ethernet frames are built by inserting the preamble and the FCS fields. Counters are provided for Ethernet statistics support. Note, 10 Gigabit Ethernet WAN PHY feature is only supported for the unchannelized OC-192 mode of operation.

The S/UNI 9953 is configured, controlled and monitored via a generic 16-bit microprocessor bus interface. The S/UNI 9953 also provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.

The S/UNI 9953 is implemented in low power, +1.8 Volt, CMOS technology in the digital-core. It has +3.3 Volt TTL compatible digital inputs and TTL/CMOS compatible digital outputs. High-speed inputs and outputs are compliant to LVDS standards. The S/UNI 9953 is packaged in an 1152 pin Flip-Chip BGA (FCBGA) package.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 6:59:32 PM

8 Pin Diagram

Figure 9 Ball View

	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A		VDDI	TDAT_N[0]	TDAT_N[3]	TDAT_N[4]	TDAT_N[7]	VSS	VDDO	TDAT_N[9]	TDCLK_N	TDAT_N[11]	TDAT_N[12]	VSS	VDDI	TSTAT[0]	TTOHCLK[3]	TTOHCLK[1]	TTOHCLK[2]	TTOH[4]	TTOHEN[1]	VDDI	VSS	TPOHFP[4]	TPOH[2]	TPOHEN[4]	TPOHEN[2]	VDDO	VSS	SALM[4]	TCLK[2]	PGMTCLK[4]	VCLK4	VDDI		A
B	VDDI	VDDI	VSS	TDAT_P[0]	TDAT_P[3]	TDAT_P[4]	TDAT_P[7]	VDDO	VSS	TDAT_P[9]	TDCLK_P	TDAT_P[11]	TDAT_P[12]	VDDI	VSS	TSTAT[1]	TTOHCLK[4]	TTOHFP[4]	TTOHFP[2]	VSS	VDDI	TPOHFP[3]	TPOH[1]	TPOH[4]	TPOHEN[1]	VSS	VDDO	SALM[3]	TCLK[1]	PGMTCLK[3]	VCLK3	VSS	VDDI	VDDI	B
C	PL4_AVDL3	VSS	VSS	VDDO	TDAT_N[1]	TDAT_N[2]	TDAT_N[5]	TDAT_N[8]	VSS	VDDO	TDAT_N[10]	TDAT_N[13]	TDAT_N[14]	NC1	VSS	VDDI	VSS	VSS	VDDI	VSS	TTOHEN[2]	TPOHCLK[4]	TPOHCLK[2]	TPOHEN[3]	VDDO	VSS	TPOHRDY[2]	TCLK[4]	PGMTCLK[2]	VCLK2	VDDO	VSS	VSS	VDDI	C
D	PL4_ATB2	PL4_OAVD	VDDO	VDDO	VSS	TDAT_P[1]	TDAT_P[2]	TDAT_P[5]	TDAT_P[8]	VDDO	VSS	TDAT_P[10]	TDAT_P[13]	TDAT_P[14]	TSCLK	VDDI	VSS	VSS	VDDI	TTOH[2]	TPOHCLK[3]	TPOHCLK[1]	TPOH[3]	VSS	VDDO	TPOHRDY[1]	TCLK[3]	PGMTCLK[1]	VCLK1	VSS	VDDO	VDDO	VSS	PHASE_ERR[4]	D
E	RDAT_P[0]	PL4_ATB0	REFCLK_N	VSS	VSS	VDDI	PL4_AVDL1	PL4_AVDH2	TDAT_N[6]	VSS	VSS	VDDO	TDAT_N[15]	TCTL_N	NC3	NC4	VSS	VSS	TTOH[3]	TTOH[1]	TTOHEN[4]	TPOHFP[2]	VDDO	VSS	TPOHRDY[4]	SALM[2]	RALM[3]	RALM[1]	VDDI	VSS	VSS	VDDO	PHASE_ERR[3]	TXDATA4_P[0]	E
F	RDAT_P[3]	RDAT_N[0]	PL4_ATB5	REFCLK_P	VDDI	VDDI	VSS	PL4_AVDH1	VSS	TDAT_P[6]	VSS	VDDO	VSS	TDAT_P[15]	TCTL_P	NC2	DTRB	TTOHFP[3]	TTOHFP[1]	TTOHEN[3]	TPOHFP[1]	VSS	VDDO	TPOHRDY[3]	SALM[1]	RALM[4]	RALM[2]	VSS	VDDI	VDDI	VSS	PHASE_INIT[1]	TXDATA4_N[0]	TXCLK4_P	F
G	VSS	RDAT_N[3]	RDAT_P[1]	PL4_ATB4	PL4_ATB3	VSS	VSS	VDDI	VDDI	VSS	VDDO	VSS	VSS	VDDO	VSS	VDDI	VSS	VSS	VDDO	VSS	VDDO	VSS	VSS	VSS	NC5	MDC	VDDI	VSS	VSS	VDDI	PHASE_ERR[1]	TXDATA4_P[3]	TXCLK4_N	VSS	G
H	VDDO	VDDO	RDAT_P[4]	RDAT_N[1]	PL4_RESK	PL4_ATB1	VDDI	VDDI	VSS	VDDI	VSS	VDDO	VSS	VDDO	VSS	VSS	VDDI	VDDO	VSS	VSS	VDDO	VSS	VSS	NC6	MDIO	VSS	VDDI	VDDI	VSS	PHASE_INIT[4]	TXDATA4_N[3]	TXCLK_SRC4_N	VDDO	VDDO	H
J	RDAT_P[6]	VSS	VSS	RDAT_N[4]	RDAT_P[2]	PL4_RES	PL4_AVDH3	VSS	VSS	VDDI	VDDI	VDDI	VDDO	VDDO	VSS	VDDO	VSS	VSS	VDDO	VSS	VDDO	VDDO	VDDI	VDDI	VDDI	VSS	VSS	VDDI	PHASE_INIT[3]	TXDATA4_P[1]	TXCLK_SRC4_P	VSS	VSS	TXDATA3_P[1]	J
K	RDCLK_P	RDAT_N[6]	VDDO	VDDO	RDAT_P[5]	RDAT_N[2]	VDDO	PL4_AVDL2	VDDI	VDDI	VSS	VDDI	VDDI	VDDO	VDDO	VDDO	VSS	VSS	VDDO	VDDO	VDDO	VDDI	VDDI	VSS	VDDI	VDDI	VSS	PHASE_INIT[2]	TXDATA4_N[1]	TXDATA4_P[2]	VDDO	VDDO	TXDATA3_N[1]	TXDATA3_P[3]	K
L	RDAT_P[1]	RDCLK_N	RDAT_P[7]	VSS	VSS	RDAT_N[5]	VSS	VDDO	VDDI	VSS	VSS	VDDI	VDDI	VDDI	VDDO	VDDO	VSS	VSS	VDDO	VDDO	VDDI	VDDI	VDDI	VSS	VSS	VDDI	PHASE_ERR[2]	OIFS_AVDH	TXDATA4_N[2]	VSS	VSS	TXDATA3_P[2]	TXDATA3_N[3]	TXDATA3_P[0]	L
M	RDAT_P[4]	RDAT_N[1]	RDAT_P[9]	VDDO	VDDO	RDAT_N[7]	VDDO	VDDI	VDDI	VDDI	VDDI	VDDI	VSS	VDDI	VDDI	VDDO	VDDO	VDDO	VDDO	VDDI	VDDI	VSS	VDDI	VDDI	VDDI	VSS	OIFS_RES	VDDO	VDDO	TXDATA3_N[2]	TXCLK_SRC2_N	TXDATA3_N[0]	TXCLK3_P	M
N	VSS	RDAT_N[14]	RDAT_P[12]	RDAT_N[9]	RDAT_P[8]	VSS	VSS	VDDI	VDDO	VDDI	VDDI	VSS	VSS	VDDI	VDDI	VDDI	VDDO	VDDO	VDDI	VDDI	VDDI	VSS	VSS	VDDI	VDDI	VDDO	OIFS_RESK	VSS	VSS	TXCLK_SRC3_N	TXCLK_SRC2_P	TXDATA2_P[3]	TXCLK3_N	VSS	N
P	VDDI	VDDI	RDAT_P[15]	RDAT_N[12]	RDAT_P[10]	RDAT_N[8]	VDDO	VDDO	VDDO	VDDO	VDDI	VDDI	VDDI	VDDI	VSS	VDDI	VDDI	VDDI	VDDI	VSS	VDDI	VDDI	VDDI	VDDI	VDDO	VDDO	VDDO	VDDO	TXCLK_SRC3_P	TXCLK2_P	TXDATA2_N[3]	TXDATA2_P[1]	VDDI	VDDI	P
R	RCTL_P	VSS	VSS	RDAT_N[15]	RDAT_P[13]	RDAT_N[10]	VSS	VSS	VSS	VDDO	VDDO	VDDI	VDDI	VSS	VSS	VDDI	VSS	VSS	VDDI	VSS	VSS	VDDI	VDDI	VDDO	VDDO	VSS	VSS	TXCLK2_N	TXDATA2_P[0]	TXDATA2_N[1]	VSS	VSS	TXDATA2_P[2]	R
T	RSCLK	RCTL_N	VDDI	VDDI	REFSEL[1]	RDAT_N[13]	VDDO	VSS	VDDO	VDDO	VDDO	VDDO	VDDI	VDDI	VDDI	VDDI	VSS	VSS	VDDI	VDDI	VDDI	VDDI	VDDO	VDDO	VDDO	VDDO	VSS	VDDI	TXDATA2_N[0]	TXCLK1_P	VDDI	VDDI	TXDATA2_N[2]	TXCLK_SRC1_N	T
U	RSTAT[1]	NC7	VCLKS	VSS	VSS	REFSEL[0]	NC12	VDDO	VSS	VSS	VSS	VDDO	VDDO	VDDI	VSS	VSS	VSS	VSS	VSS	VSS	VDDI	VDDO	VDDO	VSS	VSS	VSS	VDDI	VSS	TXCLK1_N	VSS	VSS	TXDATA1_N[3]	TXCLK_SRC1_P	TXDATA1_N[1]	U
V	RSTAT[0]	PAUSE	VCLK6	VSS	VSS	TMS	NC13	VDDI	VSS	VSS	VSS	VDDO	VDDO	VDDI	VSS	VSS	VSS	VSS	VSS	VSS	VDDI	VDDO	VDDO	VSS	VSS	VSS	VDDO	VSS	OIFS_ATB1	VSS	VSS	TXDATA1_P[3]	TXDATA1_N[2]	TXDATA1_P[1]	V
W	PAUSED	TDO	VDDI	VDDI	TRSTB	WRB	VDDI	VSS	VDDO	VDDO	VDDO	VDDO	VDDI	VDDI	VDDI	VDDI	VSS	VSS	VDDI	VDDI	VDDI	VDDI	VDDO	VDDO	VDDO	VDDO	VSS	VDDO	RXDATA4_P[1]	OIFS_ATB0	VDDI	VDDI	TXDATA1_N[0]	TXDATA1_P[2]	W
Y	TCK	VSS	VSS	TDI	RDB	NC11	VSS	VSS	VSS	VDDO	VDDO	VDDI	VDDI	VSS	VSS	VDDI	VSS	VSS	VDDI	VSS	VSS	VDDI	VDDI	VDDO	VDDO	VSS	VSS	VSS	RXDATA4_P[3]	RXDATA4_N[1]	RXDATA4_P[0]	VSS	VSS	TXDATA1_P[0]	Y
AA	VDDI	VDDI	NC9	CSB	NC10	D[6]	VDDO	VDDO	VDDO	VDDO	VDDI	VDDI	VDDI	VDDI	VSS	VDDI	VDDI	VDDI	VDDI	VSS	VDDI	VDDI	VDDI	VDDI	VDDO	VDDO	VDDO	VDDO	RXCLK3_P	RXDATA4_N[3]	RXDATA4_P[2]	RXDATA4_N[0]	VDDI	VDDI	AA
AB	VSS	VCLK7	ALE	D[15]	D[7]	VSS	VSS	VDDI	VDDO	VDDI	VDDI	VSS	VSS	VDDI	VDDI	VDDI	VDDO	VDDO	VDDI	VDDI	VDDI	VSS	VSS	VDDI	VDDI	VDDO	APS_ATB1	VSS	VSS	RXCLK3_N	RXDATA3_P[1]	RXDATA4_N[2]	RXCLK4_P	VSS	AB
AC	VCLK8	RSTB	D[14]	D[8]	VDDO	VDDO	VDDI	VSS	VDDI	VDDI	VDDI	VDDI	VSS	VDDI	VDDI	VDDO	VDDO	VDDO	VDDO	VDDI	VDDI	VSS	VDDI	VDDI	VDDI	VDDI	VSS	APS_ATB0	VDDO	VDDO	RXCLK2_P	RXDATA3_N[1]	RXDATA3_P[0]	RXCLK4_N	AC
AD	INTB	D[13]	D[9]	VSS	VSS	D[5]	VSS	VDDO	VDDI	VSS	VSS	VDDI	VDDI	VDDI	VDDO	VDDO	VSS	VSS	VDDO	VDDO	VDDI	VDDI	VDDI	VSS	VSS	VDDI	APS_OSCB	VSS	RXDATA2_P[3]	VSS	VSS	RXCLK2_N	RXDATA3_P[2]	RXDATA3_N[3]	AD
AE	D[12]	D[10]	VDDO	VDDO	D[4]	A[10]	VDDO	BTEST	VDDI	VDDI	VSS	VDDI	VDDI	VDDO	VDDO	VDDO	VSS	VSS	VDDO	VDDO	VDDO	VDDI	VDDI	VSS	VDDI	VDDI	VSS	APS_OSC	RXDATA1_P[1]	RXDATA2_N[3]	VDDO	VDDO	RXDATA3_P[0]	RXDATA3_N[2]	AE
AF	D[11]	VSS	VSS	D[3]	A[11]	A[9]	DTEST[1]	VSS	VSS	VDDI	VSS	VSS	VSS	VSS	VSS	VDDO	VSS	VSS	VDDO	VSS	VSS	VSS	VSS	VSS	VDDI	VSS	VSS	VSS	RXDATA1_P[2]	RXDATA1_N[1]	RXDATA2_P[0]	VSS	VSS	RXDATA3_N[0]	AF
AG	VDDO	VDDO	D[2]	A[12]	A[8]	QUAD248B	VDDI	VDDI	VSS	VSS	VDDI	VSS	VDDO	VDDO	VSS	VSS	IAPSFP	VDDO	VSS	VSS	VDDO	VDDI	VSS	IAPS4_P[2]	APS_AVDL4	VSS	VDDI	VDDI	VSS	RXDATA1_N[2]	RXDATA2_P[1]	RXDATA2_N[0]	VDDO	VDDO	AG
AH	VSS	D[1]	A[13]	A[7]	LAN	VSS	VSS	VDDI	VSS	VDDI	VSS	VDDO	VSS	VDDO	VSS	OAPSFP	NC8	IAPSFPC1K	VDDO	VSS	VSS	VDDO	VSS	VDDI	VSS	IAPS4_N[2]	APS_AVDL3	VDDI	VSS	VSS	APS_QAVD	RXDATA1_P[0]	RXDATA2_N[1]	RXDATA2_P[2]	VSS	AH
AJ	D[0]	A[14]	A[6]	A[0]	VDDI	VDDI	VSS	RTOHFP2]	RTOHFP[4]	RTOH[2]	RPOHFP[4]	VDDO	VSS	RPOHEN[1]	B3E[4]	B3E[1]	IAPS1_P[0]	OAPS1_N[1]	OAPS1_N[2]	OAPS2_N[1]	OAPS2_N[2]	VSS	VDDO	OAPS3_N[3]	IAPS4_P[0]	OAPS4_N[1]	APS_RES	VSS	VDDI	VDDI	RXDATA1_P[3]	RXDATA1_N[0]	RXCLK1_P	RXDATA2_N[2]	AJ
AK	DTEST[0]	A[5]	A[1]	VSS	VSS	VDDI	RTOHFP1]	RTOHFP3]	RTOH[1]	RPOHFP3]	VSS	VDDO	RPOHEN[2]	B3E[3]	B3E[2]	IAPS1_N[0]	VSS	VSS	OAPS1_P[1]	OAPS1_P[2]	OAPS2_P[1]	OAPS2_P[2]	VDDO	VSS	OAPS3_P[3]	IAPS4_N[0]	OAPS4_P[1]	APS_AVDL2	VDDI	VSS	VSS	RXDATA1_N[3]	SYNC_ERR[2]	RXCLK1_N	AK
AL	A[4]	A[2]	VDDO	VDDO	VSS	RTOHCLK[4]	RPOHCLK[2]	RPOHCLK[4]	RPOHFP[1]	VDDO	VSS	RPOHEN[4]	PGMRCLK[1]	PGMRCLK[4]	IAPS1_P[3]	VDDI	VSS	VSS	VDDI	OAPS2_N[0]	OAPS2_N[3]	IAPS3_P[0]	IAPS3_P[3]	VSS	VDDO	OAPS3_N[2]	IAPS4_P[3]	OAPS4_N[2]	APS_AVDH1	VSS	VDDO	VDDO	SYNC_ERR[4]	SYNC_ERR[1]	AL
AM	A[3]	VSS	VSS	VDDO	RTOHCLK[3]	RPOHCLK[1]	RPOHCLK[3]	RPOH[1]	VSS	VDDO	RPOHEN[3]	PGMRCLK[2]	PGMRCLK[3]	IAPS1_N[3]	VSS	VDDI	IAPS2_N[1]	IAPS2_P[1]	VDDI	VSS	OAPS2_P[0]	OAPS2_P[3]	IAPS3_N[0]	IAPS3_N[3]	VDDO	VSS	OAPS3_P[2]	IAPS4_N[3]	OAPS4_P[2]	APS_AVDL1	VDDO	VSS	VSS	SYNC_ERR[3]	AM
AN	VDDI	VDDI	VSS	RTOHCLK[2]	RTOH[4]	RPOHFP[2]	RPOH[4]	VDDO	VSS	RCLK[2]	RCLK[4]	IAPS1_P[1]	IAPS1_P[2]	VDDI	VSS	OAPS1_N[0]	OAPS1_N[3]	IAPS2_P[3]	IAPS2_P[0]	IAPS2_N[3]	VSS	VDDI	IAPS3_P[1]	IAPS3_P[2]	IAPS3_N[1]	OAPS3_N[0]	VSS	VDDO	IAPS4_P[1]	OAPS4_N[0]	APS_AVDH2	VSS	VDDI	VDDI	AN
AP		VDDI	RTOHCLK[1]	RTOH[3]	RPOH[2]	RPOH[3]	VSS	VDDO	RCLK[1]	RCLK[3]	IAPS1_N[1]	IAPS1_N[2]	VSS	VDDI	OAPS1_P[0]	OAPS1_P[3]	IAPS2_N[0]	IAPS2_P[0]	IAPS2_N[3]	IAPS2_N[2]	VDDI	VSS	IAPS3_N[1]	IAPS3_N[2]	OAPS3_P[1]	OAPS3_P[0]	VDDO	VSS	IAPS4_N[1]	OAPS4_P[0]	OAPS4_P[3]	APS_RESK	VDDI		AP
	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Download

9 Pin Description

9.1 Configuration Pin Signals (2)

Pin Name	Type	Pin No.	Function
QUAD2488	Input (integral pull-down)	AG29	The **quad 2488 Mbit/s mode select** (QUAD2488) signal selects between the OC-192 or quad OC-48 Line Side Interface modes. When QUAD2488 is low, the device is in OC-192 Line Side Interface mode. When QUAD2488 is high, the device is in quad OC-48 Line Side Interface mode. QUAD2488 must be strapped to low for IEEE 802.3ae 10 Gigabit Ethernet (10 GbE) PHY operation. QUAD2488 is considered static input and has an integral pull-down resistor.
LAN	Input (integral pull-down)	AH30	The **LAN mode select** (LAN) signal selects between the 10 GbE LAN or WAN PHY operation modes. When LAN is low, the device is in 10 GbE WAN PHY operation mode. When LAN is high, the device is in 10 GbE LAN PHY operation mode. For LAN PHY operation, QUAD2488 must be set to low and the SSMODE[1:0] in the S/UNI 9953 Master Reset and Configuration register must be set to b'00. LAN is considered static input and has an integral pull-down resistor.

9.2 Management Interface Signals (2)

Pin Name	Type	Pin No.	Function
MDIO	I/O	H10	Management Data Input/Output (MDIO) signal sends management frames and received status data from external MII PHY device. Output management frame bit serial signal is updated on the rising edge of MDC. Input bit serial status data is sampled on the rising edge of MDC.
MDC	Output	G9	Management Data Clock (MDC) signal is a CPREF_CLK/32 MHz nominally 50% duty cycle clock.

Downloaded by Content Team of Partner Inc. on Wednesday, February, 2011 09:32 PM

9.3 Line Side Interface Signals (100)

Pin Name	Type	Pin No.	Function
RXCLK4+ RXCLK4- RXCLK3+ RXCLK3- RXCLK2+ RXCLK2- RXCLK1+ RXCLK1-	Analog LVDS Input	AB2 AC1 AA6 AB5 AC4 AD3 AJ2 AK1	The **differential receive clock** (RXCLK[4:1]) inputs provide timing for the S/UNI 9953 receive operation. For SONET/SDH operation, RXCLK[N]+/- is a 622.08 MHz nominally 50% duty cycle clock. For 10 Gigabit Ethernet LAN PHY operation, RXCLK[N]+/- is a 644.53125 MHz nominally 50% duty cycle clock. For quad OC-48 mode, the rising edge of RXCLK[N]+/- is used to sample the respective RXDATA[N][3:0]+/- receive data bus (i.e. RXCLK1+/- is used to sample RXDATA1[3:0]). For OC-192 and 10 Gigabit Ethernet LAN PHY modes, the rising edge of RXCLK2+/- is used to sample the four RXDATA[4:1][3:0] buses. RXCLK1+/-, RXCLK3+/- and RXCLK4+/- are not used. Please refer to the Operation section for description in handling unused differential LVDS inputs.
RXDATA4[3]+ RXDATA4[3]- RXDATA4[2]+ RXDATA4[2]- RXDATA4[1]+ RXDATA4[1]- RXDATA4[0]+ RXDATA4[0]- RXDATA3[3]+ RXDATA3[3]- RXDATA3[2]+ RXDATA3[2]- RXDATA3[1]+ RXDATA3[1]- RXDATA3[0]+ RXDATA3[0]- RXDATA2[3]+ RXDATA2[3]- RXDATA2[2]+ RXDATA2[2]- RXDATA2[1]+ RXDATA2[1]- RXDATA2[0]+ RXDATA2[0]- RXDATA1[3]+ RXDATA1[3]- RXDATA1[2]+ RXDATA1[2]- RXDATA1[1]+ RXDATA1[1]- RXDATA1[0]+ RXDATA1[0]-	Analog LVDS Input	Y6 AA5 AA4 AB3 W6 Y5 Y4 AA3 AC2 AD1 AD2 AE1 AB4 AC3 AE2 AF1 AD6 AE5 AH2 AJ1 AG4 AH3 AF4 AG3 AJ4 AK3 AF6 AG5 AE6 AF5 AH4 AJ3	The **differential receive data** (RXDATA[4:1][3:0]) inputs carry the byte-serial STS-48c (STM-16c), STS-192 (STM-64) or 10 Gigabit Ethernet (LAN PHY) streams. For SONET/SDH operation, each differential pair is a 622.08 Mbit/s stream. For 10 Gigabit Ethernet LAN PHY operation, each differential pair is a 644.53125 Mbit/s stream. For quad OC-48 mode, each of the four RXDATA[N][3:0]+/- buses represents a single STS-48c (STM-16c) stream. RXDATA[N][3]+/- is the most significant bit (corresponding to bit 1 of each serial word, the first bit received). RXDATA[N][0]+/- is the least significant bit (corresponding to bit 4 of each word, the last bit received). RXDATA[N][3:0]+/- is sampled on the rising edge of the corresponding RXCLK[N]+/-. For quad OC-48 operation, the OIF_LSB_1ST bit in the S/UNI 9953 Master Reset and Configuration Register must be set to logic 0. For OC-192 mode, the four RXDATA[N][3:0]+/- buses represents a single STS-192 (STM-64) stream. RXDATA4[3:0]+/- represents the most significant nibble while RXDATA1[3:0]+/- represents the least significant nibble of the received word. RXDATA4[3]+/- is the most significant bit (corresponding to bit 1 of each serial word, the first bit received). RXDATA1[0]+/- is the least significant bit (corresponding to bit 16 of each word, the last bit received). RXDATA[4:1][3:0]+/- is sampled on the rising edge of the RXCLK2+/-. For OC-192 operation, the OIF_LSB_1ST bit in the S/UNI 9953 Master Reset and Configuration Register must be set to logic 0.

Downloaded by Document Team of Partmine Inc on Tuesday, February 14, 2017 08:55:55 PM

Pin Name	Type	Pin No.	Function
			For 10 Gigabit Ethernet LAN PHY mode, the four RXDATA[N][3:0]+/- buses represents a single 10320 Mbit/s stream. For IEEE 802.3ae XSBI compliant operation, the OIF_LSB_1ST bit in the S/UNI 9953 Master Reset and Configuration Register must be set to logic 1. RXDATA4[3:0]+/- represents the least significant nibble while RXDATA1[3:0]+/- represents the most significant nibble of the received XSBI word. RXDATA4[3]+/- is the most significant bit (corresponding to bit 15 of each XSBI serial word, the last bit received). RXDATA1[0]+/- is the least significant bit (corresponding to bit 0 of each XSBI word, the first bit received). RXDATA[4:1][3:0]+/- is sampled on the rising edge of the RXCLK2+/-.
SYNC_ERR4 SYNC_ERR3 SYNC_ERR2 SYNC_ERR1	Schmidt TTL Input (integral pull-down)	AL2 AM1 AK2 AL1	The **synchronization error** (SYNC_ERR[4:1]) inputs indicate if the RXDATA[4:1]+/- buses can be safely sampled. The SYNC_ERR_XOR bit in the S/UNI 9953 Master Reset and Configuration Register controls the active logic level of the SYNC_ERR[4:1] inputs. The SYNC_ERR[4:1] signals are treated as asynchronous inputs. When SYNC_ERR[N] is high and SYNC_ERR_XOR is logic 0, RXDATA[N]+/- is not derived from the optical line and is suspect. When SYNC_ERR[N] is low and SYNC_ERR_XOR is logic 0, RXDATA[N]+/- is recovered from the optical stream. When SYNC_ERR[N] is low and SYNC_ERR_XOR is logic 1, RXDATA[N]+/- is not derived from the optical line and is suspect. When SYNC_ERR[N] is high and SYNC_ERR_XOR is logic 1, RXDATA[N]+/- is recovered from the optical stream. For quad OC-48 mode, SYNC_ERR[N] indicates the validity of the RXDATA[N][3:0]+/- receive data bus (i.e. SYNC_ERR1 validates RXDATA1[3:0]). For OC-192 and 10 Gigabit Ethernet LAN PHY modes, SYNC_ERR1 indicates the validity of the RXDATA[4:1][3:0]+/- receive data buses. SYNC_ERR2, SYNC_ERR3 and SYNC_ERR4 are not used and must be strapped low.

Downloaded by Content Team of Partminer Inc on Nov 01 2007 (IST) 10:39:53 AM

Pin Name	Type	Pin No.	Function
TXCLK_SRC4+ TXCLK_SRC4- TXCLK_SRC3+ TXCLK_SRC3- TXCLK_SRC2+ TXCLK_SRC2- TXCLK_SRC1+ TXCLK_SRC1-	Analog LVDS Input	J4 H3 P6 N5 N4 M3 U2 T1	The **differential transmit clock source** (TXCLK_SRC[4:1]) inputs provide timing for the S/UNI 9953 transmit operation. For SONET/SDH operation, TXCLK_SRC[N]+/- is a 622.08 MHz nominally 50% duty cycle clock. For 10 Gigabit Ethernet LAN PHY operation, TXCLK_SRC2+/- is a 644.53125 MHz nominally 50% duty cycle clock. For quad OC-48 mode, the TXCLK_SRC[N]+/- is used to clock the respective OC-48 slice. TXCLK_SRC[N]+/- is looped back internally as the corresponding TXCLK[N]+/- output (i.e. TXCLK_SRC1+/- is looped back as TXCLK1+/-). For OC-192 and 10 Gigabit Ethernet LAN PHY modes, TXCLK_SRC2+/- is used to clock the transmit side. TXCLK_SRC2+/- is looped back internally as the TXCLK2+/- output. TXCLK1_SRC+/-, TXCLK3_SRC+/- and TXCLK4_SRC+/- are not used. Please refer to the Operation section for description in handling unused differential LVDS inputs.
TXCLK4+ TXCLK4- TXCLK3+ TXCLK3- TXCLK2+ TXCLK2- TXCLK1+ TXCLK1-	Analog LVDS Output	F1 G2 M1 N2 P5 R6 T5 U6	The **differential transmit clock** (TXCLK[4:1]) outputs provide timing references for the corresponding transmit TXDATA[N][3:0]+/- buses. For SONET/SDH operation, TXCLK[N]+/- is a 622.08 MHz nominally 50% duty cycle clock. For 10 Gigabit Ethernet LAN PHY operation, TXCLK2+/- is a 644.53125 MHz nominally 50% duty cycle clock. For quad OC-48 mode, the rising edge of TXCLK[N]+/- is used to update the corresponding TXDATA[N][3:0]+/- bus. TXCLK[N]+/- is an internally looped back version of the corresponding TXCLK_SRC[N]+/- input (i.e. TXCLK_SRC1+/- is looped back as TXCLK1+/-). For OC-192 and 10 Gigabit Ethernet LAN PHY modes, the rising edge of TXCLK2+/- is used to update the TXDATA[4:1][3:0]+/- bus. TXCLK1+/-, TXCLK3+/- and TXCLK4+/- should not be used and are optionally held static.

Downloaded by Content Team of Partminer Inc on Wednesday, Feb 20 2008 6:53:00 PM

Pin Name	Type	Pin No.	Function
TXDATA4[3]+ TXDATA4[3]- TXDATA4[2]+ TXDATA4[2]- TXDATA4[1]+ TXDATA4[1]- TXDATA4[0]+ TXDATA4[0]- TXDATA3[3]+ TXDATA3[3]- TXDATA3[2]+ TXDATA3[2]- TXDATA3[1]+ TXDATA3[1]- TXDATA3[0]+ TXDATA3[0]- TXDATA2[3]+ TXDATA2[3]- TXDATA2[2]+ TXDATA2[2]- TXDATA2[1]+ TXDATA2[1]- TXDATA2[0]+ TXDATA2[0]- TXDATA1[3]+ TXDATA1[3]- TXDATA1[2]+ TXDATA1[2]- TXDATA1[1]+ TXDATA1[1]- TXDATA1[0]+ TXDATA1[0]-	Analog LVDS Output	G3 H4 K5 L6 J5 K6 E1 F2 K1 L2 L3 M4 J1 K2 L1 M2 N3 P4 R1 T2 P3 R4 R5 T6 V3 U3 W1 V2 V1 U1 Y1 W2	The **differential transmit data** (TXDATA[4:1][3:0]) outputs carry the byte-serial STS-48c (STM-16c), STS-192 (STM-64) or 10 Gigabit Ethernet (LAN PHY) streams. For SONET/SDH operation, each differential pair is a 622.08 Mbit/s stream. For 10 Gigabit Ethernet LAN PHY operation, each differential pair is a 644.53125 Mbit/s stream. For quad OC-48 mode, each of the four TXDATA[N][3:0]+/- buses represents a single STS-48c (STM-16c) stream. TXDATA[N][3]+/- is the most significant bit (corresponding to bit 1 of each serial word, the first bit transmitted). TXDATA[N][0]+/- is the least significant bit (corresponding to bit 4 of each word, the last bit transmitted). TXDATA[N][3:0]+/- is updated on the rising edge of the corresponding TXCLK[N]+/-. For quad OC-48 operation, the OIF_LSB_1ST bit in the S/UNI 9953 Master Reset and Configuration Register must be set to logic 0. For OC-192 mode, the four TXDATA[N][3:0]+/- buses represents a single STS-192 (STM-64) stream. TXDATA4[3:0]+/- represents the most significant nibble while TXDATA1[3:0]+/- represents the least significant nibble of the transmitted word. TXDATA4[3]+/- is the most significant bit (corresponding to bit 1 of each serial word, the first bit transmitted). TXDATA1[0]+/- is the least significant bit (corresponding to bit 16 of each word, the last bit transmitted). TXDATA[4:1][3:0]+/- is updated on the rising edge of the TXCLK2+/-. For OC-192 operation, the OIF_LSB_1ST bit in the S/UNI 9953 Master Reset and Configuration Register must be set to logic 0.
			For 10 Gigabit Ethernet LAN PHY mode, the four TXDATA[N][3:0]+/- buses represents a single 10320 Mbit/s stream. For IEEE 802.3ae XSBI compliant operation, the OIF_LSB_1ST bit in the S/UNI 9953 Master Reset and Configuration Register must be set to logic 1. TXDATA4[3:0]+/- represents the least significant nibble while TXDATA1[3:0]+/- represents the most significant nibble of the transmit XSBI word. TXDATA4[3]+/- is the most significant bit (corresponding to bit 15 of each XSBI serial word, the last bit transmitted). TXDATA1[0]+/- is the least significant bit (corresponding to bit 0 of each XSBI word, the first bit transmitted). TXDATA[4:1][3:0]+/- is updated on the rising edge of the TXCLK2+/-.

Downloaded by Content Team of Partminer Inc only for ... on Feb ... 16:53:...

Pin Name	Type	Pin No.	Function
PHASE_ERR4 PHASE_ERR3 PHASE_ERR2 PHASE_ERR1	Schmidt TTL Input (integral pull-down)	D1 E2 L8 G4	The **phase error** (PHASE_ERR[4:1]) inputs indicate when the TXCLK[4:1]+/- outputs are not aligned with the corresponding TXDATA[4:1]+/- buses. When asserted, the receiving device (optic module/SerDes) cannot use the source synchronous TXCLK[N]+/- to sample the corresponding TXDATA[N]+/- bus. PHASE_ERR[N] is treated as an asynchronous signal and is used to trigger maskable interrupts. In addition, the associated PHASE_INIT[N] output should be asserted to re-initiate alignment under user control. For quad OC-48 mode, PHASE_ERR[N] indicates a phase alignment error for the corresponding transmit TXCLK[N]+/- clock and TXDATA[N]+/- data bus. For OC-192 and 10 Gigabit Ethernet LAN PHY modes, PHASE_ERR1 indicates a phase alignment error for the TXCLK2 clock and the TXDATA[4:1][3:0]+/- bus. PHASE_ERR2, PHASE_ERR3 and PHASE_ERR4 are not used and must be strapped low.
PHASE_INIT4 PHASE_INIT3 PHASE_INIT2 PHASE_INIT1	Output	H5 J6 K7 F3	The **phase initialization** (PHASE_INIT[4:1]) outputs indicate to the receiving device (optic module/SerDes) that it should start the TXCLK[4:1]+/- and TXDATA[4:1]+/- alignment processes. The PHASE_INIT[N] output is directly sourced from the S/UNI 9953 STLI Phase Alignment register and should be treated as an asynchronous signal.

9.4 Alarms and Clocks (24)

Pin Name	Type	Pin No.	Function
PGMRCLK4 PGMRCLK3 PGMRCLK2 PGMRCLK1	Output	AL21 AM22 AM23 AL22	The **programmable receive clock** (PGMRCLK) signal provides timing reference for the receive line interface during SONET/SDH operation. For quad OC-48 mode, PGMRCLK[N] is a divided version of the receive clock, RXCLK[N]+/-. For OC-192 mode, PGMRCLK[N] is a divided version of the receive clock, RXCLK2+/-. PGMRCLK[N] can be programmed to be a nominal 8 kHz, 19.44 MHz or 77.76 MHz, 50% duty cycle clock or forced to low by setting the PGMRCLKSEL[N][1:0] bits in SRLI Programmable Clock Configuration register. PGMRCLK[4:1] are forced to low in 10 Gigabit Ethernet LAN PHY mode.

Downloaded by Content Team of Partminer Inc on Wednesday, January 17, 2007

Pin Name	Type	Pin No.	Function
RCLK4 RCLK3 RCLK2 RCLK1	Output	AN24 AP25 AN25 AP26	The **receive clock** (RCLK) signal provides timing reference for the receive interface. For quad OC-48 operation, RCLK[N] is a nominally 77.76 MHz 50% duty cycle clock derived from the receive clock, RXCLK[N]+/-. For OC-192 operation, RCLK[N] is a nominally 77.76 MHz 50% duty cycle clock derived from the receive clock, RXCLK2+/-. For 10 Gigabit Ethernet LAN PHY operation, RCLK[N] is a nominally 80.56640625 MHz 50% duty cycle clock derived from the receive clock, RXCLK2+/-. The RCLK[N] output can be disabled and held low by programming the RCLK[N]EN bit in the S/UNI 9953 Clock Configuration register.
PGMTCLK4 PGMTCLK3 PGMTCLK2 PGMTCLK1	Output	A4 B5 C6 D7	The **programmable transmit clock** (PGMTCLK) signal provides timing reference for the transmit line interface during SONET/SDH operation. For quad OC-48 operation, PGMTCLK[N] is a divided version of the transmit source clock, TXCLK_SRC[N]+/-. For OC-192 operation, PGMTCLK[N] is a divided version of the transmit source clock, TXCLK_SRC2+/-. PGMTCLK[N] can be programmed to be a nominal 8 kHz, 19.44 MHz or 77.76 MHz, 50% duty cycle clock or forced to low by setting the PGMTCLKSEL[N][1:0] bits in STLI PGM Clock Configuration register. PGMTCLK[4:1] are forced to low in 10 Gigabit Ethernet LAN PHY mode.
TCLK4 TCLK3 TCLK2 TCLK1	Output	C7 D8 A5 B6	The **transmit clock** (TCLK) signal provides timing reference for the transmit interface. For quad OC-48 operation, TCLK[N] is a nominally 77.76 MHz 50% duty cycle clock derived from the transmit source clock, TXCLK_SRC[N]+/-. For OC-192 operation, TCLK[N] is a nominally 77.76 MHz 50% duty cycle clock derived from the transmit source clock, TXCLK_SRC2+/-. For 10 Gigabit Ethernet LAN PHY operation, TCLK[N] is a nominally 80.56640625 MHz 50% duty cycle clock derived from the transmit source clock, TXCLK_SRC2+/-. The TCLK[N] output can be disabled and held low by programming the TCLK[N]EN bit in the S/UNI 9953 Clock Configuration register. SALM[N] and RALM[N] are updated on the rising edge of TCLK[N] for SONET/SDH operation.

Downloaded by Content Team of Partminer Inc on Monday, 16 January 2007 6:55:12 PM

Pin Name	Type	Pin No.	Function
SALM4 SALM3 SALM2 SALM1	Output	A6 B7 E9 F10	The **section alarm** (SALM) signal is set high when an out-of-frame (OOF), loss-of-signal (LOS), loss-of-frame (LOF), line alarm indication signal (LAIS), line remote defect indication (LRDI), section trace identifier mismatch (TIM-S), section trace identifier unstable (TIU-S), signal fail (SF) or signal degrade (SD) alarm is detected. Each alarm indication can be independently enabled using bits in the SARC Section SALM Enable registers. SALM is set low when none of the enabled alarms are active. SALM[N] is updated on the rising edge of TCLK[N] for SONET/SDH operation. When in OC-192 mode, only SALM1 is valid. SALM[N] is not used for 10 Gigabit Ethernet LAN PHY operation and should be ignored.
RALM4 RALM3 RALM2 RALM1	Output	F9 E8 F8 E7	The **Receive Alarm** (RALM) signal is an aggregated output of individual alarms of the receive path. Each alarm represents the logical OR of the SALM, LOP-P, AIS-P, RDI-P, ERDI-P, LOPC-P, PAISC-P, UNEQ-P, PSLU, PSLM, PDI-P, TIU-P, TIM-P status of the path. The selection of alarms to be reported is controlled by the SARC Path RALM Enable registers. RALM[N] is updated on the rising edge of TCLK[N] for SONET/SDH operation. When in OC-192 mode, only RALM1 is valid. Please refer to the individual alarm interrupt descriptions and Functional Description Section for more details on each alarm. RALM[N] is not used for 10 Gigabit Ethernet LAN PHY operation and should be ignored.

9.5 Receive Section/Line/Path Overhead Extraction Signals (32)

Pin Name	Type	Pin No.	Function
RTOHCLK4 RTOHCLK3 RTOHCLK2 RTOHCLK1	Output	AL29 AM30 AN31 AP32	The **receive transport overhead clock** (RTOHCLK) signal provides timing for the receive section and line overhead extraction during SONET/SDH operation. In STS-192c/STM-64c mode, RTOHCLK1 is a nominal 82.94 MHz clock generated by gapping a 103.68 MHz clock. RTOHCLK2-4 are not defined. In quad STS-48c/STM-16c mode,, RTOHCLK1-4 is a nominal 82.94 MHz clock generated by gapping a 103.68 MHz clock. When the RTOH interface is configured to extract either the section DCC bytes (D1-D3) or the line DCC bytes (D4-D12), the frequency of RTOHCLK1-4 will be either 192KHz or 576KHz respectively. RTOHCLK[N] is not used for 10 Gigabit Ethernet LAN PHY operation and should be ignored.

Downloaded by Content Team of Pacific Inc online on Wednesday, January, 2007 (IP: [redacted])

Pin Name	Type	Pin No.	Function
RTOHFP4 RTOHFP3 RTOHFP2 RTOHFP1	Output	AJ26 AK27 AJ27 AK28	The **receive transport overhead frame pulse** (RTOHFP) signal provides timing for the receive section and line overhead extraction during SONET/SDH operation. In STS-192c/STM-64c mode, RTOHFP1 is used to indicate the most significant bit (MSB) on RTOH1-4 and the first possible path BIP error on B3E1. RTOHFP2-4 are not defined. In quad STS-48c/STM-16c mode, RTOHFP1-4 is used to indicate the most significant bit (MSB) on RTOH1-4 and the first possible path BIP error on B3E1-4. RTOHFP[N] is set high when the MSB of the: First A1 byte is on RTOH[N]. RTOHFP[N] is updated on the rising edge of RTOHCLK[N]. RTOHFP[N] is not used for 10 Gigabit Ethernet LAN PHY operation and should be ignored.
RTOH4 RTOH3 RTOH2 RTOH1	Output	AN30 AP31 AJ25 AK26	The **receive transport overhead** (RTOH) signal contains the received transport overhead bytes (A1, A2, J0, Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, Z1/S1, Z2/M1, and E2) extracted from the incoming stream during SONET/SDH operation. Please refer to the Functional Description section for details. RTOH[N] is updated on the rising edge of RTOHCLK[N] when extracting all the overhead bytes. RTOH[N] is updated on the falling edge of RTOHCLK[N] when extracting the DCC bytes. RTOH[N] is not used for 10 Gigabit Ethernet LAN PHY operation and should be ignored.
RPOHCLK4 RPOHCLK3 RPOHCLK2 RPOHCLK1	Output	AL27 AM28 AL28 AM29	The **receive path overhead clock** (RPOHCLK) signal provides timing for the receive path overhead extraction during SONET/SDH operation. For STS-192c/STM-64c, only RPOHCLK1 is valid. RPOHCLK[N] is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. When the RPOH interface is configured to extract either the section DCC bytes (D1-D3) or the line DCC bytes (D4-D12), the frequency of RPOHCLK1-4 will be either 192KHz or 576KHz respectively. RPOHCLK[N] is not used for 10 Gigabit Ethernet LAN PHY operation and should be ignored.

Downloaded by Content Team of Partminer Inc on Monday 05 February, 2007 00:32:19

Pin Name	Type	Pin No.	Function
RPOHFP4 RPOHFP3 RPOHFP2 RPOHFP1	Output	AJ24 AK25 AN29 AL26	The **receive path overhead frame pulse** (RPOHFP) signal provides timing for the receive path overhead extraction during SONET/SDH operation. RPOHFP[N] is used to indicate the most significant bit (MSB) on RPOH[N] and the first possible path BIP error on B3E[N]. For STS-192c/STM-64c, only RPOHFP1 is valid. RPOHFP[N] is set high when the MSB of the first J1 byte is on RPOH[N]. RPOHFP[N] is updated on the falling edge of RPOHCLK[N] when extracting all of the overhead bytes. RPOHFP[N] is updated on the rising edge of RPOHCLK[N] when extracting the DCC bytes. RPOHFP[N] is not used for 10 Gigabit Ethernet LAN PHY operation and should be ignored.
RPOH4 RPOH3 RPOH2 RPOH1	Output	AN28 AP29 AP30 AM27	The **receive path overhead** (RPOH) signal contains the received path overhead bytes (J1, B3, C2, G1, F2, H4, Z3, Z4, and Z5) extracted from a STS-48c (STM-16c) or STS-192c (STM-64c) SONET (SDH) path overhead during SONET/SDH operation. The RPOHEN[N] signal is set high to indicate valid path overhead bytes on RPOH[N]. For STS-192c/STM-64c, only RPOH1 is valid. RPOH[N] is updated on the falling edge of RPOHCLK[N]. RPOH[N] is not used for 10 Gigabit Ethernet LAN PHY operation and should be ignored.
RPOHEN4 RPOHEN3 RPOHEN2 RPOHEN1	Output	AL23 AM24 AK22 AJ21	The **receive path overhead enable** (RPOHEN) signal indicates valid path overhead bytes on RPOH[N] during SONET/SDH operation. When RPOHEN[N] signal is set high, the corresponding path overhead byte presented on RPOH[N] is valid. When RPOHEN[N] is set low, the corresponding path overhead byte presented on RPOH[N] is invalid. For STS-192c/STM-64c, only RPOHEN1 is valid. RPOHEN[N] is updated on the falling edge of RPOHCLK[N]. RPOHEN[N] is not used for 10 Gigabit Ethernet LAN PHY operation and should be ignored.

Downloaded by Content Team of Partminer Inc or Vendor of Distributor

Pin Name	Type	Pin No.	Function
B3E4 B3E3 B3E2 B3E1	Output	AJ20 AK21 AK20 AJ19	The **bit interleaved parity error** (B3E) signal carries the path BIP-8 errors detected for the SPE payload during SONET/SDH operation. B3E[N] is set high for one RPOHCLK[N] clock cycle for each path BIP-8 error detected (up to eight errors per path per frame). When BIP-8 errors are treated on a block basis, B3E[N] is set high for one RPOHCLK[N] clock cycle for up to eight path BIP-8 errors detected (up to one error per path per frame). Path BIP-8 errors are detected by comparing the extracted path BIP-8 byte (B3) with the computed path BIP-8 byte of the previous frame. For STS-192c/STM-64c, only B3E1 is valid. B3E[N] is updated on the falling edge of RPOHCLK[N]. B3E[N] is not used for 10 Gigabit Ethernet LAN PHY operation and should be ignored.

9.6 Transmit Section/Line/Path Overhead Insertion Signals (36)

Pin Name	Type	Pin No.	Function
TTOHCLK4 TTOHCLK3 TTOHCLK2 TTOHCLK1	Output	B18 A19 A17 A18	The **transmit transport overhead clock** (TTOHCLK) signal provides timing for the transmit section and line overhead insertion during SONET/SDH operation. In STS-192c/STM-64c mode, TTOHCLK1 is a nominal 82.94 MHz clock generated by gapping a 103.68 MHz clock. TTOHCLK2-4 are not defined. In quad STS-48c/STM-16c mode, TTOHCLK1-4 is a nominal 82.94 MHz clock generated by gapping a 103.68 MHz clock. When the TTOH interface is configured to insert either the section DCC bytes (D1-D3) or the line DCC bytes (D4-D12), the frequency of TTOHCLK1-4 will be either 192KHz or 576KHz respectively. TTOHCLK[N] is not used for 10 Gigabit Ethernet LAN PHY operation and should be ignored.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 10:32 PM

Pin Name	Type	Pin No.	Function
TTOHFP4 TTOHFP3 TTOHFP2 TTOHFP1	Output	B17 F17 B16 F16	The **transmit transport overhead frame pulse** (TTOHFP) signal provides timing for the transmit section and line overhead insertion during SONET/SDH operation. In STS-192c/STM-64c mode, TTOHFP1 is used to indicate the most significant bit (MSB) on TTOH1-4. TTOHFP2-4 are not defined. In quad STS-48c/STM-16c mode, TTOHFP1-4 is used to indicate the most significant bit (MSB) on TTOH1-4. TTOHFP[N] is set high when the MSB of the: First A1 byte should be present on TTOH[N]. TTOHFP[N] is updated on the rising edge of TTOHCLK[N]. TTOHFP[N] is not used for 10 Gigabit Ethernet LAN PHY operation and should be ignored.
TTOH4 TTOH3 TTOH2 TTOH1	Input	A16 E16 D15 E15	The **transmit transport overhead** (TTOH) signal contains the transport overhead bytes (A1, A2, J0, Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, Z1/S1, Z2/M1, and E2) to be transmitted and the error masks to be applied on B1, B2, H1 and H2 during SONET/SDH operation. Please refer to the Functional Description section for details. TTOH[N] is sampled on the rising edge of TTOHCLK[N] when inserting all of the overhead bytes or DCC bytes. TTOH[N] is not used for 10 Gigabit Ethernet LAN PHY operation and must be strapped low.
TTOHEN4 TTOHEN3 TTOHEN2 TTOHEN1	Input	E14 F15 C14 A15	The **transmit transport overhead insert enable** (TTOHEN) signal controls the insertion of the transmit transport overhead data which is inserted in the outgoing stream during SONET/SDH operation. When TTOHEN[N] is high during the most significant bit of a TOH byte on TTOH[N], the sampled TOH byte is inserted into the corresponding transport overhead byte position (A1, A2, J0, Z0, E1, F1, D1-D3, H3, K1, K2, D4-D12, Z1/S1, Z2/M1, and E2 bytes). When TTOHEN[N] is low during the most significant bit of a TOH byte on TTOH[N], that sampled byte is ignored and the default value is inserted into the transmit transport overhead byte position. When TTOHEN[N] is high during the most significant bit of the H1, H2, B1 or B2 TOH byte positions on TTOH[N], the sampled TOH byte is logically XORed with the associated byte to force bit errors on the transmit byte. A logic low bit in the TTOH[N] byte allows the incoming bit to go through while a bit set to logic high will toggle the outgoing bit. A low level on TTOHEN[N] during the MSB of the TOH byte disables the error forcing for the entire byte. TTOHEN[N] is sampled on the rising edge of TTOHCLK[N]. TTOHEN[N] is not used for 10 Gigabit Ethernet LAN PHY operation and must be strapped low.

Downloaded by Content Team of Partminer Inc or Vendor. Thursday, 2008-06-05 12:32 PM

Pin Name	Type	Pin No.	Function
TPOHCLK4 TPOHCLK3 TPOHCLK2 TPOHCLK1	Output	C13 D14 C12 D13	The **transmit path overhead clock** (TPOHCLK) signal provides timing for the transmit path overhead insertion during SONET/SDH operation. TPOHCLK[N] is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. When the TPOH interface is configured to insert either the section DCC bytes (D1-D3) or the line DCC bytes (D4-D12), the frequency of TPOHCLK1-4 will be either 192KHz or 576KHz respectively. TPOHCLK[N] is not used for 10 Gigabit Ethernet LAN PHY operation and should be ignored.
TPOHFP4 TPOHFP3 TPOHFP2 TPOHFP1	Output	A12 B13 E13 F14	The **transmit path overhead frame pulse** (TPOHFP) signal provides timing for the transmit path overhead insertion during SONET/SDH operation. TPOHFP[N] is used to indicate the most significant bit (MSB) on TPOH[N]. TPOHFP[N] is set high when the MSB of the first J1 byte should be present on TPOH[N]. For STS-192c/STM-64c, only TPOHFP1 is valid. TPOHFP[N] is updated on the falling edge of TPOHCLK[N] when inserting all of the overhead bytes. TPOHFP[N] is updated on the rising edge of TPOHCLK[N] when inserting the DCC bytes. TTOHFP[N] is not used for 10 Gigabit Ethernet LAN PHY operation and should be ignored.
TPOH4 TPOH3 TPOH2 TPOH1	Input	B11 D12 A11 B12	The **transmit path overhead** (TPOH) signal contains the path overhead bytes (J1, C2, G1, F2, Z3, Z4, and Z5) to be transmitted in a STS-48c (STM-16c) or STS-192c (STM-64c) SONET (SDH) path overhead and the error masks to be applied on B3 and H4. A path overhead byte is accepted for transmission when the external source indicates a valid byte (TPOHEN[N] set high) and the S/UNI 9953 indicates ready (TPOHRDY[N] set high). The S/UNI 9953 will ignore the byte on TPOH[N] when TPOHEN[N] is set low. The TPOHRDY[N] is set low to indicate the S/UNI 9953 is not ready, and the byte must be re-presented at the next opportunity. For STS-192c/STM-64c, only TPOH1 is valid. TPOH[N] is sampled on the rising edge of TPOHCLK[N]. TPOH[N] is not used for 10 Gigabit Ethernet LAN PHY operation and must be strapped low.

Downloaded by Content Team of Partminer Inc on Wednesday, 01 February 2006 16:55:32 EST

Pin Name	Type	Pin No.	Function
TPOHRDY4 TPOHRDY3 TPOHRDY2 TPOHRDY1	Output	E10 F11 C8 D9	The **transmit path overhead insert ready** (TPOHRDY) signal indicates if the S/UNI 9953 is ready to accept the byte currently on TPOH[N] during SONET/SDH operation. TPOHRDY[N] is set high during the most significant bit of a POH byte to indicate readiness to accept the byte on the TPOH[N] input. This byte will be accepted if TPOHEN[N] is also set high. If TPOHEN[N] is set low, the byte is invalid and is ignored. TPOHRDY[N] is set low to indicate that the S/UNI 9953 is unable to accept the byte on TPOH[N], and expects the byte to be re-presented at the next opportunity. For STS-192c/STM-64c, only TPOHRDY1 is valid. TPOHRDY[N] is updated on the falling edge of TPOHCLK[N]. TPOHRDY[N] is not used for 10 Gigabit Ethernet LAN PHY operation and should be ignored.
TPOHEN4 TPOHEN3 TPOHEN2 TPOHEN1	Input	A10 C11 A9 B10	The **transmit path overhead insert enable** (TPOHEN) signal controls the insertion of the transmit path overhead data which is inserted in the transmit stream during SONET/SDH operation. TPOHEN[N] shall be set high during the most significant bit of a POH byte to indicate valid data on the TPOH[N] input. This byte will be accepted for transmission if TPOHRDY[N] is also set high. If TPOHRDY[N] is set low, the byte is rejected and must be re-presented at the next opportunity. Accepted bytes sampled on TPOH[N] are inserted into the corresponding path overhead byte positions (for the J1, C2, G1, F2, Z3, Z4, and Z5 bytes). The byte on TPOH[N] is ignored when TPOHEN[N] is set low during the most significant bit position. When the byte at the B3 or H4 byte position on TPOH[N] is accepted, it is used as an error mask to modify the corresponding transmit B3 or H4 path overhead byte, respectively. The accepted error mask is XORed with the corresponding B3 or H4 byte before it is transmitted. For STS-192c/STM-64c, only TPOHEN1 is valid. TPOHEN[N] is sampled on the rising edge of the TPOHCLK[N]. TPOHEN[N] is not used for 10 Gigabit Ethernet LAN PHY operation and must be strapped low.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 January, 2015 (GMT-0600)

9.7 Side-band Flow Control Signals (2)

Pin Name	Type	Pin No.	Function
PAUSE	Input	V33	The **pause** (PAUSE) signal is controlled by the system level interface to request the internal transmit MAC to send pause frames through the line side to initiate flow control. Pause frames are sent at a prescribed interval programmed in the pause timer register. PAUSE is active high and is treated as an asynchronous input. PAUSE must be strapped to low if unused.
PAUSED	Output	W34	The **paused** (PAUSED) signal is controlled by the receive MAC to indicate that a PAUSE frame has been received and the transmit MAC is currently in a flow control state. PAUSED is active high and is asynchronous.

9.8 System Side POS-PHY Level 4 Signals (82)

Pin Name	Type	Pin No.	Function
REFSEL[1] REFSEL[0]	Schmidt TTL Input (integral pull-up)	T30 U29	The POS-PHY Level 4 **Reference** Clock **Select** (REFSEL[1:0]) input selects the source and frequency of the reference clock used to generate the internal clocks for the PL4 Bus interface logic. When REFSEL[0] is low the reference clock is derived from TDCLK+/- (slave mode). When REFSEL[0] is high the reference clock is derived from REFCLK+/- (master mode). When REFSEL[1] is low in slave mode the TRAIN_DIS and ODAT_DIS bits in the PL4IO Configuration register are initially cleared and TDCLK+/- must be valid before de-asserting RSTB. When REFSEL[1] is high in slave mode the TRAIN_DIS and ODAT_DIS bits in the PL4IO Configuration register are initially set and TDCLK+/- must be valid before these bits are cleared. When REFSEL[1] is low in master mode the selected internal PL4 reference clock frequency is ½ the PL4 data rate. When REFSEL[1] is high in master mode the selected reference clock frequency is ¼ the PL4 data rate. REFSEL should only be switched while RSTB is asserted.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 06:52:02 PM

Pin Name	Type	Pin No.	Function
REFCLK+ REFCLK-	PECL Input	F31 E32	The POS-PHY Level 4 **Reference Clock** (REFCLK+/-) is a 155.5 MHz to 350 MHz, 50% duty cycle clock reference that is used to generate RDCLK+/- and provide phase references for TDAT[15:0]+/- de-skewing. REFCLK is ignored when REFSEL[0] is logic 0 (slave mode) and used when REFSEL[0] is logic 1 (master mode). The actual frequency of REFCLK+/- in master mode must be between 311.0 MHz and 350 MHz when REFSEL[1] is low and is frequency locked to TDCLK+/-. The actual frequency of REFCLK+/- in master mode must be between 155.5 MHz and 175 MHz when REFSEL[1] is high and is frequency locked to TDCLK+/- divided by 2. REFCLK+/- should be stable before de-asserting RSTB if REFSEL[0] is a logic 1 (master mode). If the POS-PHY Level 4 Reference clock is used, it is recommended to use REFCLK as a differential PECL input. The REFCLK+/- PECL inputs are not internally terminated by the PM5390.
RDCLK+ RDCLK-	Analog LVDS Output	K34 L33	The POS-PHY **differential receive clock** (RDCLK+/-) is a 1*REFCLK, 2*REFCLK or TDCLK MHz, 50% duty cycle source synchronous clock. When operating in PL4 master mode, RDCLK+/- is a 1x or 2x multiplied version of the REFCLK+/- inputs. When operating in PL4 slave mode, RDCLK+/- is a loop-timed version of TDCLK+/-. RDCLK+/- is provided to downstream devices to clock in RDAT[15:0]+/- and RCTL+/-. The rising and falling edges of RDCLK+/- is used to update RDAT[15:0]+/- and RCTL+/-.

Downloaded by Content Team of Partminer Inc on Wednesday, 14 February 2007 16:53:37

Pin Name	Type	Pin No.	Function
RDAT[15]+ RDAT[15]- RDAT[14]+ RDAT[14]- RDAT[13]+ RDAT[13- RDAT[12]+ RDAT[12] RDAT[11]+ RDAT[11]- RDAT[10]+ RDAT[10]- RDAT[9]+ RDAT[9]- RDAT[8]+ RDAT[8]- RDAT[7]+ RDAT[7]- RDAT[6]+ RDAT[6]- RDAT[5]+ RDAT[5]- RDAT[4]+ RDAT[4]- RDAT[3]+ RDAT[3]- RDAT[2]+ RDAT[2]- RDAT[1]+ RDAT[1]- RDAT[0]+ RDAT[0]-	Analog LVDS Output	P32 R31 M34 N33 R30 T29 N32 P31 L34 M33 P30 R29 M32 N31 N30 P29 L32 M31 J34 K33 K30 L29 H32 J31 F34 G33 J30 K29 G32 H31 E34 F33	The POS-PHY **differential receive data** (RDAT[15:0]+/-) bus carries the Ethernet frames, POS packet octets and ATM cells that are read from the receive FIFOs and the in-band control words which describes the stream. In-band control words are identified using the RCTL+/- output. Please refer to the Operations section for a description of the POS-PHY Level 4 protocol and the bus data structures (cells and frames). RDAT[15:0]+/- is updated on both edges of RDCLK+/-.
RCTL+ RCTL-	Analog LVDS Output	R34 T33	The POS-PHY **differential receive control** (RCTL+/-) signals identify control words on the RDAT[15:0]+/- bus. When RCTL+/- is high, a control word is on the RDAT[15:0]+/- bus. If RCTL+/- is low, a payload word (either cell or frame) is on the RDAT[15:0]+/- bus. RCTL+/- is updated on both edges of RDCLK+/-.
RSCLK	Schmidt TTL Input	T34	The POS-PHY **receive status clock** (RSCLK) is a RDCLK/4 MHz, 40/60% duty cycle clock. RSCLK is used to clock the receive status circuitry. Conforming to the PL4 Bus specification requirement that implementation of the FIFO status channel in the receive interface is optional, RSCLK may be tied to a logic 0 if the Receive Status bus is not used. Refer to the Operation section for additional details (subsection Operation with PL4 Receive FIFO status unimplemented). The rising edge of RSCLK is used to sample RSTAT[1:0].

Downloaded by Content Team at Chartmine Inc on Wednesday, 07 February, 2007 08:

Pin Name	Type	Pin No.	Function
RSTAT[1] RSTAT[0]	Input	U34 V34	The POS-PHY **receive status** (RSTAT[1:0]) bus is used to indicate the status of the downstream device's FIFOs. When the S/UNI 9953 is configured for OC-192 operation, only one FIFO status can be indicated; when configured for quad OC-48 operation or channelized OC-192 operation, up to four FIFO status can be indicated. For each FIFO, a Satisfied, Hungry or Starving condition can be indicated. In addition, a special two-bit code is used for framing and alignment. Please refer to the Operation section for the status definitions and the status protocol. Conforming to the PL4 Bus specification requirement that implementation of the FIFO status channel in the receive interface is optional, RSTAT may be tied to a logic 0 if the Receive Status bus is not used. Refer to the Operation section for additional details (subsection Operation with PL4 Receive FIFO status unimplemented). RSTAT[1:0] is sampled on the rising edge of RSCLK.
TDCLK+ TDCLK-	Analog LVDS Input	B24 A25	The POS-PHY **differential transmit clock** (TDCLK+/-) is a 311 MHz to 350 MHz, 50% duty cycle source synchronous clock. TDCLK+/- is used to clock the transmit POS-PHY circuitry. When configured for PL4 master mode, TDCLK+/- must be frequency locked to REFCLK+/- divided by 1 or 2. The rising and falling edges of TDCLK+/- is used to sample TDAT[15:0]+/- and TCTL+/-.

Downloaded by Content Team of Partminer Inc on Tuesday, 20 Feb 2007 10:10:39

Pin Name	Type	Pin No.	Function
TDAT[15]+ TDAT[15]- TDAT[14]+ TDAT[14]- TDAT[13]+ TDAT[13]- TDAT[12]+ TDAT[12]- TDAT[11]+ TDAT[11]- TDAT[10]+ TDAT[10]- TDAT[9]+ TDAT[9]- TDAT[8]+ TDAT[8]- TDAT[7]+ TDAT[7]- TDAT[6]+ TDAT[6]- TDAT[5]+ TDAT[5]- TDAT[4]+ TDAT[4]- TDAT[3]+ TDAT[3]- TDAT[2]+ TDAT[2]- TDAT[1]+ TDAT[1]- TDAT[0]+ TDAT[0]-	Analog LVDS Input	F21 E22 D21 C22 D22 C23 B22 A23 B23 A24 D23 C24 B25 A26 D26 C27 B28 A29 F25 E26 D27 C28 B29 A30 B30 A31 D28 C29 D29 C30 B31 A32	The POS-PHY **differential transmit data** (TDAT[15:0]+/-) bus carries the Ethernet Frames, POS packet octets and ATM cells that are written into the transmit FIFOs and the in-band control words which describes the stream. In-band control words are identified using the TCTL+/- input. Please refer to the Operation section for a description of the POS-PHY Level 4 protocol and the bus data structures (cells and frames). TDAT[15:0]+/- is sampled on both edges of TDCLK+/-.
TCTL+ TCTL-	Analog LVDS Input	F20 E21	The POS-PHY **differential transmit control** (TCTL+/-) signals identify control words on the TDAT[15:0]+/- bus. When TCTL+/- is high, a control word is on the TDAT[15:0]+/- bus. If TCTL+/- is low, a payload word (either cell or frame) is on the TDAT[15:0]+/- bus. TCTL+/- is sampled on both edges of TDCLK+/-.
TSCLK	Output	D20	The POS-PHY **transmit status clock** (TSCLK) is a TDCLK/4 MHz, 40/60% duty cycle source synchronous clock. TSCLK is used to clock the transmit status circuitry. The rising edge of TSCLK is used to update TSTAT[1:0].
TSTAT[1] TSTAT[0]	Output	B19 A20	The POS-PHY **transmit status** (TSTAT[1:0]) bus is used to indicate the status of the S/UNI 9953's FIFOs. When the S/UNI 9953 is configured for OC-192 operation, only one FIFO status is indicated; when configured for quad OC-48 operation or channelized OC-192 operation, up to four FIFO status are indicated. For each FIFO, a Satisfied, Hungry or Starving condition can be indicated. Please refer to the Operation section for the status definitions and the status protocol. TSTAT[1:0] is updated on the rising edge of TSCLK.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 08:57:00

9.9 APS Serial Data Interface (67 Signals)

Pin Name	Type	Pin No.	Function
IAPS4[3]+ IAPS4[3]- IAPS4[2]+ IAPS4[2]- IAPS4[1]+ IAPS4[1]- IAPS4[0]+ IAPS4[0]- IAPS3[3]+ IAPS3[3]- IAPS3[2]+ IAPS3[2]- IAPS3[1]+ IAPS3[1]- IAPS3[0]+ IAPS3[0]- IAPS2[3]+ IAPS2[3]- IAPS2[2]+ IAPS2[2]- IAPS2[1]+ IAPS2[1]- IAPS2[0]+ IAPS2[0]- IAPS1[3]+ IAPS1[3]- IAPS1[2]+ IAPS1[2]- IAPS1[1]+ IAPS1[1]- IAPS1[0]+ IAPS1[0]-	Analog LVDS Input	AL8 AM7 AG11 AH10 AN7 AP6 AJ10 AK9 AL12 AM11 AN12 AP11 AN13 AP12 AL13 AM12 AN17 AP16 AN16 AP15 AM17 AM18 AP17 AP18 AL20 AM21 AN22 AP23 AN23 AP24 AJ18 AK19	The differential **input APS** (IAPS+/-) serial data links carries quad OC-48 or single OC-192 SONET (SDH) frame data from a mate in bit serial format. Each differential pair carries a constituent OC-12 of the data stream. For quad OC-48 mode, each IAPS[N] group carries a full STS-48c (STM-16c) stream. For OC-192 mode, IAPS[1] carries STS-48 #1 (STM-16 #1) while IAPS[4] carries STS-48 #4 (STM-16 #4). Data on IAPS+/- is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is transmitted first and the bit 'j' is transmitted last. When the S/UNI 9953 is configured to working mode, the IAPS+/- signals carry the receive data from the protect mate. When in protect mode, the IAPS+/- signals carry the transmit data from the working mate. IAPS+/- members are frequency locked but not phase locked to other members in a group. IAPS+/- are nominally 777.6 Mbit/s data streams. IAPS buses are not used for 10 Gigabit Ethernet LAN PHY operation. Please refer to the Operation section for description in handling unused differential LVDS inputs.
IAPSFP	Input	AG18	The **input APS frame pulse** signal (IAPSFP) provides system timing of the APS input serial interface during SONET/SDH operation. IAPSFP is set high once every 9720 TCLK cycles, or multiple thereof, to indicate that the J0 frame boundary 8B/10B character has been delivered on the differential LVDS bus (IAPS[4:1][3:0]+/-). IAPSFP is treated as an asynchronous signal and is edge detected. IAPSFP is not used for 10 Gigabit Ethernet LAN PHY operation and must be strapped low.

Downloaded by Content Team of Partminer Inc on Wednesday, February 20, 2008 12:12:12 PM

Pin Name	Type	Pin No.	Function
IAPSFPCLK	Schmidt TTL Input	AH17	The **input APS frame pulse clock** (IAPSFPCLK) provides a jitter-free reference clock for the 777.6 MHz Clock Synthesis Unit of the APS Port during SONET/SDH operation. IAPSFPCLK is expected to cycle at a 77.76 MHz rate, and must be synchronous with respect to TXCLK[N]+/- to ensure that IAPSFPCLK is an exact divide-by-8 in frequency, compared to TXCLK[N]+/-. IAPSFPCLK is not used for 10 Gigabit Ethernet LAN PHY operation and must be strapped low.
OAPS4[3]+ OAPS4[3]- OAPS4[2]+ OAPS4[2]- OAPS4[1]+ OAPS4[1]- OAPS4[0]+ OAPS4[0]- OAPS3[3]+ OAPS3[3]- OAPS3[2]+ OAPS3[2]- OAPS3[1]+ OAPS3[1]- OAPS3[0]+ OAPS3[0]- OAPS2[3]+ OAPS2[3]- OAPS2[2]+ OAPS2[2]- OAPS2[1]+ OAPS2[1]- OAPS2[0]+ OAPS2[0]- OAPS1[3]+ OAPS1[3]- OAPS1[2]+ OAPS1[2]- OAPS1[1]+ OAPS1[1]- OAPS1[0]+ OAPS1[0]-	Analog LVDS Output	AP4 AN5 AM6 AL7 AK8 AJ9 AP5 AN6 AK10 AJ11 AM8 AL9 AP10 AN11 AP9 AN10 AM13 AL14 AK13 AJ14 AK14 AJ15 AM14 AL15 AP19 AN18 AK15 AJ16 AK16 AJ17 AP20 AN19	The differential **output APS** (OAPS+/-) serial data links carries quad OC-48 or single OC-192 SONET (SDH) frame data from a mate in bit serial format. Each differential pair carries a constituent OC-12 of the data stream. For quad OC-48 mode, each OAPS[N] group carries a full STS-48c (STM-16c) stream. For OC-192 mode, OAPS[1] carries STS-48 #1 (STM-16 #1) while OAPS[4] carries STS-48 #4 (STM-16 #4). Data on OAPS+/- is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is transmitted first and the bit 'j' is transmitted last. When the S/UNI 9953 is configured to working mode, the OAPS+/- signals carry the transmit data to the protect mate. When in protect mode, the OAPS+/- signals carry the receive data to the working mate. OAPS+/- members are frequency locked but not phase locked to other members in a group. OAPS+/- are nominally 777.6 Mbit/s data streams. OAPS buses are not used for 10 Gigabit Ethernet LAN PHY operation and should be ignored.

Downloaded by Content Team of Partminer.com on 06/01/2021 06:52:42

Pin Name	Type	Pin No.	Function
OAPSFP	Output	AH19	The **output APS frame pulse** signal (OAPSFP) provides an optional system timing reference for the APS output serial interface during SONET/SDH operation. OAPSFP is set high once every 9720 TCLK cycles, or multiple thereof, to indicate the approximate location of the J0 frame boundary 8B/10B character on the differential LVDS buses (OAPS+/-). This signal may used to visually determine the setting for the internal delay counters. It must not be used as a source of the IAPSFP input frame pulse. OAPSFP is updated on the rising edge of IAPSFPCLK. OAPSFP is not used for 10 Gigabit Ethernet LAN PHY operation and should be ignored.

9.10 Microprocessor Interface Signals (37)

Pin Name	Type	Pin No.	Function
CSB	Input	AA31	The active low **chip select** (CSB) signal is low during S/UNI 9953 register accesses. If CSB is not required (i.e. register accesses controlled using the RDB and WRB signals only), CSB must be connected to an inverted version of the RSTB input.
RDB	Input	Y30	The active low **read enable** (RDB) signal is low during a S/UNI 9953 read access. The S/UNI 9953 drives the D[15:0] bus with the contents of the addressed register while RDB and CSB are low.
WRB	Input	W29	The active low **write strobe** (WRB) signal is low during a S/UNI 9953 register write access. The D[15:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low.
D[15] D[14] D[13] D[12] D[11] D[10] D[9] D[8] D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O	AB31 AC32 AD33 AE34 AF34 AE33 AD32 AC31 AB30 AA29 AD29 AE30 AF31 AG32 AH33 AJ34	The bi-directional **data bus** (D[15:0]) is used during S/UNI 9953 read and write accesses.
A[14]/TRS	Input	AJ33	The **test register select** (TRS) signal selects between normal and test mode register accesses. TRS is high during test mode register accesses, and is low during normal mode register accesses. TRS may be tied low.

Downloaded by Content Team of Partminer Inc on Monday, 04 February 2019 08:47:15

Pin Name	Type	Pin No.	Function
A[13] A[12] A[11] A[10] A[9] A[8] A[7] A[6] A[5] A[4] A[3] A[2] A[1] A[0]	Input	AH32 AG31 AF30 AE29 AF29 AG30 AH31 AJ32 AK33 AL34 AM34 AL33 AK32 AJ31	The **address** (A[13:0]) bus selects specific registers during S/UNI 9953 register accesses.
RSTB	Schmidt TTL Input (integral pull-up)	AC33	The active low **reset** (RSTB) signal provides an asynchronous S/UNI 9953 reset. RSTB is a Schmidt triggered input with an integral pull-up resistor.
ALE	Input (integral pull-up)	AB32	The **address latch enable** (ALE) is an active-high signal and latches the address bus A[13:0] when low. When ALE is high, the internal address latches are transparent. It allows the S/UNI 9953 to interface to a multiplexed address/data bus. The ALE input has an integral pull up resistor.
INTB	Open Drain Output	AD34	The active low **interrupt** (INTB) is set low when a S/UNI 9953 enabled interrupt source is active. The S/UNI 9953 may be enabled to report many alarms or events via interrupts. INTB is tri-stated when the interrupt is acknowledged via the appropriate register access. INTB is an open drain output.

9.11 Reserved Signals (24)

Pin Name	Type	Pin No.	Function
DTRB	Schmidt TTL Input (integral pull-down)	F18	DTRB is reserved for PMC test purposes. DTRB has an integral pull-down resistor and must be strapped to low for normal operation.
VCLK1 VCLK2 VCLK3 VCLK4 VCLK5 VCLK6 VCLK7	Input (integral pull-down)	D6 C5 B4 A3 U32 V32 AB33	VCLK[N] is reserved for PMC test purposes. VCLK[N] has an integral pull-down resistor and must be strapped to low for normal operation.
BTEST	Input (integral pull-down)	AE27	Reserved. BTEST has an integral pull-down resistor and must be strapped to low for normal operation.

Downloaded by Circuit Team Electronic on Wednesday, 07 February, 2007 06:59:32 PM

Pin Name	Type	Pin No.	Function
NC1 NC2 NC3 NC4 NC5 NC6 NC7 NC8 NC9 NC10 NC11 NC12 NC13	Input (integral pull-up)	C21 F19 E20 E19 G10 H11 U33 AH18 AA32 AA30 Y29 U28 V28	Reserved. NC1-13 have integral pull-up resistors and must not be connected.
DTEST1 DTEST0	Input (integral pull-up)	AF28 AK34	Reserved. DTEST[1:0] have integral pull-up resistors and must be strapped to low for normal operation.

9.12 JTAG Test Access Port (TAP) Signals (5)

Pin Name	Type	Pin No.	Function
TCK	Schmidt TTL Input	Y34	The **test clock** (TCK) signal provides timing for test operations that can be carried out using the IEEE P1149.1 test access port.
TMS	Input (integral pull-up)	V29	The **test mode select** (TMS) signal controls the test operations that can be carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull up resistor.
TDI	Input (integral pull-up)	Y31	When the S/UNI 9953 is configured for JTAG operation, the **test data input** (TDI) signal carries test data into the S/UNI 9953 via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull up resistor.
TDO	Tristate Output	W33	The **test data output** (TDO) signal carries test data out of the S/UNI 9953 via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output that is inactive except when scanning of data is in progress.
TRSTB	Schmidt TTL Input (integral pull-up)	W30	The active low **test reset** (TRSTB) signal provides an asynchronous S/UNI 9953 test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmidt triggered input with an integral pull up resistor. In the event that TRSTB is not used, it must be connected to RSTB.

9.13 Analog Miscellaneous Signals (19)

Pin Name	Type	Pin No.	Function
CPREF_CLK	Schmidt TTL Input (integral pull-down)	AC34	The **Charge-Pump Reference Clock** (CPREF_CLK) provides a 60 to 81 MHz clock with a 40/60 % or better duty cycle distortion as required by the analog circuitry for proper operation. A stable CPREF_CLK input is expected when RSTB is de-asserted. A nominally 77.76 MHz 50% duty cycle clock input is recommended. Note that CPREF_CLK is not a part of the boundary scan chain.

Downloaded by Conteltech@gmail.com at Gainetinc on Wednesday, 07 February, 2007 06:59:32 PM

Pin Name	Type	Pin No.	Function
OIF_ATB0 OIF_ATB1	Analog I/O	W5 V6	The **OIFS analog test bus** (OIF_ATB[1:0]) is provided for production testing only. These pins must be tied to analog ground (VSS) during normal operation. OIF_ATB0 and OIF_ATB1 are the test pins for the line side analog circuits.
APS_ATB0 APS_ATB1	Analog I/O	AC7 AB8	The **APS analog test bus** (APS_ATB[1:0]) is provided for production testing only. These pins must be tied to analog ground (VSS) during normal operation. APS_ATB0 and APS_ATB1 are the test pins for the input/output APS port analog circuits.
APS_OSC APS_OSCB	Analog LVDS Output	AE7 AD8	These pins are reserved for PMC test purposes and must not be connected during normal operation.
PL4_ATB0 PL4_ATB1 PL4_ATB2 PL4_ATB3 PL4_ATB4 PL4_ATB5	Analog I/O	E33 H29 D34 G30 G31 F32	The **PL4 analog test bus** (PL4_ATB[5:0]) is provided for production testing only. These pins must be tied to analog ground (VSS) during normal operation. PL4_ATB0, PL4_ATB1, PL4_ATB2, PL4_ATB3, PL4_ATB4 and PL4_ATB5 are the test pins for the PL4 Interface analog circuits.
OIF_RES OIF_RESK	Analog I/O	M7 N8	**OIFS Reference Resistor Connection.** An off-chip 3.16kΩ ±1% resistor is connected between the positive resistor reference pin OIF_RES and a Kelvin ground contact OIF_RESK. An on-chip negative feedback path will force an internal 0.80V reference voltage onto OIF_RES, therefore forcing 252μA of current to flow through the resistor. This current is used by the line side transmit LVDS pads.
APS_RES APS_RESK	Analog I/O	AJ8 AP3	**APS Reference Resistor Connection.** An off-chip 3.16kΩ ±1% resistor is connected between the positive resistor reference pin APS_RES and a Kelvin ground contact APS_RESK. An on-chip negative feedback path will force an internal 0.80V reference voltage onto APS_RES, therefore forcing 252μA of current to flow through the resistor. This current is used by the output APS port transmit LVDS pads.
PL4_RES PL4_RESK	Analog I/O	J29 H30	**PL4 Reference Resistor Connection.** An off-chip 3.16kΩ ±1% resistor is connected between the positive resistor reference pin PL4_RES and a Kelvin ground contact PL4_RESK. An on-chip negative feedback path will force an internal 0.80V reference voltage onto PL4_RES, therefore forcing 252μA of current to flow through the resistor. This current is used by the PL4 Interface Ingress LVDS pads.

9.14 Analog Power and Ground (15)

Pin Name	Type	Pin No.	Function
OIF_AVDH	Analog Power	L7	The **OIFS analog power** (OIF_AVDH) pin for the Line Side analog circuits. The OIF_AVDH pin should be connected through passive filtering networks to a well-decoupled +3.3V analog power supply. Please see the Operation section for detailed information.

Downloaded by Chipset Team of Chiptrainer Inc on Friday, 07 February 2014, 10:53:32 EST

Pin Name	Type	Pin No.	Function
APS_QAVD	Analog Power	AH5	The **APS quiet power** (APS_QAVD) pin for the APS port analog circuits. APS_QAVD should be connected to well-decoupled analog +3.3V supply. Please see the Operation section for detailed information
APS_AVDH1 APS_AVDH2	Analog Power	AL6 AN4	The **APS analog power** (APS_AVDH[2:1]) pins for the APS port analog circuits. The APS_AVDH[2:1] pins should be connected through passive filtering networks to a well-decoupled +3.3V analog power supply. Please see the Operation section for detailed information.
APS_AVDL1 APS_AVDL2 APS_AVDL3 APS_AVDL4	Analog Power	AM5 AK7 AH9 AG10	The **APS analog power** (APS_AVDL[4:1]) pins for the APS port analog circuits. The APS_AVDL[4:1] pins should be connected through passive filtering networks to a well-decoupled +1.8V analog power supply. Please see the Operation section for detailed information.
PL4_QAVD	Analog Power	D33	The **PL4 quiet power** (PL4_QAVD) pin for the PL4 Interface analog circuits. PL4_QAVD should be connected to well-decoupled analog +3.3V supply. Please see the Operation section for detailed information
PL4_AVDH1 PL4_AVDH2 PL4_AVDH3	Analog Power	F27 E27 J28	The **PL4 analog power** (PL4_AVDH[3:1]) pins for the PL4 Interface analog circuits. The PL4_AVDH[3:1] pins should be connected through passive filtering networks to a well-decoupled +3.3V analog power supply. Please see the Operation section for detailed information.
PL4_AVDL1 PL4_AVDL2 PL4_AVDL3	Analog Power	E28 K27 C34	The **PL4 analog power** (PL4_AVDL[3:1]) pins for the PL4 Interface analog circuits. The PL4_AVDL[3:1] pins should be connected through passive filtering networks to a well-decoupled +1.8V analog power supply. Please see the Operation section for detailed information.

9.15 Digital Power and Ground

Pin Name	Type	Pin No.	Function
VDDO	Digital I/O Power	A8, A27, AA7, AA8, AA9, AA10 AA25, AA26 AA27, AA28 AB9, AB17 AB18, AB26 AC5, AC6 AC16, AC17 AC18, AC19 AC29, AC30 AD15, AD16 AD19, AD20 AD27, AE3 AE4, AE14 AE15, AE16 AE19, AE20 AE21, AE28 AE31, AE32 AF16, AF19 AG1, AG2 AG14, AG17 AG21, AG22	The **digital I/O power** (VDDO) pins should be connected to a well-decoupled +3.3V digital power supply.

Downloaded by Content Team of Partminer Inc. on 2004-03-31

Pin Name	Type	Pin No.	Function
		AG33, AG34 AH14, AH16 AH21, AH23 AJ12, AJ23 AK12, AK23 AL3, AL4 AL10, AL25 AL31, AL32 AM4, AM10 AM25, AM31 AN8, AN27 AP8, AP27	
VDDO	Digital I/O Power	B8, B27 C4, C10 C25, C31 D3, D4 D10, D25 D31, D32 E3, E12 E23, F12 F23, G14 G16, G21 G24, H1 H2, H14 H17, H21 H23, H33 H34, J13 J14, J16 J19, J21 J22, K3 K4, K14 K15, K16 K19, K20 K21, K28 K31, K32 L15, L16 L19, L20 L27, M5 M6, M16 M17, M18 M19, M29 M30, N9 N17,N18 N26, P7 P8, P9 P10, P25 P26, P27 P28, R10 R11, R24 R25, T9	The **digital I/O power** (VDDO) pins should be connected to a well-decoupled +3.3V digital power supply.
VDDO	Digital I/O Power	T10, T11 T12, T23 T24, T25 T26, T28 U12, U13 U22, U23 U27, V8	The **digital I/O power** (VDDO) pins should be connected to a well-decoupled +3.3V digital power supply.

Downloaded by Content Team of Partminer.com on Wednesday, 07 February 2007 06:59:32 PM

Pin Name	Type	Pin No.	Function
		V12, V13 V22, V23 W7, W9 W10, W11 W12, W23 W24, W25 W26, Y10 Y11, Y24 Y25	
VDDI	Digital Core Power	A2, A14 A21, A33 AA1, AA2 AA11, AA12 AA13, AA14 AA16, AA17 AA18, AA19 AA21, AA22 AA23, AA24 AA33, AA34 AB10, AB11 AB14, AB15 AB16, AB19 AB20, AB21 AB24, AB25 AB27, AC9 AC10, AC11 AC12, AC14 AC15, AC20 AC21, AC23 AC24, AC25 AC26, AC28 AD9, AD12 AD13, AD14 AD21, AD22 AD23, AD26 AE9, AE10 AE12, AE13 AE22, AE23 AE25, AE26 AF10, AF25 AG7, AG8 AG13, AG24 AG27, AG28 AH8, AH12	The **digital core power** (VDDI) pins should be connected to a well-decoupled +1.8V digital power supply.
VDDI	Digital Core Power	AH25, AH27 AJ5, AJ6 AJ29, AJ30 AK6, AK29 AL16, AL19 AM16, AM19 AN1, AN2 AN14, AN21 AN33, AN34 AP2, AP14 AP21, AP33 B1, B2 B14, B21	The **digital core power** (VDDI) pins should be connected to a well-decoupled +1.8V digital power supply.

Downloaded by Content Team of Partmi... Wednesday, 07 February, 2007 06:59:32 PM

Pin Name	Type	Pin No.	Function
		B33, B34 C1, C16 C19, D16 D19, E6 E29, F5 F6, F29 F30, G5 G8, G19 G26, G27 H7, H8 H18, H25 H27, H28 J7, J10 J11, J12 J23, J24 J25, K9 K10, K12 K13, K22 K23, K25 K26, L9 L12, L13 L14, L21 L22, L23	
VDDI	Digital Core Power	L26, M9 M10, M11 M12, M14 M15, M20 M21, M23 M24, M25 M26, M28 N10, N11 N14, N15 N16, N19 N20, N21 N24, N25 N27, P1 P2, P11 P12, P13 P14, P16 P17, P18 P19, P21 P22, P23 P24, P33 P34, R12 R13, R16 R19, R22 R23, T3 T4, T7 T13, T14 T15, T16 T19, T20 T21, T22 T31, T32 U8, U14 U21, V14 V21, V27 W3, W4 W13, W14	The **digital core power** (VDDI) pins should be connected to a well-decoupled +1.8V digital power supply.

Downloaded by Content Team of Partminer on Wednesday, 07 February, 2007 06:59:32 PM

Pin Name	Type	Pin No.	Function
VDDI	Digital Core Power	W15, W16 W19, W20 W21, W22 W28, W31 W32, Y12 Y13, Y16 Y19, Y22 Y23	The **digital core power** (VDDI) pins should be connected to a well-decoupled +1.8V digital power supply.
VSS	Digital Analog Ground	A7, A13 A22, A28 AA15, AA20 AB1, AB6 AB7, AB12 AB13, AB22 AB23, AB28 AB29, AB34 AC8, AC13 AC22, AC27 AD4, AD5 AD7, AD10 AD11, AD17 AD18, AD24 AD25, AD28 AD30, AD31 AE8, AE11 AE17, AE18 AE24, AF2 AF3, AF7 AF8, AF9 AF11, AF12 AF13, AF14 AF15, AF17 AF18, AF20 AF21, AF22 AF23, AF24 AF26, AF27 AF32, AF33 AG6, AG9 AG12, AG15 AG16, AG19 AG20, AG23 AG25, AG26 AH1, AH6 AH7, AH11	The **digital/analog ground** (VSS) pins should be connected to the common digital/analog ground of the device power supply.
VSS	Digital Analog Ground	AH13, AH15 AH20, AH22 AH24, AH26 AH28, AH29 AH34, AJ7 AJ13, AJ22 AJ28, AK4 AK5, AK11 AK17, AK18 AK24, AK30 AK31, AL5 AL11, AL17 AL18, AL24	The **digital/analog ground** (VSS) pins should be connected to the common digital/analog ground of the device power supply.

Downloaded by Content Team of Partmine.com on Wednesday, 07 February, 2018 06:59:32 PM

Pin Name	Type	Pin No.	Function
		AL30, AM2 AM3, AM9 AM15, AM20 AM26, AM32 AM33, AN3 AN9, AN15 AN20, AN26 AN32, AP7 AP13, AP22 AP28, B3 B9, B15 B20, B26 B32, C2 C3, C9 C15, C17 C18, C20 C26, C32 C33, D2 D5, D11 D17, D18 D24, D30 E4, E5, E11, E17	
VSS	Digital Analog Ground	E18, E24 E25, E30 E31, F4 F7, F13 F22, F24 F26, F28 G1, G6 G7, G11 G12, G13 G15, G17 G18, G20 G22, G23 G25, G28 G29, G34 H6, H9 H12, H13 H15, H16 H19, H20 H22, H24 H26, J2 J3, J8 J9, J15 J17, J18 J20, J26 J27, J32 J33, K8 K11, K17 K18, K24 L4, L5 L10, L11 L17, L18 L24, L25 L28, L30 L31, M8 M13, M22	The **digital/analog ground** (VSS) pins should be connected to the common digital/analog ground of the device power supply.

Downloaded by Content Team of Partminer.com on Wednesday, 07 February, 2007 06:59:32 PM

Pin Name	Type	Pin No.	Function
		M27, N1	
VSS	Digital Analog Ground	N6, N7 N12, N13 N22, N23 N28, N29 N34, P15 P20, R2 R3, R7 R8, R9 R14, R15 R17, R18 R20, R21 R26, R27 R28, R32 R33, T8 T17, T18 T27, U4 U5, U7 U9, U10 U11, U15 U16, U17 U18, U19 U20, U24 U25, U26 U30, U31 V4, V5 V7, V9 V10, V11 V15, V16 V17, V18 V19, V20 V24, V25 V26, V30 V31, W8 W17, W18 W27, Y2 Y3, Y7	The **digital/analog ground** (VSS) pins should be connected to the common digital/analog ground of the device power supply.
VSS	Digital Analog Ground	Y8, Y9 Y14, Y15 Y17, Y18 Y20, Y21 Y26, Y27 Y28, Y32 Y33	The **digital/analog ground** (VSS) pins should be connected to the common digital/analog ground of the device power supply.

Notes on Pin Description

1. All S/UNI 9953 inputs and bi-directionals present minimum capacitive loading and operate at CMOS/TTL logic levels except the inputs marked as Analog, PECL or LVDS.
2. All S/UNI 9953 digital outputs and bi-directionals have 8 mA drive capability.
3. The S/UNI 9953 digital outputs are 3.3V LVTTL.
4. Inputs REFSEL[1:0], NC[13:1], DTEST[1:0], ALE, RSTB, TMS, TDI and TRSTB have internal pull-up resistors.
5. Inputs PHASE_ERR[4:1], SYNC_ERR[4:1], VCLK[7:1], QUAD2488, LAN, DTRB, BTEST and CPREF_CLK have internal pull-down resistors.

Downloaded by Conteq, Team of Solutions on Wednesday, 07 February, 2007 06:59:35 PM

6. The LVDS inputs and outputs should be terminated in a passive network and interface at LVDS levels as described in the Operation section.
7. It is mandatory that every digital/analog ground pin (VSS) be connected to the printed circuit board ground plane to ensure reliable device operation.
8. It is mandatory that every digital power pin (VDDO, VDDI) be connected to the printed circuit board power planes to ensure reliable device operation.
9. All analog power pins can be sensitive to noise. They must be isolated from the digital power pins. Care must be taken to correctly decouple these pins. Please refer to the Operation section.
10. Due to ESD protection structures in the pads it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions it is possible to damage these ESD protection devices or trigger latch up. Please adhere to the recommended power supply sequencing as described in the Power Information section of this document.
11. Do not exceed 100 mA of current on any pin during the power-up or power-down sequence. Refer to the Power Sequencing description in the Operation section.
12. Before any input activity occurs, ensure that the device power supplies are within their nominal voltage range.
13. Hold the device in the reset condition until the device power supplies are within their nominal voltage range.
14. ~~Ensure that all digital power is applied simultaneously, and applied before or simultaneously with the analog power. Refer to the Power Sequencing description in the Operation section.~~

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2018 @ 5:59:32 PM

10 Functional Description

The S/UNI 9953 implements SONET/SDH processing and payload termination for four OC-48 streams or one OC-192 stream when configured for SONET/SDH operation. The S/UNI 9953 processes 10320 Mbit/s Ethernet data stream when configured to support the IEEE 802.3ae 10 Gigabit Ethernet LAN PHY operation.

During SONET/SDH operation which includes IEEE 802.3ae 10 Gigabit Ethernet WAN PHY mode, the S/UNI 9953 processes the section, line and path overhead of the SONET/SDH data stream(s) using sixteen STM-4 processing slices (#1 to #16) in each of the receive and transmit directions. An STM-4 slice is responsible for processing a constituent STS-12/STM-4 or equivalent data stream in an OC-192 or an OC-48 stream. In the receive direction, a receive STM-4 processing slice consists of the RRMP (transport), RHPP (path), SVCA (AU aligner) and R8TD (APS input) blocks. In the transmit direction, a transmit STM-4 processing slice consists of the TRMP (transport), THPP (path) and T8TE (APS output) blocks.

The STM-4 slices are configured as one master and fifteen slaves when processing an STS-192c/STM-64c data stream in unchannelized OC-192 operation mode. When processing four STS-48c/STM-16c (#1 to #4) data streams in channelized OC-192 operation mode, the sixteen STM-4 processing slices are organized into four STM-16 processing groups (#1 to #4) each consisting of one master and three slave STM-4 slices. Similarly in quad OC-48 mode of operation, the sixteen STM-4 processing slices are organized into four STM-16 processing groups (#1 to #4) as described above to process the four corresponding STS-48c/STM-16c (#1 to #4) data streams. The master STM-4 slice is responsible for coordinating the operation of the slave STM-4 slices as well as handling the transport and path alarms (including SPE/VC payload extraction) for the concatenated SONET/SDH (STM-64c/STM-16c) data stream being processed.

The processing of the four STS-48c/STM-16c data streams are assisted by other SONET/SDH blocks organized as part of the four STM-16 processing groups. On the receive side, each receive STM-16 processing group has the additional SBER (signal degrade/failure), section RTTP (section trace), path RTTP (path trace) and SARC (receive alarms) blocks. On the transmit side, each transmit STM-16 processing group has the additional section TTTP (section trace), path TTTP (path trace) and SIRP (remote defect insertion) blocks. When processing a single STS-192c/STM-64c data stream, only the additional blocks in the STM-16 processing group #1 will be active (master) and those in groups #2 to #4 are inactive (slaves).

Downloaded by Content Team Under Copyright of PMC-Sierra, Inc. Not for Redistribution 07 Feb 2007 06:59:... PM

During SONET/SDH operation which includes IEEE 802.3ae 10 Gigabit Ethernet WAN PHY mode, the STS-192c/STM-64c or quad STS-48c/STM-16c data streams from the S/UNI 9953 receive line interface are de-multiplexed into its constituent STS-12/STM-4 data streams by the SRLI block for the receive STM-4 processing slices. After section, line and path processing, the constituent STS-12/STM-4 data streams are multiplexed (re-combined) into the STS-192c/STM-64c or quad STS-48c/STM-16c data streams by the RXSTSI blocks for ATM/POS/10 Gigabit Ethernet WAN PHY payload processing. For the STS-192c/STM-64c data stream, ATM/POS payload processing is performed by the RCFP-9953 block and 10 Gigabit Ethernet payload is processed by the R64B66B/RXXG blocks. For the four STS-48c/STM-16c (#1 to #4) data streams, ATM/POS payload processing is performed by the four corresponding RCFP (#1 to #4) blocks. The processed payload is synchronized and transferred to the system-side receive PL4 interface (PL4IO, PL4ODP) via the IFLX Ingress FIFO and the PL4MOS scheduler blocks.

During IEEE 802.3ae 10 Gigabit Ethernet LAN PHY operation, the 10320 Mbit/s Ethernet data stream from the S/UNI 9953 receive line interface is provided directly to the R64B66B/RXXG blocks. Similarly, the processed Ethernet payload is synchronized and transferred to the system-side receive PL4 interface (PL4IO, PL4ODP) via the IFLX Ingress FIFO and the PL4MOS scheduler blocks. All SONET/SDH related blocks in the receive data-path (including output APS ports) are disabled when the S/UNI 9953 is operating in 10 Gigabit Ethernet LAN PHY mode.

Transmit ATM/POS/10 Gigabit Ethernet WAN/LAN PHY payload is transferred from the system-side transmit PL4 interface (PL4IO, PL4IDU) and synchronized to the line-side timing domain via the EFLX Egress FIFO block. STS-192c/STM-64c ATM/POS payload is processed by the TCFP-9953 block and the 10 Gigabit Ethernet WAN/LAN PHY payload is processed by the T64B66B/TXXG blocks. For the four STS-48c/STM-16c (#1 to #4) data streams, ATM/POS payload processing is performed by the four corresponding TCFP (#1 to #4) blocks.

For SONET/SDH operation which includes IEEE 802.3ae 10 Gigabit Ethernet WAN PHY mode, the transmit STS-192c/STM-64c or quad STS-48c/STM-16c payload streams are de-multiplexed into its constituent STS-12/STM-4 data streams by the TXSTSI blocks for the transmit STM-4 processing slices. After section, line and path processing, the constituent STS-12/STM-4 data streams are multiplexed (re-combined) into the STS-192c/STM-64c or quad STS-48c/STM-16c data streams by the STLI block for transmission on the S/UNI 9953 transmit line interface.

For IEEE 802.3ae 10 Gigabit Ethernet LAN PHY operation, the transmit 10320 Mbit/s Ethernet payload stream is provided directly to the S/UNI 9953 transmit line interface for transmission. All SONET/SDH related blocks in the transmit data-path (including input APS ports) are disabled when the S/UNI 9953 is operating in 10 Gigabit Ethernet LAN PHY mode.

10.1 SONET/SDH Receive Line Interface (SRLI)

The SONET/SDH receive line interface (SRLI) allows the S/UNI 9953 to directly interface with external SERDES devices. The interface can operate in either OC-192 or quad OC-48 modes. All the I/O on this interface are Low Voltage Differential Swing (LVDS).

Downloaded by Content Solution of Parts Unit Services Tuesday, 27 February 2007 (GMT-0600)

In OC-192 mode, the interface receives 16-bit data at 622 Mbps together with a 622 MHz clock. This interface is compliant to the OIF99.102.5 SFI-4 interface.

In OC-48 mode, the interface receives 4 independent channels, each receiving 4-bit data at 622 Mbps together with a 622 MHz clock. This interface is compliant to the OIF99.102.5 SFI-4 interface.

The SRLI block performs byte and frame alignment on the incoming 9953 Mbit/s or four 2488 Mbit/s data streams based on the SONET/SDH A1/A2 framing pattern.

While out-of-frame, the SRLI monitors the receive data stream for an occurrence of the A1/A2 framing pattern. The SRLI adjusts its byte and frame alignment when three consecutive A1 bytes followed by three consecutive A2 bytes occur in the data stream. The SRLI informs the RRMP framer block when the framing pattern has been detected to reinitialize to the new transport frame alignment. While in-frame, the SRLI maintains the same byte and frame alignment until the RRMP declares out-of-frame or an external synchronization error has been detected by the clock and data recovery device.

10.2 Receive Regenerator and Multiplexer Processor (RRMP)

The Receive Regenerator and Multiplexer Processor (RRMP) block extracts and processes the transport overhead of the received data stream.

The RRMP frames to the data stream by operating with an upstream pattern detector (SRLI) that searches for occurrences of the A1/A2 framing pattern. Once the SRLI has found an A1/A2 framing pattern, the RRMP monitors for the next occurrence of the framing pattern 125µs later. Two framing pattern algorithms are provided to improve performance in the presence of bit errors. In algorithm 1, the RRMP declares frame alignment (removes OOF defect) when the 12 A1 and the 12 A2 bytes are seen error-free in the first STS-12 (STM-4) of the STS-48c (STM-16-16c) streams or the STS-192c (STM-64-64c) stream. In algorithm 2, the RRMP declares frame alignment (removes OOF defect) when only the last A1 byte and the first four bits of the first A2 byte are seen error-free in the first STS-12 (STM-4) of the STS-48c (STM-16c) or STS-192c (STM-64c). Once in-frame, the RRMP monitors the framing pattern and declares OOF when one or more bit errors in the framing pattern are detected for four consecutive frames. Again, depending upon the algorithm either 24 framing bytes or 12 framing bits are examined for bit errors in the framing pattern.

The performance of these framing algorithms in the presence of bit errors and random data is robust. When looking for frame alignment, the performance of each algorithm is dominated by the alignment algorithm used in the SRLI which always examines 3 A1 and 3 A2 framing bytes. The probability of falsely framing to random data is less than 0.00001% for either algorithm. Once in-frame alignment, the RRMP continuously monitors the framing pattern. When the incoming stream contains a 10^{-3} BER, the first algorithm provides a 99.75% probability that the mean time between OOF occurrences is 1.3 seconds and the second algorithm provides a 99.75% probability that the mean time between OOF occurrences is seven minutes.

Downloaded by [illegible] Terms of Service. Tuesday, 07 February 2007 06:59:[illegible] PM

The RRMP also detects loss-of-frame (LOF) defect and loss-of-signal (LOS) defect. LOF is declared when an out-of-frame (OOF) condition exists for a total period of 3 ms. LOF is removed when an in-frame condition exists for a continuous period of 3 ms. LOS is declared when a continuous period of 20 µs without transitions on the received data stream is detected. LOS is removed when two consecutive framing patterns are found (based on algorithm 1 or algorithm 2) and during the intervening time (one frame) there are no continuous periods of 20 µs without transitions on the received data stream.

The RRMP calculates the section BIP-8 error detection code on the scrambled data of the complete frame. The section BIP-8 code is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 code is compared with the BIP-8 code extracted from the B1 byte of STS-1 (STM-0) #1 of the following frame after de-scrambling. Any difference indicates a section BIP-8 error. The master RRMP accumulates section BIP-8 errors in a microprocessor readable 16-bit saturating counter (up to 1 second accumulation time). Optionally, block section BIP-8 errors can be accumulated.

The RRMP optionally de-scrambles the received data stream.

The RRMP calculates the line BIP-8 error detection codes on the de-scrambled line overhead and synchronous payload envelope bytes of the constituent STS-1 (STM-0). The line BIP-8 code is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 codes are compared with the BIP-8 codes extracted from the B2 byte of the constituent STS-1 (STM-0) of the following frame after de-scrambling. Any difference indicates a line BIP-8 error. The RRMP accumulates line BIP-8 errors in a microprocessor readable 24-bit saturating counter (up to 1 second accumulation time). Optionally, block BIP-24 errors can be accumulated.

The RRMP extracts the line remote error indication (REI-L) errors from the M1 byte of STS-1 (STM-0) #3 and accumulates them in a microprocessor readable 24-bit saturating counter (up to 1 second accumulation time). Optionally, block line REI errors can be accumulated.

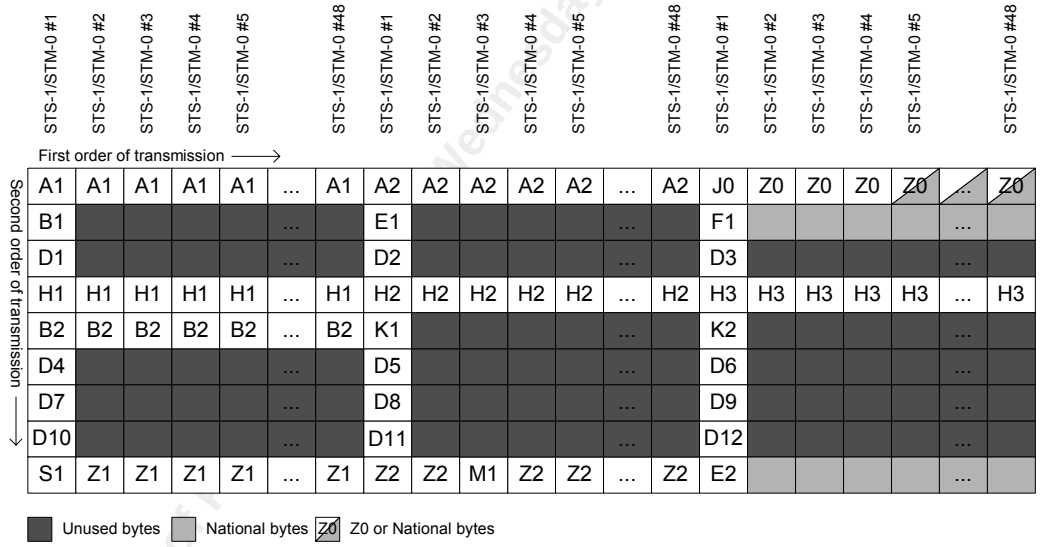
The RRMP extracts and filters the K1/K2 APS bytes for three frames. The filtered K1/K2 APS bytes are accessible through microprocessor readable registers. The RRMP also monitors the unfiltered K1/K2 APS bytes to detect APS byte failure (APSBF-L) defect, line alarm indication signal (AIS-L) defect and line remote defect indication (RDI-L) defect. APS byte failure is declared when twelve consecutive frames have been received where no three consecutive frames contain identical K1 bytes. The APS byte failure is removed upon detection of three consecutive frames containing identical K1 bytes. The detection of invalid APS codes is done in software by polling the K1/K2 APS register. Line AIS is declared when the bit pattern 111 is observed in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. Line AIS is removed when any pattern other than 111 is observed for three or five consecutive frames. Line RDI is declared when the bit pattern 110 is observed in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. Line RDI is removed when any pattern other than 110 is observed for three or five consecutive frames.

The RRMP extracts and filters the synchronization status message (SSM) for eight frames. The filtered SSM is accessible through microprocessor readable registers. The RRMP optionally inserts line alarm indication signal (AIS-L).

Downloaded by Orbit Intelligence on Wednesday, 07 February 2007 06:57:22 AM

The RRMP extracts and serially outputs all the transport overhead (TOH) bytes on the RTOH port. The TOH bytes are output in the same order that they are received (A1, A2, J0/Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, S1/Z1, Z2/M1/Z2 and E2). Figure 10, Figure 11 and Figure 12 show the transport overhead bytes on RTOH1-4 for the case where the S/UNI 9953 is processing quad OC-48/STS-48/STM-16 and OC-192/STS-192/STM-64 data streams. Transport overhead columns are labeled accord to the order of arrival of the corresponding STS-1/STM-0 time-slots. These figures do not show the bit multiplexing structure used to serially output the transport overhead on the RTOH ports. Each processing RRMP extracts and outputs serially an STS-12/STM-4 worth of transport overhead. The transport overhead serial streams of four RRMPs are multiplexed to generate an STS-48/STM-16 transport overhead serial stream for the corresponding RTOH port. Each overhead byte of each STS-12 slice is extracted to the RTOH port one bit at a time, multiplexed across four STS-12 processing slices. Refer to the Functional Timing section for a detailed description of the multiplexing structure. RTOHCLK is the generated output clock used to provide timing for the RTOH port. RTOHCLK is a nominal 82.94 MHz clock generated by gapping a 103.68 MHz clock. Sampling RTOHFP high with the rising edge of RTOHCLK identifies the MSB of the first A1 byte.

Figure 10 STS-48 (STM-16) on RTOH 1-4



Downloaded by Content Team of Pantechsolutions, Wednesday, 07 February 2017 6:08:22 PM

Figure 11 STS-192 (STM-64) on RTOH1

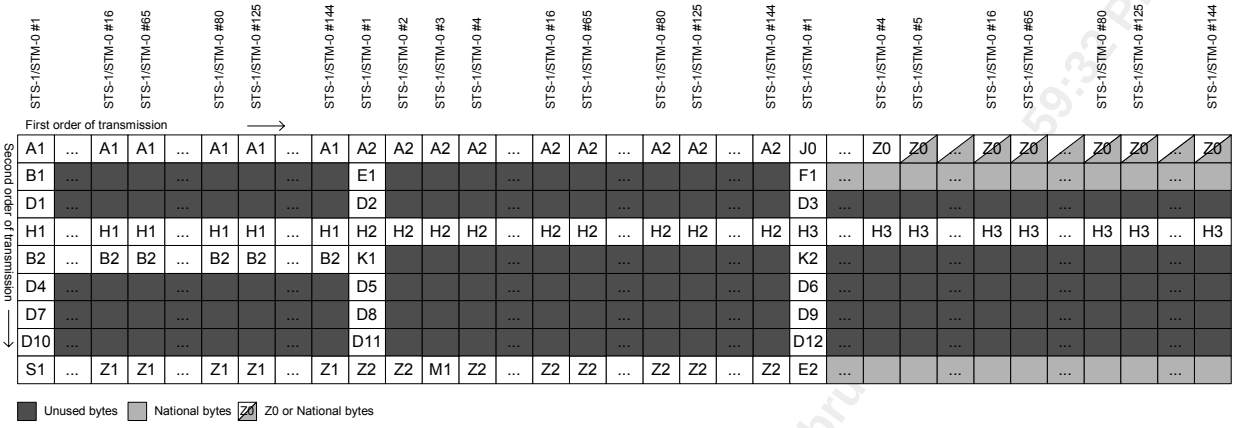
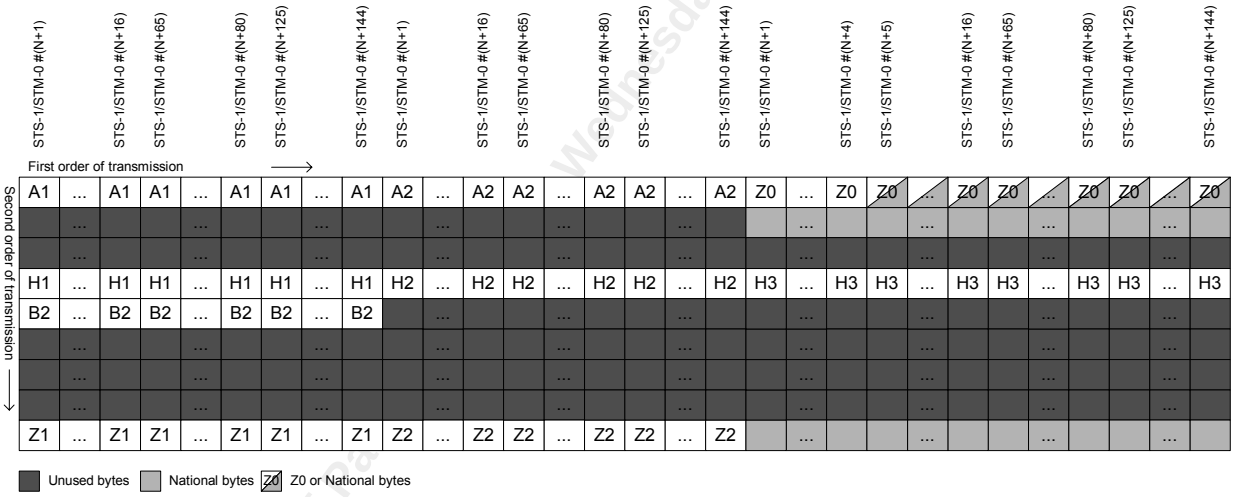


Figure 12 STS-192 (STM-64) on RTOH2-4



N=16 for RTOH2, N=32 for RTOH3, N=48 for RTOH4

A maskable interrupt is activated to indicate any change in the status of out-of-frame (OOF), loss-of-frame (LOF), loss-of-signal (LOS), line remote defect indication (RDI-L), line alarm indication signal (AIS-L), synchronization status message (COSSM), APS bytes (COAPS) and APS byte failure (APSBF) or any errors in section BIP-8, line BIP-8 and line remote error indication (REI-L).

The RRMP block provides de-scrambled data and frame alignment indication signals for use by the RHPP.

Downloaded by [illegible] Wednesday, 07 Febru [illegible] 59:32 PM

10.3 Section/Path Receive Trail Trace Processor (RTTP)

The Section/Path Receive Trail Trace Processor (RTTP) block monitors the SONET/SDH Section/Path Trail trace messages of the receive data stream for trace identifier unstable (TIU) defect and trace identifier mismatch (TIM) defect. Three Trail trace algorithms are defined. It is mandatory to select one of the algorithms for the RTTP to monitor the received message.

The first algorithm is Telcordia compliant. The algorithm detects trace identifier mismatch (TIM) defect on a 16 or 64 byte Trail trace message. A TIM defect is declared when none of the last 20 messages matches the expected message. A TIM defect is removed when 16 of the last 20 messages match the expected message. The expected trail trace message is a static message written in the expected page of the RTTP by an external microprocessor. Optionally, the expected message is matched when the trail trace message is all zeros.

The second algorithm is ITU compliant. The algorithm detects trace identifier unstable (TIU) defect and trace identifier mismatch (TIM) defect on a 16 or 64 byte trail trace message. The current trail trace message is stored in the captured page of the RTTP. If the length of the message is 16 bytes, the RTTP synchronizes on the MSB of the message. The byte with the MSB set high is placed in the first location of the captured page. If the length of the message is 64 bytes, the RTTP synchronizes on the CR/LF (CR = 0Dh, LF = 0Ah) characters of the message. The following byte is placed in the first location of the captured page.

A persistent trail trace message is declared when an identical message is received for 3 or 5 consecutive multi-frames (16 or 64 frames). A persistent message becomes the accepted message. The accepted message is stored in the accepted page of the RTTP. A TIU defect is declared when one or more erroneous bytes are detected in a total of 8 messages without any persistent message in between. A TIU defect is removed when a persistent message is received.

A TIM defect is declared when the accepted message does not match the expected message. A TIM defect is removed when the accepted message matches the expected message. The expected message is a static message written in the expected page of the RTTP by an external microprocessor. Optionally, the algorithm declares a match trail trace message when the accepted message is all zeros.

The third algorithm is not Telcordia/ITU compliant. The algorithm detects trace identifier unstable (TIU) on a single continuous trail trace byte. A TIU defect is declared when one or more erroneous bytes are detected in three consecutive 16 byte windows. The first window starts on the first erroneous byte. A TIU defect is removed when an identical byte is received for 48 consecutive frames. A maskable interrupt is activated to indicate any change in the status of trace identifier unstable (TIU) and trace identifier mismatch (TIM).

10.4 SONET/SDH Bit Error Rate Monitor (SBER)

The SBER block provides two independent bit error rate monitoring circuits (BERM block). It is used to monitor the Multiplexer Section BIP (B2) with one BERM block dedicated to monitor the Signal Degrade (SD) alarm and the other BERM block dedicated to monitor the Signal Fail (SF) alarm. These alarms can then be used to control system level features such as Automatic Protection Switching (APS).

Downloaded by Components Direct at Parts-Direct.com (Components Direct Inc.) on February 20, 2007 6:39:10 PM

The BERM block utilizes a sliding window based algorithm. This algorithm provides better performance for detection, clearing and false detection than a simple jumping window (resetable counter being polled at a regular interval) algorithm.

10.5 Receive High Order Path Processor (RHPP)

The Receive High Order Path Processor (RHPP) provides pointer interpretation, extraction of path overhead, extraction of the synchronous payload envelope (virtual container), and path level alarm and performance monitoring on the data stream from the RRMP block. Processed data is provided to the SONET (SDH) Virtual Container Aligner (SVCA) block.

10.5.1 Pointer Interpreter

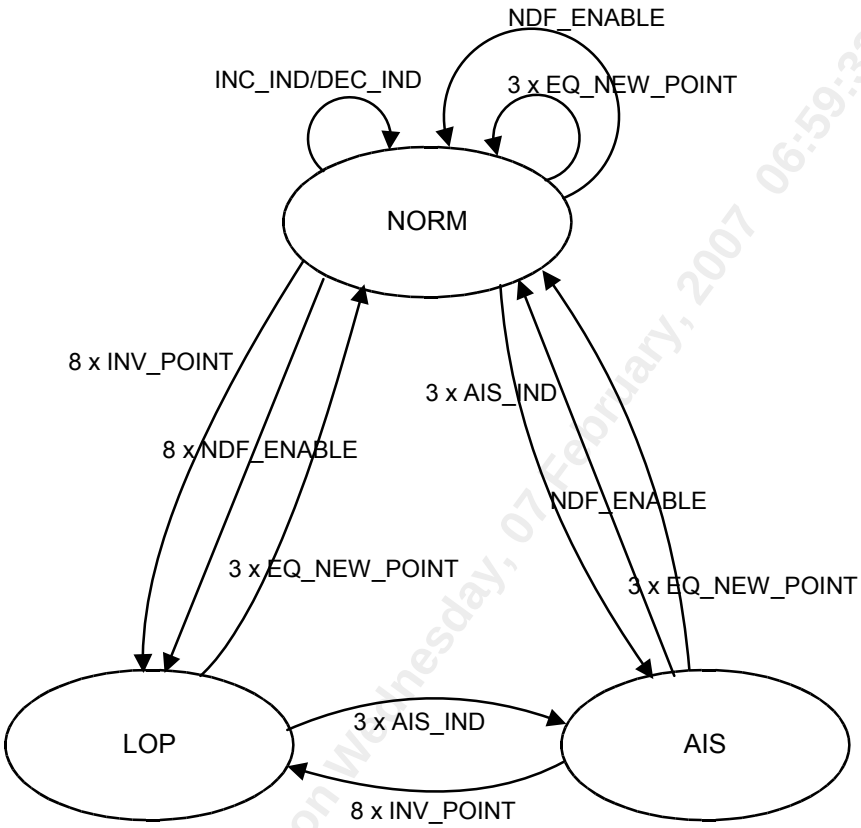
The pointer interpreter extracts and validates the H1 and H2 bytes in order to identify the location of the path overhead byte (J1) and the synchronous payload envelop bytes (SPE) of the constituent STS-48c (VC-16-16c) payloads or the STS-192c (VC-64-64c) payload. The pointer interpreter is a time multiplexed finite state machine that can process the STS-48c (AU-16-16c) pointers or a single STS-192c (AU-64-64c) pointer. Within the pointer interpretation algorithm three states are defined as shown below:

- NORM_state (NORM)
- AIS_state (AIS)
- LOP_state (LOP)

The transition between states will be consecutive events (indications), e.g., three consecutive AIS indications to go from the NORM_state to the AIS_state. The kind and number of consecutive indications activating a transition is chosen such that the behavior is stable and insensitive to low BER. The only transition on a single event is the one from the AIS_state to the NORM_state after receiving a NDF enabled with a valid pointer value. It should be noted that, since the algorithm only contains transitions based on consecutive indications, this implies that, for example, non-consecutively received invalid indications do not activate the transitions to the LOP_state.

Downloaded by Content Team of Partminer Wednesday, 01 February, 2006, 59:32 PM

Figure 13 Pointer Interpretation State Diagram



The following events (indications) are defined:

NORM_POINT:	disabled NDF + ss + offset value equal to active offset.
NDF_ENABLE:	enabled NDF + ss + offset value in range of 0 to 782.
AIS_IND:	H1 = FFh + H2 = FFh.
INC_IND:	disabled NDF + ss + majority of I bits inverted + no majority of D bits inverted + previous NDF_ENABLE, INC_IND or DEC_IND more than 3 frames ago.
DEC_IND:	disabled NDF + ss + majority of D bits inverted + no majority of I bits inverted + previous NDF_ENABLE, INC_IND or DEC_IND more than 3 frames ago.
INV_POINT:	not any of the above (i.e.: not NORM_POINT, not NDF_ENABLE, not AIS_IND, not INC_IND and not DEC_IND).

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

NEW_POINT: disabled NDF + ss + offset value in range of 0 to 782 but not equal to active offset.

Notes

1. Active offset is defined as the accepted current phase of the SPE (VC) in the NORM_state and is undefined in the other states.
2. Enabled NDF is defined as the following bit patterns:
   1001, 0001, 1101, 1011 and 1000.
3. Disabled NDF is defined as the following bit patterns:
   0110, 1110, 0010, 0100 and 0111.
4. The remaining six NDF bit patterns (0000, 0011, 0101, 1010, 1100, 1111) result in an INV_POINT indication.
5. ss bits are unspecified in SONET and have bit pattern 10 in SDH.
6. The use of ss bits in definition of indications may be optionally disabled.
7. The requirement for previous NDF_ENABLE, INC_IND or DEC_IND be more than 3 frames ago may be optionally disabled.
8. NEW_POINT is also an INV_POINT.
9. The requirement for the pointer to be within the range of 0 to 782 in 8 X NDF_ENABLE may be optionally disabled.
10. LOP is not declared if all the following conditions exist:
    - the received pointer is out of range (>782),
    - the received pointer is static,
    - the received pointer can be interpreted, according to majority voting on the I and D bits, as a positive or negative justification indication, after making the requested justification, the received pointer continues to be interpretable as a pointer justification.
    - When the received pointer returns to an in-range value, the S/UNI 9953 will interpret it correctly.
11. LOP will exit at the third frame of a three frame sequence consisting of one frame with NDF enabled followed by two frames with NDF disabled, if all three pointers have the same legal value.

The transitions indicated in the state diagram are defined as follows:

INC_IND/DEC_IND: offset adjustment (increment or decrement indication)

3 x EQ_NEW_POINT: three consecutive equal NEW_POINT indications

NDF_ENABLE: single NDF_ENABLE indication

3 x AIS_IND: three consecutive AIS indications

8 x INV_POINT: eight consecutive INV_POINT indications

8 x NDF_ENABLE eight consecutive NDF_ENABLE indications

Notes

1. The transitions from NORM_state to NORM_state do not represent state changes but imply offset changes.
2. 3 x EQ_NEW_POINT takes precedence over other events and may optionally reset the INV_POINT count.

Downloaded by Content Team on Partnumber.com on Wednesday, 07 February, 2007 06:59:52 PM

3. All three offset values received in 3 x EQ_NEW_POINT must be identical.
4. "Consecutive event counters" are reset to zero on a change of state (except the INV_POINT counter).
5. "Consecutive event counters" are reset to zero on a change of state except for consecutive NDF count.

LOP is declared on entry to the LOP_state after eight consecutive invalid pointers or eight consecutive NDF enabled indications

PAIS is declared on entry to the AIS_state after three consecutive AIS indications

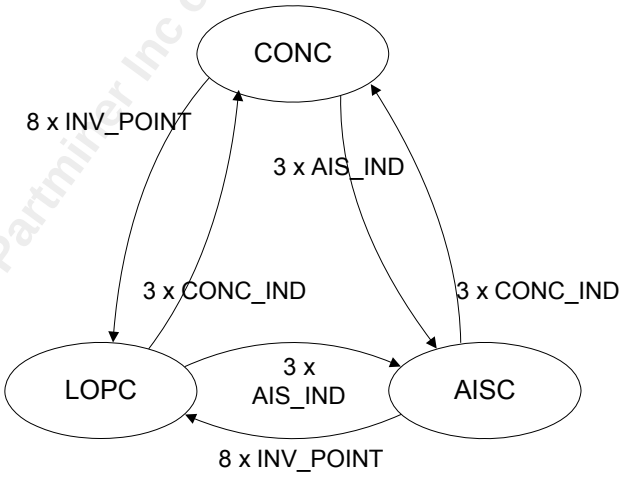
10.5.2 Concatenation Pointer Interpreter State Machine

The concatenation pointer interpreter extracts and validates the H1 and H2 concatenation bytes. Within the pointer interpretation algorithm three states are defined as shown below.

- CONC_state (CONC)
- AISC_state (AISC)
- LOPC_state (LOPC)

The transitions between the states will be consecutive events (indications), e.g. three consecutive AIS indications to go from the CONC_state to the AISC_state. The kind and number of consecutive indications activating a transition is chosen such that the behavior is stable and insensitive to low BER.

Figure 14 Concatenation Pointer Interpretation State Diagram



The following events (indications) are defined:

CONC_IND: enabled NDF + dd + “1111111111”

AIS_IND: H1 = FFh + H2 = FFh

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 06:59:32 PM

INV_POINT: not any of the above (i.e.: not CONC_IND and not AIS_IND)

Notes

1. Enabled NDF is defined as the following bit patterns: 1001, 0001, 1101, 1011 and 1000.
2. The remaining eleven NDF bit patterns (0000, 0010, 0011, 0100, 0101, 0110, 0111, 1010, 1100, 1110, 1111) result in an INV_POINT indication.
3. dd bits are unspecified in SONET/SDH.

The transitions indicated in the state diagram are defined as follows:

3 X CONC_IND: three consecutive CONC indications

3 x AIS_IND: three consecutive AIS indications

8 x INV_POINT: eight consecutive INV_POINT indications

Note

1. Consecutive event counters" are reset to zero on a change of state.

LOPC is declared on entry to the LOPC_state after eight consecutive pointers with values other than concatenation indications

PAISC is declared on entry to the AISC_state after three consecutive AIS indications

10.5.3 Error Monitoring

The RHPP calculates the path BIP-8 error detection codes on the SONET (SDH) payloads. The path BIP-8 code is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 codes are compared with the BIP-8 codes extracted from the B3 byte of the STS (VC) payload of the following frame. Any differences indicate a path BIP-8 error. The RHPP accumulates path BIP-8 errors in a microprocessor readable 16 bits saturating counter (up to 1 second accumulation time). Optionally, block BIP-8 errors can be accumulated.

The RHPP extracts the path remote error indication (REI-P) errors from bits 1, 2, 3 and 4 of the path status byte (G1) and accumulates them in a microprocessor readable 16 bits saturating counter (up to 1 second accumulation time). Optionally, block REI errors can be accumulated.

The RHPP monitors the path signal label byte (C2) payload to validate change in the accepted path signal label (APSL). The same PSL byte must be received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register) before being considered accepted.

The RHPP also monitors the path signal label byte (C2) to detect path payload label unstable (PLU-P) defect. A PSL unstable counter is incremented every time the received PSL differs from the previously accepted PSL (an erroneous PSL will cause the counter to be increment twice, once when the erroneous PSL is received and once when the error free PSL is received). The PSL unstable counter is reset when the same PSL value is received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). PLU-P is declared when the PSL unstable counter reaches five. PLU-P is removed when the PSL unstable counter is reset.

Downloaded by Document Center of Pakistan Telecom on Wednesday, 01 February, 2007 06:59:32 PM

The RHPP also monitors the path signal label byte (C2) to detect path payload label mismatch (PLM-P) defect. PLM-P is declared when the accepted PSL does not match the expected PSL according to Table 2. PLM-P is removed when the accepted PSL match the expected PSL according to Table 2. The accepted PSL is the same PSL value received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). The expected PSL is a programmable PSL value.

The RHPP also monitors the path signal label byte (C2) to detect path unequipped (UNEQ-P) defect. UNEQ-P is declared when the accepted PSL is 00H and the expected PSL is not 00H. UNEQ-P is removed when the accepted PSL is not 00H or when the accepted PSL is 00H and the expected PSL is 00H. The accepted PSL is the same PSL value received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). The expected PSL is a register programmable PSL value.

The RHPP also monitors the path signal label byte (C2) to detect path payload defect indication (PDI-P) defect. PDI-P is declared when the accepted PSL is a PDI defect that matches the expected PDI defect. The PDI-P defect is removed when the accepted PSL is not a PDI defect or when the accepted PSL is a PDI defect that does not match the expected PDI defect. The accepted PSL is the same PSL value received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). Table 3 gives the expected PDI defect based on the programmable PDI and PDI range register values.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 16:59:82 EST

Table 2 PLM-P, UNEQ-P, and PDI-P Defects Declaration

Expected PSL		Accepted PSL			PLM-P	UNEQ-P	PDI-P
00	Unequipped	00	Unequipped		Match	Inactive	Inactive
		01	Equipped non specific		Mismatch	Inactive	Inactive
		02-E0 FD-FF	Equipped specific		Mismatch	Inactive	Inactive
		E1-FC	PDI	$=_{exp}$PDI	Mismatch	Inactive	Active
				$!=_{exp}$PDI	Mismatch	Inactive	Inactive
01	Equipped non specific	00	Unequipped		Mismatch	Active	Inactive
		01	Equipped non specific		Match	Inactive	Inactive
		02-E0 FD-FF	Equipped specific		Match	Inactive	Inactive
		E1-FC	PDI	$=_{exp}$PDI	Match	Inactive	Active
				$!=_{exp}$PDI	Mismatch	Inactive	Inactive
02-FF	Equipped specific PDI	00	Unequipped		Mismatch	Active	Inactive
		01	Equipped non specific		Match	Inactive	Inactive
		02-E0 FD-FF	Equipped specific	$=_{exp}$PSL	Match	Inactive	Inactive
				$!=_{exp}$PSL	Mismatch	Inactive	Inactive
		E1-FC	PDI	$=_{exp}$PDI	Match	Inactive	Active
				$!=_{exp}$PDI	Mismatch	Inactive	Inactive

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 06:08:52 PM

Table 3 Expected PDI Defect Based on PDI and PDI Range Values

PDI register value	PDI range register value	Exp PDI	PDI register value	PDI range register value	Exp PDI
00000	Disable	None	01111	Disable	EF
	Enable			Enable	E1-EF
00001	Disable	E1	10000	Disable	F0
	Enable	E1-E1		Enable	E1-F0
00010	Disable	E2	10001	Disable	F1
	Enable	E1-E2		Enable	E1-F1
00011	Disable	E3	10010	Disable	F2
	Enable	E1-E3		Enable	E1-F2
00100	Disable	E4	10011	Disable	F3
	Enable	E1-E4		Enable	E1-F3
00101	Disable	E5	10100	Disable	F4
	Enable	E1-E5		Enable	E1-F4
00110	Disable	E6	10101	Disable	F5
	Enable	E1-E6		Enable	E1-F5
00111	Disable	E7	10110	Disable	F6
	Enable	E1-E7		Enable	E1-F6
01000	Disable	E8	10111	Disable	F7
	Enable	E1-E8		Enable	E1-F7
01001	Disable	E9	11000	Disable	F8
	Enable	E1-E9		Enable	E1-F8
01010	Disable	EA	11001	Disable	F9
	Enable	E1-EA		Enable	E1-F9
01011	Disable	EB	11010	Disable	FA
	Enable	E1-EB		Enable	E1-FA
01100	Disable	EC	11011	Disable	FB
	Enable	E1-EC		Enable	E1-FB
01101	Disable	ED	11100	Disable	FC
	Enable	E1-ED		Enable	E1-FC
01110	Disable	EE			
	Enable	E1-EE			

The RHPP monitors bits 5, 6 and 7 of the path status byte (G1) to detect path remote defect indication (RDI-P) and path enhanced remote defect indication (ERDI-P) defects.

Downloaded by Content Team Submitter Inc. on Wednesday, 07 February 2007 06:59:42 PM

RDI-P is declared when bit 5 of the G1 byte is set high for five or ten consecutive frames (selectable by the PRDI10 bit in the configuration register). RDI-P is removed when bit 5 of the G1 byte is set low for five or ten consecutive frames. ERDI-P is declared when the same 010, 100, 101, 110 or 111 pattern is detected in bits 5, 6 and 7 of the G1 byte for five or ten consecutive frames (selectable by the PRDI10 bit in the configuration register). ERDI-P is removed when the same 000, 001 or 011 pattern is detected in bits 5, 6 and 7 of the G1 byte for five or ten consecutive frames.

The RHPP extracts and serially outputs all the path overhead (POH) bytes on the time multiplexed RPOH port. The POH bytes are output in the same order that they are received (J1, B3, C2, G1, F2, H4, Z3, Z4 and N1). RPOHCLK is the generated output clock used to provide timing for the RPOH port. RPOHCLK is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock.

10.6 Receive SONET/SDH Virtual Container Aligner (SVCA)

The SONET (SDH) Virtual Container Aligner (SVCA) block aligns the payload data from an incoming SONET (SDH) data stream sourced by the RHPP blocks to a new transport frame reference. The alignment is accomplished by recalculating the STS (AU) payload pointer value based on the offset between the transport overhead of the incoming data stream and that of the outgoing data stream. The aligned stream or streams are provided to:

1. The Output APS Interface when the S/UNI 9953 is configured as the Protect Mate or

2. The Receive Cell Frame Processors (RCFP, RCFP-9953) when the S/UNI 9953 is configured for ATM or POS modes or

3. The Receive 64B/66B Processor (R64B66B) when the S/UNI 9953 is configured for IEEE 802.3ae 10G Ethernet operation.

Frequency offsets (e.g., due to plesiochronous network boundaries, or the loss of a primary reference timing source) and phase differences (due to normal network operation) between the incoming data stream and the outgoing data stream are accommodated by pointer adjustments in the outgoing data stream.

10.6.1 Elastic Store

The Elastic Store performs rate adaptation between the line side interface and the system side interface. The entire incoming payload, including path overhead bytes, is written into a first-in-first-out (FIFO) buffer at the incoming byte rate. Each FIFO word stores a payload data byte and a one-bit tag labeling the J1 byte. Incoming pointer justifications are accommodated by writing into the FIFO during the negative stuff opportunity byte or by not writing during the positive stuff opportunity byte. Data is read out of the FIFO in the Elastic Store block at the outgoing byte rate by the Pointer Generator. Analogously, outgoing pointer justifications are accommodated by reading from the FIFO during the negative stuff opportunity byte or by not reading during the positive stuff opportunity byte.

Downloaded by [illegible] on Wednesday, 08 February, 2017, 06:5[illegible]

The FIFO read and write addresses are monitored. Pointer justification requests will be made to the Pointer Generator based on the proximity of the addresses relative to programmable thresholds. The Pointer Generator schedules a pointer increment event if the FIFO depth is below the lower threshold and a pointer decrement event if the depth is above the upper threshold. FIFO underflow and overflow events are detected and path AIS is optionally inserted in the outgoing data stream for three frames to alert downstream elements of data corruption.

10.6.2 Pointer Generator

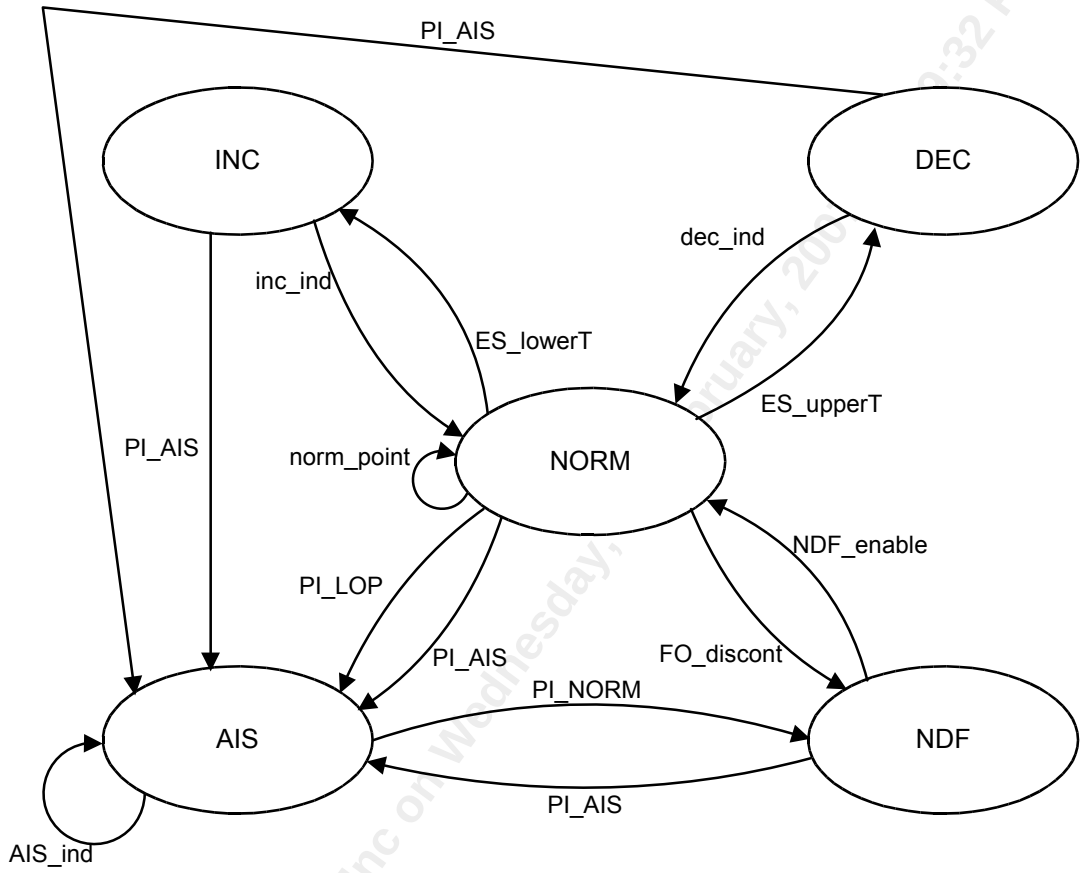
The Pointer Generator generates the H1 and H2 bytes in order to identify the location of the path overhead byte (J1) and all the synchronous payload envelope bytes (SPE) of the STS-48c (VC16-16c) or STS-192c (VC-64-64c) payloads. Within the pointer generator algorithm, five states are defined as shown below:

- NORM_state (NORM)
- AIS_state (AIS)
- NDF_state (NDF)
- INC_state (INC)
- DEC_state (DEC)

The transition from the NORM to the INC, DEC, and NDF states are initiated by events in the Elastic Store block. The transition to/from the AIS state are controlled by the pointer interpreter in the Receive High Order Path Processor block. The transitions from INC, DEC, and NDF states to the NORM state occur autonomously with the generation of special pointer patterns.

Downloaded by Content Team of Partminer Inc on Tuesday, 07 February, 2017 06:55:22 AM

Figure 15 Pointer Generation State Diagram



The following events, indicated in the state diagram, are defined:

ES_lowerT: ES filling is below the lower threshold + previous inc_ind, dec_ind or NDF_enable more than three frames ago.

ES_upperT: ES filling is above the upper threshold + previous inc_ind, dec_ind or NDF_enable more than three frames ago.

FO_discont: frame offset discontinuity

PI_AIS: PI in AIS state

PI_LOP: PI in LOP state

PI_NORM: PI in NORM state

Note

1. A frame offset discontinuity occurs if an incoming NDF enabled is received, or if an ES overflow/underflow occurred.

Downloaded by Content Team of Pulsonix Inc on Wednesday, February, 2008 10:32 PM

The autonomous transitions indicated in the state diagram are defined as follows:

inc_ind: transmit the pointer with NDF disabled and inverted I bits, transmit a stuff byte in the byte after H3, increment active offset.

dec_ind: transmit the pointer with NDF disabled and inverted D bits, transmit a data byte in the H3 byte, decrement active offset.

NDF_enable: accept new offset as active offset, transmit the pointer with NDF enabled and new offset.

norm_point: transmit the pointer with NDF disabled and active offset.

AIS_ind: active offset is undefined, transmit an all-1's pointer and payload.

Notes

1. Active offset is defined as the phase of the SPE (VC).
2. The ss bits are undefined in SONET, and has bit pattern 10 in SDH.
3. Enabled NDF is defined as the bit pattern 1001.
4. Disabled NDF is defined as the bit pattern 0110.

10.7 Receive Cell, Frame Processors (RCFP, RCFP-9953)

The Receive Cell, Frame and Packet Processors (RCFP, RCFP-9953) provide ATM cell or POS packet delineation and processing. Note, these blocks are not used when processing IEEE 802.3ae 10 Gigabit Ethernet frames.

When the S/UNI 9953 device is configured for quad STS-48c (STM-16c) mode, four RCFP blocks are used, each processing a single STS-48c (STM-16c) stream sourced from the SVCA blocks. The stream may contain either ATM cells or POS packets. ATM cells or POS packets extracted from a stream are written into the Ingress Flexible FIFO (IFLX) for access through the PL4 Interface.

When the S/UNI 9953 device is configured for STS-192c (STM-64c) mode, a single RCFP-9953 block is used to process the single STS-192c (STM-64c) stream sourced from the SVCA blocks. The stream may contain either ATM cells or POS packets. ATM cells or POS packets extracted from the stream are written into the Ingress Flexible FIFO (IFLX) for access through the PL4 Interface.

10.7.1 ATM Processing

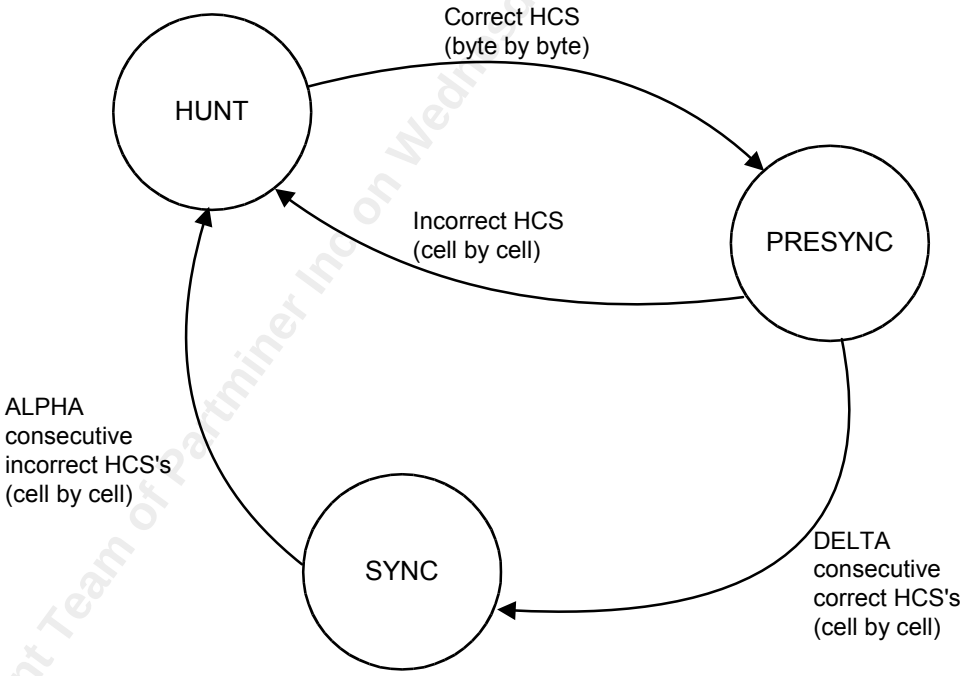
In ATM mode, the RCFP-9953 (or RCFP) can be configured to perform ATM cell delineation, HCS error detection, cell filtering based on idle/unassigned cell detection and ATM cell payload descrambling.

Downloaded by Conexant Technical Documentation on Wednesday, 07 February, 2007 06:59:32 PM

ATM Cell Delineation

Cell Delineation is the process of framing to ATM cell boundaries using the Header Check Sequence (HCS) field found in the cell header. The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. When performing delineation, correct HCS calculations are assumed to indicate cell boundaries. Cells are assumed to be byte-aligned to the synchronous payload envelope. The cell delineation algorithm searches the 53 possible cell boundary candidates individually to determine the valid cell boundary location. While searching for the cell boundary location, the cell delineation circuit is in the HUNT state. When a correct HCS is found, the cell delineation state machine locks on the particular cell boundary, corresponding to the correct HCS, and enters the PRESYNC state. The PRESYNC state validates the cell boundary location. If the cell boundary is invalid, an incorrect HCS will be received within the next DELTA cells, at which time a transition back to the HUNT state is executed. If no HCS errors are detected in this PRESYNC period, the SYNC state is entered. While in the SYNC state, synchronization is maintained until ALPHA consecutive incorrect HCS patterns are detected. In such an event a transition is made back to the HUNT state. The state diagram of the delineation process is shown in Figure 16.

Figure 16 Cell Delineation State Diagram



The values of ALPHA and DELTA determine the robustness of the delineation process. ALPHA determines the robustness against false misalignments due to bit errors. DELTA determines the robustness against false delineation in the synchronization process. ALPHA is chosen to be 7 and DELTA is chosen to be 6. These values result in an average time to delineation of less than 100.98 µs for STS-1 rate and 0.5 µs for the STS-192c/STM-64c rate.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 05:51:29 PM

ATM Descrambler

The self-synchronous descrambler operates on the 48-byte cell payload only when the Cell Delineation state machine is in PRESYNC or SYNC states. The circuitry descrambles the information field using the $x^{43}+1$ polynomial. The descrambler is disabled for the duration of the header and HCS fields and may optionally be disabled for the payload.

ATM Cell Filter and HCS Verification

Cells are filtered (or dropped) based on HCS errors and/or a cell header pattern. Cell filtering is optional and is enabled through the RCFP-9953 (or RCFP) configuration registers. Cells are passed to the downstream TSB while the cell delineation state machine is in the SYNC state as described above. When both filtering and HCS checking are enabled, cells are dropped if uncorrectable HCS errors are detected, or if the corrected header contents match the pattern contained in the RCFP-9953 (or RCFP) Idle Cell Header and Mask configuration registers. Idle or unassigned cell filtering is accomplished by writing the appropriate 8-bit cell header pattern and 8-bit mask into the 16-bit RCFP-9953 (or RCFP) Idle Cell Header and Mask configuration register. Idle/Unassigned cells are assumed to contain the all zeros pattern in the VCI and VPI fields. The RCFP-9953 (or RCFP) Idle Cell Header and Mask configuration register allows filtering control over the contents of the GFC, PTI, and CLP fields of the header.

The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. The ATM processor verifies the received HCS using the polynomial, x^8+x^2+x+1. The coset polynomial, $x^6+x^4+x^2+1$, is optionally added (modulo 2) to the received HCS octet before comparison with the calculated result.

ATM Performance Monitor

The Performance Monitor consists of two 16-bit saturating HCS error event counters and a 32-bit saturating receive cell counter. The first error counter accumulates uncorrectable HCS errors. A 32-bit receive cell counter counts all cells written into the receive FIFO. Filtered cells are not counted.

Each counter may be read through the microprocessor interface. Circuitry is provided to latch these counters so that their values can be read while simultaneously resetting the internal counters to 0 or 1, if appropriate, so that a new period of accumulation can begin without loss of any events. It is intended that the counter be polled at least once per second so as not to miss any counted events.

10.7.2 POS Processing

In POS mode the RCFP-9953 (or RCFP) can be configured to perform packet extraction, FCS error detection, packet payload descrambling, packet length verification and provides performance monitoring functions.

Downloaded by Content Team Datasheet on Wednesday, 27 March 2013, 06:59:00 AM

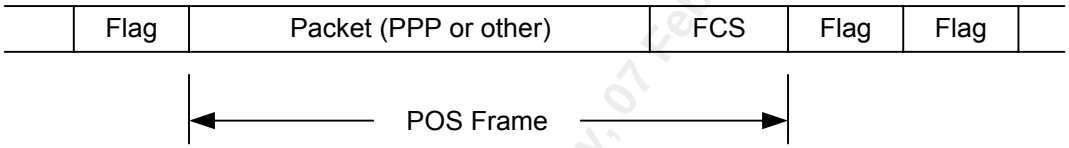
POS Descrambler

When enabled, the self-synchronous descrambler operates on the POS Frame data, descrambling the data with the polynomial $x^{43}+1$. Descrambling is performed on the raw data stream, before any POS frame delineation or byte de-stuffing is performed. Data scrambling can provide for a more robust system preventing the injection of hostile patterns into the data stream.

POS Frame Delineation

Frame boundaries are found by searching for the Flag Character (0x7E). Flags are also used to fill inter-packet spacing. The POS Frame format is shown in Figure 26.

Figure 17 Packet Over SONET Frame Format



Once the frames are delineated and de-stuffed their lengths can be checked. To be legal, packets must contain at least 8 bytes (4 bytes for RCFP), else they are denoted as malformed. Malformed packets are discarded within the RCFP-9953 (or RCFP) and counted as minimum packet length violations.

POS Byte De-stuffing

The byte de-stuffing algorithm searches for the Control Escape character (0x7D). These characters, listed in Table 4, are added for transparency in the transmit direction and must be removed to recover the user data. When the Control Escape character is encountered, it is removed and the following data byte is XORed with 0x20. Therefore, any escaped data byte will be processed properly.

Table 4 Byte De-stuffing

Original	Escaped
7E (Flag Sequence)	7D-5E
7D (Control Escape)	7D-5D
Aborted Packet	7D-7E

On detection of the Abort character sequence, setting the escaped byte as an ERRED EOP terminates the packet. This signals to a downstream TSB that the packet is to be discarded. Note that the 7E of the abort character sequence is treated as an inter-packet flag.

Downloaded by Obsolescence of Part Division on Wednesday, 07 February, 2007 06:53:07 PM

POS FCS Check

The FCS Generator performs a CRC-CCITT (RCFP only) or CRC-32 calculation on the whole POS frame, after byte destuffing and data descrambling. A parallel implementation of the CRC polynomial is used. The CRC algorithm for the Frame Checking Sequence (FCS) field is either a CRC-CCITT (RCFP only) or CRC-32 function.

The CRC-CCITT is two bytes in length and has a generating polynomial:

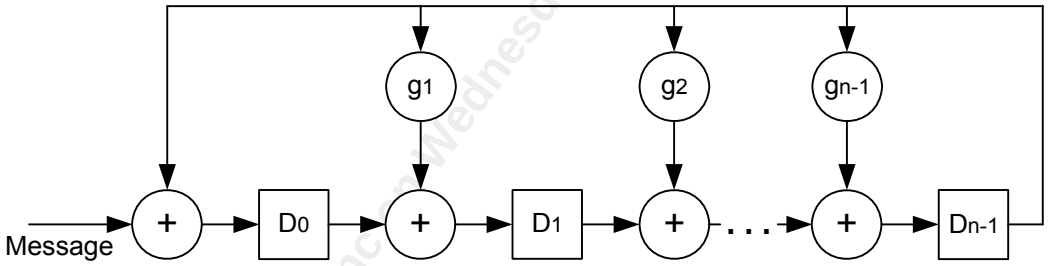
$$g(x) = 1+x^5+x^{12}+x^{16}$$

The CRC-32 is four bytes in length and has a generating polynomial:

$$g(x) = 1+x+x^2+x^4+x^5+x^7+x^8+x^{10}+x^{11}+x^{12}+x^{16}+x^{22}+x^{23}+x^{26}+x^{32}$$

The first FCS bit transmitted is the coefficient of the highest term. Packets with FCS errors are marked as such, (EOP ERRED), and should be discarded by a downstream device. Note that the FCS calculation will proceed independent of any errors detected upstream. Thus, under abort, max length violations, etc, one might also get FCS violations.

Figure 18 CRC Decoder



POS Performance Monitor

The Performance Monitor consists of four 16-bit saturating error event counters, one 32-bit saturating received good packet counter, and one 40-bit counter for accumulating non-flag bytes received, either before or after de-stuffing. The first 16-bit error event counter accumulates FCS errors. The second 16-bit error event counter accumulates minimum length violation packets. The third 16-bit error event counter accumulates maximum length violation packets. The fourth 16-bit error event counter accumulates aborted packets.

Each counter may be read through the microprocessor interface. Circuitry is provided to latch these counters so that their values can be read while simultaneously resetting the internal counters to a value dependent on the number of count events during the transfer, so that a new period of accumulation can begin without loss of any events. The counters should be polled at least once per second so error events will not be missed.

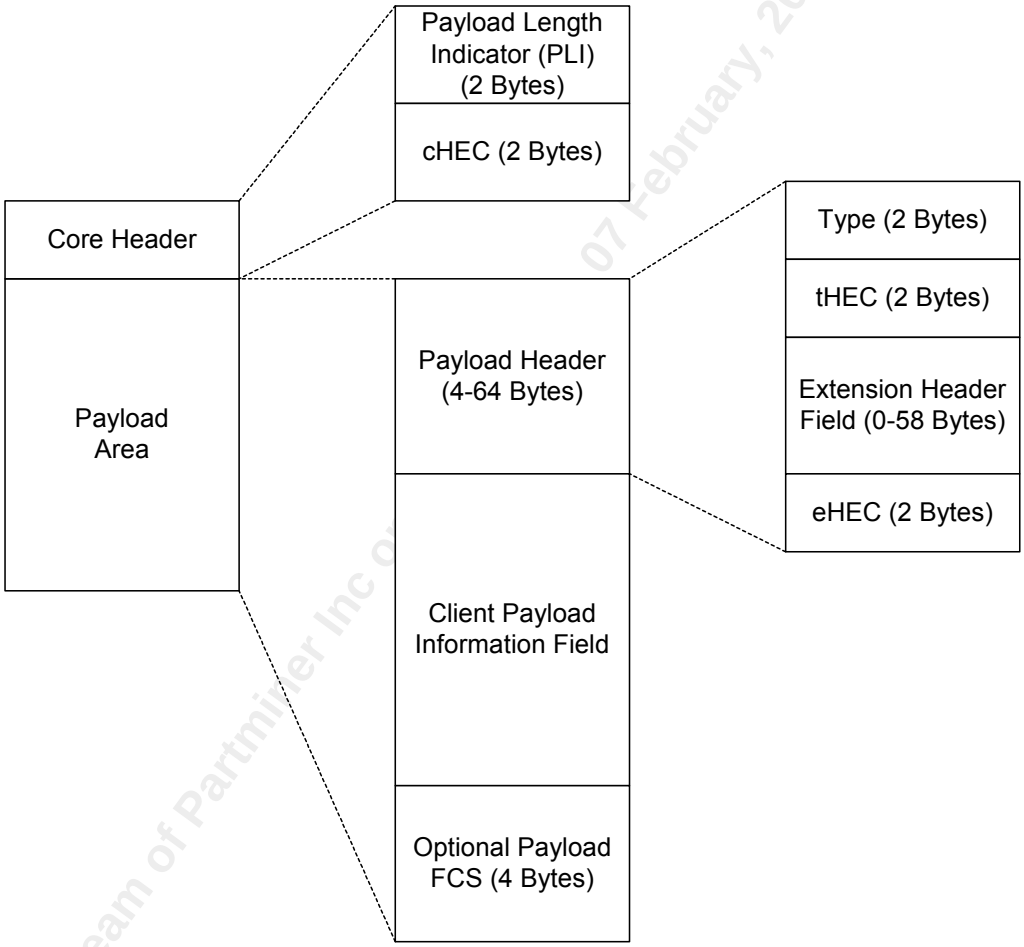
Downloaded by Cisco Technology Inc. on Wednesday, 07 February, 2007 06:59:52 PM

10.7.3 GFP Processing

In GFP mode, the RCFP-9953 performs GFP frame delineation, cHEC error detection and correction, optional payload plus FCS descrambling, idle frame detection and filtering, frame length checking and optional eHEC/tHEC , OAM sHEC and FCS validation.

The GFP Frame format is shown in Figure 19.

Figure 19 GFP Frame Format



GFP Frame Delineation

GFP Frame Delineation is the process of framing to GFP frame boundaries using the 2-byte PLI field in the GFP frame core header. When DC Balance has been applied to the core header it is XORed with the 4 byte "B6AB31E0"hex mask before applying to the CRC calculation. The cHEC is a 16-bit CRC calculation using the CRC-CCITT generating polynomial with an initial value of zero;

$$g(x) = 1+x^5+x^{12}+x^{16}$$

Downloaded by Content Team of Partminer Inc on 07 February, 2007 06:59:32 EST

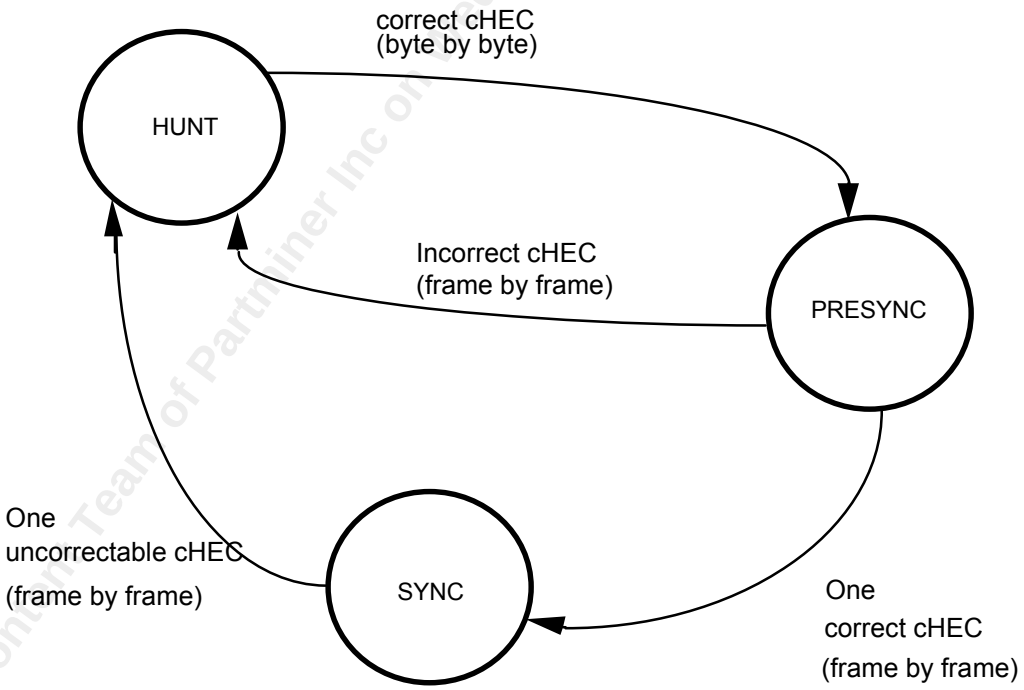
The resulting CRC residue is used without further manipulation to verify the cHEC. When performing delineation, correct cHEC calculations are assumed to indicate frame boundaries. This process is very similar to the ATM Cell Delineation process, the main difference being the delineation algorithm must allow for varying GFP frame lengths (4 to ~64k bytes) when searching for, and maintaining, frame alignment.

The last processed GFP frame length is used to locate the next GFP frame header. These corresponding bytes are applied to the cHEC verification circuitry and the result determines the next state of the GFP Frame Delineation state machine.

While searching for a frame boundary location, the GFP frame delineation circuit is in the HUNT state. When a correct cHEC is found, the GFP frame delineation state machine enters the PRESYNC state. The PRESYNC state validates the proceeding frame boundary. If the GFP frame boundary is invalid, an incorrect cHEC will be received and a transition back to HUNT state results. If a correct cHEC is received then the SYNC state is entered. The total number of consecutive correct cHEC's required to move from HUNT to SYNC state is 2.

While in the SYNC state, synchronization is maintained until an uncorrectable cHEC pattern is received. In such an event a transition back to the HUNT state results. The state diagram of the delineation process is shown in Figure 20.

Figure 20 GFP Delineation State Diagram



Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 6:59:32 PM

Core Header DC Balancing

The RCFP-9953 optionally performs Core Header DC Balancing. When the CORE_DC configuration parameter is set to logic one, the Core Header is XORed with the value 0xB6AB31E0.

GFP Frame Filter and HEC Verification

GFP frames are filtered (or dropped) based on cHEC errors, idle frame detection, OAM frame detection or illegal length. GFP frames are passed to the downstream block while the GFP frame delineation state machine is in the SYNC state as described above.

Incoming frames containing no cHEC errors are passed to the downstream block. Received frames containing apparent single-bit cHEC errors are corrected. Corrected non-idle frames are always passed to the downstream block. Frames containing uncorrectable cHEC errors will be filtered within the RCFP-9953.

If the RCFP-9953 is configured for "No cHEC Verification" the cHEC CRC test-pass result is permanently forced true, (i.e. no uncorrectable cHECs are ever received). Once in SYNC the Frame Delineation state machine will never leave this state unless a force HUNT event occurs (i.e. RXOFF = 1). The received data stream is arbitrarily delineated into frames whose lengths are determined from the corresponding PLI-field bytes. In this configuration these lengths have no real meaning.

Idle frames are identified as those having a PLI = 0 and all received Idle frames are counted in the Idle Frame statistic. Idle frames are discarded within the RCFP-9953.

OAM frames are identified as those having a PLI of 1, 2 or 3 and are 12-bytes in length. After delineation OAM frames can optionally be discarded within the RCFP-9953.

The tHEC,eHEC and OAM sHEC checking use the same CRC polynomial as used for the cHEC.

When Payload header checking is enabled, frames containing tHEC/eHEC and OAM sHEC errors are transferred to the downstream block and have the EOP byte ERRED. The Extension header is assumed not present when its configured length is set to less than 3.

When Payload Area FCS checking is enabled, frames containing FCS errors are transferred to the downstream block with their EOP byte ERRED. FCS verification is performed using the CRC-32 polynomial (as used for POS) with an initialization value of all ones.

Received frames whose lengths are less than the configured minimum or greater than the configured maximum lengths are transferred to the downstream block and have their EOP byte ERRED. Frames exceeding the configured maximum length are truncated to this length with the remaining trailing bytes of the frame filtered. Note that the configured length consists of all bytes in the GFP, (i.e. frame_length = core_header + type_header + extension_header + payload + FCS).

Downloaded by Robert Tsai of Quantenna Inc on Wednesday 17 February 2010 06:59:32 PM

Descrambler

The descrambler operates on the GFP Payload and FCS bytes (when present) using the $x^{43}+1$ descrambler polynomial when the Frame Delineation state machine is in PRESYNC or SYNC states. On reset, the descrambler is set to all ones to ensure correct descrambling on start-up.

10.8 Receive 64B/66B Processor (R64B66B)

The Receive 64B/66B Processor (R64B66B) implements the IEEE 802.3ae 10 Gigabit Ethernet PCS Sub-layer. It receives a data stream from the SVCA blocks, 64B/66B frame synchronizes to it, strips the stream and descrambles the stream. The resulting extracted 10 Gigabit Ethernet frames are provided to the Receive 10G Ethernet MAC (RXXG) block for further processing. The R64B66B block is not used when processing ATM cells, GFP frames or POS packets.

The R64B66B implements the following principal functions:

- Ethernet frame delineation
- Aligns to 32-bit SOP Boundaries
- 33:32 Rate adaptation
- 64B66B Data decoding
- 64B66B Control Code decoding
- Data De-scrambling
- Receive Link Fault signaling
- Receive Jitter test pattern checking

10.8.1 RX PCS

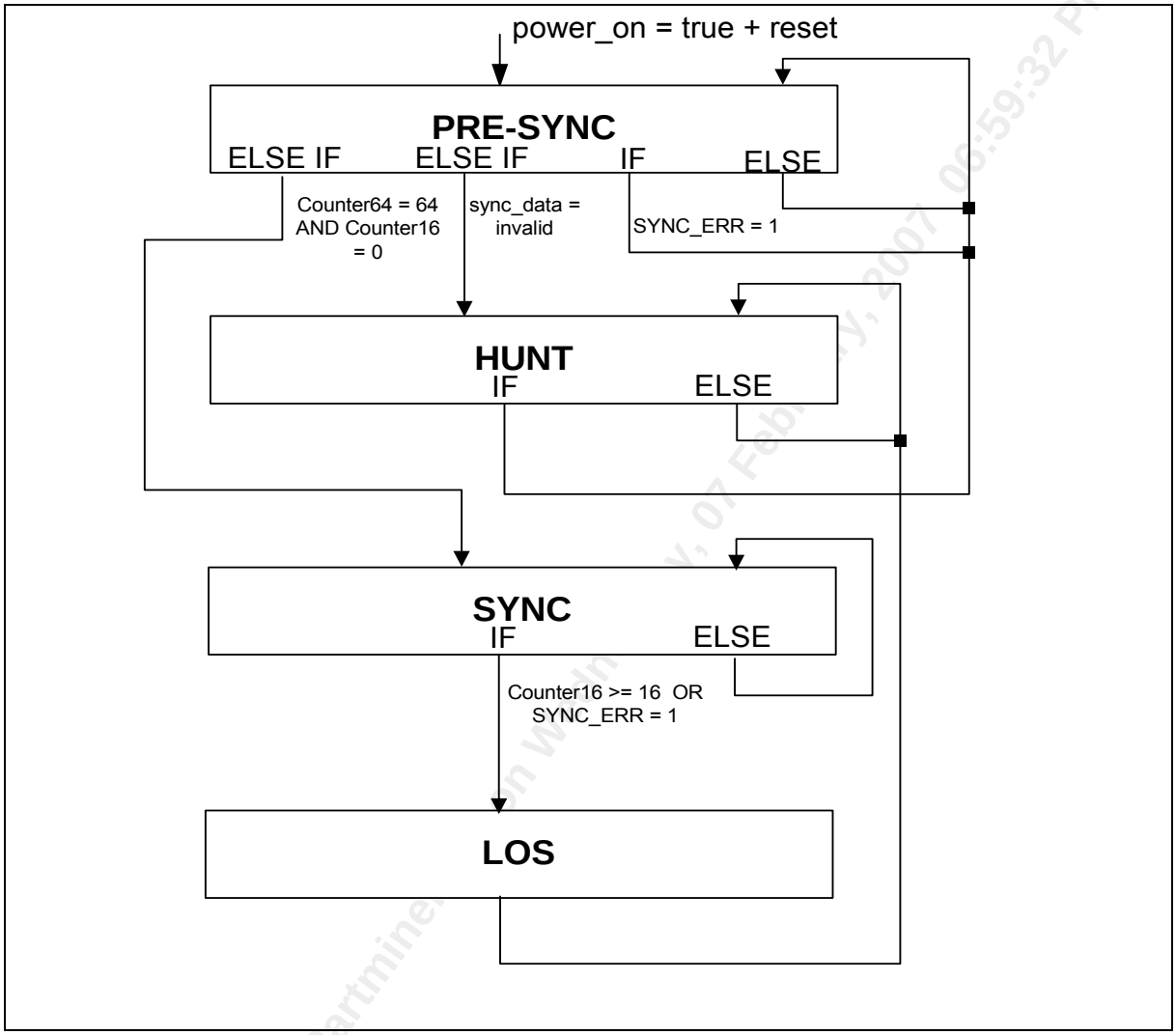
The RX PCS contains the Finite State Machines for Synchronization, Receive Data and Bit Error monitoring. It contains a de-scrambler based on $G(x) = 1 + X^{39} + X^{58}$. It provides all the timing and control necessary for capturing, aligning, and processing the downstream data. The decision(s) to leave or remain in a given state are based upon the IEEE 802.3ae Standard. The RX PCS provides Jitter Test pattern checking as per IEEE 802.3ae standard.

Downloaded by Content Team of Datasheet Inc on Wednesday, 07 February, 2007, 06:59:00 PM

The Receive SYNC State Machine, shown in Figure 10-1 below, contains four states PRE-SYNC, HUNT, SYNC and LOS and is based on the synchronization process described in IEEE 802.3ae standard clause 49. PRE-SYNC is the start-up state, when in this state, it will attempt to sync on the incoming 2-bit sync field. If the 2-bit sync field is not a proper sync character of '10' or '01' then the state machine transitions to the HUNT state. The HUNT state will then shift the data by 2-bits. This shift will now provide the Receive SYNC State Machine with a new sync field and will attempt to synchronize on this new sync field. This process will continue until the current sync field and the next sync field are valid sync characters of '10' or '01'. When this happens the Receive SYNC State Machine monitors two counters, 64 block counter and 16 bad sync counter. The 64-block counter performs the 64-block window that is needed to maintain SYNC in the RX PCS, it counts 64 66-bit blocks and rolls over and starts again. The 16 bad sync counter is needed to count the number of bad sync fields received either '11' or '00'. If the Receive SYNC State Machine is seeing good sync and the 64 block counter = 64 and the 16 bad sync counter = 0, the state machine will transition to the SYNC state. When in the SYNC state the state machine continues to monitor the 64 block counter and the 16 bad sync counter, if the 16 bad sync counter is = 16 and the 64 block counter is less than 64 then the state machine transitions to the LOS state. The transition to the LOS state will cause the assertion of Loss Of Sync and Link Fail status, which may cause an interrupt if enabled. Loss Of Sync will cause the Receive and BER state machines to transition to their INIT states. Once in the LOS state the Receive state machine, on the next clock cycle, transition to the HUNT state to try and re-acquire sync.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 16:30:00 EST

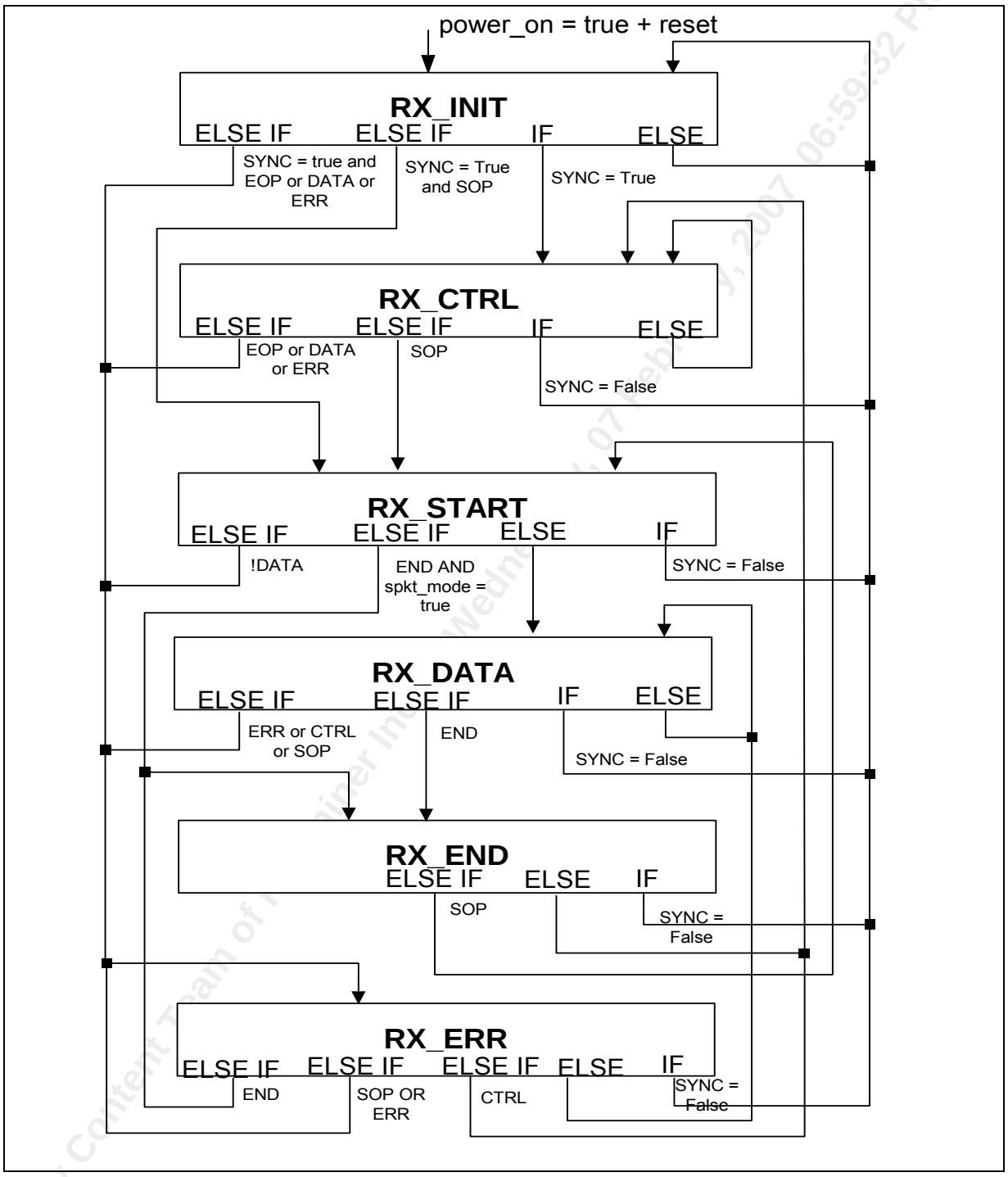
Figure 21 RX SYNC State Machine



The Receive State Machine, shown in Figure 22 below, contains six states RX_INIT, RX_CTRL, RX_START, RX_DATA, RX_END, RX_ERR and is based on the Receive State Machine process described in IEEE 802.3ae standard clause 49. The RX_INIT state is the start-up state and will not transition out of this state until the Receive SYNC State Machine is in the SYNC state. When the Receive State Machine is in the RX_INIT state no data will be transferred to the MAC. Once the Receive SYNC State Machine is in the SYNC state the Receive State Machine will monitor the sync and type fields of the incoming data stream to decide on the proper transitions between states.

Downloaded by [illegible] of Partmine [illegible] on Wed Jan [illegible] 07 Feb [illegible] y, 2007 06:59:32 PM

Figure 22 Receive State Machine

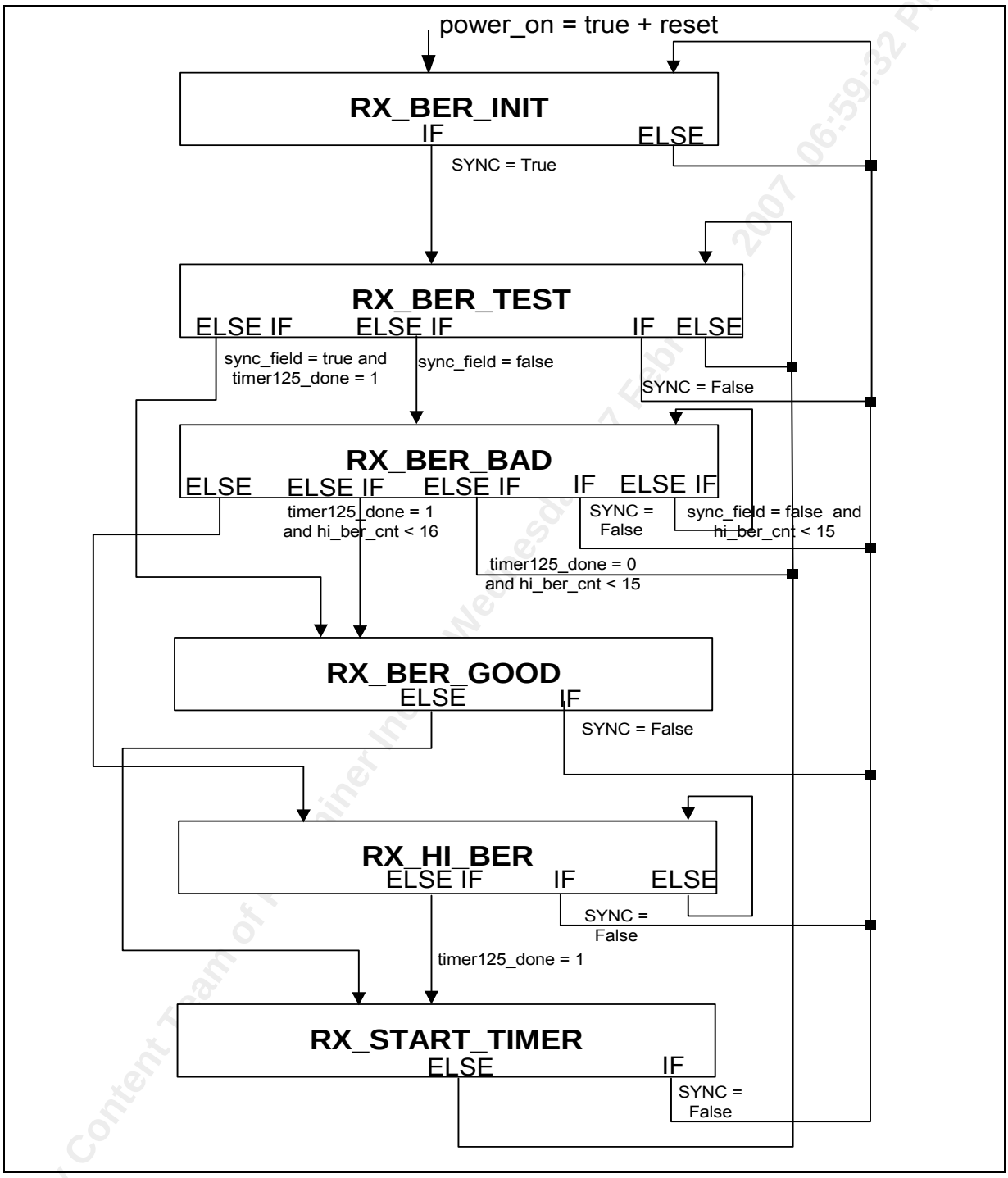


Downloaded by Content Team of Fulcrum Microsystems Inc. on Wednesday, 07 February, 2007 06:59:32 PM

The Receive Bit Error Rate (BER) State Machine, shown in Figure 23 below, contains six states RX_BER_INIT, RX_BER_TEST, RX_BER_BAD, RX_BER_GOOD, RX_HI_BER, RX_START_TIMER and is based on the Receive BER State Machine process described in IEEE 802.3ae standard clause 49. The RX_BER_INIT state is the start-up state and will not transition out of this state until the Receive SYNC State Machine is in the SYNC state. No Bit Error monitoring will be performed when in the RX_BER_INIT state. Once the Receive SYNC State Machine is in the SYNC state the Receive BER State Machine will monitor the sync field of the incoming data stream to decide on the proper transitions between states. The Receive BER State Machine monitors two counters and the sync field of the incoming data stream. The two counters are a 125µs counter and the high bit error counter. The 125µs counter is an approximation based on the SYS_CLKx2 clock. The SYS_CLKx2 period is ~6.2 ns, therefore the counter will count up to 20,162 clock periods and hold. The high bit error counter counts the number of invalid sync fields (‘11’ or ‘00’).

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2018 6:52:32 AM

Figure 23 RX BER State Machine



Downloaded by Content Team of Internet Wednesday, 07 February 2007 06:59:32 PM

10.8.2 Jitter Test Pattern Checker

The Control Detector can be put into a test mode (jitter test mode) where it counts errors in the received data. The other side of the link must be put into test mode, so that it is generating the expected data patterns.

The Jitter test pattern checker utilizes the lock state machine and the descrambler operating as they do during normal data reception. The hi_ber state machine is disabled during receive test pattern mode. When block_lock is true and the receive test pattern mode is active, the test pattern checker observes the output from the descrambler. When the output of the descrambler is the data pattern or its inverse, a match is detected. Since the transmitter's scrambler is loaded with a seed value every 128 blocks (block is 64 bits) and the receiver's descrambler is running normally, a mismatch will be detected once every 128 blocks in the absence of errors. The transmitter reseeding the scrambler, and inverting the input data, causes this mismatch. The test pattern checker will count 128-block windows. The first mismatch in a window will not increment the test pattern error counter. Any subsequent mismatch in a window indicates an error and will increment the test pattern error counter.

10.9 Receive 10G Ethernet MAC (RXXG)

The Receive 10G Ethernet MAC (RXXG) provides 10 Gigabit Media Access Control Sub-layer processing on a single 10 Gigabit Ethernet stream. The RXXG expects data from the R64B66B block when the S/UNI 9953 is configured for IEEE 802.3ae 10 Gigabit Ethernet operation. This block is not used when the S/UNI 9953 is configured for ATM cell, GFP frame or POS packet processing.

The RXXG implements the following principal functions:

- Ethernet framing (detection and framing to the standard preamble/SFD sequence, removal of the preamble/SFD, and checking of the 32-bit CRC field) and frame validation (marking of errored frames for discard).
- Frame timing check (relative to the receive input clock reference): the RXXG will verify that the interframe gap does not fall below a pre-set minimum, and will filter frames that violate this restriction, when used in LAN-mode devices.
- Optional received frame filtering: frames can be discarded if they are found to contain length or CRC errors. The RXXG block implements a 2048-byte full-frame buffer to facilitate this filtering. Note that jumbo frames (>1522 bytes) will not be filtered, but will be marked for discard by a downstream entity.
- Received frame stream parsing, and PAUSE MAC Control frame detection, validation and extraction. The PAUSE Timer fields of received PAUSE frames are extracted and sent to flow control logic on a separate set of signals.
- Receive statistics support: the RXXG checks every received frame against the IEEE 802.3 frame error criteria, and outputs a statistics vector at the end of every received frame. The statistics vector is expected to be used by an external unit to update the appropriate statistics counters, which should be used to implement the standard Ethernet MIBs for link management.
- Optional Receive PAD stripping for all non-errored packets received.

Downloaded by ConnectTech Pinout Inc on Wednesday, 07 February 2018, 08:59:32 PM

The RXXG functional sub units include:

- Receive MAC (RMAC) Framer
- CRC Checker
- Receive MAC (RMAC) Parser
- Receive FIFO

10.9.1 RMAC Framer

The RMAC Framer monitors for valid words from the R64B66B block, expecting preambles/SFD bytes. If the framer is looking for standard Ethernet preamble/ SFD, it can also be configured to validate the preamble byte contents and length. If errors are detected, RMAC Framer will discard the frame. If no errors are found, the preamble and SFD are stripped and the following frame byte marked as the MAC Header SOP. At this stage, the RMAC Framer writes the frame into an internal FIFO. The RMAC Parser starts MAC frame parsing and the CRC Checker starts accumulation. PUREP, and LONGP are register configuration bits that are set in the RXXG Configuration 1 register, address 0x2040. The device defaults to PUREP disabled where only the SFD is evaluated. If PUREP is enabled, the device will ignore frames with anything other than 0x55 or pure preamble.

Table 5 Preamble Checking

PUREP	LONGP	Preamble/SFD Framing Accepted
0	0	0-11 bytes of non-0xD5 byte values followed by 0xD5 (SFD) byte
0	1	Any number of non-0xD5 byte values followed by 0xD5 (SFD) byte
1	0	0-11 bytes of 0x55 byte values followed by 0xD5 (SFD) byte
1	1	Any number >1 byte of 0x55 byte values followed by 0xD5 (SFD) byte

RMAC Framer maintains a packet count and will perform in-range checking for Type-Length field values between 0 and 1518 bytes. Packets with in-range errors may be optionally discarded. RMAC Framer verifies packet size against the minimum value (64 bytes) and maximum programmable frame size. Packets outside this range may be optionally discarded. Table 6 lists the range, packet size checks and resulting packet classification. All the actual length value checks must have RX_MAXFR, maximum frame, and value incremented by 4 for the case where the packet is VLAN Tagged. Also note that 'CRC Result' also takes into consideration the case where the packet EOP received from the line had LINE_ERR set, and this case is treated as if the packet had a bad CRC.

Table 6 Range, Size and CRC Result Processing

Type/Length Field (TL)	Actual Packet Size	CRC Result	Packet Classification
X	< 64	Good	Undersize
X	< 64	Bad	Fragment

Downloaded by Content Delivery on Wednesday, 10 October 2007 06:59:32 PM

Type/Length Field (TL)	Actual Packet Size	CRC Result	Packet Classification
X	> RX_MAXFR	Good	FrameTooLong
X	> RX_MAXFR	Bad	Jabber
X	>63 & <= RX_MAXFR	Bad	FrameWithFCSError
46 – 1500	TL + 18	Good	Good
46 – 1500	TL + 22 & (VLAN Tagged)	Good	Good
46 – 1500	! (TL+18) & (> 63 & <= RX_MAXFR)	Good	InRangeLengthError
46 – 1500	! (TL+22) & (> 63 & <= RX_MAXFR) & (VLAN Tagged)	Good	InRangeLengthError
< 46	64	Good	Good
< 46	>63 & <= RX_MAXFR	Good	InRangeLengthError
< 46	68 & (VLAN Tagged)	Good	Good
< 46	>64 & <= RX_MAXFR & !(68 & VLAN)	Good	InRangeLengthError
1501-1536	-	Good	Good
> 1536	> 64 & <= RX_MAXFR	Good	Good

Once an EOP is received from the R64B66B block, the RMAC Framer waits for a CRC result to be returned from the CRC Checker and packet filter status from the RMAC Parser. It will then inform the FIFO Controller about FIFO flushing of the packet or forwarding of the packet to the System Interface. If the packet is terminated with an error flag set with EOP, RMAC Framer may discard the packet only if it is less than 1900 bytes in length. If the frame is larger than the internal ram capacity, the frame will not be discarded on error, but marked appropriately and transmitted.

The RMAC Framer can be configured to check for a minimum inter-packet gap between received frames. If this is enabled, the RMAC Framer will ignore packets when the SOP is received during the IPG.

10.9.2 CRC Checker

The CRC checker performs a CRC-32 calculation on the entire data frame received from the RMAC Framer. The 32-bit CRC result is compared to a constant expected value and a good / bad CRC status is returned to the RMAC Framer.

10.9.3 RMAC Parser

The RMAC Parser classifies the frame according to MAC Header fields, DA, SA, Type/Length and optional VLAN Tag. If address filters have been enabled, the required address and optional VLAN ID are applied to an address filter function, which will determine if the frame should be forwarded or filtered. In addition, if Multicast Hashing has been enabled, Multicast DAs are applied to a CRC-32 Hash function, resulting in an index into a 64-bit MHASH register and a filtering/ forwarding decision made. The address filter block resets to a promiscuous mode of operation, whereby all filtering is disabled.

Downloaded by Content Team of Partner Inc. on Wednesday, 07 February, 2007 06:58:32 PM

The RMAC Parser checks for received PAUSE Control frames and, if enabled, will transfer the extracted pause parameter to the TXXG. The RMAC Framer may be configured to forward or filter received MAC Control frames of all types. When RMAC Parser updates the RMAC Framer with frame classification information (after EOP), the RMAC Framer will make a forward/ filter decision.

10.9.4 Receive FIFO

The purpose of the FIFO is to provide the capability to discard errored frames, up to a maximum size of 1522 bytes (maximum expected frame size). This FIFO is independent of the Ingress Flexible FIFO (IFLX) that contains the main ingress system buffering. Two modes of operation are provided, store forward and cut through.

In store-and-forward mode, frame transfer to the IFLX only begins once the complete frame has been written to the FIFO. This will not deal with a situation where an oversized frame is received. Hence a FIFO Read Threshold has been provided, which will be initialized to a value > Maximum Size Frame / 8. This will ensure that if the FIFO fills beyond this level, the read port will begin transferring the frame to the IFLX.

The same FIFO Read Threshold could be used to configure the FIFO for a cut-through mode, with all error frame discard functions disabled. In this case, the IFLX would be informed to begin frame transfer when a small number of entries have been written into the FIFO.

10.10 Ingress Flexible FIFO (IFLX)

The Ingress Flexible FIFO (IFLX) provides a multi channel FIFO to separate the line-side timing from the higher layer system timing and the associated PL4 system interface. The IFLX expects line side data from the RXXG, RCFP and RCFP-9953 blocks depending on the mode of operation.

The IFLX provides 16K bytes of storage in total. When the S/UNI 9953 is configured in quad OC-48 mode, the IFLX can be configured as a four-channel FIFO with the 16K bytes distributed across the 4 channels under user control. When the S/UNI 9953 is configured in single OC-192 mode, the IFLX can be configured as a single FIFO with the 16K bytes dedicated to the channel. Each FIFO channel has a low start threshold, a low watermark, and a high watermark. The low start threshold is used to allow accumulation before burst transfers as to avoid underruns. The low and high watermarks can be used for Ethernet PAUSE Control operation.

The IFLX interfaces to the PL4MOS (scheduler), in order to achieve fairness across the various competing channels.

10.11 PL4 Multi-Channel Output Scheduler (PL4MOS)

The PL4 Multi-Channel Output Scheduler (PL4MOS) block is used to provide fairness when the IFLX is configured for more than one channel operation. The PL4MOS monitors the PL4 FIFO status inputs and schedules an IFLX FIFO channel based on a fairness criterion.

Downloaded by Content Team of Number Intl. Wednesday, 07 February, 2007 06:59:32 PM

The PL4MOS consists of three main blocks: the Status Calendar, the Fairness Controller, and the Scheduling Engine.

10.11.1 Status Calendar

The status calendar communicates with the PL4 interface to obtain the FIFO Status (FS) of each timeslot. FIFO Status is a 2-bit code used to represent the status of the PHY FIFO. The 4 possible combinations for the FIFO status are:

00 STV Starving

01 HUN Hungry

10 SAT Satisfied

11 INV Invalid

The status calendar is responsible for maintaining a local copy of the PHY channels status. It is also responsible for assigning credits to the various channels based on the status of the equivalent PHY logical channel.

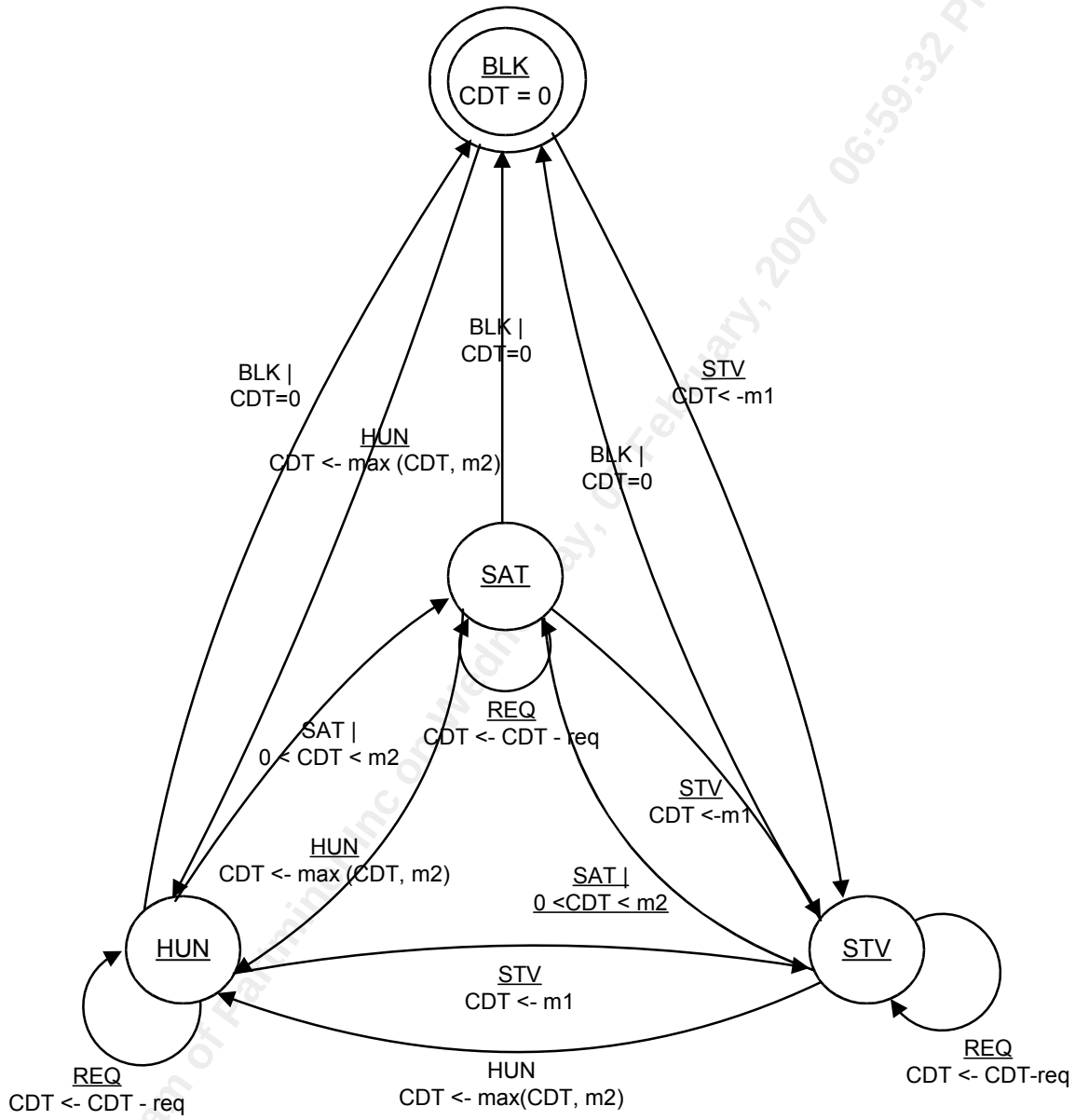
The status calendar obtains the FIFO status from the upstream block. When there is no new FIFO status available, the upstream block maintains all the FIFO status at '11'. If the upstream block has new status for a particular channel, it will update the FIFO status only for that channel. The upstream block will maintain this value for only one clock cycle. It is possible for the upstream block to update more than one channel simultaneously. If any channel status is not '11', the status calendar updates the internal channel status and the equivalent credit counter. The calendar can update any number of channel statuses simultaneously.

Figure 24 shows a state diagram for a single channel and how the FIFO status inputs affect the state machine of each channel. A credit counter (CDT) is defined for each channel. This counter is set to MaxBurst1 when the FIFO status for this channel is STV. If the new status is HUN, the CDT counter is set to the maximum of MaxBurst2 and the previous value of the CDT counter. The values of MaxBurst1, MaxBurst2 are calculated based on the overall system latency and configuration and programmed into PL4MOS registers.

If the RE_INIT (re-initialize) status is asserted at anytime to indicate loss of sync in the upstream block, the status calendar clears all the internal FIFO status and the credit counters to 0's.

Downloaded by Content Team of Radiomic at Monday, 12 February, 2007 06:50:32 PM

Figure 24 State Machine of a FIFO Channel



10.11.2 Scheduling Engine

The scheduling engine is responsible for generating data transfer requests and sending them to the Ingress FIFO (IFLX) block. When IFLX is ready to accept requests, the PL4MOS will inform the IFLX if a new request is available. If the scheduling engine is not able to create a new request because no data was available or there is no credit then no request will be provided to the IFLX even when it is ready to accept data transfer requests.

Downloaded by Content Team of Tarkwa Inc drawdrive.ay, 07 February, 2007 06:59:32 PM

The scheduler generates the request based on two parameters. First is the status of the PHY logical channel whether it is HUN, SAT, STV or BLK, where BLK stands for BLocKed and will be explained later in this section. Second is whether the FIFO block has data ready for this logical channel or not.

The Channel_Ready[TOP_CHAN:0] status from IFLX indicates which logical channels have data available. The Scheduler will check only for the number of logical channels supported. TOP_CHAN is the number of timeslots in the system minus 1. This number depends on the system configuration and is defined as CALENDAR_LEN in the PL4 standard. For S/UNI 9953, TOP_CHAN will be either 0 or 3, representing a single channel system or a four-channel system. Each logical channel is allocated one timeslot.

The scheduling is done in a round robin scheme in service cycles. Each service cycle starts from timeslot [0] up to timeslot [TOP_CHAN]. During each step of the scheduling cycle, the scheduler checks the channel status and if the FIFO has data for this channel. If the status is HUN or STV and the FIFO has data ready for this channel, a service request is generated to this channel. This request is called normal service request. If at least one of these conditions is not valid, the scheduler will allocate the service request for another starving channel, which has data ready in the FIFO and a credit > 0 (even if this channel is blocked). If a request cannot be issued for a starving channel (data not ready or no starving channels), the scheduler looks for a satisfied channel with CDT counter greater than 0 and will issue a request for that channel if it has data ready in the FIFO. Such request is referred to as a bonus request. If the scheduler could not find any suitable STV or SAT channel, it will look for a HUN channel with credit and data ready in the FIFO (even if the channel is blocked). If any channel is found, the scheduler will issue a normal service request (not bonus) for this channel and move the round robin pointer to the point to the channel following this HUN channel.

During the normal service request, the selection of the channel is subject to the round robin scheme. However, the bonus round (including the HUN case) is subject to three rotating priority schemes for STV, SAT and HUN. Those priorities are completely independent. At the start of operation all the priorities are set such that channel 0 has the highest priority in STV, SAT and HUN. When a bonus request is created for a STV channel, this channel is assigned the lowest priority and the following channel gets the highest priority. The same is true for SAT priority. However, the HUN is different. The highest priority in HUN is the current round robin channel. So, when a HUN channel *n* gets a bonus request away from its normal round robin slot, the round robin counter will be updated to *n+1* and the highest HUN priority becomes also *n+1*.

Every time the scheduler issues a request for a channel, it subtracts MAXWRDS from the CDT counter. If the channel credit became zero, this channel status is changed to BLK and no more service requests are issued to this channel until new credit is applied. MAXWRDS specifies the maximum amount of data, in 128-bit words, that should be transferred for this request. The Ingress FIFO (IFLX) will attempt to transfer the smaller of MAXWRDS and the amount of data present in the logical FIFO before retiring the request. The value of MAXWRDS is either the MAX_TRANSFER (PL4MOS register) or CDT counter whichever is less. If the CDT counter of a channel reached 0, no more service requests should be issued to this channel until a new FIFO status adds more credit.

If the RE_INIT (re-initialize) signal is asserted at anytime to indicate loss of sync in the upstream block, the scheduling engine clears all the internal counters and state machines.

Downloaded by [illegible] from Document Center on 16-Feb-2017 at 16:59:32 (MST)

10.11.3 Fairness Controller

The main objective of the fairness controller is to avoid the case where one channel is consuming most of the bandwidth and affecting the bandwidth of other channels. The algorithm is a simplistic algorithm and depends on storing the difference between data served to each channel. If the difference became large, this means that one channel is getting more service than the other channels and that this channel should be blocked.

Each channel has a 16-bit service counter, which counts the number of 16-bit words that have been served from the Ingress FIFO (IFLX) for this channel. After the FIFO executes a service request, it sends the PL4MOS a response to the request. The response message indicates the number of 16-bit words that were actually transferred while processing the request. Note that fractional 16-bit word transfers are rounded up (i.e., counted as full word transfers).

If it is a regular service request, the fairness controller adds the amount of words served to this channel to the channel service counter. If is a bonus request, the amount of words served is ignored and the service counters are not affected.

At the end of each scheduling tour (a complete service cycle starting from channel 0 to TOP_CHAN), the controller calculates the channel that had the least number of words transferred (larger than zero). The number of words served to this channel is referred to as MIN_SERVED. MIN_SERVED is compared to the MaxBurst2 and the larger of them is subtracted from all the service counters that are > 0. If a counter becomes negative, it is reset to 0. Service counters are not permitted to contain negative values.

The fairness algorithm may be enabled or disabled via PL4MOS configuration registers globally or on a per channel basis.

If the RE_INIT (re-initialize) signal is asserted at anytime to indicate loss of sync in the upstream block, the fairness controller clears all the internal counters.

10.12 Receive PL4 Interface

The Receive PL4 Interface implements the PL4 protocol as described in PMC-991635. The PL4 interface provides a 16 bits wide data and in-band control stream, a single control signal, and a dual phase source synchronous clock in the forward path. All forward path signals are differential LVDS. The clock signal is either loop-timed (slave mode) from the TDCLK+/- or internally generated (master mode) using the REFCLK+/- reference input. The control signal is used to identify the in-band control words. In the return path, the PL4 interface provides a two-bit FIFO status bus with associated clock. Please refer to PMC-991635 for protocol details.

The Receive PL4 interface takes a data stream provided by the IFLX block, inserts the in-band control (SOF, EOF, DIP-2), and bursts the stream across the PL4 bus to a data sink in accordance to the PL4 protocol. The data sink provides back to the S/UNI 9953 Receive PL4 interface FIFO status indications using a 2-bit bus and associated clock. These status signals are provided to the PL4MOS block to allow it to make scheduling decision.

In addition, the Receive PL4 interface allows for the transmission of a training sequence to allow for dynamic de skewing by a sink entity.

Downloaded by [illegible] on 07 February 2008 06:50:12 PM

The Receive PL4 Interface is implemented by the PL4ODP block and part of the PL4IO block.

10.13 Transmit PL4 Interface

The Transmit PL4 Interface implements the PL4 protocol as described in PMC-991635, "POS PHY Level 4, Saturn Interface Specification For Packet and Cell Transfer Between Physical Layer and Link Layer Devices for OC-192 SONET/SDH and 10 Gbit/s Ethernet Applications". The PL4 interface provides a 16-bit wide data and in-band control stream, a single control signal, and a dual phase source synchronous clock in the forward path. All forward path signals are differential LVDS. The control signal is used to identify the in-band control words. In the return path, the PL4 interface provides a two-bit FIFO status bus with associated clock. Please refer to PMC-991635 for protocol details.

The Transmit PL4 interface sinks data and control from a 16 bits wide stream, decodes the in-band control, verifies the integrity of the stream (DIP-2), and provides the resulting data and control streams to the EFLX FIFOs. From the EFLX, the Transmit PL4 interface receives FIFO status indications that it formats and provides to the link layer entity in the return path.

Data must contain sufficient training pattern density to allow reliable operation of the data recovery and deskew units. The PL4 interfaces transfer unencoded NRZ data streams. Consequently there may be arbitrarily long runs of consecutive zeros or ones. The Transmit PL4 interface is capable of properly recovering data once training has completed.

The Transmit PL4 Interface is implemented by the PL4IDU block and part of the PL4IO block.

10.14 Egress Flexible FIFO (EFLX)

The Egress Flexible FIFO (EFLX) provides a multi channel FIFO to separate the line-side timing from the higher layer link layer timing and the associated PL4 system interface. The IFLX provides read interfaces to the TXXG, TCFP and TCFP-9953 blocks depending on the mode of operation.

The EFLX provides 20K bytes of storage in total. When the S/UNI 9953 is configured in quad OC-48 mode, the EFLX can be configured as a 4 channel FIFO with the 20K bytes distributed across the 4 channels under user control. When the S/UNI 9953 is configured in single OC-192 mode, the EFLX can be configured as a single FIFO with the 20K bytes dedicated to the single channel. Each FIFO channels has a low start threshold, a low watermark, and a high watermark. The low start threshold is used to allow accumulation before transmission as to avoid underruns. The low and high watermarks can be used for FIFO status indications to the link layer device.

10.15 Transmit 10G Ethernet MAC (TXXG)

The Transmit 10G Ethernet MAC (TXXG) provides 10 Gigabit Media Access Control Sub-layer processing on a single 10 Gigabit Ethernet stream. The TXXG reads partially formed Ethernet frames from the Egress Flexible FIFO (EFLX) and generates completely formed Ethernet frames. When the S/UNI 9953 is configured for IEEE 802.3ae 10 Gigabit Ethernet operation, the resulting frames are forward to the T64B66B block.

Downloaded by Content Library at Luminent, Inc. on Wednesday, 07 February, 2007 09:09:32 PM

The TXXG functional sub units include:

- MAC Incoming Flow Control State-machine which responds to incoming flow control requests (from the RXXG interface) and maintains the pause timer
- MAC Outgoing Flow Control State-machine, which responds to requests from the Receive System port to build and request the transmission of 802.3 full-duplex flow control (FDFC) packets
- MAC Core, which frames Ethernet packets (with preamble, SFD, pad and CRC) from two sources – EFLX and Outgoing Flow Control State-machine.
- CRC Generator

10.15.1 MAC Incoming Flow Control State Machine

When a Receive MAC (RXXG) decodes an error-free incoming 803.2 full-duplex flow control packet, the RXXG sends a PAUSE signal to the TXXG indicating that transmission is to be paused. The pause parameter is transferred to the TXXG unit, to apply to the local pause timer. This State-machine loads the timer (on request from the RXXG unit) and decrements the timer in units of pause interval**.** Note, PAUSE control frame transmission initiated using register bits is not affected by PAUSE.

- The TXXG implements the following principal functions:
- Ethernet framing (optional insertion of an 8-byte preamble/Start Frame Delimiter sequence, plus computation and optional insertion of a 32-bit FCS).
- Frame timing relative to the system clock reference input. The TXXG will insert the correct programmable interframe gap between frames to ensure that LAN-mode operation conforms to the IEEE 802.3 specification. In WAN mode, no interframe gap is inserted; instead, the downstream payload processor is responsible for flow controlling the data stream.
- PAUSE frame generation and insertion. The TXXG block will generate and format 64-byte PAUSE MAC Control frames in response to requests from external blocks, with the specified pause timer values inserted at the proper location. Generated PAUSE frames are multiplexed into the outgoing frame stream in between data frames and with the proper spacing.
- Transmit pause implementation. PAUSE frames received from the entity at the other end of the Ethernet link must implement flow control by halting or resuming transmitted traffic. The TXXG block provides the means for this to happen: pause timer values extracted from received PAUSE frames can be input to the TXXG along with a notification signal, and will cause the TXXG block to stop or restart traffic as required at the proper boundaries.
- Transmit Statistics support. After each data or PAUSE frame has been transmitted, whether successfully or unsuccessfully, the TXXG block outputs a Statistics vector that signals the Status of the transmission. This Statistics vector is expected to be used by an external unit to update appropriate Statistics counters. These counters in turn can be used to implement Standard Ethernet MIBs for link management purposes.

Downloaded by Content Agent for Partner Inc. on Wednesday, 07 February, 2007 06:39:32 PM

- Configuration and Status maintenance. The interframe gap, preamble, FCS generation, and error checking features of the TXXG can be configured by means of internal configuration registers accessible via an ECBI bus interface.

The following sections will describe the functionality of each sub-block in more detail.

10.15.2 MAC Outgoing Flow Control State Machine

This State-machine monitors a high watermark FIFO threshold level indication from the IFLX or the external PAUSE pin, and will issue a request to the MAC Core to transmit a MAC Control PAUSE frames when required. When the MAC Core acknowledges this request, this State-machine will build the MAC Header and Data frame, and present it to the MAC Core for transmission. The Pause Parameter value can be programmed using an internal register. Pause Control frames are injected (by the MAC Core) at the rate programmed using the PAUSE Timer Interval register after the transmission of the current frame. This periodic transmission will request the far end to XOFF for the duration of the timer.

When sending out Control PAUSE frames and a low watermark FIFO indication from the IFLX is detected, the MAC core inserts a PAUSE control frame with a pause timer value of 0 after the transmission of the current frame. This transmission will request the far end to immediately XON.

The transmit MAC can also be directed by the ingress MAC to halt data transmission to the line side. If the receive MAC interprets a pause frame, the transmit MAC will be notified and also given a timer value. The transmit MAC will halt transmission of data until the pause timer value has expired. While the transmit MAC is halted, the external PAUSED pin to the line side will be asserted.

10.15.3 MAC Core

The MAC Core is the heart of the TXXG and implements the principal functions of the IEEE 802.3 MAC layer. It consists of a State machine, data steering and encapsulation logic, together with a CRC generator for computing the Standard 32-bit IEEE FCS.

At any time, it may be operating in one of three modes:

- Frame transmission disabled.
- MAC Flow Control packet transmission enabled, when the MAC Incoming Flow Control State machine indicates the transmitter is PAUSED.
- MAC Flow Control and EFLX-source packet transmission enabled, with priority being given to MAC Flow Control packet transmission, when not PAUSED.

During operation, the MAC Core waits until a frame is available to be sent, the downstream is requesting a packet for transmission and the inter-packet gap timer (IPG timer) is not active. It then generates the requisite preamble and SFD, and then transfers frame data from the packet source, 64 bits at a time. The SOF/EOF, error and valid signals supplied with the data words are processed to determine frame boundaries and control the CRC generator, and also to determine intra-frame zero-padding and post-frame IPG spacing. The processed 64-bit data words are output to the downstream block.

Downloaded by Intertech Partners Inc on Thursday, February 07, 2008 06:59:52 PM

At the end of each frame transmission, the MAC Core inserts an inter-frame gap of the required amount before starting the transfer of the next frame. Note that the inter-frame gap is counted in units of bytes rather than absolute time, permitting frame timing to be done differently based on the application.

After each packet transmit is completed, the MAC Core builds and transfers a Transmit Statistics Vector to the MSTAT block.

10.15.4 CRC Generator

The CRC Generator performs a CRC-32 calculation on the whole Ethernet frame using the standard Ethernet polynomial. A parallel implementation of the CRC polynomial is used. The result is optionally prepended to the frame.

10.16 Transmit 64B66B Encoder (T64B66B)

The Transmit 64B/66B Processor (T64B66B) implements the IEEE 802.3ae 10 Gigabit Ethernet PCS Sub-layer. It receives frames from the Transmit 10G Ethernet MAC (TXXG) block, scrambles the frames and 64B/66B encodes the scrambled stream. The resulting encoded stream is passed to the THPP blocks. The T64B66B block is not used when processing ATM cells, GFP frames or POS packets.

The T64B66B implements the following principal functions:

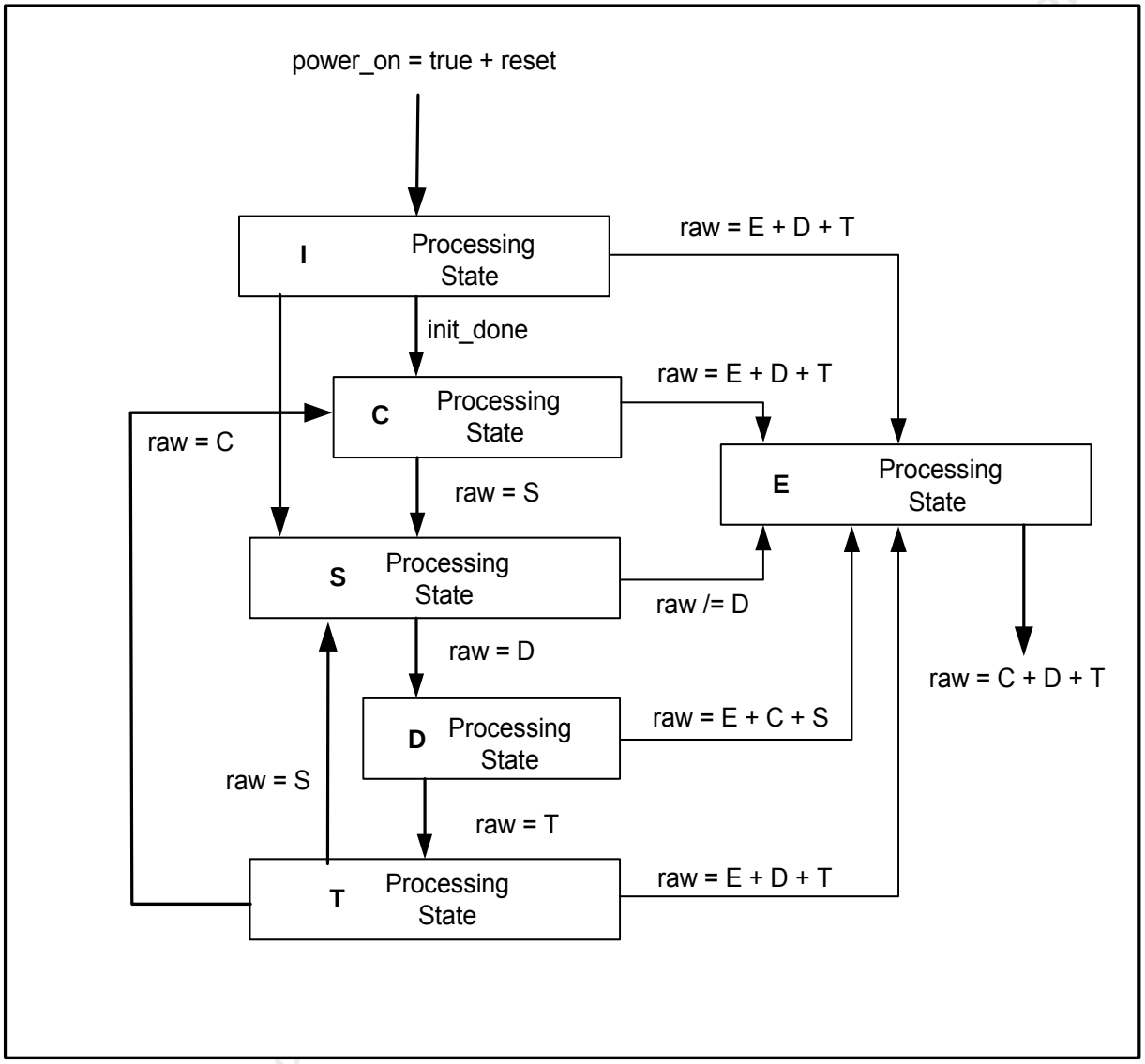
- Ethernet frame delineation
- Aligns to 32-bit SOP Boundaries
- 32 to 33 Gearbox
- 64B/66B data encoding
- Control Code Mapping
- Data Scrambling
- Bit within Byte Ordering Function
- Transmit Fault Signaling
- Transmit Jitter test pattern generator

10.16.1 TX PCS

The TX PCS contains a Finite State Machine, which sequences through the 6 basic states shown in Figure 25. It contains a scrambler based on $G(x) = 1 + X^{39} + X^{58}$. It provides all the timing and control necessary for capturing, aligning, and processing the upstream data. The decision(s) for the transmit state machine to leave or remain in a given state are based upon the IEEE 802.3ae standard. The TX PCS provides Jitter Test pattern generation as per IEEE 802.3ae standard.

Downloaded by Team Partminer Inc on Wednesday, 28 February, 2007 06:59:32 PM

Figure 25 TX Processing Steps For 66-Bit Codes



From Figure 25, the controller enters its Initialization (I) State during reset or during a power-up sequence. To exit the I State, the Input Controller must wait for the internal data formatter and barrel shifter to sequence completely through their first 33 clock processing cycle, it also may wait for the de-assertion of an overhead marker (depending on mode) from the downstream block and/or the assertion of a Control Detect indication from the Data Encoder Block. Given a successful execution of a proper initialization and the detection of the proper out-of-band control signals, the state machine will advance to its Control Code or (C) State. The C state processor will map only the incoming Control Codes. Upon detecting a valid SOP transition, the state machine advances to the S processing state.

Downloaded by

By looking at Figure 25, a typical state sequence can be defined as: S, D, and T. The Start of Packet (S) State is entered via detection of the SOP byte control indication. The Data (D) State can consist of multiple (N) 66-bit frames. The End of Packet (T) State is entered via detection of the EOP byte control indication. In this case, according to the IEEE 802.3ae specification, the outgoing EOP byte can occur in anyone of eight possible locations within a 66-bit frame. An errored sequence would be any other type of transition that doesn't follow the simple sequence of Start-of-Packet state to the Data Capture state to the End-of-Packet state. For example the following sequences: Start-of-Packet state to the End-of-Packet state, Start-of-Packet state to the Start-of-Packet state, End-of-Packet state to the Data Capture state, and Data Capture state to the Start-of-Packet state would be counted as errored sequences. After detection of an errored sequence the state machine always advances to the E state.

During any Errored state the proper errored frame will be sent downstream to the Line Interface. During a Receiver Error Event: Loss Of Signal (LOS), Remote Fault (RF), or Local Fault (LF) the Input Controller will immediately advance to the E state, where it will stay until the errored event is cleared. During LOS or LF the TX PCS will start sending Remote Fault Messages continuously downstream. During RF the TX PCS will only send IDLEs downstream.

10.16.2 Jitter Test Pattern Generator

When this is enabled via the JITT_PAT_EN (bit 6 of register 0x3080), the scrambler's normal input data is ignored and two possible patterns are instead generated. If JTST_PAT_SEL (bit 7 of register 0x3080) is set to zero a square wave signal of the wavelength defined by SWAVE_LEN+4 becomes the input to the scrambler. If instead JTST_PAT_SEL is set to one then a pseudo random signal is generated. This is done by:

1. Setting the scrambler's input to all zeros if the bit JDAT_PAT_SEL(bit 8 of register 0x3080) equals '0' or to the LF ordered set if JDAT_PAT_SEL equals '1'.

2. Seeding the scrambler every 128 blocks where the seed value repeats as follows:
   - Seed A -> Seed A inverse -> Seed B -> Seed B inverse -> Seed A …

10.17 Transmit Cell, Frame Processors (TCFP, TCFP-9953)

The Transmit Cell, Frame and Packet Processors (TCFP, TCFP-9953) provide ATM cell or POS packet delineation and processing. Note, these blocks are not used when processing IEEE 802.3ae 10 Gigabit Ethernet frames.

When the S/UNI 9953 device is configured for quad STS-48c (STM-16c) mode, four TCFP blocks are used, each processing an ATM cell or POS packet stream sourced from the Egress Flexible FIFO (EFLX).

When the S/UNI 9953 device is configured for STS-192c (STM-64c) mode, a single TCFP-9953 block is used to process an ATM cell or POS packet stream sourced from the Egress Flexible FIFO (EFLX).

Downloaded by [redacted] of Parminder Singh Wadhwa, 07 February, 2017, 16:09:32 EST

10.17.1 ATM Processing

In ATM mode, the TCFP-9953 (OR TCFP) provides rate adaptation via idle/unassigned cell insertion, provides HCS generation and insertion, and performs ATM cell scrambling.

ATM Idle/Unassigned Cell Generator

The Idle/Unassigned Cell Generator inserts idle or unassigned cells into the cell stream when enabled. Registers are provided to program the GFC, PTI, and CLP fields of the idle cell header and the idle cell payload. The idle cell HCS is automatically calculated and inserted.

ATM Scrambler

The Scrambler scrambles the 48-octet information field. Scrambling is performed using a parallel implementation of the self-synchronous scrambler ($x^{43} + 1$ polynomial) described in the ATM Forum ATM UNI 3.1 and ITU-T Recommendation I.432 specifications. The cell headers are transmitted unscrambled, and the scrambler may optionally be disabled.

ATM HCS Generator

The HCS Generator performs a CRC-8 calculation over the first four header octets. A parallel implementation of the polynomial, x^8+x^2+x+1, is used. The coset polynomial, $x^6+x^4+x^2+1$, is added (modulo 2) to the residue (if enabled). The HCS Generator optionally inserts the result into the fifth octet of the header.

An error insertion mechanism is provided for system diagnosis purposes. Error insertion is performed by inverting selected bits of the resulting HCS value before transmission. This will cause a HCS error to be detected by the eventual receiver.

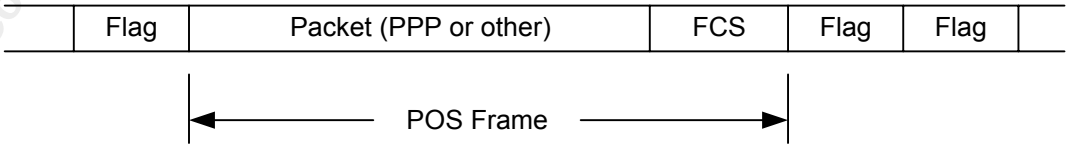
10.17.2 POS Processing

In POS mode the TCFP-9953 (OR TCFP) provides rate adaptation by transmitting flag sequences (0x7E) between packets, provides FCS generation and insertion, performs packet data scrambling, and provides performance monitoring functions.

POS PPP/HDLC Frame Generator

The POS Frame Generator creates the POS frames to be transmitted, with the format shown in Figure 26. Flags are inserted whenever the Transmit FIFO is empty and there is no data to transmit. When there is enough data to be transmitted, the block operates normally; it removes packet data from the Transmit FIFO and transmits it.

Figure 26 Packet Over SONET Frame Format



Downloaded by Content Team of Partner Inc on Wednesday, 07 February, 2007 10:59:32 PM

In the event of a FIFO underflow caused by the FIFO being empty while a packet is being transmitted, the packet is aborted by transmitting the Abort Sequence. The Abort Sequence consists of an Escape Control character (0x7D) followed by the Flag Sequence (0x7E). Bytes associated with this aborted frame are still read from the FIFO but are discarded and replaced with flag bytes in the outgoing data stream. If an overflow occurs, due to a failure in the FIFO Interface protocol, the data that would have caused the overflow is dropped. Transmission of data resumes when an *end of packet-start of packet* sequence is detected in the FIFO data stream.

The POS Frame Generator also performs Inter Packet Gapping. This operation consists of inserting a programmable number of flag bytes between each POS Frame transmission. This feature allows control of the effective data transmission rate of the system, if this is required.

POS FCS Generator

The FCS Generator performs a CRC-CCITT (TCFP only) or CRC-32 calculation on the whole POS frame, before byte stuffing and data scrambling. A parallel implementation of the CRC polynomial is used. The CRC algorithm for the frame checking sequence (FCS) field is either a CRC-CCITT (TCFP only) or CRC-32 function. The CRC-CCITT is two bytes in size and has a generating polynomial:

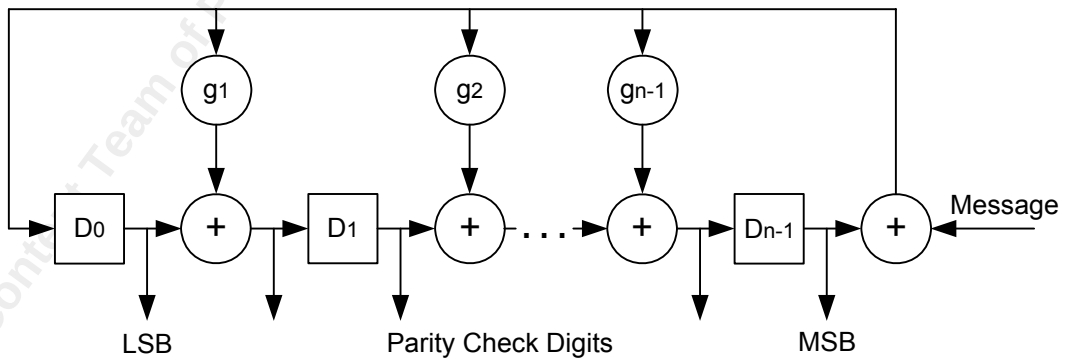
$G(x) = 1 + x^5 + x^{12} + x^{16}$

The CRC-32 is four bytes in size and has a generating polynomial:

$G(x) = 1 + x + x^2 + x^4 + x^5 + x^7 + x^8 + x^{10} + x^{11} + x^{12} + x^{16} + x^{22} + x^{23} + x^{26} + x^{32}$

The first FCS bit transmitted is the coefficient of the highest term. When transmitting a packet from the Transmit FIFO, the FCS Generator appends the result after the last data byte, before the closing flag. Note that the Frame Check Sequence is the one's complement of the CRC register after the calculation ends. FCS calculation and insertion can be disabled.

Figure 27 CRC Generator



Downloaded by Content Team of Partsinfinity.com Wednesday, February 14, 2007 06:53:30 PM

An error insertion mechanism is provided for system diagnosis purposes. Error insertion is performed by inverting selected bits in the resulting FCS value before transmission. This should cause the detection of a FCS Error by the eventual receiver.

POS Byte Stuffing

The POS Frame generator provides transparency by performing byte stuffing. This operation is done after the FCS calculation. Two characters are being escaped, the Flag Sequence (0x7E) and the Escape Character itself (0x7D). When a character is being escaped, it is XORed with 0x20 before transmission and preceded by the Control Escape (0x7D) character.

Table 7 Byte Stuffing

Original	Escaped
7E (Flag Sequence)	7D-5E
7D (Control Escape)	7D-5D
Abort Sequence	7D-7E

POS Data Scrambling

The Scrambler will optionally scramble the whole packet data, including the FCS and the flags. Scrambling is performed after the POS frame is formed using a parallel implementation of the self-synchronous scrambler polynomial, $x^{43}+1$. On reset, the scrambler is set to all ones to ensure scrambling on start-up. The scrambler may optionally be completely disabled. Data scrambling can provide for a more robust system by defeating the injection of hostile patterns into the data stream.

10.17.3 Transmit Path GFP Processing

In GFP mode, the TCFP-9953 provides rate adaptation via GFP idle frame insertion, provides optional cHEC, tHEC, eHEC and FCS calculation, and performs GFP Payload area scrambling.

The GFP Frame format is shown in Figure 19.

GFP Frame Length Checking

If the GFP frame length, as determined from the PLI field, is inconsistent with the corresponding EOP position the LEN_ERRI interrupt is asserted. The invalid frame is transmitted and will cause a loss of delineation at the receiver.

If the GFP frame length, as determined from the PLI field, is inconsistent with the EHDR_LEN[5:0] and FCS configuration parameters, the LEN_ERRI interrupt is asserted.

Idle Frame Generator

The Idle Frame Generator inserts idle GFP frames into the frame stream when no data is available from the upstream block in accordance with the rate adaptation function described later. An idle frame is a GFP frame consisting of the Core Header only, with a PLI value of zero. The GFP idle frame format is illustrated earlier.

Downloaded by Content Team of Pantronics on Wednesday, 07 February, 2007 09:32 PM

GFP Rate Adaptation

In GFP mode, the Rate Adaptation ensures that the downstream block is provided with frame data on demand.

In normal operation (XOFF set to logic 0), if there is frame data available, then this will be sent at the earliest opportunity. Between each frame a sequence of idle frames are inserted, the number of which is determined by the FLAG_IDLE[3:0] configuration parameter. Idle frames will continue to be sent until a new frame is available. Hence, the minimum number of idle frames inserted between user frames is determined by the FLAG_IDLE[3:0] value.

Prior to rate adaptation all GFP idle frames sourced from the FIFO Interface are dropped (deleted).

The Rate Adaptation mechanism does not provide any buffering. If there are any invalid bytes between frames, an idle frame may be inserted. If a contiguous user frame stream is input at the FIFO Interface, no idle frames are inserted.

If the XOFF configuration parameter is set to logic 1, the current frame transmission is completed and then idle frames are sent continuously.

HEC Generation

The TCFP-9953 optionally calculates and overwrites the various HEC fields in the GFP frame. This mechanism is controlled by the CHEC, THEC, EHEC and SHEC configuration parameters. The cHEC, tHEC, eHEC and sHEC are all calculated using the CRC-CCITT polynomial:

$$G(x) = 1 + x^5 + x^{12} + x^{16}$$

The positions of the cHEC, tHEC, eHEC and sHEC are shown in Figure 19. The eHEC position is determined by the EHDR_LEN[5:0] configuration parameter.

All HEC calculations use an initialization value of zero.

All HECs can be independently corrupted (for diagnostic purposes) using the CHEC_CRPT_EN, THEC_CRPT_EN, EHEC_CRPT_EN, SHEC_CRPT_EN and DCRC[15:0] configuration parameters. When a HEC_CRPT_EN configuration bit is set, that HEC will be XORed with the value in the DCRC[15:0] configuration parameter.

Core Header DC Balancing

The TCFP-9953 optionally performs Core Header DC Balancing. When the CORE_DC configuration parameter is set to logic one, the Core Header is XORed with the value 0xB6AB31E0.

FCS Generation

The TCFP-9953 optionally generates and overwrites the FCS field (calculated over the GFP payload area field) into the GFP frame. This mechanism is controlled by the FCS configuration parameter. The FCS is calculated using the CRC-32 polynomial:

Downloaded by Component Team @ Parsmin Inc on Wednesday, 17 February, 2010 07:55:32 PM

$$G(X) = 1 + x + x^2 + x^4 + x^5 + x^7 + x^8 + x^{10} + x^{11} + x^{12} + x^{16} + x^{22} + x^{23} + x^{26} + x^{32}$$

The insertion positions of the FCS are shown in Figure 19.

The FCS calculation has an initialization value of all ones.

The FCS calculation result value is logically inverted prior to being written into the transmission stream.

The FCS can be deliberately corrupted (for diagnostic purposes) using the FCS_CRPT_EN and DCRC[7:0] configuration parameters. When the FCS_CRPT_EN configuration bit is set, each byte of the FCS will be XORed with the value in the DCRC[7:0] configuration parameter.

Scrambler

Self-synchronous scrambling of the GFP Payload Area and FCS fields is then performed when the configuration parameter SCRAMBLE is set to logic one. The scrambler uses the polynomial:

$$G(x) = 1 + x^{43}$$

10.18 Transmit High Order Path Processor (THPP)

The Transmit High Order Path Processor (THPP) block inserts the path overhead bytes in the transmit data stream and inserts a valid pointer in the H1 and H2 pointer locations. The THPP receives a filled SPE from

1. The Transmit Cell Frame Processors (TCFP, TCFP-9953) when the S/UNI 9953 is configured for ATM or POS or GFP modes or

2. The Transmit 64B/66B Processor (T64B66B) when the S/UNI 9953 is configured for IEEE 802.3ae 10G Ethernet operation.

After the THPP processes the stream, it provides the stream to the Output APS Interface and the TRMP block.

The THPP accumulates the path BIP-8 errors detected by the RHPP during the last receive frame. The path BIP-8 errors are returned to the far end as path remote error indication (REI-P) during the next transmit frame. Because the RHPP and the THPP are in two different clock domains, none, one or two path BIP-8 errors can be accumulated per transmit frame. The minimum value between the maximum REI-P and the accumulator count is returned as the path REI in the G1 byte. Optionally, block BIP-8 errors can be accumulated.

Downloaded by Content Team of Pattmar Inc on Wednesday, 07 February 2007 06:59:32 PM

The THPP serially inputs all the path overhead (POH) bytes from the TPOH port. The POH bytes must be input in the same order that they are transmitted (J1, B3, C2, G1, F2, H4, F3, K3 and N1). TPOHCLK is the generated output clock used to provide timing for the TPOH port. TPOHCLK is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. Sampling TPOHFP high with the rising edge of TPOHCLK identifies the MSB of the first J1 byte. TPOHEN port is used to validate the byte insertion on a byte per byte basis. When TPOHEN is sampled high on the MSB of the serial byte, the serial byte is inserted. When TPOHEN is sampled low on the MSB of the serial byte, the serial byte is discarded.

The THPP calculates the path BIP-8 error detection code on the transmit data stream. The path BIP-8 byte is calculated on all the payload bytes. The path BIP-8 byte is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 error detection code is inserted in the B3 byte of the following frame.

Table 8 POH Insertion Priority

Byte	Highest Priority					Lowest Priority
J1	J1 pass through (PAIS=1)	Path trace buffer (PTBJ1=1)	J1 ind. reg. (SRCJ1=1)		TPOH (TPOHEN=1)	J1 pass through
B3	B3 pass through (PAIS=1)			Calculated B3 XOR TPOH (TPOHEN=1 AND B3MASKEN=1)	TPOH (TPOHEN=1)	Calculated B3 XOR B3MASK
C2	C2 pass through (PAIS=1)	C2 ind. reg. (SRCC2=1)			TPOH (TPOHEN=1)	C2 pass through
G1	G1 pass through (PAIS=1 OR IBER=1)	PRDI[2:0] and PREI[3:0] (ENG1REC=1)	G1 ind. reg. (SRCG1=1)		TPOH (TPOHEN=1)	G1 pass through
F2	F2 pass through (PAIS=1)	F2 ind. reg. (SRCF2=1)			TPOH (TPOHEN=1)	F2 pass through
H4	H4 pass through (PAIS=1)		H4 ind. reg. (SRCH4=1)	H4 pass through XOR TPOH (TPOHEN=1 AND H4MASK=1)	TPOH (TPOHEN=1)	H4 pass through
Z3	Z3 pass through (PAIS=1)	Z3 ind. reg. (SRCZ3=1)			TPOH (TPOHEN=1)	Z3 pass through
Z4	Z4 pass through (PAIS=1)	Z4 ind. reg. (SRCZ4=1)			TPOH (TPOHEN=1)	Z4 pass through
Z5	Z5 pass through (PAIS=1)	Z5 ind. reg. (SRCZ5=1)			TPOH (TPOHEN=1)	Z5 pass through

Downloaded by Content Team of Partsinel.com on Wednesday, 07 February, 2007 (GMT-08:00)

10.19 Section/Path Transmit Trail Trace Processor (TTTP)

The Section/Path Transmit Trail Trace Processor (TTTP) block generates the Section/Path trail trace messages to be transmitted. The TTTP can generate a 16 or 64 byte trail trace message. The message is sourced from an internal RAM and must have been previously written by an external microprocessor. Optionally, the trail trace message can be reduced to a single continuous trail trace byte.

The trail trace message must include synchronization because the TTTP does not add synchronization. The synchronization mechanism is different for a 16 bytes message and for a 64 bytes message. When the message is 16 bytes, the synchronization is based on the MSB of the trail trace byte. Only one of the 16 bytes has MSB set high. The byte with its MSB set high is considered the first byte of the message. When the message is 64 bytes, the synchronization is based on the CR/LF (CR = 0Dh, LF = 0Ah) characters of trail trace message. The byte following the CR/LF bytes is considered the first byte of the message.

To avoid generating an unstable/mismatch message, the TTTP forces the message to all zeros while the microprocessor updates the internal RAM.

10.20 Transmit Regenerator Multiplexer Processor (TRMP)

The Transmit Regenerator and Multiplexer Processor (TRMP) block inserts the transport overhead bytes in the transmit data stream. The TRMP sources transmit data from either the Transmit High Order Path Processor (THPP) or the Input APS Interface. It assumes that the sourced data already has been SONET/SDH path processed. The TRMP performs transport overhead insertion and provides the resulting stream to the STLI block.

The TRMP accumulates the line BIP-8 errors detected by the RRMP during the last receive frame. The line BIP-8 errors are returned to the far end as line remote error indication (REI-L) during the next transmit frame. Because the RRMP and the TRMP are in two different clock domains, zero, one, or two line BIP-8 errors can be accumulated per transmit frame. The minimum value between the maximum REI-L provide in Table 9 and the accumulator count is returned as the line REI-L in the M1 byte of STS-1 (STM-0) #3. Optionally, block BIP-24 errors can be accumulated. For STS-48c (STM-16c) and STS-192c (STM-64c), the maximum single BIP-8 error count is 0xFF and 0xFF respectively while the maximum block BIP-24 error count is 0x10 and 0x40 respectively.

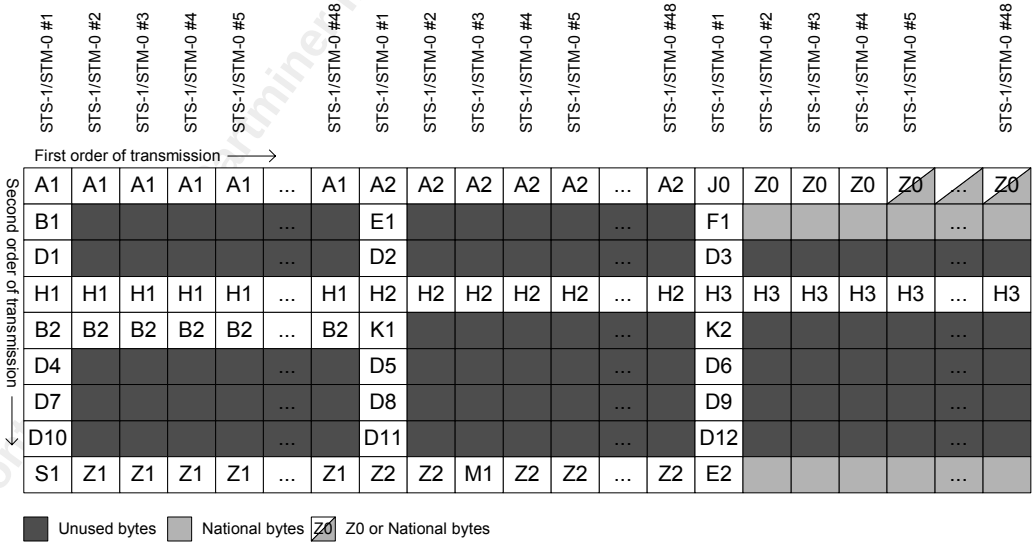
Downloaded by Content Team (Beijing) on Tuesday, 07 February 2012 06:59:00 PM

The TRMP serially inputs all the transport overhead (TOH) bytes from the TTOH port. The TOH bytes must be input in the same order that they are transmitted (A1, A2, J0/Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, S1/Z1, Z2/M1/Z2 and E2). Figure 28, Figure 29 and Figure 30 show the transport overhead bytes on TTOH1-4 for the case where the S/UNI 9953 is processing a quad OC-48/STS-48/STM-16 and an OC-192/STS-192/STM-64 data streams. Transport overhead columns are labeled accord to the order of arrival of the corresponding STS-1/STM-0 time-slots. These figures do not show the bit multiplexing structure used to serially insert the transport overhead on the TTOH ports. Each processing TRMP inserts serially an STS-12/STM-4 worth of transport overhead. Each TTOH port carries an STS-48/STM-16 worth of transport overhead. This stream is de-multiplexed to feed four TRMP blocks. Refer to the Functional Timing section for a detailed description of the multiplexing structure. TTOHCLK is the generated output clock used to provide timing for the TTOH port. TTOHCLK is a nominal 82.94 MHz clock generated by gapping a 103.68 MHz clock. Sampling TTOHFP high with the rising edge of TTOHCLK identifies the MSB of the first A1 byte. TTOHEN port is used to validate the byte insertion on a byte per byte basis. When TTOHEN is sampled high on the MSB of the serial byte, the serial byte is inserted. When TTOHEN is sampled low on the MSB of the serial byte, the serial byte is discarded.

Table 9 Maximum Line REI Errors per Transmit Frame

SONET/SDH	Maximum single BIP-8 errors LREIBLK=0	Maximum block BIP-24 errors LREIBLK=1
STS-48/STM-16	1111 1111	0001 0000
STS-192/STM-64	1111 1111	0100 0000

Figure 28 STS-48 (STM-16) on TTOH 1-4



Downloaded by Conexant Inc on Wednesday, 07 February, 2007 6:08:42 PM

Figure 29 STS-192 (STM-64) on TTOH1

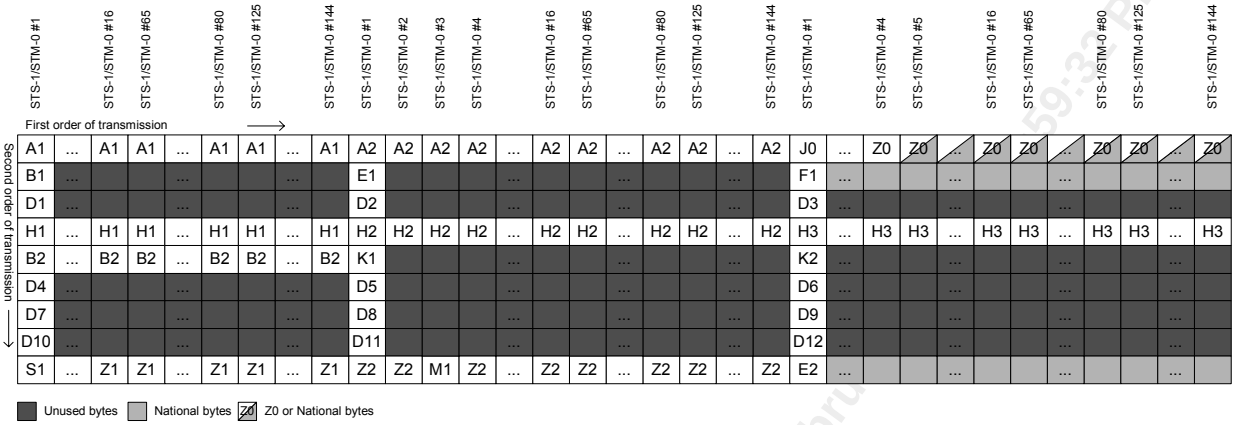
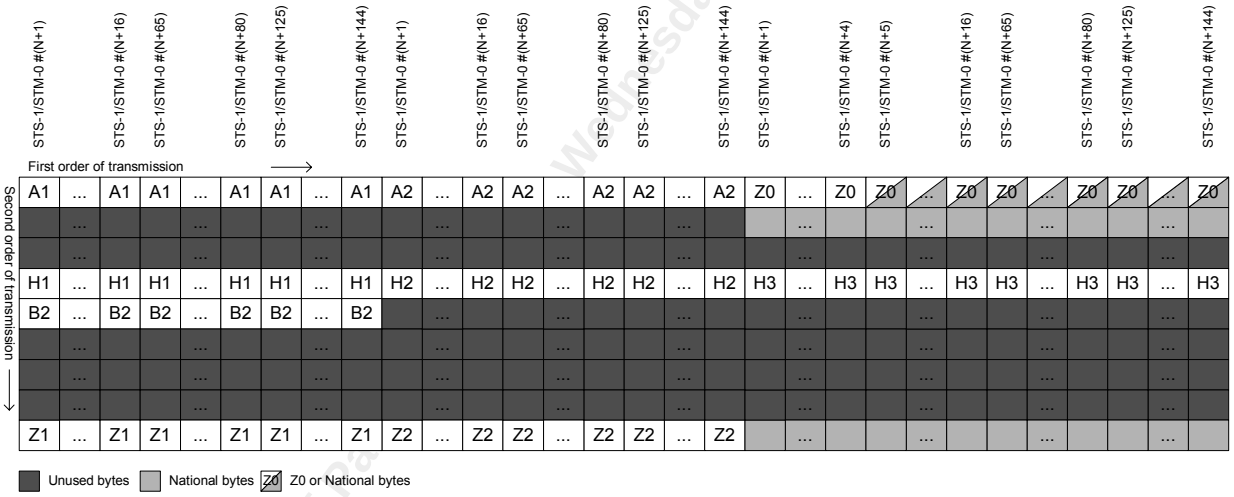


Figure 30 STS-192 (STM-64) on TTOH2-4



=16 for TOH2, N=32 for TOH3, N=48 for TTOH4

The TRMP also inserts most of the transport overhead bytes from internal registers. Since there are multiple sources for the same overhead byte, the TOH bytes must be prioritized according to Table 10 TOH Insertion Priority

before being inserted into the data stream.

Downloaded by Conexant Team of Pa... Wednesday, 07 Febru... 59:32 PM

Table 10 TOH Insertion Priority

BYTE	HIGHEST priority						LOWEST priority
A1		76h (A1ERR=1)	F6h (A1A2EN=1)	TTOH (TTOHEN=1)			A1 pass through
A2			28h (A1A2EN=1)	TTOH (TTOHEN=1)			A2 pass through
J0	STS-1/STM-0 # (J0Z0INCEN=1)	J0[7:0] (TRACEEN=1)	J0V (J0REGbEN=1)	TTOH (TTOHEN=1)			J0 pass through
Z0	STS-1/STM-0 # (J0Z0INCEN=1)		Z0V (Z0REGbEN=1)	TTOH (TTOHEN=1)			Z0 pass through
B1				Calculated B1 xor TTOH (TTOHEN=1 & B1MASKEN=1)			Calculated B1 xor B1MASK
				TTOH (TTOHEN=1 & B1MASKEN=0)			
E1			E1V (E1REGbEN=1)	TTOH (TTOHEN=1)			E1 pass through
F1			F1V (F1REGbEN=1)	TTOH (TTOHEN=1)			F1 pass through
D1-D3			D1D3V (D1D3REGbEN=1)	TTOH (TTOHEN=1)	TSLD_VAL (TSLDEN=1)		D1-D3 pass through
H1				H1 pass through xor TTOH (TTOHEN=1 & HMASKEN=1)			H1 pass through xor H1MASK
				TTOH (TTOHEN=1 & HMASKEN=0)			
H2				H2 pass through xor TTOH (TTOHEN=1 & HMASKEN=1)			H2 pass through xor H2MASK
				TTOH (TTOHEN=1 & HMASKEN=0)			
H3				TTOH (TTOHEN=1)			H3 pass through
B2				Calculated B2 xor TTOH (TTOHEN=1 & B2MASKEN=1)			Calculated B2 xor B2MASK
				TTOH (TTOHEN=1 & B2MASKEN=0)			
K1		APS[15:8] (APSEN=1)	K1V (K1K2REGbEN=1)	TTOH (TTOHEN=1)			K1 pass through
K2		APS[7:0] (APSEN=1)	K2V (K1K2REGbEN=1)	TTOH (TTOHEN=1)			K2 pass through

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:21

BYTE	HIGHEST priority						LOWEST priority
D4-D12			D4D12V (D4D12REGbEN=1)	TTOH (TTOHEN=1)		TLD_VAL (TLDEN=1)	D4-D12 pass through
S1			S1V (S1REGbEN=1)	TTOH (TTOHEN=1)			S1 pass through
Z1			Z1V (Z1REGbEN=1)	TTOH (TTOHEN=1)			Z1 pass through
Z2			Z2V (Z2REGbEN=1)	TTOH (TTOHEN=1)			Z2 pass through
M1			LREI[7:0] (LREIEN=1)	TTOH (TTOHEN=1)			M1 pass through
E2			E2V (E2REGbEN=1)	TTOH (TTOHEN=1)			E2 pass through
National			NATIONALV (NATIONALEN=1)	TTOH (TTOHEN=1)			National pass through
Unused			UNUSEDV (UNUSEDEN=1)	TTOH (TTOHEN=1)			Unused pass through
PLD							PLD pass through

The Z0DEF register bit defines the Z0/NATIONAL growth bytes for row #1. When Z0DEF is set to logic one, the Z0/NATIONAL bytes are defined according to ITU. When Z0DEF is set to logic zero, the Z0/NATIONAL bytes are defined according to Telcordia.

Table 11 Z0/National Growth Bytes Definition for Row #1

TRMP Mode	Type	Z0DEF = 1	Z0DEF = 0
Master mode process STM-4 #1 in STM-16 (STM-64)	Z0	From STS-1/STM-0 #2 to #4	From STS-1/STM-0 #2 to #12
	National	From STS-1/STM-0 #5 to #12	None
Slave mode process STM-4 #2 - #4 (#16) in STM-16 (STM-64)	Z0	From STS-1/STM-0 #1 to #4	From STS-1/STM-0 #1 to #12
	National	From STS-1/STM-0 #5 to #12	None

The H1, H2, B1 and B2 bytes input from the TTOH port are inserted or are used as a mask to toggle bits in the corresponding H1, H2, B1 and B2 bytes depending on the HMASK, B1MASK and B2MASK register bits of the TRMP Error Insertion register. When the HMASK, B1MASK or B2MASK register bit is set low and TTOHEN is sampled high on the MSB of the serial H1, H2, B1 or B2 byte, the serial byte is inserted in place of the corresponding byte. When the HMASK, B1MASK or B2MASK register bit is set high and TTOHEN is sampled high on the MSB of the serial H1, H2, B1 or B2 byte, the serial byte is XOR with the corresponding path payload pointer (already in the data stream) or the calculated BIP-8 byte before being inserted.

The TRMP inserts the APS bytes detected by the RRMP during the last receive frame. The APS bytes are returned to the far end by the TRMP during the next transmit frame. Because the RRMP and the TRMP are in two different clock domains, none, one or two APS bytes can be sampled per transmit frame. The last received APS bytes are transmitted.

Downloaded by Content Delivery Solutions LLC on Wednesday, 07 February, 2007 06:59:22

The TRMP inserts the line remote defect indication (RDI-L) into the data stream. When line RDI must be inserted, the 110 pattern is inserted in bits 6, 7, and 8 of the K2 byte of STS-1 (STM-0) #1. Line RDI insertion has priority over TOH byte insertion. The TRMP also inserts the line alarm indication signal (AIS-L) into the data stream. When line AIS must be inserted, all ones are inserted in the line overhead and in the payload (all bytes of the frame except the section overhead bytes). Line AIS insertion has priority over line RDI insertion and TOH byte insertion.

The TRMP calculates the line BIP-8 error detection codes on the transmit data stream. One line BIP-8 error detection code is calculated for each of the constituent STS-1 (STM-0). The line BIP-8 byte is calculated on the unscrambled bytes of the STS-1 (STM-0) except for the 9 SOH bytes. The line BIP-8 byte is based on a bit interleaved parity calculation using even parity. For each STS-1 (STM-0), the calculated BIP-8 error detection code is inserted in the B2 byte of the following frame before scrambling. The TRMP optionally scrambles the transmit data stream.

The TRMP calculates the section BIP-8 error detection code on the transmit data stream. The section BIP-8 byte is calculated on the scrambled bytes of the complete frame. The section BIP-8 byte is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 error detection code is inserted in the B1 byte of STS-1 (STM-0) #1 of the following frame before scrambling.

10.21 SONET/SDH Transmit Line Interface (STLI)

The SONET/SDH Transmit Line Interface (STLI) allows the S/UNI 9953 to directly interface with external SERDES devices. The interface can operate in either OC-192 or quad OC-48 modes. All the I/O on this interface are Low Voltage Differential Swing (LVDS).

In OC-192 mode, the interface transmits 16-bit data at 622 Mbps together with a 622 MHz clock, re-timed from a 622 MHz input reference clock from the SERDES. This interface is compliant to the OIF99.102.5 SFI-4 interface.

In OC-48 mode, the interface transmits 4 independent channel, each transmitting 4-bit data at 622 Mbps together with a 622 MHz clock, re-timed from a 622 MHz input reference clock from the SERDES. This interface is compliant to the OIF99.102.5 SFI-4 interface.

10.22 SONET/SDH Alarm Reporting Controller (SARC)

The SARC block receives all the section, line, and path defects detected by the receive overhead processors and, according to user specific configuration, generates consequent action indications.

- Receive section alarm (RSALM) indication: RSALM is asserted when an OOF, LOF, LOS. AIS-L, RDI-L, APSBF, TIU-S, TIM-S, SDBER or SFBER defect is detected in the receive data stream. Configuration registers allow the user to remove any defect from the previous enumeration.

Downloaded by Content from Pericom Inc. on Wednesday, 17 February, 2010 06:59:42 AM

- Receive line AIS insertion (RLAISINS) indication: RLAISINS is asserted when an OOF, LOF, LOS. AIS-L, RDI-L, APSBF, TIU-S, TIM-S, SDBER or SFBER defect is detected in the receive data stream. Configuration registers allow the user to remove any defect from the previous enumeration.
- Transmit line RDI insertion (TLRDIINS) indication: TLRDIINS is asserted when an OOF, LOF, LOS. AIS-L, RDI-L, APSBF, TIU-S, TIM-S, SDBER or SFBER defect is detected in the receive data stream. Configuration registers allow the user to remove any defect from the previous enumeration.
- Receive path alarm (RPALM) indication: RPALM is asserted when a RSALM, MSRSALM, AIS-P, LOP-P, PLU-P. PLM-P, UNEQ-P, PDI-P, RDI-P, ERDI-P, TIU-P or TIM-P defect is detected in the receive data stream. Configuration registers allow the user to remove any defect from the previous enumeration.
- Receive path alarm insertion (RPAISINS) indication: RPAISINS is asserted when a RLAISINS, MSRLAISINS, AIS-P, LOP-P, PLU-P. PLM-P, UNEQ-P, PDI-P, RDI-P, ERDI-P, TIU-P or TIM-P defect is detected in the receive data stream. Configuration registers allow the user to remove any defect from the previous enumeration.
- Transmit path ERDI insertion (TPERDIINS[2:0]) indication: TPERDIINS[2:0] is updated when a PLU-P, PLM-P, TIU-P, TIM-P, UNEQ-P, LOP-P or a AIS-P defect is detected in the receive data stream. Configuration registers allow the user to remove any defect from the previous enumeration.

10.23 SONET/SDH In-band Error Report Processor (SIRP)

The SIRP block is used for error reporting from a remote APS protect mate when operating as the working mate under a failure condition. When in the failure condition, the remote protect mate performs section, line and path termination and passes the expected REI-P and RDI-P indications back to the working mate in-band in the G1 byte via its output APS port. The SIRP block processes remote alarm indications in the SONET/SDH data stream from the Input APS port. The SIRP in the companion-working mate can be configured to extract remote defect indications (RDI) and remote error indications (REI) from an STS-48c (STM-16c) or STS-192c (STM-64c) incoming data stream. Accumulated remote error indications and remote defect indications are reported to the THPP block. Both RDI and extended RDI modes are available. The RDI report can be configured to be maintained asserted for at least 10 frames or 20 frames.

10.24 SONET/SDH Transport and Path Overhead Ports

The PM5390 device contains ports in both transmit and receive directions that optionally allow serial insertion and extraction of the SONET/SDH overhead bytes. The ports are flexible in the way they may be used. One port is designated as the Transport Overhead (TOH) port, and the other as the Path Overhead (POH) port. These exist in both transmit and receive directions, and thus are referred to as RTOH, RPOH, TTOH, and TPOH. These ports have clock and control pins, as well as the serial data.

Downloaded by [illegible] on Wednesday, 01 February 2017 05:55:32 PM

The TOH ports may be configured to access either all of the transport overhead bytes, just the section DCC bytes (D1-D3), or just the line DCC bytes (D4-D12). Similarly, the POH ports may be configured to access either all the path overhead bytes, just the section DCC bytes (D1-D3), or the line DCC bytes (D4-D12). Each port is configurable independently. Additionally, either port may be disabled completely if not used in order to reduce power.

When accessing either the line DCC, section DCC, path OH, or transport OH, the relevant interface clocks will operate at 192KHz, 576KHz, a gapped 25.92MHz, and a gapped 103.68MHz respectively.

10.25 Management Statistics (MSTAT)

The MSTAT block is used to accumulate Ethernet specific counts used for supporting management agents such RMON, SNMP, and Ether-like interfaces. The MSTAT supports full system probing capability via the use of full counter snapshot to shadow registers. Incorporated into the MSTAT block is a fully programmable interrupt array enabling per counter rollover monitoring with interrupt reporting. Each MSTAT counter is 40 bits wide.

10.25.1 Receive Statistics Counters

With the Receive Statistics, there are 30 corresponding counters. They are defined in Table 12.

Table 12 Receive Statistics Counters

Name of Counter
FramesReceivedOK
OctetsReceivedOK
FramesReceived
OctetsReceived
UnicastFramesReceivedOK
MulticastFramesReceivedOK
BroadcastFramesReceivedOK
TaggedFramesReceivedOK
PAUSEMACControlFrameReceived
MACControlFrameReceived
FrameCheckSequenceErrors
FramesLostDueToInternalMACError
SymbolError
InRangeLengthErrors
FramesTooLongErrors
Jabbers
Fragments
UndersizedFrames
ReceiveFrames64Octets
ReceiveFrames65to127Octets

Downloaded by [redacted] Gardner Inc on Wednesday, 07-February, 2007 16:59:32 EST

Name of Counter
ReceiveFrames128to255Octets
ReceiveFrames256to511Octets
ReceiveFrames512to1023Octets
ReceiveFrames1024to1518Octets (includes Tagged frames of 1522 bytes)
ReceiveFrames1519toMAXOctets
JumboOctetsReceivedOK
FilteredOctets
FilteredUnicastFrames
FilteredMulticastFrames
FilteredBroadcastFrames

10.25.2 Transmit Statistics Counters

With the Transmit Statistics, there are 22 corresponding counters. They are defined in Table 13.

Table 13 Transmit Statistics Counters

Name of Counter
FramesTransmittedOK
OctetsTransmittedOK
OctetsTransmitted
FramesLostDueToInternalMACTransmissionError
TransmitSystemError
UnicastFramesTransmittedAttempted
UnicastFramesTransmittedOK
MulticastFramesTransmittedAttempted
MulticastFramesTransmittedOK
BroadcastFramesTransmittedAttempted
BroadcastFramesTransmittedOK
PAUSEMACCTRLFramesTransmitted
MACCTRLFramesTransmitted
TaggedFramesTransmittedOK
TransmittedFrames64Octets
TransmittedFrames65to127Octets
TransmittedFrames128to255Octets
TransmittedFrames256to511Octets
TransmittedFrames512to1023Octets
TransmittedFrames1024to1518Octets (includes Tagged frames of 1522 bytes)
TransmittedFrames1519toMAXOctets
JumboOctetsTransmittedOK

Downloaded by Cortina Systems Malaysia Inc on Wednesday, 07 February, 2007 06:39:32 PM

10.26 Management Data Interface

MDIO (management data input/output) provides communication between the host processor and an external physical device by means of a two-wire interface. The MDIO block generates a clock (MDC) by dividing down the internal XSBI interface clock to provide timing reference for transfer of information on the MDI and MDO signal.

MDIO provides a MII Management interface to transmit and receive management frame serially for the purpose of controlling the physical device and gathering status from the physical device. Synchronization bits, selection addresses, and control data and address to the external MII device are sent on the MDO. Status data is received on MDI. MDOEN is a tri-state driver enable for the MDO data. MDI and MDO are expected to be combined into a bi-directional pin external to this block. The port address bus PRTADR[4:0] is used to select one of the 32 unique port and the device address bus DEVADR[4:0] is used to select a particular external physical device with which to communicate.

10.27 WAN Interface Sub-layer (WIS) Test Patterns

WIS test patterns can be generated and checked when using the device in the 10GE-WAN mode of operation. Generated patterns can be either a square wave (over the entire SONET frame) or a mixed frequency pattern using PRBS-23 within the SPE, as defined in the IEEE 802.3 specification. The polynomial used is $x^{23} + x^{18} + 1$.

Additionally, the test pattern can be configured to fill the SPE with a PRBS-23 pattern, without alternate frame inversion and without resetting the pattern at the start of each frame.

Transmit and receive portions of the WIS can be placed in test pattern mode via register bits. When the WIS transmitter is placed in test pattern mode, data is not accepted from or forwarded to the PCS layer. The data traffic is sourced directly from the WIS sublayer and terminates at the WIS sublayer.

10.28 APS Serial Data Interface

The APS Serial Data Interface consists of input and output 777.6 Mbps serial TelecomBus used to communicate between a working and protect mate for APS applications. When configured for quad OC-48 mode, four 4 channel 777.6 Mbps serial TelecomBus are provided, one for each OC-48. When configured for OC-192 operation, one 16 channel 777.6 Mbps serial TelecomBus is provided.

The data transmitted and received by the PM5390 at the APS ports and by PMC-Sierra Chess-I fabric devices use 8B10B encoding. The J1 bytes are replaced by an 8B10B control character. The APS receivers in the PM5390 recognises the J1 control character for internal alignment. However, if the APS stream is carried over intermediary devices that are not capable of transporting 8B10B control characters, the J1 alignment between the Working and Protect PM5390 devices will be lost. To address this, the PM5390 provides an additional path that directs the receive APS stream to the High Order Path Processor (RHPP) blocks. The J1 byte alignments will be recovered via pointer processing of the H1/H2 bytes.

Downloaded by [illegible] Team Partitioner [illegible] on Wednesday, 07 February 2007, 16:59 GMT

10.28.1 Output APS Serial Data Interface (T8TE, APISO, TXLV)

The Output APS Serial Data Interface uses the sets of T8TE, APISO and TXLV blocks to transmit a SONET (SDH) stream to a working or protect mate. When operating in quad OC-48 mode, four sets of 4 are provided. When operating in OC-192 mode, one set of 16 is provided. Only the operation of a OC-48 stream is described below.

The SONET (SDH) stream is selected from either the THPP or SVCA block and serialized on a 777.6 Mbps serial TelecomBus. When the S/UNI 9953 is configured as the working mate, the Output APS Serial Data Interface selects the transmit path processed SONET (SDH) stream from the THPP block and transmits it through the 4 differential LVDS pairs, OAPS[n][4:1]+/- to the protect mate where the stream is line and section processed. When the S/UNI 9953 is configured as the protect mate, the Output APS Serial Data Interface selects receive path terminated SONET (SDH) stream from the SVCA block and transmit it through the 4 differential LVDS pairs, OAPS[N][4:1]+/- to the working mate. The working mate will then process the SONET (SDH) payload (ATM or POS) and pass the results to the system via the POSPHY Level 4 interface.

There are sixteen sets of T8TE, APISO and TXLV blocks. Each set implements one of 16 serial streams that make up the output serial TelecomBus. The T8TE block takes a SONET (SDH) stream and 8B/10B encodes it. The APISO block performs a parallel to serial conversion. The TXLV block is a differential LVDS transmitter.

10.28.2 Input APS Serial Data Interface (RXLV, DRU, R8TD)

The Input APS Serial Data Interface uses the sets of RXLV, DRU and R8TD blocks to receive a SONET (SDH) stream from a working or protect mate via a serial TelecomBus. When operating in quad OC-48 mode, four sets of 4 are provided. When operating in OC-192 mode, one set of 16 is provided. Only the operation of an OC-48 stream is described below.

The received SONET (SDH) OC-48/OC-192 stream is passed either to the RCFP, RCFP-9953, R64B66B or TRMP blocks for further processing. When the S/UNI 9953 is configured as the working mate and when a failure condition exists, a receive path processed SONET (SDH) stream is expected from the protect mate on the 4 differential LVDS pairs, IAPS[N][4:1]+/-. The S/UNI 9953 will pass this received stream to the RCFP, RCFP-9953 or R64B66B for payload processing. When the S/UNI 9953 is configured as the protect mate and when a failure condition exists, a transmit path processed SONET (SDH) stream is expected from the working mate on the 4 differential LVDS pairs, IAPS[N][4:1]+/-. The S/UNI 9953 will pass this received stream to the TRMP for SONET line and section insertion before it is transmitted.

There are sixteen sets of RXLV, DRU and R8TD blocks. Each set implements one of 16 serial streams that make up the input serial TelecomBus. The RXLV block is a differential LVDS receiver. The DRU recovers the 777.6 Mbps 8B/10B encoded serial stream and deserializes it for the R8TD block. The R8TD block converts the deserialized 8B/10B stream into a SONET (SDH) stream.

Downloaded by United Technical Publications Private Limited (Renesas) on 07 February 2020 at 06:59:12 PM

10.29 LVDS Transmit Reference (TXREF)

The TXLVREF provides an on-chip band gap voltage reference (0.80V ±5%) and a precision current to the TXLVs. The reference voltage is used to control the common-mode level of the TXLV output, while the reference current is used to control the output amplitude. The precision currents are generated by forcing the reference voltage across an external, off-chip 3.16kΩ (±1%) resistor. The resulting current is then mirrored through several individual reference current outputs, so each TXLV receives its own reference current.

10.30 Clock Synthesis Unit (CSU)

The CSU is a fully integrated clock synthesis unit. It generates low jitter multi-phase differential clocks at 777.6 MHz for the usage by the transmitter. The IAPSFPCLK is used as a jitter-free reference clock to the CSU.

10.31 JTAG Test Access Port Interface

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The S/UNI 9953 identification code is R53900CD hexadecimal, where R is revision dependent.

Generic JTAG support in the S/UNI 9953 is described in Application Note, PMC-2021518, "JTAG Test Features Description".

For specific JTAG support in the S/UNI 9953, refer to section 13.2

10.32 Microprocessor Interface

The Microprocessor Interface Block provides the logic required to interface the generic microprocessor bus with the normal mode and test mode registers within the S/UNI 9953. The normal mode registers are used during normal operation to configure and monitor the S/UNI 9953. The test mode registers are used to enhance the testability of the S/UNI 9953. The register set is accessed as shown in Table 14. The S/UNI 9953 uses an STM-4 processing slice architecture for line-side SONET/SDH OC-192 and quad OC-48 data streams processing. There are sixteen transmit STM-4 processing slices for processing the sixteen constituent STS-12/STM-4 in the transmit STS-192c/STM-64c (quad STS-48c/STM-16c) data stream(s) and sixteen receive STM-4 slices for the receive STS-192c/STM-64c (quad STS-48c/STM-16c) data stream(s) processing. The mapping between these STM-4 slices and the constituent STS-12/STM-4 data streams are described for both the OC-192 and quad OC-48 operation modes in sub-sections 10.32.1, 10.32.2, 10.32.3 and 10.32.4. The association of these sixteen STM-4 slices with the four STM-16 processing groups are also described. The master/slave configuration of these STM-4 slices and thus the SONET/SDH system blocks is described in these sub-sections. This information will assist in the interpretation of register description and how registers should be accessed in the S/UNI 9953.

Downloaded by [illegible] on Wednesday, 07 February 2007 08:[illegible] GMT

The register address space of the sixteen Receive STM-4 processing slices (#1 to #16) span the addresses A[14:8]=0**n**H where 0≤**n**≤15. The register address space of the sixteen Transmit STM-4 processing slices (#1 to #16) span the addresses A[14:8]=1**n**H where 0≤**n**≤15. The index **n** corresponds to slice number minus one (slice# - 1) for a particular slice. The address mappings are identical for each Receive/Transmit STM-4 processing slice.

The register address space of the four Receive STM-16 processing groups (#1 to #4) span the addresses A[14:8]=0**k**H where 0≤**k**≤3. The register address space of the four Transmit STM-16 processing groups (#1 to #4) span the addresses A[14:8]=1**k**H where 0≤**k**≤3. The index **k** corresponds to group number minus one (group# -1) for a particular group. The address mappings are identical for each Receive/Transmit STM-16 processing group.

Addresses that are not shown are not used and must be treated as Reserved.

Table 14 Register Memory Map

Register Address A[14:0]	Register Description
0000H	S/UNI 9953 Identity, and Global Performance Monitor Update
0001H	S/UNI 9953 Master Reset and Configuration
0002H	S/UNI 9953 System-side Configuration
0003H	S/UNI 9953 Loop Back Configuration
0004H	S/UNI 9953 Transmit Control and Clock Enable
0005H	S/UNI 9953 Clock Monitors
0006H	S/UNI 9953 Line Analog Configuration
0007H	S/UNI 9953 Transmit and APS Configuration 1
0008H	S/UNI 9953 Transmit and APS Configuration 2
0009H	S/UNI 9953 Transmit and APS Configuration 3
000AH	S/UNI 9953 Transmit and APS Configuration 4
000BH	Software General Purpose (FREE[15:0])
000CH	APS Input TelecomBus Synchronization Delay
000DH	APS Output TelecomBus Synchronization Delay
000EH	S/UNI 9953 Diagnostics
000FH	S/UNI 9953 Identification Register
0010H	S/UNI 9953 Master Payload Interrupt Status
0011H	S/UNI 9953 Master FIFO/PL4 Interrupt Status
0012H	S/UNI 9953 Line Loop-back FIFO Interrupt Status
0013H	S/UNI 9953 Diagnostic Loop-back FIFO Interrupt Status
0014H	S/UNI 9953 PCS LOS Threshold
0015H	S/UNI 9953 PCS LOSB Threshold
0016H	S/UNI 9953 Input APS Frame Alignment Interrupt Status 1
0017H	S/UNI 9953 Input APS Frame Alignment Interrupt Status 2
0018H	S/UNI 9953 MDIO Command
0019H	S/UNI 9953 MMD PHY Address

Downloaded by Document Team of PMC-Sierra, Inc. on Thursday, 07 February, 2008 10:59:30 PM

Register Address A[14:0]	Register Description
001AH	S/UNI 9953 MMD Control Address Data
001BH	S/UNI 9953 MDIO Read Status Data
001CH	S/UNI 9953 PCS/LAN/MDIO Interrupt Enable and Control
001DH	S/UNI 9953 PCS/LAN/MDIO Interrupt Status
001EH	S/UNI 9953 PCS/LAN/MDIO Status
001FH	S/UNI 9953 Input APS and Loop-back Interrupt Enable
0**n**20H	S/UNI 9953 STM-4 Slice Interrupt Status
0**k**21H	S/UNI 9953 STM-64/STM-16 Stream Interrupt Status
0022H	S/UNI 9953 Overhead and DCC Configuration1
0023H	S/UNI 9953 Overhead and DCC Configuration2
0024H	S/UNI 9953 Power Down Configuration
0025H	S/UNI 9953 Overhead Port Control
0026H	S/UNI 9953 WIS PRBS-23 Pattern Mismatch Counter LSB
0027H	S/UNI 9953 WIS PRBS-23 Pattern Mismatch Counter MSB
0**n**28H	RLMPGM Configuration
0**n**29H	RLMPGM Monitor Synchronization
002A-002FH	S/UNI 9953 Reserved
0030-0031H	SRLI Reserved
0032H	SRLI Diagnostic 1
0033-0034H	SRLI Reserved
0035H	SRLI Diagnostic 2
0036-0037H	SRLI Reserved
0038H	SRLI Diagnostic 3
0039H	SRLI Synchronization Error Interrupt Status
003AH	SRLI Synchronization Error Status
003BH	SRLI Synchronization Error Interrupt Enable
003CH	SRLI Programmable Clock Configuration
003DH	SRLI Synchronize Error Configuration
003EH	SRLI Four Bytes De-Interleaver Control
003FH	SRLI Test
0**k**40H	SBER Configuration
0**k**41H	SBER Status
0**k**42H	SBER Interrupt Enable
0**k**43H	SBER Interrupt Status
0**k**44H	SBER SF BERM Accumulation Period (LSB)
0**k**45H	SBER SF BERM Accumulation Period (MSB)
0**k**46H	SBER SF BERM Saturation Threshold (LSB)
0**k**47H	SBER SF BERM Saturation Threshold (MSB)
0**k**48H	SBER SF BERM Declaring Threshold (LSB)
0**k**49H	SBER SF BERM Declaring Threshold (MSB)

Downloaded by Intelligent Team of Electronics on Wednesday, 7 February, 2007 06:59:32 PM

Register Address A[14:0]	Register Description
0**k**4AH	SBER SF BERM Clearing Threshold (LSB)
0**k**4BH	SBER SF BERM Clearing Threshold (MSB)
0**k**4CH	SBER SD BERM Accumulation Period (LSB)
0**k**4DH	SBER SD BERM Accumulation Period (MSB)
0**k**4EH	SBER SD BERM Saturation Threshold (LSB)
0**k**4FH	SBER SD BERM Saturation Threshold (MSB)
0**k**50H	SBER SD BERM Declaring Threshold (LSB)
0**k**51H	SBER SD BERM Declaring Threshold (MSB)
0**k**52H	SBER SD BERM Clearing Threshold (LSB)
0**k**53H	SBER SD BERM Clearing Threshold (MSB)
0**k**54- 0**k**5FH	SBER Reserved
0**n**60H	RRMP Configuration
0**n**61H	RRMP Status
0**n**62H	RRMP Interrupt Enable
0**n**63H	RRMP Interrupt Status
0**n**64H	RRMP Receive APS
0**n**65H	RRMP Receive SSM
0**n**66H	RRMP AIS Enable
0**n**67H	RRMP Section BIP Error Counter
0**n**68H	RRMP Line BIP Error Counter (LSB)
0**n**69H	RRMP Line BIP Error Counter (MSB)
0**n**6AH	RRMP Line REI Error Counter (LSB)
0**n**6BH	RRMP Line REI Error Counter (MSB)
0**n**6C- 0**n**6FH	RRMP Reserved
0**k**70H	RTTP Section Indirect Address
0**k**71H	RTTP Section Indirect Data
0**k**71H	(Indirect Register 00H): RTTP Section Trace Configuration
0**k**71H	(Indirect Register 40H to 7FH): RTTP Section Captured Trace
0**k**71H	(Indirect Register 80H to BFH): RTTP Section Accepted Trace
0**k**71H	(Indirect Register C0H to FFH): RTTP Section Expected Trace
0**k**72H	RTTP Section Trace Unstable Status
0**k**73H	RTTP Section Trace Unstable Interrupt Enable
0**k**74H	RTTP Section Trace Unstable Interrupt Status
0**k**75H	RTTP Section Trace Mismatch Status
0**k**76H	RTTP Section Trace Mismatch Interrupt Enable
0**k**77H	RTTP Section Trace Mismatch Interrupt Status

Downloaded by Content Team of Datasheet Catalog.com, Wednesday, 07 February, 2007 06:59:32 PM

Register Address A[14:0]	Register Description
0**k**78H	RTTP Path Indirect Address
0**k**79H	RTTP Path Indirect Data
0**k**79H	(Indirect Register 00H): RTTP Path Trace Configuration
0**k**79H	(Indirect Register 40H to 7FH): RTTP Path Captured Trace
0**k**79H	(Indirect Register 80H to BFH): RTTP Path Accepted Trace
0**k**79H	(Indirect Register C0H to FFH): RTTP Path Expected Trace
0**k**7AH	RTTP Path Trace Unstable Status
0**k**7BH	RTTP Path Trace Unstable Interrupt Enable
0**k**7CH	RTTP Path Trace Unstable Interrupt Status
0**k**7DH	RTTP Path Trace Mismatch Status
0**k**7EH	RTTP Path Trace Mismatch Interrupt Enable
0**k**7FH	RTTP Path Trace Mismatch Interrupt Status
0**n**80H	RHPP Indirect Address
0**n**81H	RHPP Indirect Data
0**n**81H	(Indirect Register 00H): RHPP Pointer Interpreter Configuration
0**n**81H	(Indirect Register 01H): RHPP Error Monitor Configuration
0**n**81H	(Indirect Register 02H): RHPP Pointer Value and ERDI
0**n**81H	(Indirect Register 03H): RHPP Captured and Accepted PSL
0**n**81H	(Indirect Register 04H): RHPP Expected PSL and PDI
0**n**81H	(Indirect Register 05H): RHPP Pointer Interpreter Status
0**n**81H	(Indirect Register 06H): RHPP Path BIP Error Counter
0**n**81H	(Indirect Register 07H): RHPP Path REI Error Counter
0**n**81H	(Indirect Register 08H): RHPP Path Negative Justification Event Counter
0**n**81H	(Indirect Register 09H): RHPP Path Positive Justification Event Counter
0**n**82H	RHPP Payload Configuration
0**n**83H	RHPP Reserved
0**n**84H	RHPP Path Interrupt Status
0**n**85H	RHPP Pointer Concatenation Processing Disable
0**n**86H	RHPP Path AIS and AISC Status
0**n**87H	RHPP Path LOP and LOPC Status

Downloaded by Content Team of PMC-Sierra on Wednesday, 7 February, 2007 06:59:32 PM

Register Address A[14:0]	Register Description
0**n**88H	RHPP Error Monitor Status
0**n**89H	RHPP Path AIS, AISC and PTRJE Enable
0**n**8AH	RHPP Path LOP and LOPC Interrupt Enable
0**n**8BH	RHPP Error Monitor Interrupt Enable
0**n**8CH	RHPP Path AIS, AISC, NJE and PJE Interrupt Status
0**n**8DH	RHPP Path LOP and LOPC Interrupt Status
0**n**8EH	RHPP Error Monitor Interrupt Status
0**n**8FH	RHPP Reserved
0**n**90H	SVCA Indirect Address
0**n**91H	SVCA Indirect Data
0**n**91H	(Indirect Register 00H): SVCA Positive Justifications Performance Monitor
0**n**91H	(Indirect Register 01H): SVCA Negative Justifications Performance Monitor
0**n**91H	(Indirect Register 02H): SVCA Diagnostic/Configuration
0**n**91H	(Indirect Register 03H): SVCA AU4 Pointer
0**n**92H	SVCA Payload Configuration
0**n**93H	SVCA Positive Pointer Justification Interrupt Status
0**n**94H	SVCA Negative Pointer Justification Interrupt Status
0**n**95H	SVCA FIFO Overflow Interrupt Status
0**n**96H	SVCA FIFO Underflow Interrupt Status
0**n**97H	SVCA Pointer Justification Interrupt Enable
0**n**98H	SVCA FIFO Interrupt Enable
0**n**99H	SVCA Pointer Justification Thresholds
0**n**9A- 0**n**9FH	SVCA Reserved
0**n**A0H	R8TD APS Control and Status
0**n**A1H	R8TD APS Interrupt Status
0**n**A2H	R8TD APS Line Code Violation Count
0**n**A3H	R8TD APS Analog Control 1
0**n**A4H	R8TD APS Analog Control 2
0**n**A5H	R8TD APS Analog Control 3
0**n**A6- 0**n**A7H	R8TD Reserved
0**n**A8H	IAMPGM Configuration
0**n**A9H	IAMPGM Monitor Synchronization
00AA- 00AFH	S/UNI 9953 Reserved
0**k**B0H	SARC Section Configuration
0**k**B1H	SARC Section RSALM Enable

Downloaded by Document Team of Partsim.com on Wednesday, 07 February, 2007 06:59:32 PM

Register Address A[14:0]	Register Description
0**k**B2H	SARC Section RLAISINS Enable
0**k**B3H	SARC Section TLRDIINS Enable
0**k**B4H	SARC Path Configuration
0**k**B5H	SARC Path RPALM Enable
0**k**B6H	SARC Path RPAISINS Enable
0**k**B7H	SARC LOP and AIS Pointer Status
0**k**B8H	SARC LOP and AIS Pointer Interrupt Enable
0**k**B9H	SARC LOP and AIS Pointer Interrupt Status
0**k**BA- 0**k**BFH	SARC Reserved
0**k**C0H	RCFP Configuration
0**k**C1H	RCFP Interrupt Enable and Status
0**k**C2H	RCFP Interrupt Indication and Status
0**k**C3H	RCFP Minimum Packet Length
0**k**C4H	RCFP Maximum Packet Length
0**k**C5H	RCFP LCD Count Threshold
0**k**C6H	RCFP Idle Cell Header and Mask
0**k**C7H	RCFP Receive Byte/Idle Cell Counter (LSB)
0**k**C8H	RCFP Receive Byte/Idle Cell Counter
0**k**C9H	RCFP Receive Byte/Idle Cell Counter (MSB)
0**k**CAH	RCFP Packet/Cell Counter (LSB)
0**k**CBH	RCFP Packet/ Cell Counter (MSB)
0**k**CCH	RCFP Receive Errored FCS/HCS Counter
0**k**CDH	RCFP Receive Aborted Packet Counter
0**k**CEH	RCFP Receive Minimum Length Packet Error Counter
0**k**CFH	RCFP Receive Maximum Length Packet Error Counter
00D0-00DFH	S/UNI 9953 Reserved
0**k**EA- 0**k**E8H	RXSTSI Reserved
00E9-00FFH	S/UNI 9953 Reserved
1000-1027H	S/UNI 9953 Reserved
1**n**28H	TLMPGM Configuration
1**n**29H	TLMPGM Reserved
102A-102FH	S/UNI 9953 Reserved
1030H	STLI Configuration
1031H	STLI PGM Clock Configuration
1032H	STLI INTERRUPT ENABLE
1033H	STLI INTERRUPT STATUS
1034-103FH	STLI Reserved
1040-105FH	S/UNI 9953 Reserved

Downloaded by Product Team of PMC-Sierra on Wednesday, 07 February, 2007 06:59:32 PM

Register Address A[14:0]	Register Description
1**n**60H	TRMP Configuration
1**n**61H	TRMP Register Insertion
1**n**62H	TRMP Error Insertion
1**n**63H	TRMP Transmit J0 and Z0
1**n**64H	TRMP Transmit E1 and F1
1**n**65H	TRMP Transmit D1D3 and D4D12
1**n**66H	TRMP Transmit K1 and K2
1**n**67H	TRMP Transmit S1 and Z1
1**n**68H	TRMP Transmit Z2 and E2
1**n**69H	TRMP Transmit H1 and H2 Mask
1**n**6AH	TRMP Transmit B1 and B2 Mask
1**n**6B- 1**n**6FH	TRMP Reserved
1**k**70H	TTTP Section Indirect Address
1**k**71H	TTTP Section Indirect Data
1**k**71H	(Indirect Register 00H): TTTP Section Trace Configuration
1**k**71H	(Indirect Register 40H to 7FH): TTTP Section Indirect Register
1**k**72- 1**k**73H	TTTP Section Reserved
1074- 1077H	S/UNI 9953 Reserved
1**k**78H	TTTP Path Indirect Address
1**k**79H	TTTP Path Indirect Data
1**k**79H	(Indirect Register 00H): TTTP Path Trace Configuration
1**k**79H	(Indirect Register 40H to 7FH): TTTP Path Indirect Register
1**k**7A- 1**k**7BH	TTTP Path Reserved
107C- 107FH	S/UNI 9953 Reserved
1**n**80H	THPP Configuration 1
1**n**81H	THPP Configuration 2
1**n**82H	THPP Transmit C2 and J1
1**n**83H	THPP Transmit F2 and G1
1**n**84H	THPP Transmit Z3 and H4
1**n**85H	THPP Transmit Z5 and Z4
1**n**86H	THPP Transmit B3MASK and Fixed Stuff Byte
1**n**87H	THPP Reserved
1088- 109FH	S/UNI 9953 Reserved

Downloaded by Document Team of PMC-Sierra, Inc. on Wednesday, 07 February, 2007 06:59:32 PM

Register Address A[14:0]	Register Description
1**n**A0H	T8TE APS Control and Status
1**n**A1H	T8TE APS Interrupt Status
1**n**A2H	T8TE APS TelecomBus Mode #1
1**n**A3H	T8TE APS TelecomBus Mode #2
1**n**A4H	T8TE APS Test Pattern
1**n**A5H	T8TE APS Analog Control
1**n**A6H	T8TE APS DTB Bus
1**n**A7H	T8TE Reserved
1**n**A8H	OAMPGM Configuration
1**n**A9H	OAMPGM Reserved
10AA-10AFH	S/UNI 9953 Reserved
1**k**B0H	SIRP Configuration Timeslot
1**k**B1-1**k**BBH	SIRP Reserved
1**k**BCH	SIRP Configuration
1**k**BD-1**k**BFH	SIRP Reserved
1**k**C0H	TCFP Configuration
1**k**C1H	TCFP Interrupt Indication
1**k**C2H	TCFP Idle/Unassigned ATM Cell Header
1**k**C3H	TCFP Diagnostics
1**k**C4H	TCFP Transmit Cell/Packet Counter (LSB)
1**k**C5H	TCFP Transmit Cell/Packet Counter (MSB)
1**k**C6H	TCFP Transmit Byte Counter (LSB)
1**k**C7H	TCFP Transmit Byte Counter
1**k**C8H	TCFP Transmit Byte Counter (MSB)
1**k**C9H	TCFP Aborted Packet Counter
1**k**CA-1**k**CFH	TCFP Reserved
10D0-10DFH	S/UNI 9953 Reserved
1**k**E0-1**k**E8H	TXSTSI Reserved
10E9-10FFH	S/UNI 9953 Reserved
2000-201FH	S/UNI 9953 Reserved
2020H	RCFP-9953 Configuration
2021H	RCFP-9953 Interrupt Enable and Status
2022H	RCFP-9953 Interrupt Indication
2023H	RCFP-9953 Min-Max Length/Bit Order/FCS Strip/Byte Count
2024H	RCFP-9953 Maximum Packet Length
2025H	RCFP-9953 LCD Count Threshold

Downloaded by [illegible] Team of Freedom [illegible] on Wednesday, 07 February, 2007 06:59:32 PM

Register Address A[14:0]	Register Description
2026H	RCFP-9953 Idle Cell Header and Mask Length
2027H	RCFP-9953 Receive Byte/Idle Cell-Packet Counter (LSB)
2028H	RCFP-9953 Receive Byte/Idle Cell-Packet Counter (ISB)
2029H	RCFP-9953 Receive Byte/Idle Cell-Packet Counter (MSB)
202AH	RCFP-9953 Receive Packet/Cell Counter (LSB)
202BH	RCFP-9953 Receive Packet/Cell Counter (MSB)
202CH	RCFP-9953 Receive Errored FCS/HCS Counter
202DH	RCFP-9953 Receive Aborted Packet Counter Error
202EH	RCFP-9953 Receive Minimum Length Packet Payload Error Counter
202FH	RCFP-9953 Receive Maximum Length Packet Payload Error Counter
2030-203FH	S/UNI 9953 Reserved
2040H	RXXG Configuration 1
2041H	RXXG Configuration 2
2042H	RXXG Configuration 3
2043H	RXXG Interrupt
2044H	RXXG Status
2045H	RXXG Maximum Frame Length
2046H	RXXG SA[15:0] – Station Address
2047H	RXXG SA[31:16] – Station Address
2048H	RXXG SA[47:32] – Station Address
2049H	RXXG Cut-Thru Threshold Select
204AH	RXXG Exact Match Address 0 Low Word
204BH	RXXG Exact Match Address 0 Mid Word
204CH	RXXG Exact Match Address 0 High Word
204DH	RXXG Exact Match Address 1 Low Word
204EH	RXXG Exact Match Address 1 Mid Word
204FH	RXXG Exact Match Address 1 High Word
2050H	RXXG Exact Match Address 2 Low Word
2051H	RXXG Exact Match Address 2 Mid Word
2052H	RXXG Exact Match Address 2 High Word
2053H	RXXG Exact Match Address 3 Low Word
2054H	RXXG Exact Match Address 3 Mid Word
2055H	RXXG Exact Match Address 3 High Word
2056H	RXXG Exact Match Address 4 Low Word
2057H	RXXG Exact Match Address 4 Mid Word
2058H	RXXG Exact Match Address 4 High Word
2059H	RXXG Exact Match Address 5 Low Word
205AH	RXXG Exact Match Address 5 Mid Word
205BH	RXXG Exact Match Address 5 High Word
205CH	RXXG Exact Match Address 6 Low Word

Downloaded by Content Team of Datasheet Catalog.com, Monday, 07 February 2007 06:59:32 PM

Register Address A[14:0]	Register Description
205DH	RXXG Exact Match Address 6 Mid Word
205EH	RXXG Exact Match Address 6 High Word
205FH	RXXG Exact Match Address 7 Low Word
2060H	RXXG Exact Match Address 7 Mid Word
2061H	RXXG Exact Match Address 7 High Word
2062H	RXXG Exact Match VID 0
2063H	RXXG Exact Match VID 1
2064H	RXXG Exact Match VID 2
2065H	RXXG Exact Match VID 3
2066H	RXXG Exact Match VID 4
2067H	RXXG Exact Match VID 5
2068H	RXXG Exact Match VID 6
2069H	RXXG Exact Match VID 7
206AH	RXXG Multicast HASH Low Word
206BH	RXXG Multicast HASH MidLow Word
206CH	RXXG Multicast HASH MidHigh Word
206DH	RXXG Multicast HASH High Word
206EH	RXXG Address Filter Control 0
206FH	RXXG Address Filter Control 1
2070H	RXXG Address Filter Control 2
2071H	RXXG Line Filter Error Counter
2072-207FH	RXXG Reserved
2080H	R64B66B Configuration
2081H	R64B66B Interrupt Enable
2082H	R64B66B Interrupt Status
2083H	R64B66B Status
2084H	R64B66B Error Frame Count
2085H	R64B66B Frame Lock Count
2086H	R64B66B Bit Error Count
2087H	R64B66B JITTER_CNT[15:0]
2088-208FH	R64B66B Reserved
2090-20FFH	S/UNI 9953 Reserved
2100H	MSTAT Control
2101H	MSTAT Counter Rollover 0
2102H	MSTAT Counter Rollover 1
2103H	MSTAT Counter Rollover 2
2104H	MSTAT Counter Rollover 3
2105H	MSTAT Interrupt Mask 0
2106H	MSTAT Interrupt Mask 1
2107H	MSTAT Interrupt Mask 2

Downloaded by Content Team of EasyDataSheet.com on 07 February, 2007 06:59:32 PM

Register Address A[14:0]	Register Description
2108H	MSTAT Interrupt Mask 3
2109H	MSTAT Counter Write Address
210AH	MSTAT Counter Write Data Low
210BH	MSTAT Counter Write Data Middle
210CH	MSTAT Counter Write Data High
210D-210FH	MSTAT Reserved
2110-2112H	MSTAT FramesReceivedOK
2114-2116H	MSTAT OctetsReceivedOK
2118-211AH	MSTAT FramesReceived
211C-211EH	MSTAT OctetsReceived
2120-2122H	MSTAT UnicastFramesReceivedOK
2124-2126H	MSTAT MulticastFramesReceivedOK
2128-212AH	MSTAT BroadcastFramesReceivedOK
212C-212EH	MSTAT TaggedFramesReceivedOK
2130-2132H	MSTAT PAUSEMACControlFrameReceived
2134-2136H	MSTAT MACControlFrameReceived
2138-213AH	MSTAT FrameCheckSequenceErrors
213C-213EH	MSTAT FramesLostDueToInternalMACError
2140-2142H	MSTAT SymbolError
2144-2146H	MSTAT InRangeLengthErrors
2148-214AH	MSTAT Reserved
214C-214EH	MSTAT FramesTooLongErrors
2150-2152H	MSTAT Jabbers
2154-2156H	MSTAT Fragments
2158-215AH	MSTAT UndersizedFrames
215C-215EH	MSTAT ReceiveFrames64Octets
2160-2162H	MSTAT ReceiveFrames65to127Octets
2164-2166H	MSTAT ReceiveFrames128to255Octets
2168-216AH	MSTAT ReceiveFrames256to511Octets
216C-216EH	MSTAT ReceiveFrames512to1023Octets
2170-2172H	MSTAT ReceiveFrames1024to1518Octets
2174-2176H	MSTAT ReceiveFrames1519toMAXOctets
2178-217AH	MSTAT JumboOctetsReceivedOK
217C-217EH	MSTAT FilteredOctets
2180-2182H	MSTAT FilteredUnicastFrames
2184-2186H	MSTAT FilteredMulticastFrames
2188-218AH	MSTAT FilteredBroadcastFrames
2190-2192H	MSTAT FramesTransmittedOK
2194-2196H	MSTAT OctetsTransmittedOK
2198-219AH	MSTAT OctetsTransmitted

Downloaded by [illegible] on Wednesday, 07 February, 2007 06:59:32 PM

Register Address A[14:0]	Register Description
219C-219EH	MSTAT FramesLostDueToInternalMACTransmissionError
21A0-21A2H	MSTAT TransmitSystemError
21A4-21A6H	MSTAT UnicastFramesTransmittedAttempted
21A8-21AAH	MSTAT UnicastFramesTransmittedOK
21AC-21AEH	MSTAT MulticastFramesTransmittedAttempted
21B0-21B2H	MSTAT MulticastFramesTransmittedOK
21B4-21B6H	MSTAT BroadcastFramesTransmittedAttempted
21B8-21BAH	MSTAT BroadcastFramesTransmittedOK
21BC-21BEH	MSTAT PAUSEMACCTRLFramesTransmitted
21C0-21C2H	MSTAT MACCTRLFramesTransmitted
21C4-21C6H	MSTAT TransmittedFrames64Octets
21C8-21CAH	MSTAT TransmittedFrames65to127Octets
21CC-21CEH	MSTAT TransmittedFrames128to255Octets
21D8-21DAH	MSTAT TransmittedFrames256to511Octets
21D8-21DAH	MSTAT TransmittedFrames512to1023Octets
21D8-21DAH	MSTAT TransmittedFrames1024to1518Octets
21D8-21DAH	MSTAT TransmittedFrames1519toMAXOctets
21E0-21E2H	MSTAT JumboOctetsTransmittedOK
21E4-21E6H	MSTAT TaggedFramesTransmittedOK
21E4-21FFH	MSTAT Reserved
2200H	IFLX Global Configuration Register
2201H	IFLX Global Status Register
2202H	IFLX Indirect Channel Address
2203H	IFLX SOF Error Enable
2204H	IFLX SOF Error Interrupt
2205H	IFLX EOF Error Enable
2206H	IFLX EOF Error Interrupt
2207H	IFLX Reserved
2208H	IFLX Reserved
2209H	IFLX Rate Adaptation Buffer Overflow Enable
220AH	IFLX Rate Adaptation Buffer Overflow Interrupt
220BH	IFLX Reserved
220CH	IFLX Reserved
220DH	IFLX Indirect Channel Address
220EH	IFLX Indirect Logical FIFO Low Limit & Provision
220FH	IFLX Indirect Logical FIFO High Limit
2210H	IFLX Indirect Full/Almost Full Status & Limit
2211H	IFLX Indirect Empty/Almost Empty Status & Limit
2212-221FH	IFLX Reserved
2220-223FH	S/UNI 9953 Reserved

Downloaded by Document Team of Electronics Weekly on 28 February, 2007 06:59:32 PM

Register Address A[14:0]	Register Description
2240H	PL4MOS Configuration
2241H	PL4MOS Mask
2242H	PL4MOS Fairness Masking
2243H	PL4MOS MaxBurst1
2244H	PL4MOS MaxBurst2
2245H	PL4MOS Transfer Size
2246-227FH	PL4MOS Reserved
2280H	PL4ODP Configuration
2281H	PL4ODP Reserved
2282H	PL4ODP Interrupt Mask
2283H	PL4ODP Interrupt
2284H	PL4ODP Configuration MAX_T Register
2285H	PL4ODP Elastic Store Limit
2286-22BFH	PL4ODP Reserved
22C0-22FFH	S/UNI 9953 Reserved
2300H	PL4IO Lock Detect Status
2301H	PL4IO Lock Detect Change
2302H	PL4IO Lock Detect Mask
2303H	PL4IO Lock Detect Limits
2304H	PL4IO Calendar Repetitions
2305H	PL4IO Configuration
2306H	PL4IO Reserved
2307H	PL4IO Reference Mode
2308-233FH	PL4IO Reserved
2340-237FH	S/UNI 9953 Reserved
2380H	CSTR Control
2381H	CSTR Interrupt Enable and CSU Lock Status
2382H	CSTR CSU Lock Interrupt Indication
2383H	CSTR Reserved
2384-23FFH	S/UNI 9953 Reserved
2400-241FH	IRAM Reserved
2420-2FFFH	S/UNI 9953 Reserved
3000-301FH	S/UNI 9953 Reserved
3020H	TCFP-9953 General Configuration
3021H	TCFP-9953 CRC Configuration
3022H	TCFP-9953 Interrupt Indication
3023H	TCFP-9953 Interrupt Enable
3024H	TCFP-9953 ATM Idle Cell Format
3025H	TCFP-9953 CRC Diagnostics
3026H	TCFP-9953 General Diagnostics

Downloaded by [illegible] team of [illegible] on Wednesday, 07 February, 2007 06:59:32 PM

Register Address A[14:0]	Register Description
3027H	TCFP-9953 Transmit Cell/Packet/Frame Counter (LSB)
3028H	TCFP-9953 Transmit Cell/Packet/Frame Counter (MSB)
3029H	TCFP-9953 Transmit Byte Counter (LSB)
302AH	TCFP-9953 Transmit Byte Counter (ISB)
302BH	TCFP-9953 Transmit Byte Counter (MSB)
302CH	TCFP-9953 Aborted Packet Counter
302DH	TCFP-9953 Transmit Idle Frame Counter (LSB)
302EH	TCFP-9953 Transmit Idle Frame Counter (MSB)
302FH	TCFP-9953 Reserved
3030-303FH	S/UNI 9953 Reserved
3040H	TXXG Configuration 1
3041H	TXXG Configuration 2
3042H	TXXG Configuration 3
3043H	TXXG Interrupt
3044H	TXXG Status
3045H	TXXG TX_MAXFR - Transmit Max Frame Size
3046H	TXXG TX_MINFR - Transmit Min Frame Size
3047H	TXXG SA[15:0] - Station Address
3048H	TXXG SA[31:16] - Station Address
3049H	TXXG SA[47:32] - Station Address
304AH	TXXG Diagnostic 1
304BH	TXXG Diagnostic 2
304CH	TXXG Diagnostic Status
304DH	TXXG PAUSE_TIME – PAUSE TIMER
304EH	TXXG PAUSE_IVAL – PAUSE Timer Interval
304FH	TXXG Packet Statistics (Lower 14 bits)
3050H	TXXG Packet Statistics (Upper 15 bits)
3051H	TXXG Filter Error Counter
3052H	TXXG Pause Quantum Value Configuration
3053-307FH	TXXG Reserved
3080H	T64B66B Configuration
3081H	~~T64B66B Interrupt Enable~~Reserved
3082H	~~T64B66B Interrupt Status~~Reserved
3083H	T64B66B Status
3084H	T64B66B FIFO Store Threshold (Reserved)
3085H	Jitter Test Seed A 3
3086H	Jitter Test Seed A 2
3087H	Jitter Test Seed A 1
3088H	Jitter Test Seed A 0
3089H	Jitter Test Seed B 3

Downloaded by Content Team of Datasheet Catalog.com, 07 February, 2007 06:59:32 PM

Register Address A[14:0]	Register Description
308AH	Jitter Test Seed B 2
308BH	Jitter Test Seed B 1
308CH	Jitter Test Seed B 0
3085-308FH	T64B66B Reserved
3090-31FFH	S/UNI 9953 Reserved
3200H	EFLX ERCU Global Configuration
3201H	EFLX ERCU Global Status
3202H	EFLX Indirect Channel Address
3203H	EFLX Indirect Logical FIFO Low Limit and Provision
3204H	EFLX Indirect Logical FIFO High Limit
3205H	EFLX Indirect Full/Almost-Full Status and Limit
3206H	EFLX Indirect Empty/Almost-Empty Status and Limit
3207H	EFLX Indirect FIFO Cut-Through Threshold
3208H	EFLX FIFO SOF Error Enable
3209H	EFLX FIFO SOF Error Indication
320AH	EFLX FIFO EOF Error Enable
320BH	EFLX FIFO EOF Error Indication
320CH	EFLX FIFO Overflow Error Enable
320DH	EFLX FIFO Overflow Error Indication
320EH	EFLX Invalid Channel Error Enable
320FH	EFLX Invalid Channel Error Indication
3210H	EFLX Channel Provision
3211-321FH	EFLX Reserved
3220-327FH	S/UNI 9953 Reserved
3280H	PL4IDU Configuration
3281H	PL4IDU Reserved
3282H	PL4IDU Interrupt Mask
3283H	PL4IDU Interrupt
3284-32BFH	PL4IDU Reserved
32C0-33FFH	S/UNI 9953 Reserved
3400-341FH	ERAM Reserved
3420-3FFFH	S/UNI 9953 Reserved
4000H	Master Test
4001-7FFFH	Reserved for Test

Notes on Register Memory Map

1. For all register accesses, CSB must be low.
2. Addresses that are not shown must be treated as Reserved.
3. A[14] is the test resister select (TRS) and should be set to logic 0 for normal mode register access.

Downloaded by Cirrent team of PMC-Sierra, Inc. on Monday, 01 October, 2007 06:59:32 PM

10.32.1 Receive STS-12/STM-4 Slice/Stream Mapping for OC-192/STS-192c/STM-64c Mode

An STS-12c/STM-64c SONET/SDH receive stream consists of 16 constituent STS-12/STM-4 equivalent data streams multiplexed together in a 4-byte interleaved manner (i.e. each STS-12/STM-4 contributes 4 bytes at time). Column 1 in Table 15 lists the sixteen STS-12/STM-4 streams (#1 to #16). The order of reception from the line is from top to bottom corresponding to the stream numbering. Column 2 lists the corresponding STM-16 group numbers for the STS-12/STM-4 streams. The STM-16 group association is for convenience in relating the STS-12/STM-4 streams to the STS-48/STM-16 oriented SONET/SDH system blocks (e.g. SBER, RTTP).

The corresponding STM-4 processing slices for the receive STS-12/STM-4 streams are listed in column 3. Column 4 lists the master/slave configuration of the 16 RRMP blocks in the 16 STM-4 processing slices required to process the transport overhead of the STS-192c/STM-64c SONET/SDH stream. Master configuration is represented by symbol **M** and slave configuration is represented by symbol **S**. Inactive blocks are marked by symbol **X**. Only the RRMP (RRMP#1) in STM-4 slice #1 is configured as a master and the remaining 15 RRMP (RRMP#2-#16) blocks are configured as slaves. Column 5 lists the configuration of the 4 SBER blocks in the 4 STM-16 processing groups. Only the SBER (SBER#1) in the STM-16 group #1 is configured as a master and the other 3 (SBER#2-#4) are inactive for processing an STS-192c/STM-64c stream. Columns 6, 7, 8, 9 and 10 list the configurations for the section RTTP, RHPP, path RTTP, SVCA and SARC blocks respectively.

The usage of register bits in a receive SONET/SDH system block when configured as a master may differ from that when it is configured as a slave. Although only one set of register description is provided per unique block (there may be more than one instance of the block in the device), the master/slave behavior of each register bit is described as appropriate.

Table 15 Receive STS-12/STM-4 Slice/Stream Mapping for OC-192/STS-192c/STM-64c Mode

SONET/ SDH STM-64 STM-4 #	S/UNI 9953 STM-16 Group #	S/UNI 9953 STM-4 Slice #	RRMP Slice (M/S)	SBER Group (M/S)	RTTP Section Group (M/S)	RHPP Slice (M/S)	RTTP Path Group (M/S)	SVCA Slice (M/S)	SARC Group (M/S)
1	1	1	M	M	M	M	M	M	M
2	1	2	S	—	—	S	—	S	—
3	1	3	S	—	—	S	—	S	—
4	1	4	S	—	—	S	—	S	—
5	2	5	S	X	X	S	X	S	X
6	2	6	S	—	—	S	—	S	—
7	2	7	S	—	—	S	—	S	—
8	2	8	S	—	—	S	—	S	—
9	3	9	S	X	X	S	X	S	X
10	3	10	S	—	—	S	—	S	—
11	3	11	S	—	—	S	—	S	—
12	3	12	S	—	—	S	—	S	—

Downloaded by Content Team of Pericom Inc. (Andrew Chen) on Oct 20, 2008 at 10:56:37 PM

SONET/ SDH STM-64 STM-4 #	S/UNI 9953 STM-16 Group #	S/UNI 9953 STM-4 Slice #	RRMP Slice (M/S)	SBER Group (M/S)	RTTP Section Group (M/S)	RHPP Slice (M/S)	RTTP Path Group (M/S)	SVCA Slice (M/S)	SARC Group (M/S)
13	4	13	S	X	X	S	X	S	X
14	4	14	S	—	—	S	—	S	—
15	4	15	S	—	—	S	—	S	—
16	4	16	S	—	—	S	—	S	—

10.32.2 Receive STS-12/STM-4 Slice/Stream mapping for OC-192/quad OC-48/STS-48c/STM-16c Modes

An OC-192 SONET/SDH receive stream channelized to 4 STS-48c/STM-16c (#1 to #4) each consisting of 4 constituent STS-12/STM-4 (#1 to #4) equivalent data streams is processed in this operation mode. Quad OC-48 SONET/SDH receive streams also supported by S/UNI 9953 consists of the same 16 constituent STS-12/STM-4 equivalent data streams as above multiplexed together in a 4-byte interleaved manner (i.e. each STS-12/STM-4 contributes 4 bytes at time to each STS-48c/STM-16c). Column 1 in Table 16 lists the sixteen STS-12/STM-4 streams (STM-16#1 STM-4#1 to STM-16#4 STM-4 #4) and the order of reception from the line is from top to bottom for an OC-192 operation. In the case of quad OC-48 operation, the order of reception is from the top to bottom within respective STS-48c/STM-16c streams. Column 2 lists the corresponding STM-16 group numbers for the STS-12/STM-4 streams. The STM-16 group association is for convenience in relating the STS-12/STM-4 streams to the STS-48/STM-16 oriented SONET/SDH system blocks (e.g. SBER, RTTP). In this case, the STM-16 group numbers matches the actual STM-48/STM-16 stream number listed in column 1.

The corresponding STM-4 processing slices for the receive STS-12/STM-4 streams are listed in column 3. Column 4 lists the master/slave configuration of the 16 RRMP blocks in the 16 STM-4 processing slices required to process the transport overhead of the four STS-48c/STM-16c data streams. Master configuration is represented by symbol **M** and slave configuration is represented by symbol **S**. STS-48c/STM-16c#1 is processed by RRMP#1-#4, STS-48c/STM-16c#2 is processed by RRMP#5-#8, STS-48c/STM-16c#3 is processed by RRMP#9-#12 and STS-48c/STM-16c#4 is processed by RRMP#13-#16. The RRMP (RRMP#1,#5,#9,#13) blocks in STM-4 slice #1, #5, #9 and #13 are configured as masters. The remaining 12 RRMP blocks are configured as slaves. Column 5 lists the master/slave configuration of the 4 SBER blocks in the 4 STM-16 processing groups. All four SBER (SBER#1-#4) blocks are configured as masters for processing the four corresponding STS-48c/STM-16c streams. Columns 6, 7, 8, 9 and 10 list the configurations for the section RTTP, RHPP, path RTTP, SVCA and SARC blocks respectively.

The usage of register bits in a receive SONET/SDH system block when configured as a master may differ from that when it is configured as a slave. Although only one set of register description is provided per unique block (there may be more than one instance of the block in the device), the master/slave behavior of each register bit is described as appropriate.

Downloaded by Circuit Team Electronics (www.circuit.ru) on Monday, July 2007 06:16:32 PM

Table 16 Receive STS-12/STM-4 Slice/Stream mapping for OC-192/quad OC-48/STS-48c/STM-16c Modes

SONET/ SDH STM-16 # STM-4 #	S/UNI 9953 STM-16 Group #	S/UNI 9953 STM-4 Slice #	RRMP Slice (M/S)	SBER Group (M/S)	RTTP Section Group (M/S)	RHPP Slice (M/S)	RTTP Path Group (M/S)	SVCA Slice (M/S)	SARC Group (M/S)
1,1	1	1	M	M	M	M	M	M	M
1,2	1	2	S	—	—	S	—	S	—
1,3	1	3	S	—	—	S	—	S	—
1,4	1	4	S	—	—	S	—	S	—
2,1	2	5	M	M	M	M	M	M	M
2,2	2	6	S	—	—	S	—	S	—
2,3	2	7	S	—	—	S	—	S	—
2,4	2	8	S	—	—	S	—	S	—
3,1	3	9	M	M	M	M	M	M	M
3,2	3	10	S	—	—	S	—	S	—
3,3	3	11	S	—	—	S	—	S	—
3,4	3	12	S	—	—	S	—	S	—
4,1	4	13	M	M	M	M	M	M	M
4,2	4	14	S	—	—	S	—	S	—
4,3	4	15	S	—	—	S	—	S	—
4,4	4	16	S	—	—	S	—	S	—

10.32.3 Transmit STS-12/STM-4 Slice/Stream Mapping for OC-192/STS-192c/STM-64c Mode

An STS-192c/STM-64c SONET/SDH transmit stream consists of 16 constituent STS-12/STM-4 equivalent data streams multiplexed together in a 4-byte interleaved manner (i.e. each STM-4 contributes 4 bytes at time). Column 1 in Table 17 lists the sixteen STS-12/STM-4 streams (#1 to #16). The order of line transmission is from top to bottom corresponding to the stream numbering. Column 2 lists the corresponding STM-16 group numbers for the STS-12/STM-4 streams. The STM-16 group association is for convenience in relating the STS-12/STM-4 streams to the STS-48/STM-16 oriented SONET/SDH system blocks (e.g. RTTP, SIRP).

The corresponding STM-4 processing slices for the transmit STS-12/STM-4 streams are listed in column 3. Column 4 lists the master/slave configuration of the 16 TRMP blocks in the 16 STM-4 processing slices required to process the transport overhead of the STS-192c/STM-64c SONET/SDH stream. Master configuration is represented by symbol **M** and slave configuration is represented by symbol **S**. Inactive blocks are marked by symbol **X**. Only the TRMP (TRMP#1) in STM-4 slice #1 is configured as a master and the remaining 15 TRMP (TRMP#2-#16) blocks are configured as slaves. Column 5 lists the configuration of the 4 section TTTP blocks in the 4 STM-16 processing groups. Only the TTTP (TTTP#1) in the STM-16 group #1 is configured as a master and the other 3 (TTTP#2-#4) are inactive for processing an STS-192c/STM-64c stream. Columns 6, 7 and 8 list the configurations for the section THPP, path TTTP and SIRP blocks respectively.

Downloaded by [illegible] on Wednesday, 01 February, 2006, 06:59:[illegible] GMT

The usage of register bits in a transmit SONET/SDH system block when configured as a master may differ from that when it is configured as a slave. Although only one set of register description is provided per unique block (there may be more than one instance of the block in the device), the master/slave behavior of each register bit is described as appropriate.

Table 17 Transmit STS-12/STM-4 Slice/Stream Mapping for OC-192/STS-192c/STM-64c Mode

SONET/ SDH STM-64 STM-4 #	S/UNI 9953 STM-16 Group #	S/UNI 9953 STM-4 Slice #	TRMP Slice (M/S)	TTTP Section Group (M/S)	THPP Slice (M/S)	TTTP Path Group (M/S)	SIRP Slice (M/S)
1	1	1	M	M	M	M	M
2	1	2	S	—	S	—	—
3	1	3	S	—	S	—	—
4	1	4	S	—	S	—	—
5	2	5	S	X	S	X	X
6	2	6	S	—	S	—	—
7	2	7	S	—	S	—	—
8	2	8	S	—	S	—	—
9	3	9	S	X	S	X	X
10	3	10	S	—	S	—	—
11	3	11	S	—	S	—	—
12	3	12	S	—	S	—	—
13	4	13	S	X	S	X	X
14	4	14	S	—	S	—	—
15	4	15	S	—	S	—	—
16	4	16	S	—	S	—	—

10.32.4 Transmit STS-12/STM-4 Slice/Stream mapping for OC-192/quad OC-48/STS-48c/STM-16c Modes

An OC-192 SONET/SDH transmit stream channelized to 4 STS-48c/STM-16c (#1 to #4) each consisting of 4 constituent STS-12/STM-4 (#1 to #4) equivalent data streams is processed in this operation mode. Quad OC-48 SONET/SDH transmit streams also supported by S/UNI 9953 consists of the same 16 constituent STS-12/STM-4 equivalent data streams as above multiplexed together in a 4-byte interleaved manner (i.e. each STS-12/STM-4 contributes 4 bytes at time to each STS-48c/STM-16c). Column 1 in Table 18 lists the sixteen STS-12/STM-4 streams (STM-16#1 STM-4#1 to STM-16#4 STM-4 #4). The order of line transmission is from top to bottom for an OC-192 operation. In the case of quad OC-48 operation, the order of line transmission is from the top to bottom within respective STS-48c/STM-16c streams. Column 2 lists the corresponding STM-16 group numbers for the STS-12/STM-4 streams. The STM-16 group association is for convenience in relating the STS-12/STM-4 streams to the STS-48/STM-16 oriented SONET/SDH system blocks (e.g. TTTP, SIRP). In this case, the STM-16 group numbers matches the actual STS-48/STM-16 stream number listed in column 1.

Downloaded by [redacted] on Wednesday, 07 February 2007, 06:39:32 PM

The corresponding STM-4 processing slices for the transmit STS-12/STM-4 streams are listed in column 3. Column 4 lists the master/slave configuration of the 16 TRMP blocks in the 16 STM-4 processing slices required to process the transport overhead of the four STS-48c/STM-16c data streams. Master configuration is represented by symbol **M** and slave configuration is represented by symbol **S**. STS-48c/STM-16c#1 is processed by TRMP#1-#4, STS-48c/STM-16c#2 is processed by TRMP#5-#8, STS-48c/STM-16c#3 is processed by TRMP#9-#12 and STS-48c/STM-16c#4 is processed by TRMP#13-#16. The TRMP (TRMP#1,#5,#9,#13) blocks in STM-4 slice #1, #5, #9 and #13 are configured as masters. The remaining 12 TRMP blocks are configured as slaves. Column 5 lists the configuration of the 4 section TTTP blocks in the 4 STM-16 processing groups. All four section TTTP (TTTP#1-#4) blocks are configured as masters for processing the four corresponding STS-48c/STM-16c streams. Columns 6, 7 and 8 list the configurations for the THPP, path TTTP and SIRP blocks respectively.

The usage of register bits in a transmit SONET/SDH system block when configured as a master may differ from that when it is configured as a slave. Although only one set of register description is provided per unique block (there may be more than one instance of the block in the device), the master/slave behavior of each register bit is described as appropriate.

Table 18 Transmit STS-12/STM-4 Slice/Stream Mapping for OC-192/Quad OC-48/STS-48c/STM-16c Modes

SONET/ SDH STM-16 # STM-4 #	S/UNI 9953 STM-16 Group #	S/UNI 9953 STM-4 Slice #	TRMP Slice (M/S)	TTTP Section Group (M/S)	THPP Slice (M/S)	TTTP Path Group (M/S)	SIRP Slice (M/S)
1,1	1	1	M	M	M	M	M
1,2	1	2	S	—	S	—	—
1,3	1	3	S	—	S	—	—
1,4	1	4	S	—	S	—	—
2,1	2	5	M	M	M	M	M
2,2	2	6	S	—	S	—	—
2,3	2	7	S	—	S	—	—
2,4	2	8	S	—	S	—	—
3,1	3	9	M	M	M	M	M
3,2	3	10	S	—	S	—	—
3,3	3	11	S	—	S	—	—
3,4	3	12	S	—	S	—	—
4,1	4	13	M	M	M	M	M
4,2	4	14	S	—	S	—	—
4,3	4	15	S	—	S	—	—
4,4	4	16	S	—	S	—	—

Downloaded by Conexant on behalf of Pathmine Inc on Tuesday 07 February 2017 at 12:00 AM

11 Addressing Soft-Errors

Some circuits in today's deep sub-micron processes are susceptible to strikes from alpha particles. These strikes result in soft-errors. For example, direct alpha strikes to embedded memories (including standard 6T and 8T SRAM bit cells) can change the stored information. Although the error rates are extremely small (typically less than one failure per twenty years per megabit of ram) the cumulative system level effect of these errors can be significant if the system contains a large amount of RAM.

Since all semiconductor materials contain trace amounts of radioactivity and can be influenced by high-energy neutrons inherent in cosmic rays, all sub-micron designs must deal with soft-error. The semiconductor industry employs many techniques to address soft-errors. Unfortunately, implementing soft-error handling techniques tends to increase device cost. For example, hardening the semiconductor process to alpha strikes or providing error correction is often more costly than choosing to provide error detection or interrupts to flag soft-errors at the system level.

The largest section of RAM contained within the PM5390 is used for the packet FIFO of the PL4 subsystem. The receive (ingress) FIFO is 16K bytes and the transmit (egress) FIFO is 20K bytes. They are referred to as the IRAM (ingress) and ERAM (egress) blocks. These RAMs provide parity protection to assist in identifying issues due to soft errors. Interrupts may be triggered based on detected parity errors. Please see the register description for these blocks for further details.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 04:02:22 PM

12 Normal Mode Register Description

Normal mode registers are used to configure and monitor the operation of the S/UNI 9953. Normal mode registers (as opposed to test mode registers) are selected when TRS (A[14]) is low.

Notes on Normal Mode Register Bits

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of this product, unused register bits must be written with logic 0. Reading back unused bits can produce either a logic 1 or a logic 0; hence, unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the S/UNI 9953 to determine the programming state of the device.

3. Writeable normal mode register bits are cleared to logic 0 upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect S/UNI 9953 operation unless otherwise noted.

5. Certain register bits are reserved. These bits are associated with mega-cell functions that are unused in this application. To ensure that the S/UNI 9953 operates as intended, reserved register bits must only be written with the logic level as specified. Writing to reserved registers should be avoided.

Downloaded by Content Team of Partminer Inc on Wednesday, 01 February 2017 06:59:... PM

12.1 Top Level

Register 0000H S/UNI 9953 Identity, and Global Performance Monitor Update

Bit	Type	Function	Default
Bit 15	R	TIP	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	R	TYPE[4]	0
Bit 7	R	TYPE [3]	0
Bit 6	R	TYPE[2]	0
Bit 5	R	TYPE[1]	0
Bit 4	R	TYPE[0]	0
Bit 3	R	ID[3]	0
Bit 2	R	ID[2]	0
Bit 1	R	ID[1]	1
Bit 0	R	ID[0]	0

This register allows the revision number of the S/UNI 9953 to be read by software permitting graceful migration to newer, feature-enhanced versions of the S/UNI 9953.

In addition, writing to this register performs a global performance monitor update by simultaneously loading all the performance meter registers in the device. Writing to this register has no effect on the MSTAT block. The performance meter registers in the MSTAT block is updated by setting the SNAP bit in MSTAT Control register to logic 1.

ID[3:0]

The ID bits can be read to provide a binary S/UNI 9953 revision number.

This value is 0x0 for Revision A, 0x1 for Revision B, and 0x2 for Revision C.

TYPE[4:0]

The TYPE bits can be read to distinguish the S/UNI 9953 from the other members of the family of devices. The TYPE[4:0] register for the PM5390 S/UNI 9953 is 00000.

Downloaded by Content Team of Partmaker Inc on Wednesday, 07 February, 2007 06:59:32 PM

TIP

The TIP bit is set to a logic one when the performance meter registers are being loaded. Writing to this register with DRESET equal to logic 0 initiates an accumulation interval transfer and loads all the performance meter registers in the S/UNI 9953. TIP remains high while the transfer is in progress, and is set to a logic zero when the transfer is complete. TIP can be polled by a microprocessor to determine when the accumulation interval transfer is complete.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 08:38:42 AM

Register 0001H: S/UNI 9953 Master Reset and Configuration

Bit	Type	Function	Default
Bit 15	R/W	DRESET	0
Bit 14	R/W	ARESET_APS	0
Bit 13	R/W	ARESET_OIF	0
Bit 12	R/W	ARESET_PL4	0
Bit 11	R/W	Reserved	1
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	R/W	SYNC_ERR_XOR	0
Bit 7	R/W	OIF_LSB_1ST	0
Bit 6	R/W	WCIMODE	0
Bit 5	R	QUAD2488	X
Bit 4	R/W	LAN	0
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R/W	SSMODE[1]	0
Bit 0	R/W	SSMODE[0]	0

This register allows the configuration of S/UNI 9953 features and enables software reset.

SSMODE[1:0]

The S/UNI 9953 SONET/SDH Mode (SSMODE[1:0]) bits are provided for configuring the device operation mode in both the transmit and receive direction. The SONET/SDH Telecom Standard Blocks (TSB) in the device will be configured to operate in master or slave mode as appropriate to support the selected device operation mode (see Operation section).

SSMODE[1:0]	S/UNI 9953 Transmit/Receive Operation Mode
00	OIF: OC-192 SONET/SDH Transport: STS-192/STM-64 SONET/SDH Path Payload: STS-192c/AU-4-64c RCFP-9953 enabled for ATM/POS payload (R10GbEEN=0) TCFP-9953 enabled for ATM/POS payload (T10GbEEN=0) RXXG enabled for 10G Ethernet payload (R10GbEEN=1) TXXG enabled for 10G Ethernet payload (T10GbEEN=1) Ingress FIFO (IFLX) / Rx PL4 configured for single channel. Egress FIFO (EFLX) / Tx PL4 configured for single channel.
01	OIF: OC-192 SONET/SDH Transport: STS-192/STM-64 SONET/SDH Path Payload: 4xSTS-48c/4xAU-4-16c RCFP enabled for ATM/POS payload TCFP enabled for ATM/POS payload Ingress FIFO (IFLX) / Rx PL4 configured for four channels. Egress FIFO (EFLX) / Tx PL4 configured for four channels.
10	OIF: 4xOC-48

Downloaded by Content Team of Partminer.com on Wednesday, 07 February, 2007 06:39:32 PM

SSMODE[1:0]	S/UNI 9953 Transmit/Receive Operation Mode
	SONET/SDH Transport: 4xSTS-48/STM-16 SONET/SDH Path Payload: 4xSTS-48c/4xAU-4-16c RCFP enabled for ATM/POS payload TCFP enabled for ATM/POS payload Ingress FIFO (IFLX) / Rx PL4 configured for four channels. Egress FIFO (EFLX) / Tx PL4 configured for four channels.
11	Reserved

LAN

The LAN mode select (LAN) bit selects between the 10 GbE LAN or WAN PHY operation modes. When LAN is low, the device is in 10 GbE WAN PHY operation mode. When LAN is high, the device is in 10 GbE LAN PHY operation mode. This bit is logically ORed with the corresponding LAN configuration device input pin. When the corresponding LAN configuration input is set high, this register bit will be read as high regardless of its register setting. For LAN PHY operation, the SSMODE[1:0] must be set to b'00 and the QUAD2488 configuration input must be set to low.

QUAD2488

This register bit provides a software read-out of the logic level setting at the corresponding QUAD2488 pin.

WCIMODE

The write on clear interrupt mode (WCIMODE) bit selects the clear interrupt mode. When a logic 1 is written to WCIMODE, the clear interrupt mode is clear on write. When a logic 0 is written to WCIMODE, the clear interrupt mode is clear on read. The WCIMODE bit has no effect on the MSTAT block. All interrupts are cleared on read in the MSTAT block.

Note that WCIMODE bit should be considered a static register bit. It is not expected to continuously change the setting of this bit, as unpredictable clearing of the interrupt status bits may occur.

Also note, that when WCIMODE bit is set high (clear on write), then it is necessary to set a logic one in the respective bit position of the interrupt that is to be cleared .

OIF_LSB_1ST

The OIF Least Significant Bit transmit/receive First enable (OIF_LSB_1ST) bit selects between the LSB/MSB first order of bit transmission/reception of 16-bit words at the Line Interface. When OIF_LSB_1ST is set to logic 0, the normal MSB first transmission/reception mode is enabled. When OIF_LSB_1ST is set to logic 1, the special LSB first transmission/reception mode is enabled. This register bit must be set high for 10 GbE LAN PHY operation where the LAN PHY optical transponder transmits/receives LSB first.

Downloaded by Content Team of Pattinson on Wednesday, 07 February 2007 06:13:32 PM

SYNC_ERR_XOR

This SYNC_ERR XOR enable (SYNC_ERR_XOR) bit is for controlling the polarity of the SYNC_ERR[4:1] input pins. When SYNC_ERR_XOR is set to logic 1, the inputs provided at SYNC_ERR[4:1] are inverted before being used. When SYNC_ERR_XOR is set to logic 0, the inputs provided at SYNC_ERR[4:1] are used as is.

ARESET_PL4

The ARESET_PL4 bit allows the PL4 analog circuitry in the S/UNI 9953 to be reset under software control. If the ARESET_PL4 bit is a logic one, PL4 analog circuitry is held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring the PL4 analog blocks out of reset. Holding the ARESET_PL4 in a reset state places it into a low power, analog stand-by mode. A hardware reset clears the ARESET_PL4 bit, thus negating the analog software reset.

ARESET_OIF

The ARESET_OIF bit allows the OIF analog circuitry in the S/UNI 9953 to be reset under software control. If the ARESET_OIF bit is a logic one, OIF analog circuitry is held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring the OIF analog blocks out of reset. Holding the ARESET_OIF in a reset state places it into a low power, analog stand-by mode. A hardware reset clears the ARESET_OIF bit, thus negating the analog software reset.

ARESET_APS

The ARESET_APS bit allows the APS Port analog circuitry in the S/UNI 9953 to be reset under software control. If the ARESET_APS bit is a logic one, APS Port analog circuitry is held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring the APS Port analog blocks out of reset. Holding the ARESET_APS in a reset state places it into a low power, analog stand-by mode. A hardware reset clears the ARESET_APS bit, thus negating the analog software reset.

DRESET

The DRESET bit allows the digital circuitry in the S/UNI 9953 to be reset under software control. If the DRESET bit is a logic one, all the S/UNI 9953 digital circuitry is held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring the S/UNI 9953 out of reset. A hardware reset clears the DRESET bit, thus negating the digital software reset.

Downloaded by Cores Team of Pacificinc on Wed, Sep, 07 Febr 2007 06:59:33 PM

Register 0002H: S/UNI 9953 System-side Configuration

Bit	Type	Function	Default
Bit 15	R/W	TOP_CHAN[3]	0
Bit 14	R/W	TOP_CHAN[2]	0
Bit 13	R/W	TOP_CHAN[1]	0
Bit 12	R/W	TOP_CHAN[0]	0
Bit 11	R/W	WIS_GEN_FRAME_INV	1
Bit 10	R/W	WIS_GEN_FRAME_RST	1
Bit 9	R/W	WIS_GEN_CID_EN	1
Bit 8	R/W	WIS_GEN_PRBS_EN	0
Bit 7	R/W	FAST_SYNC_ERR	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	WIS_GEN_SQUARE_EN	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	R10GbEEN	0
Bit 0	R/W	T10GbEEN	0

The S/UNI 9953 System-side Configuration Register is provided to enable ATM cells, POS packets or IEEE 802.3ae 10 Gigabit Ethernet frames processing on the system-side.

T10GbEEN

The Transmit 10 Gigabit Ethernet Enable (T10GbEEN) bit is provided to select ATM cells, POS packets, GFP frames or the IEEE 802.3ae 10 Gigabit Ethernet frames processing on transmit system-side when the S/UNI 9953 is configured to process STS-192c/STM-64c SONET/SDH data stream. When T10GbEEN is logic one, the TXXG block is enabled to process 10 Gigabit Ethernet frames. When T10GbEEN is logic zero, the TCFP-9953 block is enabled to process ATM cells, GFP frames or POS packets. This register bit is ignored when S/UNI 9953 is not configured to process STS-192c/STM-64c SONET/SDH data stream.

R10GbEEN

The Receive 10 Gigabit Ethernet Enable (R10GbEEN) bit is provided to select ATM cells, POS packets, GFP frames or the IEEE 802.3ae 10 Gigabit Ethernet frames processing on receive system-side when the S/UNI 9953 is configured to process STS-192c/STM-64c SONET/SDH data stream. When R10GbEEN is logic one, the RXXG block is enabled to process 10 Gigabit Ethernet frames. When R10GbEEN is logic zero, the RCFP-9953 block is enabled to process ATM cells, GFP frames or POS packets. This register bit is ignored when S/UNI 9953 is not configured to process STS-192c/STM-64c SONET/SDH data stream.

Downloaded by Content Team of pmc on Wednesday, 07 February, 2007 06:59:32 PM

Reserved

These register bits are reserved for future product enhancement, and must be left in its default setting for proper operation of the S/UNI 9953.

WIS_GEN_SQUARE_EN

WIS layer Square wave Pattern Generator Enable. When WIS_GEN_SQUARE_EN is set high, a square wave pattern is forced out on the line interface. The square wave is defined as a serialized 0x00FF pattern. This bit takes priority over the WIS_GEN_PRBS_EN bit. When set low, normal data path is transmitted on the line interface.

WIS_GEN_PRBS_EN

WIS layer PRBS wave Pattern Generator Enable. When WIS_GEN_PRBS_EN is set high, a PRBS-23 pattern is generated within the WIS payload. The WIS_GEN_SQUARE_EN bit takes priority over this bit. When set low, normal data path is transmitted on the line interface.

WIS_GEN_CID_EN

WIS layer CID Pattern Enable. When WIS_GEN_CID_EN is set high, the Consecutive Identical Digit (CID) pattern in the last 9 Z0 octets of a STS-192c frame. The CID pattern is defined in the IEEE 802.3ae specification. When low, the Z0 bytes are 0xCC.

Note that the TRMP needs to be configured to pass the Z0 bytes unmodified so that the CID is transmitted on the line interface.

WIS_GEN_FRAME_RST.

WIS layer Frame Reset. When WIS_GEN_FRAME_RST is set high, the generated WIS PRBS pattern is reset to the standard seed as defined in IEEE 802.3ae at the start of each frame. When low, the PRBS pattern is left free running.

WIS_GEN_FRAME_INV

WIS layer Frame Invert. When WIS_GEN_FRAME_INV is set high, the generated WIS PRBS pattern is bit-wise inverted every other frame as defined in IEEE 802.3ae. When low, the PRBS pattern is not inverted.

FAST_SYNC_ERR

This register bit is reserved for future product enhancement, and must be left in its default setting for proper operation of the S/UNI 9953.

Downloaded by content team of Datasheet Inc on Wednesday, 07 February, 2007 06:59:32 PM

TOP_CHAN[3:2]

These register bits are reserved for PMC debug purposes only, and must be left in its default setting for proper operation of the S/UNI 9953.

TOP_CHAN[1:0]

The Top Channel configuration (TOP_CHAN[1:0]) bits are the number of active channels to be processed by the Ingress/Egress Flex FIFO blocks. The value reflects the highest channel that will be processed, where 0 is the bottom channel (for single channel operation). Up to 4 active channels are supported. The number of active channels must be in agreement with the setting of the SSMODE[1:0] bits (Register 0001H: S/UNI 9953 Master Reset and Configuration), so that the maximum bandwidth is not surpassed. TOP_CHAN[1:0] bits must be set before the Flex FIFO blocks are enabled.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 06:59:32 PM

Register 0003H: S/UNI 9953 Loop Back Configuration

Bit	Type	Function	Default
Bit 15	R/W	SDLBEN4	0
Bit 14	R/W	SDLBEN3	0
Bit 13	R/W	SDLBEN2	0
Bit 12	R/W	SDLBEN1	0
Bit 11	R/W	SLLBEN4	0
Bit 10	R/W	SLLBEN3	0
Bit 9	R/W	SLLBEN2	0
Bit 8	R/W	SLLBEN1	0
Bit 7	R/W	LLBEN4	0
Bit 6	R/W	LLBEN3	0
Bit 5	R/W	LLBEN2	0
Bit 4	R/W	LLBEN1	0
Bit 3	R/W	PDLEN4	0
Bit 2	R/W	PDLEN3	0
Bit 1	R/W	PDLEN2	0
Bit 0	R/W	PDLEN1	0

This register allows the diagnostic/line loop back configuration of the S/UNI 9953.

Note that setting loopback bits will switch internal clock paths as well as data paths. It is recommended to apply a soft reset to the system blocks to avoid potential clock phase issues, as these blocks use multi-phase aligned clocks. These resets are RXSYS192_RST and TXSYS192_RST in register 001Fh.

PDLEN[4:1]

The Parallel Diagnostic Loop Back (PDLEN[N]) bit enables the S/UNI 9953 Line Side diagnostic loop back for the constituent STS-48c (STM-16c) #N transmit stream where the corresponding output port of STLI block carrying the stream are directly connected to the corresponding input port of the SRLI block. When PDLEN[N] is logic one, loop back is enabled. Under this operating condition, the S/UNI 9953 continues to operate normally in the transmit direction. When PDLEN[N] is logic zero, the S/UNI 9953 operates normally. TXCLK[N] and RXCLK[N] must be frequency locked for parallel diagnostic loop back to operate properly.

(Loop back path [2] with reference to Loop Back Modes Diagram)

Downloaded by Content Finder Examiner from IHS on Wednesday, 07 February, 2007 06:39:32 PM

LLBEN[4:1]

The (Line-side) Line Loop back Enable (LLBEN[N]) bit enables the S/UNI 9953 line loop back for the constituent STS-48c (STM-16c) #N receive stream where the OIFS system-side output for the receive stream is directly connected to the corresponding OIFS system-side input to provide the transmit stream. When LLBEN[N] is logic one, the loop back is enabled. When LLBEN[N] is logic zero, the S/UNI 9953 operates normally. The LLBEN[N] bit is only used for test purposes. It provides a convenient mechanism for Line Interface and Line optics testing. TXCLK[N] and RXCLK[N] must be frequency locked for this line loop back to operate properly.

(Loop back path [1] with reference to Loop back Modes Diagram)

SLLBEN[4:1]

The System Line Loop back Enable (SLLBEN[N]) bit enables the S/UNI 9953 line loop back for the constituent STS-48c (STM-16c) #N receive stream where the SVCA output for the stream is directly connected to the corresponding THPP (via SIRP) input. When SLLBEN[N] is logic one, the loop back is enabled. When SLLBEN[N] is logic zero, the S/UNI 9953 operates normally. The SLLBEN[N] bit is only used for test purposes and allows the POS-PHY Level 4 interface to be isolated from the SONET interface.

(Loop back path [3] with reference to Loop back Modes Diagram)

SDLBEN[4:1]

The System Diagnostic Loop back Enable (SDLBEN[N]) bit enables the S/UNI 9953 diagnostic loop back for the constituent STS-48c (STM-16c) #N transmit stream where the TXSTSI output for the stream is directly connected to the corresponding RXSTSI input. When SDLBEN[N] is logic one, the loop back is enabled. When SDLBEN[N] is logic zero, the S/UNI 9953 operates normally. The SDLBEN[N] bit is only used for test purposes and allows the SONET interface to be isolated from POS-PHY Level 4 interface.

Note that this loop back is not applicable for LAN mode. A similar loop back path may be obtained for LAN mode by using the Parallel Diagnostic Loop back (PDLEN[4:1]).

(Loop back path [4] with reference to Loop back Modes Diagram)

Downloaded by Content Team of Datasheet.in on Wednesday 07 February 2007 08:07:07 PM

Register 0004H: S/UNI 9953 Transmit Control and Clock Enable Register

Bit	Type	Function	Default
Bit 15	R/W	RESYNC_EN	1
Bit 14	R/W	TREQ_ADVANCE[6]	1
Bit 13	R/W	TREQ_ADVANCE[5]	0
Bit 12	R/W	TREQ_ADVANCE[4]	1
Bit 11	R/W	TREQ_ADVANCE[3]	0
Bit 10	R/W	TREQ_ADVANCE[2]	0
Bit 9	R/W	TREQ_ADVANCE[1]	0
Bit 8	R/W	TREQ_ADVANCE[0]	0
Bit 7	R/W	RCLK4EN	0
Bit 6	R/W	RCLK3EN	0
Bit 5	R/W	RCLK2EN	0
Bit 4	R/W	RCLK1EN	0
Bit 3	R/W	TCLK4EN	0
Bit 2	R/W	TCLK3EN	0
Bit 1	R/W	TCLK2EN	0
Bit 0	R/W	TCLK1EN	0

TCLK[4:1]EN

The TCLK[N] Enable (TCLK[4:1]EN) bits are provided to control the corresponding TCLK[4:1] outputs. When TCLK[N]EN is set to logic 1, the TCLK[N] output is enabled. When TCLK[N]EN is set to logic 0, the TCLK[N] output is forced low.

RCLK[4:1]EN

The RCLK[N] Enable (RCLK[4:1]EN) bits are provided to control the corresponding RCLK[4:1] outputs. When RCLK[N]EN is set to logic 1, the RCLK[N] output is enabled. When RCLK[N]EN is set to logic 0, the RCLK[N] output is forced low.

TREQ_ADVANCE[6:0]

The TREQ_ADVANCE[6:0] bits control an internal pipeline. It should be left at the default of 80 decimal for all modes of operation, except for the WIS test patterns. In this case, it should be set to 72 decimal.

RESYNC_EN

This register bit must be set to logic 1 for normal operation of the S/UNI 9953.

Downloaded by Contentmaster of Container Int. on Wednesday, 07 February, 2007 06:59:32 PM

Register 0005H: S/UNI 9953 Clock Monitors

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	IAPSFPCLKA	X
Bit 10	R	TDCLKA	X
Bit 9	R	RSCLKA	X
Bit 8	R	RDCLKA	X
Bit 7	R	RCLK4A	X
Bit 6	R	RCLK3A	X
Bit 5	R	RCLK2A	X
Bit 4	R	RCLK1A	X
Bit 3	R	TCLK4A	X
Bit 2	R	TCLK3A	X
Bit 1	R	TCLK2A	X
Bit 0	R	TCLK1A	X

TCLK[4:1]A

The TCLK[4:1] active (TCLK[4:1]A) bits monitor for low to high transitions on the TCLK[4:1]. TCLK[N]A is set high on a rising edge of TCLK[N], and is set low when this register is read.

RCLK[4:1]A

The RCLK[4:1] active (RCLKA[4:1]) bits monitor for low to high transitions on the RCLK[4:1]. RCLK[N]A is set high on a rising edge of RCLK[N], and is set low when this register is read.

RDCLKA

The RDCLK active (RDCLKA) bit monitors for low to high transitions on the RDCLK+/- clock input. RDCLKA is set high on a rising edge of RDCLK+/-, and is set low when this register is read.

RSCLKA

The RSCLK active (RSCLKA) bit monitors for low to high transitions on the RSCLK clock input. RSCLKA is set high on a rising edge of RSCLK, and is set low when this register is read.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:09:32 PM

TDCLKA

The TDCLK active (TDCLKA) bit monitors for low to high transitions on the TDCLK clock input. TDCLKA is set high on a rising edge of TDCLK, and is set low when this register is read.

IAPSFPCLKA

The IAPSFPCLK active (IAPSFPCLKA) bit monitors for low to high transitions on the IAPSFPCLK clock input. IAPSFPCLKA is set high on a rising edge of IAPSFPCLK, and is set low when this register is read.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0006H: S/UNI 9953 Line Analog Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	1
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	—	Unused	X
Bit 0	—	Unused	X

The S/UNI 9953 Line Analog Configuration Register is reserved and provided for diagnostic purposes only. The reserved register bits must be set to the default values as indicated for proper operation of the S/UNI 9953.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:09:32 PM

Register 0007H: S/UNI 9953 Transmit and APS Configuration 1

Bit	Type	Function	Default
Bit 15	R/W	IAPS_NDF_EN	0
Bit 14	R/W	IAPS_PAIS_EN	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	APSMUX0CTL	0
Bit 10	R/W	APSMUX1CTL	0
Bit 9	R/W	APSMUX2CTL	0
Bit 8	R/W	APSMUX3CTL	0
Bit 7	R/W	SS_H1[1]	1
Bit 6	R/W	SS_H1[0]	0
Bit 5	R/W	SS_CONCAT[1]	0
Bit 4	R/W	SS_CONCAT[0]	0
Bit 3	R/W	TPAIS_EN	0
Bit 2	R/W	TLD_VAL	0
Bit 1	R/W	TSLD_VAL	0
Bit 0	R/W	LOCK0	0

Registers 0x0007 – 0x000A controls a) the configuration of the S/UNI 9953 transmit SONET/SDH frame, b) input APS consequential actions, and c) the configuration of the APS muxes.

Groups b) and c) defined above are controlled independently of the device mode (ie concatenated, channelised, or quad modes). These bits must be set for each STS-48c/STM-16c slice. This applies to bits APSMUX[n]CTL, IAPS_PAIS_EN and IAPS_NDF_EN.

Group a) is controlled independently in quad STS-48c/STM-16c, or channelized STS-192/STM-64 modes. In concatenated STS-192c/STM-64c mode, register 0x0007 (ie slice #1) controls all of group a) functions. This applies to bits LOCK0, TSLD_VAL, TLD_VAL, TPAIS_EN, SS_CONCAT, and SS_H1.

LOCK0

This bit controls the generation of the J1 Path Overhead Byte location for the transmit direction, and thus, the H1 H2 pointer value for the transmit direction. When set to logic 0, the H1 H2 pointer value is set at 522. This is the normal pointer location for ATM configuration. When set to logic 1, the H1 H2 pointer value is set at 0. This register bit configures all data streams in OC-192 mode and STS-48c/STM-16c #1 data stream in quad OC-48 mode.

Downloaded by Conexant Beam of Mindspeed on Wednesday, 07 February, 2007 06:39:32 PM

TSLD_VAL

The TSLD value (TSLD_VAL) bit is used to set the value optionally inserted into the section DCC (D1-D3) in the transmit data stream as configured using the TSLDEN bit in the TRMP Configuration register. When set to logic 1, ones are inserted. When set to logic 0, zeros are inserted. This register bit configures all data streams in OC-192 mode and STS-48c/STM-16c #1 data stream in quad OC-48 mode.

TLD_VAL

The TLD value (TLD_VAL) bit is used to set the value optionally inserted into the line DCC (D4-D12) in the transmit data stream as configured using the TLDEN bit in the TRMP Configuration register. When set to logic 1, ones are inserted. When set to logic 0, zeros are inserted. This register bit configures all data streams in OC-192 mode and STS-48c/STM-16c #1 data stream in quad OC-48 mode.

TPAIS_EN

The Transmit Path AIS Enable bit controls the insertion of Transmit Path AIS in corresponding data stream. When logic 0, the S/UNI 9953 does not generate Transmit Path AIS. When logic 1, the S/UNI 9953 will generate Transmit Path AIS. This register bit configures all data streams in OC-192 mode and STS-48c/STM-16c #1 data stream in quad OC-48 mode.

Note that setting the TPAIS_EN bit causes all TOH bytes upstream of the TRMP to be set to all ones, as well as the SPE bytes. The TRMP will then over-ride any necessary TOH bytes. Any TOH bytes not explicity set by the TRMP (pass through bytes for example) will thus be set one and not zero. These bytes may be explicitly set to zero by the TRMP if required.

The byte location occupying the G1 location is not overwritten with 0xFF. The SIRP modifies the G1 byte when the TPAIS_EN bit is set with RDI and REI information.

When operating in OC-192/STS-192 mode, TPAIS_EN cannot be used to assert Path AIS on a single channel. In this case, the H1 and H2 mask in the TRMP #1, (Register 1069h) can be written with FFh to force transmit Path AIS on a single channel.

SS_CONCAT[1:0]

These register bits control the value of the SS field of the H1 concatenation pointer indication for the STS-192c (STM-64c) / STS-48c (STM-16c) transmit streams in OC-192 mode. In quad OC-48 mode, the SS_CONCAT[1:0] bits configure the STS-48c/STM-16c #1 data stream only.

Downloaded by Conduit Team (Gerhard Sc... Wednesday, 07 February 2007 06:59:32 PM

SS_H1[1:0]

These register bits control the value of the SS field of the H1 pointer byte of the STS-192c (STM-64c) / STS-48c (STM-16c) transmit streams in OC-192 mode. In quad OC-48 mode, the SS_H1[1:0] bits configure the STS-48c/STM-16c #1 data stream only.

APSMUX0CTL

The APS MUX0 Control (APSMUX0CTL) register bit controls whether or not the corresponding RHPPs receive data from the RRMPs (normal operation) or from the corresponding R8TD (IAPS[1][3:0]+/-) APS Port (when configured as a working mate during an APS switchover). When APSMUX0CTL is a logic 0, the RHPPs receive data normally from the RRMP. When APSMUX0CTL is a logic 1, the RHPPs receive data from the R8TD APS Port. This register bit would be set if the S/UNI 9953 is configured to terminate path in the RHPP blocks during an APS failure condition. In this configuration, the downstream packet processing blocks (RCFP, RCFP-9953) would need the data to be received from the SVCA, and thus APSMUX1CTL would be set to logic 0.

APSMUX1CTL

The APS MUX1 Control (APSMUX1CTL) register bit controls whether or not the corresponding RCFP (RCFP-9953, RXXG) receive data from the SVCAs (normal operation) or from the corresponding R8TD (IAPS[1][3:0]+/-) APS Port (when configured as a working mate during an APS switchover). When APSMUX1CTL is a logic 0, the RCFP (RCFP-9953, RXXG) receive data normally from the SVCAs. When APSMUX1CTL is a logic 1, the RCFP receive data from the R8TD APS Port. This register bit would be set if the S/UNI 9953 is configured as a working device during an APS failure condition.

APSMUX2CTL

The APS MUX2 Control (APSMUX2CTL) register bit controls whether or not data from the corresponding THPPs (normal operation) or SVCAs (when configured as the protect device) are transmitted over the T8TE (OAPS[1][3:0]+/-) APS port. When APSMUX2CTL is a logic 0, the T8TEs receive data from the THPPs (normal mode of operation). When APSMUX2CTL is a logic 1, the T8TEs receive data from the SVCAs (S/UNI 9953 is configured as a protect device). These data are transmitted over the OAPS[1][3:0]+/- port. In this mode, the S/UNI 9953 receives a SONET/SDH stream from a protect mate via the input APS port and presents the payload out through the POS-PHY Level 4 interface. The S/UNI 9953 transmits data from its POS-PHY Level 4 interface out through its output APS port to a protect mate device. It is assumed that the mate device will transmit data onto the line.

Downloaded by Copyright Datasheetminer Inc. Wednesday, 01 August 2007 06:59:32 AM

APSMUX3CTL

The APS MUX3 Control (APSMUX3CTL) register bit controls whether data received by the corresponding TRMPs are sourced from the THPPs (normal operation) or from the R8TD (IAPS[1][3:0]+/-) APS port (when the S/UNI 9953 is configured as a protect device). When APSMUX3CTL is a logic 0, the TRMPs (normal mode of operation) receive data from the THPPs. When APSMUX3CTL is a logic 1 (S/UNI 9953 is configured as a protect device), the TRMPs receive data from the R8TD (IAPS[1][3:0]+/-) APS port. Under this mode of operation the input APS port is expected to contain a bridged transmit SONET/SDH stream from a working mate device. In addition, the S/UNI 9953 will output a received SONET/SDH stream on the output APS ports to the same mate device.

IAPS_PAIS_EN

The Input APS Path AIS Enable (IAPS_PAIS_EN) register bit controls the assertion of Path AIS when link failure is detected at the input APS port for the constituent STS-48c/STM-16c #1 data stream in both OC-192 and quad OC-48 modes. When set to logic 1, Path AIS is inserted in the data stream when link failure is detected. Upon link recovery, Path AIS is de-asserted. When set to logic 0, the data stream is not affected.

IAPS_NDF_EN

The Input APS NDF Enable (IAPS_NDF_EN) register bit controls the assertion of NDF on link recovery at the input APS port for the constituent STS-48c/STM-16c #1 data stream in both OC-192 and quad OC-48 modes. When set to logic 1, NDF is inserted once in the data stream when link failure induced Path AIS is removed. When set to logic 0, the data stream is not affected. This bit has no effect when IAPS_PAIS_EN is set to logic 0.

Downloaded by Content Team of Partminer Inc. on Wednesday 01 February, 2012 03:38:22 PM

Register 0008H: S/UNI 9953 Transmit and APS Configuration 2

Bit	Type	Function	Default
Bit 15	R/W	IAPS_NDF_EN	0
Bit 14	R/W	IAPS_PAIS_EN	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	APSMUX0CTL	0
Bit 10	R/W	APSMUX1CTL	0
Bit 9	R/W	APSMUX2CTL	0
Bit 8	R/W	APSMUX3CTL	0
Bit 7	R/W	SS_H1[1]	1
Bit 6	R/W	SS_H1[0]	0
Bit 5	R/W	SS_CONCAT[1]	0
Bit 4	R/W	SS_CONCAT[0]	0
Bit 3	R/W	TPAIS_EN	0
Bit 2	R/W	TLD_VAL	0
Bit 1	R/W	TSLD_VAL	0
Bit 0	R/W	LOCK0	0

Registers 0x0007 – 0x000A controls a) the configuration of the S/UNI 9953 transmit SONET/SDH frame, b) input APS consequential actions, and c) the configuration of the APS muxes.

Groups b) and c) defined above are controlled independently of the device mode (ie concatenated, channelised, or quad modes). These bits must be set for each STS-48c/STM-16c slice. This applies to bits APSMUX[n]CTL, IAPS_PAIS_EN and IAPS_NDF_EN.

Group a) is controlled independently in quad STS-48c/STM-16c, or channelized STS-192/STM-64 modes. In concatenated STS-192c/STM-64c mode, register 0x0007 (ie slice #1) controls all of group a) functions. This applies to bits LOCK0, TSLD_VAL, TLD_VAL, TPAIS_EN, SS_CONCAT, and SS_H1.

LOCK0

This bit controls the generation of the J1 Path Overhead Byte location for the transmit direction, and thus, the H1 H2 pointer value for the transmit direction. When set to logic 0, the H1 H2 pointer value is set at 522. This is the normal pointer location for ATM configuration. When set to logic 1, the H1 H2 pointer value is set at 0. This register bit configures the STS-48c/STM-16c #2 data stream in quad OC-48 mode only.

Downloaded by Conrad Stream of Nortel Networks on Wednesday, 07 February, 2007 06:39:32 PM

TSLD_VAL

The TSLD value (TSLD_VAL) bit is used to set the value optionally inserted into the section DCC (D1-D3) in the transmit data stream as configured using the TSLDEN bit in the TRMP Configuration register. When set to logic 1, ones are inserted. When set to logic 0, zeros are inserted. This register bit configures the STS-48c/STM-16c #2 data stream in quad OC-48 mode only.

TLD_VAL

The TLD value (TLD_VAL) bit is used to set the value optionally inserted into the line DCC (D4-D12) in the transmit data stream as configured using the TLDEN bit in the TRMP Configuration register. When set to logic 1, ones are inserted. When set to logic 0, zeros are inserted. This register bit configures the STS-48c/STM-16c #2 data stream in quad OC-48 mode only.

TPAIS_EN

The Transmit Path AIS Enable bit controls the insertion of Transmit Path AIS in corresponding data stream. When logic 0, the S/UNI 9953 does not generate Transmit Path AIS. When logic 1, the S/UNI 9953 will generate Transmit Path AIS. This register bit configures the STS-48c/STM-16c #2 data stream in quad OC-48 mode only.

Note that setting the TPAIS_EN bit causes all TOH bytes upstream of the TRMP to be set to all ones, as well as the SPE bytes. The TRMP will then over-ride any necessary TOH bytes. Any TOH bytes not explicity set by the TRMP (pass through bytes for example) will thus be set one and not zero. These bytes may be explicitly set to zero by the TRMP if required.

The byte location occupying the G1 location is not overwritten with 0xFF. The SIRP modifies the G1 byte when the TPAIS_EN bit is set with RDI and REI information.

When operating in OC-192/STS-192 mode, TPAIS_EN cannot be used to assert Path AIS on a single channel. In this case, the H1 and H2 mask in the TRMP #5, (Register 1469h) can be written with FFh to force transmit Path AIS on a single channel.

SS_CONCAT[1:0]

These register bits control the value of the SS field of the H1 concatenation pointer indication for the STS-48c (STM-16c) #2 transmit stream in quad OC-48 mode only.

SS_H1[1:0]

These register bits control the value of the SS field of the H1 pointer byte of the STS-48c (STM-16c) #2 transmit stream in quad OC-48 mode only.

Downloaded by Content Team of Chamber Inc. Wednesday, 07 February 2007 06:58:32 AM

APSMUX0CTL

The APS MUX0 Control (APSMUX0CTL) register bit controls whether or not the corresponding RHPPs receive data from the RRMPs (normal operation) or from the corresponding R8TD (IAPS[2][3:0]+/-) APS Port (when configured as a working mate during an APS switchover). When APSMUX0CTL is a logic 0, the RHPPs receive data normally from the RRMP. When APSMUX0CTL is a logic 1, the RHPPs receive data from the R8TD APS Port. This register bit would be set if the S/UNI 9953 is configured to terminate path in the RHPP blocks during an APS failure condition. In this configuration, the downstream packet processing blocks (RCFP, RCFP-9953) would need the data to be received from the SVCA, and thus APSMUX1CTL would be set to logic 0.

APSMUX1CTL

The APS MUX1 Control (APSMUX1CTL) register bit controls whether or not the corresponding RCFP (RCFP-9953, RXXG) receive data from the SVCAs (normal operation) or from the corresponding R8TD (IAPS[2][3:0]+/-) APS Port (when configured as a working mate during an APS switchover). When APSMUX1CTL is a logic 0, the RCFP (RCFP-9953, RXXG) receive data normally from the SVCAs. When APSMUX1CTL is a logic 1, the RCFP receive data from the R8TD APS Port. This register bit would be set if the S/UNI 9953 is configured as a working device during an APS failure condition.

APSMUX2CTL

The APS MUX2 Control (APSMUX2CTL) register bit controls whether or not data from the corresponding THPPs (normal operation) or SVCAs (when configured as the protect device) are transmitted over the T8TE (OAPS[2][3:0]+/-) APS port. When APSMUX2CTL is a logic 0, the T8TEs receive data from the THPPs (normal mode of operation). When APSMUX2CTL is a logic 1, the T8TEs receive data from the SVCAs (S/UNI 9953 is configured as a protect device). These data are transmitted over the OAPS[2][3:0]+/- port. In this mode, the S/UNI 9953 receives a SONET/SDH stream from a protect mate via the input APS port and presents the payload out through the POS-PHY Level 4 interface. The S/UNI 9953 transmits data from its POS-PHY Level 4 interface out through its output APS port to a protect mate device. It is assumed that the mate device will transmit data onto the line.

Downloaded by Content Team on Wednesday, 27 February, 2013 05:50:02 PM

APSMUX3CTL

The APS MUX3 Control (APSMUX3CTL) register bit controls whether data received by the corresponding TRMPs are sourced from the THPPs (normal operation) or from the R8TD (IAPS[2][3:0]+/-) APS port (when the S/UNI 9953 is configured as a protect device). When APSMUX3CTL is a logic 0, the TRMPs (normal mode of operation) receive data from the THPPs. When APSMUX3CTL is a logic 1 (S/UNI 9953 is configured as a protect device), the TRMPs receive data from the R8TD (IAPS[2][3:0]+/-) APS port. Under this mode of operation the input APS port is expected to contain a bridged transmit SONET/SDH stream from a working mate device. In addition, the S/UNI 9953 will output a received SONET/SDH stream on the output APS ports to the same mate device.

IAPS_PAIS_EN

The Input APS Path AIS Enable (IAPS_PAIS_EN) register bit controls the assertion of Path AIS when link failure is detected at the input APS port for the constituent STS-48c/STM-16c #2 data stream in both OC-192 and quad OC-48 modes. When set to logic 1, Path AIS is inserted in the data stream when link failure is detected. Upon link recovery, Path AIS is de-asserted. When set to logic 0, the data stream is not affected.

IAPS_NDF_EN

The Input APS NDF Enable (IAPS_NDF_EN) register bit controls the assertion of NDF on link recovery at the input APS port for the constituent STS-48c/STM-16c #2 data stream in both OC-192 and quad OC-48 modes. When set to logic 1, NDF is inserted once in the data stream when link failure induced Path AIS is removed. When set to logic 0, the data stream is not affected. This bit has no effect when IAPS_PAIS_EN is set to logic 0.

Downloaded by Content Team of Partminer Inc. on Wednesday 19 February, 2014 at 08:38:22 AM

Register 0009H: S/UNI 9953 Transmit and APS Configuration 3

Bit	Type	Function	Default
Bit 15	R/W	IAPS_NDF_EN	0
Bit 14	R/W	IAPS_PAIS_EN	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	APSMUX0CTL	0
Bit 10	R/W	APSMUX1CTL	0
Bit 9	R/W	APSMUX2CTL	0
Bit 8	R/W	APSMUX3CTL	0
Bit 7	R/W	SS_H1[1]	1
Bit 6	R/W	SS_H1[0]	0
Bit 5	R/W	SS_CONCAT[1]	0
Bit 4	R/W	SS_CONCAT[0]	0
Bit 3	R/W	TPAIS_EN	0
Bit 2	R/W	TLD_VAL	0
Bit 1	R/W	TSLD_VAL	0
Bit 0	R/W	LOCK0	0

Registers 0x0007 – 0x000A controls a) the configuration of the S/UNI 9953 transmit SONET/SDH frame, b) input APS consequential actions, and c) the configuration of the APS muxes.

Groups b) and c) defined above are controlled independently of the device mode (ie concatenated, channelised, or quad modes). These bits must be set for each STS-48c/STM-16c slice. This applies to bits APSMUX[n]CTL, IAPS_PAIS_EN and IAPS_NDF_EN.

Group a) is controlled independently in quad STS-48c/STM-16c, or channelized STS-192/STM-64 modes. In concatenated STS-192c/STM-64c mode, register 0x0007 (ie slice #1) controls all of group a) functions. This applies to bits LOCK0, TSLD_VAL, TLD_VAL, TPAIS_EN, SS_CONCAT, and SS_H1.

LOCK0

This bit controls the generation of the J1 Path Overhead Byte location for the transmit direction, and thus, the H1 H2 pointer value for the transmit direction. When set to logic 0, the H1 H2 pointer value is set at 522. This is the normal pointer location for ATM configuration. When set to logic 1, the H1 H2 pointer value is set at 0. This register bit configures the STS-48c/STM-16c #3 data stream in quad OC-48 mode only.

Downloaded by Conexant Systems on Wednesday, 07 February, 2007 06:39:32 PM

TSLD_VAL

The TSLD value (TSLD_VAL) bit is used to set the value optionally inserted into the section DCC (D1-D3) in the transmit data stream as configured using the TSLDEN bit in the TRMP Configuration register. When set to logic 1, ones are inserted. When set to logic 0, zeros are inserted. This register bit configures the STS-48c/STM-16c #3 data stream in quad OC-48 mode only.

TLD_VAL

The TLD value (TLD_VAL) bit is used to set the value optionally inserted into the line DCC (D4-D12) in the transmit data stream as configured using the TLDEN bit in the TRMP Configuration register. When set to logic 1, ones are inserted. When set to logic 0, zeros are inserted. This register bit configures the STS-48c/STM-16c #3 data stream in quad OC-48 mode only.

TPAIS_EN

The Transmit Path AIS Enable bit controls the insertion of Transmit Path AIS in corresponding data stream. When logic 0, the S/UNI 9953 does not generate Transmit Path AIS. When logic 1, the S/UNI 9953 will generate Transmit Path AIS. This register bit configures the STS-48c/STM-16c #3 data stream in quad OC-48 mode only.

Note that setting the TPAIS_EN bit causes all TOH bytes upstream of the TRMP to be set to all ones, as well as the SPE bytes. The TRMP will then over-ride any necessary TOH bytes. Any TOH bytes not explicity set by the TRMP (pass through bytes for example) will thus be set one and not zero. These bytes may be explicitly set to zero by the TRMP if required.

The byte location occupying the G1 location is not overwritten with 0xFF. The SIRP modifies the G1 byte when the TPAIS_EN bit is set with RDI and REI information.

When operating in OC-192/STS-192 mode, TPAIS_EN cannot be used to assert Path AIS on a single channel. In this case, the H1 and H2 mask in the TRMP #9, (Register 1869h) can be written with FFh to force transmit Path AIS on a single channel.

SS_CONCAT[1:0]

These register bits control the value of the SS field of the H1 concatenation pointer indication for the STS-48c (STM-16c) #3 transmit stream in quad OC-48 mode only.

SS_H1[1:0]

These register bits control the value of the SS field of the H1 pointer byte of the STS-48c (STM-16c) #3 transmit stream in quad OC-48 mode only.

Downloaded by Content Team of Chamber Inc. Wednesday, 07 February 2007 06:58:32 AM

APSMUX0CTL

The APS MUX0 Control (APSMUX0CTL) register bit controls whether or not the corresponding RHPPs receive data from the RRMPs (normal operation) or from the corresponding R8TD (IAPS[3][3:0]+/-) APS Port (when configured as a working mate during an APS switchover). When APSMUX0CTL is a logic 0, the RHPPs receive data normally from the RRMP. When APSMUX0CTL is a logic 1, the RHPPs receive data from the R8TD APS Port. This register bit would be set if the S/UNI 9953 is configured to terminate path in the RHPP blocks during an APS failure condition. In this configuration, the downstream packet processing blocks (RCFP, RCFP-9953) would need the data to be received from the SVCA, and thus APSMUX1CTL would be set to logic 0.

APSMUX1CTL

The APS MUX1 Control (APSMUX1CTL) register bit controls whether or not the corresponding RCFP (RCFP-9953, RXXG) receive data from the SVCAs (normal operation) or from the corresponding R8TD (IAPS[3][3:0]+/-) APS Port (when configured as a working mate during an APS switchover). When APSMUX1CTL is a logic 0, the RCFP (RCFP-9953, RXXG) receive data normally from the SVCAs. When APSMUX1CTL is a logic 1, the RCFP receive data from the R8TD APS Port. This register bit would be set if the S/UNI 9953 is configured as a working device during an APS failure condition.

APSMUX2CTL

The APS MUX2 Control (APSMUX2CTL) register bit controls whether or not data from the corresponding THPPs (normal operation) or SVCAs (when configured as the protect device) are transmitted over the T8TE (OAPS[3][3:0]+/-) APS port. When APSMUX2CTL is a logic 0, the T8TEs receive data from the THPPs (normal mode of operation). When APSMUX2CTL is a logic 1, the T8TEs receive data from the SVCAs (S/UNI 9953 is configured as a protect device). These data are transmitted over the OAPS[3][3:0]+/- port. In this mode, the S/UNI 9953 receives a SONET/SDH stream from a protect mate via the input APS port and presents the payload out through the POS-PHY Level 4 interface. The S/UNI 9953 transmits data from its POS-PHY Level 4 interface out through its output APS port to a protect mate device. It is assumed that the mate device will transmit data onto the line.

Downloaded by Content Team on Wednesday, 27 February, 2013 05:50:02 PM

APSMUX3CTL

The APS MUX3 Control (APSMUX3CTL) register bit controls whether data received by the corresponding TRMPs are sourced from the THPPs (normal operation) or from the R8TD (IAPS[3][3:0]+/-) APS port (when the S/UNI 9953 is configured as a protect device). When APSMUX3CTL is a logic 0, the TRMPs (normal mode of operation) receive data from the THPPs. When APSMUX3CTL is a logic 1 (S/UNI 9953 is configured as a protect device), the TRMPs receive data from the R8TD (IAPS[3][3:0]+/-) APS port. Under this mode of operation the input APS port is expected to contain a bridged transmit SONET/SDH stream from a working mate device. In addition, the S/UNI 9953 will output a received SONET/SDH stream on the output APS ports to the same mate device.

IAPS_PAIS_EN

The Input APS Path AIS Enable (IAPS_PAIS_EN) register bit controls the assertion of Path AIS when link failure is detected at the input APS port for the constituent STS-48c/STM-16c #3 data stream in both OC-192 and quad OC-48 modes. When set to logic 1, Path AIS is inserted in the data stream when link failure is detected. Upon link recovery, Path AIS is de-asserted. When set to logic 0, the data stream is not affected.

IAPS_NDF_EN

The Input APS NDF Enable (IAPS_NDF_EN) register bit controls the assertion of NDF on link recovery at the input APS port for the constituent STS-48c/STM-16c #3 data stream in both OC-192 and quad OC-48 modes. When set to logic 1, NDF is inserted once in the data stream when link failure induced Path AIS is removed. When set to logic 0, the data stream is not affected. This bit has no effect when IAPS_PAIS_EN is set to logic 0.

Downloaded by Content Team of Partminer Inc. on Wednesday 01 February, 2006 05:58:32 PM

Register 000AH: S/UNI 9953 Transmit and APS Configuration 4

Bit	Type	Function	Default
Bit 15	R/W	IAPS_NDF_EN	0
Bit 14	R/W	IAPS_PAIS_EN	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	APSMUX0CTL	0
Bit 10	R/W	APSMUX1CTL	0
Bit 9	R/W	APSMUX2CTL	0
Bit 8	R/W	APSMUX3CTL	0
Bit 7	R/W	SS_H1[1]	1
Bit 6	R/W	SS_H1[0]	0
Bit 5	R/W	SS_CONCAT[1]	0
Bit 4	R/W	SS_CONCAT[0]	0
Bit 3	R/W	TPAIS_EN	0
Bit 2	R/W	TLD_VAL	0
Bit 1	R/W	TSLD_VAL	0
Bit 0	R/W	LOCK0	0

Registers 0x0007 – 0x000A controls a) the configuration of the S/UNI 9953 transmit SONET/SDH frame, b) input APS consequential actions, and c) the configuration of the APS muxes.

Groups b) and c) defined above are controlled independently of the device mode (ie concatenated, channelised, or quad modes). These bits must be set for each STS-48c/STM-16c slice. This applies to bits APSMUX[n]CTL, IAPS_PAIS_EN and IAPS_NDF_EN.

Group a) is controlled independently in quad STS-48c/STM-16c, or channelized STS-192/STM-64 modes. In concatenated STS-192c/STM-64c mode, register 0x0007 (ie slice #1) controls all of group a) functions. This applies to bits LOCK0, TSLD_VAL, TLD_VAL, TPAIS_EN, SS_CONCAT, and SS_H1.

LOCK0

This bit controls the generation of the J1 Path Overhead Byte location for the transmit direction, and thus, the H1 H2 pointer value for the transmit direction. When set to logic 0, the H1 H2 pointer value is set at 522. This is the normal pointer location for ATM configuration. When set to logic 1, the H1 H2 pointer value is set at 0. This register bit configures the STS-48c/STM-16c #4 data stream in quad OC-48 mode only.

Downloaded by Conexant Stream of Mindspeed on Wednesday, 07 February, 2007 06:39:32 PM

TSLD_VAL

The TSLD value (TSLD_VAL) bit is used to set the value optionally inserted into the section DCC (D1-D3) in the transmit data stream as configured using the TSLDEN bit in the TRMP Configuration register. When set to logic 1, ones are inserted. When set to logic 0, zeros are inserted. This register bit configures the STS-48c/STM-16c #4 data stream in quad OC-48 mode only.

TLD_VAL

The TLD value (TLD_VAL) bit is used to set the value optionally inserted into the line DCC (D4-D12) in the transmit data stream as configured using the TLDEN bit in the TRMP Configuration register. When set to logic 1, ones are inserted. When set to logic 0, zeros are inserted. This register bit configures the STS-48c/STM-16c #4 data stream in quad OC-48 mode only.

TPAIS_EN

The Transmit Path AIS Enable bit controls the insertion of Transmit Path AIS in corresponding data stream. When logic 0, the S/UNI 9953 does not generate Transmit Path AIS. When logic 1, the S/UNI 9953 will generate Transmit Path AIS. This register bit configures the STS-48c/STM-16c #4 data stream in quad OC-48 mode only.

Note that setting the TPAIS_EN bit causes all TOH bytes upstream of the TRMP to be set to all ones, as well as the SPE bytes. The TRMP will then over-ride any necessary TOH bytes. Any TOH bytes not explicity set by the TRMP (pass through bytes for example) will thus be set one and not zero. These bytes may be explicitly set to zero by the TRMP if required.

The byte location occupying the G1 location is not overwritten with 0xFF. The SIRP modifies the G1 byte when the TPAIS_EN bit is set with RDI and REI information.

When operating in OC-192/STS-192 mode, TPAIS_EN cannot be used to assert Path AIS on a single channel. In this case, the H1 and H2 mask in the TRMP #13, (Register 1C69h) can be written with FFh to force transmit Path AIS on a single channel.

SS_CONCAT[1:0]

These register bits control the value of the SS field of the H1 concatenation pointer indication for the STS-48c (STM-16c) #4 transmit stream in quad OC-48 mode only.

SS_H1[1:0]

These register bits control the value of the SS field of the H1 pointer byte of the STS-48c (STM-16c) #4 transmit stream in quad OC-48 mode only.

Downloaded by Content Team of Chinese Internet Solutions, 07 Febr... 2007 06:...2 PM

APSMUX0CTL

The APS MUX0 Control (APSMUX0CTL) register bit controls whether or not the corresponding RHPPs receive data from the RRMPs (normal operation) or from the corresponding R8TD (IAPS[4][3:0]+/-) APS Port (when configured as a working mate during an APS switchover). When APSMUX0CTL is a logic 0, the RHPPs receive data normally from the RRMP. When APSMUX0CTL is a logic 1, the RHPPs receive data from the R8TD APS Port. This register bit would be set if the S/UNI 9953 is configured to terminate path in the RHPP blocks during an APS failure condition. In this configuration, the downstream packet processing blocks (RCFP, RCFP-9953) would need the data to be received from the SVCA, and thus APSMUX1CTL would be set to logic 0.

APSMUX1CTL

The APS MUX1 Control (APSMUX1CTL) register bit controls whether or not the corresponding RCFP (RCFP-9953, RXXG) receive data from the SVCAs (normal operation) or from the corresponding R8TD (IAPS[4][3:0]+/-) APS Port (when configured as a working mate during an APS switchover). When APSMUX1CTL is a logic 0, the RCFP (RCFP-9953, RXXG) receive data normally from the SVCAs. When APSMUX1CTL is a logic 1, the RCFP receive data from the R8TD APS Port. This register bit would be set if the S/UNI 9953 is configured as a working device during an APS failure condition.

APSMUX2CTL

The APS MUX2 Control (APSMUX2CTL) register bit controls whether or not data from the corresponding THPPs (normal operation) or SVCAs (when configured as the protect device) are transmitted over the T8TE (OAPS[4][3:0]+/-) APS port. When APSMUX2CTL is a logic 0, the T8TEs receive data from the THPPs (normal mode of operation). When APSMUX2CTL is a logic 1, the T8TEs receive data from the SVCAs (S/UNI 9953 is configured as a protect device). These data are transmitted over the OAPS[4][3:0]+/- port. In this mode, the S/UNI 9953 receives a SONET/SDH stream from a protect mate via the input APS port and presents the payload out through the POS-PHY Level 4 interface. The S/UNI 9953 transmits data from its POS-PHY Level 4 interface out through its output APS port to a protect mate device. It is assumed that the mate device will transmit data onto the line.

Downloaded by Content Team on Wednesday, 01 February, 2006 05:02 PM

APSMUX3CTL

The APS MUX3 Control (APSMUX3CTL) register bit controls whether data received by the corresponding TRMPs are sourced from the THPPs (normal operation) or from the R8TD (IAPS[4][3:0]+/-) APS port (when the S/UNI 9953 is configured as a protect device). When APSMUX3CTL is a logic 0, the TRMPs (normal mode of operation) receive data from the THPPs. When APSMUX3CTL is a logic 1 (S/UNI 9953 is configured as a protect device), the TRMPs receive data from the R8TD (IAPS[4][3:0]+/-) APS port. Under this mode of operation the input APS port is expected to contain a bridged transmit SONET/SDH stream from a working mate device. In addition, the S/UNI 9953 will output a received SONET/SDH stream on the output APS ports to the same mate device.

IAPS_PAIS_EN

The Input APS Path AIS Enable (IAPS_PAIS_EN) register bit controls the assertion of Path AIS when link failure is detected at the input APS port for the constituent STS-48c/STM-16c #4 data stream in both OC-192 and quad OC-48 modes. When set to logic 1, Path AIS is inserted in the data stream when link failure is detected. Upon link recovery, Path AIS is de-asserted. When set to logic 0, the data stream is not affected.

IAPS_NDF_EN

The Input APS NDF Enable (IAPS_NDF_EN) register bit controls the assertion of NDF on link recovery at the input APS port for the constituent STS-48c/STM-16c #4 data stream in both OC-192 and quad OC-48 modes. When set to logic 1, NDF is inserted once in the data stream when link failure induced Path AIS is removed. When set to logic 0, the data stream is not affected. This bit has no effect when IAPS_PAIS_EN is set to logic 0.

Downloaded by Content Team of Partminer Inc. on Wednesday 19 February, 2014 at 08:38:22 AM

Register 000BH: Software General Purpose (FREE[15:0]) Register

Bit	Type	Function	Default
Bit 15	R/W	FREE[15]	0
Bit 14	R/W	FREE[14]	0
Bit 13	R/W	FREE[13]	0
Bit 12	R/W	FREE[12]	0
Bit 11	R/W	FREE[11]	0
Bit 10	R/W	FREE[10]	0
Bit 9	R/W	FREE[9]	0
Bit 8	R/W	FREE[8]	0
Bit 7	R/W	FREE[7]	0
Bit 6	R/W	FREE[6]	0
Bit 5	R/W	FREE[5]	0
Bit 4	R/W	FREE[4]	0
Bit 3	R/W	FREE[3]	0
Bit 2	R/W	FREE[2]	0
Bit 1	R/W	FREE[1]	0
Bit 0	R/W	FREE[0]	0

FREE[15:0]

General-purpose register bits. These do not affect the operation of the device in any way but will hold a value written to them.

This register may be used as a software diagnostic register, in order to verify device read/write operation.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:09:32 PM

Register 000CH: APS Input TelecomBus Synchronization Delay

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R/W	AIJ0DLY[13]	0
Bit 12	R/W	AIJ0DLY[12]	0
Bit 11	R/W	AIJ0DLY[11]	0
Bit 10	R/W	AIJ0DLY[10]	0
Bit 9	R/W	AIJ0DLY[9]	0
Bit 8	R/W	AIJ0DLY[8]	0
Bit 7	R/W	AIJ0DLY[7]	0
Bit 6	R/W	AIJ0DLY[6]	0
Bit 5	R/W	AIJ0DLY[5]	1
Bit 4	R/W	AIJ0DLY[4]	0
Bit 3	R/W	AIJ0DLY[3]	0
Bit 2	R/W	AIJ0DLY[2]	0
Bit 1	R/W	AIJ0DLY[1]	0
Bit 0	R/W	AIJ0DLY[0]	0

This register controls the delay from the IAPSFP input signal to the time when the S/UNI 9953 may safely process the J0 characters delivered by the APS Input serial data links (IAPS[4:1][3:0]+/-).

AIJ0DLY[13:0]

The APS Input transport frame delay bits (AIJ0DLY[13:0]) controls the delay, in IAPSFPCLK cycles, inserted by the S/UNI 9953 before processing the J0 characters delivered by the APS Input serial data links (IAPS[4:1][3:0]+/-). AIJ0DLY is set such that after the specified delay, all active APS Input links would have delivered the J0 character. The relationships of IAPSFP, AIJ0DLY[13:0] and the system configuration are described in the Functional Timing section. Valid values of AIJ0DLY[13:0] are 0000H to 25F7H.

Note that for the case where the OAPS port of the PM5390 is directly connected to the IAPS port (for diagnostics for example), then a value for the AIJ0DLY[13:0] would be 0x0030.

Downloaded by Content Team on Synchronet Inc on Wednesday, 07 February, 2007 06:39:32 PM

Register 000DH: APS Output TelecomBus Synchronization Delay

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R/W	AOJ0REFDLY[13]	0
Bit 12	R/W	AOJ0REFDLY[12]	0
Bit 11	R/W	AOJ0REFDLY[11]	0
Bit 10	R/W	AOJ0REFDLY[10]	0
Bit 9	R/W	AOJ0REFDLY[9]	0
Bit 8	R/W	AOJ0REFDLY[8]	0
Bit 7	R/W	AOJ0REFDLY[7]	0
Bit 6	R/W	AOJ0REFDLY[6]	0
Bit 5	R/W	AOJ0REFDLY[5]	0
Bit 4	R/W	AOJ0REFDLY[4]	0
Bit 3	R/W	AOJ0REFDLY[3]	0
Bit 2	R/W	AOJ0REFDLY[2]	0
Bit 1	R/W	AOJ0REFDLY[1]	0
Bit 0	R/W	AOJ0REFDLY[0]	0

This register controls the delay from the IAPSFP input signal to the time when the S/UNI 9953 produces the J0 pulse on the APS Output serial data links (OAPS[4:1][3:0]+/-)

AOJ0REFDLY[13:0]

The APS Output transport frame delay bits (AOJ0REFDLY [13:0]) control the delay, in IAPSFPCLK cycles, inserted by the S/UNI 9953 between receiving a reference J0 frame pulse on IAPSFP, and presenting the outgoing J0 character on OAPS[4:1][3:0]+/-. The relationships of IAPSFP, AOJ0REFDLY [13:0] and the system configuration are described in the Functional Timing section. Valid values of AOJ0REFDLY [13:0] are 0000H to 25F7H

Downloaded by Content Team of Parts Engine on Wednesday, 07 February, 2007 06:09:32 PM

Register 000EH: S/UNI 9953 Diagnostics

Bit	Type	Function	Default
Bit 15	R/W	IAPSFP_THRESH[7]	0
Bit 14	R/W	IAPSFP_THRESH[6]	0
Bit 13	R/W	IAPSFP_THRESH[5]	0
Bit 12	R/W	IAPSFP_THRESH[4]	1
Bit 11	R/W	IAPSFP_THRESH[3]	0
Bit 10	R/W	IAPSFP_THRESH[2]	0
Bit 9	R/W	IAPSFP_THRESH[1]	0
Bit 8	R/W	IAPSFP_THRESH[0]	0
Bit 7	R/W	DIAGSHORT	0
Bit 6	R/W	SVCA_ESDIS	0
Bit 5	—	Unused	X
Bit 4	R/W	TX_OH_EN	0
Bit 3	R/W	TXJ0DLYEN	0
Bit 2	R/W	OAPSFPDLYEN	1
Bit 1	R/W	DS	0
Bit 0	R/W	DD	0

DD

The Disable Descrambling (DD) bit is used to disable SONET descrambling performed by the RRMP block. When set to logic 1, SONET descrambling is disabled. When set to logic 0, SONET descrambling is enabled. For normal operation, this bit should be set to logic zero.

DS

The Disable Scrambling (DS) bit is used to disable SONET scrambling performed by the TRMP block. When set to logic 1, SONET scrambling is disabled. When set to logic 0, SONET scrambling is enabled. For normal operation, this bit should be set to logic zero.

OAPSFPDLYEN

This register bit is for PMC debug purposes only, and must be left in its default setting for proper operation of the S/UNI 9953.

TXJ0DLYEN

This register bit is for PMC debug purposes only, and must be left in its default setting for proper operation of the S/UNI 9953.

Downloaded by ContentTeam of Platminer Inc. on Wednesday, 07 February, 2007 06:59:32 PM

TX_OH_EN

This register bit is for PMC debug purposes only, and must be left in its default setting for proper operation of the S/UNI 9953.

SVCA_ESDIS

The SVCA elastic store disable (SVCA_ESDIS) bit is used to disable the elastic store. This bit should normally be set to 0.

DIAGSHORT

The diagnostic short frame (DIAGSHORT) bit sets a reduced frame size. This register bit is for test purposes only.

IAPSFP_THRESH[7:0]

This field is for PMC debug purposes only, and must be left in its default setting for proper operation of the S/UNI 9953.

Downloaded by Content Team of Partminer Inc on Wednesday 07 February, 2007 06:59:32 PM

Register 000FH: S/UNI 9953 Identification Register

Bit	Type	Function	Default
Bit 15	R	CHIPID[15]	0
Bit 14	R	CHIPID[14]	1
Bit 13	R	CHIPID[13]	0
Bit 12	R	CHIPID[12]	1
Bit 11	R	CHIPID[11]	0
Bit 10	R	CHIPID[10]	0
Bit 9	R	CHIPID[9]	1
Bit 8	R	CHIPID[8]	1
Bit 7	R	CHIPID[7]	1
Bit 6	R	CHIPID[6]	0
Bit 5	R	CHIPID[5]	0
Bit 4	R	CHIPID[4]	1
Bit 3	R	CHIPID[3]	0
Bit 2	R	CHIPID[2]	0
Bit 1	R	CHIPID[1]	0
Bit 0	R	CHIPID[0]	0

CHIPID[15:0]

The CHIPID[15:0] is set to 5390H to identify the PM5390 S/UNI 9953.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:09:32 PM

Register 0010H: S/UNI 9953 Master Payload Interrupt Status

Bit	Type	Function	Default
Bit 15	R/W	INTE	0
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	R	TXXGI	X
Bit 11	R	T64B66BI	X
Bit 10	R	TCFP9953I	X
Bit 9	—	Unused	X
Bit 8	R	STLII	X
Bit 7	—	Unused	X
Bit 6	R	CSTRI	X
Bit 5	R	MSTATI	X
Bit 4	R	RXXGI	X
Bit 3	R	R64B66BI	X
Bit 2	R	RCFP9953I	X
Bit 1	—	Unused	X
Bit 0	R	SRLII	X

This register allows the source of an active interrupt to be identified down to the block level for the ATM/POS/10GbE payload processing system blocks and the SONET/SDH multiplexing/de-multiplexing blocks. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

STLII

The STLI interrupt event indication (STLII) transitions to logic 1 when a hardware interrupt event is sourced from STLI block. This bit is cleared to logic 0 when the interrupt in the STLI block is cleared.

RCFP9953I

The RCFP9953 interrupt event indication (RCFP9953I) transitions to logic 1 when a hardware interrupt event is sourced from RCFP-9953 block. This bit is cleared to logic 0 when the interrupt in the RCFP-9953 block is cleared.

R64B66BI

The R64B66B interrupt event indication (R64B66BI) transitions to logic 1 when a hardware interrupt event is sourced from R64B66B block. This bit is cleared to logic 0 when the interrupt in the R64B66B block is cleared.

Downloaded by Content Agent of Parameter Inc on Wednesday, 07 February, 2007 06:09:32 PM

RXXGI

The RXXG interrupt event indication (RXXGI) transitions to logic 1 when a hardware interrupt event is sourced from RXXG block. This bit is cleared to logic 0 when the interrupt in the RXXG block is cleared.

MSTATI

The MSTAT interrupt event indication (MSTATI) transitions to logic 1 when a hardware interrupt event is sourced from MSTAT block. This bit is cleared to logic 0 when the interrupt in the MSTAT block is cleared.

CSTRI

The CSTR interrupt event indication (CSTRI) transitions to logic 1 when a hardware interrupt event is sourced from CSTR block. This bit is cleared to logic 0 when the interrupt in the CSTR block is cleared.

SRLII

The SRLI interrupt event indication (SRLII) transitions to logic 1 when a hardware interrupt event is sourced from SRLI block. This bit is cleared to logic 0 when the interrupt in the SRLI block is cleared.

TCFP9953I

The TCFP9953 interrupt event indication (TCFP9953I) transitions to logic 1 when a hardware interrupt event is sourced from TCFP-9953 block. This bit is cleared to logic 0 when the interrupt in the TCFP-9953 block is cleared.

T64B66BI

The T64B66B interrupt event indication (T64B66BI) transitions to logic 1 when a hardware interrupt event is sourced from T64B66B block. This bit is cleared to logic 0 when the interrupt in the T64B66B block is cleared.

TXXGI

The TXXG interrupt event indication (TXXGI) transitions to logic 1 when a hardware interrupt event is sourced from TXXG block. This bit is cleared to logic 0 when the interrupt in the TXXG block is cleared.

Downloaded by Content Team of Partminer, Inc on Wednesday, 07 February, 2001 06:59:32 PM

INTE

The interrupt enable (INTE) bit controls the assertion of the interrupt (INTB) output. When a logic 1 is written to INTE, the pending interrupt(s) listed in this register will assert the interrupt (INTB) output. When a logic 0 is written to INTE, the pending interrupt(s) will not assert the interrupt (INTB) output.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0011H: S/UNI 9953 Master FIFO/PL4 Interrupt Status

Bit	Type	Function	Default
Bit 15	R/W	INTE	0
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	R	ERAMI	X
Bit 11	—	Unused	X
Bit 10	R	PL4IDUI	X
Bit 9	—	Unused	X
Bit 8	R	EFLXI	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R	IRAMI	X
Bit 3	R	PL4IOI	X
Bit 2	R	PL4ODPI	X
Bit 1	—	Unused	X
Bit 0	R	IFLXI	X

This register allows the source of an active interrupt to be identified down to the block level for the system FIFO and PL4 interface blocks. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

IFLXI

The IFLX interrupt event indication (IFLXI) transitions to logic 1 when a hardware interrupt event is sourced from IFLX block. This bit is cleared to logic 0 when the interrupt in the IFLX block is cleared.

PL4ODPI

The PL4ODP interrupt event indication (PL4ODPI) transitions to logic 1 when a hardware interrupt event is sourced from PL4ODP block. This bit is cleared to logic 0 when the interrupt in the PL4ODP block is cleared.

PL4IOI

The PL4IO interrupt event indication (PL4IOI) transitions to logic 1 when a hardware interrupt event is sourced from PL4IO block. This bit is cleared to logic 0 when the interrupt in the PL4IO block is cleared.

Downloaded by Content Area of Partner Inc on Wednesday, 07 February, 2007 06:39:32 PM

IRAMI

The IRAM interrupt event indication (IRAMI) transitions to logic 1 when a hardware interrupt event is sourced from IRAM block. This bit is cleared to logic 0 when the interrupt in the IRAM block is cleared.

EFLXI

The EFLX interrupt event indication (EFLXI) transitions to logic 1 when a hardware interrupt event is sourced from EFLX block. This bit is cleared to logic 0 when the interrupt in the EFLX block is cleared.

PL4IDUI

The PL4IDU interrupt event indication (PL4IDUI) transitions to logic 1 when a hardware interrupt event is sourced from PL4IDU block. This bit is cleared to logic 0 when the interrupt in the PL4IDU block is cleared.

ERAMI

The ERAM interrupt event indication (ERAMI) transitions to logic 1 when a hardware interrupt event is sourced from ERAM block. This bit is cleared to logic 0 when the interrupt in the ERAM block is cleared.

INTE

The interrupt enable (INTE) bit controls the assertion of the interrupt (INTB) output. When a logic 1 is written to INTE, the pending interrupt(s) listed in this register will assert the interrupt (INTB) output. When a logic 0 is written to INTE, the pending interrupt(s) will not assert the interrupt (INTB) output.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0012H: S/UNI 9953 Line Loop-Back FIFO Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R	LLB_FIFOSLIP4I	X
Bit 2	R	LLB_FIFOSLIP3I	X
Bit 1	R	LLB_FIFOSLIP2I	X
Bit 0	R	LLB_FIFOSLIP1I	X

The S/UNI 9953 Line Loop-Back FIFO Status Register is reserved and provided for diagnostic purposes only.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0013H: S/UNI 9953 Diagnostic Loop-Back FIFO Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R	DLB_FIFOSLIP4I	X
Bit 2	R	DLB_FIFOSLIP3I	X
Bit 1	R	DLB_FIFOSLIP2I	X
Bit 0	R	DLB_FIFOSLIP1I	X

The S/UNI 9953 Diagnostic Loop-Back FIFO Status Register is reserved and provided for diagnostic purposes only.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0014H: S/UNI 9953 PCS LOS Threshold

Bit	Type	Function	Default
Bit 15	R/W	PCS_LOS_TH[17]	0
Bit 14	R/W	PCS_LOS_TH[16]	1
Bit 13	R/W	PCS_LOS_TH[15]	0
Bit 12	R/W	PCS_LOS_TH[14]	0
Bit 11	R/W	PCS_LOS_TH[13]	1
Bit 10	R/W	PCS_LOS_TH[12]	0
Bit 9	R/W	PCS_LOS_TH[11]	1
Bit 8	R/W	PCS_LOS_TH[10]	1
Bit 7	R/W	PCS_LOS_TH[7]	1
Bit 6	R/W	PCS_LOS_TH[6]	1
Bit 5	R/W	PCS_LOS_TH[5]	1
Bit 4	R/W	PCS_LOS_TH[4]	1
Bit 3	R/W	PCS_LOS_TH[3]	0
Bit 2	R/W	PCS_LOS_TH[2]	0
Bit 1	R/W	PCS_LOS_TH[1]	0
Bit 0	R/W	PCS_LOS_TH[0]	0

PCS_LOS_TH[15:0]

This field is for PMC debug purposes only, and must be left in its default setting for proper operation of the S/UNI 9953.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0015H: S/UNI 9953 PCS LOSB Threshold

Bit	Type	Function	Default
Bit 15	R/W	PCS_LOSB_TH[17]	0
Bit 14	R/W	PCS_LOSB_TH[16]	0
Bit 13	R/W	PCS_LOSB_TH[15]	0
Bit 12	R/W	PCS_LOSB_TH[14]	1
Bit 11	R/W	PCS_LOSB_TH[13]	1
Bit 10	R/W	PCS_LOSB_TH[12]	0
Bit 9	R/W	PCS_LOSB_TH[11]	0
Bit 8	R/W	PCS_LOSB_TH[10]	1
Bit 7	R/W	PCS_LOSB_TH[7]	0
Bit 6	R/W	PCS_LOSB_TH[6]	1
Bit 5	R/W	PCS_LOSB_TH[5]	0
Bit 4	R/W	PCS_LOSB_TH[4]	1
Bit 3	R/W	PCS_LOSB_TH[3]	0
Bit 2	R/W	PCS_LOSB_TH[2]	0
Bit 1	R/W	PCS_LOSB_TH[1]	0
Bit 0	R/W	PCS_LOSB_TH[0]	0

PCS_LOSB_TH[15:0]

This field is for PMC debug purposes only, and must be left in its default setting for proper operation of the S/UNI 9953.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0016H: S/UNI 9953 Input APS Frame Alignment Interrupt Status 1

Bit	Type	Function	Default
Bit 15	R	NO_DJ016I	X
Bit 14	R	NO_DJ015I	X
Bit 13	R	NO_DJ014I	X
Bit 12	R	NO_DJ013I	X
Bit 11	R	NO_DJ012I	X
Bit 10	R	NO_DJ011I	X
Bit 9	R	NO_DJ010I	X
Bit 8	R	NO_DJ09I	X
Bit 7	R	NO_DJ08I	X
Bit 6	R	NO_DJ07I	X
Bit 5	R	NO_DJ06I	X
Bit 4	R	NO_DJ05I	X
Bit 3	R	NO_DJ04I	X
Bit 2	R	NO_DJ03I	X
Bit 1	R	NO_DJ02I	X
Bit 0	R	NO_DJ01I	X

NO_DJ0[N]I

The No Detected J0 Error Interrupt status (NO_DJ0[N]I) bit is an event indicator for the IAPS[x][y] input data stream. NO_DJ0[N]I is set to logic one to indicate that no input J0 was detected at the expected position as programmed via the AIJ0DLY[13:0] register bits. This interrupt status can activate the INTB output if the corresponding interrupt enable bit, NO_DJ0E, is set to logic one. If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, this interrupt status bit is cleared to logic 0 on writing a logic 1 to this register bit. Otherwise, this interrupt status bit is cleared on read

NO_DJ0[1]I	IAPS1[3]
NO_DJ0[2]I	IAPS1[2]
NO_DJ0[3]I	IAPS1[1]
NO_DJ0[4]I	IAPS1[0]
NO_DJ0[5]I	IAPS2[3]
NO_DJ0[6]I	IAPS2[2]
NO_DJ0[7]I	IAPS2[1]
NO_DJ0[8]I	IAPS2[0]
NO_DJ0[9]I	IAPS3[3]
NO_DJ0[10]I	IAPS3[2]
NO_DJ0[11]I	IAPS3[1]
NO_DJ0[12]I	IAPS3[0]
NO_DJ0[13]I	IAPS4[3]

Downloaded by Copyright Union of Partners on Wednesday, 07 February, 2007 06:39:32 PM

NO_DJ0[14]I	IAPS4[2]
NO_DJ0[15]I	IAPS4[1]
NO_DJ0[16]I	IAPS4[0]

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0017H: S/UNI 9953 Input APS Frame Alignment Interrupt Status 2

Bit	Type	Function	Default
Bit 15	R	BAD_DJ016I	X
Bit 14	R	BAD_DJ015I	X
Bit 13	R	BAD_DJ014I	X
Bit 12	R	BAD_DJ013I	X
Bit 11	R	BAD_DJ012I	X
Bit 10	R	BAD_DJ011I	X
Bit 9	R	BAD_DJ010I	X
Bit 8	R	BAD_DJ09I	X
Bit 7	R	BAD_DJ08I	X
Bit 6	R	BAD_DJ07I	X
Bit 5	R	BAD_DJ06I	X
Bit 4	R	BAD_DJ05I	X
Bit 3	R	BAD_DJ04I	X
Bit 2	R	BAD_DJ03I	X
Bit 1	R	BAD_DJ02I	X
Bit 0	R	BAD_DJ01I	X

BAD_DJ0[N]I

The Bad Detected J0 Error Interrupt status (BAD_DJ0[N]I) bit is an event indicator for the IAPS[x][y] input data stream. BAD_DJ0[N]I is set to logic one to indicate that bad input J0 was detected outside the expected position as programmed via the AIJ0DLY[13:0] register bits. This interrupt status can activate the INTB output if the corresponding interrupt enable bit, BAD_DJ0E, is set to logic one. If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, this interrupt status bit is cleared to logic 0 on writing a logic 1 to this register bit. Otherwise, this interrupt status bit is cleared on read.

BAD_DJ0[1]I	IAPS1[3]
BAD_DJ0[2]I	IAPS1[2]
BAD_DJ0[3]I	IAPS1[1]
BAD_DJ0[4]I	IAPS1[0]
BAD_DJ0[5]I	IAPS2[3]
BAD_DJ0[6]I	IAPS2[2]
BAD_DJ0[7]I	IAPS2[1]
BAD_DJ0[8]I	IAPS2[0]
BAD_DJ0[9]I	IAPS3[3]
BAD_DJ0[10]I	IAPS3[2]
BAD_DJ0[11]I	IAPS3[1]
BAD_DJ0[12]I	IAPS3[0]
BAD_DJ0[13]I	IAPS4[3]

Downloaded by Copyright Holder of Partial Copy on Wednesday, 07 February, 2007 06:59:32 PM

BAD_DJ0[14]I	IAPS4[2]
BAD_DJ0[15]I	IAPS4[1]
BAD_DJ0[16]I	IAPS4[0]

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0018H: S/UNI 9953 MDIO Command

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R/W	RDINC	0
Bit 3	R/W	RSTAT	0
Bit 2	R/W	LCTLD	0
Bit 1	R/W	LCTLA	0
Bit 0	R/W	SPRE	0

This register allows MDIO command to be programmed and initiated via the microprocessor port of the S/UNI 9953.

SPRE

This bit controls the preamble suppression in the MDIO output stream. When SPRE is set to logic 0, a sequence of 32 contiguous logic 1 bits is provided on the MDIO output to establish synchronization. When SPRE is set to logic 1, the 32-bit preamble is suppressed.

LCTLA

A logic 0 to 1 transition on this bit will result in a management frame being sent via the MDIO pin with payload containing address (CTLAD[15:0]) of the external MII PHY register to be accessed in the subsequent operation. A logic 0 to 1 transition is achieved by first setting the bit to logic 0 followed by setting it to logic 1. The logic 0 to 1 transition is ignored if MDIO_BUSY is at logic 1.

LCTLD

A logic 0 to 1 transition on this bit will result in a management frame being sent via the MDIO pin with payload containing control data (CTLAD[15:0]) to be written to the external MII PHY register whose address was provided in the previous address frame. A logic 0 to 1 transition is achieved by first setting the bit to logic 0 followed by setting it to logic 1. The logic 0 to 1 transition is ignored if MDIO_BUSY is at logic 1.

Downloaded by Content Partner Partmine Inc on Wednesday, 07 February, 2007 06:59:32 PM

RSTAT

A logic 0 to 1 transition on this bit will result in a read operation management frame being sent via the MDIO pin. The status from the external MII PHY register whose address was specified in the previous address frame will be read via the MDIO pin and placed in the PRSD[15:0] bits. A logic 0 to 1 transition is achieved by first setting the bit to logic 0 followed by setting it to logic 1. The logic 0 to 1 transition is ignored if MDIO_BUSY is at logic 1.

RDINC

A logic 0 to 1 transition on this bit will result in a post-read-increment-address operation management frame being sent via the MDIO pin. The status from the external MII PHY register whose address was specified in the previous address frame will be read via the MDIO pin and placed in the PRSD[15:0] bits. Upon completion of the read operation, the slave device will increment the address register by one. A logic 0 to 1 transition is achieved by first setting the bit to logic 0 followed by setting it to logic 1. The logic 0 to 1 transition is ignored if MDIO_BUSY is at logic 1.

Downloaded by Content Team of Partminer Inc on Wednesday, 01 February 2007 06:03:32 AM

Register 0019H: S/UNI 9953 MMD PHY Address

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	R/W	DEVADR[4]	0
Bit 11	R/W	DEVADR[3]	0
Bit 10	R/W	DEVADR[2]	0
Bit 9	R/W	DEVADR[1]	0
Bit 8	R/W	DEVADR[0]	0
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R/W	PRTADR[4]	0
Bit 3	R/W	PRTADR[3]	0
Bit 2	R/W	PRTADR[2]	0
Bit 1	R/W	PRTADR[1]	0
Bit 0	R/W	PRTADR[0]	0

This register allows the MMD PHY Device/Port Addresses to be programmed via the microprocessor port of the S/UNI 9953.

PRTAD[4:0]

This is a 5-bit port address allowing 32 unique port addresses per MDIO. The first port address bit to be transmitted is the MSB of the address.

DEVADR[4:0

This is a 5-bit device address allowing 32 unique devices per port. The first device address bit to be transmitted is the MSB of the address.

Downloaded by Content Team of Chartmine Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 001AH: S/UNI 9953 MMD Control Address Data

Bit	Type	Function	Default
Bit 15	R/W	CTLAD[15]	0
Bit 14	R/W	CTLAD[14]	0
Bit 13	R/W	CTLAD[13]	0
Bit 12	R/W	CTLAD[12]	0
Bit 11	R/W	CTLAD[11]	0
Bit 10	R/W	CTLAD[10]	0
Bit 9	R/W	CTLAD[9]	0
Bit 8	R/W	CTLAD[8]	0
Bit 7	R/W	CTLAD[7]	0
Bit 6	R/W	CTLAD[6]	0
Bit 5	R/W	CTLAD[5]	0
Bit 4	R/W	CTLAD[4]	0
Bit 3	R/W	CTLAD[3]	0
Bit 2	R/W	CTLAD[2]	0
Bit 1	R/W	CTLAD[1]	0
Bit 0	R/W	CTLAD[0]	0

CTLAD[15:0]

Control Address/Data input bus. 16-bit register address indexing external PHY register table during an address command. 16-bit write data for management writes during a write command.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 001BH: S/UNI 9953 MDIO Read Status Data

Bit	Type	Function	Default
Bit 15	R	PRSD [15]	X
Bit 14	R	PRSD [14]	X
Bit 13	R	PRSD [13]	X
Bit 12	R	PRSD [12]	X
Bit 11	R	PRSD [11]	X
Bit 10	R	PRSD [10]	X
Bit 9	R	PRSD [9]	X
Bit 8	R	PRSD [8]	X
Bit 7	R	PRSD [7]	X
Bit 6	R	PRSD [6]	X
Bit 5	R	PRSD [5]	X
Bit 4	R	PRSD [4]	X
Bit 3	R	PRSD [3]	X
Bit 2	R	PRSD [2]	X
Bit 1	R	PRSD [1]	X
Bit 0	R	PRSD [0]	X

PRSD [15:0]

Read Status Data from external MII PHY device. The 16-bit result from the read operation of status register whose address is specified in the previous address frame. The read status data is only valid when MDIO_BUSY is at logic 0.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:59:32 PM

Register 001CH: S/UNI 9953 PCS/LAN/MDIO Interrupt Enable and Control

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	R/W	PCS_LCDE	0
Bit 13	—	Unused	X
Bit 12	R/W	PRBS23_MISE	0
Bit 11	R/W	LERR_ENA	0
Bit 10	R/W	LSYNC_ERRE	0
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	LPHASE_INIT	0
Bit 6	—	Unused	X
Bit 5	R/W	LPH_ERR_RE	0
Bit 4	R/W	LPH_ERR_FE	0
Bit 3	—	Unused	X
Bit 2	R/W	MDIO_BUSYE	0
Bit 1	R/W	MDIO_ST[1]	0
Bit 0	R/W	MDIO_ST[0]	0

This register provides interrupt enable and control associated with receive PCS (R64B66B) LCD generation, 10GbE LAN PHY input SYNC_ERR and PHASE_ERR assertion and MDIO command execution. No additional global interrupt control is required to condition the interrupt enable bits in this register. The device interrupt output signal, INTB, will be asserted when an interrupt status and the corresponding enable bits are both set to logic 1.

MDIO_ST[1:0]

The MDIO Start of frame (MDIO_ST[1:0]) bits allow the corresponding field in the MDIO Management frame to be configured. For 10 Gigabit Ethernet PHY operation, MDIO_ST[1:0] should left in the default state of b'00.

MDIO_BUSYE

The MDIO BUSY Interrupt Enable (MDIO_BUSYE) bit controls the assertion of the interrupt (INTB) output upon detection of an MDIO_BUSYI interrupt event. If MDIO_BUSYE is set to logic one, the MDIO_BUSYI pending interrupt will assert the interrupt (INTB) output. When MDIO_BUSYE is logic zero, the MDIO_BUSYI pending interrupt will not assert the interrupt (INTB).

Downloaded by Courtesy of Pericom Inc. on Thursday, 01 February, 2007 06:59:32 PM

LPH_ERR_FE

The 10GbE LAN PHY phase error falling edge interrupt enable (LPH_ERR_FE) bit enables or disables PHASE_ERR1 input as the source for a falling edge interrupt. When LPH_ERR_FE is set to logic one, a falling edge on the PHASE_ERR1 input will cause an interrupt (INTB). When LPH_ERR_FE is set to logic 0, a falling edge on the PHASE_ERR1 input can not cause an interrupt (INTB).

LPH_ERR_RE

The 10GbE LAN PHY phase error rising edge interrupt enable (LPH_ERR_RE) bit enables or disables PHASE_ERR1 input as the source for a rising edge interrupt. When LPH_ERR_RE is set to logic one, a rising edge on the PHASE_ERR1 input will cause an interrupt (INTB). When LPH_ERR_RE is set to logic 0, a rising edge on the PHASE_ERR1 input cannot cause an interrupt (INTB).

LPHASE_INIT

The 10GbE LAN PHY Phase Initialization (LPHASE_INIT) bit controls the logic level of the PHASE_INIT1 outputs when S/UNI 9953 is configured to support 10GbE LAN PHY operation. If set to logic 0, the PHASE_INIT1 output will be set low. If set to logic 1, the PHASE_INIT1 output will be set high.

LSYNC_ERRE

The 10GbE LAN PHY Synchronization Error Interrupt Enable (LSYNC_ERRE) bit controls the assertion of the interrupt (INTB) output upon detection of an LSYNC_ERRI interrupt event. If LSYNC_ERRE is set to logic one, the LSYNC_ERRI pending interrupt will assert the interrupt (INTB) output. When LSYNC_ERRE is logic zero, the LSYNC_ERRI pending interrupt will not assert the interrupt (INTB).

LERR_ENA

The 10GbE LAN PHY error enable (LERR_ENA) bit allows the SYNC_ERR1 input to squelch the receive 10 Gigabit data stream. When LERR_ENA is set to logic 1, a high on SYNC_ERR1 input will force the receive data stream to all zeros before it is provided to the R64B66B block. When LERR_ENA is set to logic 0, the receive data stream is provided to the R64B66B block without modification regardless of SYNC_ERR1 input.

PRBS23_MISE

The PRBS-23 Pattern Mismatch Interrupt Enable (PRBS23_MISE) bit controls the assertion of the interrupt (INTB) output upon detection of a PRBS-23 interrupt event. If PRBS23_MISE is set to logic one, the PRBS23_MISI pending interrupt will assert the interrupt (INTB) output. When PRBS23_MISE is logic zero, the PRBS23_MISI pending interrupt will not assert the interrupt (INTB).

Downloaded by Content Group of Partner1 Inc on Wednesday, 07 February 2007 06:39:22 PM

PCS_LCDE

The PCS Loss of Cell Delineation Interrupt Enable (PCS_LCDE) bit controls the assertion of the interrupt (INTB) output upon detection of a PCS_LCDI interrupt event. If PCS_LCDE is set to logic one, the PCS_LCDI pending interrupt will assert the interrupt (INTB) output. When PCS_LCDE is logic zero, the PCS_LCDI pending interrupt will not assert the interrupt (INTB).

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:58:02 PM

Register 001DH: S/UNI 9953 PCS/LAN/MDIO Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	R	PCS_LCDI	X
Bit 13	—	Unused	X
Bit 12	R	PRBS23_MISI	X
Bit 11	—	Unused	X
Bit 10	R	LSYNC_ERRI	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R	LPH_ERR_RI	X
Bit 4	R	LPH_ERR_FI	X
Bit 3	—	Unused	X
Bit 2	R	MDIO_BUSYI	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

This register provides the interrupt status associated with receive PCS (R64B66B) LCD generation, 10GbE LAN PHY input SYNC_ERR and PHASE_ERR assertion and MDIO command execution.

MDIO_BUSYI

The MDIO BUSY interrupt status (MDIO_BUSYI) transitions to logic 1 when there is a change in the MDIO_BUSY status. This interrupt status can activate the INTB output if the corresponding interrupt enable bit, MDIO_BUSYE, is set to logic one. If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, this interrupt status bit is cleared to logic 0 on writing a logic 1 to this register bit. Otherwise, this interrupt status bit is cleared on read.

Downloaded by Content Team of IHS Inc on Wednesday, 07 February, 2007 06:09:32 PM

LPH_ERR_RI

The 10GbE LAN PHY phase error rising edge interrupt status (LPH_ERR_RI) bit is set to logic one if a rising edge has been detected on the PHASE_ERR1 input. This interrupt status can activate the INTB output if the corresponding interrupt enable bit, LPH_ERR_RE, is set to logic one. If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, this interrupt status bit is cleared to logic 0 on writing a logic 1 to this register bit. Otherwise, this interrupt status bit is cleared on read.

LPH_ERR_FI

The 10GbE LAN PHY phase error falling edge interrupt status (LPH_ERR_FI) bit is set to logic one if a falling edge has been detected on the PHASE_ERR1 input. This interrupt status can activate the INTB output if the corresponding interrupt enable bit, LPH_ERR_FE, is set to logic one. If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, this interrupt status bit is cleared to logic 0 on writing a logic 1 to this register bit. Otherwise, this interrupt status bit is cleared on read.

LSYNC_ERRI

The 10GbE LAN PHY Synchronization Error Interrupt status (LSYNC_ERRI) bit is an event indicator. LSYNC_ERRI is set to logic one to indicate a change in the status of SYNC_ERR1 input. This interrupt status can activate the INTB output if the corresponding interrupt enable bit, LSYNC_ERRE, is set to logic one. If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, this interrupt status bit is cleared to logic 0 on writing a logic 1 to this register bit. Otherwise, this interrupt status bit is cleared on read.

PCS_LCDI

The PCS Loss of Cell Delineation Interrupt status (PCS_LCDI) bit is an event indicator. PCS_LCDI is set to logic one to indicate a change in the PCS_LCD status. This interrupt status can activate the INTB output if the corresponding interrupt enable bit, PCS_LCDE, is set to logic one. If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, this interrupt status bit is cleared to logic 0 on writing a logic 1 to this register bit. Otherwise, this interrupt status bit is cleared on read.

Downloaded by Content Tools (Partminer) - Wednesday, January, 2007 10:30:32 AM

PRBS23_MISI

The PRBS-23 Pattern Mismatch Interrupt status (PRBS23_MISI) bit is an event indicator. PRBS23_MISI is set to logic one to indicate a change in the PRBS23_MIS status. This interrupt status can activate the INTB output if the corresponding interrupt enable bit, PRBS23_MISE, is set to logic one. If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, this interrupt status bit is cleared to logic 0 on writing a logic 1 to this register bit. Otherwise, this interrupt status bit is cleared on read.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 08:57:02 AM

Register 001EH: S/UNI 9953 PCS/LAN/MDIO Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	R	PCS_LCD	X
Bit 13	—	Unused	X
Bit 12	R	PRBS23_MIS	X
Bit 11	—	Unused	X
Bit 10	R	LSYNC_ERR	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	LPH_ERR	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R	MDIO_BUSY	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

This register provides the status associated with receive PCS (R64B66B) LCD generation, 10GbE LAN PHY input SYNC_ERR and PHASE_ERR assertion and MDIO command execution.

MDIO_BUSY

The active high MDIO busy (MDIO_BUSY) bit reports if a previously initiated MDIO command has been completed. BUSY is set to logic 1 upon setting a logic 0 to 1 transition on the LCTLD, LCTLA, RSTAT, or RDINC bit in the S/UNI 9953 MDIO Command Register. BUSY is set to logic 0, upon completion of the MDIO command.

Downloaded by Content Team of Parts Life Inc on Wednesday, 07 February, 2007 06:09:32 PM

LPH_ERR

The 10GbE LAN PHY phase error status (PH_ERR]) bit simply reflects the logic level of the PHASE_ERR1 input.

LSYNC_ERR

The 10GbE LAN PHY Synchronization Error status (LSYNC_ERR]) bit simply reflects the logic level of the SYNC_ERR1 input.

PCS_LCD

The PCS Loss of Cell Delineation status (PCS_LCD) bit contains the filtered Loss of code group Synchronization status from the receive PCS (R64B66B) block. If the Loss of code group Synchronization is asserted for the duration of 3 ms or greater then PCS Loss of Cell Delineation is declared and the corresponding RDI-P (or ERDI-P) is transmitted to the far-end if enabled. This feature is required only by 10 GbE WAN PHY operation.

PRBS23_MIS

The PRBS-23 Pattern Mismatch status (PRBS23_MIS) bit contains the PRBS-23 pattern mismatch status from the PRBS-23 monitor block.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 001FH: S/UNI 9953 Input APS and Loop-back Interrupt Enable

Bit	Type	Function	Default
Bit 15	R/W	NO_DJ0E	0
Bit 14	R/W	BAD_DJ0E	0
Bit 13	—	Unused	X
Bit 12	R/W	PL4_TIP_DIS	0
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	R/W	TX_FCOUNT_RST	0
Bit 7	R/W	LLB_FIFOSLIPE	0
Bit 6	R/W	DLB_FIFOSLIPE	0
Bit 5	—	Unused	X
Bit 4	R/W	APS_NOCLK	1
Bit 3	R/W	TCFP2488_RST	1
Bit 2	R/W	TXSYS192_RST	0
Bit 1	R/W	RCFP2488_RST	1
Bit 0	R/W	RXSYS192_RST	0

The S/UNI 9953 Input APS and Loop-back Interrupt Enable Register is reserved and provided for diagnostic purposes only. The register bits must be set to the default value indicated for normal operation of the S/UNI 9953.

RXSYS192_RST

The Receive System STS-192c/STM-64c payload processor Reset (RXSYS192_RST) bit allows the RCFP-9953, R64B66B and RXXG blocks in the S/UNI 9953 to be reset under software control. If the RXSYS192_RST bit is a logic one, the RCFP-9953, R64B66B and RXXG blocks are held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring these blocks out of reset. A hardware reset clears the RXSYS192_RST bit, thus negating the software reset.

RCFP2488_RST

The Receive Cell/Frame Processor for 2488 Mbit/s (RCFP2488) Reset (RCFP2488_RST) bit allows the four RCFP blocks in the S/UNI 9953 to be reset under software control. If the RCFP2488_RST bit is a logic one, the RCFP blocks are held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring these blocks out of reset. A hardware reset sets the RCFP2488_RST bit to logic 1, thus forcing the software reset by default.

Downloaded by Cores Ocean Electronics Inc on Wednesday, 07 February 2007 06:59:32 PM

TXSYS192_RST

The Transmit System STS-192c/STM-64c payload processor Reset (TXSYS192_RST) bit allows the TCFP-9953, T64B66B and TXXG blocks in the S/UNI 9953 to be reset under software control. If the TXSYS192_RST bit is a logic one, the TCFP-9953, T64B66B and TXXG blocks are held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring these blocks out of reset. A hardware reset clears the TXSYS192_RST bit, thus negating the software reset.

TCFP2488_RST

The Transmit Cell/Frame Processor for 2488 Mbit/s (RCFP2488) Reset (RCFP2488_RST) bit allows the four TCFP blocks in the S/UNI 9953 to be reset under software control. If the TCFP2488_RST bit is a logic one, the TCFP blocks are held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring these blocks out of reset. A hardware reset sets the TCFP2488_RST bit to logic 1, thus forcing the software reset by default.

APS_NOCLK

The APS No Clock (APS_NOCLK) bit controls the squelching of input clocks to the APS digital subsystem. If the APS_NOCLK bit is set to logic 1, the input clocks to the APS digital subsystem are forced to low. Registers in the CSTRI, T8TE and R8TD blocks in the subsystem remain accessible. If the APS_NOCLK bit is set to logic 0, the input clocks to the APS digital subsystem are not affected. The APS_NOCLK bit allows the power-down of the APS digital subsystem to conserve power when the APS port functions are not required.

DLB_FIFOSLIPE

This register bit is for PMC debug purposes only, and must be left in its default setting for proper operation of the S/UNI 9953.

LLB_FIFOSLIPE

This register bit is for PMC debug purposes only, and must be left in its default setting for proper operation of the S/UNI 9953.

TX_FCOUNT_RST

This register bit is for PMC debug purposes only, and must be left in its default setting for proper operation of the S/UNI 9953.

Downloaded by Content Team of Partminer Inc on Thursday, 07 June 2007 08:52:32 GMT

PL4_TIP_DIS

PL4 Subsystem TIP Disable. This bit should be set high when the PL4 sub-system is disabled to prevent the PL4 sub-system TIP bit from propogating to the main TIP bit in Register 0x0000. The PL4 sub-system would be disabled if the device is used as an APS protect mode, whereby the PL4 interface is not required. The PL4 sub-system is disabled by clearing the ENABLE bit in the PL4IO Configuration register 0x2305.

BAD_DJ0E

The Bad Detected J0 Error Interrupt Enable (BAD_DJ0E) bit controls the assertion of the interrupt (INTB) output upon detection of an BAD_DJ0[N]I interrupt event. If BAD_DJ0E is set to logic one, the BAD_DJ0[N]I pending interrupt will assert the interrupt (INTB) output. When BAD_DJ0E is logic zero, the BAD_DJ0[N]I pending interrupt will not assert the interrupt (INTB).

NO_DJ0E

The No Detected J0 Error Interrupt Enable (NO_DJ0E) bit controls the assertion of the interrupt (INTB) output upon detection of an NO_DJ0[N]I interrupt event. If NO_DJ0E is set to logic one, the NO_DJ0[N]I pending interrupt will assert the interrupt (INTB) output. When NO_DJ0E is logic zero, the NO_DJ0[N]I pending interrupt will not assert the interrupt (INTB).

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 06:58:32 PM

Register 0n20H: S/UNI 9953 STM-4 Slice Interrupt Status

Bit	Type	Function	Default
Bit 15	R/W	INTE	0
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	T8TEI	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R	RLMPGMI	X
Bit 4	R	IAMPGMI	X
Bit 3	R	R8TDI	X
Bit 2	R	SVCAI	X
Bit 1	R	RHPPI	X
Bit 0	R	RRMPI	X

This register allows the source of an active interrupt to be identified down to the block level for the corresponding SONET/SDH STM-4 slice. There are 16 such slices in the S/UNI 9953 required to process an STS-192c/STM-64c or four STS-48c/STM-16c data streams (see Operation section for details). Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source. These register bits should normally not be used when the SONET/SDH blocks in the STM-4 slice are configured as slaves unless indicated otherwise.

Note that the address of this register is 0x0n20, where n = 0 to F, and n represents the STM-4 slice number. See the section on the Microprocessor Interface for details.

RRMPI

The RRMP interrupt event indication (RRMPI) transitions to logic 1 when a hardware interrupt event is sourced from RRMP block. This bit is cleared to logic 0 when the interrupt in the RRMP block is cleared.

RHPPI

The RHPP interrupt event indication (RHPPI) transitions to logic 1 when a hardware interrupt event is sourced from RHPP block. This bit is cleared to logic 0 when the interrupt in the RHPP block is cleared.

Downloaded by Content Portal of Partnumber.com on Wednesday, 07 February, 2007 06:09:32 PM

SVCAI

The SVCA interrupt event indication (SVCAI) transitions to logic 1 when a hardware interrupt event is sourced from SVCA block. This bit is cleared to logic 0 when the interrupt in the SVCA block is cleared.

R8TDI

The R8TD interrupt event indication (R8TDI) transitions to logic 1 when a hardware interrupt event is sourced from R8TD block. This bit is cleared to logic 0 when the interrupt in the R8TD block is cleared.

IAMPGMI

The IAMPGM interrupt event indication (IAMPGMI) transitions to logic 1 when a hardware interrupt event is sourced from Input APS MPGM (IAMPGM) block. This bit is cleared to logic 0 when the interrupt in the IAMPGMI block is cleared.

RLMPGMI

The RLMPGM interrupt event indication (RLMPGMI) transitions to logic 1 when a hardware interrupt event is sourced from Receive Line MPGM (RLMPGM) block. This bit is cleared to logic 0 when the interrupt in the RLMPGMI block is cleared.

T8TEI

The T8TE interrupt event indication (T8TEI) transitions to logic 1 when a hardware interrupt event is sourced from T8TE block. This bit is cleared to logic 0 when the interrupt in the T8TE block is cleared.

INTE

The interrupt enable (INTE) bit controls the assertion of the interrupt (INTB) output. When a logic 1 is written to INTE, the pending interrupt(s) listed in this register will assert the interrupt (INTB) output. When a logic 0 is written to INTE, the pending interrupt(s) will not assert the interrupt (INTB) output.

Downloaded by Content Team on Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0k21H: S/UNI 9953 STM-64/STM-16 Stream Interrupt Status

Bit	Type	Function	Default
Bit 15	R/W	INTE	0
Bit 14	—	Unused	X
Bit 13	R	Reserved	X
Bit 12	R	TCFPI	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R	Reserved	X
Bit 4	R	RCFPI	X
Bit 3	R	SARCI	X
Bit 2	R	PATHRTTPI	X
Bit 1	R	SECTIONRTTPI	X
Bit 0	R	SBERI	X

This register allows the source of an active interrupt to be identified down to the block level for the corresponding SONET/SDH STM-16c data stream processing group. There are four STM-16c processing groups in the S/UNI 9953 required to process an STS-192c/STM-64c or four STS-48c/STM-16c data streams (see Operation section for details). Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source. These register bits should normally not be used when the SONET/SDH blocks in the STM-16c processing group are configured as slaves unless indicated otherwise.

Note that the address of this register is 0x0k21, where k = 0 to 3, and k represents the STM-16 slice number. See the section on the Microprocessor Interface for details.

SBERI

The SBER interrupt event indication (SBERI) transitions to logic 1 when a hardware interrupt event is sourced from SBER block. This bit is cleared to logic 0 when the interrupt in the SBER block is cleared.

SECTIONRTTPI

The SECTIONRTTP interrupt event indication (SECTIONRTTPI) transitions to logic 1 when a hardware interrupt event is sourced from Section RTTP block. This bit is cleared to logic 0 when the interrupt in the Section RTTP block is cleared.

Downloaded by Contents Team of Partsinel.com Wednesday, 07 February, 2007 06:09:32 PM

PATHRTTPI

The PATHRTTP interrupt event indication (PATHRTTPI) transitions to logic 1 when a hardware interrupt event is sourced from Path RTTP block. This bit is cleared to logic 0 when the interrupt in the Path RTTP block is cleared.

SARCI

The SARC interrupt event indication (SARCI) transitions to logic 1 when a hardware interrupt event is sourced from SARC block. This bit is cleared to logic 0 when the interrupt in the SARC block is cleared.

RCFPI

The RCFP interrupt event indication (RCFPI) transitions to logic 1 when a hardware interrupt event is sourced from RCFP block. This bit is cleared to logic 0 when the interrupt in the RCFP block is cleared.

TCFPI

The TCFP interrupt event indication (TCFPI) transitions to logic 1 when a hardware interrupt event is sourced from TCFP block. This bit is cleared to logic 0 when the interrupt in the TCFP block is cleared.

INTE

The interrupt enable (INTE) bit controls the assertion of the interrupt (INTB) output. When a logic 1 is written to INTE, the pending interrupt(s) listed in this register will assert the interrupt (INTB) output. When a logic 0 is written to INTE, the pending interrupt(s) will not assert the interrupt (INTB) output.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0022H: S/UNI 9953 Overhead and DCC Configuration1

Bit	Type	Function	Default
Bit 15	R/W	RPOH2_SEL[1]	0
Bit 14	R/W	RPOH2_SEL[0]	0
Bit 13	R/W	RTOH2_SEL[1]	0
Bit 12	R/W	RTOH2_SEL[0]	0
Bit 11	R/W	TPOH2_SEL[1]	0
Bit 10	R/W	TPOH2_SEL[0]	0
Bit 9	R/W	TTOH2_SEL[1]	0
Bit 8	R/W	TTOH2_SEL[0]	0
Bit 7	R/W	RPOH1_SEL[1]	0
Bit 6	R/W	RPOH1_SEL[0]	0
Bit 5	R/W	RTOH1_SEL[1]	0
Bit 4	R/W	RTOH1_SEL[0]	0
Bit 3	R/W	TPOH1_SEL[1]	0
Bit 2	R/W	TPOH1_SEL[0]	0
Bit 1	R/W	TTOH1_SEL[1]	0
Bit 0	R/W	TTOH1_SEL[0]	0

This register and the following register is used to control how the Overhead Insert and Extract ports are to operate. Full flexibility of both receive/transmit and transport/path ports are provided. Either of the ports may be used to insert/extract either full overhead bytes, section DCC (D1-D3 bytes) only, line DCC (D4-D12 bytes) only, or null operation. The latter is useful for power dissipation control if the interface is not being used.

A description of the mapping is given in the following register.

Downloaded by Content Team of Partmine Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0023H: S/UNI 9953 Overhead and DCC Configuration2

Bit	Type	Function	Default
Bit 15	R/W	RPOH4_SEL[1]	0
Bit 14	R/W	RPOH4_SEL[0]	0
Bit 13	R/W	RTOH4_SEL[1]	0
Bit 12	R/W	RTOH4_SEL[0]	0
Bit 11	R/W	TPOH4_SEL[1]	0
Bit 10	R/W	TPOH4_SEL[0]	0
Bit 9	R/W	TTOH4_SEL[1]	0
Bit 8	R/W	TTOH4_SEL[0]	0
Bit 7	R/W	RPOH3_SEL[1]	0
Bit 6	R/W	RPOH3_SEL[0]	0
Bit 5	R/W	RTOH3_SEL[1]	0
Bit 4	R/W	RTOH3_SEL[0]	0
Bit 3	R/W	TPOH3_SEL[1]	0
Bit 2	R/W	TPOH3_SEL[0]	0
Bit 1	R/W	TTOH3_SEL[1]	0
Bit 0	R/W	TTOH3_SEL[0]	0

TTOH*k*_SEL[1:0]

The TTOH*k*_SEL controls the mapping of the TTOH*k* ports for slice number *k*. The TTOH*k* ports may be mapped to either the line or section DCC bytes based on the configuration of TRMP #*k * 4* (master for slice *k* in 4xOC48 mode).

If the interface is not required, it is recommended to set the select bits to “01” to reduce the power.

The possible values for TTOH*k*_SEL are:

TTOH*k*_SEL[1:0]	TTOH*k* Mapping
00	TTOHk
01	Power Down
10	TLDk (line DCC)
11	TSLDk (section or line DCC) Selected by the relevant TRMP #(*k**4) control bit TSLDSEL, where *k* = 1..4. This bit is available in registers 1n60H

TPOH*k*_SEL[1:0]

The TPOH*k*_SEL controls the mapping of the TPOH*k* ports for slice number *k*. The TPOH*k* ports may be mapped to either the line or section DCC bytes based on the configuration of TRMP #*k*4* (master for slice *k* in 4xOC48 mode).

Downloaded by Content Team of Pacmine Inc on Wednesday, 07 February, 2007 06:59:32 PM

If the interface is not required, it is recommended to set the select bits to "01" to reduce the power.

The possible values for TPOH*k*_SEL are:

TPOH*k*_SEL[1:0]	TPOH*k* Mapping
00	TPOHk
01	Power Down
10	TLDk (line DCC)
11	TSLDk (section or line DCC) Selected by the relevant TRMP #(*k**4) control bit TSLDSEL, where *k* = 1..4. This bit is available in registers 1n60H

Note that if TTOH*k*_SEL[1:0] and TPOH*k*_SEL[1:0] are set equal for the same slice (*k* is the same), TTOH data port is used to insert section or line DCC and TPOH data port is ignored.

RTOH*k*_SEL[1:0]

The RTOH*k*_SEL controls the mapping of the RTOH*k* port to overhead bytes. The RTOH*k* ports may be mapped to the line or section DCC based on the configuration of the RRMP #*k**4 (master for slice *k* in 4xOC48 mode) and the RTOH*k*_SEL value.

If the interface is not required, it is recommended to set the select bits to "01" to reduce the power.

The possible values for RTOH*k*_SEL are:

RTOH*k*_SEL [1:0]	RTOH*k* Mapping
00	RTOHk
01	Power Down
10	RLDk (line DCC)
11	RSLDk (section or line DCC) Selected by the relevant RRMP #(*k**4) control bit RSLDSEL, where *k* = 1..4. This bit is available in registers 0n60H

RPOH*k*_SEL[1:0]

The RPOH*k*_SEL controls the mapping of the RPOH*k* port to overhead bytes. The RPOH*k* ports may be mapped to the line or section DCC based on the configuration of the RRMP #*k**4 (master for slice *k* in 4xOC48 mode) and the RPOH*k*_SEL value.

If the interface is not required, it is recommended to set the select bits to "01" to reduce the power.

The possible values for RPOH*k*_SEL are:

Downloaded by Conexant Team of Part Miner on Wednesday, 07 February 2007 06:59:32 PM

RPOH*k*_SEL [1:0]	RPOH*k* Mapping
00	RPOHk
01	Power Down
10	RLDk (line DCC)
11	RSLDk (section or line DCC) Selected by the relevant RRMP #(*k**4) control bit RSLDSEL, where *k* = 1..4. This bit is available in registers 0n60H

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 10:59:32 PM

Register 0024H: S/UNI 9953 Power Down Configuration

Bit	Type	Function	Default
Bit 15	R/W	APS_PD	0
Bit 14	R/W	STSI_PD	0
Bit 13	R/W	TTTP_PATH_PD	0
Bit 12	R/W	RTTP_PATH_PD	0
Bit 11	R/W	TTTP_SECTION_PD	0
Bit 10	R/W	RTTP_SECTION_PD	0
Bit 9	R/W	SARC_PD	0
Bit 8	R/W	MSTAT_PD	0
Bit 7	R/W	T64B66B_PD	0
Bit 6	R/W	R64B66B_PD	0
Bit 5	R/W	TXXG_PD	0
Bit 4	R/W	RXXG_PD	0
Bit 3	R/W	TCFP9953_PD	0
Bit 2	R/W	RCFP9953_PD	0
Bit 1	R/W	TCFP_PD	0
Bit 0	R/W	RCFP_PD	0

RCFP_PD

When the RCFP_PD is set to 1, the 4 RCFP blocks are powered down to reduce power consumption. This bit can be set for any mode of operation except for OC-48 and channelized OC-192 modes.

TCFP_PD

When the TCFP_PD is set to 1, the 4 TCFP blocks are powered down to reduce power consumption. This bit can be set for any mode of operation except for OC-48 and channelized OC-192 modes.

RCFP9953_PD

When the RCFP9953_PD is set to 1, the RCFP9953 block is powered down to reduce power consumption. This bit can be set for any mode of operation except for OC-192C ATM, GFP and POS modes.

TCFP9953_PD

When the TCFP9953_PD is set to 1, the TCFP9953 block is powered down to reduce power consumption. This bit can be set for any mode of operation except for OC-192C ATM, GFP and POS modes.

Downloaded by Content Team of Datasheet Inc on Wednesday, 07 February, 2007 06:59:32 PM

RXXG_PD

When the RXXG_PD is set to 1, the RXXG block is powered down to reduce power consumption. This bit can be set for any mode of operation except for 10G WAN and LAN modes.

TXXG_PD

When the TXXG_PD is set to 1, the TXXG block is powered down to reduce power consumption. This bit can be set for any mode of operation except for 10G WAN and LAN modes.

R64B66B_PD

When the R64B66B_PD is set to 1, the R64B66B block is powered down to reduce power consumption. This bit can be set for any mode of operation except for 10G WAN and LAN modes.

T64B66B_PD

When the T64B66B_PD is set to 1, the T64B66B block is powered down to reduce power consumption. This bit can be set for any mode of operation except for 10G WAN and LAN modes.

MSTAT_PD

When the MSTAT_PD is set to 1, the MSTAT block is powered down to reduce power consumption. This bit can be set for any mode of operation, even in 10G WAN and LAN modes if the management statistics are not required.

SARC_PD

When the SARC _PD is set to 1, the SARC blocks are powered down to reduce power consumption. This bit can be set for any mode of operation, even in 10G WAN and LAN modes if the SONET alarms are not required. This bit would typically be set in 10GE LAN mode only.

RTTP_SECTION_PD

When the RTTP_SECTION_PD is set to 1, the 4 RTTP_SECTION blocks are powered down to reduce power consumption. This bit can be set for any mode of operation if the section trace extraction is not required.

Downloaded by Content Team - Partminer, Inc on Wednesday, 07 February, 2007 06:59:32 PM

TTTP_SECTION_PD

When the TTTP_SECTION_PD is set to 1, the 4 TTTP_SECTION blocks are powered down to reduce power consumption. This bit can be set for any mode of operation if the section trace insertion is not required.

RTTP_PATH_PD

When the RTTP_PATH_PD is set to 1, the 4 RTTP_PATH blocks are powered down to reduce power consumption. This bit can be set for any mode of operation if the path trace extraction is not required.

TTTP_PATH_PD

When the TTTP_PATH_PD is set to 1, the 4 TTTP_PATH blocks are powered down to reduce power consumption. This bit can be set for any mode of operation if the path trace insertion is not required.

STSI_PD

When the STSI_PD is set to 1, logic used in the System to SONET interface will be powered down to reduce power consumption. This bit can be set for 10GE LAN mode only.

APS_PD

The APS Power Down (APS_PD) bit controls the squelching of input clocks to the APS digital subsystem. If the APS_PD bit is set to logic 1, the input clocks to the APS digital subsystem are forced to low. Registers in the CSTRI, T8TE and R8TD blocks in the subsystem remain accessible. If the APS_PD bit is set to logic 0, the input clocks to the APS digital subsystem are not affected. The APS_PD bit allows the power-down of the APS digital subsystem to conserve power when the APS port functions are not required.

This bit is logically OR'ed with the APS_NOCLK bit in register 0x001F.

Downloaded by Content Team of Parvati ... on Wednesday, 07 February, 2007 06:59:32 PM

Register 0025H: S/UNI 9953 Overhead Port Control

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	~~Reserved~~ RCFP9953_PAIS_CNT	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	—	Unused	X
Bit 8	R/W	ROHI_OOF_RST_EN	0
Bit 7	R/W	ROHI_RST[4]	0
Bit 6	R/W	ROHI_RST[3]	0
Bit 5	R/W	ROHI_RST[2]	0
Bit 4	R/W	ROHI_RST[1]	0
Bit 3	R/W	Reserved	1
Bit 2	R/W	Reserved	1
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

ROHI_RST[4:1]

Receive Overhead Interface Reset. This register allows the individual receive overhead ports to be reset independently. This could be done based on the detection of the RRMP slices losing frame lock. When ROHI_RST[k] is set high, the logic controlling the RTOH[k] and RPOH[k] ports will be held in a reset state. When set low, the logic will be removed from reset.

ROHI_OOF_RST_EN

Receive Overhead Interface Out of Frame Reset Enable. This register allows the receive overhead ports to be reset automatically, based on the status of the RRMP internal Out of Frame (OOF) indications. When ROHI_OOF_RST_EN is set high, the logic will be reset based on the RRMP status. When set low, the logic will be free running, unless forced reset by the ROHI_RST[4:1] bits.

RCFP9953_PAIS_CNT

This bit is applicable for OC-192 POS/ATM modes. When set high, the RCFP-9953 will count received bytes correctly during PAIS condition. When low, the RCFP-9953 will incorrectly continue to count receive bytes during PAIS.

This bit must be set to logic 1 for correct counting operation.

Downloaded by Content Control Department on Wednesday, 07 February, 2007 06:59:32 PM

Register 0026H: S/UNI 9953 WIS PRBS-23 Pattern Mismatch Counter LSB

Bit	Type	Function	Default
Bit 15	R	PRBS_PAT_MIS[15]	X
Bit 14	R	PRBS_PAT_MIS[14]	X
Bit 13	R	PRBS_PAT_MIS[13]	X
Bit 12	R	PRBS_PAT_MIS[12]	X
Bit 11	R	PRBS_PAT_MIS[11]	X
Bit 10	R	PRBS_PAT_MIS[10]	X
Bit 9	R	PRBS_PAT_MIS[9]	X
Bit 8	R	PRBS_PAT_MIS[8]	X
Bit 7	R	PRBS_PAT_MIS[7]	X
Bit 6	R	PRBS_PAT_MIS[6]	X
Bit 5	R	PRBS_PAT_MIS[5]	X
Bit 4	R	PRBS_PAT_MIS[4]	X
Bit 3	R	PRBS_PAT_MIS[3]	X
Bit 2	R	PRBS_PAT_MIS[2]	X
Bit 1	R	PRBS_PAT_MIS[1]	X
Bit 0	R	PRBS_PAT_MIS[0]	X

PRBS_PAT_MIS[15:0]

PRBS-23 Pattern Mismatch Counter (LSB). This register counts the number of PRBS-23 pattern mismatches received by the PRBS-23 monitor. A mismatch is counted based on a 128-bit comparison.

The PRBS-23 generator is typically used 10GbE WAN mode, but can be used in normal OC-192 mode. The PRBS-23 monitor will still count PRBS-23 mismatches.

~~The register is held in a shadow register~~

Downloaded by Content Team of Parmiter, Inc. on Wednesday, 07 February, 2007 06:59:32 PM

Register 0027H: S/UNI 9953 WIS PRBS-23 Pattern Mismatch Counter MSB

Bit	Type	Function	Default
Bit 15	R	PRBS_PAT_MIS[31]	X
Bit 14	R	PRBS_PAT_MIS[30]	X
Bit 13	R	PRBS_PAT_MIS[29]	X
Bit 12	R	PRBS_PAT_MIS[28]	X
Bit 11	R	PRBS_PAT_MIS[27]	X
Bit 10	R	PRBS_PAT_MIS[26]	X
Bit 9	R	PRBS_PAT_MIS[25]	X
Bit 8	R	PRBS_PAT_MIS[24]	X
Bit 7	R	PRBS_PAT_MIS[23]	X
Bit 6	R	PRBS_PAT_MIS[22]	X
Bit 5	R	PRBS_PAT_MIS[21]	X
Bit 4	R	PRBS_PAT_MIS[20]	X
Bit 3	R	PRBS_PAT_MIS[19]	X
Bit 2	R	PRBS_PAT_MIS[18]	X
Bit 1	R	PRBS_PAT_MIS[17]	X
Bit 0	R	PRBS_PAT_MIS[16]	X

PRBS_PAT_MIS[31:16]

PRBS-23 Pattern Mismatch Counter (MSB). This register counts the number of WIS PRBS-23 pattern mismatches received by the PRBS-23 monitor, when used in 10GbE WAN mode. A mismatch is counted based on a 128-bit comparison.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:59:32 PM

12.2 SONET/SDH Receive Line Interface (SRLI)

Register 0032H: SRLI Diagnostic 1

Register 0035H: SRLI Diagnostic 2

Register 0038H: SRLI Diagnostic 3

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

These registers must be written to their default values for normal operation.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0039H: SRLI Synchronization Error Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	SYNC_ERR4I	X
Bit 2	R/W	SYNC_ERR3I	X
Bit 1	R/W	SYNC_ERR2I	X
Bit 0	R/W	SYNC_ERR1I	X

If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, these interrupt status bits are cleared on a write of logic one. Otherwise, these interrupt status bits are cleared on read.

SYNC_ERR1-4I

The Synchronization Error Interrupt status (SYNC_ERR[N]I) bit is an event indicator. SYNC_ERR[N]I is set to logic one to indicate a change in the status of SYNC_ERR[N]V. The interrupt bit is independent of the interrupt enable.

Downloaded by Content Team of Partner, Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 003AH: SRLI Synchronization Error Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R	SYNC_ERR4V	0
Bit 2	R	SYNC_ERR3V	0
Bit 1	R	SYNC_ERR2V	0
Bit 0	R	SYNC_ERR1V	0

SYNC_ERR1-4V

The Synchronization Error status (SYNC_ERR[N]V) bit reflects the current status of the SYNC_ERR[N] input. These bits can be used to monitor an external integrated optical module's clock and data recovery state. Four bits are provided to monitor four clock and data recovery units when the S/UNI 9953 is configured for quad OC-48 operation. Change of state can be determined by using the status bits in this register and the interrupt bits in the SRLI Synchronization Error Interrupt Status register.

Downloaded by Content Team of Partminer on Wednesday, 07 February, 2007 06:59:32 PM

Register 003BH: SRLI Synchronization Error Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	SYNC_ERR4E	0
Bit 2	R/W	SYNC_ERR3E	0
Bit 1	R/W	SYNC_ERR2E	0
Bit 0	R/W	SYNC_ERR1E	0

SYNC_ERR1-4E

The Synchronization Error Interrupt Enable (SYNC_ERR[N]E) bit controls the assertion of the interrupt (INTB) output upon detection of an SYNC_ERR[N]I interrupt event. If SYNC_ERR[N]E is set to logic one, the SYNC_ERR[N]I pending interrupt will assert the interrupt (INTB) output. When SYNC_ERR[N]E is logic zero, the SYNC_ERR[N]I pending interrupt will not assert the interrupt (INTB).

Downloaded by Content Team of Partminer on Wednesday, 07 February, 2007 06:59:32 PM

Register 003CH: SRLI Programmable Clock Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	PGMRCLKSEL4[1]	0
Bit 6	R/W	PGMRCLKSEL4[0]	0
Bit 5	R/W	PGMRCLKSEL3[1]	0
Bit 4	R/W	PGMRCLKSEL3[0]	0
Bit 3	R/W	PGMRCLKSEL2[1]	0
Bit 2	R/W	PGMRCLKSEL2[0]	0
Bit 1	R/W	PGMRCLKSEL1[1]	0
Bit 0	R/W	PGMRCLKSEL1[0]	0

The SRLI Programmable Clock Configuration Register is used to configure the frequencies of the PGMRCLK[4:1] output clocks.

PGMRCLKSEL1-4[1:0]

The receive programmable clock frequency bits enables and selects the frequency of the output clocks on PGMRCLK[4:1]. The output clocks are generated based on dividing down the corresponding input clock, RXCLK[4:1]+/-. When configured for OC-192 operation, output clocks PGMRCLK[4:2] should be disabled to reduce board noise.

PGMRCLKSEL[1:0]	Clock frequency
00	Disabled
01	8 kHz
10	19.44 MHz
11	77.76 MHz

Downloaded by Content Team of Parts Engine on Wednesday, 07 February, 2007 06:59:32 PM

Register 003DH: SRLI Synchronize Error Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	ERR_ENA4	0
Bit 2	R/W	ERR_ENA3	0
Bit 1	R/W	ERR_ENA2	0
Bit 0	R/W	ERR_ENA1	0

ERR_ENA1-4

The error enable register bits enable the SYNC_ERR1-4 inputs.

In OC-192 and 10GbE WAN modes, when ERR_ENA1 is logic 1, the SYNC_ERR1 is taken into account and SYNC_ERR2-4 will be ignored. If a logic 1 is received on SYNC_ERR1, the SRLI block will force the receive data stream to all zeros. In quad OC-48 mode, when ERR_ENA[n] is set to logic 1, the SYNC_ERR[n] will be taken into account. If a logic 1 is received on SYNC_ERR[n], the SRLI block will force the corresponding receive data stream to all zeros.

ERR_ENAx must be set to logic 1 to allow the propogation of the SYNC_ERRx input pin to downstream blocks.

In 10GbE LAN mode, these bits are not used.

~~In 10GbE LAN or WAN modes, ERR_ENA1 must be set to logic 1 to allow the SYNC_ERR1 input pin to cause the R64B66B to lose sync.~~

Downloaded by Conta Team Patent [illegible] on Wednesday, 07 February, 2007 06:59:32 PM

Register 003EH: SRLI Four Bytes De-Interleave control

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	FBDIEN4	1
Bit 2	R/W	FBDIEN3	1
Bit 1	R/W	FBDIEN2	1
Bit 0	R/W	FBDIEN1	1

FBDIEN1-4

The FBDI enable (FBDIEN1-4) bit controls a rotation matrix. When FBDIENx is set to logic 1, the FBDI rotation matrix is active and the bytes on the output bus are de-interleaved. When FBDIENx is set to logic 0, the FBDI rotation matrix is inactive. When used in STS-192c (STM-64c) mode, only FBDIEN1 is valid and FBDIEN2-4 is ignored.

For normal operation, these bits should be written with their default values.

Downloaded by Content Team of Partminer on Wednesday, 07 February, 2007 06:59:32 PM

Register 003FH: SRLI Test

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	R/W	Reserved	1
Bit 11	R/W	Reserved	1
Bit 10	R/W	Reserved	1
Bit 9	R/W	Reserved	1
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	1

The SRLI test register should be written to its default values for normal operation.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

12.3 SONET/SDH Bit Error Rate Monitor (SBER #1 - #4)

There are 4 SBER (#1 - #4) blocks in 4 STM-16 processing groups with independent register sets. When the S/UNI 9953 is configured for quad OC-48 mode, all four blocks are configured as masters to process the STS-48c/STM-16c data streams. When configured for OC-192 mode, only SBER#1 is configured as master and the other three (#2 - #4) blocks are inactive and may be considered as slaves.

Register 0k40H: SBER Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	SFBERTEN	0
Bit 4	R/W	SFSMODE	0
Bit 3	R/W	SFCMODE	0
Bit 2	R/W	SDBERTEN	0
Bit 1	R/W	SDSMODE	0
Bit 0	R/W	SDCMODE	0

SDCMODE

The SDCMODE alarm bit selects the Signal Degrade BERM window size to use for clearing alarms. When SDCMODE is a logic 0, the SD BERM will clear an alarm using the same window size used for declaration. When SDCMODE is a logic 1, the SD BERM will clear an alarm using a window size that is 8 times longer than alarm declaration window size. The declaration window size is defined by the SBER SD BERM Accumulation Period register.

SDSMODE

The SDSMODE bit selects the Signal Degrade BERM saturation mode. When SDSMODE is a logic 0, the SD BERM will saturate the BIP count on a per frame basis using the SBER SD Saturation Threshold register value. When SDSMODE is a logic 1, the SD BERM will saturate the BIP count on a per window subtotals accumulation period basis using the SBER SD Saturation Threshold register value.

Downloaded by Content Team at Partminer Limited on Wednesday, 07 February, 2007 06:52:10 PM

SDBERTEN

The SDBERTEN bit enables automatic monitoring of line bit error rate threshold events by the Signal Degrade BERM. When SDBERTEN is a logic one, the SD BERM continuously monitors line BIP errors over a period defined in the BERM configuration registers. When SDBERTEN is a logic zero, the SD BERM BIP accumulation logic is disabled and the BERM logic is reset to restart in the declaration monitoring state.

All SD BERM configuration registers should be set up before the monitoring is enabled.

SFCMODE

The SFCMODE alarm bit selects the Signal Failure BERM window size to use for clearing alarms. When SFCMODE is a logic 0, the SF BERM will clear an alarm using the same window size used for declaration. When SFCMODE is a logic 1, the SF BERM will clear an alarm using a window size that is 8 times longer than alarm declaration window size. The declaration window size is defined by the SBER SF BERM Accumulation Period register.

SFSMODE

The SFSMODE bit selects the Signal Failure BERM saturation mode. When SFSMODE is a logic 0, the SF BERM will saturate the BIP count on a per frame basis using the SBER SF Saturation Threshold register value. When SFSMODE is a logic 1, the SF BERM will saturate the BIP count on a per window subtotals accumulation period basis using the SBER SD Saturation Threshold register value.

SFBERTEN

The SFBERTEN bit enables automatic monitoring of line bit error rate threshold events by the Signal Failure BERM. When SFBERTEN is a logic one, the SF BERM continuously monitors line BIP errors over a period defined in the BERM configuration registers. When SFBERTEN is a logic zero, the SF BERM BIP accumulation logic is disabled, and the BERM logic is reset to restart in the declaration monitoring state.

All SF BERM configuration registers should be set up before the monitoring is enabled.

Downloaded by Content Team of Datasheet Inc on Wednesday, 01 January, 2001 06:58:32 PM

Register 0k41H: SBER Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R	SFBERV	X
Bit 0	R	SDBERV	X

SDBERV

The SDBERV bit indicates the Signal Failure BERM alarm state. The alarm is declared (SDBERV is a logic one) when the declaring threshold has been exceeded. The alarm is removed (SDBERV is a logic zero) when the clearing threshold has been reached.

SFBERV

The SFBERV bit indicates the Signal Failure BERM alarm state. The alarm is declared (SFBERV is a logic one) when the declaring threshold has been exceeded. The alarm is removed (SFBERV is a logic zero) when the clearing threshold has been reached.

Downloaded by Content Team of Datapiner Inc. on Wednesday, 07 February, 2007 06:09:32 PM

Register 0k42H: SBER Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R/W	SFBERE	0
Bit 0	R/W	SDBERE	0

SDBERE

The SDBERE bit is the interrupt enable for the SDBER alarm. When SDBERE set to logic 1, the pending interrupt in the SBER Interrupt Status register, SDBERI, will assert the interrupt (INTB) output. When SDBERE is set to logic 0, the pending interrupt will not assert the interrupt (INTB) output.

SFBERE

The SFBERE bit is the interrupt enable for the SFBER alarm. When SFBERE set to logic 1, the pending interrupt in the SBER Interrupt Status Register, SFBERI, will assert the interrupt (INTB) output. When SFBERE is set to logic 0, the pending interrupt will not assert the interrupt (INTB) output.

Downloaded by Content Team at Netminer Inc on Wednesday, 07 February, 2007 06:09:32 PM

Register 0k43H: SBER Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R	SFBERI	X
Bit 0	R	SDBERI	X

If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, these interrupt status bits are cleared on a write of logic one. Otherwise, these interrupt status bits are cleared on read.

SDBERI

The SDBERI bit is an event indicator set to logic 1 to indicate any changes in the status of SDBERV. This interrupt status bit is independent of the SDBERE interrupt enable bits.

SFBERI

The SFBERI bit is an event indicator set to logic 1 to indicate any changes in the status of SFBERV. This interrupt status bit is independent of the SFBERE interrupt enable bits.

Downloaded by Content Team of Partmine Inc on Wednesday, 07 February, 2007 06:09:32 PM

Register 0k44H: SBER SF BERM Accumulation Period (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFSAP[15:0]	0000

Register 0k45H: SBER SF BERM Accumulation Period (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFSAP[31:16]	0000

SFSAP[31:0]

The SFSAP[31:0] bits represent the number of STS-N frames to be used to accumulate a BIP error subtotal. The total evaluation window to declare an alarm is broken into 8 subtotals, so this register value represents 1/8 of the total sliding window size. Refer to the Operation section for the recommended settings.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007, 06:59:32 PM

Register 0k46H: SBER SF BERM Saturation Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFSATH[15:0]	FFFF

Register 0k47H: SBER SF BERM Saturation Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 8	—	Unused	XX
Bit 7 to Bit 0	R/W	SFSATH[23:16]	FF

SFSATH[23:0]

The SFSTH[23:0] bits represent the allowable number of BIP errors that can be accumulated during a BIP accumulation period before a BER threshold event is asserted. Setting this threshold to 0xFFFFFF disables the saturation functionality. Refer to the Operation section for the recommended settings.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007, 06:59:32 PM

Register 0k48H: SBER SF BERM Declaring Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFDECTH[15:0]	0000

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0k49H: SBER SF BERM Declaring Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 8	—	Unused	XX
Bit 7 to Bit 0	R/W	SFDECTH [23:16]	00

SFDECTH[23:0]

The SFDECTH[23:0] register represents the number of BIP errors that must be accumulated during a full evaluation window in order to declare a BER alarm. Refer to the Operation section for the recommended settings.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 7, 2007 06:39:32 PM

Register 0k4AH: SBER SF BERM Clearing Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFCLRTH[15:0]	0000

Register 0k4BH: SBER SF BERM Clearing Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 8	—	Unused	XX
Bit 7 to Bit 0	R/W	SFCLRTH [23:16]	00

SFCLRTH[23:0]

The SFCLRTH[23:0] register represents the number of BIP errors that can be accumulated but not exceeded during a full evaluation window in order to clear a BER alarm. Refer to the Operation section for the recommended settings.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007, 06:59:32 PM

Register 0k4CH: SBER SD BERM Accumulation Period (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDSAP[15:0]	0000

Register 0k4DH: SBER SD BERM Accumulation Period (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDSAP[31:16]	0000

SDSAP[31:0]

The SDSAP[31:0] bits represent the number of STS-N frames to be used to accumulate a BIP error subtotal. The total evaluation window to declare an alarm is broken into 8 subtotals, so this register value represents 1/8 of the total sliding window size. Refer to the Operation section for the recommended settings.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007, 06:59:32 PM

Register 0k4EH: SBER SD BERM Saturation Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDSATH[15:0]	FFFF

Register 0k4FH: SBER SD BERM Saturation Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 8	—	Unused	XX
Bit 7 to Bit 0	R/W	SDSATH[23:16]	FF

SDSATH[23:0]

The SDSATH[23:0] bits represent the allowable number of BIP errors that can be accumulated during a BIP accumulation period before a BER threshold event is asserted. Setting this threshold to 0xFFFFFFFF disables the saturation functionality. Refer to the Operation section for the recommended settings.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007, 06:59:32 PM

Register 0k50H: SBER SD BERM Declaring Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDDECTH[15:0]	0000

Register 0k51H: SBER SD BERM Declaring Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 8	—	Unused	XX
Bit 7 to Bit 0	R/W	SDDECTH[23:16]	00

SDDECTH[23:0]

The SDDECTH[23:0] register represents the number of BIP errors that must be accumulated during a full evaluation window in order to declare a BER alarm. Refer to the Operation section for the recommended settings.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0k52H: SBER SD BERM Clearing Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDCLRTH[15:0]	0000

Register 0k53H: SBER SD BERM Clearing Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 8	—	Unused	XX
Bit 7 to Bit 0	R/W	SDCLRTH[23:16]	00

SDCLRTH[23:0]

The SDCLRTH[23:0] register represents the number of BIP errors that can be accumulated but not exceeded during a full evaluation window in order to clear a BER alarm. Refer to the Operation section for the recommended settings.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007, 06:59:32 PM

12.4 Receive Regenerator and Multiplexer Processor (RRMP #1 - #16)

There are 16 RRMP (#1 - #16) blocks in 16 STM-4 processing slices with independent register sets. When the S/UNI 9953 is configured for quad OC-48 mode, RRMP #1, #5, #9, #13 are configured as masters and the remaining RRMP blocks are configured as slaves. When configured for OC-192 mode, only RRMP #1 is configured as master and the remaining blocks are configured as slaves.

Register 0n60H: RRMP Configuration

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	—	Unused	X
Bit 13	R/W	Reserved	0
Bit 12	R/W	LREIBLK	0
Bit 11	R/W	LBIPECNTSBLK	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	LBIPEACCBLK	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	SBIPEACCBLK	0
Bit 6	R/W	Reserved	1
Bit 5	R/W	~~Reserved~~RSLDSEL	0
Bit 4	R/W	Reserved	1
Bit 3	R/W	LRDI3	0
Bit 2	R/W	LAIS3	0
Bit 1	R/W	ALGO2	0
Bit 0	W	FOOF	X

The RRMP Configuration register controls the regenerator and Multiplexer functions.

These register bits are valid for both master and slave slices. Please refer to individual bit for details.

FOOF

The force out of frame (FOOF) bit forces the out of frame condition. When a logic 1 is written to FOOF, the framer block is forced out of frame at the next frame boundary regardless of the framing pattern value. The OOF event initiates re framing in an upstream frame detector. Once out of frame condition has been achieved, this bit should be cleared to allow re-framing.

This bit is only valid for master slices.

Downloaded by Control Team of Paltronet Inc. on Wednesday, 07 February 2007 06:42:32 PM

ALGO2

The ALGO2 bit selects the framing pattern used to determine and maintain the frame alignment. When ALGO2 is set to logic 1, the framing pattern consist of the 8 bits of the first A1 framing bytes and the first 4 bits of the last A2 framing bytes (12 bits total). This algorithm examines only 12 framing bits; all other framing bits are ignored. When ALGO2 is set to logic 0, the framing patterns consist of 12 A1 framing bytes and 12 A2 framing bytes.

This bit is only valid for master slices.

LAIS3

The line alarm indication signal detection (LAIS3) bit selects the Line AIS detection algorithm. When LAIS3 is set to logic 1, Line AIS is declared when a 111 pattern is detected in bits 6,7,8 of the K2 byte for three consecutive frames. When LAIS3 is set to logic 0, Line AIS is declared when a 111 pattern is detected in bits 6,7,8 of the K2 byte for five consecutive frames.

This bit is only valid for master slices.

LRDI3

The line remote defect indication detection (LRDI3) bit selects the Line RDI detection algorithm. When LRDI3 is set to logic 1, Line RDI is declared when a 110 pattern is detected in bits 6,7,8 of the K2 byte for three consecutive frames. When LRDI3 is set to logic 0, Line RDI is declared when a 110 pattern is detected in bits 6,7,8 of the K2 byte for five consecutive frames.

This bit is only valid for master slices.

RSLDSEL

The RSLD channel select (RSLDSEL) bit selects the contents of the overhead port and the frequency of the overhead port clock.

Note that this bit is used in conjunction with registers 0x0022 and 0x0023.

~~The receive section line data communication channel select (RSLDSEL) bit selects the contents of the RSLD serial output and the frequency of the RSLDCLK clock.~~

RSLDSEL	Contents
0	Section DCC (D1-D3)
1	Line DCC (D4-D12)

Downloaded by Content Team of Partminer Inc. on Wednesday, 01 February, 2007 00:42:32 PM

SBIPEACCBLK

The section BIP error accumulation block (SBIPEACCBLK) bit controls the accumulation of section BIP errors. When SBIPEACCBLK is set to logic 1, the section BIP accumulation represents BIP-8 block errors (a maximum of 1 error per frame). When SBIPEACCBLK is set to logic 0, the section BIP accumulation represents BIP-8 errors (a maximum of 8 errors per frame).

This bit is valid for master and slave slices.

LBIPEACCBLK

The line BIP error accumulation block (LBIPEACCBLK) bit controls the accumulation of line BIP errors. When LBIPEACCBLK is set to logic 1, the line BIP accumulation represents BIP-24 block errors (a maximum of 1 error per STS-3/STM-1 per frame). When LBIPEACCBLK is set to logic 0, the line BIP accumulation represents BIP-8 errors (a maximum of 8 errors per STS-1/STM-0 per frame).

This bit is valid for master and slave slices.

LBIPECNTSBLK

The line BIP error count saturated block (LBIPECNTSBLK) bit controls the indication of line BIP errors on the LBIPECNTS[7:0] output. When LBIPECNTSBLK is set to logic 1, the LBIPECNTS[7:0] output represents BIP-24 block errors (a maximum of 1 error per STS-3/STM-1 per frame saturated to 255). When LBIPECNTSBLK is set to logic 0, the LBIPECNTS[7:0] output represents BIP-8 errors (a maximum of 8 errors per STS-1/STM-0 per frame saturated to 255).

This bit should be set to logic 1 if block mode REI-L insertion is required on the transmit path.

LREIBLK

The line REI block (LREIBLK) bit controls the extraction of line REI errors from the M1 byte. When LREIBLK is set to logic 1, the extracted line REI is interpreted as block BIP-24 errors (a maximum of 1 error per STS-3/STM-1 per frame). When LREIBLK is set to logic 0, the extracted line REI are interpreted as BIP-8 errors (a maximum of 8 errors per STS-1/STM-0 per frame).

This bit is valid for master and slave slices.

Downloaded by Content Agent of Partminer Inc on Wednesday, 07 February, 2007 06:50:02 PM

BUSY

The BUSY (BUSY) bit reports the status of the transfer of section BIP, line BIP and line REI error counters to the holding registers. BUSY is set to logic 1 upon writing to the holding register addresses or by a microprocessor write to the S/UNI 9953 Identity and Global Performance Monitor Update register (0000H). BUSY is set to logic 0 upon completion of the transfer. This bit should be polled to determine when new data is available in the holding registers.

This bit is only valid for master slices.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 08:51:12 AM

Register 0n61H: RRMP Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R	APSBFV	X
Bit 4	R	LRDIV	X
Bit 3	R	LAISV	X
Bit 2	R	LOSV	X
Bit 1	R	LOFV	X
Bit 0	R	OOFV	X

These register bits are only valid for master slices.

OOFV

The OOFV bit reflects the current status of the out of frame defect. The OOF defect is declared when four consecutive frames have one or more bit error in their framing pattern. The OOF defect is cleared when two error free framing pattern are found.

LOFV

The LOFV bit reflects the current status of the loss of frame defect. The LOF defect is declared when an out of frame condition exists for a total period of 3 ms during which there is no continuous in frame period of 3 ms. The LOF defect is cleared when an in frame condition exists for a continuous period of 3 ms.

LOSV

The LOSV bit reflects the current status of the loss of signal defect. The LOS defect is declared when 20 µs of consecutive all zeros pattern is detected. The LOS defect is cleared when two consecutive error free framing patterns are found and during the intervening time (one frame) there is no violating period of consecutive all zeros pattern.

Downloaded by Content Team Department on Wednesday, 07 February, 2007 06:09:32 PM

LAISV

The LAISV bit reflects the current status of the line alarm indication signal defect. The AIS-L defect is declared when the 111 pattern is detected in bits 6,7 and 8 of the K2 byte for three or five consecutive frames. The AIS-L defect is cleared when any pattern other than 111 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames.

LRDIV

The LRDIV bit reflects the current status of the line remote defect indication signal defect. The RDI-L defect is declared when the 110 pattern is detected in bits 6, 7, and 8 of the k2 byte for three or five consecutive frames. The RDI-L defect is cleared when any pattern other than 110 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames.

APSBFV

The APSBF bit reflects the current status of the APS byte failure defect. The APS byte failure defect is declared when no three consecutive identical K1 bytes are received in the last twelve consecutive frames starting with the last frame containing a previously consistent byte. The APS byte failure defect is cleared when three consecutive identical K1 bytes are received.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 06:32:32 AM

Register 0n62H: RRMP Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	R/W	LREIEE	0
Bit 9	R/W	LBIPEE	0
Bit 8	R/W	SBIPEE	0
Bit 7	R/W	COSSME	0
Bit 6	R/W	COAPSE	0
Bit 5	R/W	APSBFE	0
Bit 4	R/W	LRDIE	0
Bit 3	R/W	LAISE	0
Bit 2	R/W	LOSE	0
Bit 1	R/W	LOFE	0
Bit 0	R/W	OOFE	0

These register bits are only valid for master slices. For slave slices they should be set to their default values.

OOFE, LOFE, LOSE, LAISE, LRDIE, APSBFE, COAPSE, COSSME, SBIPEE, LBIPEE, LREIEE

The interrupt enable bits controls the activation of the interrupt (INTB) output. When the interrupt enable bit is set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When the interrupt enable bit is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

Downloaded by Content Team of Parts Dev Inc on Wednesday, 07 February, 2007 06:39:32 PM

Register 0n63H: RRMP Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	R/W	LREIEI	X
Bit 9	R/W	LBIPEI	X
Bit 8	R/W	SBIPEI	X
Bit 7	R/W	COMMSI	X
Bit 6	R/W	COAPSI	X
Bit 5	R/W	APSBFI	X
Bit 4	R/W	LRDII	X
Bit 3	R/W	LAISI	X
Bit 2	R/W	LOSI	X
Bit 1	R/W	LOFI	X
Bit 0	R/W	OOFI	X

These register bits are only valid for master slices. For slave slices they should be ignored.

If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, these interrupt status bits are cleared on a write of logic one. Otherwise, these interrupt status bits are cleared on read.

OOFI

The out of frame interrupt status (OOFI) bit is an event indicator. OOFI is set to logic 1 to indicate any change in the status of OOFV. The interrupt status bit is independent of the interrupt enable bit. OOFI is cleared to logic 0 when this register is read or written as described above.

LOFI

The loss of frame interrupt status (LOFI) bit is an event indicator. LOFI is set to logic 1 to indicate any change in the status of LOFV. The interrupt status bit is independent of the interrupt enable bit. LOFI is cleared to logic 0 when this register is read or written as described above.

Downloaded by Conor Team of Planner Inc on Wednesday, 07 February, 2007 06:09:32 PM

LOSI

The loss of signal interrupt status (LOSI) bit is an event indicator. LOSI is set to logic 1 to indicate any change in the status of LOSV. The interrupt status bit is independent of the interrupt enable bit. LOSI is cleared to logic 0 when this register is read or written as described above.

LAISI

The line alarm indication signal interrupt status (LAISI) bit is an event indicator. LAISI is set to logic 1 to indicate any change in the status of LAISV. The interrupt status bit is independent of the interrupt enable bit. LAISI is cleared to logic 0 when this register is read or written as described above.

LRDII

The line remote defect indication interrupt status (LRDII) bit is an event indicator. LRDII is set to logic 1 to indicate any change in the status of LRDIV. The interrupt status bit is independent of the interrupt enable bit. LRDII is cleared to logic 0 when this register is read or written as described above.

APSBFI

The APS byte failure interrupt status (APSBFI) bit is an event indicator. APSBFI is set to logic 1 to indicate any change in the status of APSBFV. The interrupt status bit is independent of the interrupt enable bit. APSBFI is cleared to logic 0 when this register is read or written as described above.

COAPSI

The change of APS bytes interrupt status (COAPSI) bit is an event indicator. COAPSI is set to logic 1 to indicate new APS bytes. The interrupt status bit is independent of the interrupt enable bit. COAPSI is cleared to logic 0 when this register is read or written as described above.

COSSMI

The change of SSM message interrupt status (COSSMI) bit is an event indicator. COSSMI is set to logic 1 to indicate a new SSM message. The interrupt status bit is independent of the interrupt enable bit. COSSMI is cleared to logic 0 when this register is read or written as described above.

Downloaded by Conrad Team of Datasheetminer Inc on Wednesday 07 February 2007 06:59:32 PM

SBIPEI

The section BIP error interrupt status (SBIPEI) bit is an event indicator. SBIPEI is set to logic 1 to indicate a section BIP error. The interrupt status bit is independent of the interrupt enable bit. SBIPEI is cleared to logic 0 when this register is read or written as described above.

LBIPEI

The line BIP error interrupt status (LBIPEI) bit is an event indicator. LBIPEI is set to logic 1 to indicate a line BIP error. The interrupt status bit is independent of the interrupt enable bit. LBIPEI is cleared to logic 0 when this register is read or written as described above.

LREIEI

The line REI error interrupt status (LREIEI) bit is an event indicator. LREIEI is set to logic 1 to indicate a line REI error. The interrupt status bit is independent of the interrupt enable bit. LREIEI is cleared to logic 0 when this register is read or written as described above.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 06:59:32 PM

Register 0n64H: RRMP Receive APS

Bit	Type	Function	Default
Bit 15	R	K1V[7]	X
Bit 14	R	K1V[6]	X
Bit 13	R	K1V[5]	X
Bit 12	R	K1V[4]	X
Bit 11	R	K1V[3]	X
Bit 10	R	K1V[2]	X
Bit 9	R	K1V[1]	X
Bit 8	R	K1V[0]	X
Bit 7	R	K2V[7]	X
Bit 6	R	K2V[6]	X
Bit 5	R	K2V[5]	X
Bit 4	R	K2V[4]	X
Bit 3	R	K2V[3]	X
Bit 2	R	K2V[2]	X
Bit 1	R	K2V[1]	X
Bit 0	R	K2V[0]	X

These register bits are only valid for master slices. For slave slices they should be ignored.

K1V[7:0]/K2V[7:0]

The APS K1/K2 bytes value (K1V[7:0]/K2V[7:0]) bits represent the extracted K1/K2 APS bytes. K1V/K2V is updated when the same K1 and K2 bytes (forming a single entity) are received for three consecutive frames.

Downloaded by Content Team of Partminer.com on Wednesday, 07 February, 2007 06:09:32 PM

Register 0n65H: RRMP Receive SSM

Bit	Type	Function	Default
Bit 15	R/W	BYTESSM	0
Bit 14	R/W	FLTRSSM	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	SSMV[7]	X
Bit 6	R	SSMV[6]	X
Bit 5	R	SSMV[5]	X
Bit 4	R	SSMV[4]	X
Bit 3	R	SSMV[3]	X
Bit 2	R	SSMV[2]	X
Bit 1	R	SSMV[1]	X
Bit 0	R	SSMV[0]	X

These register bits are only valid for master slices. For slave slices they should be ignored or written to their default values.

SSMV[7:0]

The synchronization status message value (SSMV[7:0]) bits represent the extracted S1 nibble (or byte). When filtering is enabled via the FLTRSSM register bit, SSMV is updated when the same S1 nibble (or byte) is received for eight consecutive frames. When filtering is disabled, SSMV is updated every frame.

FLTRSSM

The filter synchronization status message (FLTRSSM) bit enables the filtering of the SSM nibble (or byte). When FLTRSSM is set to logic 1, the SSM value is updated when the same SSM is received for eight consecutive frames. When FLTRSSM is set to logic 0, the SSM value is updated every frame.

BYTESSM

The byte synchronization status message (BYTESSM) bit extends the SSM from a nibble to a byte. When BYTESSM is set to logic 1, the SSM is a byte and bits 1 to 8 of the S1 byte are considered. When BYTESSM is set to logic 0, the SSM is a nibble and only bits 5 to 8 of the S1 byte are considered.

Downloaded by Content Team of Partsrelease on Wednesday, 07 February, 2007 06:39:32 PM

Register 0n66H: RRMP AIS Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R/W	K2AIS	0
Bit 3	R/W	RLAISINS	0
Bit 2	R/W	RLAISEN	0
Bit 1	R/W	RLOHAISEN	0
Bit 0	R/W	RSOHAISEN	0

These register bits are valid for both master and slave slices. Please refer to individual bit for details.

RSOHAISEN

The receive section overhead AIS enable (RSOHAISEN) bit enables AIS insertion on RTOH when carrying section overhead bytes. When RSOHAISEN is set to logic 1, all ones are forced on the section overhead bytes when a LOF or LOS condition exists. When RSOHAISEN is set to logic 0, no AIS are forced on the section overhead bytes regardless of the alarm condition.

This bit is valid for master and slave slices.

RLOHAISEN

The receive line overhead AIS enable (RLOHAISEN) bit enables AIS insertion on RTOH, when carrying line overhead bytes. When RLOHAISEN is set to logic 1, all ones are forced on the line overhead bytes when a LOF or LOS condition exists. When RLOHAISEN is set to logic 0, no AIS are forced on the line overhead bytes regardless of the alarm condition.

This bit is valid for master and slave slices.

Downloaded by Content Team of patricg@pmc on Wednesday, 07 February, 2007 06:39:32 PM

RLAISEN

The receive line AIS enable (RLAISEN) bit enables line AIS insertion in the data stream to the POS-PHY Level 4 interface. When RLAISEN is set to logic 1, line AIS is inserted in the upstream PL4 data stream when a LOF or LOS condition exists. When RLAISEN is set to logic 0, no line AIS is inserted regardless of the alarm condition.

This bit should be set to logic 1 for normal operation. This bit is valid for master and slave slices.

RLAISINS

The receive line AIS insertion (RLAISIN) bit forces line AIS insertion in the receive SONET data stream to the POS-PHY Level 4 interface. When RLAISINS is set to logic 1, all ones are inserted in the line overhead bytes and in the payload bytes (all the bytes of the frame except the section overhead bytes) to force a line AIS condition. When RLAISINS is set to logic 0, the line AIS condition is removed.

This bit is valid for master and slave slices.

K2AIS

The K2 line AIS (K2AIS) bit restricts line AIS to the K2 byte. When K2AIS is set to logic 1, line AIS is only inserted in bits 6, 7 and 8 of the K2 byte. When K2AIS is set to logic 0, line AIS is inserted in the line overhead bytes and in the payload bytes (all the bytes of the frame except the section overhead bytes).

This bit is valid for the master slices.

Downloaded by Content Team of Partminer Inc. (Wednesday, 07 February, 2007 16:59:28 PM

Register 0n67H: RRMP Section BIP Error Counter

Bit	Type	Function	Default
Bit 15	R	SBIPE[15]	X
Bit 14	R	SBIPE[14]	X
Bit 13	R	SBIPE[13]	X
Bit 12	R	SBIPE[12]	X
Bit 11	R	SBIPE[11]	X
Bit 10	R	SBIPE[10]	X
Bit 9	R	SBIPE[9]	X
Bit 8	R	SBIPE[8]	X
Bit 7	R	SBIPE[7]	X
Bit 6	R	SBIPE[6]	X
Bit 5	R	SBIPE[5]	X
Bit 4	R	SBIPE[4]	X
Bit 3	R	SBIPE[3]	X
Bit 2	R	SBIPE[2]	X
Bit 1	R	SBIPE[1]	X
Bit 0	R	SBIPE[0]	X

These register bits are only valid for master slices.

SBIPE[15:0]

The section BIP error (SBIPE[15:0]) bits represent the number of section BIP errors that have been detected since the last accumulation interval. The error counter is transferred to the holding registers by a microprocessor write to any of the RRMP counter registers of a particular slice or the S/UNI 9953 Identity, and Global Performance Monitor Update register (0000H).

Downloaded by Content Team of Partminer.com on Wednesday, 07 February, 2007 06:09:32 PM

Register 0n68H: RRMP Line BIP Error Counter (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	LBIPE[15:0]	XXXX

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0n69H: RRMP Line BIP Error Counter (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 8	—	Unused	X
Bit 7 to Bit 0	R	LBIPE[23:16]	XX

These register bits are only valid for master slices.

LBIPE[23:0]

The line BIP error (LBIPE[23:0]) bits represent the number of line BIP errors that have been detected since the last accumulation interval. The error counter is transferred to the holding registers by a microprocessor write to any of the RRMP counter registers or the S/UNI 9953 Identity, and Global Performance Monitor Update register (0000H).

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0n6AH: RRMP Line REI Error Counter (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	LREIE[15:0]	XXXX

Register 0n6BH: RRMP Line REI Error Counter (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 8	—	Unused	X
Bit 7 to Bit 0	R	LREIE[23:16]	XX

These register bits are only valid for master slices.

LREIE[23:0]

The line REI error (LREIE[23:0]) bits represent the number of line REI errors that have been detected since the last accumulation interval. The error counter is transferred to the holding registers by a microprocessor write to any of the RRMP counter registers or the S/UNI 9953 Identity, and Global Performance Monitor Update register (0000H).

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007, 06:59:32 PM

12.5 Receive Trail Trace Processor, Section (RTTP #1 - #4)

There are 4 Section RTTP (#1 - #4) blocks in 4 STM-16 processing groups with independent register sets. When the S/UNI 9953 is configured for quad OC-48 mode, all four blocks are configured as masters to process the STS-48c/STM-16c data streams. When configured for OC-192 mode, only RTTP #1 is configured as master and the other three (#2 - #4) blocks are inactive and may be considered as slaves.

Register 0k70H: RTTP Section Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	R/W	IADDR[7]	0
Bit 12	R/W	IADDR[6]	0
Bit 11	R/W	IADDR[5]	0
Bit 10	R/W	IADDR[4]	0
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

IADDR[7:0]

The indirect address location (IADDR[7:0]) bits select which indirect address location is accessed by the current indirect transfer.

Indirect Address IADDR[7:0]	Indirect Data
0000 0000	Configuration
0000 0001 to 0011 1111	Invalid address
0100 0000	First byte of the 1/16/64 byte captured trace
0100 0001 to 0111 1111	Other bytes of the 16/64 byte captured trace
1000 0000	First byte of the 1/16/64 byte accepted trace

Downloaded by Components Department Inc. on Wednesday, 07 February, 2007 06:56:02 PM

Indirect Address IADDR[7:0]	Indirect Data
1000 0001 to 1011 1111	Other bytes of the 16/64 byte accepted trace
1100 0000	First byte of the 16/64 byte expected trace
1100 0001 to 1111 1111	Other bytes of the 16/64 byte expected trace

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 08:59:32 PM

Register 0k71H: RTTP Section Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	Unused	X
Bit 14	R/W	Unused	X
Bit 13	R/W	Unused	X
Bit 12	R/W	Unused	X
Bit 11	R/W	Unused	X
Bit 10	R/W	Unused	X
Bit 9	R/W	Unused	X
Bit 8	R/W	Unused	X
Bit 7	R/W	DATA[7]	X
Bit 6	R/W	DATA[6]	X
Bit 5	R/W	DATA[5]	X
Bit 4	R/W	DATA[4]	X
Bit 3	R/W	DATA[3]	X
Bit 2	R/W	DATA[2]	X
Bit 1	R/W	DATA[1]	X
Bit 0	R/W	DATA[0]	X

DATA[7:0]

The indirect access data (DATA[7:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transfer to DATA[7:0]. BUSY should be polled to determine when the new data is available in DATA[7:0]. When RWB is set to logic 0 (indirect write), the data from DATA[7:0] will be transferred to the addressed location in the internal RAM. The Indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[7:0] has a different meaning depending on which address of the internal RAM is being accessed.

Downloaded by Content Team of Northern Star on Wednesday, 07 February, 2007 06:59:32 PM

Register 0k71H (Indirect Register 00H): RTTP Section Trace Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R/W	SYNC_CRLF	0
Bit 5	R/W	ZEROEN	0
Bit 4	R/W	PER5	0
Bit 3	R/W	NOSYNC	0
Bit 2	R/W	LENGTH16	0
Bit 1	R/W	ALGO[1]	0
Bit 0	R/W	ALGO[0]	0

ALGO[1:0]

The trail trace algorithm select (ALGO[1:0]) bits select the algorithm used to process the trail trace message.

ALGO[1:0]	Trail Tace Agorithm
00	Algorithm disable
01	Algorithm 1
10	Algorithm 2
11	Algorithm 3

When ALGO[1:0] is set to logic 00b, the trail trace algorithms are disabled. The corresponding TIUV, TIMV register bits and the corresponding TIU, TIM output signals are set to logic 0.

Note that the algorithms 1-3 are defined in subsequent registers under each defect.

LENGTH16

The message length (LENGTH16) bit selects the length of the trail trace message used by algorithm 1 and algorithm 2. When LENGTH16 is set to logic 1, the length of the trail trace message is 16 bytes. When LENGTH16 is set to logic 0, the length of the trail trace message is 64 bytes.

Downloaded by Content Team Partner (IP) on Wednesday, 07 February, 2007 06:59:32 PM

NOSYNC

The synchronization disable (NOSYNC) bit disables the synchronization of the trail trace message in algorithm 1 and algorithm 2. When NOSYNC is set to logic 1, no synchronization is done on the trail trace message. The bytes of the trail trace message are written in the captured page as in a circular buffer. When NOSYNC is set to logic 0, synchronization is done on the trail trace message. See SYNC_CRLF to determine how synchronization is handled when NOSYNC = 0.

PER5

The message persistency (PER5) bit selects the number of multi-frames (messages) a trail trace message must receive in order to be declared persistent in algorithm 2. When PER5 is set to logic 1, the same trail trace message must be received for 5 consecutive multi-frames to be declared persistent. When PER5 is set to logic 0, the same trail trace message must be received for 3 consecutive multi-frames to be declared persistent.

ZEROEN

The all zero message enable (ZEROEN) bit selects if the all zero messages are validated or not against the expected message in algorithm 1 and algorithm 2. When ZEROEN is set to logic 1, all zero captured messages in algorithm 1 and all zero accepted messages in algorithm 2 are validated against the expected message. A match is declared when both the captured/accepted message and the expected message are all zero. When ZEROEN is set to logic 0, all zero captured messages in algorithm 1 and all zero accepted messages in algorithm 2 are not validated against the expected message but are considered match. A match is declared when the captured/accepted message is all zero regardless of the expected message.

SYNC_CRLF

The synchronization on CR/LF characters (SYNC_CRLF) bit selects if the current algorithm (except algo3) synchronizes on the CR/LF ASCII characters or on the byte with its MSB set high. When SYNC_CRLF is set to logic 1, the current algorithm synchronizes when it receives a byte containing the ASCII character “CR” (carriage return) followed by a byte containing “LF” (line feed). The current active byte then becomes the last byte of the message. When SYNC_CRLF is set to 0, the current algorithm synchronizes when receiving a byte with its MSB set to logic 1. The current active byte then becomes the first byte of the message.

Downloaded by Content Guard Datamine Inc. Wednesday, 07 February 2007 08:31:32 PM

Register 0k71H (Indirect Register 40H to 7FH): RTTP Section Captured Trace

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	CTRACE[7]	X
Bit 6	R/W	CTRACE[6]	X
Bit 5	R/W	CTRACE[5]	X
Bit 4	R/W	CTRACE[4]	X
Bit 3	R/W	CTRACE[3]	X
Bit 2	R/W	CTRACE[2]	X
Bit 1	R/W	CTRACE[1]	X
Bit 0	R/W	CTRACE[0]	X

CTRACE[7:0]

The captured trail trace message (CTRACE[7:0]) bits contain the currently received trail trace message. When algorithm 1 or 2 is selected and LENGTH16 is set to logic 1, the captured message is stored between address 40h and 4Fh. When algorithm 1 or 2 is selected and LENGTH16 is set to logic 0, the captured message is stored between address 40h and 7Fh. When NOSYNC is set to logic 1, the captured message is not synchronized. When NOSYNC is set to logic 0, the captured message is synchronized and the first byte of the message is stored at address 40h. When algorithm 3 is selected, the captured byte is stored at address 40h.

Downloaded by Content Team of Pantelion on Wednesday, 07 February, 2007 06:59:32 PM

Register 0k71H (Indirect Register 80H to BFH): RTTP Section Accepted Trace

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	ATRACE[7]	X
Bit 6	R/W	ATRACE[6]	X
Bit 5	R/W	ATRACE[5]	X
Bit 4	R/W	ATRACE[4]	X
Bit 3	R/W	ATRACE[3]	X
Bit 2	R/W	ATRACE[2]	X
Bit 1	R/W	ATRACE[1]	X
Bit 0	R/W	ATRACE[0]	X

ATRACE[7:0]

The accepted trail trace message (ATRACE[7:0]) bits contain the persistent trail trace message. When algorithm 2 is selected and PER5 is set to logic 1, the accepted message is the same trail trace message received for 5 consecutive multi-frames. When algorithm 2 is selected and PER5 is set to logic 0, the accepted message is the same trail trace message received for 3 consecutive multi-frames. When algorithm 2 is selected and LENGTH16 is set to logic 1, the accepted message is stored between address 80h and 8Fh. When algorithm 2 is selected and LENGTH16 is set to logic 0, the accepted message is stored between address 80h and BFh. When algorithm 3 is selected, the accepted byte is the same trail trace byte received for 48 frames. When algorithm 3 is selected, the accepted byte is stored at address 80h.

Downloaded by Content Team on behalf of PMC on Wednesday, 07 February, 2007 06:59:32 PM

Register 0k71H (Indirect Register C0H to FFH): RTTP Section Expected Trace

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	ETRACE[7]	X
Bit 6	R/W	ETRACE[6]	X
Bit 5	R/W	ETRACE[5]	X
Bit 4	R/W	ETRACE[4]	X
Bit 3	R/W	ETRACE[3]	X
Bit 2	R/W	ETRACE[2]	X
Bit 1	R/W	ETRACE[1]	X
Bit 0	R/W	ETRACE[0]	X

ETRACE[7:0]

The expected trail trace message (ETRACE[7:0]) bits contain a static message written by an external microprocessor. In algorithm 1, the expected message is used to validate the captured message. In algorithm 2, the expected message is used to validate the accepted message. When LENGTH16 is set to logic 1, the expected message must be written between address C0h and CFh. When LENGTH16 is set to logic 0, the accepted message must be written between address C0h and FFh.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0k72H: RTTP Section Trace Unstable Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R	TIUV	X

TIUV

Algorithm 1: TIUV is set to logic 0.

Algorithm 2: TIUV is set to logic 1 when one or more erroneous bytes are detected between the current message and the previous message in a total of 8 trail trace messages without any persistent message in between. TIUV is set to logic 0 when a persistent message is found. A persistent message is found when the same message is receive for 3 or 5 consecutive multi-frames.

Algorithm 3: TIUV is set to logic 1 when one or more erroneous bytes are detected in three consecutive sixteen byte windows. The first window starts on the first erroneous trail trace byte. TIUV is set to logic 0 when the same trail trace byte is received for 48 consecutive frames.

Downloaded by Content Team Courtesy of Wednesday, 07 February, 2007 06:59:32 PM

Register 0k73H: RTTP Section Trace Unstable Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R/W	TIUE	0

TIUE

The trace identifier unstable interrupt enable (TIUE) bit controls the activation of the interrupt (INTB) output. When this bit location is set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When this bit location is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:59:32 PM

Register 0k74H: RTTP Section Trace Unstable Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R	TIUI	X

If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, these interrupt status bits are cleared on a write of logic one. Otherwise, these interrupt status bits are cleared on read.

TIUI

The trace identifier unstable interrupt status (TIUI) bit is an event indicator. TIUI is set to logic 1 to indicate any changes in the status of TIUV (stable to unstable, unstable to stable). This interrupt status bit is independent of the interrupt enable bit.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0k75H: RTTP Section Trace Mismatch Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R	TIMV	X

TIMV

Algorithm 1: TIMV is set to logic 1 when none of the last 20 messages matches the expected message. TIMV is set to logic 0 when 16 of the last 20 messages match the expected message.

Algorithm 2: TIMV is set to logic 1 when the accepted message does not match the expected message. TIMV is set to logic 0 when the accepted message matches the expected message.

Algorithm 3: TIMV is set to logic 0.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0k76H: RTTP Section Trace Mismatch Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R/W	TIME	0

TIME

The trace identifier mismatch interrupt enable (TIME) bit controls the activation of the interrupt (INTB) output. When this bit location is set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When this bit location is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:59:32 PM

Register 0k77H: RTTP Section Trace Mismatch Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R	TIMI	X

If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, these interrupt status bits are cleared on a write of logic one. Otherwise, these interrupt status bits are cleared on read.

TIMI

The trace identifier mismatch interrupt status (TIMI) bit is an event indicator. TIMI is set to logic 1 to indicate any changes in the status of TIMV (match to mismatch, mismatch to match). This interrupt status bit is independent of the interrupt enable bit.

Downloaded by Content Team of Partsbase Inc on Wednesday, 07 February, 2007 06:59:32 PM

12.6 Receive Trail Trace Processor, Path (RTTP #1 - #4)

There are 4 Path RTTP (#1 - #4) blocks in 4 STM-16 processing groups with independent register sets. When the S/UNI 9953 is configured for quad OC-48 mode, all four blocks are configured as masters to process the STS-48c/STM-16c data streams. When configured for OC-192 mode, only RTTP #1 is configured as master and the other three (#2 - #4) blocks are inactive and may be considered as slaves.

Register 0k78H: RTTP Path Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	R/W	IADDR[7]	0
Bit 12	R/W	IADDR[6]	0
Bit 11	R/W	IADDR[5]	0
Bit 10	R/W	IADDR[4]	0
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

IADDR[7:0]

The indirect address location (IADDR[7:0]) bits select which indirect address location is accessed by the current indirect transfer.

Indirect Address IADDR[7:0]	Indirect Data
0000 0000	Configuration
0000 0001 to 0011 1111	Invalid address
0100 0000	First byte of the 1/16/64 byte captured trace
0100 0001 to 0111 1111	Other bytes of the 16/64 byte captured trace
1000 0000	First byte of the 1/16/64 byte accepted trace

Downloaded by Components Unlimited on Bartminer Inc. on Wednesday, 07 February, 2007 06:56:07 PM

Indirect Address IADDR[7:0]	Indirect Data
1000 0001 to 1011 1111	Other bytes of the 16/64 byte accepted trace
1100 0000	First byte of the 16/64 byte expected trace
1100 0001 to 1111 1111	Other bytes of the 16/64 byte expected trace

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 08:59:32 PM

Register 0k79H: RTTP Path Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	Unused	X
Bit 14	R/W	Unused	X
Bit 13	R/W	Unused	X
Bit 12	R/W	Unused	X
Bit 11	R/W	Unused	X
Bit 10	R/W	Unused	X
Bit 9	R/W	Unused	X
Bit 8	R/W	Unused	X
Bit 7	R/W	DATA[7]	X
Bit 6	R/W	DATA[6]	X
Bit 5	R/W	DATA[5]	X
Bit 4	R/W	DATA[4]	X
Bit 3	R/W	DATA[3]	X
Bit 2	R/W	DATA[2]	X
Bit 1	R/W	DATA[1]	X
Bit 0	R/W	DATA[0]	X

DATA[7:0]

The indirect access data (DATA[7:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transfer to DATA[7:0]. BUSY should be polled to determine when the new data is available in DATA[7:0]. When RWB is set to logic 0 (indirect write), the data from DATA[7:0] will be transferred to the addressed location in the internal RAM. The Indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[7:0] has a different meaning depending on which address of the internal RAM is being accessed.

Downloaded by Content Team of Northern Star on Wednesday, 07 February, 2007 06:59:32 PM

Register 0k79H (Indirect Register 00H): RTTP Path Trace Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R/W	SYNC_CRLF	0
Bit 5	R/W	ZEROEN	0
Bit 4	R/W	PER5	0
Bit 3	R/W	NOSYNC	0
Bit 2	R/W	LENGTH16	0
Bit 1	R/W	ALGO[1]	0
Bit 0	R/W	ALGO[0]	0

ALGO[1:0]

The trail trace algorithm select (ALGO[1:0]) bits select the algorithm used to process the trail trace message.

ALGO[1:0]	Trail Tace Agorithm
00	Algorithm disable
01	Algorithm 1
10	Algorithm 2
11	Algorithm 3

When ALGO[1:0] is set to logic 00b, the trail trace algorithms are disabled. The corresponding TIUV, TIMV register bits and the corresponding TIU, TIM output signals are set to logic 0.

Note that the algorithms 1-3 are defined in subsequent registers under each defect.

LENGTH16

The message length (LENGTH16) bit selects the length of the trail trace message used by algorithm 1 and algorithm 2. When LENGTH16 is set to logic 1, the length of the trail trace message is 16 bytes. When LENGTH16 is set to logic 0, the length of the trail trace message is 64 bytes.

Downloaded by Content Team Partner (IP) on Wednesday, 07 February, 2007 06:59:32 PM

NOSYNC

The synchronization disable (NOSYNC) bit disables the synchronization of the trail trace message in algorithm 1 and algorithm 2. When NOSYNC is set to logic 1, no synchronization is done on the trail trace message. The bytes of the trail trace message are written in the captured page as in a circular buffer. When NOSYNC is set to logic 0, synchronization is done on the trail trace message. See SYNC_CRLF to determine how synchronization is handled when NOSYNC = 0.

PER5

The message persistency (PER5) bit selects the number of multi-frames (messages) a trail trace message must receive in order to be declared persistent in algorithm 2. When PER5 is set to logic 1, the same trail trace message must be received for 5 consecutive multi-frames to be declared persistent. When PER5 is set to logic 0, the same trail trace message must be received for 3 consecutive multi-frames to be declared persistent.

ZEROEN

The all zero message enable (ZEROEN) bit selects if the all zero messages are validated or not against the expected message in algorithm 1 and algorithm 2. When ZEROEN is set to logic 1, all zero captured messages in algorithm 1 and all zero accepted messages in algorithm 2 are validated against the expected message. A match is declared when both the captured/accepted message and the expected message are all zero. When ZEROEN is set to logic 0, all zero captured messages in algorithm 1 and all zero accepted messages in algorithm 2 are not validated against the expected message but are considered match. A match is declared when the captured/accepted message is all zero regardless of the expected message.

SYNC_CRLF

The synchronization on CR/LF characters (SYNC_CRLF) bit selects if the current algorithm (except algo3) synchronizes on the CR/LF ASCII characters or on the byte with its MSB set high. When SYNC_CRLF is set to logic 1, the current algorithm synchronizes when it receives a byte containing the ASCII character “CR” (carriage return) followed by a byte containing “LF” (line feed). The current active byte then becomes the last byte of the message. When SYNC_CRLF is set to 0, the current algorithm synchronizes when receiving a byte with its MSB set to logic 1. The current active byte then becomes the first byte of the message.

Downloaded by Content Search Partminer Inc. Wednesday, 07 February 2007 00:00:32 PM

Register 0k79H (Indirect Register 40H to 7FH): RTTP Path Captured Trace

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	CTRACE[7]	X
Bit 6	R/W	CTRACE[6]	X
Bit 5	R/W	CTRACE[5]	X
Bit 4	R/W	CTRACE[4]	X
Bit 3	R/W	CTRACE[3]	X
Bit 2	R/W	CTRACE[2]	X
Bit 1	R/W	CTRACE[1]	X
Bit 0	R/W	CTRACE[0]	X

CTRACE[7:0]

The captured trail trace message (CTRACE[7:0]) bits contain the currently received trail trace message. When algorithm 1 or 2 is selected and LENGTH16 is set to logic 1, the captured message is stored between address 40h and 4Fh. When algorithm 1 or 2 is selected and LENGTH16 is set to logic 0, the captured message is stored between address 40h and 7Fh. When NOSYNC is set to logic 1, the captured message is not synchronized. When NOSYNC is set to logic 0, the captured message is synchronized and the first byte of the message is stored at address 40h. When algorithm 3 is selected, the captured byte is stored at address 40h.

Downloaded by Content Team of Pantelion on Wednesday, 07 February, 2007 06:59:32 PM

Register 0k79H (Indirect Register 80H to BFH): RTTP Path Accepted Trace

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	ATRACE[7]	X
Bit 6	R/W	ATRACE[6]	X
Bit 5	R/W	ATRACE[5]	X
Bit 4	R/W	ATRACE[4]	X
Bit 3	R/W	ATRACE[3]	X
Bit 2	R/W	ATRACE[2]	X
Bit 1	R/W	ATRACE[1]	X
Bit 0	R/W	ATRACE[0]	X

ATRACE[7:0]

The accepted trail trace message (ATRACE[7:0]) bits contain the persistent trail trace message. When algorithm 2 is selected and PER5 is set to logic 1, the accepted message is the same trail trace message received for 5 consecutive multi-frames. When algorithm 2 is selected and PER5 is set to logic 0, the accepted message is the same trail trace message received for 3 consecutive multi-frames. When algorithm 2 is selected and LENGTH16 is set to logic 1, the accepted message is stored between address 80h and 8Fh. When algorithm 2 is selected and LENGTH16 is set to logic 0, the accepted message is stored between address 80h and BFh. When algorithm 3 is selected, the accepted byte is the same trail trace byte received for 48 frames. When algorithm 3 is selected, the accepted byte is stored at address 80h.

Downloaded by Content Team of Chandler Inc. on Wednesday, 07 February, 2007 06:59:32 PM

Register 0k79H (Indirect Register C0H to FFH): RTTP Path Expected Trace

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	ETRACE[7]	X
Bit 6	R/W	ETRACE[6]	X
Bit 5	R/W	ETRACE[5]	X
Bit 4	R/W	ETRACE[4]	X
Bit 3	R/W	ETRACE[3]	X
Bit 2	R/W	ETRACE[2]	X
Bit 1	R/W	ETRACE[1]	X
Bit 0	R/W	ETRACE[0]	X

ETRACE[7:0]

The expected trail trace message (ETRACE[7:0]) bits contain a static message written by an external microprocessor. In algorithm 1 the expected message is used to validate the captured message. In algorithm 2 the expected message is used to validate the accepted message. When LENGTH16 is set to logic 1, the expected message must be written between address C0h and CFh. When LENGTH16 is set to logic 0, the accepted message must be written between address C0h and FFh.

Downloaded by Content Team of Partminer Wednesday, 07 February, 2007 06:59:32 PM

Register 0k7AH: RTTP Path Trace Unstable Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R	TIUV	X

TIUV

Algorithm 1: TIUV is set to logic 0.

Algorithm 2: TIUV is set to logic 1 when one or more erroneous bytes are detected between the current message and the previous message in a total of 8 trail trace messages without any persistent message in between. TIUV is set to logic 0 when a persistent message is found. A persistent message is found when the same message is receive for 3 or 5 consecutive multi-frames.

Algorithm 3: TIUV is set to logic 1 when one or more erroneous bytes are detected in three consecutive sixteen byte windows. The first window starts on the first erroneous trail trace byte. TIUV is set to logic 0 when the same trail trace byte is received for 48 consecutive frames.

Downloaded by Content Team Of Northrop Grumman on Wednesday, 07 February, 2007, 06:59:32 PM

Register 0k7BH: RTTP Path Trace Unstable Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R/W	TIUE	0

TIUE

The trace identifier unstable interrupt enable (TIUE) bit controls the activation of the interrupt (INTB) output. When this bit location is set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When this bit location is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:59:32 PM

Register 0k7CH: RTTP Path Trace Unstable Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R	TIUI	X

If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, these interrupt status bits are cleared on a write of logic one. Otherwise, these interrupt status bits are cleared on read.

TIUI

The trace identifier unstable interrupt status (TIUI) bit is an event indicator. TIUI is set to logic 1 to indicate any changes in the status of TIUV (stable to unstable, unstable to stable). This interrupt status bit is independent of the interrupt enable bit.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0k7DH: RTTP Path Trace Mismatch Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R	TIMV	X

TIMV

Algorithm 1: TIMV is set to logic 1 when none of the last 20 messages matches the expected message. TIMV is set to logic 0 when 16 of the last 20 messages match the expected message.

Algorithm 2: TIMV is set to logic 1 when the accepted message does not match the expected message. TIMV is set to logic 0 when the accepted message matches the expected message.

Algorithm 3: TIMV is set to logic 0.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0k7EH: RTTP Path Trace Mismatch Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R/W	TIME	0

TIME

The trace identifier mismatch interrupt enable (TIME) bit controls the activation of the interrupt (INTB) output. When this bit location is set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When this bit location is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:59:32 PM

Register 0k7FH: RTTP Path Trace Mismatch Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R	TIMI	X

If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, these interrupt status bits are cleared on a write of logic one. Otherwise, these interrupt status bits are cleared on read.

TIMI

The trace identifier mismatch interrupt status (TIMI) bit is an event indicator. TIMI is set to logic 1 to indicate any changes in the status of TIMV (match to mismatch, mismatch to match). This interrupt status bit is independent of the interrupt enable bit.

Downloaded by Content Team of Partsbase Inc on Wednesday, 07 February, 2007 06:59:32 PM

12.7 Receive High Order Path Processor (RHPP #1 - #16)

There are 16 RHPP (#1 - #16) blocks in 16 STM-4 processing slices with independent register sets. When the S/UNI 9953 is configured for quad OC-48 mode, RHPP #1, #5, #9, #13 are configured as masters and the remaining RHPP blocks are configured as slaves. When configured for OC-192 mode, only RHPP #1 is configured as master and the remaining blocks are configured as slaves.

Register 0n80H: RHPP Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R/W	ADDR[3]	0
Bit 8	R/W	ADDR[2]	0
Bit 7	R/W	ADDR[1]	0
Bit 6	R/W	ADDR[0]	0
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

The RHPP Indirect Address Register together with the RHPP Indirect Data Register are provided by RHPP for configuration and status retrieval for individual STS-1/STM-0 paths within the STS-12c/STM-4c data stream processed by RHPP.

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer.

PATH[3:0]	STS-1/STM-0 Pth #
0000	Invalid path
0001-1100	Path #1 to Path #12
1101-1111	Invalid path

Downloaded by Company Team of Parliament House on Wednesday, 07 February, 2007 06:53:07 PM

ADDR[2:0]

The address location (ADDR[2:0]) bits select which address location is accessed by the current indirect transfer.

Indirect Address ADDR[3:0]	Indirect Data
0000	Pointer Interpreter Configuration
0001	Error Monitor Configuration
0010	Pointer Value and ERDI
0011	Captured and Accepted PSL
0100	Expected PSL and PDI
0101	RHPP Pointer Interpreter status
0110	RHPP Path BIP Error Counter
0111	RHPP Path REI Error Counter
1000	RHPP Path Negative Justification Event Counter
1001	RHPP Path Positive Justification Event Counter
1010 to 1111	Unused

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

Downloaded by Content Team of Partmaster - Wednesday, 7 February, 2007 06:59:32 PM

Register 0n81H: RHPP Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

The Indirect Data Register together with the Indirect Address Register are provided by RHPP for configuration and status retrieval for individual STS-1/STM-0 paths within the STS-12c/STM-4c data stream processed by RHPP.

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Downloaded by Content Team Electronics Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0n81H (Indirect Register 00H): RHPP Pointer Interpreter Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved2	0
Bit 6	R/W	Reserved1	0
Bit 5	R/W	NDFCNT	0
Bit 4	R/W	INVCNT	0
Bit 3	R/W	RELAYPAIS	0
Bit 2	R/W	JUST3DIS	0
Bit 1	R/W	SSEN	0
Bit 0	—	Unused	X

The Pointer Interpreter Configuration Indirect Register is provided at RHPP r/w indirect address 00H. These register bits should normally be set low when the RHPP is configured as a slave unless indicated otherwise.

SSEN

The SS bits enable (SSEN) bit selects whether or not the SS bits are taking into account in the pointer interpreter state machine. When SSEN is set to logic 1, the SS bits must be set to 10 for a valid NORM_POINT, NDF_ENABLE, INC_IND, DEC_IND or NEW_POINT indication. When SSEN is set to logic 0, the SS bits are ignored.

JUST3DIS

The "justification more than 3 frames ago disable" (JUST3DIS) bit selects whether or not the NDF_ENABLE, INC_IND or DEC_IND pointer justifications must be more than 3 frames apart to be considered valid. When JUST3DIS is set to logic 0, the previous NDF_ENABLE, INC_IND or DEC_IND indication must be more than 3 frames ago or the present NDF_ENABLE, INC_IND or DEC_IND indication is considered an INV_POINT indication. When JUST3DIS is set to logic 1, NDF_ENABLE, INC_IND or DEC_IND indication can be every frame.

Downloaded by Conversation of Part 15 Inc on Wednesday, 07 February, 2007 06:59:32 PM

RELAYPAIS

The relay path AIS (RELAYPAIS) bit selects the condition to enter the path AIS state in the pointer interpreter state machine. When RELAYPAIS is set to logic 1, the path AIS state is entered with 1 X AIS_ind indication. When RELAYPAIS is set to logic 0, the path AIS state is entered with 3 X AIS_ind indications. This configuration bit also affects the concatenation pointer interpreter state machine. NOTE: This register bit is active even when RHPP is configured as a slave.

INVCNT

The invalid counter (INVCNT) bit selects the behavior of the consecutive INV_POINT event counter in the pointer interpreter state machine. When INVCNT is set to logic 1, the consecutive INV_POINT event counter is reset by 3 EQ_NEW_POINT indications. When INVCNT is set to logic 0, the counter is not reset by 3 EQ_NEW_POINT indications.

NDFCNT

The new data flag counter (NDFCNT) bit selects the behavior of the consecutive NDF_ENABLE event counter in the pointer interpreter state machine. When NDFCNT is set to logic 1, the NDF_ENABLE definition is enabled NDF + ss. When NDFCNT is set to logic 0, the NDF_ENABLE definition is enabled NDF + ss + offset value in the range 0 to 782. This configuration bit only changes the NDF_ENABLE definition for the consecutive NDF_ENABLE event counter to count towards LOP-P defect when the pointer is out of range, this configuration bit does not change the NDF_ENABLE definition for pointer justification.

Reserved[2:1]

The Reserved bits must be set to default logic states as indicated for proper operation of the S/UNI 9953.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 08:58:32 AM

Register 0n81H (Indirect Register 01H): RHPP Error Monitor Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	B3EONRPOH	0
Bit 10	R/W	IPREIBLK	0
Bit 9	R/W	IBER	0
Bit 8	R/W	PREIBLKACC	0
Bit 7	R/W	B3EBLK	0
Bit 6	R/W	PBIPECNTBLK	0
Bit 5	R/W	PBIPEBLKACC	0
Bit 4	R/W	Unused	0
Bit 3	R/W	PRDI10	0
Bit 2	R/W	PLMEND	0
Bit 1	R/W	PSL5	0
Bit 0	R/W	ALGO2	0

The Error Monitor Configuration Indirect Register is provided at RHPP r/w indirect address 01H. These register bits should normally be set low when the RHPP is configured as a slave unless indicated otherwise.

ALGO2

The payload signal label algorithm 2 (ALGO2) bit selects the algorithm for the PSL monitoring. When ALGO2 is set to logic 1, the ITU compliant algorithm is (algorithm 2) is used to monitor the PSL. When ALGO2 is set to logic 0, the TELCORDIA compliant algorithm (algorithm 1) is used to monitor the PSL. ALGO2 changes the PLU-P, PLM-P and PDI-P defect definitions but has no effect on UNEQ-P defect, accepted PSL and change of PSL definitions

PSL5

The payload signal label detection (PSL5) bit selects the path PSL persistence. When PSL5 is set to logic 1, a new PSL is accepted when the same PSL value is detected in the C2 byte for five consecutive frames. When PSL5 is set to logic 0, a new PSL is accepted when the same PSL value is detected in the C2 byte for three consecutive frames.

Downloaded by Cores Team of Empires Inc on Wednesday, 07 February, 2007 06:59:32 PM

PLMEND

The payload label mismatch removal (PLMEND) bit controls the removal of a PLM-P defect when an UNEQ-P defect is declared. When PLMEND is set to logic 1, a PLM-P defect is terminated when an UNEQ-P defect is declared. When PLMEND is set to logic 0, a PLM-P defect is not terminated when an UNEQ-P defect is declared.

PRDI10

The path remote defect indication detection (PRDI10) bit selects the path RDI and path ERDI persistence. When PRDI10 is set to logic 1, path RDI and path ERDI are accepted when the same pattern is detected in bits 5,6,7 of the G1 byte for ten consecutive frames. When PRDI10 is set to logic 0, path RDI and path ERDI are accepted when the same pattern is detected in bits 5,6,7 of the G1 byte for five consecutive frames.

PBIPEBLKACC

The path block BIP-8 errors accumulation (PBIPEBLKACC) bit controls the accumulation of path BIP-8 errors. When PBIPEBLKACC is set to logic 1, the path BIP-8 error accumulation represents block BIP-8 errors (a maximum of 1 error per frame). When PBIPEBLKACC is set to logic 0, the path BIP-8 error accumulation represents BIP-8 errors (a maximum of 8 errors per frame).

PBIPECNTBLK

The path block BIP-8 errors count (PBIPECNTBLK) bit controls the path BIP-8 errors on the PBIPECNT[3:0] output. When PBIPECNTBLK is set to logic 1, the PBIPECNT[3:0] outputs block BIP-8 errors (a maximum of 1 error per frame). When PBIPECNTBLK is set to logic 0, PBIPECNT[3:0] outputs BIP-8 errors (a maximum of 8 errors per frame).

This bit should be set to logic 1 if block mode REI-P insertion is required on the transmit path.

B3EBLK

The serial path block BIP-8 errors (B3EBLK) bit controls the indication of path BIP-8 errors on the B3E serial output. When B3EBLK is set to logic 1, B3E outputs block BIP-8 errors (a maximum of 1 error per frame). When B3EBLK is set to logic 0, B3E outputs BIP-8 errors (a maximum of 8 errors per frame).

Downloaded by Content Team of Partsim.com on Wednesday 07 February 2007 06:59:32 PM

PREIBLKACC

The path block REI errors accumulation (PREIBLKACC) bit controls the accumulation of path REI errors from the path status (G1) byte. When PREIBLKACC is set to logic 1, the extracted path REI errors are interpreted as block BIP-8 errors (a maximum of 1 error per frame). When PREIBLK is set to logic 0, the extracted path REI errors are interpret as BIP-8 errors (a maximum of 8 errors per frame).

IBER

The in-band error reporting (IBER) bit controls the in-band regeneration of the path status (G1) byte. When IBER is set to logic 1, the path status byte is updated with the REI-P and the ERDI-P defects that must be returned to the far end. When IBER is set to logic 0, the path status byte is not altered.

IPREIBLK

The in-band path REI block errors (IPREIBLK) bit controls the regeneration of the path REI errors in the path status (G1) byte. When IPREIBLK is set to logic 1, the path REI is updated with block BIP-8 errors (a maximum of 1 error per frame). When IPREIBLK is set to logic 0, the path REI is updated with BIP-8 errors (a maximum of 8 errors per frame).

B3EONRPOH

The B3E On RPOH bit controls whether the normal B3E output on RPOH should be replaced by the BIP-8 Error byte. When set to logic zero, B3 is output normally. When set to logic one, B3 is replaced by the BIP-8 error code.

Downloaded by Content Team of Partminer Inc on Wednesday 07 February 2007 06:53:25 PM

Register 0n81H (Indirect Register 02H): RHPP Pointer value and ERDI

Bit	Type	Function	Default
Bit 15	R	PERDIV[2]	X
Bit 14	R	PERDIV[1]	X
Bit 13	R	PERDIV[0]	X
Bit 12	—	Unused	X
Bit 11	R	SSV[1]	X
Bit 10	R	SSV[0]	X
Bit 9	R	PTRV[9]	X
Bit 8	R	PTRV[8]	X
Bit 7	R	PTRV[7]	X
Bit 6	R	PTRV[6]	X
Bit 5	R	PTRV[5]	X
Bit 4	R	PTRV[4]	X
Bit 3	R	PTRV[3]	X
Bit 2	R	PTRV[2]	X
Bit 1	R	PTRV[1]	X
Bit 0	R	PTRV[0]	X

The Pointer Value and ERDI Indirect Register is provided at RHPP r/w address 02H.

PTRV[9:0]

The path pointer value (PTRV[9:0]) bits represent the current STS (AU) pointer being processed by the pointer interpreter state machine or by the concatenation pointer interpreter state machine.

SSV[1:0]

The SS value (SSV[1:0]) bits represent the current SS (DD) bits being processed by the pointer interpreter state machine or by the concatenation pointer interpreter state machine.

PERDIV[2:0]

The path enhanced remote defect indication value (PERDIV[2:0]) bits represent the filtered path enhanced remote defect indication value. PERDIV[2:0] is updated when the same ERDI pattern is detected in bits 5,6,7 of the G1 byte for five or ten consecutive frames (selectable with the PRDI10 register bit). NOTE: PERDIV[2:0] is undefined when the RHPP is configured as a slave.

Downloaded by Cortina Team of Partminer Co. on Wednesday, 07 February, 2007 06:59:32 PM

Register 0n81H (Indirect Register 03H): RHPP captured and accepted PSL

Bit	Type	Function	Default
Bit 15	R	CPSLV[7]	X
Bit 14	R	CPSLV[6]	X
Bit 13	R	CPSLV[5]	X
Bit 12	R	CPSLV[4]	X
Bit 11	R	CPSLV[3]	X
Bit 10	R	CPSLV[2]	X
Bit 9	R	CPSLV[1]	X
Bit 8	R	CPSLV[0]	X
Bit 7	R	APSLV[7]	X
Bit 6	R	APSLV[6]	X
Bit 5	R	APSLV[5]	X
Bit 4	R	APSLV[4]	X
Bit 3	R	APSLV[3]	X
Bit 2	R	APSLV[2]	X
Bit 1	R	APSLV[1]	X
Bit 0	R	APSLV[0]	X

The Captured and Accepted PSL Indirect Register is provided at RHPP r/w address 03H. These register bits should normally be ignored when the RHPP is configured as a slave unless indicated otherwise.

APSLV[7:0]

The accepted path signal label value (APSLV[7:0]) bits represent the last accepted path signal label value. A new PSL is accepted when the same PSL value is detected in the C2 byte for three or five consecutive frames (selectable with the PSL5 register bit). This is the case when ALGO2 is set to logic one (algorithm 2).

APSLV[7:0] is undefined when ALGO2 register bit is set to logic zero (i.e. algorithm 1).

CPSLV[7:0]

The captured path signal label value (CPSLV[7:0]) bits represent the last captured path signal label value. A new PSL is captured every frame from the C2 byte.

Downloaded by Conten Team of Pairs Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0n81H (Indirect Register 04H): RHPP Expected PSL and PDI

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R/W	PDIRANGbE	0
Bit 12	R/W	PDI[4]	0
Bit 11	R/W	PDI[3]	0
Bit 10	R/W	PDI[2]	0
Bit 9	R/W	PDI[1]	0
Bit 8	R/W	PDI[0]	0
Bit 7	R/W	EPSL[7]	0
Bit 6	R/W	EPSL[6]	0
Bit 5	R/W	EPSL[5]	0
Bit 4	R/W	EPSL[4]	0
Bit 3	R/W	EPSL[3]	0
Bit 2	R/W	EPSL[2]	0
Bit 1	R/W	EPSL[1]	0
Bit 0	R/W	EPSL[0]	0

The Expected PSL and PDI Indirect Register is provided at RHPP r/w indirect address 04H. These register bits should normally be set low when the RHPP is configured as a slave unless indicated otherwise.

EPSL[7:0]

The expected path signal label (EPSL[7:0]) bits represent the expected path signal label. The expected PSL and the expected PDI validate the received or the accepted PSL to declare PLM-P, UNEQ-P and PDI-P defects according Table 2.

PDI[4:0], PDIRANGbE

The payload defect indication (PDI[4:0]) bits and the payload defect indication range (PDIRANGbE) bit determine the expected payload defect indication according to Table 3. When PDIRANGbE is set to logic 1, the PDI range is enabled and the expected PDI range is from E1H to E0H+PDI[4:0]. When PDIRANGbE is set to logic 0, the PDI range is disable and the expected PDI value is E0H+PDI[4:0]. The expected PSL and the expected PDI validate the received or the accepted PSL to declare PLM-P, UNEQ-P and PDI-P defects according Table 2.

Downloaded by Cooper Standard Partners Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0n81H (Indirect Register 05H): RHPP Pointer Interpreter status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R	NDFV	X
Bit 5	R	Reserved	X
Bit 4	R	INVNDF	X
Bit 3	R	DISCOPA	X
Bit 2	R	CONCAT	X
Bit 1	R	ILLJREQ	X
Bit 0	—	Unused	X

The Pointer Interpreter Status Indirect Register is provided at RHPP r/w indirect address 05H. These register bits should normally be ignored when the RHPP is configured as a slave unless indicated otherwise.

ILLJREQ

The illegal pointer justification request (ILLJREQ) signal is set high when a positive and/or negative pointer adjustment is received within three frames of a pointer justification event (inc_ind, dec_ind) or an NDF triggered active offset adjustment (NDF_enable).

CONCAT

The CONCAT bit is set high if the H1 and H2 pointer bytes received match the concatenation indication (one of the five NDF_enable patterns in the NDF field, don't care in the size field, and all-ones in the pointer offset field). NOTE: This register bit is active when RHPP is configured as a slave.

DISCOPA

The discontinuous change of pointer alignment (DISCOPA) signal is set high when there is a pointer adjustment due to receiving a pointer repeated three times.

Downloaded by Content Group of Partner Inc on Wednesday, 07 February, 2007 06:59:32 PM

INVNDF

The invalid new data flag (INVNDF) signal is set high when an invalid NDF code is received.

NDFV

The new data flag (NDFV) signal is set high when an enabled New Data Flag is received indicating a pointer adjustment (NDF_enabled indication).

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0n81H (Indirect Register 06H): RHPP Path BIP Error Counter

Bit	Type	Function	Default
Bit 15	R	PBIPE[15]	X
Bit 14	R	PBIPE[14]	X
Bit 13	R	PBIPE[13]	X
Bit 12	R	PBIPE[12]	X
Bit 11	R	PBIPE[11]	X
Bit 10	R	PBIPE[10]	X
Bit 9	R	PBIPE[9]	X
Bit 8	R	PBIPE[8]	X
Bit 7	R	PBIPE[7]	X
Bit 6	R	PBIPE[6]	X
Bit 5	R	PBIPE[5]	X
Bit 4	R	PBIPE[4]	X
Bit 3	R	PBIPE[3]	X
Bit 2	R	PBIPE[2]	X
Bit 1	R	PBIPE[1]	X
Bit 0	R	PBIPE[0]	X

The Path BIP Error Counter Indirect register is provided at RHPP r/w indirect address 06H. These register bits should normally be ignored when the RHPP is configured as a slave unless indicated otherwise.

PBIPE[15:0]

The path BIP error (PBIPE[15:0]) bits represent the number of path BIP errors that have been detected in the B3 byte since the last accumulation interval. The error counters are transferred to the holding registers by a microprocessor write to the S/UNI 9953 Identity, and Global Performance Monitor Update register (Register 0000H). The TIP register bit indicates the transfer status.

Downloaded by Content Team of Parts Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0n81H (Indirect Register 07H): RHPP Path REI Error Counter

Bit	Type	Function	Default
Bit 15	R	PREIE[15]	X
Bit 14	R	PREIE[14]	X
Bit 13	R	PREIE[13]	X
Bit 12	R	PREIE[12]	X
Bit 11	R	PREIE[11]	X
Bit 10	R	PREIE[10]	X
Bit 9	R	PREIE[9]	X
Bit 8	R	PREIE[8]	X
Bit 7	R	PREIE[7]	X
Bit 6	R	PREIE[6]	X
Bit 5	R	PREIE[5]	X
Bit 4	R	PREIE[4]	X
Bit 3	R	PREIE[3]	X
Bit 2	R	PREIE[2]	X
Bit 1	R	PREIE[1]	X
Bit 0	R	PREIE[0]	X

The Path REI Error Counter Indirect register is provided at RHPP r/w indirect address 07H. These register bits should normally be ignored when the RHPP is configured as a slave unless indicated otherwise.

PREIE[15:0]

The path REI error (PREIE[15:0]) bits represent the number of path REI errors that have been extracted from the G1 byte since the last accumulation interval. The error counters are transferred to the holding registers by a microprocessor write to the S/UNI 9953 Identity, and Global Performance Monitor Update register (Register 0000H). The TIP register bit indicates the transfer status.

Downloaded by Content Team of Parts-i-Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0n81H (Indirect Register 08H): RHPP Path Negative Justification Event Counter

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	R	PNJE[12]	X
Bit 11	R	PNJE[11]	X
Bit 10	R	PNJE[10]	X
Bit 9	R	PNJE[9]	X
Bit 8	R	PNJE[8]	X
Bit 7	R	PNJE[7]	X
Bit 6	R	PNJE[6]	X
Bit 5	R	PNJE[5]	X
Bit 4	R	PNJE[4]	X
Bit 3	R	PNJE[3]	X
Bit 2	R	PNJE[2]	X
Bit 1	R	PNJE[1]	X
Bit 0	R	PNJE[0]	X

The Path Negative Justification Event Counter Indirect register is provided at RHPP r/w indirect address 08H. These register bits should normally be ignored when the RHPP is configured as a slave unless indicated otherwise.

PNJE[12:0]

The Path Negative Justification Event (PNJE[12:0]) bits represent the number of Path Negative Justification Events that have occurred since the last accumulation interval. The event counters are transferred to the holding registers by a microprocessor write to the S/UNI 9953 Identity, and Global Performance Monitor Update register (Register 0000H). The TIP register bit indicates the transfer status.

Downloaded by Content Team of Pericom Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0n81H (Indirect Register 09H): RHPP Path Positive Justification Event Counter

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	R	PPJE[12]	X
Bit 11	R	PPJE[11]	X
Bit 10	R	PPJE[10]	X
Bit 9	R	PPJE[9]	X
Bit 8	R	PPJE[8]	X
Bit 7	R	PPJE[7]	X
Bit 6	R	PPJE[6]	X
Bit 5	R	PPJE[5]	X
Bit 4	R	PPJE[4]	X
Bit 3	R	PPJE[3]	X
Bit 2	R	PPJE[2]	X
Bit 1	R	PPJE[1]	X
Bit 0	R	PPJE[0]	X

The Path Positive Justification Event Counter Indirect register is provided at RHPP r/w indirect address 09H. These register bits should normally be ignored when the RHPP is configured as a slave unless indicated otherwise.

PPJE[12:0]

The Path Positive Justification Event (PPJE[12:0]) bits represent the number of Path Positive Justification Events that have occurred since the last accumulation interval. The event counters are transferred to the holding registers by a microprocessor write to the S/UNI 9953 Identity, and Global Performance Monitor Update register (Register 0000H). The TIP register bit indicates the transfer status.

Downloaded by Content Team of Parts-i-e Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0n82H: RHPP Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved2	0
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	R/W	Reserved1	0
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

The RHPP Payload Configuration Register is provided for master/slave configuration of the RHPP.

Reserved[2:1]

The Reserved[2:1] bits must be set to logic 0 for proper operation of the S/UNI 9953.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0n84H: RHPP Path Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	P_INT[12]	X
Bit 10	R	P_INT[11]	X
Bit 9	R	P_INT[10]	X
Bit 8	R	P_INT[9]	X
Bit 7	R	P_INT[8]	X
Bit 6	R	P_INT[7]	X
Bit 5	R	P_INT[6]	X
Bit 4	R	P_INT[5]	X
Bit 3	R	P_INT[4]	X
Bit 2	R	P_INT[3]	X
Bit 1	R	P_INT[2]	X
Bit 0	R	P_INT[1]	X

The RHPP Path Interrupt Status Register provides an overview of the interrupt status on a per STS-1/STM-0 path basis within the STS-12c/STM-4c payload processed by RHPP.

P_INT[1:12]

The Path Interrupt Status bit (P_INT[1:12]) tells which path(s) have interrupts that are still active. Reading from this register will not clear any of the interrupts, it is simply added to reduce the average number of accesses required to service interrupts.

Downloaded by Content Team of Partminer.inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0n85H: RHPP Pointer Concatenation processing Disable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	PTRCDIS[12]	0
Bit 10	R/W	PTRCDIS[11]	0
Bit 9	R/W	PTRCDIS[10]	0
Bit 8	R/W	PTRCDIS[9]	0
Bit 7	R/W	PTRCDIS[8]	0
Bit 6	R/W	PTRCDIS[7]	0
Bit 5	R/W	PTRCDIS[6]	0
Bit 4	R/W	PTRCDIS[5]	0
Bit 3	R/W	PTRCDIS[4]	0
Bit 2	R/W	PTRCDIS[3]	0
Bit 1	R/W	PTRCDIS[2]	0
Bit 0	R/W	PTRCDIS[1]	0

The RHPP Pointer Concatenation processing Disable Register is provided for selective disable of concatenation pointer processing on a per STS-1/STM-0 path basis within the STS-12c/STM-4c payload processed by RHPP.

PTRCDIS[1:12]

The concatenation pointer processing disable (PTRCDIS[1:12]) bits disable the path concatenation pointer interpreter state machine. When PTRCDIS[n] is set to logic 1, the path concatenation pointer interpreter state-machine (for the path n) is disabled and excluded from the LOPC-P, AISC-P and ALLAISC-P defect declaration. When PTRCDIS is set to logic 0, the path concatenation pointer interpreter state-machine is enabled and included in the LOPC-P, AISC-P and ALLAISC-P defect declaration.

Downloaded by Content Team of Datasheet Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0n86H: RHPP Path AIS and AISC Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	R	PAISCV[12]	X
Bit 11	R	PAISCV[11]	X
Bit 10	R	PAISCV[10]	X
Bit 9	R	PAISCV[9]	X
Bit 8	R	PAISCV[8]	X
Bit 7	R	PAISCV[7]	X
Bit 6	R	PAISCV[6]	X
Bit 5	R	PAISCV[5]	X
Bit 4	R	PAISCV[4]	X
Bit 3	R	PAISCV[3]	X
Bit 2	R	PAISCV[2]	X
Bit 1	R	PAISCV[1]	X
Bit 0	R	PAISV	X

The RHPP Path AIS and AISC Status Register provides the path alarm on a per STS-1/STM-0 path basis within the STS-12c/STM-4c payload processed by RHPP.

PAISV

The path alarm indication signal state (PAISV) bit indicates the current status of the pointer interpreter state machine. PAISV is set to logic 1 when the state machine is in the AIS_state. PAISV is set to logic 0 when the state machine is not in the AIS_state. PAISV can only arise from path one since this TSB can only process STS-12c pointers. PAISV is undefined when processing a slave STS-12c that is part of STS-nX12c (like a STS-48c).

PAISCV[1:12]

The path concatenation alarm indication signal state (PAISCV[1:12]) register bits indicate the current status of the concatenation pointer interpreter state machines. PAISCV[n] is set to logic 1 when the state machine (for the path n) is in the AISC_state. PAISCV[n] is set to logic 0 when the state machine (for the path n) is not in the LOPC_state.

Downloaded by Content Team of Parts Life Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0n87H: RHPP Path LOP and LOPC Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	R	PLOPCV[12]	X
Bit 11	R	PLOPCV[11]	X
Bit 10	R	PLOPCV[10]	X
Bit 9	R	PLOPCV[9]	X
Bit 8	R	PLOPCV[8]	X
Bit 7	R	PLOPCV[7]	X
Bit 6	R	PLOPCV[6]	X
Bit 5	R	PLOPCV[5]	X
Bit 4	R	PLOPCV[4]	X
Bit 3	R	PLOPCV[3]	X
Bit 2	R	PLOPCV[2]	X
Bit 1	R	PLOPCV[1]	X
Bit 0	R	PLOPV	X

The RHPP Path LOP and LOPC Status Register provides the path alarm on a per STS-1/STM-0 path basis within the STS-12c/STM-4c payload processed by RHPP.

PLOPV

The path lost of pointer state (PLOPV) bit indicates the current status of the pointer interpreter state machine. PLOPV is set to logic 1 when the state machine is in the LOP_state. PLOPV is set to logic 0 when the state machine is not in the LOP_state. PLOPV can only arise from path one since this TSB can only process STS-12c pointers. PLOPV is undefined when processing a slave STS-12c that is part of STS-nX12c (like a STS-48c).

PLOPCV[1:12]

The path lost of pointer concatenation state (PLOPCV[1:12]) register bits indicate the current status of the concatenation pointer interpreter state machines. PLOPCV[n] is set to logic 1 when the state machine (for the path n) is in the LOPC_state. PLOPCV[n] is set to logic 0 when the state machine (for the path n) is not in the LOPC_state.

Downloaded by Conseil Exam of Paris Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0n88H: RHPP Error Monitor Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R	PERDIV	X
Bit 5	R	PRDIV	X
Bit 4	R	PPDIV	X
Bit 3	R	PUNEQV	X
Bit 2	R	PPLMV	X
Bit 1	R	PPLUV	X
Bit 0	—	Unused	X

The RHPP Error Monitor Status Register provides the path alarm for the STS-12c/STM-4c payload processed by RHPP. These register bits should normally be ignored when the RHPP is configured as a slave unless indicated otherwise.

PPLUV

The path payload label unstable status (PPLUV) bit indicates the current status of the PLU-P defect.

Algorithm 1: PPLUV is set to logic 0.

Algorithm 2: PPLUV is set to logic 1 when a total of 5 received PSL differs from the previously accepted PSL without any persistent PSL in between. PPLUV is set to logic 0 when a persistent PSL is found. A persistent PSL is found when the same PSL is received for 3 or 5 consecutive frames.

Downloaded by Content Team at Palomine Inc on Wednesday, 07 February, 2007 06:59:32 PM

PPLMV

The path payload label mismatch status (PPLMV) bit indicates the current status of the PLM-P defect.

Algorithm 1: PPLMV is set to logic 1 when the received PSL does not match, according to Table 2, the expected PSL for 3 or 5 consecutive frames (selectable with the PSL5 register bit). PPLMV is set to logic 0 when the received PSL matches, according to Table 2, the expected PSL for 3 or 5 consecutive frames.

Algorithm 2: PPLMV is set to logic 1 when the accepted PSL does not match, according to Table 2, the expected PSL. PPLMV is set to logic 0 when the accepted PSL matches, according to Table 2, the expected PSL.

PUNEQV

The path unequipped status (PUNEQV) bit indicates the current status of the UNEQ-P defect.

PUNEQV is set to logic 1 when the received PSL indicates unequipped, according to Table 2, for 3 or 5 consecutive frames (selectable with the PSL5 register bit). An PUNEQV is set to logic 0 when the received PSL indicates not unequipped, according to Table 2, for 3 or 5 consecutive frames.

PPDIV

The path payload defect indication status (PPDIV) bit indicates the current status of the PPDI-P defect.

Algorithm 1: PPDIV is set to logic one when the received PSL is a defect, according to Table 2, for 3 or 5 consecutive frames (selectable with the PSL5 register bit). PPDIV is set to logic 0 when the received PSL is not a defect, according to Table 2, for 3 or 5 consecutive frames.

Algorithm 2: PPDIV is set to logic 1 when the accepted PSL is a defect, according to Table 2. PPDI is set to logic 0 when the accepted PSL is not a defect, according to Table 2.

PRDIV

The path remote defect indication status (PRDIV) bit indicates the current status of the RDI-P defect. PRDIV is set to logic 1 when bit 5 of the G1 byte is set high for five or ten consecutive frames (selectable with the PRDI10 register bit). PRDIV is set to logic 0 when bit 5 of the G1 byte is set low for five or ten consecutive frames.

Downloaded by Content Team of Pantheon Info on Wednesday, 07 February 2007 08:09:32 PM

PERDIV

The path enhanced remote defect indication status (PERDIV) bit indicates the current status of the ERDI-P defect. PERDIV is set to logic 1 when the same 010, 100, 101, 110 or 111 pattern is detected in bits 5, 6 and 7 of the G1 byte for five or ten consecutive frames (selectable with the PRDI10 register bit). PERDIV is set to logic 0 when the same 000, 001 or 011 pattern is detected in bits 5, 6 and 7 of the G1 byte for five or ten consecutive frames.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 08:38:32 AM

Register 0n89H: RHPP Path AIS, AISC and PTRJE Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R/W	PTRJEE	0
Bit 12	R/W	PAISCE[12]	0
Bit 11	R/W	PAISCE[11]	0
Bit 10	R/W	PAISCE[10]	0
Bit 9	R/W	PAISCE[9]	0
Bit 8	R/W	PAISCE[8]	0
Bit 7	R/W	PAISCE[7]	0
Bit 6	R/W	PAISCE[6]	0
Bit 5	R/W	PAISCE[5]	0
Bit 4	R/W	PAISCE[4]	0
Bit 3	R/W	PAISCE[3]	0
Bit 2	R/W	PAISCE[2]	0
Bit 1	R/W	PAISCE[1]	0
Bit 0	R/W	PAISE	0

The RHPP Path AIS, AISC and PTRJE Enable Register is provided for path alarm interrupt enable on a per STS-1/STM-0 path basis within the STS-12c/STM-4c payload processed by RHPP.

PTRJEE

The pointer justification event interrupt enable (PTRJEE) bit control the activation of the interrupt (INTB) output. When PTRJEE is set to logic 1, the NJEI and PJEI pending interrupt will assert the interrupt (INTB) output. When PTRJEE is set to logic 0, the NJEI and PJEI pending interrupt will not assert the interrupt (INTB) output. NOTE: This register bit should normally be set low when the RHPP is configured as a slave.

PAISE

The path alarm indication signal interrupt enable (PAISE) bit controls the activation of the interrupt (INTB) output. When PAISE is set to logic 1, the PAISI pending interrupt will assert the interrupt (INTB) output. When PAISE is set to logic 0, the PAISI pending interrupt will not assert the interrupt (INTB) output. NOTE: This register bit should normally be set low when the RHPP is configured as a slave.

Downloaded by Courtesy of Pmc-Sierra Inc on Wednesday, 07 February, 2007 06:59:32 PM

PAISCE[1:12]

The path concatenation alarm indication signal interrupt enable (PAISCE[1:12]) register bits control the activation of the interrupt (INTB) output. When PAISCE[n] is set to logic 1, the PAISCI[n] pending interrupt will assert the interrupt (INTB) output. When PAISCE[n] is set to logic 0, the PAISCI[n] pending interrupt will not assert the interrupt (INTB) output.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:5[illegible] AM

Register 0n8AH: RHPP Path LOP and LOPC Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	R/W	PLOPCE[12]	0
Bit 11	R/W	PLOPCE[11]	0
Bit 10	R/W	PLOPCE[10]	0
Bit 9	R/W	PLOPCE[9]	0
Bit 8	R/W	PLOPCE[8]	0
Bit 7	R/W	PLOPCE[7]	0
Bit 6	R/W	PLOPCE[6]	0
Bit 5	R/W	PLOPCE[5]	0
Bit 4	R/W	PLOPCE[4]	0
Bit 3	R/W	PLOPCE[3]	0
Bit 2	R/W	PLOPCE[2]	0
Bit 1	R/W	PLOPCE[1]	0
Bit 0	R/W	PLOPE	0

The RHPP Path LOP and LOPC Interrupt Enable Register is provided for path alarm interrupt enable on a per STS-1/STM-0 path basis within the STS-12c/STM-4c payload processed by RHPP.

PLOPE

The path loss of pointer interrupt enable (PLOPE) bit controls the activation of the interrupt (INTB) output. When PLOPE is set to logic 1, the PLOPI pending interrupt will assert the interrupt (INTB) output. When PLOPE is set to logic 0, the PLOPI pending interrupt will not assert the interrupt (INTB) output. NOTE: This register bit should normally be set low when the RHPP is configured as a slave.

PLOPCE

The path loss of pointer concatenation interrupt enable (PLOPCE) register bits control the activation of the interrupt (INTB) output. When PLOPCE[n] is set to logic 1, the PLOPCI[n] pending interrupt will assert the interrupt (INTB) output. When PLOPCE[n] is set to logic 0, the PLOPCI[n] pending interrupt will not assert the interrupt (INTB) output.

Downloaded by Conten Team of PMC-Sierra Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0n8BH: RHPP Error Monitor Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R/W	PREIEE	0
Bit 8	R/W	PBIPEE	0
Bit 7	R/W	COPERDIE	0
Bit 6	R/W	PERDIE	0
Bit 5	R/W	PRDIE	0
Bit 4	R/W	PPDIE	0
Bit 3	R/W	PUNEQE	0
Bit 2	R/W	PPLME	0
Bit 1	R/W	PPLUE	0
Bit 0	R/W	COPSLE	0

The RHPP Error Monitor Interrupt Enable Register is provided for path alarm interrupt enable for the STS-12c/STM-4c payload processed by RHPP. These register bits should normally be set low when the RHPP is configured as a slave unless indicated otherwise.

COPSLE

The change of path payload signal label interrupt enable (COPSLE) bit controls the activation of the interrupt (INTB) output. When COPSLE is set to logic 1, the COPSLI pending interrupt will assert the interrupt (INTB) output. When COPSLE is set to logic 0, the COPSLI pending interrupt will not assert the interrupt (INTB) output.

PPLUE

The path payload label unstable interrupt enable (PPLUE) bit controls the activation of the interrupt (INTB) output. When PPLUE is set to logic 1, the PPLUI pending interrupt will assert the interrupt (INTB) output. When PPLUE is set to logic 0, the PPLUI pending interrupt will not assert the interrupt (INTB) output.

PPLME

The path payload label mismatch interrupt enable (PPLME) bit controls the activation of the interrupt (INTB) output. When PPLME is set to logic 1, the PPLMI pending interrupt will assert the interrupt (INTB) output. When PPLME is set to logic 0, the PPLMI pending interrupt will not assert the interrupt (INTB) output.

Downloaded by Content Agent of Parts-i.e. Inc on Wednesday, 07 February, 2007 06:59:32 PM

PUNEQE

The path payload unequipped interrupt enable (PUNEQE) bit controls the activation of the interrupt (INTB) output. When PUNEQE is set to logic 1, the PUNEQI pending interrupt will assert the interrupt (INTB) output. When PUNEQE is set to logic 0, the PUNEQI pending interrupt will not assert the interrupt (INTB) output.

PPDIE

The path payload defect indication interrupt enable (PPDIE) bit controls the activation of the interrupt (INTB) output. When PPDIE is set to logic 1, the PPDI pending interrupt will assert the interrupt (INTB) output. When PPDIE is set to logic 0, the PPDI pending interrupt will not assert the interrupt (INTB) output.

PRDIE

The path remote defect indication interrupt enable (PRDIE) bit controls the activation of the interrupt (INTB) output. When PRDIE is set to logic 1, the PRDII pending interrupt will assert the interrupt (INTB) output. When PRDIE is set to logic 0, the PRDII pending interrupt will not assert the interrupt (INTB) output.

PERDIE

The path enhanced remote defect indication interrupt enable (PERDIE) bit controls the activation of the interrupt (INTB) output. When PERDIE is set to logic 1, the PERDII pending interrupt will assert the interrupt (INTB) output. When PERDIE is set to logic 0, the PERDII pending interrupt will not assert the interrupt (INTB) output.

COPERDIE

The change of path enhanced remote defect indication interrupt enable (COPERDIE) bit controls the activation of the interrupt (INTB) output. When COPERDIE is set to logic 1, the COPERDII pending interrupt will assert the interrupt (INTB) output. When COPERDIE is set to logic 0, the COPERDII pending interrupt will not assert the interrupt (INTB) output.

PBIPEE

The path BIP-8 error interrupt enable (PBIPEE) bit controls the activation of the interrupt (INTB) output. When PBIPEE is set to logic 1, the PBIPEI pending interrupt will assert the interrupt (INTB) output. When PBIPEE is set to logic 0, the PBIPEI pending interrupt will not assert the interrupt (INTB) output.

Downloaded by Component Team at Planner Inc on Wednesday, 07 February 2007 06:59:42 PM

PREIEE

The path REI error interrupt enable (PREIEE) bit controls the activation of the interrupt (INTB) output. When PREIEE is set to logic 1, the PREIEI pending interrupt will assert the interrupt (INTB) output. When PREIEE is set to logic 0, the PREIEI pending interrupt will not assert the interrupt (INTB) output.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0n8CH: RHPP Path AIS, AISC, NJE and PJE Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	R	PJEI	X
Bit 13	R	NJEI	X
Bit 12	R	PAISCI[12]	X
Bit 11	R	PAISCI[11]	X
Bit 10	R	PAISCI[10]	X
Bit 9	R	PAISCI[9]	X
Bit 8	R	PAISCI[8]	X
Bit 7	R	PAISCI[7]	X
Bit 6	R	PAISCI[6]	X
Bit 5	R	PAISCI[5]	X
Bit 4	R	PAISCI[4]	X
Bit 3	R	PAISCI[3]	X
Bit 2	R	PAISCI[2]	X
Bit 1	R	PAISCI[1]	X
Bit 0	R	PAISI	X

The RHPP Path AIS, AISC, NJE and PJE Interrupt Status Register provides path alarm interrupt status on a per STS-1/STM-0 path basis within the STS-12c/STM-4c payload processed by RHPP. If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, these interrupt status bits are cleared on write with a logic 1. Otherwise, these interrupt status bits are cleared on read as per register bit description.

NJEI

The negative pointer justification event interrupt status (NJEI) bit is an event indicator. NJEI is set to logic 1 to indicate a negative pointer justification event. The interrupt status bit is independent of the interrupt enable bit. NJEI is cleared to logic 0 when this register is read. NOTE: This register bit should normally be ignored when the RHPP is configured as a slave.

PJEI

The positive pointer justification event interrupt status (PJEI) bit is an event indicator. PJEI is set to logic 1 to indicate a positive pointer justification event. The interrupt status bit is independent of the interrupt enable bit. PJEI is cleared to logic 0 when this register is read. NOTE: This register bit should normally be ignored when the RHPP is configured as a slave.

Downloaded by Cortet Team of Mariner Inc on Wednesday, 07 February, 2007 06:59:32 PM

PAISI

The path alarm indication signal interrupt status (PAISI) bit is an event indicator. PAISI is set to logic 1 to indicate any change in the status of PAISV (entry to the AIS_state or exit from the AIS_state). The interrupt status bit is independent of the interrupt enable bit. PAISI is cleared to logic 0 when this register is read. NOTE: This register bit should normally be ignored when the RHPP is configured as a slave.

PAISCI[1:12]

The path concatenation alarm indication signal interrupt status (PAISCI[1:12]) register bits are event indicators. PAISCI[n] is set to logic 1 to indicate any change in the status of PAISCV[n] (entry to the AISC_state or exit from the AISC_state for the path n). The interrupt status bit is independent of the interrupt enable bit. PAISCI[1:12] is cleared to logic 0 when this register is read.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 Feb 2007 06:58:22 PM

Register 0n8DH: RHPP Path LOP and LOPC Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	R	PLOPCI[12]	X
Bit 11	R	PLOPCI[11]	X
Bit 10	R	PLOPCI[10]	X
Bit 9	R	PLOPCI[9]	X
Bit 8	R	PLOPCI[8]	X
Bit 7	R	PLOPCI[7]	X
Bit 6	R	PLOPCI[6]	X
Bit 5	R	PLOPCI[5]	X
Bit 4	R	PLOPCI[4]	X
Bit 3	R	PLOPCI[3]	X
Bit 2	R	PLOPCI[2]	X
Bit 1	R	PLOPCI[1]	X
Bit 0	R	PLOPI	X

The RHPP Path LOP and LOPC Interrupt Status Register provides path alarm interrupt status on a per STS-1/STM-0 path basis within the STS-12c/STM-4c payload processed by RHPP. If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, these interrupt status bits are cleared on write with a logic 1. Otherwise, these interrupt status bits are cleared on read as per register bit description.

PLOPI

The path loss of pointer interrupt status (PLOPI) bit is an event indicator. PLOPI is set to logic 1 to indicate any change in the status of PLOPV (entry to the LOP_state or exit from the LOP_state). The interrupt status bit is independent of the interrupt enable bit. PLOPI is cleared to logic 0 when this register is read. NOTE: This register bit should normally be ignored when the RHPP is configured as a slave.

PLOPCI[1:12]

The path loss of pointer concatenation interrupt status (PLOPCI[1:12]) register bits are event indicator. PLOPCI[n] is set to logic 1 to indicate any change in the status of PLOPCV[n] (entry to the LOPC_state or exit from the LOPC_state for the path n). The interrupt status bit is independent of the interrupt enable bit. PLOPCI[1:12] is cleared to logic 0 when this register is read.

Downloaded by Conexant Team (Conexant Inc.) on Wednesday, 07 February, 2007 06:59:32 PM

Register 0n8EH: RHPP Error Monitor Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R	PREIEI	X
Bit 8	R	PBIPEI	X
Bit 7	R	COPERDII	X
Bit 6	R	PERDII	X
Bit 5	R	PRDII	X
Bit 4	R	PPDII	X
Bit 3	R	PUNEQI	X
Bit 2	R	PPLMI	X
Bit 1	R	PPLUI	X
Bit 0	R	COPSLI	X

The RHPP Error Monitor Interrupt Status Register provides path alarm interrupt status for the STS-12c/STM-4c payload processed by RHPP. These register bits should normally be ignored when the RHPP is configured as a slave unless indicated otherwise. If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, these interrupt status bits are cleared on write with a logic 1. Otherwise, these interrupt status bits are cleared on read as per register bit description.

COPSLI

The change of path payload signal label interrupt status (COPSLI) bit is an event indicator. COPSLI is set to logic 1 to indicate a new PSL-P value. The interrupt status bit is independent of the interrupt enable bit. COPSLI is cleared to logic 0 when this register is read. ALGO2 register bit has no effect on COPSLI.

PPLUI

The path payload label unstable interrupt status (PPLUI) bit is an event indicator. PPLUI is set to logic 1 to indicate any change in the status of PPLUV (stable to unstable or unstable to stable). The interrupt status bit is independent of the interrupt enable bit. PPLUI is cleared to logic 0 when this register is read.

Downloaded by Conti Team for Jiminer Inc. on Wednesday, 07 February, 2007 06:59:32 PM

PPLMI

The path payload label mismatch interrupt status (PPLMI) bit is an event indicator. PPLMI is set to logic 1 to indicate any change in the status of PPLMV (match to mismatch or mismatch to match). The interrupt status bit is independent of the interrupt enable bit. PPLMI is cleared to logic 0 when this register is read.

PUNEQI

The path payload unequipped interrupt status (PUNEQI) bit is an event indicator. PUNEQI is set to logic 1 to indicate any change in the status of PUNEQV (equipped to unequipped or unequipped to equipped). The interrupt status bit is independent of the interrupt enable bit. PUNEQI is cleared to logic 0 when this register is read.

PPDII

The path payload defect indication interrupt status (PPDII) bit is an event indicator. PPDII is set to logic 1 to indicate any change in the status of PPDIV (no defect to payload defect or payload defect to no defect). The interrupt status bit is independent of the interrupt enable bit. PPDII is cleared to logic 0 when this register is read.

PRDII

The path remote defect indication interrupt status (PRDII) bit is an event indicator. PRDII is set to logic 1 to indicate any change in the status of PRDIV (no defect to RDI defect or RDI defect to no defect). The interrupt status bit is independent of the interrupt enable bit. PRDII is cleared to logic 0 when this register is read.

PERDII

The path enhanced remote defect indication interrupt status (PERDII) bit is an event indicator. PERDII is set to logic 1 to indicate any change in the status of PERDIV (no defect to ERDI defect or ERDI defect to no defect). The interrupt status bit is independent of the interrupt enable bit. PERDII is cleared to logic 0 when this register is read.

COPERDII

The change of path enhanced remote defect indication interrupt status (COPERDII) bit is an event indicator. COPERDII is set to logic 1 to indicate a new ERDI-P value. The interrupt status bit is independent of the interrupt enable bit. COPERDII is cleared to logic 0 when this register is read.

Downloaded by Content Team (Datasheet Miner Inc) on Wednesday, 07 February 2007 06:59:02 PM

PBIPEI

The path BIP-8 error interrupt status (PBIPEI) bit is an event indicator. PBIPEI is set to logic 1 to indicate a path BIP-8 error. The interrupt status bit is independent of the interrupt enable bit. PBIPEI is cleared to logic 0 when this register is read.

PREIEI

The path REI error interrupt status (PREIEI) bit is an event indicator. PREIEI is set to logic 1 to indicate a path REI error. The interrupt status bit is independent of the interrupt enable bit. PREIEI is cleared to logic 0 when this register is read.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 AM

12.8 Receive SONET/SDH Virtual Container Aligner (SVCA #1 - #16)

There are 16 SVCA (#1 - #16) blocks in 16 STM-4 processing slices with independent register sets. When the S/UNI 9953 is configured for quad OC-48 mode, SVCA #1, #5, #9, #13 are configured as masters and the remaining SVCA blocks are configured as slaves. When configured for OC-192 mode, only SVCA #1 is configured as master and the remaining blocks are configured as slaves.

Register 0n90H: SVCA Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

The SVCA Indirect Address Register together with the SVCA Indirect Data Register are provided by SVCA for configuration and status retrieval for individual STS-1/STM-0 paths within the STS-12c/STM-4c data stream processed by SVCA. Only the STS-1/STM-0 path #1 should be used for S/UNI 9953 operation when the SVCA is configured as a master. These register bits should normally be set low when the SVCA is configured as a slave unless indicated otherwise.

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

Downloaded by Content Team (CT) - Printed on Wednesday, 07 February, 2007 06:55:07 PM

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer. Some indirect registers are valid only when the PATH[3:0] have certain values. Only the STS-1/STM-0 path #1 should be used for S/UNI 9953 operation when the SVCA is configured as a master.

PATH[3:0]	STS-1/STM-0 Path #
0000	Invalid path
0001-1100	Path #1 to Path #12
1101-1111	Invalid path

IADDR[2:0]

The address location (ADDR[2:0]) bits select which address location is accessed by the current indirect transfer.

IADDR[2:0]	Indirect Register
000	SVCA Outgoing Positive Justification Performance Monitor
001	SVCA Outgoing Negative Justification Performance Monitor
010	SVCA Diagnostic/Configuration Register
011	AU-4 pointer
100	Unused
101	Unused
110 to 111	unused

Downloaded by Content Team of Parts Group, Wednesday, 07 February 2007 06:58:32 PM

Register 0n91H: SVCA Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

The SVCA Indirect Data Register together with the SVCA Indirect Address Register are provided by SVCA for configuration and status retrieval for individual STS-1/STM-0 paths within the STS-12c/STM-4c data stream processed by SVCA.

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The SVCA Indirect Data register must contain valid data before the indirect write is initiated by writing to the SVCA Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Downloaded by Content Delivery Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0n91H (Indirect Register 00H): SVCA Positive Justifications Performance Monitor

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	R	PJPMON[12]	0
Bit 11	R	PJPMON[11]	0
Bit 10	R	PJPMON[10]	0
Bit 9	R	PJPMON[9]	0
Bit 8	R	PJPMON[8]	0
Bit 7	R	PJPMON[7]	0
Bit 6	R	PJPMON[6]	0
Bit 5	R	PJPMON[5]	0
Bit 4	R	PJPMON[4]	0
Bit 3	R	PJPMON[3]	0
Bit 2	R	PJPMON[2]	0
Bit 1	R	PJPMON[1]	0
Bit 0	R	PJPMON[0]	0

The outgoing Positive Justifications Performance Monitor Register is provided at SVCA indirect r/w address 00H. Only the STS-1/STM-0 path #1 should be monitored for S/UNI 9953 operation when the SVCA is configured as a master.

PJPMON[12:0]

This register reports the number of positive pointer justification events that occurred on the outgoing side in the previous accumulation interval. The performance monitor register content is updated by a microprocessor write to the S/UNI 9953 Identity, and Global Performance Monitor Update register (Register 0000H). The TIP register bit indicates the update status. The value of PJPMON is only valid for master slices. If PJPMON[12:0] is read for a slave slice, the master path's value will be returned.

Downloaded by Content Team for Printer Inc on Thursday, 07 February, 2007 06:59:32 PM

Register 0n91H (Indirect Register 01H): SVCA Negative Justifications Performance Monitor

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	R	NJPMON[12]	0
Bit 11	R	NJPMON[11]	0
Bit 10	R	NJPMON[10]	0
Bit 9	R	NJPMON[9]	0
Bit 8	R	NJPMON[8]	0
Bit 7	R	NJPMON[7]	0
Bit 6	R	NJPMON[6]	0
Bit 5	R	NJPMON[5]	0
Bit 4	R	NJPMON[4]	0
Bit 3	R	NJPMON[3]	0
Bit 2	R	NJPMON[2]	0
Bit 1	R	NJPMON[1]	0
Bit 0	R	NJPMON[0]	0

The outgoing Negative Justifications Performance Monitor Register is provided at SVCA indirect r/w address 01H. Only the STS-1/STM-0 path #1 should be monitored for S/UNI 9953 operation when the SVCA is configured as a master.

NJPMON[12:0]

This register reports the number of negative pointer justification events that occurred on the outgoing side in the previous accumulation interval. The performance monitor register content is updated by a microprocessor write to the S/UNI 9953 Identity, and Global Performance Monitor Update register (Register 0000H). The TIP register bit indicates the update status. The value of NJPMON is only valid for master slices. If NJPMON[12:0] is read for a slave slice, the master path's value will be returned.

Downloaded by Content Team for Printer Inc on Thursday, 07 February, 2007 06:59:32 PM

Register 0n91H (Indirect Register 02H): SVCA Diagnostic/Configuration

Bit	Type	Function	Default
Bit 15	R/W	PTRRST	0
Bit 14	R/W	PTRSS[1]	0
Bit 13	R/W	PTRSS[0]	0
Bit 12	R/W	JUS3DIS	0
Bit 11	R/W	PTRDD[1]	0
Bit 10	R/W	PTRDD[0]	0
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	Diag_NDFREQ	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Diag_PAIS	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

The SVCA Diagnostic/Configuration Register is provided at SVCA r/w address 02H. The diagnostic related register bits should be set to their default values during normal operation of the SVCA. The Diagnostic/Config register is only valid for master paths. Slave path Diagnostic/Config registers are overwritten with the master path's Diagnostic/Config register value.

Diag_PAIS

When set high, the Diag_PAIS bit forces the SVCA to insert path AIS in the selected outgoing stream for at least three consecutive frames. AIS is inserted by writing an all ones pattern in the transport overhead bytes H1, H2, and H3, as well as in the entire STS synchronous payload envelope. The first frame after PAIS negates will contain a new data flag in the transport overhead H1 byte.

Diag_NDFREQ

When set high, Diag_NDFREQ bit forces the SVCA to insert a NEW DATA FLAG indication in the frame regardless of the state of the pointer generation state machine.

PTRDD[1:0]

The PTRDD[1:0] defines the STS-N/AU-N concatenation pointer bits DD. ITU requires that DD be set to 10 when processing AU data streams. On the other side, TELCORDIA does not specify these two bits.

Downloaded by Conexant Team at Gartner Inc on Wednesday, 07 February, 2007 06:59:32 PM

JUST3DIS

When set high, JUST3DIS allows the SVCA to perform 1 justification per frame when necessary. When set to zero, pointer justifications are allowed only every 4 frames.

PTRSS[1:0]

The PTRSS[1:0] defines the STS-N/AU-N pointer bits SS. ITU requires that SS be set to 10 when processing AU-N data streams. On the other side, TELCORDIA does not specify these two bits. The ss bits are set to 00 when processing a slave STS-1/STM-0 path.

PTR_RST

When set high, Incoming and outgoing pointers are reset to their default values. This bit is level sensitive.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0n91H (Indirect Register 03H): SVCA AU-4 Pointer

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R/W	AU4PTR[9]	0
Bit 8	R/W	AU4PTR[8]	0
Bit 7	R/W	AU4PTR[7]	0
Bit 6	R/W	AU4PTR[6]	0
Bit 5	R/W	AU4PTR[5]	0
Bit 4	R/W	AU4PTR[4]	0
Bit 3	R/W	AU4PTR[3]	0
Bit 2	R/W	AU4PTR[2]	0
Bit 1	R/W	AU4PTR[1]	0
Bit 0	R/W	AU4PTR[0]	0

The AU-4 Pointer Register is provided at SVCA indirect r/w address 03H. Only the STS-1/STM-0 path #1 should be used for S/UNI 9953 operation when the SVCA is configured as a master.

AU4PTR[9:0]

This register holds the AU pointer of the STS-12c/STM-4c payload processed by the SVCA as a master.

Downloaded by Content Team of Partmine Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0n92H: SVCA Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved10	0
Bit 14	R/W	Reserved9	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved8	0
Bit 6	R/W	Reserved7	0
Bit 5	R/W	Reserved6	0
Bit 4	R/W	Reserved5	0
Bit 3	R/W	Reserved4	0
Bit 2	R/W	Reserved3	0
Bit 1	R/W	Reserved2	0
Bit 0	R/W	Reserved1	0

The SVCA Payload Configuration Register is provided for payload configuration not required by S/UNI 9953.

Reserved [10:1]

The Reserved bits must be set to the logic states as indicated for proper operation of the S/UNI 9953.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0n93H: SVCA Positive Pointer Justification Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R	PPJI	X

The SVCA Positive Pointer Justification Interrupt Status Register provides the corresponding interrupt status of the STS-12c/STM-4c payload processed by the SVCA. This register bit should normally be ignored when the SVCA is configured as a slave.

PPJI

The positive pointer justification interrupt status (PPJI) bit is an event indicator for STS-12c/STM-4c payload. PPJI is set to logic 1 to indicate a positive pointer justification event in the payload stream. This interrupt status bit is independent of the corresponding interrupt enable bit. If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, this interrupt status bit is cleared to logic 0 on write to this register. Otherwise, this interrupt status bit is cleared on read.

Note that this interrupt status will cause a block level interrupt if the PJIE enable bit in register 0x0097 is set to logic 1.

Downloaded by Content Team of Newark Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0n94H: SVCA Negative Pointer Justification Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R	NPJI	X

The SVCA Negative Pointer Justification Interrupt Status Register provides the corresponding interrupt status of the STS-12c/STM-4c payload processed by the SVCA. This register bit should normally be ignored when the SVCA is configured as a slave.

NPJI

The negative pointer justification interrupt status (NPJI) bit is an event indicator for STS-12c/STM-4c payload. NPJI is set to logic 1 to indicate a negative pointer justification event in the payload stream. This interrupt status bit is independent of the corresponding interrupt enable bit. If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, this interrupt status bit is cleared to logic 0 on write to this register. Otherwise, this interrupt status bit is cleared on read.

Note that this interrupt status will cause a block level interrupt if the PJIE enable bit in register 0x0097 is set to logic 1.

Downloaded by Content Team of Newark Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0n95H: SVCA FIFO Overflow Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R	FOVRI	X

The SVCA FIFO overflow Event Interrupt Status Register provides the corresponding interrupt status of the STS-12c/STM-4c payload processed by the SVCA. This register bit should normally be ignored when the SVCA is configured as a slave.

FOVRI

The FIFO overflow event interrupt status (FOVRI) bit is an event indicator for STS-12c/STM-4c payload. FOVRI is set to logic 1 to indicate a FIFO overflow event. This interrupt status bit is independent of the corresponding interrupt enable bit. If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, this interrupt status bit is cleared to logic 0 on write to this register. Otherwise, this interrupt status bit is cleared on read.

Downloaded by Content Team of Chip One Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0n96H: SVCA FIFO Underflow Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R	FUDRI	X

The SVCA FIFO underflow Event Interrupt Status Register provides the corresponding interrupt status of the STS-12c/STM-4c payload processed by the SVCA. This register bit should normally be ignored when the SVCA is configured as a slave.

FUDRI

The FIFO underflow event interrupt status (FUDRI) bit is an event indicator for STS-12c/STM-4c payload. FUDRI is set to logic 1 to indicate a FIFO underflow event. This interrupt status bit is independent of the corresponding interrupt enable bit. If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, this interrupt status bit is cleared to logic 0 on write to this register. Otherwise, this interrupt status bit is cleared on read.

Downloaded by Content Team of Chip One Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0n97H: SVCA Pointer Justification Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	Reserved11	0
Bit 10	R/W	Reserved10	0
Bit 9	R/W	Reserved9	0
Bit 8	R/W	Reserved8	0
Bit 7	R/W	Reserved7	0
Bit 6	R/W	Reserved6	0
Bit 5	R/W	Reserved5	0
Bit 4	R/W	Reserved4	0
Bit 3	R/W	Reserved3	0
Bit 2	R/W	Reserved2	0
Bit 1	R/W	Reserved1	0
Bit 0	R/W	PJIE	0

The SVCA Pointer Justification Interrupt Enable Register is provided for configuring the corresponding STS-12c/STM-4c payload status reporting via device interrupt output. This register bit should normally be set low when the SVCA is configured as a slave.

PJIE

The pointer justification event interrupt enable (PJIE) bit controls the activation of the interrupt (INTB) output for the STS-12c/STM-4c payload. When PJIE is set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When PJIE is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

Note that the corresponding pending interrupt status for this enable is either PPJI or NPJI, as defined in registers 0x0093 and 0x0094 respectively.

Reserved [11:1]

The Reserved bits must be set to the logic states as indicated for proper operation of the S/UNI 9953.

Downloaded by Control Team (Pacific) Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0n98H: SVCA FIFO Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	Reserved11	0
Bit 10	R/W	Reserved10	0
Bit 9	R/W	Reserved9	0
Bit 8	R/W	Reserved8	0
Bit 7	R/W	Reserved7	0
Bit 6	R/W	Reserved6	0
Bit 5	R/W	Reserved5	0
Bit 4	R/W	Reserved4	0
Bit 3	R/W	Reserved3	0
Bit 2	R/W	Reserved2	0
Bit 1	R/W	Reserved1	0
Bit 0	R/W	FIE	0

The SVCA FIFO Event Interrupt Enable Register is provided for configuring the corresponding STS-12c/STM-4c payload status reporting via device interrupt output. This register bit should normally be set low when the SVCA is configured as a slave.

FIE

The FIFO event interrupt enable (FIE) bit controls the activation of the interrupt (INTB) output for the STS-12c/STM-4c payload caused by a FIFO overflow or a FIFO underflow. When FIE is set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When FIE is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

Reserved [11:1]

The Reserved bits must be set to the logic states as indicated for proper operation of the S/UNI 9953.

Downloaded by Content Agent of PMC-Sierra, Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0n99H: SVCA Pointer Justification Thresholds

Bit	Type	Function	Default
Bit 15	R/W	NTHRES[3]	0
Bit 14	R/W	NTHRES[2]	1
Bit 13	R/W	NTHRES[1]	1
Bit 12	R/W	NTHRES[0]	1
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	PTHRES[3]	0
Bit 2	R/W	PTHRES[2]	1
Bit 1	R/W	PTHRES[1]	1
Bit 0	R/W	PTHRES[0]	1

The SVCA Pointer Justification Thresholds Register is provided for pointer justification control of the receive stream.

PTHRES[3:0]

The SVCA positive pointer justification threshold determines the FIFO fill thresholds that triggers a positive pointer justification is requested. If the FIFO fill level is less than the PTHRES, than a positive justification is performed.

NTHRES[3:0]

The SVCA positive pointer justification threshold determines the FIFO fill thresholds that triggers a negative pointer justification is requested. If the FIFO fill level is greater than the NTHRES, than a negative justification is performed.

Downloaded by Content Team Partmic Inc on Wednesday, 07 February, 2007 06:59:32 PM

12.9 Receive 8B/10B TelecomBus Decoder (R8TD #1 - #16)

There are 16 R8TD (#1 - #16) blocks in 16 STM-4 processing slices with independent register sets.

Register 0nA0H: R8TD APS Control and Status

Bit	Type	Function	Default
Bit 15	R/W	DLBEN	0
Bit 14	R/W	Reserved	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R/W	PININV	0
Bit 8	R/W	OFAAIS	0
Bit 7	R/W	FUOE	0
Bit 6	R/W	LCVE	0
Bit 5	R/W	OFAE	0
Bit 4	R/W	OCAE	0
Bit 3	R	OFAV	X
Bit 2	R	OCAV	X
Bit 1	R/W	FOFA	0
Bit 0	R/W	FOCA	0

FOCA

The force out-of-character-alignment bit (FOCA) controls the operation of the character alignment circuit on a serial link. A transition from logic zero to logic one in this bit forces the receiver to the out-of-character-alignment state where it will search for the transport frame alignment character (K28.5). This bit must be manually set to logic zero before it can be used again.

FOFA

The force out-of-frame-alignment bit (FOFA) controls the operation of the frame alignment circuit. A transition from logic zero to logic one in this bit forces the receiver to the out-of-frame-alignment state where it will search for the transport frame alignment character (K28.5). This bit must be manually set to logic zero before it can be used again.

Downloaded by Content Team of Datasheet Inc. on Wednesday, 07 February, 2007 06:59:32 PM

OCAV

The out-of-character-alignment status bit (OCAV) reports the state of the character alignment circuit. OCAV is set high when the receiver is in the out-of-character-alignment state. OCAV is set low when the receiver is in the in-character-alignment state.

OFAV

The out-of-frame-alignment status bit (OFAV) reports the state of the frame alignment circuit. OFAV is set high when the receiver is in the out-of-frame-alignment state. OFAV is set low when the receiver is in the in-frame-alignment state.

OCAE

The out-of-character-alignment interrupt enable bit (OCAE) controls the change of character alignment state interrupts. Interrupts may be generated when the character alignment circuit changes state to the out-of-character-alignment state or to the in-character-alignment state. When OCAE is set high, an interrupt is generated when a change of state occurs. Interrupts due to changes of character alignment state are masked when OCAE is set low.

OFAE

The out-of-frame-alignment interrupt enable bit (OFAE) controls the change of frame alignment state interrupts. Interrupts may be generated when the frame alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. When OFAE is set high, an interrupt is generated when a change of state occurs. Interrupts due to changes of frame alignment state are masked when OFAE is set low.

LCVE

The line code violation interrupt enable bit (LCVE) controls the line code violation event interrupts. Interrupts may be generated when a line code violation is detected. When LCVE is set high, an interrupt is generated when an LCV is detected. Interrupts due to LCVs are masked when LCVE is set low.

FUOE

The FIFO underrun/overrun status interrupt enable (FUOE) controls the underrun/overrun event interrupts. Interrupts may be generated when the underrun/overrun event is detected. When FUOE is set high, an interrupt is generated when a FIFO underrun or overrun condition is detected. Interrupts due to FIFO underrun of overrun conditions are masked when FUEO is set low.

Downloaded by Content Team - Partminer on Wednesday, 07 February, 2007 06:59:32 PM

OFAAIS

The out of frame alignment alarm indication signal (OFAAIS) is set high to force high-order AIS signals in the R8TD egress data stream if the R8TD is in the out-of-frame-alignment state. The R8TD egress data stream is left unaffected in the out-of-frame alignment state when the OFFAIS is set low.

PININV

The parallel incoming data invert bit (PININV) controls the active polarity of the incoming data stream. When PININV is set high, the incoming data stream is complemented before further processing by the R8TD. When PININV is set low, the incoming data stream is not complemented.

DLBEN

The APS port Diagnostic Loop-back Enable (DLBEN) bit controls the parallel loop-back from output APS port to input APS port. When DLBEN is set to logic 1, the output APS data stream from the correspondingT8TE block is loop-backed to the input of the R8TD block. When DLBEN is set to logic 0, the APS input/output ports operate normally.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 06:59:38 AM

Register 0nA1H: R8TD APS Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	FUOI	X
Bit 6	R	LCVI	X
Bit 5	R	OFAI	X
Bit 4	R	OCAI	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, these interrupt status bits are cleared on write with a logic 1. Otherwise, these interrupt status bits are cleared on read.

OCAI

The out-of-character-alignment interrupt status bit (OCAI) reports and acknowledges change of character alignment state interrupts. Interrupts are generated when the character alignment block changes state to the out-of-character-alignment state or to the in-character-alignment state. OCAI is set high when change of state occurs. When the interrupt is masked by the OCAE bit the OCAI remains valid and may be polled to detect change of frame alignment events.

OFAI

The out-of-frame-alignment interrupt status bit (OFAI) reports and acknowledges change of frame alignment state interrupts. Interrupts are generated when the frame alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. OFAI is set high when change of state occurs. When the interrupt is masked by the OFAE bit the OFAI remains valid and may be polled to detect change of frame alignment events.

Downloaded by Content Team on Excelint Inc on Wednesday, 07 February, 2007 06:09:32 PM

LCVI

The line code violation event interrupt status bit (LCVI) reports and acknowledges line code violation interrupts. Interrupts are generated when the character alignment block detects a line code violation in the incoming data stream. LCVI is set high when a line code violation event is detected. When the interrupt is masked by the LCVE bit the LCVI remains valid and may be polled to detect change of frame alignment events.

FUOI

The FIFO underrun/overrun event interrupt status bit (FUOI) reports and acknowledges the FIFO underrun/overrun interrupts. Interrupts are generated when the character alignment block detects that the read and write pointers are within one of each other. FUOI is set high when this event is detected. When the interrupt is masked by the FUOE bit the FUOI remains valid and may be polled to detect underrun/overrun events.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 08:58:22 AM

Register 0nA2H: R8TD APS Line Code Violation Count

Bit	Type	Function	Default
Bit 15	R	LCV[15]	X
Bit 14	R	LCV[14]	X
Bit 13	R	LCV[13]	X
Bit 12	R	LCV[12]	X
Bit 11	R	LCV[11]	X
Bit 10	R	LCV[10]	X
Bit 9	R	LCV[9]	X
Bit 8	R	LCV[8]	X
Bit 7	R	LCV[7]	X
Bit 6	R	LCV[6]	X
Bit 5	R	LCV[5]	X
Bit 4	R	LCV[4]	X
Bit 3	R	LCV[3]	X
Bit 2	R	LCV[2]	X
Bit 1	R	LCV[1]	X
Bit 0	R	LCV[0]	X

LCV[15:0]

The LCV[15:0] bits report the number of line code violations that have been detected since the last time the LCV registers were polled. The LCV registers are polled by writing to this register or to register 0000H, the S/UNI 9953 Identity and Global Performance Monitor Update. This action transfers the internally accumulated error count to the LCV registers within 6 TCLK cycles and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Downloaded by Content Team of Partminer on Wednesday, 07 February, 2007 06:09:32 PM

Register 0nA3H: R8TD APS Analog Control 1

Bit	Type	Function	Default
Bit 15	R/W	Reserved	1
Bit 14	R/W	Reserved	1
Bit 13	R/W	DRU_ENB	0
Bit 12	R/W	RX_ENB	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	A_RSTB	1
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	DRU_CTRL[3]	0
Bit 4	R/W	DRU_CTRL[2]	0
Bit 3	R/W	DRU_CTRL[1]	0
Bit 2	R/W	DRU_CTRL[0]	0
Bit 1	R/W	Reserved	0
Bit 0	—	Unused	X

This register controls internal analog functions.

DRU_CTRL[3:0]

The DRU_CTRL[3:0] bits control the DRU CTRL[3:0] inputs.

The DRU_CTRL[3:0] bus must be set to “1101” for correct operation of the APS port.

A_RSTB

The A_RSTB bit is a soft-reset for the Data Recovery Unit Analog block. Setting A_RSTB to logic 0 will reset the block.

RX_ENB

The RXLV enable bit (RX_ENB) bit controls the operation of RXLV block #X. Setting RX_ENB to logic 0 enables the block. Setting RX_ENB to logic 1 disables the block.

DRU_ENB

The DRU enable (DRU_ENB) bit controls the operation of Data Recovery Unit Analog block #X. Setting DRU_ENB to logic 0 enables the block. Setting DRU_ENB to logic 1 disables the block.

Downloaded by Content Team of Startmineo Inc on Wednesday, 07 February, 2007 06:09:32 PM

Register 0nA4H: R8TD APS Analog Control 2

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

This register controls internal analog functions. This register should not be used.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:09:32 PM

Register 0nA5H: R8TD APS Analog Control 3

Bit	Type	Function	Default
Bit 15	R/W	Reserved	X
Bit 14	R/W	Reserved	X
Bit 13	R/W	Reserved	X
Bit 12	R/W	Reserved	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 06:59:32 PM

12.10 SONET/SDH Alarm Reporting Controller (SARC #1 - #4)

There are 4 SARC (#1 - #4) blocks in 4 STM-16 processing groups with independent register sets. When the S/UNI 9953 is configured for quad OC-48 mode, all four blocks are configured as masters to process the STS-48c/STM-16c data streams. When configured for OC-192 mode, only SARC #1 is configured as master and the other three (#2 - #4) blocks are inactive and may be considered as slaves.

Register 0kB0H: SARC Section Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R/W	LRDI22	0
Bit 0	R/W	Reserved	0

The SARC Section Configuration Register is provided for configuring line RDI assertion in the transmit stream. These register bits should normally be set low when the SARC is configured as a slave unless indicated otherwise.

Reserved

The Reserved bit must be set to the logic state as indicated for proper operation of the S/UNI 9953.

LRDI22

The line remote defect indication (LRDI22) bit selects the line RDI persistence. When LRDI22 is set to logic 1, a new line RDI indication is transmitted for at least 20 frames. When LRDI22 is set to logic 0, a new line RDI indication is transmitted for at least 10 frames.

Downloaded by Content Team of Pacific Microchip Wednesday, 07 February, 2007 06:58:08PM

Register 0kB1H: SARC Section RSALM Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	SYNC_ERREN	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	SFBEREN	0
Bit 8	R/W	SDBEREN	0
Bit 7	R/W	STIMEN	0
Bit 6	R/W	STIUEN	0
Bit 5	R/W	APSBFEN	0
Bit 4	R/W	LRDIEN	0
Bit 3	R/W	LAISEN	0
Bit 2	R/W	LOSEN	0
Bit 1	R/W	LOFEN	0
Bit 0	R/W	OOFEN	0

The SARC Section RSALM Enable Register is provided for configuring the receive section/line alarm (RSALM) for the corresponding data stream. The state of the RSALM is provided on the corresponding SALM output. These register bits should normally be set low when the SARC is configured as a slave unless indicated otherwise.

OOFEN

The OOF enable bit allows the out of frame defect to be ORed into the RSALM. When the OOFEN bit is set high, the corresponding defect indication is ORed with other defect indications to the RSALM. When the OOFEN bit is set low, the corresponding defect indication does not affect the RSALM.

LOFEN

The LOF enable bit allows the loss of frame defect to be ORed into the RSALM. When the LOFEN bit is set high, the corresponding defect indication is ORed with other defect indications to the RSALM. When the LOFEN bit is set low, the corresponding defect indication does not affect the RSALM.

LOSEN

The LOS enable bit allows the loss of signal defect to be ORed into the RSALM. When the LOSEN bit is set high, the corresponding defect indication is ORed with other defect indications to the RSALM. When the LOSEN bit is set low, the corresponding defect indication does not affect the RSALM.

Downloaded by Conrad Team of Pioneer Inc on Wednesday, 07 February, 2007 06:59:32 PM

LAISEN

The LAIS enable bit allows the line alarm indication signal defect to be ORed into the RSALM. When the LAISEN bit is set high, the corresponding defect indication is ORed with other defect indications to the RSALM. When the LAISEN bit is set low, the corresponding defect indication does not affect the RSALM.

LRDIEN

The LRDI enable bit allows the line remote defect indication defect to be ORed into the RSALM. When the LRDIEN bit is set high, the corresponding defect indication is ORed with other defect indications to the RSALM. When the LRDIEN bit is set low, the corresponding defect indication does not affect the RSALM.

APSBFEN

The APSBF enable bit allows the APS byte failure defect to be ORed into the RSALM. When the APSBFEN bit is set high, the corresponding defect indication is ORed with other defect indications to the RSALM. When the APSBFEN bit is set low, the corresponding defect indication does not affect the RSALM.

STIUEN

The STIU enable bit allows the section trace identifier unstable defect to be ORed into the RSALM. When the STIUEN bit is set high, the corresponding defect indication is ORed with other defect indications to the RSALM. When the STIUEN bit is set low, the corresponding defect indication does not affect the RSALM.

STIMEN

The STIM enable bit allows the section trace identifier mismatch defect to be ORed into the RSALM. When the STIMEN bit is set high, the corresponding defect indication is ORed with other defect indications to the RSALM. When the STIMEN bit is set low, the corresponding defect indication does not affect the RSALM.

SDBEREN

The SDBER enable bit allows the signal degrade BER defect to be ORed into the RSALM. When the SDBEREN bit is set high, the corresponding defect indication is ORed with other defect indications to the RSALM. When the SDBEREN bit is set low, the corresponding defect indication does not affect the RSALM.

Downloaded by Control Team Datasheet Online Wednesday, 07 February 2007 06:59:02 AM

SFBEREN

The SFBER enable bit allows the signal failure BER defect to be ORed into the RSALM. When the SFBEREN bit is set high, the corresponding defect indication is ORed with other defect indications to the RSALM. When the SFBEREN bit is set low, the corresponding defect indication does not affect the RSALM.

SYNC_ERREN

The SYNC_ERR enable bit allows the input SYNC_ERR alarm to be ORed into the RSALM. When the SYNC_ERREN bit is set high, the corresponding alarm indication is ORed with other defect indications to the RSALM. When the SYNC_ERREN bit is set low, the corresponding alarm indication does not affect the RSALM.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 06:59:32 AM

Register 0kB2H: SARC Section RLAISINS Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	SYNC_ERREN	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	SFBEREN	0
Bit 8	R/W	SDBEREN	0
Bit 7	R/W	STIMEN	0
Bit 6	R/W	STIUEN	0
Bit 5	R/W	APSBFEN	0
Bit 4	R/W	LRDIEN	0
Bit 3	R/W	LAISEN	0
Bit 2	R/W	LOSEN	0
Bit 1	R/W	LOFEN	0
Bit 0	R/W	OOFEN	0

The SARC Section RLAISINS Enable Register is provided for configuring line AIS assertion in the receive stream. When receive AIS-L is asserted, the corresponding RLAISINS alarm condition is asserted. These register bits should normally be set low when the SARC is configured as a slave unless indicated otherwise.

OOFEN

The OOF enable bit allows the out of frame defect to affect receive AIS-L assertion. When the OOFEN bit is set high, the corresponding defect indication asserts receive AIS-L. When the OOFEN bit is set low, the corresponding defect indication has no effect on the receive stream.

LOFEN

The LOF enable bit allows the loss of frame defect to affect receive AIS-L assertion. When the LOFEN bit is set high, the corresponding defect indication asserts receive AIS-L. When the LOFEN bit is set low, the corresponding defect indication has no effect on the receive stream.

LOSEN

The LOS enable bit allows the loss of signal defect to affect receive AIS-L assertion. When the LOSEN bit is set high, the corresponding defect indication asserts receive AIS-L. When the LOSEN bit is set low, the corresponding defect indication has no effect on the receive stream.

Downloaded by Content Team of Partsolver Inc on Wednesday, 07 February, 2007 06:59:32 PM

LAISEN

The LAIS enable bit allows the line alarm indication signal defect to affect receive AIS-L assertion. When the LAISEN bit is set high, the corresponding defect indication asserts receive AIS-L. When the LAISEN bit is set low, the corresponding defect indication has no effect on the receive stream.

LRDIEN

The LRDI enable bit allows the line remote defect indication defect to affect receive AIS-L assertion. When the LRDIEN bit is set high, the corresponding defect indication asserts receive AIS-L. When the LRDIEN bit is set low, the corresponding defect indication has no effect on the receive stream.

APSBFEN

The APSBF enable bit allows the APS byte failure defect to affect receive AIS-L assertion. When the APSBFEN bit is set high, the corresponding defect indication asserts receive AIS-L. When the APSBFEN bit is set low, the corresponding defect indication has no effect on the receive stream.

STIUEN

The STIU enable bit allows the section trace identifier unstable defect to affect receive AIS-L assertion. When the STIUEN bit is set high, the corresponding defect indication asserts receive AIS-L. When the STIUEN bit is set low, the corresponding defect indication has no effect on the receive stream.

STIMEN

The STIM enable bit allows the section trace identifier mismatch defect to affect receive AIS-L assertion. When the STIMEN bit is set high, the corresponding defect indication asserts receive AIS-L. When the STIMEN bit is set low, the corresponding defect indication has no effect on the receive stream.

SDBEREN

The SDBER enable bit allows the signal degrade BER defect to affect receive AIS-L assertion. When the SDBEREN bit is set high, the corresponding defect indication asserts receive AIS-L. When the SDBEREN bit is set low, the corresponding defect indication has no effect on the receive stream.

Downloaded by Conexant Team (Datasheet Miner Inc) on Wednesday, 07 February 2007 06:59:32 PM

SFBEREN

The SFBER enable bit allows the signal failure BER defect to affect receive AIS-L assertion. When the SFBEREN bit is set high, the corresponding defect indication asserts receive AIS-L. When the SFBEREN bit is set low, the corresponding defect indication has no effect on the receive stream.

SYNC_ERREN

The SYNC_ERR enable bit allows the input SYNC_ERR alarm to affect receive AIS-L assertion. When the SYNC_ERREN bit is set high, the corresponding alarm indication asserts receive AIS-L. When the SYNC_ERREN bit is set low, the corresponding alarm indication has no effect on the receive stream.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 06:59:02 PM

Register 0kB3H: SARC Section TLRDIINS Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	SYNC_ERREN	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	SFBEREN	0
Bit 8	R/W	SDBEREN	0
Bit 7	R/W	STIMEN	0
Bit 6	R/W	STIUEN	0
Bit 5	R/W	APSBFEN	0
Bit 4	R/W	LRDIEN	0
Bit 3	R/W	LAISEN	0
Bit 2	R/W	LOSEN	0
Bit 1	R/W	LOFEN	0
Bit 0	R/W	OOFEN	0

The SARC Section TLRDIINS Enable Register is provided for configuring line RDI assertion in the transmit stream as a consequence of receive alarms. These register bits should normally be set low when the SARC is configured as a slave unless indicated otherwise.

OOFEN

The OOF enable bit allows the out of frame defect to affect transmit RDI-L assertion. When the OOFEN bit is set high, the corresponding defect indication asserts transmit RDI-L. When the OOFEN bit is set low, the corresponding defect indication has no effect on the transmit stream.

LOFEN

The LOF enable bit allows the loss of frame defect to affect transmit RDI-L assertion. When the LOFEN bit is set high, the corresponding defect indication asserts transmit RDI-L. When the LOFEN bit is set low, the corresponding defect indication has no effect on the transmit stream.

LOSEN

The LOS enable bit allows the loss of signal defect to affect transmit RDI-L assertion. When the LOSEN bit is set high, the corresponding defect indication asserts transmit RDI-L. When the LOSEN bit is set low, the corresponding defect indication has no effect on the transmit stream.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

LAISEN

The LAIS enable bit allows the line alarm indication signal defect to affect transmit RDI-L assertion. When the LAISEN bit is set high, the corresponding defect indication asserts transmit RDI-L. When the LAISEN bit is set low, the corresponding defect indication has no effect on the transmit stream.

LRDIEN

The LRDI enable bit allows the line remote defect indication defect to affect transmit RDI-L assertion. When the LRDIEN bit is set high, the corresponding defect indication asserts transmit RDI-L. When the LRDIEN bit is set low, the corresponding defect indication has no effect on the transmit stream.

APSBFEN

The APSBF enable bit allows the APS byte failure defect to affect transmit RDI-L assertion. When the APSBFEN bit is set high, the corresponding defect indication asserts transmit RDI-L. When the APSBFEN bit is set low, the corresponding defect indication has no effect on the transmit stream.

STIUEN

The STIU enable bit allows the section trace identifier unstable defect to affect transmit RDI-L assertion. When the STIUEN bit is set high, the corresponding defect indication asserts transmit RDI-L. When the STIUEN bit is set low, the corresponding defect indication has no effect on the transmit stream.

STIMEN

The STIM enable bit allows the section trace identifier mismatch defect to affect transmit RDI-L assertion. When the STIMEN bit is set high, the corresponding defect indication asserts transmit RDI-L. When the STIMEN bit is set low, the corresponding defect indication has no effect on the transmit stream.

SDBEREN

The SDBER enable bit allows the signal degrade BER defect to affect transmit RDI-L assertion. When the SDBEREN bit is set high, the corresponding defect indication asserts transmit RDI-L. When the SDBEREN bit is set low, the corresponding defect indication has no effect on the transmit stream.

Downloaded by Conexant Team (Examiner) IC on Wednesday, 07 February 2007 06:59:32 PM

SFBEREN

The SFBER enable bit allows the signal failure BER defect to affect transmit RDI-L assertion. When the SFBEREN bit is set high, the corresponding defect indication asserts transmit RDI-L. When the SFBEREN bit is set low, the corresponding defect indication has no effect on the transmit stream.

SYNC_ERREN

The SYNC_ERR enable bit allows the input SYNC_ERR alarm to affect transmit RDI-L assertion. When the SYNC_ERREN bit is set high, the corresponding alarm indication asserts transmit RDI-L. When the SYNC_ERREN bit is set low, the corresponding alarm indication has no effect on the transmit stream.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 06:59:32 PM

Register 0kB4H: SARC Path Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	PRDIEN	0
Bit 6	R/W	PERDI22	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	PLOPTREND	0
Bit 3	R/W	PAISPTRCFG[1]	0
Bit 2	R/W	PAISPTRCFG[0]	0
Bit 1	R/W	PLOPTRCFG[1]	0
Bit 0	R/W	PLOPTRCFG[0]	0

The SARC Path Configuration Register is provided for configuring the receive path alarm detection and the consequent transmit path RDI/ERDI assertion. These register bits should normally be set low when the SARC is configured as a slave unless indicated otherwise.

PLOPTRCFG[1:0]

The path loss of pointer configuration (PLOPTRCFG[1:0]) bits define the LOP-P defect. When PLOPTRCFG[1:0] is set to 00b, an LOP-P defect is declared when the pointer is in the LOP state and an LOP-P defect is removed when the pointer is not in the LOP state. When PLOPTRCFG[1:0] is set to 01b, an LOP-P defect is declared when the pointer or any of the concatenated pointers is in the LOP state and an LOP-P defect is removed when the pointer and all the concatenation pointers are not in the LOP state. When PLOPTRCFG[1:0] is set to 10b, an LOP-P defect is declared when the pointer or any of the concatenated pointers is in the LOP state or in the AIS state and an LOP-P defect is removed when the pointer and all the concatenation pointers are not in the LOP state or in the AIS state.

Downloaded by Content Area Networks Inc on Monday, 07 February, 2007 06:59:32 PM

PAISPTRCFG[1:0]

The path AIS pointer configuration (PAISPTRCFG[1:0]) bits define the AIS-P defect. When PAISPTRCFG[1:0] is set to 00b, an AIS-P defect is declared when the pointer is in the AIS state and an AIS-P defect is removed when the pointer is not in the AIS state. When PAISPTRCFG[1:0] is set to 01b, an AIS-P defect is declared when the pointer or any of the concatenated pointers is in the AIS state and an AIS-P defect is removed when the pointer and all the concatenation pointers are not in the AIS state. When PAISPTRCFG[1:0] is set to 10b, an AIS-P defect is declared when the pointer and all the concatenated pointers are in the AIS state and an AIS-P defect is removed when the pointer or any of the concatenation pointers is not in the AIS state.

PLOPTREND

The path loss of pointer removal (PLOPTREND) bit controls the removal of a LOP-P defect when an AIS-P defect is declared. When PLOPTREND is set to logic 1, a LOP-P defect is terminated when an AIS-P defect is declared. When PLOPTREND is set to logic 0, a LOP-P defect is not terminated when an AIS-P defect is declared.

Reserved

The Reserved bit must be set to the logic state as indicated for proper operation of the S/UNI 9953.

PERDI22

The path enhance remote defect indication (PERDI22) bit selects the path ERDI persistence. When PERDI22 is set to logic 1, a new path ERDI indication is transmitted for at least 22 frames. When PERDI22 is set to logic 0, a new path ERDI indication is transmitted for at least 12 frames.

PRDIEN

The path remote defect indication enable (PRDIEN) bit selects between the 1 bit RDI code and the 3 bits ERDI code. When PRDIEN is set to logic 1, the 1 bit RDI code is transmitted. When PRDIEN is set to logic 0, the 3 bit ERDI code is transmitted.

Downloaded by Content Team of Partminer Inc on Wednesday, 01 February, 2017 @ 09:32:32 AM

Register 0kB5H: SARC Path RPALM Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R/W	LCDEN	0
Bit 12	R/W	PGROWTHEN	0
Bit 11	R/W	PTIMEN	0
Bit 10	R/W	PTIUEN	0
Bit 9	R/W	PERDIEN	0
Bit 8	R/W	PRDIEN	0
Bit 7	R/W	PPDIEN	0
Bit 6	R/W	PUNEQEN	0
Bit 5	R/W	PPLMEN	0
Bit 4	R/W	PPLUEN	0
Bit 3	R/W	PAISPTREN	0
Bit 2	R/W	PLOPTREN	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	RSALMEN	0

The SARC Path RPALM Enable Register is provided for configuring the receive path alarm (RPALM) for the corresponding data stream. The state of the RPALM is provided at the corresponding RALM output. These register bits should normally be set low when the SARC is configured as a slave unless indicated otherwise.

RSALMEN

The RSALM enable bit allows the receive section alarm to be ORed into the RPALM. When the RSALMEN bit is set high, the corresponding alarm indication is ORed with other defect indications to the RPALM. When the RSALMEN bit is set low, the corresponding alarm indication does not affect the RPALM.

Reserved

The Reserved bit must be set to the logic state as indicated for proper operation of the S/UNI 9953.

PLOPTREN

The PLOPTR enable bit allows the path loss of pointer defect to be ORed into the RPALM. When the PLOPTREN bit is set high, the corresponding defect indication is ORed with other defect indications to the RPALM. When the PLOPTREN bit is set low, the corresponding defect indication does not affect the RPALM.

Downloaded by Conexant Team of Pointer Inc on Wednesday, 07 February, 2007 06:59:32 PM

PAISPTREN

The PAISPTR enable bit allows the path AIS pointer defect to be ORed into the RPALM. When the PAISPTREN bit is set high, the corresponding defect indication is ORed with other defect indications to the RPALM. When the PAISPTREN bit is set low, the corresponding defect indication does not affect the RPALM.

PPLUEN

The PPLU enable bit allows the path payload label unstable defect to be ORed into the RPALM. When the PPLUEN bit is set high, the corresponding defect indication is ORed with other defect indications to the RPALM. When the PPLUEN bit is set low, the corresponding defect indication does not affect the RPALM.

PPLMEN

The PPLM enable bit allows the path payload label mismatch defect to be ORed into the RPALM. When the PPLMEN bit is set high, the corresponding defect indication is ORed with other defect indications to the RPALM. When the PPLMEN bit is set low, the corresponding defect indication does not affect the RPALM.

PUNEQEN

The PUNEQ enable bit allows the path unequipped defect to be ORed into the RPALM. When the PUNEQEN bit is set high, the corresponding defect indication is ORed with other defect indications to the RPALM. When the PUNEQEN bit is set low, the corresponding defect indication does not affect the RPALM.

PPDIEN

The PPDI enable bit allows the path payload defect indication defect to be ORed into the RPALM. When the PPDIEN bit is set high, the corresponding defect indication is ORed with other defect indications to the RPALM. When the PPDIEN bit is set low, the corresponding defect indication does not affect the RPALM.

PRDIEN

The PRDI enable bit allows the path remote defect indication defect to be ORed into the RPALM. When the PRDIEN bit is set high, the corresponding defect indication is ORed with other defect indications to the RPALM. When the PRDIEN bit is set low, the corresponding defect indication does not affect the RPALM.

Downloaded by Conrad Team Electronic Engineer Inc. on Wednesday, 07 February 2007 06:59:32 AM

PERDIEN

The PERDI enable bit allows the path enhanced remote defect indication defect to be ORed into the RPALM. When the PERDIEN bit is set high, the corresponding defect indication is ORed with other defect indications to the RPALM. When the PERDIEN bit is set low, the corresponding defect indication does not affect the RPALM.

PTIUEN

The PTIU enable bit allows the path trace identifier unstable defect to be ORed into the RPALM. When the PTIUEN bit is set high, the corresponding defect indication is ORed with other defect indications to the RPALM. When the PTIUEN bit is set low, the corresponding defect indication does not affect the RPALM.

PTIMEN

The PTIM enable bit allows the path trace identifier mismatch defect to be ORed into the RPALM. When the PTIMEN bit is set high, the corresponding defect indication is ORed with other defect indications to the RPALM. When the PTIMEN bit is set low, the corresponding defect indication does not affect the RPALM.

PGROWTHEN

The PGROWTH enable bit allows the growth defect to be ORed into the RPALM. When the PGROWTHEN bit is set high, the corresponding defect indication is ORed with other defect indications to the RPALM. When the PGROWTHEN bit is set low, the corresponding defect indication does not affect the RPALM.

LCDEN

The LCD enable bit allows the loss of cell delineation defect to be ORed into the RPALM. When the LCDEN bit is set high, the corresponding defect indication is ORed with other defect indications to the RPALM. When the LCDEN bit is set low, the corresponding defect indication does not affect the RPALM.

Downloaded by Content Team for Examiner Use on Wednesday, 07 February 2007 06:59:32 AM

Register 0kB6H: SARC Path RPAISINS Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R/W	Reserved	0
Bit 12	R/W	PGROWTHEN	0
Bit 11	R/W	PTIMEN	0
Bit 10	R/W	PTIUEN	0
Bit 9	R/W	PERDIEN	0
Bit 8	R/W	PRDIEN	0
Bit 7	R/W	PPDIEN	0
Bit 6	R/W	PUNEQEN	0
Bit 5	R/W	PPLMEN	0
Bit 4	R/W	PPLUEN	0
Bit 3	R/W	PAISPTREN	0
Bit 2	R/W	PLOPTREN	0
Bit 1	R/W	MSRLAISINSEN	0
Bit 0	R/W	RLAISINSEN	0

The SARC Path RPAISINS Enable Register is provided for configuring path AIS assertion in the receive stream. When receive AIS-P is asserted, the corresponding RPAISINS alarm condition is asserted. These register bits should normally be set low when the SARC is configured as a slave unless indicated otherwise.

RLAISINSEN

The RLAISINS enable bit allows the line AIS insertion indication to affect receive AIS-P assertion. When the RLAISINSEN bit is set high, the corresponding insertion indication (RLAISINS) asserts receive AIS-P. When the RLAISINSEN bit is set low, the corresponding insertion indication has no effect on the receive stream.

Reserved

The Reserved bit must be set to the logic state as indicated for proper operation of the S/UNI 9953.

MSRLAISINSEN

The master RLAISINS enable bit allows the master line AIS insertion indication to affect receive AIS-P assertion. When the MSRLAISINSEN bit is set high, the corresponding insertion indication asserts receive AIS-P. When the MSRLAISINSEN bit is set low, the corresponding insertion indication has no effect on the receive stream.

Downloaded by Content Team of Pericom Semiconductor Inc on Wednesday, 07 February, 2007 06:59:32 PM

PLOPTREN

The PLOPTR enable bit allows the path loss of pointer defect to affect receive AIS-P assertion. When the PLOPTREN bit is set high, the corresponding defect indication asserts receive AIS-P. When the PLOPTREN bit is set low, the corresponding defect indication has no effect on the receive stream.

PAISPTREN

The PAISPTR enable bit allows the path AIS pointer defect to affect receive AIS-P assertion. When the PAISPTREN bit is set high, the corresponding defect indication asserts receive AIS-P. When the PAISPTREN bit is set low, the corresponding defect indication has no effect on the receive stream.

PPLUEN

The PPLU enable bit allows the path payload label unstable defect to affect receive AIS-P assertion. When the PPLUEN bit is set high, the corresponding defect indication asserts receive AIS-P. When the PPLUEN bit is set low, the corresponding defect indication has no effect on the receive stream.

PPLMEN

The PPLM enable bit allows the path payload label mismatch defect to affect receive AIS-P assertion. When the PPLMEN bit is set high, the corresponding defect indication asserts receive AIS-P. When the PPLMEN bit is set low, the corresponding defect indication has no effect on the receive stream.

PUNEQEN

The PUNEQ enable bit allows the path unequipped defect to affect receive AIS-P assertion. When the PUNEQEN bit is set high, the corresponding defect indication asserts receive AIS-P. When the PUNEQEN bit is set low, the corresponding defect indication has no effect on the receive stream.

PPDIEN

The PPDI enable bit allows the path payload defect indication defect to affect receive AIS-P assertion. When the PPDIEN bit is set high, the corresponding defect indication asserts receive AIS-P. When the PPDIEN bit is set low, the corresponding defect indication has no effect on the receive stream.

Downloaded by Conexant Team at Examiner Inc. on Wednesday 07 February 2007 06:59:32 PM

PRDIEN

The PRDI enable bit allows the path remote defect indication defect to affect receive AIS-P assertion. When the PRDIEN bit is set high, the corresponding defect indication asserts receive AIS-P. When the PRDIEN bit is set low, the corresponding defect indication has no effect on the receive stream.

PERDIEN

The PERDI enable bit allows the path enhanced remote defect indication defect to affect receive AIS-P assertion. When the PERDIEN bit is set high, the corresponding defect indication asserts receive AIS-P. When the PERDIEN bit is set low, the corresponding defect indication has no effect on the receive stream.

PTIUEN

The PTIU enable bit allows the path trace identifier unstable defect to affect receive AIS-P assertion. When the PTIUEN bit is set high, the corresponding defect indication asserts receive AIS-P. When the PTIUEN bit is set low, the corresponding defect indication has no effect on the receive stream.

PTIMEN

The PTIM enable bit allows the path trace identifier mismatch defect to affect receive AIS-P assertion. When the PTIMEN bit is set high, the corresponding defect indication asserts receive AIS-P. When the PTIMEN bit is set low, the corresponding defect indication has no effect on the receive stream.

PGROWTHEN

The PGROWTH enable bit allows the growth defect to affect receive AIS-P assertion. When the PGROWTHEN bit is set high, the corresponding defect indication asserts receive AIS-P. When the PGROWTHEN bit is set low, the corresponding defect indication has no effect on the receive stream.

Downloaded by Content Team @ Datamine Inc. on Wednesday, 07 February 2007 06:59:32 PM

Register 0kB7H: SARC LOP and AIS Pointer Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R	PAISPTRV	X
Bit 0	R	PLOPTRV	X

The SARC LOP and AIS Pointer Status Register provides receive path alarm status as configured in the SARC Path Configuration Register. These register bits should normally be ignored when the SARC is configured as a slave unless indicated otherwise.

PLOPTRV

The path loss of pointer status (PLOPTRV) bit indicates the current status of the LOP-P defect for the corresponding receive stream. When PLOPTRCFG register bits are set to 00b, PLOPTRV is asserted when the pointer is in the LOP state and PLOPTRV is negated when the pointer is not in the LOP state. When PLOPTRCFG register bits are set to 01b, PLOPTRV is asserted when the pointer or any of the concatenated pointers is in the LOP state and PLOPTRV is negated when the pointer and all the concatenation pointers are not in the LOP state. When PLOPTRCFG register bits are set to 10b, PLOPTRV is asserted when the pointer or any of the concatenated pointers is in the LOP state or in the AIS state and PLOPTRV is negated when the pointer and all the concatenation pointers are not in the LOP state or in the AIS state. When the PLOPTREND register bit is set to one, PLOPTRV is negated when a AIS-P defect is detected.

Downloaded by Conterline Inc on Wednesday, 07 February, 2007 06:59:32 PM

PAISPTRV

The path AIS pointer status (PAISPTRV) bit indicates the current status of the AIS-P defect for the corresponding receive stream. When PAISPTRCFG register bits are set to 00b, PAISPTRV is asserted when the pointer is in the AIS state and PAISPTRV is negated when the pointer is not in the AIS state. When PAISPTRCFG register bits are set to 01b, PAISPTRV is asserted when the pointer or any of the concatenated pointers is in the AIS state and PAISPTRV is negated when the pointer and all the concatenation pointers are not in the AIS state. When PAISPTRCFG register bits are set to 10b, PAISPTRV is asserted when the pointer and all the concatenated pointers are in the AIS state and PAISPTRV is negated when the pointer or any of the concatenation pointers are not in the AIS state.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 05:05:32 PM

Register 0kB8H: SARC LOP and AIS Pointer Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R/W	PAISPTRE	0
Bit 0	R/W	PLOPTRE	0

The SARC LOP and AIS Pointer Interrupt Enable Register is provided for configuring the corresponding interrupt status reporting via device interrupt output. These register bits should normally be set low when the SARC is configured as a slave unless indicated otherwise.

PLOPTRE

The path loss of pointer interrupt enable (PLOPTRE) bit controls the activation of the interrupt (INTB) output. When this bit is set to logic 1, the pending interrupt will assert the interrupt (INTB) output. When this bit is set to logic 0, the pending interrupt will not assert the interrupt (INTB) output.

PAISPTRE

The path AIS signal pointer interrupt enable (PAISPTRE) bit controls the activation of the interrupt (INTB) output. When any of this bit location is set to logic 1, the pending interrupt will assert the interrupt (INTB) output. When this bit is set to logic 0, the pending interrupt will not assert the interrupt (INTB) output.

Downloaded by Content Agent of Parts-i-fy Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0kB9H: SARC LOP and AIS Pointer Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R	PAISPTRI	X
Bit 0	R	PLOPTRI	X

The SARC LOP and AIS Pointer Interrupt Status Register provides receive path alarm interrupt status as configured in the SARC Path Configuration Register. These register bits should normally be ignored when the SARC is configured as a slave unless indicated otherwise.

PLOPTRI

The path loss of pointer interrupt status (PLOPTRI) bit is an event indicator for the corresponding receive stream. PLOPTRI is set to logic 1 to indicate any changes in the status of PLOPTRV. This interrupt status bit is independent of the interrupt enable bit. If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, this interrupt status bit is cleared to logic 0 on write to this register. Otherwise, this interrupt status bit is cleared on read.

PAISPTRI

The path AIS pointer interrupt status (PAISPTRI) bit is an event indicator for the corresponding receive stream. PAISPTRI is set to logic 1 to indicate any changes in the status of PAISPTRV. This interrupt status bit is independent of the interrupt enable bit. If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, this interrupt status bit is cleared to logic 0 on write to this register. Otherwise, this interrupt status bit is cleared on read.

Downloaded by Conexant Team of Conexant, Inc on Wednesday, 07 February, 2007 06:59:32 PM

12.11 Receive Cell Frame Processor (RCFP #1 - #4)

There are 4 RCFP (#1 - #4) blocks in 4 STM-16 processing groups with independent register sets. When the S/UNI 9953 is configured for quad OC-48 mode, all four blocks are configured as masters to process the STS-48c/STM-16c data streams. When configured for OC-192 mode, all 4 RCFP (#1 - #4) blocks are inactive. When operating in OC-192 mode, please refer to the RCFP-9953 registers.

Register 0kC0H: RCFP Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	POS_SEL	0
Bit 9	R/W	INVERT	0
Bit 8	R/W	STRIP_SEL	0
Bit 7	R/W	DELINDIS	0
Bit 6	R/W	IDLEPASS	0
Bit 5	R/W	CRCPASS	0
Bit 4	R/W	CRC_SEL[1]	1
Bit 3	R/W	CRC_SEL[0]	1
Bit 2	R/W	RXOTYP	0
Bit 1	R/W	DESCRMBL	1
Bit 0	R/W	PROV	0

PROV

The processor provision bit (PROV) is used to enable the RCFP. When PROV is logic 0, the RCFP ATM and packet processors are disabled and will not transfer any valid data to the Receive FIFOs. When PROV is logic 1, the RCFP ATM or packet processor is enabled and will process data presented to it and transfer data to the Receive FIFOs.

Note that when provisioning in POS mode, an initial spurious POS packet may be transmitted from the RCFP FIFO.

DESCRMBL

The DESCRMBL bit controls the descrambling of the packet or ATM cell payload with the polynomial $x^{43} + 1$. When DESCRMBL is set to logic 0, frame or cell payload descrambling is disabled. When DESCRMBL is set to logic 1, payload descrambling is enabled.

Downloaded by Content Team by Dartmineer Ltd on Wednesday, 07 February, 2007 06:53:37 PM

RXOTYP

The RXOTYP bit determines if an alarm signal will stop a packet by simply asserting EOP, (RXOTYP set to logic 0), or by asserting EOP Abort, (RXOTYP set to logic 1). When RXOTYP is set to logic 0, premature termination of the packet will result in that packet failing a FCS check.

This bit is only valid when in POS mode. In ATM mode the RCFP will finish processing any cell in progress and then stop until the alarm signal is cleared.

CRC_SEL[1:0]

The CRC select (CRC_SEL[1:0]) bits control the CRC calculation according to the table below. For ATM cells, the CRC is calculated over the first four ATM header bytes. For packet applications, the CRC is calculated over the whole packet data, after byte destuffing and descrambling.

Table 19 Functionality of the CRC_SEL[1:0] Register Bits

CRC_SEL[1:0]	HCS Operation (ATM)	FCS Operation (POS)
00	Reserved	Reserved
01	Reserved	Reserved
10	CRC-8 without coset polynomial	CRC-CCITT (2 bytes)
11	CRC-8 with coset polynomial added	CRC-32 (4 bytes)

CRCPASS

The CRCPASS bit controls the dropping of cells and packets based on the detection of an incorrect CRC.

When in ATM mode and when CRCPASS is a logic 0, cells containing an uncorrectable HCS error are dropped and the HCS verification state machine transitions to the 'Detection Mode'.

When CRCPASS is logic 1, cells are passed to the receive FIFO regardless of errors detected in the HCS. Additionally, the HCS verification finite state machine never exits the SYNC state ('Correction Mode'), and hence will never lose cell delineation. Note that HCS errors are still counted

Note that ATM idle cells that contain HCS errors will cause the state machine to change state regardless of the setting of the IDLEPASS register bit.

When in POS mode and CRCPASS is logic 1, packets with FCS errors are not marked as such and are passed to the receive FIFO as if no FCS error occurred. When CRCPASS is logic 0, then packets with FCS errors are marked as EOP Abort words across the POS-PHY Level 4 interface.

Downloaded by Content Server of Pericom Inc on Wednesday 07 February, 2007 06:59:32 PM

Regardless of the programming of this bit, ATM cells are always dropped while the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states unless the DELINDIS bit in this register is set to logic 1.

IDLEPASS

The IDLEPASS bit controls the function of the ATM Idle Cell filter. It is only valid when in ATM mode. When IDLEPASS is written with logic 0, all cells that match the Idle Cell Header Pattern and Idle Cell Header Mask are filtered out. When IDLEPASS is logic 1, the Idle Cell Header Pattern and Mask register bits are ignored. The default state of this bit and the bits in the RCFP Idle Cell Header and Mask Register enable the dropping of Idle cells.

DELINDIS

When DELINDIS is set to logic 1, all payload data read by the RCFP is passed to the receive FIFO interface without the requirement of having to find cell delineation or packet delineation first.

In ATM mode the DELINDIS bit is used to disable all ATM cell filtering and ATM cell delineation. If cell alignment has been reached before DELINDIS is enabled, then the current cell alignment position is kept.

In POS mode the DELINDIS bit is used to disable the HDLC flag alignment, byte destuffing and flag removal. The data stream is arbitrarily segmented into 64 byte long packets. FCS and descrambling operations still follow how they have been set in their respective configuration registers.

STRIP_SEL

The frame check sequence stripping bit (STRIP_SEL) selects the CRC stripping mode of the RCFP. When STRIP_SEL is logic 1, CRC stripping is enabled. When STRIP_SEL is logic 0, CRC stripping is disabled. Note that CRC_SEL[1:0] must not equal "00", (no CRC) for stripping to be enabled. When stripping is enabled the received packet FCS or ATM cell HCS byte(s) are not passed to the receive FIFO. When STRIP is disabled the received packet FCS are transferred over the receive FIFO interface. When DELINDIS is enabled, packets and cells are not delineated therefore the value of STRIP_SEL is ignored. The STRIP_SEL bit must be set to logic 1 if working in ATM mode.

INVERT

The data inversion bit (INVERT) configures the processor to logically invert the incoming stream before processing it. When INVERT is set to logic 1, the stream is logically inverted before processing. When INVERT is set to logic 0, the stream is not inverted before processing.

Downloaded by Content Technologies Inc on Wednesday, 07 February, 2018 16:59:32 PM

POS_SEL

The Packet Over SONET (POS_SEL) bit selects the data type mode of the RCFP. When POS_SEL is logic 1, POS mode is selected. When POS_SEL is logic 0, ATM mode is selected.

Reserved

All Reserved bits must be set to their default values for proper operation.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0kC1H: RCFP Interrupt Enable and Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R	OCDV	X
Bit 8	R	LCDV	X
Bit 7	R/W	MINLE	0
Bit 6	R/W	MAXLE	0
Bit 5	R/W	ABRTE	0
Bit 4	R/W	XFERE	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	UCRCE	0
Bit 1	R/W	OCDE	0
Bit 0	R/W	LCDE	0

LCDE

The LCDE bit enables the generation of an interrupt due to a change in the ATM LCD state. When LCDE is set to logic 1, the interrupt is enabled.

OCDE

The OCDE bit enables the generation of an interrupt due to a change in ATM cell delineation state or packet Idle state. When OCDE is set to logic 1, the interrupt is enabled.

UCRCE

The UCRCE bit enables the generation of an interrupt due to the detection of an uncorrectable ATM HCS or packet FCS error. When UCRCE is set to logic 1, the interrupt is enabled.

Reserved

The Reserved bit should be set to logic 0 for proper operation.

Downloaded by Content Host of Partsminer Inc on Wednesday, 07 February, 2007 06:09:32 PM

XFERE

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the RCFP performance monitor counter holding registers. When XFERE is set to logic 1, the interrupt is enabled.

ABRTE

The Abort Packet Enable bit enables the generation of an interrupt due to the reception of an aborted packet. When ABRTE is set to logic 1, the interrupt is enabled.

MAXLE

The Maximum Length Packet Enable bit enables the generation of an interrupt due to the reception of a packet exceeding the programmable maximum packet length. When MAXLE is set to logic 1, the interrupt is enabled.

MINLE

The Minimum Length Packet Enable bit enables the generation of an interrupt due to the reception of a packet that is smaller than the programmable minimum packet length. When MINLE is set to logic 1, the interrupt is enabled.

LCDV

The LCDV bit gives the ATM Loss of Cell Delineation state. When LCDV is logic 1, an out of cell delineation (LCD) defect has persisted for the number of cells specified in the RCFP LCD Count Threshold register. When LCDV is logic 0, the RCFP has been in cell delineation for the number of cells specified in the RCFP LCD Count Threshold register. The cell time period can be varied by using the LCDC[10:0] register bits in the RCFP LCD Count Threshold register.

OCDV

The OCDV bit indicates the ATM cell delineation or packet out of frame alignment state. When OCDV is logic 1, the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states and is hunting for the cell boundaries or the packet processor is in out of frame alignment. When OCDV is logic 0, the cell delineation state machine is in the 'SYNC' state (either Correction or Detection mode) and cells are being written into the receive FIFO, or the packet processor is in frame alignment and frames are being written into the receive FIFO.

Downloaded by Conexion of Parsippany on Wednesday, 07 February, 2007 06:59:32 AM

Register 0kC2H: RCFP Interrupt Indication and Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	MINLI	X
Bit 6	R	MAXLI	X
Bit 5	R	ABRTI	X
Bit 4	R	XFERI	X
Bit 3	R	Reserved	X
Bit 2	R	UCRCI	X
Bit 1	R	OCDI	X
Bit 0	R	LCDI	X

If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, these interrupt status bits are cleared on a write of logic one. Otherwise, these interrupt status bits are cleared on read.

LCDI

The LCDI bit is set to logic 1 when there is a change in the loss of cell delineation (LCD) state. The current value of the LCD state is available through the LCDV bit in the RCFP Interrupt Enable and Status register.

OCDI

The OCDI bit is set to logic 1 when the RCFP enters or exits the SYNC state or the packet processor enters or exits the frame alignment state. The current value of the OCD state is available through the OCDV bit in the RCFP Interrupt Enable and Status register.

UCRCI

The UCRCI bit is set to logic 1 when an uncorrectable ATM HCS or packet FCS error is detected.

Reserved

This bit is not used.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:09:32 PM

XFERI

The XFERI bit indicates that a transfer of accumulated counter data has occurred. Logic 1 in this bit position indicates that the RCFP performance monitor counter holding registers have been updated. This update is initiated by writing to one of the RCFP counter register locations, or by writing to the S/UNI 9953 Identity, and Global Performance Monitor Update register.

ABRTI

The ABRTI bit indicates the generation of an interrupt due to the reception of an aborted packet.

MAXLI

The MAXLI bit indicates an interrupt due to the reception of a packet exceeding the programmable maximum packet length.

MINLI

The MINLI bit indicates an interrupt due to the reception of a packet that is smaller than the programmable minimum packet length.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:5[illegible] AM

Register 0kC3H: RCFP Minimum Packet Length

Bit	Type	Function	Default
Bit 15	R/W	MINPL[7]	0
Bit 14	R/W	MINPL[6]	0
Bit 13	R/W	MINPL[5]	0
Bit 12	R/W	MINPL[4]	0
Bit 11	R/W	MINPL[3]	0
Bit 10	R/W	MINPL[2]	1
Bit 9	R/W	MINPL[1]	0
Bit 8	R/W	MINPL[0]	0
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	RBY_MODE	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	0

Reserved

The Reserved bits should be set to their default values for proper operation.

RBY_MODE

The receive byte counter mode (RBY_MODE) bit is used to select the mode in which the RBY_IC[39:0] counters work. When RBY_MODE is logic 0, RBY_IC[39:0] will count all bytes in received packets (including FCS and Abort bytes) after the byte destuffing operation. When RBY_MODE is logic 1, RBY_IC[39:0] will count all bytes in received packets (including FCS, Abort, and stuff bytes) before the byte destuffing operation. Flag bytes will not be counted in either case. The RBY_MODE bit is only valid when working in POS mode.

Note: If byte counting is desired when DELINDIS=1, this bit must be set to a logic 1.

MINPL[7:0]

The Minimum Packet Length (MINPL[7:0]) bits are used to set the minimum packet length. Packets smaller than this length are marked with an error. The packet length used here is defined as the number of bytes encapsulated into the POS frame after destuffing but including the FCS. The default minimum packet length is 4 octets. Values smaller than 4 should not be used.

Downloaded by Content Team Solutions Partner Inc on Wednesday, 07 February, 2007 06:39:32 PM

Register 0kC4H: RCFP Maximum Packet Length

Bit	Type	Function	Default
Bit 15	R/W	MAXPL[16]	0
Bit 14	R/W	MAXPL[15]	0
Bit 13	R/W	MAXPL[14]	0
Bit 12	R/W	MAXPL[13]	0
Bit 11	R/W	MAXPL[12]	0
Bit 10	R/W	MAXPL[11]	0
Bit 9	R/W	MAXPL[10]	1
Bit 8	R/W	MAXPL[9]	1
Bit 7	R/W	MAXPL[8]	0
Bit 6	R/W	MAXPL[7]	0
Bit 5	R/W	MAXPL[6]	0
Bit 4	R/W	MAXPL[5]	0
Bit 3	R/W	MAXPL[4]	0
Bit 2	R/W	MAXPL[3]	0
Bit 1	R/W	MAXPL[2]	0
Bit 0	R/W	MAXPL[1]	0

MAXPL[16:1]

The Maximum Packet Length (MAXPL[16:0]) bits are used to set the maximum packet length. Only the top 16 bits of this 17 bit value are programmable. MAXPL[0] is automatically set to logic 0. Packets larger than this length are marked with an error. This Maximum Packet Length defaults to 1.5 Kbytes. The packet length used here is defined as the number of bytes encapsulated into the POS frame excluding byte stuffing but including the FCS. The default maximum packet length is 1536 octets.

MAXPL[16:0] should not be set higher than 0x1FFFA or lower than 0x00006 to guarantee correct behavior.

Downloaded by Content Team of Parmiter & Co. on Wednesday, 07 February, 2007 06:09:32 PM

Register 0kC5H: RCFP LCD Count Threshold

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	R/W	LCDC[10]	0
Bit 9	R/W	LCDC[9]	0
Bit 8	R/W	LCDC[8]	1
Bit 7	R/W	LCDC[7]	0
Bit 6	R/W	LCDC[6]	1
Bit 5	R/W	LCDC[5]	1
Bit 4	R/W	LCDC[4]	0
Bit 3	R/W	LCDC[3]	1
Bit 2	R/W	LCDC[2]	0
Bit 1	R/W	LCDC[1]	0
Bit 0	R/W	LCDC[0]	0

LCDC[10:0]

The LCDC[10:0] bits represent the number of consecutive cell periods the receive cell processor must be out of cell delineation before loss of cell delineation (LCD) is declared. Likewise, LCD is not removed until the receive cell processor is in cell delineation for the number of cell periods specified by LCDC[10:0].

The default value of LCD[10:0] is 360. For STS-48c, the average cell period is 176.9 ns and the default LCD integrate period is 63.8 μs.

Downloaded by Content Team of Partminer on Wednesday, 07 February, 2007 06:09:32 PM

Register 0kC6H: RCFP Idle Cell Header and Mask

Bit	Type	Function	Default
Bit 15	R/W	GFC[3]	0
Bit 14	R/W	GFC[2]	0
Bit 13	R/W	GFC[1]	0
Bit 12	R/W	GFC[0]	0
Bit 11	R/W	PTI[3]	0
Bit 10	R/W	PTI[2]	0
Bit 9	R/W	PTI[1]	0
Bit 8	R/W	CLP	1
Bit 7	R/W	MGFC[3]	1
Bit 6	R/W	MGFC[2]	1
Bit 5	R/W	MGFC[1]	1
Bit 4	R/W	MGFC[0]	1
Bit 3	R/W	MPTI[3]	1
Bit 2	R/W	MPTI[2]	1
Bit 1	R/W	MPTI[1]	1
Bit 0	R/W	MCLP	1

MCLP

The CLP bit contains the mask pattern for the eighth bit of the fourth octet of the 53-octet cell. This mask is applied to this register to select the bits included in the cell filter. Logic 1 in this bit position enables the CLP bit in the pattern register to be compared. Logic 0 causes the masking of the CLP bit. The default enables the register bit comparison.

MPTI[3:0]

The MPTI[3:0] bits contain the mask pattern for the fifth, sixth, and seventh bits of the fourth octet of the 53-octet cell. This mask is applied to the Idle Cell Header field to select the bits included in the cell filter. A logic 1 in any bit position enables the corresponding bit in the pattern register to be compared. A logic 0 causes the masking of the corresponding bit. The default enables the register bit comparison.

MGFC[3:0]

The MGFC[3:0] bits contain the mask pattern for the first, second, third, and fourth bits of the first octet of the 53-octet cell. This mask is applied to the Idle Cell Header field to select the bits included in the cell filter. Logic 1 in any bit position enables the corresponding bit in the pattern register to be compared. Logic 0 causes the masking of the corresponding bit. The default enables the register bit comparison.

Downloaded by Content Team @ Dortmine on Wednesday, 07 February, 2007 06:39:32 PM

CLP

The CLP bit contains the pattern to match in the eighth bit of the fourth octet of the 53-octet cell, in conjunction with the Idle Cell Header and Mask register bit. The IDLEPASS bit in the RCFP Configuration Register must be set to logic 0 to enable dropping of cells matching this pattern.

PTI[2:0]

The PTI[2:0] bits contain the pattern to match in the fifth, sixth, and seventh bits of the fourth octet of the 53-octet cell, in conjunction with the Idle Cell Header and Mask register bits. The IDLEPASS bit in the RCFP Configuration Register must be set to logic 0 to enable dropping of cells matching this pattern.

GFC[3:0]

The GFC[3:0] bits contain the pattern to match in the first, second, third, and fourth bits of the first octet of the 53-octet cell, in conjunction with the Idle Cell Header and Mask register bits. The IDLEPASS bit in the RCFP Configuration Register must be set to logic 0 to enable dropping of cells matching this pattern.

Note: an all-zeros pattern must be present in the VPI and VCI fields of the Idle or unassigned cell.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 06:59:22 AM

Register 0kC7H: RCFP Receive Byte/Idle Cell Counter (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	RBY_IC[15:0]	XXXX

Register 0kC8H: RCFP Receive Byte/Idle Cell Counter

Bit	Type	Function	Default
Bit 15 to Bit 0	R	RBY_IC[31:16]	XXXX

Register 0kC9H: RCFP Receive Byte/Idle Cell Counter (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 8	R	Unused	XXXX
Bit 7 to Bit 0	R	RBY_IC[39:32]	XXXX

RBY_IC[39:0]

When POS mode is selected, the RBY_IC[39:0] bits indicate the number of bytes received within POS frames during the last accumulation interval. The byte counts include all user payload bytes, FCS bytes, and abort bytes. Inclusion of stuffed bytes in the count is controlled by the RBY_MODE register bit. HDLC flags are not counted. In either mode, an abort sequence (0x7d7e) is counted as one byte.

When ATM mode is selected, the RBY_IC[39:0] bits indicate the number of Idle cells received and passed to the FIFO interface in the last accumulation interval.

A write to any one of the RCFP performance monitor counter registers or to the S/UNI 9953 Identity, and Global Performance Monitor Update register loads the registers with the current counter value and resets the internal 40 bit counter to 4,3,2,1 or 0. The counter reset value is dependent on if there were counter events during the transfer of the count to RCFP performance monitor Counter registers. The counter should be polled regularly to avoid saturation.

Downloaded by Content Now Partner Network Wednesday, 07 February, 2007, 06:59:32 PM

Register 0kCAH: RCFP Packet/Cell Counter (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	RP_RC[15:0]	XXXX

Register 0kCBH: RCFP Packet/Cell Counter (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	RP_RC[31:16]	XXXX

RP_RC[31:0]

When POS mode is selected, the RP_RC[31:0] bits indicate the number of received good packets passed to the receive FIFO interface during the last accumulation interval.

When ATM mode is selected, the RP_RC[31:0] bits indicate the number of received ATM cells passed to the receive FIFO interface in the last accumulation interval.

A write to any one of the RCFP performance monitor Counter registers or to the S/UNI 9953 Identity, and Global Performance Monitor Update register loads the registers with the current counter value and resets the internal 32 bit counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the RCFP performance monitor Counter registers. The counter should be polled regularly to avoid saturation.

Downloaded by Content Team of Partminer Inc on Wednesday 07 February 2007 06:59:32 PM

Register 0kCCH: RCFP Receive Errored FCS/HCS Counter

Bit	Type	Function	Default
Bit 15	R	EFCS[15]	X
Bit 14	R	EFCS[14]	X
Bit 13	R	EFCS[13]	X
Bit 12	R	EFCS[12]	X
Bit 11	R	EFCS[11]	X
Bit 10	R	EFCS[10]	X
Bit 9	R	EFCS[9]	X
Bit 8	R	EFCS[8]	X
Bit 7	R	EFCS[7]/UHCS[7]	X
Bit 6	R	EFCS[6]/UHCS[6]	X
Bit 5	R	EFCS[5]/UHCS[5]	X
Bit 4	R	EFCS[4]/UHCS[4]	X
Bit 3	R	EFCS[3]/UHCS[3]	X
Bit 2	R	EFCS[2]/UHCS[2]	X
Bit 1	R	EFCS[1]/UHCS[1]	X
Bit 0	R	EFCS[0]/UHCS[0]	X

EFCS[15:0]

When POS mode is selected, the EFCS[15:0] bits indicate the number of received FCS errors during the last accumulation interval.

UHCS[7:0]

When ATM mode is selected, the UHCS[7:0] bits indicate the number of uncorrectable HCS errors received in the last accumulation interval.

A write to any one of the RCFP performance monitor registers or to the S/UNI 9953 Identity, and Global Performance Monitor Update register loads the registers with the current counter value and resets the internal counters to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to these Counter registers. The counter should be polled regularly to avoid saturation.

Downloaded by Content Team of Chartwell Inc on Wednesday, 07 February, 2007 06:09:32 PM

Register 0kCDH: RCFP Receive Aborted Packet Counter

Bit	Type	Function	Default
Bit 15	R	RABR[15]	X
Bit 14	R	RABR[14]	X
Bit 13	R	RABR[13]	X
Bit 12	R	RABR[12]	X
Bit 11	R	RABR[11]	X
Bit 10	R	RABR[10]	X
Bit 9	R	RABR[9]	X
Bit 8	R	RABR[8]	X
Bit 7	R	RABR[7]	X
Bit 6	R	RABR[6]	X
Bit 5	R	RABR[5]	X
Bit 4	R	RABR[4]	X
Bit 3	R	RABR[3]	X
Bit 2	R	RABR[2]	X
Bit 1	R	RABR[1]	X
Bit 0	R	RABR[0]	X

RABR[15:0]

When POS mode is selected, the RABR[15:0] bits indicate the number of aborted packets received during the last accumulation interval. This counter is held at value 0 when ATM mode is selected.

A write to any one of the RCFP performance monitor registers or to the S/UNI 9953 Identity, and Global Performance Monitor Update register loads the registers with the current counter value and resets the internal counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the Receive Aborted Packet Counter registers. The counter should be polled regularly to avoid saturation.

Downloaded by Content Team of National Inc on Wednesday, 07 February, 2007 06:09:32 PM

Register 0kCEH: RCFP Receive Minimum Length Packet Error Counter

Bit	Type	Function	Default
Bit 15	R	RMINL[15]	X
Bit 14	R	RMINL[14]	X
Bit 13	R	RMINL[13]	X
Bit 12	R	RMINL[12]	X
Bit 11	R	RMINL[11]	X
Bit 10	R	RMINL[10]	X
Bit 9	R	RMINL[9]	X
Bit 8	R	RMINL[8]	X
Bit 7	R	RMINL[7]	X
Bit 6	R	RMINL[6]	X
Bit 5	R	RMINL[5]	X
Bit 4	R	RMINL[4]	X
Bit 3	R	RMINL[3]	X
Bit 2	R	RMINL[2]	X
Bit 1	R	RMINL[1]	X
Bit 0	R	RMINL[0]	X

RMINL[15:0]

When POS mode is selected, the RMINL[15:0] bits indicate the number of minimum length packet errors received during the last accumulation interval. This counter is held at value 0 when ATM mode is selected.

A write to any one of the RCFP performance monitor registers or to the S/UNI 9953 Identity, and Global Performance Monitor Update register loads the registers with the current counter value and resets the internal counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the Receive Minimum Length Packet Counter registers. The counter should be polled regularly to avoid saturation.

Downloaded by Content Team of Parallax Inc on Wednesday, 07 February, 2007 06:09:32 PM

Register 0kCFH: RCFP Receive Maximum Length Packet Error Counter

Bit	Type	Function	Default
Bit 15	R	RMAXL[15]	X
Bit 14	R	RMAXL[14]	X
Bit 13	R	RMAXL[13]	X
Bit 12	R	RMAXL[12]	X
Bit 11	R	RMAXL[11]	X
Bit 10	R	RMAXL[10]	X
Bit 9	R	RMAXL[9]	X
Bit 8	R	RMAXL[8]	X
Bit 7	R	RMAXL[7]	X
Bit 6	R	RMAXL[6]	X
Bit 5	R	RMAXL[5]	X
Bit 4	R	RMAXL[4]	X
Bit 3	R	RMAXL[3]	X
Bit 2	R	RMAXL[2]	X
Bit 1	R	RMAXL[1]	X
Bit 0	R	RMAXL[0]	X

RMAXL[15:0]

When POS mode is selected, the RMAXL[15:0] bits indicate the number of maximum length packet errors received during the last accumulation interval. This counter is held at value 0 when ATM mode is selected.

A write to any one of the RCFP performance monitor registers or to the S/UNI 9953 Identity, and Global Performance Monitor Update register loads the registers with the current counter value and resets the internal counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the Receive Maximum Length Packet Counter registers. The counter should be polled regularly to avoid saturation.

Downloaded by Content Team of Pericom Int'l on Wednesday, 07 February, 2007 06:09:32 PM

12.12 SONET/SDH Transmit Line Interface (STLI)

Register 1030H: STLI Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	Reserved	1
Bit 10	R/W	Reserved	1
Bit 9	R/W	Reserved	1
Bit 8	R/W	Reserved	1
Bit 7	R/W	PHASE_INIT[4]	0
Bit 6	R/W	PHASE_INIT[3]	0
Bit 5	R/W	PHASE_INIT[2]	0
Bit 4	R/W	PHASE_INIT[1]	0
Bit 3	R/W	INTERLEAVEEN4	1
Bit 2	R/W	INTERLEAVEEN3	1
Bit 1	R/W	INTERLEAVEEN2	1
Bit 0	R/W	INTERLEAVEEN1	1

INTERLEAVEEN[4:1]

The 4 byte interleave enable one (INTERLEAVEEN1) bit controls the 4 byte interleave rotation matrix in both OC-192 and in quad OC-48 modes. In OC-192 mode, only INTERLEAVEEN1 is active and INTERLEAVEEN[4:3] has no effect. In quad OC-48 mode, INTERLEAVEEN[n] bit controls the 4 byte interleave rotation matrix in the corresponding STS-48c (STM-16c) #n data stream. These bits should be set to there default values for normal operation.

PHASE_INIT[4:1]

The Phase Initialization register bits control the logic levels of the PHASE_INIT[N] outputs. If set to logic 0, the corresponding PHASE_INIT[N] output will be set low. If set to logic 1, the corresponding PHASE_INIT[N] output will be set high.

Reserved

The Reserved bits should be set to their default values for proper operation of the S/UNI 9953.

Downloaded by Content Team of Pantel Technologies on Wednesday, 07 February, 2007 06:59:32 PM

Register 1031H: STLI Programmable Clock Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	PGMTCLKSEL4[1]	0
Bit 6	R/W	PGMTCLKSEL4[0]	0
Bit 5	R/W	PGMTCLKSEL3[1]	0
Bit 4	R/W	PGMTCLKSEL3[0]	0
Bit 3	R/W	PGMTCLKSEL2[1]	0
Bit 2	R/W	PGMTCLKSEL2[0]	0
Bit 1	R/W	PGMTCLKSEL1[1]	0
Bit 0	R/W	PGMTCLKSEL1[0]	0

The STLI Programmable Clock Configuration Register is used to configure the frequencies of the TCLK[4:1] output clocks.

PGMTCLKSEL4-1[1:0]

The transmit programmable clock frequency bits enables and selects the frequency of the output clocks on PGMTCLK[4:1]. The output clocks are generated based on dividing down the corresponding input clock, TXCLK_SRC[4:1]. When configured for OC-192 operation, output clocks PGMTCLK[4:2] should be disabled to reduce board noise.

PGMTCLKSEL4-1[1:0]	Source
00	Inactive
01	8KHz
10	19.44MHz
11	77.76MHz

Downloaded by Content Team of Parts Engine on Wednesday, 07 February, 2007 08:59:32 PM

Register 1032H: STLI Interrupt Enable

Bit	Type	Function	Default
Bit 15	R	PH_ERR4	X
Bit 14	R	PH_ERR3	X
Bit 13	R	PH_ERR2	X
Bit 12	R	PH_ERR1	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	PH_ERR_FE[4]	0
Bit 6	R/W	PH_ERR_FE[3]	0
Bit 5	R/W	PH_ERR_FE[2]	0
Bit 4	R/W	PH_ERR_FE[1]	0
Bit 3	R/W	PH_ERR_RE[4]	0
Bit 2	R/W	PH_ERR_RE[3]	0
Bit 1	R/W	PH_ERR_RE[2]	0
Bit 0	R/W	PH_ERR_RE[1]	0

PH_ERR_RE[4:1]

The phase error rising edge interrupt enable (PH_ERR_RE[4:1]) bits enable or disable PHASE_ERR[4:1] inputs as the source for a rising edge interrupt. When any PH_ERR_RE[4:1] bits are set to logic one, a rising edge on the corresponding PHASE_ERR[4:1] input will cause an interrupt. When any PH_ERR_RE[4:1] bits are set to logic 0, a rising edge on the corresponding PHASE_ERR[4:1] input can not cause an interrupt.

PH_ERR_FE[4:1]

The phase error falling edge interrupt enable (PH_ERR_FE[4:1] bits enable or disable PHASE_ERR[4:1] inputs as the source for a falling edge interrupt. When any PH_ERR_FE[4:1] bits are set to logic one, a falling edge on the corresponding PHASE_ERR[4:1] input will cause an interrupt. When any PH_ERR_FE[4:1] bits are set to logic 0, a falling edge on the corresponding PHASE_ERR[4:1] input can not cause an interrupt.

PH_ERR[4:1]

The phase error status (PH_ERR[4:1]) bits simply reflect the logic levels of the PHASE_ERR[4:1] inputs.

Downloaded by Content Control Department on Wednesday, 07 February, 2007 06:59:32 PM

Register 1033H: STLI Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	PH_ERR4_FI	X
Bit 6	R	PH_ERR3_FI	X
Bit 5	R	PH_ERR2_FI	X
Bit 4	R	PH_ERR1_FI	X
Bit 3	R	PH_ERR4_RI	X
Bit 2	R	PH_ERR3_RI	X
Bit 1	R	PH_ERR2_RI	X
Bit 0	R	PH_ERR1_RI	X

If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, these interrupt status bits are cleared on a write of logic one. Otherwise, these interrupt status bits are cleared on read.

PH_ERR[4:1]_RI

The phase error rising edge interrupt status (PH_ERR[N]_RI) bit is set to logic one if a rising edge has been detected on the corresponding PHASE_ERR[N] input. These interrupt sources can activate the INTB output if the corresponding interrupt bit, PH_ERR_RE[N] is set to logic one.

PH_ERR[4:1]_FI

The phase error falling edge interrupt status (PH_ERR[N]_FI) bit is set to logic one if a falling edge has been detected on the corresponding PHASE_ERR[N] input. These interrupt sources can activate the INTB output if the corresponding interrupt bit, PH_ERR_FE[N] is set to logic one.

Downloaded by Content Team of Partsbase Inc on Wednesday, 07 February, 2007 06:59:32 PM

12.13 Transmit Regenerator and Multiplexer Processor (TRMP #1 - #16)

There are 16 TRMP (#1 - #16) blocks in 16 STM-4 processing slices with independent register sets. When the S/UNI 9953 is configured for quad OC-48 mode, TRMP #1, #5, #9, #13 are configured as masters and the remaining TRMP blocks are configured as slaves. When configured for OC-192 mode, only TRMP #1 is configured as master and the remaining blocks are configured as slaves.

Register 1n60H: TRMP Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	LREIBLK	0
Bit 10	R/W	LREIEN	1
Bit 9	R/W	APSEN	1
Bit 8	R/W	Reserved	1
Bit 7	R/W	TLDEN	0
Bit 6	R/W	~~Reserved~~TSLDSEL	0
Bit 5	R/W	Reserved	1
Bit 4	R/W	TSLDEN	0
Bit 3	R/W	TRACEEN	0
Bit 2	R/W	J0Z0INCEN	0
Bit 1	R/W	Z0DEF	0
Bit 0	R/W	A1A2EN	1

The TRMP Configuration register controls the transmit regenerator and Multiplexer functions.

These register bits are valid for both master and slave slices. Please refer to individual bit for details.

A1A2EN

The A1A2 framing enable (A1A2EN) bit controls the insertion of the framing bytes in the data stream. When A1A2EN is set to logic 1, F6h and 28h are inserted in the A1 and A2 bytes according to the priority of Table 10. When A1A2EN is set to logic 0, the framing bytes are not inserted.

This bit is valid for master and slave slices. For normal operation, this bit should be set to logic one for both master and slave slices.

Downloaded by Colum Team of Pathfinder Inc on Wednesday, 07 February 2007 06:02:32 PM

Z0DEF

The Z0 definition (Z0DEF) bit defines the Z0 growth bytes. When Z0DEF is set to logic 1, the Z0 bytes are defined according to ITU. The Z0 bytes are located in STS-1/STM-0 #2 to #12. When Z0DEF is set to logic 0, the Z0 bytes are defined according to TELCORDIA. The Z0 bytes are located in STS-1/STM-0 #2 to #192.

This bit is valid for master and slave slices. For normal operation, this bit should be set to the same value for both master and slave slices.

J0Z0INCEN

The J0 and Z0 increment enable (J0Z0INCEN) bit controls the insertion of an incremental pattern in the section trace and Z0 growth bytes. When J0ZOINCEN is set to logic 1, the corresponding STS-1/STM-0 path # is inserted in the J0 and Z0 bytes according to the priority of Table 10. When J0Z0INCEN is set to logic 0, no incremental pattern is inserted.

This bit is valid for master and slave slices. For normal operation, this bit should be set to the same value for both master and slave slices.

TRACEEN

The section trace enable (TRACEEN) bit controls the insertion of section trace in the data stream. When TRACEEN is set to logic 1, the section trace from the Section TTTP block is inserted in the J0 byte of STS-1/STM-0 #1 according to the priority of Table 10. When TRACEEN is set to logic 0, the section trace from the Section TTTP block is not inserted.

This bit is only valid for master slices.

TSLDEN

The TSLD enable (TSLDEN) bit controls the insertion of section or line DCC in the data stream. When TSLDEN is set to logic 1, the S/UNI 9953 inserts all ones or all zeros as selected using the TSLD_VAL bit in the S/UNI 9953 Transmit Control Register into the D1-D3 bytes or D4-D12 bytes of STS-1/STM-0 #1 according to the priority of Table 10. When TSLDEN is set to logic 0, the section or line DCC is not inserted.

This bit is only valid for master slices.

TSLDSEL

The TSLD channel select (TSLDSEL) bit selects the contents of the overhead ~~TSLD~~ port and the frequency of the overhead port ~~TSLDCLK~~ clock.

Note that this bit is used in conjunction with registers 0x0022 and 0x0023.

Downloaded by Content Team of Datasheet Inc on Wednesday, 07 February, 2007 16:59:02 PM

TSLDSEL	Contents
0	Section DCC (D1-D3)
1	Line DCC (D4-D12)

TLDEN

The TLD enable (TLDEN) bit controls the insertion of line DCC in the data stream. When TLDEN is set to logic 1, the S/UNI 9953 inserts all ones or all zeros as selected using the TLD_VAL bit in the S/UNI 9953 Transmit Control Register into in the D4-D12 bytes of STS-1/STM-0 #1 according to the priority of Table 10. When TLDEN is set to logic 0, line DCC is not inserted.

This bit is only valid for master slices.

APSEN

The APS enable (APSEN) bit controls the insertion of automatic protection switching in the data stream. When APSEN is set to logic 1, the APS bytes from the RRMP are inserted in the K1/K2 bytes of STS-1/STM-0 #1 according to the priority of Table 10. When APSEN is set to logic 0, the APS bytes from the RRMP are not inserted.

This bit is only valid for master slices.

LREIEN

The line REI enable (LREIEN) bit controls the insertion of line remote error indication in the data stream. When LREIEN is set to logic 1, the line REI from the RRMP is inserted in the M1 byte of STS-1/STM-0 #3 according to the priority of Table 10. When LREIEN is set to logic 0, the line REI from the RRMP is not inserted.

This bit is only valid for master slices.

LREIBLK

The line REI block error (LREIBLK) bit controls the generation of line remote error indication. When LREIBLK is set to logic 1, the line REI inserted in the M1 byte represents BIP-24 block errors (a maximum of 1 error per STS-3/STM-1 per frame). When LREIBLK is set to logic 0, the line REI inserted in the M1 byte represents BIP-8 errors (a maximum of 8 error per STS-1/STM-0 per frame up to a maximum of 255).

This bit is only valid for master slices.

Downloaded by Content Team of Parenthesis on Wednesday, 07 February, 2007 05:59:32 PM

Register 1n61H: TRMP Register Insertion

Bit	Type	Function	Default
Bit 15	R/W	UNUSEDV	0
Bit 14	R/W	UNUSEDEN	0
Bit 13	R/W	NATIONALV	0
Bit 12	R/W	NATIONALEN	0
Bit 11	—	Unused	X
Bit 10	R/W	E2REGbEN	0
Bit 9	R/W	Z2REGbEN	0
Bit 8	R/W	Z1REGbEN	0
Bit 7	R/W	S1REGbEN	0
Bit 6	R/W	D4D12REGbEN	0
Bit 5	R/W	K1K2REGbEN	0
Bit 4	R/W	D1D3REGbEN	0
Bit 3	R/W	F1REGbEN	0
Bit 2	R/W	E1REGbEN	0
Bit 1	R/W	Z0REGbEN	1
Bit 0	R/W	J0REGbEN	1

The TRMP Register Insertion register controls the transmit regenerator and Multiplexer functions.

These register bits are only valid for master slices.

J0REGbEN

The J0 register enable (J0REGbEN) bit controls the insertion of section trace in the data stream. When J0REGbEN is set to logic 1, the section trace from the TRMP Transmit J0 and Z0 register is inserted in the J0 byte of STS-1/STM-0 #1 according to the priority of Table 10. When J0REGbEN is set to logic 0, the section trace from the TRMP Transmit J0 and Z0 register is not inserted.

Z0REGbEN

The Z0 register enable (Z0REGbEN) bit controls the insertion of Z0 growth bytes in the data stream. When Z0REGbEN is set to logic 1, the Z0 growth byte from the TRMP Transmit J0 and Z0 register is inserted in the Z0 bytes according to the priority of Table 10. When Z0REGbEN is set to logic 0, the Z0 growth byte from the TRMP Transmit J0 and Z0 register is not inserted. The Z0DEF bit in the TRMP Configuration register defines the Z0 bytes.

Downloaded by Comstream of Comtier Inc on Wednesday, 07 February, 2007 06:39:32 PM

E1REGbEN

The E1 register enable (E1REGbEN) bit controls the insertion of section order wire in the data stream. When E1REGbEN is set to logic 1, the section order wire from the TRMP Transmit E1 and F1 register is inserted in the E1 byte of STS-1/STM-0 #1 according to the priority of Table 10. When E1REGbEN is set to logic 0, the section order wire from the TRMP Transmit E1 and F1 register is not inserted.

F1REGbEN

The F1 register enable (F1REGbEN) bit controls the insertion of section user channel in the data stream. When F1REGbEN is set to logic 1, the section user channel from the TRMP Transmit E1 and F1 register is inserted in the F1 byte of STS-1/STM-0 #1 according to the priority of Table 10. When F1REGbEN is set to logic 0, the section user channel from the TRMP Transmit E1 and F1 register is not inserted.

D1D3REGbEN

The D1 to D3 register enable (D1D3REGbEN) bit controls the insertion of section data communication channel in the data stream. When D1D3REGbEN is set to logic 1, the section DCC from the TRMP Transmit D1D3 and D4D12 register is inserted in the D1 to D3 bytes of STS-1/STM-0 #1 according to the priority of Table 10. When D1D3REGbEN is set to logic 0, the section DCC from the TRMP Transmit D1D3 and D4D12 register is not inserted.

K1K2REGbEN

The K1K2 register enable (K1K2REGbEN) bit controls the insertion of automatic protection switching in the data stream. When K1K2REGbEN is set to logic 1, the APS bytes from the TRMP Transmit K1 and K2 register are inserted in the K1, K2 bytes of STS-1/STM-0 #1 according to the priority of Table 10. When K1K2REGbEN is set to logic 0, the APS bytes from the TRMP Transmit K1 and K2 register are not inserted.

D4D12REGbEN

The D4 to D12 register enable (D4D12REGbEN) bit controls the insertion of line data communication channel in the data stream. When D4D12REGbEN is set to logic 1, the line DCC from the TRMP Transmit D1D3 and D4D12 register is inserted in the D4 to D12 bytes of STS-1/STM-0 #1 according to the priority of Table 10. When D4D12REGbEN is set to logic 0, the line DCC from the TRMP Transmit D1D3 and D4D12 register is not inserted.

Downloaded by Conexant on behalf of Paetec Holding on Wed Feb 07 2007 06:59:02 PM

S1REGbEN

The S1 register enable (S1REGbEN) bit controls the insertion of the synchronization status message in the data stream. When S1REGbEN is set to logic 1, the SSM from the TRMP Transmit S1 and Z1 register is inserted in the S1 byte of STS-1/STM-0 #1 according to the priority of Table 10. When S1REGbEN is set to logic 0, the SSM from the TRMP Transmit S1 and Z1 register is not inserted.

Z1REGbEN

The Z1 register enable (Z1REGbEN) bit controls the insertion of Z1 growth bytes in the data stream. When Z1REGbEN is set to logic 1, the Z1 byte from the TRMP Transmit S1 and Z1 register is inserted in the Z1 bytes according to the priority of Table 10. When Z1REGbEN is set to logic 0, the Z1 byte from the TRMP Transmit S1 and Z1 register is not inserted.

Z2REGbEN

The Z2 register enable (Z2REGbEN) bit controls the insertion of Z2 growth bytes in the data stream. When Z2REGbEN is set to logic 1, the Z2 byte from the TRMP Transmit Z2 and E2 register is inserted in the Z2 bytes according to the priority of Table 10. When Z2REGbEN is set to logic 0, the Z2 byte from the TRMP Transmit Z2 and E2 register is not inserted.

E2REGbEN

The E2 register enable (E2REGbEN) bit controls the insertion of line order wire in the data stream. When E2REGbEN is set to logic 1, the line order wire from the TRMP Transmit Z2 and E2 register is inserted in the E2 byte of STS-1/STM-0 #1 according to the priority of Table 10. When E2REGbEN is set to logic 0, the line order wire from the TRMP Transmit Z2 and E2 register is not inserted.

NATIONALEN

The national enable (NATIONALEN) bit controls the insertion of national bytes in the data stream. When NATIONALEN is set to logic 1, an all one or an all zero pattern is inserted in the national bytes according to the priority of Table 10. When NATIONALEN is set to logic 0, no pattern is inserted. The Z0DEF bit in the TRMP Configuration register defines the national bytes of ROW #1.

NATIONALV

The national value (NATIONALV) bit controls the value inserted in the national bytes. When NATIONALV is set to logic 1, an all one pattern is inserted in the national bytes if enabled via the NATIONALEN register bit. When NATIONALV is set to logic 0, an all zero pattern is inserted in the national bytes if enabled via the NATIONALEN register bit.

Downloaded by Content Part of PMC on Wednesday, 07 February 2007 06:5[illegible] PM

UNUSEDEN

The unused enable (UNUSEDEN) bit controls the insertion of unused bytes in the data stream. When UNUSEDEN is set to logic 1, an all one or an all zero pattern is inserted in the unused bytes according to the priority of Table 10. When UNUSEDEN is set to logic 0, no pattern is inserted.

UNUSEDV

The unused value (UNUSEDV) bit controls the value inserted in the unused bytes. When UNUSEDV is set to logic 1, an all one pattern is inserted in the unused bytes if enabled via the UNUSEDEN register bit. When UNUSEDV is set to logic 0, an all zero pattern is inserted in the unused bytes if enabled via the UNUSEDEN register bit.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 06:59:32 PM

Register 1n62H: TRMP Error Insertion

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	LOSINS	0
Bit 5	R/W	LAISINS	0
Bit 4	R/W	LRDIINS	0
Bit 3	R/W	A1ERR	0
Bit 2	R/W	HMASKEN	1
Bit 1	R/W	B2MASKEN	1
Bit 0	R/W	B1MASKEN	1

The TRMP Error Insertion register controls the transmit regenerator and Multiplexer diagnostic features.

These register bits are valid for both master and slave slices. Please refer to individual bit for details.

B1MASKEN

The B1 mask enable (B1MASKEN) bit selects the use of the B1 byte extracted from the TTOH port. When B1MASKEN is set to logic 1, the B1 byte extracted from the TTOH port is used as a mask to toggle bits in the calculated B1 byte (the B1 byte extracted from the TTOH port is XOR with the calculated B1 byte). When B1MASKEN is set to logic 0, the B1 byte extracted from the TTOH port is inserted instead of the calculated B1 byte.

This bit is only valid for master slices.

Downloaded by Content Team Datasheet Inc on Wednesday, 07 February, 2007 06:09:32 PM

B2MASKEN

The B2 mask enable (B2MASKEN) bit selects the use of the B2 bytes extracted from the TTOH port. When B2MASKEN is set to logic 1, the B2 bytes extracted from the TTOH port are used as a mask to toggle bits in the calculated B2 bytes (the B2 bytes extracted from the TTOH port are XOR with the calculated B2 bytes). When B2MASKEN is set to logic 0, the B2 bytes extracted from the TTOH port are inserted instead of the calculated B2 bytes.

This bit is valid for both master and slave slices.

HMASKEN

The H1/H2 mask enable (HMASKEN) bit selects the use of the H1/H2 bytes extracted from the TTOH port. When HMASKEN is set to logic 1, the H1/H2 bytes extracted from the TTOH port are used as a mask to toggle bits in the H1/H2 path payload pointer bytes (the H1/H2 bytes extracted from the TTOH port are XOR with the path payload pointer bytes). When HMASKEN is set to logic 0, the H1/H2 bytes extracted from the TTOH port are inserted instead of the internally generated path payload pointer bytes.

This bit is valid for both master and slave slices.

A1ERR

The A1 error insertion (A1ERR) bit is used to introduce framing errors in the A1 bytes. When A1ERR is set to logic 1, 76h instead of F6h is inserted in all of the A1 bytes of the STS-12/STM-4 #1 according to the priority of Table 10. When A1ERR is set to logic 0, no framing errors are introduced.

This bit is only valid for master slices.

LRDIINS

The line RDI insertion (LRDIINS) bit is used to force a line remote defect indication in the data stream. When LRDIINS is set to logic 1, the 110 pattern is inserted in bits 6, 7 and 8 of the K2 byte of STS-1/STM-0 #1 to force a line RDI condition. When LRDIINS is set to logic 0, the line RDI condition is removed.

This bit is only valid for master slices.

Downloaded by Content Team of Partminer Inc on Wednesday, 01 February, 2007 08:58:22 AM

LAISINS

The line AIS insertion (LAISINS) bit is used to force a line alarm indication signal in the data stream. When LAISINS is set to logic 1, all ones are inserted in the line overhead and in the payload (all the bytes of the frame except the section overhead bytes) to force a line AIS condition. When LAISINS is set to logic 0, the line AIS condition is removed. Line AIS is inserted/removed on frame boundary before scrambling.

This bit is valid for master and slave slices.

LOSINS

The LOS insertion (LOSINS) bit is used to force a loss of signal condition in the data stream. When LOSINS is set to logic 1, the data steam is set to all zeros (after scrambling) to force a loss of signal condition. When LOSINS is set to logic 0, the loss of signal condition is removed.

This bit is valid for master and slave slices.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:58:32 PM

Register 1n63H: TRMP Transmit J0 and Z0

Bit	Type	Function	Default
Bit 15	R/W	J0V[7]	0
Bit 14	R/W	J0V[6]	0
Bit 13	R/W	J0V[5]	0
Bit 12	R/W	J0V[4]	0
Bit 11	R/W	J0V[3]	0
Bit 10	R/W	J0V[2]	0
Bit 9	R/W	J0V[1]	0
Bit 8	R/W	J0V[0]	1
Bit 7	R/W	Z0V[7]	1
Bit 6	R/W	Z0V[6]	1
Bit 5	R/W	Z0V[5]	0
Bit 4	R/W	Z0V[4]	0
Bit 3	R/W	Z0V[3]	1
Bit 2	R/W	Z0V[2]	1
Bit 1	R/W	Z0V[1]	0
Bit 0	R/W	Z0V[0]	0

These register bits are only valid for master slices.

Z0V[7:0]

The Z0 byte value (Z0V[7:0]) bits hold the Z0 growth byte to be inserted into the data stream. The Z0V[7:0] value is inserted in the Z0 bytes if the insertion is enabled via the Z0REGbEN bit in the TRMP Register Insertion register. The Z0DEF bit in the TRMP Configuration register defines the Z0 bytes.

J0V[7:0]

The J0 byte value (J0V[7:0]) bits hold the section trace to be inserted into the data stream. The J0V[7:0] value is inserted in the J0 byte of STS-1/STM-0 #1 if the insertion is enabled via the J0REGbEN bit in the TRMP Register Insertion register.

Downloaded by Content Team at Partminer.com on Wednesday, 07 February, 2007 06:09:32 PM

Register 1n64H: TRMP Transmit E1 and F1

Bit	Type	Function	Default
Bit 15	R/W	E1V[7]	0
Bit 14	R/W	E1V[6]	0
Bit 13	R/W	E1V[5]	0
Bit 12	R/W	E1V[4]	0
Bit 11	R/W	E1V[3]	0
Bit 10	R/W	E1V[2]	0
Bit 9	R/W	E1V[1]	0
Bit 8	R/W	E1V[0]	0
Bit 7	R/W	F1V[7]	0
Bit 6	R/W	F1V[6]	0
Bit 5	R/W	F1V[5]	0
Bit 4	R/W	F1V[4]	0
Bit 3	R/W	F1V[3]	0
Bit 2	R/W	F1V[2]	0
Bit 1	R/W	F1V[1]	0
Bit 0	R/W	F1V[0]	0

These register bits are only valid for master slices.

F1V[7:0]

The F1 byte value (F1V[7:0]) bits hold the section user channel to be inserted into the data stream. The F1V[7:0] value is inserted in the F1 byte of STS-1/STM-0 #1 if the insertion is enabled via the F1REGbEN bit in the TRMP Register Insertion register.

E1V[7:0]

The E1 byte value (E1V[7:0]) bits hold the section order wire to be inserted into the data stream. The E1V[7:0] value is inserted in the E1 byte of STS-1/STM-0 #1 if the insertion is enabled via the E1REGbEN bit in the TRMP Register Insertion register.

Downloaded by Content Team Department on Wednesday, 07 February, 2007 06:09:32 PM

Register 1n65H: TRMP Transmit D1D3 and D4D12

Bit	Type	Function	Default
Bit 15	R/W	D1D3V[7]	0
Bit 14	R/W	D1D3V[6]	0
Bit 13	R/W	D1D3V[5]	0
Bit 12	R/W	D1D3V[4]	0
Bit 11	R/W	D1D3V[3]	0
Bit 10	R/W	D1D3V[2]	0
Bit 9	R/W	D1D3V[1]	0
Bit 8	R/W	D1D3V[0]	0
Bit 7	R/W	D4D12V[7]	0
Bit 6	R/W	D4D12V[6]	0
Bit 5	R/W	D4D12V[5]	0
Bit 4	R/W	D4D12V[4]	0
Bit 3	R/W	D4D12V[3]	0
Bit 2	R/W	D4D12V[2]	0
Bit 1	R/W	D4D12V[1]	0
Bit 0	R/W	D4D12V[0]	0

These register bits are only valid for master slices.

D4D12V[7:0]

The D4D12 byte value (D4D12V[7:0]) bits hold the line data communication channel to be inserted into the data stream. The D4D12V[7:0] value is inserted in the D4 to D12 bytes of STS-1/STM-0 #1 if the insertion is enabled via the D4D12REGbEN bit in the TRMP Register Insertion register.

D1D3V[7:0]

The D1D3 byte value (D1D3V[7:0]) bits hold the section data communication channel to be inserted into the data stream. The D1D3V[7:0] value is inserted in the D1 to D3 bytes of STS-1/STM-0 #1 if the insertion is enabled via the D1D3REGbEN bit in the TRMP Register Insertion register.

Downloaded by Content Team Partminer.com on Wednesday, 07 February, 2007 06:39:32 PM

Register 1n66H: TRMP Transmit K1 and K2

Bit	Type	Function	Default
Bit 15	R/W	K1V[7]	0
Bit 14	R/W	K1V[6]	0
Bit 13	R/W	K1V[5]	0
Bit 12	R/W	K1V[4]	0
Bit 11	R/W	K1V[3]	0
Bit 10	R/W	K1V[2]	0
Bit 9	R/W	K1V[1]	0
Bit 8	R/W	K1V[0]	0
Bit 7	R/W	K2V[7]	0
Bit 6	R/W	K2V[6]	0
Bit 5	R/W	K2V[5]	0
Bit 4	R/W	K2V[4]	0
Bit 3	R/W	K2V[3]	0
Bit 2	R/W	K2V[2]	0
Bit 1	R/W	K2V[1]	0
Bit 0	R/W	K2V[0]	0

These register bits are only valid for master slices.

K1V[7:0], K2V[7:0]

The K1, K2 bytes value (K1V[7:0], K2V[7:0]) bits hold the APS bytes to be inserted into the data stream. The K1V[7:0], K2V[7:0] values are inserted in the K1, K2 bytes of STS-1/STM-0 #1 if the insertion is enabled via the K1K2REGbEN bit in the TRMP Register Insertion register.

Downloaded by Content Team of Partminer.com on Wednesday, 07 February, 2007 06:09:32 PM

Register 1n67H: TRMP Transmit S1 and Z1

Bit	Type	Function	Default
Bit 15	R/W	S1V[7]	0
Bit 14	R/W	S1V[6]	0
Bit 13	R/W	S1V[5]	0
Bit 12	R/W	S1V[4]	0
Bit 11	R/W	S1V[3]	0
Bit 10	R/W	S1V[2]	0
Bit 9	R/W	S1V[1]	0
Bit 8	R/W	S1V[0]	0
Bit 7	R/W	Z1V[7]	0
Bit 6	R/W	Z1V[6]	0
Bit 5	R/W	Z1V[5]	0
Bit 4	R/W	Z1V[4]	0
Bit 3	R/W	Z1V[3]	0
Bit 2	R/W	Z1V[2]	0
Bit 1	R/W	Z1V[1]	0
Bit 0	R/W	Z1V[0]	0

These register bits are only valid for master slices.

Z1V[7:0]

The Z1 byte value (Z1V[7:0]) bits hold the Z1 growth byte to be inserted into the data stream. The Z1V[7:0] value is inserted in the Z1 byte if the insertion is enabled via the Z1REGbEN bit in the TRMP Register Insertion register.

S1V[7:0]

The S1 byte value (S1V[7:0]) bits hold the synchronization status message to be inserted into the data stream. The S1V[7:0] value is inserted in the S1 byte of STS-1/STM-0 #1 if the insertion is enabled via the S1REGbEN bit in the TRMP Register Insertion register.

Downloaded by Content Team at Chartmine.com on Wednesday, 07 February, 2007 06:09:32 PM

Register 1n68H: TRMP Transmit Z2 and E2

Bit	Type	Function	Default
Bit 15	R/W	Z2V[7]	0
Bit 14	R/W	Z2V[6]	0
Bit 13	R/W	Z2V[5]	0
Bit 12	R/W	Z2V[4]	0
Bit 11	R/W	Z2V[3]	0
Bit 10	R/W	Z2V[2]	0
Bit 9	R/W	Z2V[1]	0
Bit 8	R/W	Z2V[0]	0
Bit 7	R/W	E2V[7]	0
Bit 6	R/W	E2V[6]	0
Bit 5	R/W	E2V[5]	0
Bit 4	R/W	E2V[4]	0
Bit 3	R/W	E2V[3]	0
Bit 2	R/W	E2V[2]	0
Bit 1	R/W	E2V[1]	0
Bit 0	R/W	E2V[0]	0

These register bits are only valid for master slices.

E2V[7:0]

The E2 byte value (E2[7:0]) bits hold the line order wire to be inserted into the data stream. The E2V[7:0] value is inserted in the E2 byte of STS-1/STM-0 #1 if the insertion is enabled via the E2REGbEN bit in the TRMP Register Insertion register.

Z2V[7:0]

The Z2 byte value (Z2V[7:0]) bits hold the Z2 growth byte to be inserted into the data stream. The Z2V[7:0] value is inserted in the Z2 byte if the insertion is enabled via the Z2REGbEN bit in the TRMP Register Insertion register.

Downloaded by Content Team Department on Wednesday, 07 February, 2007 06:09:32 PM

Register 1n69H: TRMP Transmit H1 and H2 Mask

Bit	Type	Function	Default
Bit 15	R/W	H1MASK[7]	0
Bit 14	R/W	H1MASK[6]	0
Bit 13	R/W	H1MASK[5]	0
Bit 12	R/W	H1MASK[4]	0
Bit 11	R/W	H1MASK[3]	0
Bit 10	R/W	H1MASK[2]	0
Bit 9	R/W	H1MASK[1]	0
Bit 8	R/W	H1MASK[0]	0
Bit 7	R/W	H2MASK[7]	0
Bit 6	R/W	H2MASK[6]	0
Bit 5	R/W	H2MASK[5]	0
Bit 4	R/W	H2MASK[4]	0
Bit 3	R/W	H2MASK[3]	0
Bit 2	R/W	H2MASK[2]	0
Bit 1	R/W	H2MASK[1]	0
Bit 0	R/W	H2MASK[0]	0

These register bits are only valid for master slices.

H2MASK[7:0]

The H2 mask (H2MASK[7:0]) bits hold the H2 path payload pointer errors to be inserted into the data stream. The H2MASK[7:0] is XORed with the path payload pointer already in the data stream.

H1MASK[7:0]

The H1 mask (H1MASK[7:0]) bits hold the H1 path payload pointer errors to be inserted into the data stream. The H1MASK[7:0] is XORed with the path payload pointer already in the data stream.

Downloaded by Content Team of Chartminer.com on Wednesday, 07 February, 2007 06:09:32 PM

Register 1n6AH: TRMP Transmit B1 and B2 Mask

Bit	Type	Function	Default
Bit 15	R/W	B1MASK[7]	0
Bit 14	R/W	B1MASK[6]	0
Bit 13	R/W	B1MASK[5]	0
Bit 12	R/W	B1MASK[4]	0
Bit 11	R/W	B1MASK[3]	0
Bit 10	R/W	B1MASK[2]	0
Bit 9	R/W	B1MASK[1]	0
Bit 8	R/W	B1MASK[0]	0
Bit 7	R/W	B2MASK[7]	0
Bit 6	R/W	B2MASK[6]	0
Bit 5	R/W	B2MASK[5]	0
Bit 4	R/W	B2MASK[4]	0
Bit 3	R/W	B2MASK[3]	0
Bit 2	R/W	B2MASK[2]	0
Bit 1	R/W	B2MASK[1]	0
Bit 0	R/W	B2MASK[0]	0

These register bits are only valid for master slices.

B2MASK[7:0]

The B2 mask (B2MASK[7:0]) bits hold the B2 BIP-8 errors to be inserted into the data stream. The B2MASK[7:0] is XORed with the calculated B2 before insertion in the B2 byte.

B1MASK[7:0]

The B1 mask (B1MASK[7:0]) bits hold the B1 BIP-8 errors to be inserted into the data stream. The B1MASK[7:0] is XORed with the calculated B1 before insertion in the B1 byte.

Downloaded by Content Team of Chartminer.com on Wednesday, 07 February, 2007 06:09:32 PM

12.14 Transmit Trail Trace Processor, Section (TTTP #1 - #4)

There are 4 Section TTTP (#1 - #4) blocks in 4 STM-16 processing groups with independent register sets. When the S/UNI 9953 is configured for quad OC-48 mode, all four blocks are configured as masters to process the STS-48c/STM-16c data streams. When configured for OC-192 mode, only TTTP #1 is configured as master and the other three (#2 - #4) blocks are inactive and may be considered as slaves.

Register 1k70H: TTTP Section Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	—	Unused	X
Bit 12	R/W	IADDR[6]	0
Bit 11	R/W	IADDR[5]	0
Bit 10	R/W	IADDR[4]	0
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	SECTION[3]	0
Bit 2	R/W	SECTION[2]	0
Bit 1	R/W	SECTION[1]	0
Bit 0	R/W	SECTION[0]	0

SECTION[3:0]

The Section (SECTION[3:0]) bits must be set to b’0001 for proper operation of the S/UNI 9953.

Note: The default value of b’0000 must be modified during initial device configuration.

IADDR[6:0]

The indirect address location (IADDR[6:0]) bits select which indirect address location is accessed by the current indirect transfer.

Indirect Address IADDR[6:0]	Indirect Data
000 0000	Configuration
000 0001 to	Invalid address

Downloaded by Content Team of Portminer Inc on Wednesday, 07 February 2007 06:56:07 PM

Indirect Address IADDR[6:0]	Indirect Data
011 1111	
100 0000	First byte of the 1/16/64 byte trace
100 0001 to 111 1111	Other bytes of the 16/64 byte trace

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0 upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 06:59:32 PM

Register 1k71H: TTTP Section Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Downloaded by Content Team of Partner for use on Wednesday, 07 February, 2007 06:09:32 PM

Register 1k71H (Indirect Register 00H): TTTP Section Trace Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R/W	ZEROEN	0
Bit 1	R/W	BYTEEN	0
Bit 0	R/W	LENGTH16	0

LENGTH16

The message length (LENGTH16) bit selects the length of the trial trace message to be transmitted. When LENGTH16 is set to logic 1, the length of the trial trace message is 16 bytes. When LENGTH16 is set to logic 0, the length of the trial trace message is 64 bytes.

BYTEEN

The single byte message enable (BYTEEN) bit enables the single byte trial trace message. When BYTEEN is set to logic 1, the length of the trial trace message is 1 byte. When BYTEEN is set to logic 0, the length of the trial trace message is determined by LENGTH16. BYTEEN has precedence over LENGTH16.

ZEROEN

The all zero message enable (ZEROEN) bit enables the transmission of an all zero trial trace message. When ZEROEN is set to logic 1, an all zero message is transmitted. When ZEROEN is set to logic 0, the RAM message is transmitted. The enabling and disabling of the all zero trial trace message is not done on message boundary since the receiver is required to perform filtering on the message.

Downloaded by Content Team of Datasheet Inc. on Wednesday, 07 February, 2007 06:39:32 PM

Register 1k71H (Indirect Register 40H to 7FH): TTTP Section Indirect Register

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	TRACE[7]	X
Bit 6	R/W	TRACE[6]	X
Bit 5	R/W	TRACE[5]	X
Bit 4	R/W	TRACE[4]	X
Bit 3	R/W	TRACE[3]	X
Bit 2	R/W	TRACE[2]	X
Bit 1	R/W	TRACE[1]	X
Bit 0	R/W	TRACE[0]	X

TRACE[7:0]

The trial trace message (TRACE[7:0]) bits contain the trial trace message to be transmitted. When BYTEEN is set to logic 1, the message is stored at indirect register address 40h. When BYTEEN is set to logic 0 and LENGTH16 is set to logic 1, the message is stored between indirect register address 40h and 4Fh. When BYTEEN is set to logic 0 and LENGTH16 is set to logic 0, the message is stored between indirect register address 40h and 7Fh.

Downloaded by Content Team of Partminer on Wednesday, 07 February, 2007 06:09:32 PM

12.15 Transmit Trail Trace Processor, Path (TTTP #1 - #4)

There are 4 Path TTTP (#1 - #4) blocks in 4 STM-16 processing groups with independent register sets. When the S/UNI 9953 is configured for quad OC-48 mode, all four blocks are configured as masters to process the STS-48c/STM-16c data streams. When configured for OC-192 mode, only TTTP #1 is configured as master and the other three (#2 - #4) blocks are inactive and may be considered as slaves.

Register 1k78H: TTTP Path Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	—	Unused	X
Bit 12	R/W	IADDR[6]	0
Bit 11	R/W	IADDR[5]	0
Bit 10	R/W	IADDR[4]	0
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]

The Path (PATH[3:0]) bits must be set to b’0001 for proper operation of the S/UNI 9953.

Note: The default value of b’0000 must be modified during initial device configuration.

IADDR[6:0]

The indirect address location (IADDR[6:0]) bits select which indirect address location is accessed by the current indirect transfer.

Indirect Address IADDR[6:0]	Indirect Data
000 0000	Configuration
000 0001 to 011 1111	Invalid address

Downloaded by Comet Team of Portminer Inc. on Wednesday, 07 February, 2007 06:52:07PM

Indirect Address IADDR[6:0]	Indirect Data
100 0000	First byte of the 1/16/64 byte trace
100 0001 to 111 1111	Other bytes of the 16/64 byte trace

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0 upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 06:59:32 PM

Register 1k79H: TTTP Path Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Downloaded by Content Team of Partner on Wednesday, 07 February, 2007 06:09:32 PM

Register 1k79H (Indirect Register 00H): TTTP Path Trace Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R/W	ZEROEN	0
Bit 1	R/W	BYTEEN	0
Bit 0	R/W	LENGTH16	0

LENGTH16

The message length (LENGTH16) bit selects the length of the trial trace message to be transmitted. When LENGTH16 is set to logic 1, the length of the trial trace message is 16 bytes. When LENGTH16 is set to logic 0, the length of the trial trace message is 64 bytes.

BYTEEN

The single byte message enable (BYTEEN) bit enables the single byte trial trace message. When BYTEEN is set to logic 1, the length of the trial trace message is 1 byte. When BYTEEN is set to logic 0, the length of the trial trace message is determined by LENGTH16. BYTEEN has precedence over LENGTH16.

ZEROEN

The all zero message enable (ZEROEN) bit enables the transmission of an all zero trial trace message. When ZEROEN is set to logic 1, an all zero message is transmitted. When ZEROEN is set to logic 0, the RAM message is transmitted. The enabling and disabling of the all zero trial trace message is not done on message boundary since the receiver is required to perform filtering on the message.

Downloaded by Content Team of Datasheet Inc. on Wednesday, 07 February, 2007 06:39:32 PM

Register 1k79H (Indirect Register 40H to 7FH): TTTP Path Indirect Register

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	TRACE[7]	X
Bit 6	R/W	TRACE[6]	X
Bit 5	R/W	TRACE[5]	X
Bit 4	R/W	TRACE[4]	X
Bit 3	R/W	TRACE[3]	X
Bit 2	R/W	TRACE[2]	X
Bit 1	R/W	TRACE[1]	X
Bit 0	R/W	TRACE[0]	X

TRACE[7:0]

The trial trace message (TRACE[7:0]) bits contain the trial trace message to be transmitted. When BYTEEN is set to logic 1, the message is stored at indirect register address 40h. When BYTEEN is set to logic 0 and LENGTH16 is set to logic 1, the message is stored between indirect register address 40h and 4Fh. When BYTEEN is set to logic 0 and LENGTH16 is set to logic 0, the message is stored between indirect register address 40h and 7Fh.

Downloaded by Content Team of Partminer on Wednesday, 07 February, 2007 06:09:32 PM

12.16 Transmit High Order Path Processor (THPP #1 - #16)

There are 16 THPP (#1 - #16) blocks in 16 STM-4 processing slices with independent register sets. When the S/UNI 9953 is configured for quad OC-48 mode, THPP #1, #5, #9, #13 are configured as masters and the remaining THPP blocks are configured as slaves. When configured for OC-192 mode, only THPP #1 is configured as master and the remaining blocks are configured as slaves.

Register 1n80H: THPP Configuration 1

Bit	Type	Function	Default
Bit 15	R/W	SRCJ1	0
Bit 14	R/W	SRCC2	0
Bit 13	R/W	SRCG1	0
Bit 12	R/W	SRCF2	0
Bit 11	R/W	SRCH4	0
Bit 10	R/W	SRCZ3	0
Bit 9	R/W	SRCZ4	0
Bit 8	R/W	SRCZ5	0
Bit 7	R/W	PTBJ1	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	ENG1REC	1
Bit 4	R/W	FSBEN	0
Bit 3	R/W	PREIEBLK	0
Bit 2	R/W	IBER	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

The THPP Configuration 1 (and 2) Register is provided for configuring the manner in which the STS-12c/STM-4c payload is processed by THPP. These register bits should normally be set low when the THPP is configured as a slave unless indicated otherwise.

IBER

When the IBER register bit is set to logic 1, the G1 byte is allowed to pass through the THPP without modification. When IBER is set to logic 0, the G1 byte is not passed through transparently and can be modified by one of the THPP POH sources.

PREIEBLK

When PREIEBLK is set to logic 1, the path REI value transmitted represents BIP-8 block errors, i.e. the REI-P value allowed in G1 is either 0 or 1. When PREIEBLK is set to logic 0, the path REI value transmitted represents BIP-8 errors, i.e. the REI-P value allowed in G1 is from 0 to 8.

Downloaded by Content Team of Pacific Internet - Wednesday, 07 February, 2007 06:55:47 PM

FSBEN

When FSBEN is set to logic 1, THPP overwrites the fixed stuff byte with the value (FSBV[7:0]) found in the THPP Transmit B3MASK and Fixed Stuff Byte Register. When FSBEN is set to logic 0, the fixed stuff byte is transparently passed through THPP.

ENG1REC

This bit should be left in its default logic 1 for normal operation.

PTBJ1

The PTBJ1 register bit is used to determine the origin of the path trace byte to be inserted in the transmit stream. When PTBJ1 is set high, the J1 byte source is the corresponding TTTP block. When PTBJ1 is set to logic low, the J1 byte source is other than the TTTP block.

SRCJ1, SRCC2, SRCH4, SRCG1, SRCF2, SRCZ3, SRCZ4, SRCZ5

The SRCxx bits are used to determine the source of the path overhead bytes in the transmit stream. For example, when a logic 1 is written to SRCJ1, the J1 byte inserted (J1V[7:0]) is sourced from the THPP Transmit C2 and J1 Register. When a logic 0 is written to SRCJ1, the J1 byte source can be the path trace buffer (TTTP) depending on the value of the register bit PTBJ1. If PTBJ1 and SRCJ1 are both equal to logic 0, the J1 byte is passed through THPP transparently without modification.

Downloaded by Content Team of Partminer Inc on Tuesday, 27 February, 2007 06:59:32 PM

Register 1n81H: THPP Configuration 2

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	H4MASK	0
Bit 2	R/W	B3MASKEN	0
Bit 1	R/W	UNEQ	0
Bit 0	R/W	UNEQV	0

The THPP Configuration 2 (and 1) Register is provided for configuring the manner in which the STS-12c/STM-4c payload is processed by THPP. These register bits should normally be set low when the THPP is configured as a slave unless indicated otherwise.

UNEQV

The unequipped value (UNEQV) bit controls the value inserted in the path overhead and in the payload. When UNEQV is set to logic 1, an all one pattern is inserted in the path overhead and in the payload if enable via the UNEQ register bit. When UNEQV is set to logic 0, an all zero pattern is inserted in the path overhead and in the payload if enable via the UNEQ register bit.

UNEQ

The unequipped bit (UNEQ) controls the insertion of an all one or an all zero pattern in the path overhead and in the payload, the fixed stuff bytes are excluded from insertion. When UNEQ is set to logic one, an all one or an all zero pattern is inserted in the path overhead and in the payload. When UNEQ is set logic 0, no pattern is inserted.

B3MASKEN

When B3MASKEN is logic high, the byte received via the TPOH (valid only if TPOHEN is logic high) bit serial stream is to be used as a mask for an internally generated B3. When B3MASKEN is logic low, the byte received on TPOH (valid only if TPOHEN is logic high) will be inserted into the transmit stream only if the path overhead source priority is TPOH.

Downloaded by Conte Team of Pmc-Sierra Inc on Wednesday, 07 February, 2007 06:59:32 PM

When TPOHEN is logic low, the calculated B3 is XORed with B3MASK, independent of the setting of the B3MASKEN bit.

H4MASK

When H4MASK is logic high, the byte received via the TPOH (valid only if TPOHEN is logic high) bit serial stream is used as an error mask for the H4 byte passing through the THPP. When H4MASK is logic low, the byte received on TPOH (valid only if TPOHEN is logic high) will be inserted into the transmit stream only if the path overhead source priority is TPOH.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 09:39:32 PM

Register 1n82H: THPP Transmit C2 and J1

Bit	Type	Function	Default
Bit 15	R/W	C2V[7]	0
Bit 14	R/W	C2V[6]	0
Bit 13	R/W	C2V[5]	0
Bit 12	R/W	C2V[4]	0
Bit 11	R/W	C2V[3]	0
Bit 10	R/W	C2V[2]	0
Bit 9	R/W	C2V[1]	0
Bit 8	R/W	C2V[0]	0
Bit 7	R/W	J1V[7]	0
Bit 6	R/W	J1V[6]	0
Bit 5	R/W	J1V[5]	0
Bit 4	R/W	J1V[4]	0
Bit 3	R/W	J1V[3]	0
Bit 2	R/W	J1V[2]	0
Bit 1	R/W	J1V[1]	0
Bit 0	R/W	J1V[0]	0

The THPP Transmit C2 and J1 Register provides the corresponding POH byte source for the STS-12c/STM-4c payload processed by THPP. These register bits should normally be set low when the THPP is configured as a slave unless indicated otherwise.

J1V[7:0]

When SRCJ1 is logic high, this byte is inserted in the J1 path overhead byte position in the transmit stream.

C2 [7:0]

When SRCC2 is logic high, this byte is inserted in the C2 path overhead byte position in the transmit stream.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 1n83H: THPP Transmit F2 and G1

Bit	Type	Function	Default
Bit 15	R/W	F2V[7]	0
Bit 14	R/W	F2V[6]	0
Bit 13	R/W	F2V[5]	0
Bit 12	R/W	F2V[4]	0
Bit 11	R/W	F2V[3]	0
Bit 10	R/W	F2V[2]	0
Bit 9	R/W	F2V[1]	0
Bit 8	R/W	F2V[0]	0
Bit 7	R/W	G1V[7]	0
Bit 6	R/W	G1V[6]	0
Bit 5	R/W	G1V[5]	0
Bit 4	R/W	G1V[4]	0
Bit 3	R/W	G1V[3]	0
Bit 2	R/W	G1V[2]	0
Bit 1	R/W	G1V[1]	0
Bit 0	R/W	G1V[0]	0

The THPP Transmit F2 and G1 Register provides the corresponding POH byte source for the STS-12c/STM-4c payload processed by THPP. These register bits should normally be set low when the THPP is configured as a slave unless indicated otherwise.

G1V[7:0]

When SRCG1 is logic high, this byte is inserted in the G1 path overhead byte position in the transmit stream.

F2V[7:0]

When SRCF2 is logic high, this byte is inserted in the F2 path overhead byte position in the transmit stream.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 1n84H: THPP Transmit Z3 and H4

Bit	Type	Function	Default
Bit 15	R/W	Z3V[7]	0
Bit 14	R/W	Z3V[6]	0
Bit 13	R/W	Z3V[5]	0
Bit 12	R/W	Z3V[4]	0
Bit 11	R/W	Z3V[3]	0
Bit 10	R/W	Z3V[2]	0
Bit 9	R/W	Z3V[1]	0
Bit 8	R/W	Z3V[0]	0
Bit 7	R/W	H4V[7]	0
Bit 6	R/W	H4V[6]	0
Bit 5	R/W	H4V[5]	0
Bit 4	R/W	H4V[4]	0
Bit 3	R/W	H4V[3]	0
Bit 2	R/W	H4V[2]	0
Bit 1	R/W	H4V[1]	0
Bit 0	R/W	H4V[0]	0

The THPP Transmit Z3 and H4 Register provides the corresponding POH byte source for the STS-12c/STM-4c payload processed by THPP. These register bits should normally be set low when the THPP is configured as a slave unless indicated otherwise.

H4V[7:0]

When SRCH4 is logic high, this byte is inserted in the H4 path overhead byte position in the transmit stream.

Z3V[7:0]

When SRCZ3 is logic high, this byte is inserted in the Z3 path overhead byte position in the transmit stream.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 1n85H: THPP Transmit Z5 and Z4

Bit	Type	Function	Default
Bit 15	R/W	Z5V[7]	0
Bit 14	R/W	Z5V[6]	0
Bit 13	R/W	Z5V[5]	0
Bit 12	R/W	Z5V[4]	0
Bit 11	R/W	Z5V[3]	0
Bit 10	R/W	Z5V[2]	0
Bit 9	R/W	Z5V[1]	0
Bit 8	R/W	Z5V[0]	0
Bit 7	R/W	Z4V[7]	0
Bit 6	R/W	Z4V[6]	0
Bit 5	R/W	Z4V[5]	0
Bit 4	R/W	Z4V[4]	0
Bit 3	R/W	Z4V[3]	0
Bit 2	R/W	Z4V[2]	0
Bit 1	R/W	Z4V[1]	0
Bit 0	R/W	Z4V[0]	0

The THPP Transmit Z5 and Z4 Register provides the corresponding POH byte source for the STS-12c/STM-4c payload processed by THPP. These register bits should normally be set low when the THPP is configured as a slave unless indicated otherwise.

Z4V[7:0]

When SRCZ4 is logic high, this byte is inserted in the Z4 path overhead byte position in the transmit stream.

Z5V[7:0]

When SRCZ5 is logic high, this byte is inserted in the Z5 path overhead byte position in the transmit stream.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 1n86H: THPP Transmit B3MASK and Fixed Stuff Byte

Bit	Type	Function	Default
Bit 15	R/W	B3MASK[7]	0
Bit 14	R/W	B3MASK[6]	0
Bit 13	R/W	B3MASK[5]	0
Bit 12	R/W	B3MASK[4]	0
Bit 11	R/W	B3MASK[3]	0
Bit 10	R/W	B3MASK[2]	0
Bit 9	R/W	B3MASK[1]	0
Bit 8	R/W	B3MASK[0]	0
Bit 7	R/W	FSBV[7]	0
Bit 6	R/W	FSBV[6]	0
Bit 5	R/W	FSBV[5]	0
Bit 4	R/W	FSBV[4]	0
Bit 3	R/W	FSBV[3]	0
Bit 2	R/W	FSBV[2]	0
Bit 1	R/W	FSBV[1]	0
Bit 0	R/W	FSBV[0]	0

The THPP Transmit B3MASK and Fixed Stuff Byte Register provides the corresponding B3 error mask and fixed stuff byte source for the STS-12c/STM-4c payload processed by THPP. These register bits should normally be set low when the THPP is configured as a slave unless indicated otherwise.

FSBV[7:0]

When FSBEN is logic one, the THPP inserts this value in all the fixed stuff bytes in the transmit stream.

B3MASK[7:0]

The transmit B3 byte is XORed with this error mask value when the B2MASKEN bit is set high to enable diagnostic B3 error insertion.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

12.17 Transmit 8B/10B TelecomBus Encoder (T8TE #1 - #16)

There are 16 T8TE (#1 - #16) blocks in 16 STM-4 processing slices with independent register sets.

Register 1nA0H: T8TE APS Control and Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	FIFOERRE	0
Bit 3	R/W	TPINS	0
Bit 2	R/W	Reserved	0
Bit 1	W	CENTER	0
Bit 0	R/W	DLCV	0

DLCV

The diagnose line code violation bit (DLCV) controls the insertion of line code violations in the outgoing data stream. When this bit is set high, the transmit encoded data bus is inverted to generate the complementary running disparity.

CENTER

The FIFO centering control bit (CENTER) controls the separation of the FIFO read and write pointers. CENTER is a write only bit. When a logic high is written to CENTER, and the current FIFO depth is not in the range of 3, 4 or 5 characters, the FIFO depth is forced to be four 8B/10B characters deep with a momentary data corruption. Writing to the CENTER bit when the FIFO depth is in the 3, 4 or 5 character range produces no effect. CENTER always returns a logic low when read.

Downloaded by Copyright © of Parameter Inc. on Wednesday, 07 February, 2007 06:59:32 PM

TPINS

The Test Pattern Insertion (TPINS) controls the insertion of test pattern in the outgoing data stream for jitter testing purpose. When this bit is set high, the test pattern stored in the registers (TP[9:0]) is used to replace all the overhead and payload bytes of the output data stream. When TPINS is set low, no test patterns are generated.

FIFOERRE

The FIFO overrun/underrun error interrupt enable bit (FIFOERRE) controls the FIFO overrun interrupt event. An interrupt is generated on a FIFO error event if the FIFOERRE is set to logic 1. No interrupt is generated if FIFOERRE if is set to logic 0.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 06:59:32 PM

Register 1nA1H: T8TE APS Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R	FIFOERRI	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, these interrupt status bits are cleared on write with a logic 1. Otherwise, these interrupt status bits are cleared on read.

FIFOERRI

The FIFO overrun/underrun error interrupt indication bit (FIFOERRI) reports a FIFO overrun/underrun error event. FIFO overrun/underrun errors occur when FIFO logic detects FIFO read and write pointers in close proximity to each other. FIFOERRI is set to logic 1 on a FIFO overrun/underrun error. FIFOERRI is set to logic 0 when the T8TE Interrupt status register is read. This bit does not cause a hardware interrupt on INTB unless the FIFOERRE bit is set high.

Downloaded by Content Team of Element 14 Inc on Wednesday, 07 February, 2007 06:09:32 PM

Register 1nA2H: T8TE APS TelecomBus Mode #1

Bit	Type	Function	Default
Bit 15	R/W	TMODE7[1]	0
Bit 14	R/W	TMODE7[0]	0
Bit 13	R/W	TMODE6[1]	0
Bit 12	R/W	TMODE6[0]	0
Bit 11	R/W	TMODE5[1]	0
Bit 10	R/W	TMODE5[0]	0
Bit 9	R/W	TMODE4[1]	0
Bit 8	R/W	TMODE4[0]	0
Bit 7	R/W	TMODE3[1]	0
Bit 6	R/W	TMODE3[0]	0
Bit 5	R/W	TMODE2[1]	0
Bit 4	R/W	TMODE2[0]	0
Bit 3	R/W	TMODE1[1]	0
Bit 2	R/W	TMODE1[0]	0
Bit 1	R/W	TMODE0[1]	0
Bit 0	R/W	TMODE0[0]	0

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:09:32 PM

Register 1nA3H: T8TE APS TelecomBus Mode #2

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	TMODE11[1]	0
Bit 6	R/W	TMODE11[0]	0
Bit 5	R/W	TMODE10[1]	0
Bit 4	R/W	TMODE10[0]	0
Bit 3	R/W	TMODE9[1]	0
Bit 2	R/W	TMODE9[0]	0
Bit 1	R/W	TMODE8[1]	0
Bit 0	R/W	TMODE8[0]	0

TMODE0[1:0]-TMODE11[1:0]

The TelecomBus mode (TMODE0[1:0]-TMODE11[1:0]) bits contain TelecomBus mode settings for each STS-1 timeslot in the corresponding STS-12 stream. Each STS-1 stream can work in MST, HPT or LPT mode. The setting stored in TMODE**x**[1:0] (**x** can be 0-11) determines which set of TelecomBus control signals are to be encoded in 8B/10B characters. Table below shows the possible configurations for each STS-1 stream:

TMODEx[1:0]	Functional Description
00	MST Mode
01	HPT Mode
10	Reserved
11	Reserved

Downloaded by Content Team of Partminer on Wednesday, 07 February, 2007 06:09:32 PM

Register 1nA4H: T8TE APS Test Pattern

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R/W	TP[9]	1
Bit 8	R/W	TP[8]	0
Bit 7	R/W	TP[7]	1
Bit 6	R/W	TP[6]	0
Bit 5	R/W	TP[5]	1
Bit 4	R/W	TP[4]	0
Bit 3	R/W	TP[3]	1
Bit 2	R/W	TP[2]	0
Bit 1	R/W	TP[1]	1
Bit 0	R/W	TP[0]	0

TP[9:0]

The Test Pattern registers (TP[9:0]) contain the test pattern that is used to insert into the outgoing data stream for jitter test purpose. When the TPINS bit is set high, the test pattern stored in TP[9:0] is used to replace all the overhead and payload bytes of the output data stream.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:09:32 PM

Register 1nA5H: T8TE APS Analog Control

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	TXLV_ENB	0
Bit 7	R/W	PISO_ENB	0
Bit 6	R/W	ATIN[3]	0
Bit 5	R/W	ATIN[2]	0
Bit 4	R/W	ATIN[1]	0
Bit 3	R/W	ATIN[0]	0
Bit 2	R/W	TXLV_ATMSB	1
Bit 1	R/W	PISO_ATMSB	1
Bit 0	R/W	ARSTB	1

ARSTB

The analog reset bit (ARSTB) controls the TXLV and PISO operation. When ARSTB is set low, the TXLV and PISO are reset. This bit must be set to logic 1 for normal operation.

PISO_ATMSB

The PISO analog test mode select bit (PISO_ATMSB) controls the PISO test operation. PISO_ATMSB drives the output PISO_ATMSB pin low to enable test mode in the PISO. This bit must be set to logic 1 for normal operation.

TXLV_ATMSB

The TXLV analog test mode select bit (TXLV_ATMSB) controls the TXLV test operation. TXLV_ATMSB drives the output TXLV_ATMSB pin low to enable test mode in the TXLV block. This bit must be set to logic 1 for normal operation.

ATIN[3:0]

The analog test control inputs (ATIN[3:0]) control the PISO and TXLV test circuitry. These bits are not used for normal operation.

Downloaded by Content Team of Partner Inc on Wednesday, 07 February, 2007 06:09:32 PM

PISO_ENB

The PISO enable bit (PISO_ENB) controls the PISO operation. When set to logic 1, PISO_ENB disables the PISO. When set to logic 0, PISO_ENB enables the PISO.

TXLV_ENB

The TXLV enable bit (TXLV_ENB) controls the TXLV operation. When set to logic 1, TXLV_ENB disables the TXLV. When set to logic 0, TXLV_ENB enables the TXLV.

Reserved

The Reserved bits should be set to logic 0 for proper operation.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 1nA6H: T8TE APS DTB Bus

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	DTBO[0]	0
Bit 6	R/W	DTBO[0]	0
Bit 5	R/W	DTBO[0]	0
Bit 4	R/W	DTBO[0]	0
Bit 3	R	DTBI[3]	X
Bit 2	R	DTBI[2]	X
Bit 1	R	DTBI[1]	X
Bit 0	R	DTBI[0]	X

DTBO[3:0]

The analog wrapper digital test bus output bits (DTB_OUT[3:0]) are used to drive values on the digital test bus (DTB[3:0]). These bits are not used in normal operation.

DTBI[3:0]

The analog wrapper digital test bus input bits (DTB_IN[3:0]) are used to read values from the digital test bus (DTB[3:0]). These bits are not used in normal operation.

Downloaded by Content Team of Partsoner Inc on Wednesday, 07 February, 2007 06:09:32 PM

12.18 SONET/SDH In-band Error Report Processor (SIRP #1 - #4)

There are 4 SIRP (#1 - #4) blocks in 4 STM-16 processing groups with independent register sets. When the S/UNI 9953 is configured for quad OC-48 mode, all four blocks are configured as masters to process the STS-48c/STM-16c data streams. When configured for OC-192 mode, only SIRP #1 is configured as master and the other three (#2 - #4) blocks are inactive and may be considered as slaves.

Register 1kB0H: SIRP Configuration Timeslot

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	TS1_FORCE_LCD	0
Bit 4	R/W	TS1_RDI20F	0
Bit 3	R/W	TS1_ERDI	0
Bit 2	R/W	Reserved	1
Bit 1	R/W	Reserved	1
Bit 0	R/W	TS1_PROV	0

TS1_PROV

TS1_PROV suppresses the flow of data through the SIRP. For proper operation of the S/UNI 9953, the TS1_PROV must be set to 1.

The TS1_ERDI bit selects between normal and extended RDI encoding. When TS1_ERDI is set high, extended RDI is selected. When TS1_ERDI is set low, normal RDI is selected. These selections are summarized in Table 20.

Table 20 SIRP RDI Settings

	ERDI Code	ERDI Interpretation
TS1_ERDI = 1	001	No RDI-P defect
	010	ERDI-P payload defect
	101	ERDI-P server defect
	110	ERDI-P connectivity defect
	000	No RDI-P defect

Downloaded by Content Central on Partminer Inc on Wednesday, 07 February, 2007 06:55:10 PM

	ERDI Code	ERDI Interpretation
TS1_ERDI = 1	001	No RDI-P defect
	010	ERDI-P payload defect
	101	ERDI-P server defect
	110	ERDI-P connectivity defect
TS1_ERDI = 0	000	No RDI-P defect
	100	RDI-P defect
	100	RDI-P defect

TS1_RDI20F

The TS1_RDI20F bits specify the configuration of RDI maintenance duration. The standard required duration is 10 frames. The GR-253 objective duration is 20 frames. The two options are specified by the TS1_RDI20F bit are selected as shown in Table 21.

Table 21 SIRP RDI Maintenance

TS1_RDI20F	Configuration
0	A particular RDI value for will be maintained for the required 10 frames before changing to a lower priority RDI code.
1	A particular RDI value for will be maintained for the GR-253 objective 20 frames before changing to a lower priority RDI code.

TS1_FORCE_LCD

The TS1_FORCE_LCD bit is used to force a Loss of ATM Cell Delineation (LCD) event. A logic OR operation is performed on the LCD indication and the TS1_FORCE_LCD bit. When TS1_FORCE_LCD is set high, an LCD event is assumed and RDI[1:0] is sourced entirely from a specified 2 bit RDI code (LCD[1:0]).

Downloaded by Content Team of Partminer.com on Wednesday, 07 February, 2007 06:59:32 PM

Register 1kBCH: SIRP Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	RDIPRIHI[1]	0
Bit 4	R/W	RDIPRIHI[0]	0
Bit 3	R/W	RDIPRIMID[1]	0
Bit 2	R/W	RDIPRIMID[0]	0
Bit 1	R/W	LCD[1]	1
Bit 0	R/W	LCD[0]	0

LCD[1:0]

The LCD[1:0] bits represent the top two bits of the RDI code generated when a Loss of ATM Cell Delineation (LCD) event is detected. The third bit (LSB) is the inverse of the second (LCD[0]). For proper operation in the S/UNI 9953, this register field must be written 01.

RDIPRIMID[1:0]

The RDIPRIMID[1:0] bits specify which two-bit alarm code point (RDI) will be treated as the second highest priority code. These bits combined with the RDIPRIHI bits allow almost any priority scheme to be specified. The bits are interpreted as shown in RDIPRIH[1:0].

RDIPRIHI[1:0]

The RDIPRIHI[1:0] bits specify which two-bit alarm code point (RDI) will be treated as the highest priority code. High priority codes will replace low priority codes at the next transmit G1 byte, instead of allowing 10/20 copies to be sent. The highest priority alarm is sent 10/20 times before replacement is allowed.

Downloaded by ContentTeam of Rattminer Inc. on Wednesday, 07 February, 2007 06:39:32 PM

Table 22 SIRP RDI Priority Schemes

RDIPRIHI[1:0]	RDIPRIMID[1:0]	Priority of Codes (3 = highest)	
		Code	Priority
11	01	110	3
		010	2
		101	1
		001	0
11	10	110	3
		101	2
		010	1
		001	0
10	11	101	3
		110	2
		010	1
		001	0
10	01	101	3
		010	2
		110	1
		001	0
01	11	010	3
		110	2
		101	1
		001	0
01	10	010	3
		101	2
		110	1
		001	0
00	00	110	1
		101	1
		010	1
		001	0
Other codes	other codes	Reserved	

Note

- When RDIPRIHI[1:0] and RDIPRIMID[1:0] are both equal to b'00, all RDI codes have equal priority except RDI[1:0] = b'00 which always has lowest priority.

12.19 Transmit Cell Frame Processor (TCFP #1 - #4)

There are 4 TCFP (#1 - #4) blocks in 4 STM-16 processing groups with independent register sets. When the S/UNI 9953 is configured for quad OC-48 mode, all four blocks are configured as masters to process the STS-48c/STM-16c data streams. When configured for OC-192 mode, all 4 TCFP (#1 - #4) blocks are inactive. When operating in OC-192 mode, please refer to the TCFP-9953 registers.

Downloaded by Content Team of Parsminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 1kC0H: TCFP Configuration

Bit	Type	Function	Default
Bit 15	R/W	FIFO_ERRE	0
Bit 14	R/W	FIFO_UDRE	0
Bit 13	R/W	XFERE	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	DELINDIS	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	POS_SEL	0
Bit 7	R/W	CRC_SEL[1]	1
Bit 6	R/W	CRC_SEL[0]	1
Bit 5	R/W	FLAG[3]	0
Bit 4	R/W	FLAG[2]	0
Bit 3	R/W	FLAG[1]	0
Bit 2	R/W	FLAG[0]	0
Bit 1	R/W	SCRMBL	1
Bit 0	R/W	PROV	0

PROV

The processor provision bit (PROV) is used to enable the TCFP. When PROV is logic 0, the TCFP ATM and packet processors are disabled and will not request data from the Transmit FIFO interface. When PROV is logic 1, the TCFP ATM or packet processor is enabled and will respond to data requests with valid data after requesting and processing data from the Transmit FIFO interface.

SCRMBL

The SCRMBL bit controls the scrambling of the packet data stream or ATM cell payload. When SCRMBL is a logic 1, scrambling is enabled. When SCRMBL is a logic 0, scrambling is disabled.

FLAG[3:0]

The flag insertion control (FLAG[3:0]) configures the minimum number of flag bytes the packet processor inserts between packets. The minimum number of flags (01111110) inserted between packets is shown in the table below. FLAG[3:0] are used only in POS mode.

Table 23 Selection of the Number of Flag Bytes

FLAG[3:0]	Minimum Number of FLAG Bytes
0000	1 flag

Downloaded by Content Team at Fortmine on Wednesday, 07 February, 2007 06:59:32 PM

FLAG[3:0]	Minimum Number of FLAG Bytes
0001	2 flags
0010	4 flags
0011	8 flags
0100	16 flags
0101	32 flags
0110	64 flags
0111	128 flags
1000	256 flags
1001	512 flags
1010	1024 flags
1011	2048 flags
1100	4096 flags
1101	8192 flags
1110	16384 flags
1111	32768 flags

CRC_SEL[1:0]

The CRC select (CRC_SEL[1:0]) bits allow the control of the CRC calculation according to the table below. For ATM cells, the CRC is calculated over the first four ATM header bytes. For packet applications, the CRC is calculated over the whole packet data, before byte stuffing and scrambling.

Note that CRC_SEL[1:0] = 0x is invalid for ATM mode, as all ATM cells transferred across the PL4 interface must be 52 bytes, and thus a valid HCS needs to be generated.

Table 24 CRC Mode Selection

CRC_SEL[1:0]	HCS Operation (ATM)	FCS Operation (POS)
00	Reserved	No FCS inserted
01	Reserved	No FCS inserted
10	CRC-8 without coset polynomial	CRC-CCITT (2 bytes)
11	CRC-8 with coset polynomial added	CRC-32 (4 bytes)

POS_SEL

The POS_SEL bit enables the POS HDLC frame processing mode. When POS_SEL is set to logic 1, POS processing will occur. When POS_SEL is set to logic 0, ATM mode is selected.

Reserved

The Reserved bits should be set to logic 0 for proper operation.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

DELINDIS

The DELINDIS bit enables the transmission of unmodified POS traffic. When set to logic one in POS mode, flags are not inserted (unless in FIFO underrun) and stuffing is disabled. FCS insertion and scrambling are still controlled by the CRC_SEL and SCRMBL bits.

XFERE

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the transmitted packet/cell counter, transmitted byte counter, and aborted packet counter holding registers. When XFERE is set to logic 1, the interrupt is enabled.

FIFO_UDRE

The FIFO_UDRE bit enables the generation of an interrupt due to a FIFO underrun. When FIFO_UDRE is set to logic 1, the interrupt is enabled and the INTB signal will be set to logic 0 whenever FIFO_UDRI is set to logic 1.

FIFO_ERRE

The FIFO_ERRE bit enables the generation of an interrupt due to a FIFO error. When FIFO_ERRE is set to logic 1, the interrupt is enabled and the INTB signal will be set to logic 0 whenever FIFO_ERRI is set to logic 1.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:07 PM

Register 1kC1H: TCFP Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	FIFO_ERRI	X
Bit 14	R	FIFO_UDRI	X
Bit 13	R	XFERI	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, these interrupt status bits are cleared on a write of logic one. Otherwise, these interrupt status bits are cleared on read.

XFERI

The XFERI bit indicates that a transfer of accumulated counter data has occurred. A logic 1 in this bit position indicates that the transmitted cell/packet counter, transmitted byte counter, and aborted packet counter holding registers have been updated. This update is initiated by writing to one of the TCFP counter register locations, or the S/UNI 9953 Identity, and Global Performance Monitor Update register.

FIFO_UDRI

The FIFO_UDRI bit is set high when an attempt is made to read from the transmit FIFO while it is empty. This is considered a system error.

FIFO_ERRI

This bit is set to one when an error is detected on the read side of the transmit FIFO. An error can be caused by an abnormal sequence of start of packet or end of packet FIFO indications. Such errors are normally caused by a previous FIFO overrun or underrun condition or a user asserted error from the POS-PHY Level 4 interface.

Downloaded by Content Team of Pericom Inc on Wednesday, 07 February, 2007 06:09:32 PM

Note that if a FIFO under-run condition is triggered, then the subsequent aborted packet will not be counted in the aborted packet counter.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 1kC2H: TCFP Idle/Unassigned ATM Cell Header

Bit	Type	Function	Default
Bit 15	R/W	GFC[3]	0
Bit 14	R/W	GFC[2]	0
Bit 13	R/W	GFC[1]	0
Bit 12	R/W	GFC[0]	0
Bit 11	R/W	PTI[2]	0
Bit 10	R/W	PTI[1]	0
Bit 9	R/W	PTI[0]	0
Bit 8	R/W	CLP	1
Bit 7	R/W	PAYLD[7]	0
Bit 6	R/W	PAYLD[6]	1
Bit 5	R/W	PAYLD[5]	1
Bit 4	R/W	PAYLD[4]	0
Bit 3	R/W	PAYLD[3]	1
Bit 2	R/W	PAYLD[2]	0
Bit 1	R/W	PAYLD[1]	1
Bit 0	R/W	PAYLD[0]	0

PAYLD[7:0]

The PAYLD[7:0] (Idle Cell Payload) value reflects the payload bytes which will be inserted into the ATM Idle cell generated by the TCFP.

CLP

The CLP (Cell Loss Priority) bit contains the eighth bit position of the fourth octet of the idle/unassigned cell pattern. Cell rate decoupling is accomplished by transmitting idle cells when the TCFP detects that no outstanding cells are available from the external FIFO and data is requested on the TCFP egress interface. Additionally, XOFF can be used to force the transmission of Idle/Unassigned cells in ATM mode.

PTI[2:0]

The PTI[2:0] (Payload Type) bits contain the fifth, sixth, and seventh bit positions of the fourth octet of the idle/unassigned cell pattern. Idle cells are transmitted when the TCFP detects that no outstanding cells are available from the external FIFO and data is requested on the TCFP egress interface. Additionally, XOFF can be used to force the transmission of Idle/Unassigned cells in ATM mode.

Downloaded by ContentTeam of Datasheet Inc on Wednesday, 07 February, 2007 06:39:32 PM

GFC[3:0]

The GFC[3:0] (Generic Flow Control) bits contain the first, second, third, and fourth bit positions of the first octet of the idle/unassigned cell pattern. Idle/unassigned cells are transmitted when the TCFP detects that no outstanding cells are available from the FIFO and data is requested on the TCFP egress interface. Additionally, XOFF can be used to force the transmission of Idle/Unassigned cells in ATM mode. The all zeros pattern is transmitted in the VCI and VPI fields of the idle/unassigned cell.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 08:37:02 PM

Register 1kC3H: TCFP Diagnostics

Bit	Type	Function	Default
Bit 15	R/W	DCRC[7]	0
Bit 14	R/W	DCRC[6]	0
Bit 13	R/W	DCRC[5]	0
Bit 12	R/W	DCRC[4]	0
Bit 11	R/W	DCRC[3]	0
Bit 10	R/W	DCRC[2]	0
Bit 9	R/W	DCRC[1]	0
Bit 8	R/W	DCRC[0]	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	TX_BYTE_MODE	0
Bit 4	R/W	XOFF	0
Bit 3	R/W	INVERT	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

Reserved

The Reserved bits should be set to their default values for proper operation.

INVERT

The data inversion bit (INVERT) configures the ATM or packet processor to logically invert the outgoing data stream. When INVERT is set to logic 1, the outgoing data stream is logically inverted. The outgoing data stream is not inverted when INVERT is set to logic 0.

XOFF

The XOFF serves as a transmission enable bit. When XOFF is set to logic 0, ATM cells or packets are transmitted normally. When XOFF is set to logic 1, the cell or packet currently being transmitted is completed and transmission is then suspended. When XOFF is set to logic 1, the TCFP will not request data from the FIFO. ATM Idle cells or HDLC flags will be sent on the TCFP egress interface. During the time at which the XOFF bit is set or cleared, data from other cells or packets may still reside within the TCFP internal FIFOs, and thus the TCFP counts may not be accurate.

Downloaded by Cortest Kft. of Partner Inc on Wednesday, 07 February, 2007 06:09:32 PM

TX_BYTE_MODE

The transmit byte counter mode (TX_BYTE_MODE) bit is used to select the mode in which the TX_BYTE[39:0] counters work. When TX_BYTE_MODE is logic 0, TX_BYTE[39:0] will count all bytes in transmitted packets (including FCS and Abort EOP bytes) before the byte stuffing operation. When TX_BYTE_MODE is logic 1, TX_BYTE[39:0] will count all bytes in transmitted packets (including FCS, Abort EOP, and stuff bytes) after the byte stuffing operation. Flag bytes will not be counted in either case. The TX_BYTE_MODE bit is only valid when working in POS mode.

DCRC[7:0]

The diagnostic CRC word (DCRC[7:0]) configures the ATM or packet processor to logically invert bits in the inserted CRC on the outgoing data stream for diagnostic purposes. When any bit in DCRC[7:0] is set to logic 1, the corresponding bit in the FCS value inserted by the POS processor or the HCS value inserted by the ATM processor is logically inverted. DCRC[7:0] is ignored when no FCS is inserted. Each DCRC[x] bit will cause a bit error in each byte of the 2 byte or 4 byte FCS.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 03:09:12 PM

Register 1kC4H: TCFP Transmit Cell/Packet Counter (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	TX_CELL[15:0]	XXXX

Register 1kC5H: TCFP Transmit Cell/Packet Counter (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	TX_CELL[31:16]	XXXX

TX_CELL[31:0]

The TX_CELL[31:0] bits indicate the number of cells or non-aborted packets transmitted during the last accumulation interval. ATM Idle cells, HDLC flags, and HDLC Abort bytes inserted into the transmission stream are not counted.

A write to any one of the TCFP Transmit Cell/Packet Counter registers or to the S/UNI 9953 Identity, and Global Performance Monitor Update register loads the registers with the current counter value and resets the internal 32 bit counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the Transmit Cell/Packet Counter registers. The counter should be polled regularly to avoid saturation..

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007, 06:59:32 PM

Register 1kC6H: TCFP Transmit Byte Counter (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	TX_BYTE[15:0]	XXXX

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 1kC7H: TCFP Transmit Byte Counter

Bit	Type	Function	Default
Bit 15 to Bit 0	R	TX_BYTE[31:16]	XXXX

Register 1kC8H: TCFP Transmit Byte Counter (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 8	—	Unused	XX
Bit 7 to Bit 0	R	TX_BYTE[39:32]	XX

TX_BYTE[39:0]

The TX_ BYTE[39:0] bits indicate the number of bytes in packets transmitted during the last accumulation interval. The byte counts include all user payload bytes, FCS bytes, and abort EOP bytes. Inclusion of stuffed bytes is controlled by the TX_BYTE_MODE register bit. HDLC flags are not counted. The TX_BYTE[39:0] counters are only valid when processing packets.

A write to any one of the TCFP counter registers loads the registers or to the S/UNI 9953 Identity, and Global Performance Monitor Update register with the current counter value and resets the internal 40 bit counter to between 0 and 8. The counter reset value is dependent on if there were count events during the transfer of the count to the Transmit Byte Counter registers. The counter should be polled regularly to avoid saturation.

Downloaded by Content Team of Partminer at Wednesday, 07 February, 2007, 06:59:32 PM

Register 1kC9H: TCFP Aborted Packet Counter

Bit	Type	Function	Default
Bit 15 to Bit 0	R	TX_ABT[15:0]	XXXX

TX_ABT[15:0]

The TX_ ABT[15:0] bits indicate the number of aborted packets transmitted during the last accumulation interval. These counters are only valid when in POS mode.

A write to any one of the TCFP counter registers or to the S/UNI 9953 Identity, and Global Performance Monitor Update register loads the registers with the current counter value and resets the internal 16 bit counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the Transmit Byte Counter registers. The counter should be polled regularly to avoid saturation.

Note that if a FIFO under-run condition is triggered, then the subsequent aborted packet will not be counted in the aborted packet counter. Additionally, the aborted underrun packet is counted as a regular TX_CELL packet. The abort byte is not counted in the TX_BYTE count. When the rest of the packet arrives, its bytes along with the generated CRC bytes are counted in the TX_BYTE counts.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 March, 2007 06:59:32 PM

12.20 Receive Cell Frame Processor (OC-192) (RCFP-9953)

Register 2020H: RCFP-9953 Configuration

Bit	Type	Function	Default
Bit 15	R/W	IDLEPASS	0
Bit 14	R/W	RBY_MODE	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	MODE[1]	0
Bit 10	R/W	MODE[0]	0
Bit 9	R/W	INVERT	0
Bit 8	R/W	CORE_DC	0
Bit 7	R/W	CRCPASS	0
Bit 6	R/W	CRC_SEL[4]	1
Bit 5	R/W	CRC_SEL[3]	1
Bit 4	R/W	CRC_SEL[2]	1
Bit 3	R/W	CRC_SEL[1]	1
Bit 2	R/W	CRC_SEL[0]	1
Bit 1	R/W	DESCRMBL	1
Bit 0	R/W	PROV	0

PROV

The processor provision bit (PROV) is used to enable the RCFP_9953. When PROV is logic 0, the RCFP-9953 DELINDIS, ATM, GFP and POS processors are disabled and will not transfer any valid data. When PROV is logic 1, the RCFP-9953 DELINDIS, ATM, GFP or POS processors are enabled and will process the incoming data.

Note: when the state of PROV is changed, the processing of the data stream is started or terminated immediately. The data stream is not delineated in a graceful manner.

DESCRMBL

The DESCRMBL bit controls the descrambling of the DELINDIS data stream, POS data stream, GFP frame payload and FCS or ATM cell payload with the polynomial $x^{43}+1$. When DESCRMBL is set to logic 0, packet, frame and cell payload descrambling is disabled. When DESCRMBL is set to logic 1, packet, frame and cell payload descrambling is enabled.

Downloaded by Cores Team of Pakmicro.com on Wednesday, 07 February, 2007 06:59:32 PM

CRC_SEL[4:0]

The CRC select (CRC_SEL[4:0]) bits allow the control of the CRC calculation according to the table below. In ATM mode the CRC is calculated over the first four ATM header bytes. In POS mode the CRC is calculated over the whole packet data, after byte destuffing and descrambling. In GFP mode the CRC is calculated over the Core, Payload header bytes, OAM payload and FCS, dependent on the configured framing format.

Note that in accordance with the register table, the reserved CRC_SEL bits must be left in their default state of logic 1, for normal operation.

Table 25 Functionality of the CRC_SEL[4:0] Register Bit

Mode	CRC_SEL[4]	CRC_SEL[3]	CRC_SEL[2]	CRC_SEL[1]	CRC_SEL[0]
ATM	Reserved	Reserved	Reserved	0 - No COSET 1 - COSET	0 – No HCS 1 - HCS
POS	Reserved	Reserved	Reserved	Reserved	0 – No FCS 1 - FCS
GFP	0 – No FCS 1 - FCS	0 - No_sHEC 1 - sHEC	0 – No eHEC 1 – eHEC	0 – No tHEC 1 tHEC	0 – No cHEC 1 – cHEC

CRCPASS

The CRCPASS bit controls the dropping of ATM cells and POS packets based on the detection of an incorrect HCS/FCS.

When in ATM mode and when CRCPASS is a logic 0, cells containing an uncorrectable HCS error are dropped and the HCS verification state machine transitions to the 'Detection Mode'.

When CRCPASS is logic 1, cells are passed to the external downstream block interface regardless of errors detected in the HCS. Additionally, the HCS verification finite state machine never exits the SYNC state ('Correction Mode'), and hence will never lose cell delineation. Note that HCS errors are still counted.

ATM idle cells that contain HCS errors will cause the state machine to change state regardless of the setting of the IDLEPASS register bit.

In POS mode and CRCPASS is logic 1, packets with FCS errors are not marked as such and are passed to the external downstream block interface as if no FCS error occurred. Note however that these packets are still counted as FCS errors. When CRCPASS is logic 0, then packets with FCS errors are marked.

This configuration bit is ignored in GFP mode.

Downloaded by Control Team of datasheetq.com on Wednesday, 07 February, 2007 06:56:22 PM

CORE_DC

In GFP mode the CORE_DC bit controls whether the core header bytes are EXORed with the 4-byte DC balance code. The EXOR operation takes place when this bit is set to logic 1.

This configuration bit is ignored in DELINDIS, ATM and POS modes.

INVERT

The data inversion bit (INVERT) configures the processor to logically invert the incoming data stream. When INVERT is set to logic 1, the data stream is logically inverted before processing. When INVERT is set to logic 0, the data stream is not inverted before processing. The use of this configuration bit is independent of the RCFP-9953 mode.

MODE[1:0]

The MODE[1:0] bits select the operational mode of the RCFP_9953.

Table 26 Operational Mode

MODE[1:0]	RCFP Operational Mode
00	DELINDIS
01	ATM
10	POS
11	GFP

RBY_MODE

The receive byte counter mode (RBY_MODE) bit is used to select the mode in which the RBY_IC[39:0] counters work. When RBY_MODE is logic 0, RBY_IC[39:0] will count all bytes in received POS packets, (including FCS and Abort bytes), after the byte destuffing operation. When RBY_MODE is logic 1, RBY_IC[39:0] will count all bytes in received POS packets (including FCS, Abort, and stuff bytes) before the byte destuffing operation. Flag bytes will not be counted in either case. The RBY_MODE bit is only valid in POS mode.

IDLEPASS

In ATM mode the IDLEPASS bit controls the function of the Idle Cell filter. When IDLEPASS is written with logic 0, all cells that match the Idle Cell Header Pattern and Idle Cell Header Mask are filtered out. When IDLEPASS is enabled, the Idle Cell Header Pattern and Mask registers are ignored. The default state of this bit and the bits in the Idle Cell Header Mask and Idle Cell Header Pattern Registers enable the dropping of Idle cells.

This configuration bit is ignored in DELINDIS, POS and GFP modes.

Downloaded by Content Team of Datasheet Inc on Wednesday, 07 February 2007 06:59:32 AM

Register 2021H: RCFP-9953 Interrupt Enable and Status

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R	OCDV	X
Bit 12	R	LCDV	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	GFP_FCSE	X
Bit 9	R/W	SHECE	X
Bit 8	R/W	THEC_EHECE	0
Bit 7	R/W	MINLE	0
Bit 6	R/W	MAXLE	0
Bit 5	R/W	ABRTE	0
Bit 4	R/W	XFERE	0
Bit 3	R/W	CCRCE	0
Bit 2	R/W	UCRCE	0
Bit 1	R/W	OCDE	0
Bit 0	R/W	LCDE	0

LCDE

The LCDE bit enables the generation of an interrupt due to a change in the ATM or GFP Loss of Cell/Frame Delineation state. When LCDE is set to logic 1, the interrupt is enabled.

OCDE

The OCDE bit enables the generation of an interrupt due to a change in ATM/GFP cell/frame delineation state or POS packet in/out of frame alignment. When OCDE is set to logic 1, the interrupt is enabled.

UCRCE

The UCRCE bit enables the generation of an interrupt due to the detection of an uncorrectable ATM HCS, GFP cHEC or POS FCS error. When UCRCE is set to logic 1, the interrupt is enabled.

CCRCE

The CCRCE bit enables the generation of an interrupt due to the detection of a correctable, (i.e. single bit), GFP cHEC error. When CCRCE is set to logic 1, the interrupt is enabled. Note this bit is not valid in POS or ATM modes.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

XFERE

The XFERE bit enables the generation of an interrupt when a performance monitor counter update is completed and new values are stored in the RCFP-9953 performance monitor counter holding registers. When XFERE is set to logic 1, the interrupt is enabled.

ABRTE

The Abort Packet Enable bit enables the generation of an interrupt due to the reception of an aborted packet when in POS mode. When ABRTE is set to logic 1, the interrupt is enabled.

MAXLE

The Maximum Length Packet Enable bit enables the generation of an interrupt due to the reception of a POS packet or GFP frame exceeding the programmable maximum packet/frame payload length. When MAXLE is set to logic 1, the interrupt is enabled.

MINLE

The Minimum Length Packet Enable bit enables the generation of an interrupt due to the reception of a POS packet or GFP frame that is smaller than the programmable minimum packet/frame length. When MINLE is set to logic 1, the interrupt is enabled.

THEC_EHECE

The THEC/EHECE bit enables the generation of an interrupt due to the detection of an GFP THEC or eHEC error. When THEC_EHECE is set to logic 1, the interrupt is enabled.

SHECE

The SHECE bit enables the generation of an interrupt due to the detection of a GFP OAM sHEC error. When SHECE is set to logic 1, the interrupt is enabled.

GFP_FCSE

The GFP_FCSE bit enables the generation of an interrupt due to the detection of a GFP FCS error. When GFP_FCSE is set to logic 1, the interrupt is enabled.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:02 PM

LCDV

The LCDV bit gives the ATM or GFP Loss of Cell/Frame Delineation state. When LCDV is logic 1, an out of cell/frame delineation (OCD) defect has persisted for the number of cells or TCLKX2 cycles specified in the LCD Count Threshold register. When LCDV is logic 0, the RCFP-9953 has been in cell/frame delineation for the number of cells or TCLKX2 cycles specified in the LCD Count Threshold register. The number of cell or TCLKX2 time periods can be varied by using the LCDC[10:0] register bits in the RCFP-9953 LCD Count Threshold register.

OCDV

The OCDV bit indicates when the ATM/GFP delineation or POS packet framer are out of alignment. When OCDV is logic 1, the ATM/GFP delineation state machine is in the 'HUNT' or 'PRESYNC' states and is hunting for the cell/frame boundaries or the POS packet processor is out of frame alignment. When OCDV is logic 0, the ATM/GFP delineation state machine is in the 'SYNC' state and cells/frames are being passed through to the downstream block or the POS packet processor is in frame alignment, (i.e. detected the first SOP).

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 10:53:22 AM

Register 2022H: RCFP-9953 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	Reserved	X
Bit 14	R	Reserved	X
Bit 13	R	Reserved	X
Bit 12	R	Reserved	X
Bit 11	R	Reserved	X
Bit 10	R	GFP_FCSI	X
Bit 9	R	SHECI	X
Bit 8	R	THEC_EHECI	X
Bit 7	R	MINLI	X
Bit 6	R	MAXLI	X
Bit 5	R	ABRTI	X
Bit 4	R	XFERI	X
Bit 3	R	CCRCI	X
Bit 2	R	UCRCI	X
Bit 1	R	OCDI	X
Bit 0	R	LCDI	X

Note that the RCFP-9953 interrupts are set to logic one when an event occurs.

If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, these interrupt status bits are cleared on write with a logic 1. Otherwise, these interrupt status bits are cleared on read.

LCDI

The LCDI bit is set to logic 1 when there is a change in the loss of cell/frame delineation (LCD) state. The current value of the LCD state is available through the LCDV bit in register 5. This interrupt can be masked using LCDE.

OCDI

The OCDI bit is set to logic 1 when the ATM/GFP delineation state machine enters or exits the SYNC state or the POS framing processor enters or exits the frame alignment state. The current value of the out-of-delineation state or Out-of-frame-alignment State is available in the OCDV bit in RCFP-9953 Interrupt Enable and Status. This interrupt can be masked using OCDE.

UCRCI

The UCRCI bit is set to logic 1 when an uncorrectable ATM HCS, an uncorrectable GFP cHEC or POS packet FCS error are detected. This interrupt can be masked using UCRCE.

Downloaded by Conexant Systems of Planner Inc on Wednesday, 07 February, 2007 06:59:32 PM

CCRCI

The CCRCI bit is set to logic 1 when a correctable GFP cHEC is detected. This interrupt can be masked using CCRCE.

XFERI

The XFERI bit indicates that a transfer of accumulated counter data has occurred. Logic 1 in this bit position indicates that the RCFP-9953 performance monitor counter holding registers have been updated. This update is initiated by writing to one of the counter register locations, or by a microprocessor write to the S/UNI 9953 Identity and Global Performance Monitor Update register (0000H). This interrupt can be masked using XFERE.

ABRTI

The ABRTI bit indicates the generation of an interrupt due to the reception of an aborted POS packet. This interrupt can be masked using ABRTE.

MAXLI

The MAXLI bit indicates an interrupt due to the reception of a GFP or POS frame/packet exceeding the programmable maximum length. This interrupt can be masked using MAXLE.

MINLI

The MINLI bit indicates an interrupt due to the reception of a GFP or POS frame/packet that is smaller than the programmable minimum length. This interrupt can be masked using MINLE.

THEC_EHECI

The THEC_EHECI bit is set to logic 1 when a GFP tHEC or eHEC error is detected. This interrupt can be masked using THEC_EHECE.

SHECI

The SHECI bit is set to logic 1 when a GFP OAM sHEC error is detected. This interrupt can be masked using SHECE.

GFP_FCSI

The GFP_FCSI bit is set to logic 1 when a GFP FCS error is detected. This interrupt can be masked using GFP_FCSE.

Downloaded by Content Team of Partminer Inc on Wednesday, 7 February 2007 06:59:32 PM

Register 2023H: RCFP-9953 Min-Max Length/Bit Order/FCS Strip/Byte Count

Bit	Type	Function	Default
Bit 15	R/W	MINPL[7]	0
Bit 14	R/W	MINPL[6]	0
Bit 13	R/W	MINPL[5]	0
Bit 12	R/W	MINPL[4]	0
Bit 11	R/W	MINPL[3]	1
Bit 10	R/W	MINPL[2]	0
Bit 9	R/W	MINPL[1]	0
Bit 8	R/W	MINPL[0]	0
Bit 7	R/W	STRIP_SEL	0
Bit 6	R/W	RXOTYP	0
Bit 5	R/W	MAXPL[0]	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	0

MAXPL[0]

The Maximum Packet Length (MAXPL[0]) bit is used to set the LSB value of the maximum allowed POS/GFP packet/frame payload length. The higher order bits are located in RCFP-9953 Maximum Packet/Frame Length register.

RXOTYP

In POS mode, the RXOTYP bit determines if an alarm signal will stop a packet by simply asserting EOP, (RXOTYP set to logic 0), or by asserting EOP Abort, (RXOTYP set to logic 1). When RXOTYP is set to logic 0, premature termination of the packet will result in that packet failing a FCS check.

This configuration bit is ignored in all other modes.

Downloaded by Content Team of Datasheet Inc. Wednesday, 07 February, 2007 06:59:32 PM

STRIP_SEL

In POS mode the indirect Frame Check Sequence stripping bit (STRIP_SEL) selects the FCS stripping mode of the RCFP_9953. When set to logic 1, FCS stripping is enabled. For stripping to be enabled in POS mode CRC_SEL[0] must be set to logic 1, (i.e. checking FCS). When stripping is enabled the received packet FCS bytes are discarded within the RCFP_9953. When STRIP is disabled the received packet FCS bytes are transferred over the downstream block.

This configuration bit is ignored in DELINDIS, GFP and ATM modes.

MINPL[7:0]

The Minimum Packet Length (MINPL[7:0]) bits are used to set the minimum POS and GFP packet/frame payload lengths. POS packets and GFP frame payload smaller than this length are marked with an error when transferred to the downstream block. Note that delineated byte streams less than 8-bytes long are counted here and internally discarded.

In POS mode the packet length used is defined as the number of bytes encapsulated into the POS frame excluding byte stuffing and including the FCS bytes.

In GFP mode the length used is defined as the number of bytes encapsulated into the frame payload only, excluding the core and extended header lengths.

The default minimum POS packet and GFP frame lengths are eight bytes. Values smaller than the default are invalid and will be treated as 8 bytes.

Downloaded by Content Team of Partminer Inc (We bought it on February, 2007 08:58:02 AM

Register 2024H: RCFP-9953 Maximum Packet/Frame Length

Bit	Type	Function	Default
Bit 15	R/W	MAXPL[16]	0
Bit 14	R/W	MAXPL[15]	0
Bit 13	R/W	MAXPL[14]	0
Bit 12	R/W	MAXPL[13]	0
Bit 11	R/W	MAXPL[12]	0
Bit 10	R/W	MAXPL[11]	0
Bit 9	R/W	MAXPL[10]	1
Bit 8	R/W	MAXPL[9]	1
Bit 7	R/W	MAXPL[8]	0
Bit 6	R/W	MAXPL[7]	0
Bit 5	R/W	MAXPL[6]	0
Bit 4	R/W	MAXPL[5]	0
Bit 3	R/W	MAXPL[4]	0
Bit 2	R/W	MAXPL[3]	0
Bit 1	R/W	MAXPL[2]	0
Bit 0	R/W	MAXPL[1]	0

MAXPL[16:1]

The Maximum Packet Length (MAXPL[16:0]) bits are used to set the maximum allowed POS/GFP packet/frame payload length. MAXPL[16:1] are configurable using this register and MAXPL[0] which is located in RCFP-9953 Min-Max Length/Bit Order/FCS Strip/Byte Count register. Values entered less that 8 are internally forced equal to 8.

In POS mode, packets larger than this length are terminated and marked with an error. The remainder of the packet is discarded. The packet length used here is defined as the number of bytes encapsulated into the POS frame (bytes between flags, including FCS bytes) after the destuffing operation.

In GFP mode, frame payloads larger than this length are marked with an error. The frame length used here is defined as the number of bytes encapsulated into the frame payload only, excluding the core and extended header lengths.

Note that errored packets or frames will result in an EOP_ABORT at the PL4 interface.

The default maximum packet/frame length is 1536 bytes.

Downloaded by Content Team of Navaner Inc. on Wednesday, 07 February, 2007 06:59:32 PM

Register 2025H: RCFP-9953 LCD Count Threshold

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	OAM_DISCARD	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	LCDC[10]	0
Bit 9	R/W	LCDC[9]	0
Bit 8	R/W	LCDC[8]	1
Bit 7	R/W	LCDC[7]	0
Bit 6	R/W	LCDC[6]	1
Bit 5	R/W	LCDC[5]	1
Bit 4	R/W	LCDC[4]	0
Bit 3	R/W	LCDC[3]	1
Bit 2	R/W	LCDC[2]	0
Bit 1	R/W	LCDC[1]	0
Bit 0	R/W	LCDC[0]	0

LCDC[10:0]

The LCDC[10:0] bits represent the number of consecutive cell/TCLKX2 periods the receive cell/frame processor must be out of cell/frame delineation before loss of cell/frame delineation (LCD) is declared. Likewise, LCD is not reset to logic 0 until the HCS/cHEC delineation state machine is in SYNC for the number of cell/TCLKX2 periods specified by LCDC[10:0].

The default value of LCD[10:0] is 360, which in ATM mode translates to the following, given a 77.76MHz TCLK:

Table 27 Average Cell Period vs. STS Rate

Format	Average Cell Period	Default LCD Integration Period
STS-192c	44.2 ns	15.9 μs

OAM_DISCARD

The GFP OAM Frame Discard (OAM_DISCARD) bit is used to set the internal discarding of GFP OAM frames. OAM DISCARD is enabled when set to logic 1. When set to logic 0 OAM frames are transferred to the downstream block.

Downloaded by Content Team of Pantiner Inc. on Wednesday, 07 February, 2007 06:59:32 PM

Register 2026H: RCFP-9953 Idle Cell Header and Mask/eHEC Length and GFP Delineation

Bit	Type	Function	Default
Bit 15	R/W	GFC[3] /EHDR_LEN[5]	0
Bit 14	R/W	GFC[2] /EHDR_LEN[4]	0
Bit 13	R/W	GFC[1] /EHDR_LEN[3]	0
Bit 12	R/W	GFC[0] /EHDR_LEN[2]	0
Bit 11	R/W	PTI[2] /EHDR_LEN[1]	0
Bit 10	R/W	PTI[1] /EHDR_LEN[0]	0
Bit 9	R/W	PTI[0]	0
Bit 8	R/W	CLP	1
Bit 7	R/W	MGFC[3]	1
Bit 6	R/W	MGFC[2]	1
Bit 5	R/W	MGFC[1]	1
Bit 4	R/W	MGFC[0]	1
Bit 3	R/W	MPTI[2]	1
Bit 2	R/W	MPTI[1]	1
Bit 1	R/W	MPTI[0]	1
Bit 0	R/W	MCLP	1

MCLP

In ATM mode the MCLP bit contains the mask pattern for the eighth bit of the fourth octet of the 53-octet cell. This mask is applied to the Idle Cell Header field to select the bits included in the cell filter. Logic 1 in this bit position enables the CLP bit to be compared. Logic 0 causes the masking of the CLP bit. The default enables the register bit comparison.

MPTI[2:0]

In ATM mode the MPTI[2:0] bits contain the mask pattern for the fifth, sixth, and seventh bits of the fourth octet of the 53-octet cell. This mask is applied to the Idle Cell Header field to select the bits included in the cell filter. A logic 1 in any bit position enables the corresponding PTI[2:0] bits to be compared. A logic 0 causes the masking of the corresponding bit. The default enables the register bit comparison.

MGFC[3:0]

In ATM mode the MGFC[3:0] bits contain the mask pattern for the first, second, third, and fourth bits of the first octet of the 53-octet cell. This mask is applied to the Idle Cell Header field to select the bits included in the cell filter. Logic 1 in any bit position enables the corresponding GFC[3:0] bits to be compared. Logic 0 causes the masking of the corresponding bit. The default enables the register bit comparison.

Downloaded by Content Team (Optimized) on Wednesday, 07 February, 2007 06:59:32 PM

CLP

In ATM mode the CLP bit contains the pattern to match in the eighth bit of the fourth octet of the 53-octet cell, in conjunction with the MCLP register bit. The IDLEPASS bit in the Configuration Register must be set to logic 0 to enable dropping of cells matching this pattern.

PTI[2:0]

In ATM mode the PTI[2:0] bits contain the pattern to match in the fifth, sixth, and seventh bits of the fourth octet of the 53-octet cell, in conjunction with the MPTI[2:0] register bits. The IDLEPASS bit in the Configuration Register must be set to logic 0 to enable dropping of cells matching this pattern.

GFC[3:0]

In ATM mode the GFC[3:0] bits contain the pattern to match in the first, second, third, and fourth bits of the first octet of the 53-octet cell, in conjunction with the MGFC[3:0] register bits. The IDLEPASS bit in the Configuration Register must be set to logic 0 to enable dropping of cells matching this pattern.

Note: an all-zeros pattern must be present in the VPI and VCI fields of the Idle or Unassigned cell.

EHDR_LEN[5:0]

In GFP mode the EHDR_LEN[5:0] bits contain the length of the Extension Header field. A length of zero implies there is no Extension Header field present. A length of one or two is an illegal configuration and disables eHEC verification. The maximum extended header length is 60 bytes. Values set greater than this length are internally set to a maximum value of 60 bytes.

Downloaded by Content Team of Partmaster on Wednesday, 07 February 2007 06:59:32 AM

Register 2027H: RCFP-9953 Receive Byte/Idle Cell-Packet-Frame Counter (LSB)

Bit	Type	Function	Default
Bit 15	R	RBY_ICF[15]	X
Bit 14	R	RBY_ICF[14]	X
Bit 13	R	RBY_ICF[13]	X
Bit 12	R	RBY_ICF[12]	X
Bit 11	R	RBY_ICF[11]	X
Bit 10	R	RBY_ICF[10]	X
Bit 9	R	RBY_ICF[9]	X
Bit 8	R	RBY_ICF[8]	X
Bit 7	R	RBY_ICF[7]	X
Bit 6	R	RBY_ICF[6]	X
Bit 5	R	RBY_ICF5]	X
Bit 4	R	RBY_ICF[4]	X
Bit 3	R	RBY_ICF[3]	X
Bit 2	R	RBY_ICF2]	X
Bit 1	R	RBY_ICF[1]	X
Bit 0	R	RBY_ICF[0]	X

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 2028H: RCFP-9953 Receive Byte/Idle Cell-Packet-Frame Counter (ISB)

Bit	Type	Function	Default
Bit 15	R	RBY_ICF[31]	X
Bit 14	R	RBY_ICF[30]	X
Bit 13	R	RBY_ICF[29]	X
Bit 12	R	RBY_ICF[28]	X
Bit 11	R	RBY_ICF[27]	X
Bit 10	R	RBY_ICF[26]	X
Bit 9	R	RBY_ICF[25]	X
Bit 8	R	RBY_ICF[24]	X
Bit 7	R	RBY_ICF[23]	X
Bit 6	R	RBY_ICF[22]	X
Bit 5	R	RBY_ICF[21]	X
Bit 4	R	RBY_ICF[20]	X
Bit 3	R	RBY_ICF[19]	X
Bit 2	R	RBY_ICF[18]	X
Bit 1	R	RBY_ICF[17]	X
Bit 0	R	RBY_ICF[16]	X

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 2029H: RCFP-9953 Receive Byte/Idle Cell-Packet-Frame Counter (MSB) and GFP FCS Error

Bit	Type	Function	Default
Bit 15	R	GFP_FCS_ERR[7]	X
Bit 14	R	GFP_FCS_ERR[6]	X
Bit 13	R	GFP_FCS_ERR[5]	X
Bit 12	R	GFP_FCS_ERR[4]	X
Bit 11	R	GFP_FCS_ERR[3]	X
Bit 10	R	GFP_FCS_ERR[2]	X
Bit 9	R	GFP_FCS_ERR[1]	X
Bit 8	R	GFP_FCS_ERR[0]	X
Bit 7	R	RBY_ICF[39]	X
Bit 6	R	RBY_ICF[38]	X
Bit 5	R	RBY_ICF[37]	X
Bit 4	R	RBY_ICF[36]	X
Bit 3	R	RBY_ICF[35]	X
Bit 2	R	RBY_ICF[34]	X
Bit 1	R	RBY_ICF[33]	X
Bit 0	R	RBY_ICF[32]	X

RBY_ICF[39:0]

In POS mode the RBY_ICF[39:0] bits indicate the number of bytes received within POS packets during the last accumulation interval. The byte count includes all user payload bytes, FCS bytes and abort bytes. The RBY_MODE register bit controls inclusion of stuffed bytes in the count. HDLC flags are not counted.

In ATM and GFP modes the RBY_ICF[39:0] bits indicate the number of Idle cells/frames received in the last accumulation interval.

A write to any one of the RCFP-9953 performance monitor counter registers loads the registers with the current counter value and resets the internal 40-bit counter to a value between 0 and 8. The counter reset value is dependent on the number of count events during the transfer of the register contents to the RCFP performance monitor Counter registers. The counter should be polled regularly to avoid saturating.

This counter can also be loaded by a microprocessor write to the S/UNI 9953 Identity and Global Performance Monitor Update register (0000H).

Downloaded by Content Team Partner on Wednesday, 07 February, 2007 06:59:32 PM

GFP_FCS_ERR[7:0]

In GFP mode the GFP_FCS_ERR[7:0] bits indicate the number of frames received with FCS errors during the last accumulation interval.

A write to any one of the RCFP_9953 performance monitor counter registers loads the registers with the current counter value and resets the internal 8 bit counter to a value between 0 and 8. The counter reset value is dependent on the number of count events during the transfer of the register contents to the RCFP performance monitor Counter registers. The counter should be polled regularly to avoid saturating.

This counter can also be loaded by a microprocessor write to the S/UNI 9953 Identity and Global Performance Monitor Update register (0000H).

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 09:09:32 PM

Register 202AH: RCFP-9953 Receive Packet/Cell/Frame Counter (LSB)

Bit	Type	Function	Default
Bit 15	R	RX_PCF[15]	X
Bit 14	R	RX_PCF[14]	X
Bit 13	R	RX_PCF[13]	X
Bit 12	R	RX_PCF[12]	X
Bit 11	R	RX_PCF[11]	X
Bit 10	R	RX_PCF[10]	X
Bit 9	R	RX_PCF[9]	X
Bit 8	R	RX_PCF[8]	X
Bit 7	R	RX_PCF[7]	X
Bit 6	R	RX_PCF[6]	X
Bit 5	R	RX_PCF[5]	X
Bit 4	R	RX_PCF[4]	X
Bit 3	R	RX_PCF[3]	X
Bit 2	R	RX_PCF[2]	X
Bit 1	R	RX_PCF[1]	X
Bit 0	R	RX_PCF[0]	X

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 202BH: RCFP-9953 Receive Packet/Cell/Frame Counter (MSB)

Bit	Type	Function	Default
Bit 15	R	RX_PCF[31]	X
Bit 14	R	RX_PCF[30]	X
Bit 13	R	RX_PCF[29]	X
Bit 12	R	RX_PCF[28]	X
Bit 11	R	RX_PCF[27]	X
Bit 10	R	RX_PCF[26]	X
Bit 9	R	RX_PCF[25]	X
Bit 8	R	RX_PCF[24]	X
Bit 7	R	RX_PCF[23]	X
Bit 6	R	RX_PCF[22]	X
Bit 5	R	RX_PCF[21]	X
Bit 4	R	RX_PCF[20]	X
Bit 3	R	RX_PCF[19]	X
Bit 2	R	RX_PCF[18]	X
Bit 1	R	RX_PCF[17]	X
Bit 0	R	RX_PCF[16]	X

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

RX_PCF[31:0]

In POS and GFP modes the RX_PCF[31:0] bits indicate the number of good packets/frames passed to the downstream block during the last accumulation interval. A good packet/frame is one whose EOP byte is not ERRED.

Note: the definition of a good packet/frame depends on the configured testing that it is performing on the data stream. A good packet is one that has passed all the configured POS checks such as length and FCS. Similarly a good frame is one that has passed all the configured GFP checks such as cHEC, eHEC and length.

In ATM mode the RX_PCF[31:0] bits indicate the number of ATM cells passed to the downstream block interface in the last accumulation interval. Any received cells that are dropped, such as uncorrectable HCS errors or Idle cell filtering, are not included in this count.

A write to any one of the RCFP-9953 performance monitor Counter registers loads the registers with the current counter value and resets the internal 32-bit counter to a value between 0 and 2. The counter reset value is dependent on the number of count events during the transfer of the register contents to the RCFP-9953 performance monitor Counter registers. The counter should be polled regularly to avoid saturating. The contents of these registers are valid three TCLK cycles after a transfer is triggered by a write to any of the RCFP-9953 performance monitor registers.

This counter can also be loaded by a microprocessor write to the S/UNI 9953 Identity and Global Performance Monitor Update register (0000H).

Downloaded by Content Team of Partminer Inc on Wednesday, 7 February 2001 @ 05:59:32 PM

Register 202CH: RCFP-9953 Receive Errored FCS/HCS/cHEC Counter

Bit	Type	Function	Default
Bit 15	R	EFCS[15]/CHEC[7]	X
Bit 14	R	EFCS[14]/CHEC[6]	X
Bit 13	R	EFCS[13]/CHEC[5]	X
Bit 12	R	EFCS[12]/CHEC[4]	X
Bit 11	R	EFCS[11]/CHEC[3]	X
Bit 10	R	EFCS[10]/CHEC[2]	X
Bit 9	R	EFCS[9]/CHEC[1]	X
Bit 8	R	EFCS[8]/CHEC[0]	X
Bit 7	R	EFCS[7]/UHCS[7] /UHEC[7]	X
Bit 6	R	EFCS[6]/UHCS[6] /UHEC[6]	X
Bit 5	R	EFCS[5]/UHCS[5] /UHEC[5]	X
Bit 4	R	EFCS[4]/UHCS[4] /UHEC[4]	X
Bit 3	R	EFCS[3]/UHCS[3] /UHEC[3]	X
Bit 2	R	EFCS[2]/UHCS[2] /UHEC[2]	X
Bit 1	R	EFCS[1]/UHCS[1] /UHEC[1]	X
Bit 0	R	EFCS[0]/UHCS[0] /UHEC[0]	X

EFCS[15:0]/UHCS[7:0] /CHEC[7:0]/UHEC[7:0]

In POS mode the EFCS[15:0] bits indicate the number of packets received containing FCS errors during the last accumulation interval.

In ATM mode the UHCS[7:0] bits indicate the number of uncorrectable HCS errors, (including all HCS errors when in DETECT mode), received in the last accumulation interval.

In GFP mode the CHEC[7:0] bits indicate the number of correctable cHEC errors received in the last accumulation interval, (i.e. apparent single bit errors when correction enabled). The UHEC[7:0] bits indicate the number of uncorrectable cHEC errors received in the last accumulation interval, (i.e. multi-bit cHEC errors).

A write to any one of the RCFP-9953 performance monitor registers loads the registers with the current counter value and resets the internal counter(2) to a value between 0 and 2. The counter reset value is dependent on the number of count events during the transfer of the register contents to the Receive Erred FCS/HCS Counter registers. The counter should be polled regularly to avoid saturating. The contents of these registers are valid three TCLK cycles after a transfer is triggered by a write to any of the RCFP-9953 performance monitor registers.

This counter can also be loaded by a microprocessor write to the S/UNI 9953 Identity and Global Performance Monitor Update register (0000H).

Downloaded by Comstream Communications Inc. on Wednesday, 07 February, 2007 06:59:32 PM

Register 202DH: RCFP-9953 Receive Aborted Packet Counter/eHEC/tHEC/sHEC error

Bit	Type	Function	Default
Bit 15	R	RABR[15] /SHEC[7]	X
Bit 14	R	RABR[14] /SHEC[6]	X
Bit 13	R	RABR[13] /SHEC[5]	X
Bit 12	R	RABR[12] /SHEC[4]	X
Bit 11	R	RABR[11] /SHEC[3]	X
Bit 10	R	RABR[10] /SHEC[2]	X
Bit 9	R	RABR[9] /SHEC[1]	X
Bit 8	R	RABR[8] /SHEC [0]	X
Bit 7	R	RABR[7] /EHEC_THEC [7]	X
Bit 6	R	RABR[6] /EHEC_THEC [6]	X
Bit 5	R	RABR[5] /EHEC_THEC [5]	X
Bit 4	R	RABR[4] /EHEC_THEC[4]	X
Bit 3	R	RABR[3] /EHEC_THEC[3]	X
Bit 2	R	RABR[2] /EHEC_THEC[2]	X
Bit 1	R	RABR[1] /EHEC_THEC[1]	X
Bit 0	R	RABR[0] /EHEC_THEC[0]	X

RABR[15:0]

In POS mode the RABR[15:0] bits indicate the number of aborted packets received during the last accumulation interval.

A write to any one of the RCFP-9953 performance monitor registers loads the registers with the current counter value and resets the internal counter to a value between 0 and 4. The counter reset value is dependent on the number of count events during the transfer of the register contents to the Receive Aborted Packet/eHEC error Counter registers. The counter should be polled regularly to avoid saturating. The contents of these registers are valid three TCLK cycles after a transfer is triggered by a write to any of the RCFP-9953 performance monitor registers.

This counter can also be loaded by a microprocessor write to the S/UNI 9953 Identity and Global Performance Monitor Update register (0000H).

SHEC[7:0]

In GFP mode the SHEC[7:0] bits indicate the number of OAM frames with incorrect sHEC CRC-16 checks received during the last accumulation interval.

Downloaded by Content Team on Equipment Inc on Wednesday, 07 February, 2007 06:59:32 PM

EHEC_THEC[7:0]

In GFP mode the EHEC_THEC[7:0] bits indicate the number of frames with incorrect Type and/or Extended Header CRC-16 checks (tHEC/eHEC) received during the last accumulation interval.

This counter is held at value 0 in ATM mode.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 202EH: RCFP-9953 Receive Minimum Length Packet-Frame Payload Error Counter

Bit	Type	Function	Default
Bit 15	R	RMINL[15]	X
Bit 14	R	RMINL[14]	X
Bit 13	R	RMINL[13]	X
Bit 12	R	RMINL[12]	X
Bit 11	R	RMINL[11]	X
Bit 10	R	RMINL[10]	X
Bit 9	R	RMINL[9]	X
Bit 8	R	RMINL[8]	X
Bit 7	R	RMINL[7]	X
Bit 6	R	RMINL[6]	X
Bit 5	R	RMINL[5]	X
Bit 4	R	RMINL[4]	X
Bit 3	R	RMINL[3]	X
Bit 2	R	RMINL[2]	X
Bit 1	R	RMINL[1]	X
Bit 0	R	RMINL[0]	X

RMINL[15:0]

In POS mode the RMINL[15:0] bits indicate the number of minimum length packet errors received during the last accumulation interval. This count includes detected/discarded malformed packets. Malformed packets are defined as being less than 8-bytes in length.

In GFP mode the RMINL[15:0] bits indicate the number of minimum length frames received during the last accumulation interval. A minimum length frame is defined as a frame whose length is less than the core plus extended header lengths or a frame whose payload is less than MINPL[7:0].

This counter is held at value 0 when in ATM mode.

A write to any one of the RCFP-9953 performance monitor registers loads the registers with the current counter value and resets the internal counter to a value between 0 and 8. The counter reset value is dependent on the number of count events during the transfer of the register contents to the Receive Minimum Length Packet-Frame Counter registers. The counter should be polled regularly to avoid saturating. The contents of these registers are valid three TCLK cycles after a transfer is triggered by a write to any of the RCFP-9953 performance monitor registers.

This counter can also be loaded by a microprocessor write to the S/UNI 9953 Identity and Global Performance Monitor Update register (0000H).

Downloaded by Conseil em Paramétrage on Wednesday, 07 February, 2007 06:59:32 PM

Register 202FH: RCFP-9953 Receive Maximum Length Packet-Frame Payload Error Counter

Bit	Type	Function	Default
Bit 15	R	RMAXL[15]	X
Bit 14	R	RMAXL[14]	X
Bit 13	R	RMAXL[13]	X
Bit 12	R	RMAXL[12]	X
Bit 11	R	RMAXL[11]	X
Bit 10	R	RMAXL[10]	X
Bit 9	R	RMAXL[9]	X
Bit 8	R	RMAXL[8]	X
Bit 7	R	RMAXL[7]	X
Bit 6	R	RMAXL[6]	X
Bit 5	R	RMAXL[5]	X
Bit 4	R	RMAXL[4]	X
Bit 3	R	RMAXL[3]	X
Bit 2	R	RMAXL[2]	X
Bit 1	R	RMAXL[1]	X
Bit 0	R	RMAXL[0]	X

RMAXL[15:0]

In POS mode the RMAXL[15:0] bits indicate the number of maximum length packet errors received during the last accumulation interval.

In GFP mode the RMAXL[15:0] bits indicate the number of maximum length frame errors received during the last accumulation interval.

This counter is held at value 0 when in ATM mode.

A write to any one of the RCFP-9953 performance monitor registers loads the registers with the current counter value and resets the internal counter to a value of 0 or 1. The counter reset value is dependent on the number of count events during the transfer of the register contents to the Receive Maximum Length Packet-Frame Counter registers. The counter should be polled regularly to avoid saturating. The contents of these registers are valid three TCLK cycles after a transfer is triggered by a write to any of the RCFP performance monitor registers.

This counter can also be loaded by a microprocessor write to the S/UNI 9953 Identity and Global Performance Monitor Update register (0000H).

Downloaded by Component Parametrics Inc on Wednesday, 07 February, 2007 06:59:32 PM

12.21 Receive Ethernet Processor 10 Gigabits (RXXG)

Register 2040H: RXXG Configuration 1

Bit	Type	Function	Default
Bit 15	R/W	RXEN	0
Bit 14	R/W	ROCF	0
Bit 13	R/W	PAD_STRIP	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	PUREP	1
Bit 9	R/W	LONGP	0
Bit 8	R/W	PARF	0
Bit 7	R/W	FLCHK	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	PASS_CTRL	0
Bit 4	R/W	RX_CONTIG	1
Bit 3	R/W	CRC_STRIP	0
Bit 2	R/W	Reserved	1
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

RXEN

When ‘1’, Receive packet parsing and transfer is enabled. When ‘0’, no packet parsing will be initiated, but a packet reception in progress will be completed. RXXG should be configured before writing this bit as ‘1’.

ROCF

Respond to Oversize Control Frames. When ‘1’, the RXXG will pause when an oversize (>=64) byte pause frame is received. When ‘0’ the RXXG will ONLY pause when 64 byte pause frames are received.

PAD_STRIP

When ‘1’, the RXXG will pad strip all non-errored and non-vlan tagged packets received. Pad stripping means that all frames will be truncated to the length field specified in the frame. When ‘0’, pad stripping will be disabled. Note that if CRC_STRIP must be set to ‘1’ when PAD_STRIP = ‘1’. Behavior is not defined if CRC_STRIP is ‘0’ and PAD_STRIP = ‘1’.

Downloaded by Content Team of Partminer.com on Wednesday, 07 February, 2007 06:59:32 PM

NOTE: if Frame Length Check is enabled and pad strip is also enabled, packets padded up to 64 bytes are the only padded packets that will not generate a frame length check error. VLAN tagged frames are not pad stripped.

PUREP

Pure Preamble. Set this bit to cause RXXG to check the contents of the preamble field of the packet, ensuring a data pattern of 0x55. Clear this bit if no preamble checking is desired.

LONGP

Long Preamble. Set this bit to permit reception of packets with any number of preamble. Clear this bit to cause RXXG to discard packets with >11 bytes of preamble.

PARF

Pass All Receive Frames. When this bit is '0', RXXG will process PAUSE Control frames, extracting the pause parameter from the packet to transfer to the TXXG and then discard the packet. When this bit is '1', RXXG will not process PAUSE Control frames and will forward the packet to the FIFO interface (provided it is not filtered for error reasons).

FLCHK

Frame Length Check. When this bit is '1', RXXG will compare the actual frame length against the value contained in the Type/Length field of the MAC header. This check is only done if the Type/Length field is in the range (0-1518). If a length mismatch occurs, the frame will be discarded. When this bit is '0', this check is not performed.

PASS_CTRL

Pass MAC Control frames. When this bit is '1', RXXG will forward MAC Control non-PAUSE frames to the System interface. When this bit is '0', RXXG will filter these frames. MAC Control PAUSE frame processing and filtering is determined by PARF bit.

RX_CONTIG

Receive Packet Contiguous. This configuration register bit must ALWAYS be sent to 0 on initialization. Operation is not guaranteed if this bit is set to 1.

CRC_STRIP

CRC Strip Register Bit. When this bit is '1', RXXG will strip the CRC from the packet. When this bit is '0', the packet is forwarded through RXXG with the CRC appended.

Downloaded by Content Team on Examiner Name on Wednesday, 07 February, 2007 05:59:32 PM

Register 2041H: RXXG Configuration 2

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 2042H: RXXG Configuration 3

Bit	Type	Function	Default
Bit 15	R/W	MIN_LERRE	0
Bit 14	R/W	MAX_LERRE	0
Bit 13	R/W	ODD_ALIGNE	0
Bit 12	R/W	LINE_ERRE	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	RX_OVRE	0
Bit 9	R/W	ADR_FILTERE	0
Bit 8	R/W	ERR_DETECTE	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	PRMB_ERRE	0
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

MIN_LERRE

The MIN_LERRE bit enables the generation of an interrupt due to a packet sourced from the Line Interface being less that the minimum frame size of 64 bytes. The frame size does not include preamble/ SFD bytes or prepended frame delineation headers. It just covers the MAC frame contents including CRC.

MAX_LERRE

The MAX_LERRE bit enables the generation of an interrupt due to a packet sourced from the Line interface exceeding the maximum frame size programmed in the Maximum Frame Length register. The frame size does not include preamble/ SFD bytes or prepended frame delineation headers. It just covers the MAC frame contents including CRC.

ODD_ALIGNE

The ODD_ALIGNE bit enables the generation of an interrupt due to a packet sourced from the Line interface not starting on a 32-bit alignment. This is in support of the requirements for the 64b/66b PCS framing schemes, which are constrained to 32-bit start alignment. This interrupt indicates a possible framing error.

Downloaded by Content Team of Datminer Inc. on Wednesday, 07 February, 2007 06:59:32 PM

LINE_ERRE

The LINE_ERRE bit enables the generation of an interrupt due to any Line interface errors. See the description of LINE_ERRI in the RXXG Interrupt register for a description of errors.

RX_OVRE

The RX_OVRE bit enables the generation of an interrupt due to a receive overrun causes by upstream blockage subsequently causing an overrun of the RXXG internal FIFO.

ADR_FILTERE

The ADR_FILTERE bit enables the generation of an interrupt whenever a packet is filtered by RXXG, due to MAC Address filter functions.

ERR_DETECTE

This bit is set when a protocol error (CRC, Frame Length, Range Check) is seen in a packet. The packet will be filtered by RXXG when the packet is less than the programmable FIFO Threshold value, otherwise the packet is forwarded and marked as errored

PRMB_ERRE

PRMB_ERRE enables the PRMB_ERRI bit generating an interrupt output (INTB). PRMB_ERRI is set when a packet is received that violates the preamble expected. The expected preamble is dependent on PUREP, LONGP and NO_PRMB in RXXG Configuration Register 1. If PRMB_ERRE is ‘1’ in Configuration 3 register, an interrupt will also be generated (INTB output asserted).

Downloaded by Content Team of Partminer.com on Wednesday, 07 February, 2007 06:59:32 PM

Register 2043H: RXXG Interrupt

Bit	Type	Function	Default
Bit 15	R	MIN_LERRI	X
Bit 14	R	MAX_LERRI	X
Bit 13	R	ODD_ALIGNI	X
Bit 12	R	LINE_ERRI	X
Bit 11	R	Reserved	X
Bit 10	R	RX_OVRI	X
Bit 9	R	ADR_FILTERI	X
Bit 8	R	ERR_DETECTI	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	PRMB_ERRI	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, these interrupt status bits are cleared on write with a logic 1. Otherwise, these interrupt status bits are cleared on read.

Note that there is no priority encoding on the interrupts. Some interrupts will trigger even if the RXXG is receiving invalid data due to non synchronization of upstream blocks. Thus, the triggering of some interrupts may imply other interrupts should be ignored due to a higher level condition.

MIN_LERRI

The MIN_LERRI bit will be set when the packet sourced from the Line Interface is less than the legal minimum of 64 bytes. The frame size does not include preamble/ SFD bytes or prepended frame delineation headers. It just covers the MAC frame contents including CRC. If MIN_LERRE is ‘1’ in Configuration 3 register, an interrupt will also be generated (INTB output asserted).

MAX_LERRI

The MAX_LERRI bit will be set when the packet sourced from the Line Interface exceeds the maximum frame size programmed in the Maximum Frame Length register. The frame size does not include preamble/ SFD bytes or prepended frame delineation headers. It just covers the MAC frame contents including CRC. If MAX_LERRE is ‘1’ in Configuration 3 register, an interrupt will also be generated (INTB output asserted)

Downloaded by Content Team at Partminer.com Wednesday, 07 February, 2007 06:59:32 PM

ODD_ALIGNI

The ODD_ALIGNI bit is set when the packet sourced from the Line interface does not start on an even 32-bit alignment. This is in support of the requirements for XAUI and 64b/66b PCS framing schemes which are constrained to this start alignment. RXXG will accept frames on any byte alignment. This interrupt is just an indication of a possible framing error. If ODD_ALIGNE is '1' in Configuration 3 register, an interrupt will also be generated (INTB output asserted).

LINE_ERRI

The LINE_ERRI bit is set when a Line Interface error is detected. If LINE_ERRE is '1' in RXXG Configuration 3 register, an interrupt will also be generated (INT output asserted). Failure modes are (1) Breakdown in alternating SOP-EOP sequence (2) Invalid byte(s) between SOP and EOP not part of a completely invalid word. (3) Reception of frames less than 14 bytes.

RX_OVRI

The RX_OVRI bit is set when a receive overrun is caused by the FIFO_FULL status being asserted by downstream FIFO block and subsequently causing an overrun of the RXXG internal FIFO. If RX_OVRE is '1' in Configuration 3 register, an interrupt will also be generated (INTB output asserted).

ADR_FILTERI

The ADR_FILTERI bit is set whenever a packet is filtered by RXXG, due to MAC Address filter functions. If ADR_FILTERE is '1' in Configuration 3 register, an interrupt will also be generated (INTB output asserted).

ERR_DETECTI

The ERR_DETECTI bit is set whenever a packet is filtered by RXXG, due protocol error conditions. If ERR_DETECTE is '1' in Configuration 3 register, an interrupt will also be generated (INTB output asserted).

PRMB_ERRI

PRMB_ERRI is set when a packet is received that violates the preamble expected. The expected preamble is dependent on PUREP and LONGP in RXXG Configuration Register 1. If PRMB_ERRE is '1' in Configuration 3 register, an interrupt will also be generated (INTB output asserted).

Downloaded by Component Search Department Inc on Wednesday, 07 February 2007 08:58:32 AM

Register 2044H: RXXG Status

Bit	Type	Function	Default
Bit 15	R	Reserved	x
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 2045H: RXXG Maximum Frame Length

Bit	Type	Function	Default
Bit 15	R/W	RX_MAXFR[15]	0
Bit 14	R/W	RX_MAXFR[14]	0
Bit 13	R/W	RX_MAXFR[13]	0
Bit 12	R/W	RX_MAXFR[12]	0
Bit 11	R/W	RX_MAXFR[11]	0
Bit 10	R/W	RX_MAXFR[10]	1
Bit 9	R/W	RX_MAXFR[9]	0
Bit 8	R/W	RX_MAXFR[8]	1
Bit 7	R/W	RX_MAXFR[7]	1
Bit 6	R/W	RX_MAXFR[6]	1
Bit 5	R/W	RX_MAXFR[5]	1
Bit 4	R/W	RX_MAXFR[4]	0
Bit 3	R/W	RX_MAXFR[3]	1
Bit 2	R/W	RX_MAXFR[2]	1
Bit 1	R/W	RX_MAXFR[1]	1
Bit 0	R/W	RX_MAXFR[0]	0

RX_MAXFR[15:0]

This field resets to 0x05EE, which represents a maximum receive frame of 1518 octets. An untagged maximum size Ethernet frame is 1518 octets in length. A tagged frame adds four octets for a total of 1522 octets. If a different maximum length restriction is desired, program this 16-bit field. Frames which exceed this length will be truncated to match the specified length. Note: This does not include the length of preamble/ SFD bytes.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:59:32 PM

Register 2046H: RXXG SA[15:0] – Station Address

Bit	Type	Function	Default
Bit 15	R/W	SA[15]	0
Bit 14	R/W	SA [14]	0
Bit 13	R/W	SA [13]	0
Bit 12	R/W	SA [12]	0
Bit 11	R/W	SA [11]	0
Bit 10	R/W	SA [10]	0
Bit 9	R/W	SA [9]	0
Bit 8	R/W	SA [8]	0
Bit 7	R/W	SA [7]	0
Bit 6	R/W	SA [6]	0
Bit 5	R/W	SA [5]	0
Bit 4	R/W	SA [4]	0
Bit 3	R/W	SA [3]	0
Bit 2	R/W	SA [2]	0
Bit 1	R/W	SA[1]	0
Bit 0	R/W	SA[0]	0

SA[15:0]

Station Address Low Word. MAC Control PAUSE frames may be addressed to the well-known Multicast address assigned for this purpose, or to the Station Address directly i.e. SA[47 :0]. The MAC Control Sub-layer expects either the Multicast address or the Station address as criteria to respond to the PAUSE frame received.

Downloaded by Content Team of Partminer on Wednesday, 07 February, 2007 06:59:32 PM

Register 2047H: RXXG SA[31:16] – Station Address

Bit	Type	Function	Default
Bit 15	R/W	SA[31]	0
Bit 14	R/W	SA [30]	0
Bit 13	R/W	SA [29]	0
Bit 12	R/W	SA [28]	0
Bit 11	R/W	SA [27]	0
Bit 10	R/W	SA [26]	0
Bit 9	R/W	SA [25	0
Bit 8	R/W	SA [24]	0
Bit 7	R/W	SA [23]	0
Bit 6	R/W	SA [22]	0
Bit 5	R/W	SA [21]	0
Bit 4	R/W	SA [20]	0
Bit 3	R/W	SA [19]	0
Bit 2	R/W	SA [18]	0
Bit 1	R/W	SA[17]	0
Bit 0	R/W	SA[16]	0

SA[31:16]

Station Address Mid Word. MAC Control PAUSE frames may be addressed to the well-known Multicast address assigned for this purpose, or to the Station Address directly i.e. SA[47 :0]. The MAC Control Sub-layer expects either the Multicast address or the Station address as criteria to respond to the PAUSE frame received.

Downloaded by Content Team of Partminer on Wednesday, 07 February, 2007 06:59:32 PM

Register 2048H: RXXG SA[47:32] – Station Address

Bit	Type	Function	Default
Bit 15	R/W	SA[47]	0
Bit 14	R/W	SA [46]	0
Bit 13	R/W	SA [45]	0
Bit 12	R/W	SA [44]	0
Bit 11	R/W	SA [43]	0
Bit 10	R/W	SA [42]	0
Bit 9	R/W	SA [41]	0
Bit 8	R/W	SA [40]	0
Bit 7	R/W	SA [39]	0
Bit 6	R/W	SA [38]	0
Bit 5	R/W	SA [37]	0
Bit 4	R/W	SA [36]	0
Bit 3	R/W	SA [35]	0
Bit 2	R/W	SA [34]	0
Bit 1	R/W	SA[33]	0
Bit 0	R/W	SA[32]	0

SA[47:32]

Station Address High Word. MAC Control PAUSE frames may be addressed to the well-known Multicast address assigned for this purpose, or to the Station Address directly i.e. SA[47 :0]. The MAC Control Sub-layer expects either the Multicast address or the Station address as criteria to respond to the PAUSE frame received.

Downloaded by Content Team of Partminer on Wednesday, 07 February, 2007 06:59:32 PM

Register 2049H: RXXG Cut-Thru Threshold Select

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R/W	CUT_THRU_THRES_SEL[2]	1
Bit 1	R/W	CUT_THRU_THRES_SEL[1]	0
Bit 0	R/W	CUT_THRU_THRES_SEL[0]	1

CUT_THRU_THRES_SEL [2:0]

Cut_thru_thres_sel	Pkt_Fifo_Threshold
0	8 (64 bytes)
1	64 (512 bytes)
2	128 (1024 bytes)
3	192 (1536 bytes)
4	224 (1792 bytes)
5	EOP write triggers reading from PKT FIFO

Cut-Thru threshold select, sets the forwarding threshold in the internal receive FIFO for initiating packet transfer to the System FIFO interface. Default is 0x5 or 255 x 64-bit entries or 2040 bytes (+/-7 bytes). This defines a store-and-forward mode of operation. This mode of operation can be used only when all packets received are expected to be less than or equal to 2000. Packets greater than 2000 will be truncated (to prevent FIFO filling) and marked as errored. To configure RXXG for cut-through mode, program cut_thru_thres_sel to 0,1, 2, 3, or 4. Increasing the threshold value, increases the errored packet size RXXG can filter. This mode of operation can be used where packets greater than the FIFO size (~2000 bytes) are expected, i.e. jumbo packets, but errored packets less than the threshold value are to be filtered. If a packet breaks the cut-through threshold, RXXG begins to read the packet out. As RXXG can only determine if a packet is errored after the EOP is received, it is not possible to filter this packet. Since each word in the RAM can occupy 8 bytes of data, packets that are under the minimum size to fill the threshold can only be filtered by RXXG. For example,

Downloaded by Conexant Partner on Wednesday, 07 February, 2007 06:59:32 PM

CUT_THRU_SEL = 4
=> 224 Words
=> 1 byte on first

+ 222 x 8 bytes

+ 2 x 8 bytes (Latency)

- 8 bytes (Possible Line Gap inside a packet, i.e. dead-band

1786 byte packet

Hence, the absolute maximum size packet RXXG can guarantee to filter, when CUT_THRU_SEL = 4, is a 1785 byte packet. Depending on the offset of the SOP in the RAM, i.e. is the SOP in the MSByte of the RAM, the RXXG will filter or forward packets between 1786 bytes and 1808 (224x8) bytes. Below is a Table illustrating the acceptable packet sizes for filtering based on the CUT_THRU_SEL value.

Table 28 CUT_THRU_THRES Packet Sizes

CUT_THRU_SEL	0	1	2	3	4	5
Words to Threshold	8	64	128	192	224	N/A
Guaranteed maximum size packet RXXG will filter	57	505	1017	1529	1785	1992
Filter or forward packets in this range	58 - 80	–506 - 528	–1018 - 1040	–1530 - 1552	–1786 - 1808	N/A
Guaranteed minimum size packet RXXG will not filter	>80	>528	>1041	>1552	>1808	N/A

A cut_thru_thres_sel value of 5 will mean that the Pkt FIFO will never go into cut_thru mode, i.e. no support for jumbo packets in RXXG. When the packet size goes over 2040 bytes the Pkt FIFO will overrun.

Downloaded by Content Team of Partminer Inc on Wednesday 21 February, 2007 06:59:32 PM

Register 204AH: RXXG Exact Match Address 0 Low Word

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH0[15]	0
Bit 14	R/W	ADR_MATCH0 [14]	0
Bit 13	R/W	ADR_MATCH0 [13]	0
Bit 12	R/W	ADR_MATCH0 [12]	0
Bit 11	R/W	ADR_MATCH0 [11]	0
Bit 10	R/W	ADR_MATCH0 [10]	0
Bit 9	R/W	ADR_MATCH0 [9]	0
Bit 8	R/W	ADR_MATCH0 [8]	0
Bit 7	R/W	ADR_MATCH0 [7]	0
Bit 6	R/W	ADR_MATCH0 [6]	0
Bit 5	R/W	ADR_MATCH0 [5]	0
Bit 4	R/W	ADR_MATCH0 [4]	0
Bit 3	R/W	ADR_MATCH0 [3]	0
Bit 2	R/W	ADR_MATCH0 [2]	0
Bit 1	R/W	ADR_MATCH0 [1]	0
Bit 0	R/W	ADR_MATCH0 [0]	0

ADR_MATCH0[15:0]

The Exact Match Address 0 Low Word is used for the Low Word [15:0] of the 48-bit MAC Address that the Address Filter Logic uses to compare on. This register is one of eight separate Exact Match Address registers that the Address Filter Logic can use to compare on.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:09:32 PM

Register 204BH: RXXG Exact Match Address 0 Mid Word

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH0[31]	0
Bit 14	R/W	ADR_MATCH0 [30]	0
Bit 13	R/W	ADR_MATCH0 [29]	0
Bit 12	R/W	ADR_MATCH0 [28]	0
Bit 11	R/W	ADR_MATCH0 [27]	0
Bit 10	R/W	ADR_MATCH0 [26]	0
Bit 9	R/W	ADR_MATCH0 [25	0
Bit 8	R/W	ADR_MATCH0 [24]	0
Bit 7	R/W	ADR_MATCH0 [23]	0
Bit 6	R/W	ADR_MATCH0 [22]	0
Bit 5	R/W	ADR_MATCH0 [21]	0
Bit 4	R/W	ADR_MATCH0 [20]	0
Bit 3	R/W	ADR_MATCH0 [19]	0
Bit 2	R/W	ADR_MATCH0 [18]	0
Bit 1	R/W	ADR_MATCH0 [17]	0
Bit 0	R/W	ADR_MATCH0 [16]	0

ADR_MATCH0[31:16]

The Exact Match Address 0 Mid Word is used for the Mid Word [31:16] of the 48-bit MAC Address that the Address Filter Logic uses to compare on. This register is one of eight separate Exact Match Address registers that the Address Filter Logic can use to compare on.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:09:32 PM

Register 204CH: RXXG Exact Match Address 0 High Word

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH0[47]	0
Bit 14	R/W	ADR_MATCH0 [46]	0
Bit 13	R/W	ADR_MATCH0 [45]	0
Bit 12	R/W	ADR_MATCH0 [44]	0
Bit 11	R/W	ADR_MATCH0 [43]	0
Bit 10	R/W	ADR_MATCH0 [42]	0
Bit 9	R/W	ADR_MATCH0 [41]	0
Bit 8	R/W	ADR_MATCH0 [40]	0
Bit 7	R/W	ADR_MATCH0 [39]	0
Bit 6	R/W	ADR_MATCH0 [38]	0
Bit 5	R/W	ADR_MATCH0 [37]	0
Bit 4	R/W	ADR_MATCH0 [36]	0
Bit 3	R/W	ADR_MATCH0 [35]	0
Bit 2	R/W	ADR_MATCH0 [34]	0
Bit 1	R/W	ADR_MATCH0 [33]	0
Bit 0	R/W	ADR_MATCH0 [32]	0

ADR_MATCH0[47:32]

The Exact Match Address 0 High Word is used for the High Word [47:32] of the 48-bit MAC Address that the Address Filter Logic uses to compare on. This register is one of eight separate Exact Match Address registers that the Address Filter Logic can use to compare on.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:09:32 PM

Register 204DH: RXXG Exact Match Address 1 Low Word

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH1[15]	0
Bit 14	R/W	ADR_MATCH1 [14]	0
Bit 13	R/W	ADR_MATCH1 [13]	0
Bit 12	R/W	ADR_MATCH1 [12]	0
Bit 11	R/W	ADR_MATCH1 [11]	0
Bit 10	R/W	ADR_MATCH1 [10]	0
Bit 9	R/W	ADR_MATCH1 [9]	0
Bit 8	R/W	ADR_MATCH1 [8]	0
Bit 7	R/W	ADR_MATCH1 [7]	0
Bit 6	R/W	ADR_MATCH1 [6]	0
Bit 5	R/W	ADR_MATCH1 [5]	0
Bit 4	R/W	ADR_MATCH1 [4]	0
Bit 3	R/W	ADR_MATCH1 [3]	0
Bit 2	R/W	ADR_MATCH1 [2]	0
Bit 1	R/W	ADR_MATCH1 [1]	0
Bit 0	R/W	ADR_MATCH1 [0]	0

ADR_MATCH1[15:0]

The Exact Match Address 1 Low Word is used for the Low Word [15:0] of the 48-bit MAC Address that the Address Filter Logic uses to compare on. This register is one of eight separate Exact Match Address registers that the Address Filter Logic can use to compare on.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:09:32 PM

Register 204EH: RXXG Exact Match Address 1 Mid Word

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH1[31]	0
Bit 14	R/W	ADR_MATCH1 [30]	0
Bit 13	R/W	ADR_MATCH1 [29]	0
Bit 12	R/W	ADR_MATCH1 [28]	0
Bit 11	R/W	ADR_MATCH1 [27]	0
Bit 10	R/W	ADR_MATCH1 [26]	0
Bit 9	R/W	ADR_MATCH1 [25	0
Bit 8	R/W	ADR_MATCH1 [24]	0
Bit 7	R/W	ADR_MATCH1 [23]	0
Bit 6	R/W	ADR_MATCH1 [22]	0
Bit 5	R/W	ADR_MATCH1 [21]	0
Bit 4	R/W	ADR_MATCH1 [20]	0
Bit 3	R/W	ADR_MATCH1 [19]	0
Bit 2	R/W	ADR_MATCH1 [18]	0
Bit 1	R/W	ADR_MATCH1 [17]	0
Bit 0	R/W	ADR_MATCH1 [16]	0

ADR_MATCH1[31:16]

The Exact Match Address 1 Mid Word is used for the Mid Word [31:16] of the 48-bit MAC Address that the Address Filter Logic uses to compare on. This register is one of eight separate Exact Match Address registers that the Address Filter Logic can use to compare on.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:09:32 PM

Register 204FH: RXXG Exact Match Address 1 High Word

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH1[47]	0
Bit 14	R/W	ADR_MATCH1 [46]	0
Bit 13	R/W	ADR_MATCH1 [45]	0
Bit 12	R/W	ADR_MATCH1 [44]	0
Bit 11	R/W	ADR_MATCH1 [43]	0
Bit 10	R/W	ADR_MATCH1 [42]	0
Bit 9	R/W	ADR_MATCH1 [41]	0
Bit 8	R/W	ADR_MATCH1 [40]	0
Bit 7	R/W	ADR_MATCH1 [39]	0
Bit 6	R/W	ADR_MATCH1 [38]	0
Bit 5	R/W	ADR_MATCH1 [37]	0
Bit 4	R/W	ADR_MATCH1 [36]	0
Bit 3	R/W	ADR_MATCH1 [35]	0
Bit 2	R/W	ADR_MATCH1 [34]	0
Bit 1	R/W	ADR_MATCH1 [33]	0
Bit 0	R/W	ADR_MATCH1 [32]	0

ADR_MATCH1[47:32]

The Exact Match Address 1 High Word is used for the High Word [47:32] of the 48-bit MAC Address that the Address Filter Logic uses to compare on. This register is one of eight separate Exact Match Address registers that the Address Filter Logic can use to compare on.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:09:32 PM

Register 2050H: RXXG Exact Match Address 2 Low Word

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH2[15]	0
Bit 14	R/W	ADR_MATCH2 [14]	0
Bit 13	R/W	ADR_MATCH2 [13]	0
Bit 12	R/W	ADR_MATCH2 [12]	0
Bit 11	R/W	ADR_MATCH2 [11]	0
Bit 10	R/W	ADR_MATCH2 [10]	0
Bit 9	R/W	ADR_MATCH2 [9]	0
Bit 8	R/W	ADR_MATCH2 [8]	0
Bit 7	R/W	ADR_MATCH2 [7]	0
Bit 6	R/W	ADR_MATCH2 [6]	0
Bit 5	R/W	ADR_MATCH2 [5]	0
Bit 4	R/W	ADR_MATCH2 [4]	0
Bit 3	R/W	ADR_MATCH2 [3]	0
Bit 2	R/W	ADR_MATCH2 [2]	0
Bit 1	R/W	ADR_MATCH2 [1]	0
Bit 0	R/W	ADR_MATCH2 [0]	0

ADR_MATCH2[15:0]

The Exact Match Address 2 Low Word is used for the Low Word [15:0] of the 48-bit MAC Address that the Address Filter Logic uses to compare on. This register is one of eight separate Exact Match Address registers that the Address Filter Logic can use to compare on.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:09:32 PM

Register 2051H: RXXG Exact Match Address 2 Mid Word

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH2[31]	0
Bit 14	R/W	ADR_MATCH2 [30]	0
Bit 13	R/W	ADR_MATCH2 [29]	0
Bit 12	R/W	ADR_MATCH2 [28]	0
Bit 11	R/W	ADR_MATCH2 [27]	0
Bit 10	R/W	ADR_MATCH2 [26]	0
Bit 9	R/W	ADR_MATCH2 [25	0
Bit 8	R/W	ADR_MATCH2 [24]	0
Bit 7	R/W	ADR_MATCH2 [23]	0
Bit 6	R/W	ADR_MATCH2 [22]	0
Bit 5	R/W	ADR_MATCH2 [21]	0
Bit 4	R/W	ADR_MATCH2 [20]	0
Bit 3	R/W	ADR_MATCH2 [19]	0
Bit 2	R/W	ADR_MATCH2 [18]	0
Bit 1	R/W	ADR_MATCH2 [17]	0
Bit 0	R/W	ADR_MATCH2 [16]	0

ADR_MATCH2[31:16]

The Exact Match Address 2 Mid Word is used for the Mid Word [31:16] of the 48-bit MAC Address that the Address Filter Logic uses to compare on. This register is one of eight separate Exact Match Address registers that the Address Filter Logic can use to compare on.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:09:32 PM

Register 2052H: RXXG Exact Match Address 2 High Word

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH2[47]	0
Bit 14	R/W	ADR_MATCH2 [46]	0
Bit 13	R/W	ADR_MATCH2 [45]	0
Bit 12	R/W	ADR_MATCH2 [44]	0
Bit 11	R/W	ADR_MATCH2 [43]	0
Bit 10	R/W	ADR_MATCH2 [42]	0
Bit 9	R/W	ADR_MATCH2 [41]	0
Bit 8	R/W	ADR_MATCH2 [40]	0
Bit 7	R/W	ADR_MATCH2[39]	0
Bit 6	R/W	ADR_MATCH2 [38]	0
Bit 5	R/W	ADR_MATCH2 [37]	0
Bit 4	R/W	ADR_MATCH2 [36]	0
Bit 3	R/W	ADR_MATCH2 [35]	0
Bit 2	R/W	ADR_MATCH2 [34]	0
Bit 1	R/W	ADR_MATCH2 [33]	0
Bit 0	R/W	ADR_MATCH2 [32]	0

ADR_MATCH2[47:32]

The Exact Match Address 2 High Word is used for the High Word [47:32] of the 48-bit MAC Address that the Address Filter Logic uses to compare on. This register is one of eight separate Exact Match Address registers that the Address Filter Logic can use to compare on.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:09:32 PM

Register 2053H: RXXG Exact Match Address 3 Low Word

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH3[15]	0
Bit 14	R/W	ADR_MATCH3 [14]	0
Bit 13	R/W	ADR_MATCH3 [13]	0
Bit 12	R/W	ADR_MATCH3 [12]	0
Bit 11	R/W	ADR_MATCH3 [11]	0
Bit 10	R/W	ADR_MATCH3 [10]	0
Bit 9	R/W	ADR_MATCH3 [9]	0
Bit 8	R/W	ADR_MATCH3 [8]	0
Bit 7	R/W	ADR_MATCH3 [7]	0
Bit 6	R/W	ADR_MATCH3 [6]	0
Bit 5	R/W	ADR_MATCH3 [5]	0
Bit 4	R/W	ADR_MATCH3 [4]	0
Bit 3	R/W	ADR_MATCH3 [3]	0
Bit 2	R/W	ADR_MATCH3 [2]	0
Bit 1	R/W	ADR_MATCH3 [1]	0
Bit 0	R/W	ADR_MATCH3 [0]	0

ADR_MATCH3[15:0]

The Exact Match Address 3 Low Word is used for the Low Word [15:0] of the 48-bit MAC Address that the Address Filter Logic uses to compare on. This register is one of eight separate Exact Match Address registers that the Address Filter Logic can use to compare on.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:09:32 PM

Register 2054H: RXXG Exact Match Address 3 Mid Word

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH3[31]	0
Bit 14	R/W	ADR_MATCH3 [30]	0
Bit 13	R/W	ADR_MATCH3 [29]	0
Bit 12	R/W	ADR_MATCH3 [28]	0
Bit 11	R/W	ADR_MATCH3 [27]	0
Bit 10	R/W	ADR_MATCH3 [26]	0
Bit 9	R/W	ADR_MATCH3 [25	0
Bit 8	R/W	ADR_MATCH3 [24]	0
Bit 7	R/W	ADR_MATCH3 [23]	0
Bit 6	R/W	ADR_MATCH3 [22]	0
Bit 5	R/W	ADR_MATCH3 [21]	0
Bit 4	R/W	ADR_MATCH3 [20]	0
Bit 3	R/W	ADR_MATCH3 [19]	0
Bit 2	R/W	ADR_MATCH3 [18]	0
Bit 1	R/W	ADR_MATCH3 [17]	0
Bit 0	R/W	ADR_MATCH3 [16]	0

ADR_MATCH3[31:16]

The Exact Match Address 3 Mid Word is used for the Mid Word [31:16] of the 48-bit MAC Address that the Address Filter Logic uses to compare on. This register is one of eight separate Exact Match Address registers that the Address Filter Logic can use to compare on.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:09:32 PM

Register 2055H: RXXG Exact Match Address 3 High Word

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH3[47]	0
Bit 14	R/W	ADR_MATCH3 [46]	0
Bit 13	R/W	ADR_MATCH3 [45]	0
Bit 12	R/W	ADR_MATCH3 [44]	0
Bit 11	R/W	ADR_MATCH3 [43]	0
Bit 10	R/W	ADR_MATCH3 [42]	0
Bit 9	R/W	ADR_MATCH3 [41]	0
Bit 8	R/W	ADR_MATCH3 [40]	0
Bit 7	R/W	ADR_MATCH3 [39]	0
Bit 6	R/W	ADR_MATCH3 [38]	0
Bit 5	R/W	ADR_MATCH3 [37]	0
Bit 4	R/W	ADR_MATCH3 [36]	0
Bit 3	R/W	ADR_MATCH3 [35]	0
Bit 2	R/W	ADR_MATCH3 [34]	0
Bit 1	R/W	ADR_MATCH3 [33]	0
Bit 0	R/W	ADR_MATCH3 [32]	0

ADR_MATCH3[47:32]

The Exact Match Address 3 High Word is used for the High Word [47:32] of the 48-bit MAC Address that the Address Filter Logic uses to compare on. This register is one of eight separate Exact Match Address registers that the Address Filter Logic can use to compare on.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:09:32 PM

Register 2056H: RXXG Exact Match Address 4 Low Word

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH4[15]	0
Bit 14	R/W	ADR_MATCH4 [14]	0
Bit 13	R/W	ADR_MATCH4 [13]	0
Bit 12	R/W	ADR_MATCH4 [12]	0
Bit 11	R/W	ADR_MATCH4 [11]	0
Bit 10	R/W	ADR_MATCH4 [10]	0
Bit 9	R/W	ADR_MATCH4 [9]	0
Bit 8	R/W	ADR_MATCH4 [8]	0
Bit 7	R/W	ADR_MATCH4 [7]	0
Bit 6	R/W	ADR_MATCH4 [6]	0
Bit 5	R/W	ADR_MATCH4 [5]	0
Bit 4	R/W	ADR_MATCH4 [4]	0
Bit 3	R/W	ADR_MATCH4 [3]	0
Bit 2	R/W	ADR_MATCH4 [2]	0
Bit 1	R/W	ADR_MATCH4 [1]	0
Bit 0	R/W	ADR_MATCH4 [0]	0

ADR_MATCH4[15:0]

The Exact Match Address 4 Low Word is used for the Low Word [15:0] of the 48-bit MAC Address that the Address Filter Logic uses to compare on. This register is one of eight separate Exact Match Address registers that the Address Filter Logic can use to compare on.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:09:32 PM

Register 2057H: RXXG Exact Match Address 4 Mid Word

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH4[31]	0
Bit 14	R/W	ADR_MATCH4 [30]	0
Bit 13	R/W	ADR_MATCH4 [29]	0
Bit 12	R/W	ADR_MATCH4 [28]	0
Bit 11	R/W	ADR_MATCH4 [27]	0
Bit 10	R/W	ADR_MATCH4 [26]	0
Bit 9	R/W	ADR_MATCH4 [25	0
Bit 8	R/W	ADR_MATCH4 [24]	0
Bit 7	R/W	ADR_MATCH4 [23]	0
Bit 6	R/W	ADR_MATCH4 [22]	0
Bit 5	R/W	ADR_MATCH4 [21]	0
Bit 4	R/W	ADR_MATCH4 [20]	0
Bit 3	R/W	ADR_MATCH4 [19]	0
Bit 2	R/W	ADR_MATCH4 [18]	0
Bit 1	R/W	ADR_MATCH4 [17]	0
Bit 0	R/W	ADR_MATCH4 [16]	0

ADR_MATCH4[31:16]

The Exact Match Address 4 Mid Word is used for the Mid Word [31:16] of the 48-bit MAC Address that the Address Filter Logic uses to compare on. This register is one of eight separate Exact Match Address registers that the Address Filter Logic can use to compare on.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:09:32 PM

Register 2058H: RXXG Exact Match Address 4 High Word

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH4[47]	0
Bit 14	R/W	ADR_MATCH4 [46]	0
Bit 13	R/W	ADR_MATCH4 [45]	0
Bit 12	R/W	ADR_MATCH4 [44]	0
Bit 11	R/W	ADR_MATCH4 [43]	0
Bit 10	R/W	ADR_MATCH4 [42]	0
Bit 9	R/W	ADR_MATCH4 [41]	0
Bit 8	R/W	ADR_MATCH4 [40]	0
Bit 7	R/W	ADR_MATCH4 [39]	0
Bit 6	R/W	ADR_MATCH4 [38]	0
Bit 5	R/W	ADR_MATCH4 [37]	0
Bit 4	R/W	ADR_MATCH4 [36]	0
Bit 3	R/W	ADR_MATCH4 [35]	0
Bit 2	R/W	ADR_MATCH4 [34]	0
Bit 1	R/W	ADR_MATCH4 [33]	0
Bit 0	R/W	ADR_MATCH4 [32]	0

ADR_MATCH4[47:32]

The Exact Match Address 4 High Word is used for the High Word [47:32] of the 48-bit MAC Address that the Address Filter Logic uses to compare on. This register is one of eight separate Exact Match Address registers that the Address Filter Logic can use to compare on.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:09:32 PM

Register 2059H: RXXG Exact Match Address 5 Low Word

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH5[15]	0
Bit 14	R/W	ADR_MATCH5 [14]	0
Bit 13	R/W	ADR_MATCH5 [13]	0
Bit 12	R/W	ADR_MATCH5 [12]	0
Bit 11	R/W	ADR_MATCH5 [11]	0
Bit 10	R/W	ADR_MATCH5 [10]	0
Bit 9	R/W	ADR_MATCH5 [9]	0
Bit 8	R/W	ADR_MATCH5 [8]	0
Bit 7	R/W	ADR_MATCH5 [7]	0
Bit 6	R/W	ADR_MATCH5 [6]	0
Bit 5	R/W	ADR_MATCH5 [5]	0
Bit 4	R/W	ADR_MATCH5 [4]	0
Bit 3	R/W	ADR_MATCH5 [3]	0
Bit 2	R/W	ADR_MATCH5 [2]	0
Bit 1	R/W	ADR_MATCH5 [1]	0
Bit 0	R/W	ADR_MATCH5 [0]	0

ADR_MATCH5[15:0]

The Exact Match Address 5 Low Word is used for the Low Word [15:0] of the 48-bit MAC Address that the Address Filter Logic uses to compare on. This register is one of eight separate Exact Match Address registers that the Address Filter Logic can use to compare on.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:09:32 PM

Register 205AH: RXXG Exact Match Address 5 Mid Word

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH5[31]	0
Bit 14	R/W	ADR_MATCH5 [30]	0
Bit 13	R/W	ADR_MATCH5 [29]	0
Bit 12	R/W	ADR_MATCH5 [28]	0
Bit 11	R/W	ADR_MATCH5 [27]	0
Bit 10	R/W	ADR_MATCH5 [26]	0
Bit 9	R/W	ADR_MATCH5 [25	0
Bit 8	R/W	ADR_MATCH5 [24]	0
Bit 7	R/W	ADR_MATCH5 [23]	0
Bit 6	R/W	ADR_MATCH5 [22]	0
Bit 5	R/W	ADR_MATCH5 [21]	0
Bit 4	R/W	ADR_MATCH5 [20]	0
Bit 3	R/W	ADR_MATCH5 [19]	0
Bit 2	R/W	ADR_MATCH5 [18]	0
Bit 1	R/W	ADR_MATCH5 [17]	0
Bit 0	R/W	ADR_MATCH5 [16]	0

ADR_MATCH5[31:16]

The Exact Match Address 5 Mid Word is used for the Mid Word [31:16] of the 48-bit MAC Address that the Address Filter Logic uses to compare on. This register is one of eight separate Exact Match Address registers that the Address Filter Logic can use to compare on.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:09:32 PM

Register 205BH: RXXG Exact Match Address 5 High Word

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH5[47]	0
Bit 14	R/W	ADR_MATCH5 [46]	0
Bit 13	R/W	ADR_MATCH5 [45]	0
Bit 12	R/W	ADR_MATCH5 [44]	0
Bit 11	R/W	ADR_MATCH5 [43]	0
Bit 10	R/W	ADR_MATCH5 [42]	0
Bit 9	R/W	ADR_MATCH5 [41]	0
Bit 8	R/W	ADR_MATCH5 [40]	0
Bit 7	R/W	ADR_MATCH5 [39]	0
Bit 6	R/W	ADR_MATCH5 [38]	0
Bit 5	R/W	ADR_MATCH5 [37]	0
Bit 4	R/W	ADR_MATCH5 [36]	0
Bit 3	R/W	ADR_MATCH5 [35]	0
Bit 2	R/W	ADR_MATCH5 [34]	0
Bit 1	R/W	ADR_MATCH5 [33]	0
Bit 0	R/W	ADR_MATCH5 [32]	0

ADR_MATCH5[47:32]

The Exact Match Address 5 High Word is used for the High Word [47:32] of the 48-bit MAC Address that the Address Filter Logic uses to compare on. This register is one of eight separate Exact Match Address registers that the Address Filter Logic can use to compare on.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:09:32 PM

Register 205CH: RXXG Exact Match Address 6 Low Word

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH6[15]	0
Bit 14	R/W	ADR_MATCH6 [14]	0
Bit 13	R/W	ADR_MATCH6 [13]	0
Bit 12	R/W	ADR_MATCH6 [12]	0
Bit 11	R/W	ADR_MATCH6 [11]	0
Bit 10	R/W	ADR_MATCH6 [10]	0
Bit 9	R/W	ADR_MATCH6 [9]	0
Bit 8	R/W	ADR_MATCH6 [8]	0
Bit 7	R/W	ADR_MATCH6 [7]	0
Bit 6	R/W	ADR_MATCH6 [6]	0
Bit 5	R/W	ADR_MATCH6 [5]	0
Bit 4	R/W	ADR_MATCH6 [4]	0
Bit 3	R/W	ADR_MATCH6 [3]	0
Bit 2	R/W	ADR_MATCH6 [2]	0
Bit 1	R/W	ADR_MATCH6 [1]	0
Bit 0	R/W	ADR_MATCH6 [0]	0

ADR_MATCH6[15:0]

The Exact Match Address 6 Low Word is used for the Low Word [15:0] of the 48-bit MAC Address that the Address Filter Logic uses to compare on. This register is one of eight separate Exact Match Address registers that the Address Filter Logic can use to compare on.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:09:32 PM

Register 205DH: RXXG Exact Match Address 6 Mid Word

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH6[31]	0
Bit 14	R/W	ADR_MATCH6 [30]	0
Bit 13	R/W	ADR_MATCH6 [29]	0
Bit 12	R/W	ADR_MATCH6 [28]	0
Bit 11	R/W	ADR_MATCH6 [27]	0
Bit 10	R/W	ADR_MATCH6 [26]	0
Bit 9	R/W	ADR_MATCH6 [25	0
Bit 8	R/W	ADR_MATCH6 [24]	0
Bit 7	R/W	ADR_MATCH6 [23]	0
Bit 6	R/W	ADR_MATCH6 [22]	0
Bit 5	R/W	ADR_MATCH6 [21]	0
Bit 4	R/W	ADR_MATCH6 [20]	0
Bit 3	R/W	ADR_MATCH6 [19]	0
Bit 2	R/W	ADR_MATCH6 [18]	0
Bit 1	R/W	ADR_MATCH6 [17]	0
Bit 0	R/W	ADR_MATCH6 [16]	0

ADR_MATCH6[31:16]

The Exact Match Address 6 Mid Word is used for the Mid Word [31:16] of the 48-bit MAC Address that the Address Filter Logic uses to compare on. This register is one of eight separate Exact Match Address registers that the Address Filter Logic can use to compare on.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:09:32 PM

Register 205EH: RXXG Exact Match Address 6 High Word

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH6[47]	0
Bit 14	R/W	ADR_MATCH6 [46]	0
Bit 13	R/W	ADR_MATCH6 [45]	0
Bit 12	R/W	ADR_MATCH6 [44]	0
Bit 11	R/W	ADR_MATCH6 [43]	0
Bit 10	R/W	ADR_MATCH6 [42]	0
Bit 9	R/W	ADR_MATCH6 [41]	0
Bit 8	R/W	ADR_MATCH6 [40]	0
Bit 7	R/W	ADR_MATCH6 [39]	0
Bit 6	R/W	ADR_MATCH6 [38]	0
Bit 5	R/W	ADR_MATCH6 [37]	0
Bit 4	R/W	ADR_MATCH6 [36]	0
Bit 3	R/W	ADR_MATCH6 [35]	0
Bit 2	R/W	ADR_MATCH6 [34]	0
Bit 1	R/W	ADR_MATCH6 [33]	0
Bit 0	R/W	ADR_MATCH6 [32]	0

ADR_MATCH6[47:32]

The Exact Match Address 6 High Word is used for the High Word [47:32] of the 48-bit MAC Address that the Address Filter Logic uses to compare on. This register is one of eight separate Exact Match Address registers that the Address Filter Logic can use to compare on.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:09:32 PM

Register 205FH: RXXG Exact Match Address 7 Low Word

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH7[15]	0
Bit 14	R/W	ADR_MATCH7 [14]	0
Bit 13	R/W	ADR_MATCH7 [13]	0
Bit 12	R/W	ADR_MATCH7 [12]	0
Bit 11	R/W	ADR_MATCH7 [11]	0
Bit 10	R/W	ADR_MATCH7 [10]	0
Bit 9	R/W	ADR_MATCH7 [9]	0
Bit 8	R/W	ADR_MATCH7 [8]	0
Bit 7	R/W	ADR_MATCH7 [7]	0
Bit 6	R/W	ADR_MATCH7 [6]	0
Bit 5	R/W	ADR_MATCH7 [5]	0
Bit 4	R/W	ADR_MATCH7 [4]	0
Bit 3	R/W	ADR_MATCH7 [3]	0
Bit 2	R/W	ADR_MATCH7 [2]	0
Bit 1	R/W	ADR_MATCH7 [1]	0
Bit 0	R/W	ADR_MATCH7 [0]	0

ADR_MATCH7[15:0]

The Exact Match Address 7 Low Word is used for the Low Word [15:0] of the 48-bit MAC Address that the Address Filter Logic uses to compare on. This register is one of eight separate Exact Match Address registers that the Address Filter Logic can use to compare on.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:09:32 PM

Register 2060H: RXXG Exact Match Address 7 Mid Word

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH7[31]	0
Bit 14	R/W	ADR_MATCH7 [30]	0
Bit 13	R/W	ADR_MATCH7 [29]	0
Bit 12	R/W	ADR_MATCH7 [28]	0
Bit 11	R/W	ADR_MATCH7 [27]	0
Bit 10	R/W	ADR_MATCH7 [26]	0
Bit 9	R/W	ADR_MATCH7 [25	0
Bit 8	R/W	ADR_MATCH7 [24]	0
Bit 7	R/W	ADR_MATCH7 [23]	0
Bit 6	R/W	ADR_MATCH7 [22]	0
Bit 5	R/W	ADR_MATCH7 [21]	0
Bit 4	R/W	ADR_MATCH7 [20]	0
Bit 3	R/W	ADR_MATCH7 [19]	0
Bit 2	R/W	ADR_MATCH7 [18]	0
Bit 1	R/W	ADR_MATCH7 [17]	0
Bit 0	R/W	ADR_MATCH7 [16]	0

ADR_MATCH7[31:16]

The Exact Match Address 7 Mid Word is used for the Mid Word [31:16] of the 48-bit MAC Address that the Address Filter Logic uses to compare on. This register is one of eight separate Exact Match Address registers that the Address Filter Logic can use to compare on.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:09:32 PM

Register 2061H: RXXG Exact Match Address 7 High Word

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH7[47]	0
Bit 14	R/W	ADR_MATCH7 [46]	0
Bit 13	R/W	ADR_MATCH7 [45]	0
Bit 12	R/W	ADR_MATCH7 [44]	0
Bit 11	R/W	ADR_MATCH7 [43]	0
Bit 10	R/W	ADR_MATCH7 [42]	0
Bit 9	R/W	ADR_MATCH7 [41]	0
Bit 8	R/W	ADR_MATCH7 [40]	0
Bit 7	R/W	ADR_MATCH7 [39]	0
Bit 6	R/W	ADR_MATCH7 [38]	0
Bit 5	R/W	ADR_MATCH7 [37]	0
Bit 4	R/W	ADR_MATCH7 [36]	0
Bit 3	R/W	ADR_MATCH7 [35]	0
Bit 2	R/W	ADR_MATCH7 [34]	0
Bit 1	R/W	ADR_MATCH7 [33]	0
Bit 0	R/W	ADR_MATCH7 [32]	0

ADR_MATCH7[47:32]

The Exact Match Address 7 High Word is used for the High Word [47:32] of the 48-bit MAC Address that the Address Filter Logic uses to compare on. This register is one of eight separate Exact Match Address registers that the Address Filter Logic can use to compare on.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:09:32 PM

Register 2062H: RXXG Exact Match VID 0

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	VID_MATCH0[11]	0
Bit 10	R/W	VID_MATCH0[10]	0
Bit 9	R/W	VID_MATCH0[9]	0
Bit 8	R/W	VID_MATCH0[8]	0
Bit 7	R/W	VID_MATCH0[7]	0
Bit 6	R/W	VID_MATCH0[6]	0
Bit 5	R/W	VID_MATCH0[5]	0
Bit 4	R/W	VID_MATCH0[4]	0
Bit 3	R/W	VID_MATCH0[3]	0
Bit 2	R/W	VID_MATCH0[2]	0
Bit 1	R/W	VID_MATCH0[1]	0
Bit 0	R/W	VID_MATCH0[0]	0

VID_MATCH0[11:0]

The Exact Match VID 0 register is used by the Address Filter Logic to compare on the 12 bit VID field on VLAN tagged frames. This register is one of eight separate Exact Match VID registers that the Address Filter Logic can use to compare on.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer India Wednesday, 07 February, 2007 06:09:32 PM

Register 2063H: RXXG Exact Match VID 1

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	VID_MATCH1[11]	0
Bit 10	R/W	VID_MATCH1[10]	0
Bit 9	R/W	VID_MATCH1[9]	0
Bit 8	R/W	VID_MATCH1[8]	0
Bit 7	R/W	VID_MATCH1[7]	0
Bit 6	R/W	VID_MATCH1[6]	0
Bit 5	R/W	VID_MATCH1[5]	0
Bit 4	R/W	VID_MATCH1[4]	0
Bit 3	R/W	VID_MATCH1[3]	0
Bit 2	R/W	VID_MATCH1[2]	0
Bit 1	R/W	VID_MATCH1[1]	0
Bit 0	R/W	VID_MATCH1[0]	0

VID_MATCH1[11:0]

The Exact Match VID 1 register is used by the Address Filter Logic to compare on the 12 bit VID field on VLAN tagged frames. This register is one of eight separate Exact Match VID registers that the Address Filter Logic can use to compare on.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer India, Wednesday, 07 February, 2007 06:09:32 PM

Register 2064H: RXXG Exact Match VID 2

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	VID_MATCH2[11]	0
Bit 10	R/W	VID_MATCH2[10]	0
Bit 9	R/W	VID_MATCH2[9]	0
Bit 8	R/W	VID_MATCH2[8]	0
Bit 7	R/W	VID_MATCH2[7]	0
Bit 6	R/W	VID_MATCH2[6]	0
Bit 5	R/W	VID_MATCH2[5]	0
Bit 4	R/W	VID_MATCH2[4]	0
Bit 3	R/W	VID_MATCH2[3]	0
Bit 2	R/W	VID_MATCH2[2]	0
Bit 1	R/W	VID_MATCH2[1]	0
Bit 0	R/W	VID_MATCH2[0]	0

VID_MATCH2[11:0]

The Exact Match VID 2 register is used by the Address Filter Logic to compare on the 12 bit VID field on VLAN tagged frames. This register is one of eight separate Exact Match VID registers that the Address Filter Logic can use to compare on.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer India, Wednesday, 07 February, 2007 06:09:32 PM

Register 2065H: RXXG Exact Match VID 3

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	VID_MATCH3[11]	0
Bit 10	R/W	VID_MATCH3[10]	0
Bit 9	R/W	VID_MATCH3[9]	0
Bit 8	R/W	VID_MATCH3[8]	0
Bit 7	R/W	VID_MATCH3[7]	0
Bit 6	R/W	VID_MATCH3[6]	0
Bit 5	R/W	VID_MATCH3[5]	0
Bit 4	R/W	VID_MATCH3[4]	0
Bit 3	R/W	VID_MATCH3[3]	0
Bit 2	R/W	VID_MATCH3[2]	0
Bit 1	R/W	VID_MATCH3[1]	0
Bit 0	R/W	VID_MATCH3[0]	0

VID_MATCH3[11:0]

The Exact Match VID 3 register is used by the Address Filter Logic to compare on the 12 bit VID field on VLAN tagged frames. This register is one of eight separate Exact Match VID registers that the Address Filter Logic can use to compare on.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer India, Wednesday, 07 February, 2007 06:09:32 PM

Register 2066H: RXXG Exact Match VID 4

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	VID_MATCH4[11]	0
Bit 10	R/W	VID_MATCH4[10]	0
Bit 9	R/W	VID_MATCH4[9]	0
Bit 8	R/W	VID_MATCH4[8]	0
Bit 7	R/W	VID_MATCH4[7]	0
Bit 6	R/W	VID_MATCH4[6]	0
Bit 5	R/W	VID_MATCH4[5]	0
Bit 4	R/W	VID_MATCH4[4]	0
Bit 3	R/W	VID_MATCH4[3]	0
Bit 2	R/W	VID_MATCH4[2]	0
Bit 1	R/W	VID_MATCH4[1]	0
Bit 0	R/W	VID_MATCH4[0]	0

VID_MATCH4[11:0]

The Exact Match VID 4 register is used by the Address Filter Logic to compare on the 12 bit VID field on VLAN tagged frames. This register is one of eight separate Exact Match VID registers that the Address Filter Logic can use to compare on.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer India, Wednesday, 07 February, 2007 06:09:32 PM

Register 2067H: RXXG Exact Match VID 5

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	VID_MATCH5[11]	0
Bit 10	R/W	VID_MATCH5[10]	0
Bit 9	R/W	VID_MATCH5[9]	0
Bit 8	R/W	VID_MATCH5[8]	0
Bit 7	R/W	VID_MATCH5[7]	0
Bit 6	R/W	VID_MATCH5[6]	0
Bit 5	R/W	VID_MATCH5[5]	0
Bit 4	R/W	VID_MATCH5[4]	0
Bit 3	R/W	VID_MATCH5[3]	0
Bit 2	R/W	VID_MATCH5[2]	0
Bit 1	R/W	VID_MATCH5[1]	0
Bit 0	R/W	VID_MATCH5[0]	0

VID_MATCH5[11:0]

The Exact Match VID 5 register is used by the Address Filter Logic to compare on the 12 bit VID field on VLAN tagged frames. This register is one of eight separate Exact Match VID registers that the Address Filter Logic can use to compare on.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer India, Wednesday, 07 February, 2007 06:09:32 PM

Register 2068H: RXXG Exact Match VID 6

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	VID_MATCH6[11]	0
Bit 10	R/W	VID_MATCH6[10]	0
Bit 9	R/W	VID_MATCH6[9]	0
Bit 8	R/W	VID_MATCH6[8]	0
Bit 7	R/W	VID_MATCH6[7]	0
Bit 6	R/W	VID_MATCH6[6]	0
Bit 5	R/W	VID_MATCH6[5]	0
Bit 4	R/W	VID_MATCH6[4]	0
Bit 3	R/W	VID_MATCH6[3]	0
Bit 2	R/W	VID_MATCH6[2]	0
Bit 1	R/W	VID_MATCH6[1]	0
Bit 0	R/W	VID_MATCH6[0]	0

VID_MATCH6[11:0]

The Exact Match VID 6 register is used by the Address Filter Logic to compare on the 12 bit VID field on VLAN tagged frames. This register is one of eight separate Exact Match VID registers that the Address Filter Logic can use to compare on.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer India Wednesday, 07 February, 2007 06:09:32 PM

Register 2069H: RXXG Exact Match VID 7

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	VID_MATCH7[11]	0
Bit 10	R/W	VID_MATCH7[10]	0
Bit 9	R/W	VID_MATCH7[9]	0
Bit 8	R/W	VID_MATCH7[8]	0
Bit 7	R/W	VID_MATCH7[7]	0
Bit 6	R/W	VID_MATCH7[6]	0
Bit 5	R/W	VID_MATCH7[5]	0
Bit 4	R/W	VID_MATCH7[4]	0
Bit 3	R/W	VID_MATCH7[3]	0
Bit 2	R/W	VID_MATCH7[2]	0
Bit 1	R/W	VID_MATCH7[1]	0
Bit 0	R/W	VID_MATCH7[0]	0

VID_MATCH7[11:0]

The Exact Match VID 7 register is used by the Address Filter Logic to compare on the 12 bit VID field on VLAN tagged frames. This register is one of eight separate Exact Match VID registers that the Address Filter Logic can use to compare on.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer India Wednesday, 07 February, 2007 06:09:32 PM

Register 206AH: RXXG Multicast HASH Low Word

Bit	Type	Function	Default
Bit 15	R/W	MHASH[15]	0
Bit 14	R/W	MHASH[14]	0
Bit 13	R/W	MHASH[13]	0
Bit 12	R/W	MHASH[12]	0
Bit 11	R/W	MHASH[11]	0
Bit 10	R/W	MHASH[10]	0
Bit 9	R/W	MHASH[9]	0
Bit 8	R/W	MHASH[8]	0
Bit 7	R/W	MHASH[7]	0
Bit 6	R/W	MHASH[6]	0
Bit 5	R/W	MHASH[5]	0
Bit 4	R/W	MHASH[4]	0
Bit 3	R/W	MHASH[3]	0
Bit 2	R/W	MHASH[2]	0
Bit 1	R/W	MHASH[1]	0
Bit 0	R/W	MHASH[0]	0

MHASH[15:0]

The MHASH[15:0] is the Low Word of the 64-bit Multicast Hash bin. This is used by the Address Filter Logic for filtering of Multicast Addressed frames when MHASH_EN is ‘1’ in Address Filter Control 2 register.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:09:32 PM

Register 206BH: RXXG Multicast HASH MidLow Word

Bit	Type	Function	Default
Bit 15	R/W	MHASH[31]	0
Bit 14	R/W	MHASH[30]	0
Bit 13	R/W	MHASH[29]	0
Bit 12	R/W	MHASH[28]	0
Bit 11	R/W	MHASH[27]	0
Bit 10	R/W	MHASH[26]	0
Bit 9	R/W	MHASH[25]	0
Bit 8	R/W	MHASH[24]	0
Bit 7	R/W	MHASH[23]	0
Bit 6	R/W	MHASH[22]	0
Bit 5	R/W	MHASH[21]	0
Bit 4	R/W	MHASH[20]	0
Bit 3	R/W	MHASH[19]	0
Bit 2	R/W	MHASH[18]	0
Bit 1	R/W	MHASH[17]	0
Bit 0	R/W	MHASH[16]	0

MHASH[31:16]

The MHASH[31:16] is the MidLow Word of the 64-bit Multicast Hash bin. This is used by the Address Filter Logic for filtering of Multicast Addressed frames when MHASH_EN is '1' in Address Filter Control 2 register.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:09:32 PM

Register 206CH: RXXG Multicast HASH MidHigh Word

Bit	Type	Function	Default
Bit 15	R/W	MHASH[47]	0
Bit 14	R/W	MHASH[46]	0
Bit 13	R/W	MHASH[45]	0
Bit 12	R/W	MHASH[44]	0
Bit 11	R/W	MHASH[43]	0
Bit 10	R/W	MHASH[42]	0
Bit 9	R/W	MHASH[41]	0
Bit 8	R/W	MHASH[40]	0
Bit 7	R/W	MHASH[39]	0
Bit 6	R/W	MHASH[38]	0
Bit 5	R/W	MHASH[37]	0
Bit 4	R/W	MHASH[36]	0
Bit 3	R/W	MHASH[35]	0
Bit 2	R/W	MHASH[34]	0
Bit 1	R/W	MHASH[33]	0
Bit 0	R/W	MHASH[32]	0

MHASH[47:32]

The MHASH[47:32] is the MidHigh Word of the 64-bit Multicast Hash bin. This is used by the Address Filter Logic for filtering of Multicast Addressed frames when MHASH_EN is '1' in Address Filter Control 2 register.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:09:32 PM

Register 206DH: RXXG Multicast HASH High Word

Bit	Type	Function	Default
Bit 15	R/W	MHASH[63]	0
Bit 14	R/W	MHASH[62]	0
Bit 13	R/W	MHASH[61]	0
Bit 12	R/W	MHASH[60]	0
Bit 11	R/W	MHASH[59]	0
Bit 10	R/W	MHASH[58]	0
Bit 9	R/W	MHASH[57]	0
Bit 8	R/W	MHASH[56]	0
Bit 7	R/W	MHASH[55]	0
Bit 6	R/W	MHASH[54]	0
Bit 5	R/W	MHASH[53]	0
Bit 4	R/W	MHASH[52]	0
Bit 3	R/W	MHASH[51]	0
Bit 2	R/W	MHASH[50]	0
Bit 1	R/W	MHASH[49]	0
Bit 0	R/W	MHASH[48]	0

MHASH[63:48]

The MHASH[63:48] is the High Word of the 64-bit Multicast Hash bin. This is used by the Address Filter Logic for filtering of Multicast Addressed frames when MHASH_EN is ‘1’ in Address Filter Control 2 register.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:09:32 PM

Register 206EH: RXXG Address Filter Control 0

Bit	Type	Function	Default
Bit 15	R/W	ADRFILT_CTRL3[3]	0
Bit 14	R/W	ADRFILT_CTRL3[2]	0
Bit 13	R/W	ADRFILT_CTRL3[1]	0
Bit 12	R/W	ADRFILT_CTRL3[0]	0
Bit 11	R/W	ADRFILT_CTRL2[3]	0
Bit 10	R/W	ADRFILT_CTRL2[2]	0
Bit 9	R/W	ADRFILT_CTRL2[1]	0
Bit 8	R/W	ADRFILT_CTRL2[1]	0
Bit 7	R/W	ADRFILT_CTRL1[3]	0
Bit 6	R/W	ADRFILT_CTRL1[2]	0
Bit 5	R/W	ADRFILT_CTRL1[1]	0
Bit 4	R/W	ADRFILT_CTRL1[0]	0
Bit 3	R/W	ADRFILT_CTRL0[3]	0
Bit 2	R/W	ADRFILT_CTRL0[2]	0
Bit 1	R/W	ADRFILT_CTRL0[1]	0
Bit 0	R/W	ADRFILT_CTRL0[0]	0

The Address Filter Control 0 register contains the Control bits for the first 4 filters 0-3. Each filter needs 4 bits of control information.

ADRFILT_CTRLx[3]

Forward Enable bit. When this bit is ‘1’, the Address Filter Logic will only **accept** frames that match the corresponding Exact Match Address register, and if the VLAN enable bit is set the corresponding VID_MATCH register. All other frames are filtered. When this bit is ‘0’, the Address Filter Logic will only **discard** frames that match the corresponding Exact Match Address register, and if the VLAN enable bit is set the corresponding VID_MATCH register. All other frames are filtered.

ADRFILT_CTRLx[2]

VLAN Enable bit. When this bit is ‘1’, the Address Filter Logic will use the corresponding 12-bit VID_MATCH register along with the corresponding Exact Match Address register to perform the compare. When this bit is ‘0’, the Address Filter logic will only use the corresponding Exact Match Address register to perform the compare.

ADRFILT_CTRLx[1]

Source Address Enable bit. When this bit is ‘0’, the Address Filter Logic will use the Destination Address to perform a compare to the corresponding Exact Match Address register. When this bit is ‘1’, the Address Filter Logic will use the Source Address to perform a compare to the corresponding Exact Match Address register.

Downloaded by Content Team of Parts Engine on Wednesday, 07 February, 2007 06:09:32 PM

ADRFILT_CTRLx[0]

Match Enable bit. When this bit is ‘0’, the Address Filter Logic will not use the corresponding filter. When this bit is ‘1’, the Address Filter Logic will use the corresponding filter based on ADRFILT_CTRLx[3:1]. This bit must be written to ‘0’ before making any updates to the corresponding Exact Match Address and VID registers., and can then be written as ‘1’ again.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2001 06:57:32 PM

Register 206FH: RXXG Address Filter Control 1

Bit	Type	Function	Default
Bit 15	R/W	ADRFILT_CTRL7[3]	0
Bit 14	R/W	ADRFILT_CTRL7[2]	0
Bit 13	R/W	ADRFILT_CTRL7[1]	0
Bit 12	R/W	ADRFILT_CTRL7[0]	0
Bit 11	R/W	ADRFILT_CTRL6[3]	0
Bit 10	R/W	ADRFILT_CTRL6[2]	0
Bit 9	R/W	ADRFILT_CTRL6[1]	0
Bit 8	R/W	ADRFILT_CTRL6[1]	0
Bit 7	R/W	ADRFILT_CTRL5[3]	0
Bit 6	R/W	ADRFILT_CTRL5[2]	0
Bit 5	R/W	ADRFILT_CTRL5[1]	0
Bit 4	R/W	ADRFILT_CTRL5[0]	0
Bit 3	R/W	ADRFILT_CTRL4[3]	0
Bit 2	R/W	ADRFILT_CTRL4[2]	0
Bit 1	R/W	ADRFILT_CTRL4[1]	0
Bit 0	R/W	ADRFILT_CTRL4[0]	0

The Address Filter Control 1 register contains the Control bits for the second 4 filters 4-7. Each filter needs 4 bits of control information.

ADRFILT_CTRLx[3]

Forward Enable bit. When this bit is ‘1’, the Address Filter Logic will only **accept** frames that match the corresponding Exact Match Address register, and if the VLAN enable bit is set the corresponding VID_MATCH register. All other frames are filtered. When this bit is ‘0’, the Address Filter Logic will only **discard** frames that match the corresponding Exact Match Address register, and if the VLAN enable bit is set the corresponding VID_MATCH register. All other frames are filtered.

ADRFILT_CTRLx[2]

VLAN Enable bit. When this bit is ‘1’, the Address Filter Logic will use the corresponding 12-bit VID_MATCH register along with the corresponding Exact Match Address register to perform the compare. When this bit is ‘0’, the Address Filter logic will only use the corresponding Exact Match Address register to perform the compare.

ADRFILT_CTRLx[1]

Source Address Enable bit. When this bit is ‘0’, the Address Filter Logic will use the Destination Address to perform a compare to the corresponding Exact Match Address register. When this bit is ‘1’, the Address Filter Logic will use the Source Address to perform a compare to the corresponding Exact Match Address register.

Downloaded by Content Team of PMC-Sierra Inc on Wednesday, 07 February, 2007 06:09:32 PM

ADRFILT_CTRLx[0]

Match Enable bit. When this bit is ‘0’, the Address Filter Logic will not use the corresponding filter. When this bit is ‘1’, the Address Filter Logic will use the corresponding filter based on ADRFILT_CTRLx[3:1]. This bit must be written to ‘0’ before making any updates to the corresponding Exact Match Address and VID registers., and can then be written as ‘1’ again.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2001 06:57:32 PM

Register 2070H: RXXG Address Filter Control 2

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R/W	PMODE	1
Bit 0	R/W	MHASH_EN	0

MHASH_EN

Multicast Hash Filter Enable. When this bit is '1', the 64-bit Multicast Hash Filter function will look at all Multicast -addressed frames for filter processing. When this bit is '0', no Multicast Hash look-ups are performed.

PMODE

Promiscuous Mode. When this bit is '1', the PM5390 will allow all frames to pass through to the PL4 interface regardless of the DA/SA Addresses, unless Address Filtering Logic is enabled and there is a match to filter the incoming frame based on the DA/SA/VID fields. When this bit is '0', the PM5390 will not allow any frames to pass through to the PL4 interface unless Address Filtering Logic is enabled and there is a match to the incoming frame.

Note: Please refer to the operation section for proper use of these registers.

Downloaded by Content Team @ Partsimer Inc. on Wednesday, 07 February, 2007 06:09:32 PM

Register 2071H: RXXG Line Filter Error Counter

Bit	Type	Function	Default
Bit 15	R/W	FILTER_ERROR[15]	0
Bit 14	R/W	FILTER_ERROR[14]	0
Bit 13	R/W	FILTER_ERROR[13]	0
Bit 12	R/W	FILTER_ERROR[12]	0
Bit 11	R/W	FILTER_ERROR[11]	0
Bit 10	R/W	FILTER_ERROR[10]	0
Bit 9	R/W	FILTER_ERROR[9]	0
Bit 8	R/W	FILTER_ERROR[8]	0
Bit 7	R/W	FILTER_ERROR[7]	0
Bit 6	R/W	FILTER_ERROR[6]	0
Bit 5	R/W	FILTER_ERROR[5]	0
Bit 4	R/W	FILTER_ERROR[4]	0
Bit 3	R/W	FILTER_ERROR[3]	0
Bit 2	R/W	FILTER_ERROR[2]	0
Bit 1	R/W	FILTER_ERROR[1]	0
Bit 0	R/W	FILTER_ERROR[0]	0

FILTER_ERROR[15:0]

The FILTER_ERROR[15:0] register indicates the number of packets that were filtered by the Line Interface during the last accumulation interval.

A write to any one of the bits in this register loads the register with the current filter error counter value and resets the internal 16 bit counter. The counter reset value is dependant on the number of count events during the transfer. The counter should be polled regularly to avoid saturating. The contents of this register are valid three TCLK cycles after a transfer is triggered by a write to any of the bits in the register.

This counter can also be loaded by a microprocessor write to the S/UNI 9953 Identity and Global Performance Monitor Update register (0000H).

Downloaded by Content Team on Patton Inc @ Wednesday, 07 February 2007 06:09:32 PM

12.22 Receive 64B/66B Processor (R64B66B)

Register 2080H: R64B66B Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R/W	TIP	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	JITTER_PATTERN_SLCT	0
Bit 10	R/W	JITTER_TEST_ENABLE	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	1
Bit 2	R/W	Reserved	0
Bit 1	R/W	INT_EN	0
Bit 0	R/W	Reserved	1

INT_EN

When ‘1’, the Interrupts are enabled.

When ‘0’, the Interrupts are disabled.

Setting this bit to a logic 1 allows the propagation of the interrupt to the Master Payload Interrupt Status register (0010H).

JITTER_TEST_ENABLE

Setting this bit to ‘1’ enables jitter test mode. This disables the BER and Receive state machines.

JITTER_PATTERN_SLCT

Setting this to ‘1’ causes the R64B66B to look for the all zeroes pattern (128 zeroes). Setting it to ‘0’ causes it to look for one of the three local fault patterns, types 0x2d, 0x4b, and 0x55. Type 0x66 is omitted because it codes for start of frame.

Downloaded by Content Team of Pericom Inc on Wednesday, 07 February, 2007 06:59:32 PM

TIP

Writing a ‘1’ to this bit copies the current value of registers 0x2083 – 0x2087 to a set of shadow registers. When this bit is read as ‘1’ the transfer is still in progress. When this bit is read as ‘0’, the transfer is complete.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 2081H: R64B66B Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	LINK_FAILE	0
Bit 4	R/W	RX_LFE	0
Bit 3	R/W	RX_RFE	0
Bit 2	R/W	RX_LOSE	0
Bit 1	R/W	HI_BERE	0
Bit 0	R/W	SYNC_ERRE	0

SYNC_ERRE, HI_BERE, RX_LOSE, RX_RFE, RX_LFE, LINK_FAILE

The interrupt enable bit controls the activation of the interrupt (INTB) output. When the interrupt enable bit is set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When the interrupt enable bit is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

Note that the INTB output will only be asserted if the INTE bit in the Master Payload Interrupt Status register (0010H) is enabled.

Downloaded by Content Team of Partsriver on Wednesday, 07 February, 2007 06:59:32 PM

Register 2082H: R64B66B Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R	LINK_FAILI	X
Bit 4	R	RX_LFI	X
Bit 3	R	RX_RFI	X
Bit 2	R	RX_LOSI	X
Bit 1	R	HI_BERI	X
Bit 0	R	SYNC_ERRI	X

If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, these interrupt status bits are cleared on write with a logic 1. Otherwise, these interrupt status bits are cleared on read.

SYNC_ERRI

When ‘1’, it indicates that the SYNC_ERR input is asserted due to a loss of signal from the optics or the SONET/SDH processor is unable to recover payload. SYNC_ERRI is cleared to logic 0 when this register is read or written as described above.

HI_BERI

When ‘1’, it indicates that the BER state machine has entered a High Bit-Error-Rate state. HI_BERI is cleared to logic 0 when this register is read or written as described above.

When ‘0’, it indicates that the BER is below 16 errors per 125us period.

RX_LOSI

When ‘1’, it indicates that the R64B66B has entered a Loss Of 64b/66b code-group Synchronization state. RX_LOSI is cleared to logic 0 when this register is read or written as described above.

Downloaded by Content Team of Partsrepublic Inc on Wednesday, 07 February, 2007 06:59:32 PM

RX_RFI

When ‘1’, it indicates that the R64B66B block has just received at least 3 Remote Fault messages. RX_RFI is cleared to logic 0 when this register is read or written as described above.

RX_LFI

When ‘1’, it indicates that the R64B66B block has just received at least 3 Local Fault messages. RX_LFI is cleared to logic 0 when this register is read or written as described above.

LINK_FAILI

When ‘1’, it indicates that the R64B66B link has failed due to either Loss of Code Group Synchronization or a Local Fault status was observed. LINK_FAILI is cleared to logic 0 when this register is read or written as described above.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 AM

Register 2083H: R64B66B Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R	LINK_FAIL	X
Bit 4	R	RX_LF	X
Bit 3	R	RX_RF	X
Bit 2	R	RX_LOS	X
Bit 1	R	HI_BER	X
Bit 0	R	SYNC_ERR	X

SYNC_ERR

When ‘1’, it indicates that the SYNC_ERR input is asserted due to a loss of signal from the optics or the SONET/SDH processor is unable to recover payload.

When ‘0’, it indicates that the SYNC_ERR input is de-asserted and the SONET/SDH processor is able to recover payload.

HI_BER

When ‘1’, it indicates that the BER state machine has entered a High Bit-Error-Rate state.

When ‘0’, it indicates that the BER is below 16 errors per 125us period.

RX_LOS

When ‘1’, it indicates that the R64B66B has entered a Loss Of 64b/66b code-group Synchronization state.

When ‘0’, it indicates that the R64B66B is able to process the received 64b/66b code.

Downloaded by Corlent Team of Hartmintinc on Wednesday, 07 February, 2007 06:59:32 PM

RX_RF

When ‘1’, it indicates that the R64B66B block has just received at least 3 Remote Fault messages.

When ‘0’, it indicates that there was an absence of Remote Fault messages for at least 6 TCLK cycles.

RX_LF

When ‘1’, it indicates that the R64B66B block has just received at least 3 Local Fault messages.

When ‘0’, it indicates that there was an absence of Local Fault messages for at least 6 TCLK cycles.

LINK_FAIL

When ‘1’, it indicates that the R64B66B link has failed due to either Loss of Code Group Synchronization or a Local Fault status was observed.

When ‘0’, it indicates that the Receive State Machine is receiving good data.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 2084H: R64B66B Error Frame Count

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	ERROR_FRAME_CNT[7]	X
Bit 6	R	ERROR_FRAME_CNT[6]	X
Bit 5	R	ERROR_FRAME_CNT[5]	X
Bit 4	R	ERROR_FRAME_CNT[4]	X
Bit 3	R	ERROR_FRAME_CNT[3]	X
Bit 2	R	ERROR_FRAME_CNT[2]	X
Bit 1	R	ERROR_FRAME_CNT[1]	X
Bit 0	R	ERROR_FRAME_CNT[0]	X

ERROR_FRAME_CNT[7:0]

These bits indicate the number of invalid PCS code sequences detected in the Ingress path. The counter only increments when the R64B66B block is in a SYNC'd state. The counter should be polled regularly to avoid saturating. The counter can saturate at values 0x00FE or 0x00FF. This register is cleared on read.

Downloaded by Content Team of Partminer on Wednesday, February 07, 2007 06:09:32 PM

Register 2085H: R64B66B Frame Lock Count

Bit	Type	Function	Default
Bit 15	R	FRAME_LOCK_CNT[15]	X
Bit 14	R	FRAME_LOCK_CNT[14]	X
Bit 13	R	FRAME_LOCK_CNT[13]	X
Bit 12	R	FRAME_LOCK_CNT[12]	X
Bit 11	R	FRAME_LOCK_CNT[11]	X
Bit 10	R	FRAME_LOCK_CNT[10]	X
Bit 9	R	FRAME_LOCK_CNT[9]	X
Bit 8	R	FRAME_LOCK_CNT[8]	X
Bit 7	R	FRAME_LOCK_CNT[7]	X
Bit 6	R	FRAME_LOCK_CNT[6]	X
Bit 5	R	FRAME_LOCK_CNT[5]	X
Bit 4	R	FRAME_LOCK_CNT[4]	X
Bit 3	R	FRAME_LOCK_CNT[3]	X
Bit 2	R	FRAME_LOCK_CNT[2]	X
Bit 1	R	FRAME_LOCK_CNT[1]	X
Bit 0	R	FRAME_LOCK_CNT[0]	X

FRAME_LOCK_CNT[5:0]

These bits indicate the number times the Synchronizer state machine has gone from a non-sync'd state to a sync'd state. The counter should be polled regularly to avoid saturating. The counter can saturate at values 0xFFFF or 0xFFFE. This register is cleared on read.

Downloaded by Content Team of Partminer Inc. on Wednesday, February 21 2007 06:59:32 PM

Register 2086H: R64B66B Bit Error Count

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R	HI_BER_CNT[5]	X
Bit 4	R	HI_BER_CNT[4]	X
Bit 3	R	HI_BER_CNT[3]	X
Bit 2	R	HI_BER_CNT[2]	X
Bit 1	R	HI_BER_CNT[1]	X
Bit 0	R	HI_BER_CNT[0]	X

HI_BER_CNT[5:0]

These bits indicate the number of Bit errors during a 125us interval. The counter resets to zero after every 125us. The counter only increments when the R64B66B block is in a SYNC'd state. This register is cleared on read.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:59:32 PM

Register 0x2087H: R64B66B JITTER_CNT[15:0]

Bit	Type	Function	Default
Bit 15	R	JITTER_CNT[15]	X
Bit 14	R	JITTER_CNT[14]	X
Bit 13	R	JITTER_CNT[13]	X
Bit 12	R	JITTER_CNT[12]	X
Bit 11	R	JITTER_CNT[11]	X
Bit 10	R	JITTER_CNT[10]	X
Bit 9	R	JITTER_CNT[9]	X
Bit 8	R	JITTER_CNT[8]	X
Bit 7	R	JITTER_CNT[7]	X
Bit 6	R	JITTER_CNT[6]	X
Bit 5	R	JITTER_CNT[5]	X
Bit 4	R	JITTER_CNT[4]	X
Bit 3	R	JITTER_CNT[3]	X
Bit 2	R	JITTER_CNT[2]	X
Bit 1	R	JITTER_CNT[1]	X
Bit 0	R	JITTER_CNT[0]	X

JITTER_CNT[15:0]

Putting the R64B66B into jitter mode (JITTER_TEST_ENABLE=1) enables this counter. This counter is incremented for every unscrambled 66 bit frame that doesn't match the expected frame data. The expected frame type is set by JITTER_PATTERN_SLCT. This register is cleared upon read. See section 49.2.12 of the IEEE 802.3ae standard for a description of the receive jitter algorithm. The counter can saturate at values 0xFFFF or 0xFFFE.

Downloaded by Content Team of Partminer on Wednesday, 07 February 2007 06:59:32 PM

12.23 Management Statistics (MSTAT)

Register 2100H: MSTAT Control

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R	Reserved	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	Reserved	0
Bit 4	R	Reserved	0
Bit 3	R	Reserved	0
Bit 2	R/W	WRITE	0
Bit 1	R/W	CLEAR	0
Bit 0	R/W	SNAP	0

The MSTAT Control Register provides general control over the MSTAT.

SNAP

The SNAP bit is used to snap all management statistics counters into their complimentary system probe shadow registers for full static system probes. The SNAP bit will perform the copy operation when set high (logic 1). The SNAP bit will automatically clear itself to low (logic 0) after the operation completes.

Note that the MSTAT counters themselves will NOT clear when setting the SNAP bit. The software needs only to check for rollover and keep a count greater than 40 bits.

CLEAR

The CLEAR bit is used to clear all management statistic registers. The CLEAR bit clears all registers when set high (logic 1). The CLEAR bit will automatically clear itself to low (logic 0) after the operation completes.

Downloaded by Content Team of Packet Inc on Wednesday, 07 February, 2007 06:59:32 PM

WRITE

The WRITE bit is used to initiate a data update write to the selected counter indicated by the MSTAT Counter Write Address Register. The contents of the MSTAT Counter Write Data Registers will be copied into the associative counter. The write is initiated by setting this bit high (logic 1). The WRITE bit will automatically clear itself to low (logic 0) after the operation completes.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:58:22 AM

Register 2101H: MSTAT Counter Rollover 0

Bit	Type	Function	Default
Bit 15	R	FramesTooLongErrors	0
Bit 14	R	Reserved	0
Bit 13	R	InRangeLengthErrors	0
Bit 12	R	SymbolError	0
Bit 11	R	FramesLostDueToInternal MACError	0
Bit 10	R	FrameCheckSequence Errors	0
Bit 9	R	MACControlFrameReceived	0
Bit 8	R	PAUSEMACControlFrame Received	0
Bit 7	R	TaggedFramesReceivedOK	0
Bit 6	R	BroadcastFramesReceivedOK	0
Bit 5	R	MulticastFramesReceived OK	0
Bit 4	R	UnicastFramesReceivedOK	0
Bit 3	R	OctetsReceived	0
Bit 2	R	FramesReceived	0
Bit 1	R	OctetsReceivedOK	0
Bit 0	R	FramesReceivedOK	0

The MSTAT Counter Rollover Registers provide indication of counter roll over conditions. The register bit remains set until the register is read. Reading this register clears all bits within this register.

Downloaded by Content Team of Partminer Inc on Monday, 26 February 2007 06:59:32 PM

Register 2102H: MSTAT Counter Rollover 1

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	FilteredBroadcastFrames	0
Bit 13	R	FilteredMulticastFrames	0
Bit 12	R	FilteredUnicastFrames	0
Bit 11	R	FilteredOctets	0
Bit 10	R	JumboOctetsReceivedOK	0
Bit 9	R	ReceiveFrames1519to MAXOctets	0
Bit 8	R	ReceiveFrames1024to 1518Octets	0
Bit 7	R	ReceiveFrames512to 1023Octets	0
Bit 6	R	ReceiveFrames256to 511Octets	0
Bit 5	R	ReceiveFrames128to 255Octets	0
Bit 4	R	ReceiveFrames65to 127Octets	0
Bit 3	R	ReceiveFrames64Octets	0
Bit 2	R	UndersizedFrames	0
Bit 1	R	Fragments	0
Bit 0	R	Jabbers	0

The MSTAT Counter Rollover Registers provide indication of counter roll over conditions. The register bit remains set until the register is read. Reading this register clears all bits within this register.

Downloaded by Content Team of Partminer Corporation Tuesday, 07 February, 2007 06:09:32 PM

Register 2103H: MSTAT Counter Rollover 2

Bit	Type	Function	Default
Bit 15	R	TransmittedFrames128to 255Octets	0
Bit 14	R	TransmittedFrames65to 127Octets	0
Bit 13	R	TransmittedFrames 64Octets	0
Bit 12	R	MACCTRLFrames Transmitted	0
Bit 11	R	PAUSEMACCTRLFrames Transmitted	0
Bit 10	R	BroadcastFrames TransmittedOK	0
Bit 9	R	BroadcastFrames TranmittedAttempted	0
Bit 8	R	MulticastFrames TransmittedOK	0
Bit 7	R	MulticastFramesTransmittedAttempted	0
Bit 6	R	UnicastFramesTransmittedOK	0
Bit 5	R	UnicastFramesTransmittedAttempted	0
Bit 4	R	TransmitSystemError	0
Bit 3	R	FramesLostDueToInternal MacTransmissionError	0
Bit 2	R	OctetsTransmitted	0
Bit 1	R	OctetsTransmittedOK	0
Bit 0	R	FramesTransmitteOK	0

The MSTAT Counter Rollover Registers provide indication of counter roll over conditions. The register bit remains set until the register is read. Reading this register clears all bits within this register.

Downloaded by Content Team of Partner Electronics, 07 February 2007 06:59:32 PM

Register 2104H: MSTAT Counter Rollover 3

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R	Reserved	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	TaggedFramesTransmitted OK	0
Bit 4	R	JumboOctetsTransmitted OK	0
Bit 3	R	TransmittedFrames1519to MAXOctets	0
Bit 2	R	TransmittedFrames1024to 1518Octets	0
Bit 1	R	TransmittedFrames512to 1023Octets	0
Bit 0	R	TransmittedFrames256to 511Octets	0

The MSTAT Counter Rollover Registers provide indication of counter roll over conditions. The register bit remains set until the register is read. Reading this register clears all bits within this register.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:59:32 PM

Register 2105H:MSTAT Interrupt Mask 0

Bit	Type	Function	Default
Bit 15	R/W	MASK0[15]	0
Bit 14	R/W	MASK0[14]	0
Bit 13	R/W	MASK0[13]	0
Bit 12	R/W	MASK0[12]	0
Bit 11	R/W	MASK0[11]	0
Bit 10	R/W	MASK0[10]	0
Bit 9	R/W	MASK0[9]	0
Bit 8	R/W	MASK0[8]	0
Bit 7	R/W	MASK0[7]	0
Bit 6	R/W	MASK0[6]	0
Bit 5	R/W	MASK0[5]	0
Bit 4	R/W	MASK0[4]	0
Bit 3	R/W	MASK0[3]	0
Bit 2	R/W	MASK0[2]	0
Bit 1	R/W	MASK0[1]	0
Bit 0	R/W	MASK0[0]	0

The MSTAT Interrupt Mask Registers provide programmable interrupt masking of the MSTAT Counter Rollover Register bits.

MASK0[15:0]

The MASK0[15:0] bits are used as a logical mask for each corresponding bit in the **MSTAT Counter Rollover Register 0**. If the MASK bit is high (logic 1), the given counter overflow condition in the **MSTAT Counter Rollover Register 0** will cause the MSTAT to assert the INTB pin, if globally enabled. If the MASK bit is low (logic 0), the corresponding **MSTAT Counter Rollover Register 0** bit state has no effect on the INTB pin.

Downloaded by Content Team of Parts Group Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 2106H:MSTAT Interrupt Mask 1

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R/W	MASK1[14]	0
Bit 13	R/W	MASK1[13]	0
Bit 12	R/W	MASK1[12]	0
Bit 11	R/W	MASK1[11]	0
Bit 10	R/W	MASK1[10]	0
Bit 9	R/W	MASK1[9]	0
Bit 8	R/W	MASK1[8]	0
Bit 7	R/W	MASK1[7]	0
Bit 6	R/W	MASK1[6]	0
Bit 5	R/W	MASK1[5]	0
Bit 4	R/W	MASK1[4]	0
Bit 3	R/W	MASK1[3]	0
Bit 2	R/W	MASK1[2]	0
Bit 1	R/W	MASK1[1]	0
Bit 0	R/W	MASK1[0]	0

The MSTAT Interrupt Mask Registers provide programmable interrupt masking of the MSTAT Counter Rollover Register bits.

MASK1[14:0]

The MASK1[14:0] bits are used as a logical mask for each corresponding bit in the **MSTAT Counter Rollover Register 1**. If the MASK bit is high (logic 1), the given counter overflow condition in the **MSTAT Counter Rollover Register 1** will cause the MSTAT to assert the INTB pin, if globally enabled. If the MASK bit is low (logic 0), the corresponding **MSTAT Counter Rollover Register 1** bit state has no effect on the INTB pin.

Downloaded by Content Team of Parts Group inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 2107H:MSTAT Interrupt Mask 2

Bit	Type	Function	Default
Bit 15	R/W	MASK2[15]	0
Bit 14	R/W	MASK2[14]	0
Bit 13	R/W	MASK2[13]	0
Bit 12	R/W	MASK2[12]	0
Bit 11	R/W	MASK2[11]	0
Bit 10	R/W	MASK2[10]	0
Bit 9	R/W	MASK2[9]	0
Bit 8	R/W	MASK2[8]	0
Bit 7	R/W	MASK2[7]	0
Bit 6	R/W	MASK2[6]	0
Bit 5	R/W	MASK2[5]	0
Bit 4	R/W	MASK2[4]	0
Bit 3	R/W	MASK2[3]	0
Bit 2	R/W	MASK2[2]	0
Bit 1	R/W	MASK2[1]	0
Bit 0	R/W	MASK2[0]	0

The MSTAT Interrupt Mask Registers provide programmable interrupt masking of the MSTAT Counter Rollover Register bits.

MASK2[15:0]

The MASK2[15:0] bits are used as a logical mask for each corresponding bit in the **MSTAT Counter Rollover Register 2**. If the MASK bit is high (logic 1), the given counter overflow condition in the **MSTAT Counter Rollover Register 2** will cause the MSTAT to assert the INTB pin, if globally enabled. If the MASK bit is low (logic 0), the corresponding **MSTAT Counter Rollover Register 2** bit state has no effect on the INTB pin.

Downloaded by Content Team of Parts Group Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 2108H:MSTAT Interrupt Mask 3

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R	Reserved	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R/W	MASK3[5]	0
Bit 4	R/W	MASK3[4]	0
Bit 3	R/W	MASK3[3]	0
Bit 2	R/W	MASK3[2]	0
Bit 1	R/W	MASK3[1]	0
Bit 0	R/W	MASK3[0]	0

The MSTAT Interrupt Mask Registers provide programmable interrupt masking of the MSTAT Counter Rollover Register bits.

MASK3[5:0]

The MASK3[5:0] bits are used as a logical mask for each corresponding bit in the **MSTAT Counter Rollover Register 3**. If the MASK bit is high (logic 1), the given counter overflow condition in the **MSTAT Counter Rollover Register 3** will cause the MSTAT to assert the INTB pin, if globally enabled. If the MASK bit is low (logic 0), the corresponding **MSTAT Counter Rollover Register 3** bit state has no effect on the INTB pin.

Downloaded by Content Team of Parts Group Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 2109H: MSTAT Counter Write Address

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R	Reserved	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R/W	ADDRESS[5]	0
Bit 4	R/W	ADDRESS[4]	0
Bit 3	R/W	ADDRESS[3]	0
Bit 2	R/W	ADDRESS[2]	0
Bit 1	R/W	ADDRESS[1]	0
Bit 0	R/W	ADDRESS[0]	0

The MSTAT Counter Write Address Register provides the write address used during a write operation to the MSTAT counters.

ADDRESS[5:0]

The ADDRESS[5:0] bits are used as the write address during a write operation to the MSTAT counters. A proper counter address must be written to the MSTAT Counter Write Address prior to initiating a write operation via the WRITE bit in the MSTAT Control register. Please refer to Table 29 for the correct counter write address.

Downloaded by Content Team of Partsbase, Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 210AH: MSTAT Counter Write Data Low

Bit	Type	Function	Default
Bit 15:0	R/W	DATA[15:0]	0

Register 210BH: MSTAT Counter Write Data Middle

Bit	Type	Function	Default
Bit 15:0	R/W	DATA[31:16]	0000

Register 210CH: MSTAT Counter Write Data High

Bit	Type	Function	Default
Bit 15:8	R	Reserved	00
Bit 7:0	R/W	DATA[39:32]	00

The MSTAT Counter Write Data Registers provide the write data used during a write operation to the MSTAT counters. The MSTAT Counter Write Data Registers are partitioned into low, middle, and high register entities.

DATA[15:0]

The DATA[15:0] bits are used as the write data during a write operation to the MSTAT counters. The proper counter data must be written to the MSTAT Counter Write Data Register prior to initiating a write operation via the WRITE bit in the MSTAT Control register.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 6:59:32 PM

Register 2110H to 218AH: MSTAT0 Receive Statistical Counters

Bit	Type	Function	Default
Bits 39:0	R/W	COUNT[39:0]	0

The MSTAT Statistical Counters are defined in Table 29. The MSTAT Statistical Counters are 40 bits. The MSTAT Statistical Counters represent the individual counters split between high, middle, and low registers. The low register contains bits 15:0, the middle register contains bits 31:16, and the high register contains bits 39:32 as well as 8 unused or reserved bits in the MSB of the high register. Please see Table 29 for a description of each counter.

COUNT[39:0]

The COUNT[39:0] bits are used as the 40 bit counter.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 12:02:02 PM

Register 2190H to 21E6H: MSTAT0 Transmit Statistical Counters

Bit	Type	Function	Default
Bits 39:0	R/W	COUNT[39:0]	0

The MSTAT Statistical Counters are defined in Table 29. The MSTAT Statistical Counters are 40 bits. The MSTAT Statistical Counters represent the individual counters split between high, middle, and low registers. The low register contains bits 15:0, the middle register contains bits 31:16, and the high register contains bits 39:32 as well as 8 unused or reserved bits in the MSB of the high register. Please see Table 29 for a description of each counter.

COUNT[39:0]

The COUNT[39:0] bits are used as the 40 bit counter.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 @ 09:32 PM

Table 29 MSTAT Counter Description

MSTAT Counter Registers		
Read Address		
2110	Low	**FramesReceivedOK** Contains a count of frames that are successfully received. This does not include frames received that are classified under: FrameCheckSequenceErrors, FramesLostDueToInternalMACError, SymbolError, InRangeLengthErrors, FramesTooLongErrors, Jabbers, Fragments, or UndersizedFrames. MSTAT Counter Write Address = 0x0
2111	Mid	
2112	High	
2114	Low	**OctetsReceivedOK** Contains a count of data and padding octets in frames (not including Preamble, SFD, destination/source address, type/length field, Q-Tag prefix or FCS) that are successfully received. This does not include octets in frames received that are classified under: FrameCheckSequenceErrors, FramesLostDueToInternalMACError, SymbolError, InRangeLengthErrors, FramesTooLongErrors, Jabbers, Fragments, UndersizedFrames. ifInOctets (MIB-II) can be computed using the following: ifInOctets = OctetsReceivedOK + (18 * FramesReceivedOK) ifInOctets includes the count of data, padding, destination/source address, length/type field, Q-Tag prefix, and FCS. (excludes preamble and SFD). MSTAT Counter Write Address = 0x1
2115	Mid	
2116	High	
2118	Low	**FramesReceived** The total number of frames (including bad frames, unicast frames, broadcast frames, and multicast frames) received. This count includes those frames of Jumbo Size. MSTAT Counter Write Address = 0x2
2119	Mid	
211A	High	
211C	Low	**OctetsReceived** The total number of octets of data (including those in bad frames) received (excluding framing bits but including FCS octets). This includes the count of bytes from the first byte of the Destination address to the last byte of the FCS field. MSTAT Counter Write Address = 0x3
211D	Mid	
211E	High	
2120	Low	UnicastFramesReceivedOK Contains a count of frames that are successfully received and are directed to a unicast group address. This does not include octets in frames received that are classified under: FrameCheckSequenceErrors, FramesLostDueToInternalMACError, SymbolError, InRangeLengthErrors, FramesTooLongErrors, Jabbers, Fragments, or UndersizedFrames. MSTAT Counter Write Address = 0x4
2121	Mid	
2122	High	
2124	Low	**MulticastFramesReceivedOK** Contains count of frames that are successfully received and are directed to a
2125	Mid	

Downloaded by Content Team of Parts Group Inc. on Tuesday, February 20, 2018 06:59:32 PM

MSTAT Counter Registers		
2126	High	multicast group address. This counter will not increment for frames classified as unicast or broadcast. This does not include frames received that are classified under: FrameCheckSequenceErrors, FramesLostDueToInternalMACError, SymbolError, InRangeLengthErrors, OutofRangeLengthErrors, FramesTooLongErrors, Jabbers, Fragments, or UndersizedFrames. MSTAT Counter Write Address = 0x5
2128	Low	**BroadcastFramesReceivedOK** Contains a count of frames that are successfully received and are directed to the broadcast group address. This counter will not increment for frames classified as unicast or multicast. This does not include frames received that are classified under: FrameCheckSequenceErrors, FramesLostDueToInternalMACError, SymbolError, InRangeLengthErrors, FramesTooLongErrors, Jabbers, Fragments, or UndersizedFrames. MSTAT Counter Write Address = 0x6
2129	Mid	
212A	High	
212C	Low	**TaggedFramesReceivedOK** Contains a count of tagged frames that are successfully received. This does not include tagged frames received that are classified under: FrameCheckSequenceErrors, FramesLostDueToInternalMACError, SymbolError, InRangeLengthErrors, FramesTooLongErrors, Jabbers, Fragments, or UndersizedFrames. MSTAT Counter Write Address = 0x7
212D	Mid	
212E	High	
2130	Low	**PAUSEMACControlFrameReceived** Contains a count of MAC Control frames passed by the MAC sub-layer to the MAC Control sub-layer. This counter is incremented when a ReceiveFrame function call returns a valid frame with: A lengthOrType field value equal to the reserved Type for 802.3_MAC_Control as specified in 802.3-1998 (31.4.1.3), and An opcode indicating the PAUSE operation. This does not include frames received that are classified under: FrameCheckSequenceErrors, FramesLostDueToInternalMACError, SymbolError, InRangeLengthErrors, FramesTooLongErrors, Jabbers, Fragments, or UndersizedFrames. MSTAT Counter Write Address = 0x8
2131	Mid	
2132	High	
2134	Low	**MACControlFrameReceived** Contains a count of MAC Control frames passed by the MAC sub-layer to the MAC Control sub-layer. This counter is incremented when a ReceiveFrame function call returns a valid frame with: (1) a lengthOrType field value equal to the reserved Type for 802.3_MAC_Control as specified in 802.3-1998 (31.4.1.3). This does not include frames received that are classified under: FrameCheckSequenceErrors, FramesLostDueToInternalMACError, SymbolError, InRangeLengthErrors, FramesTooLongErrors, Jabbers, Fragments, or UndersizedFrames. MSTAT Counter Write Address = 0x9
2135	Mid	
2136	High	
2138	Low	**FrameCheckSequenceErrors** Contains a count of receive frames that are an integral number of octets in
2139	Mid	

Downloaded by Content Team of Partner Only Content at 07 February, 2007 06:59:32

MSTAT Counter Registers		
213A	High	length and do not pass the FCS check. This does not include frames received that are too long(jabbers), or too short (fragments). MSTAT Counter Write Address = 0xA
213C	Low	**FramesLostDueToInternalMACError** Contains a count of frames that would otherwise be received by the device, but could not be accepted due to an internal MAC sub-layer receive error (I.E. FIFO overrun). If this counter is incremented, then none of the other error counters in this section are incremented. MSTAT Counter Write Address = 0xB
213D	Mid	
213E	High	
2140	Low	**SymbolError** A count of the number of times when valid length frame was received at the port and during which time there was at least one occurrence of an event that causes the PHY to indicate “Data reception error” or invalid “Data symbol error.” This counter shall be incremented only once per valid CarrierEvent. MSTAT Counter Write Address = 0xC
2141	Mid	
2142	High	
2144	Low	**InRangeLengthErrors** Contains a count of frames with a length/type field value between 46 and 1500 that does not match the number of MAC client data octets received. The counter also increments for frames whose length/type field value is from 0 to 45 regardless of the number of MAC client data octets received. MSTAT Counter Write Address = 0xD
2145	Mid	
2146	High	
214C	Low	**FramesTooLongErrors** Contains a count of frames received that exceed the maximum permitted frame size and have no other errors. This counter is aware of both tagged and non tagged frames as well as frames of Jumbo size. MSTAT Counter Write Address = 0xF
214D	Mid	
214E	High	
2150	Low	**Jabbers** Contains a count of the total number of frames received that were longer than the maximum permitted frame size and had a bad Frame Check Sequence (FCS). MSTAT Counter Write Address = 0x10
2151	Mid	
2152	High	
2154	Low	**Fragments** The total number of frames received that were less than minimum permitted frame size (64 octets long excluding framing bits, but including FCS octets) and had a bad frame check sequence (FCS). MSTAT Counter Write Address = 0x11
2155	Mid	
2156	High	
2158	Low	**UndersizedFrames** The total number of frames received that were less than the minimum permitted frame size (64 octets long excluding framing bits, but including FCS octets) and were otherwise well formed. MSTAT Counter Write Address = 0x12
2159	Mid	
215A	High	
215C	Low	**ReceiveFrames64Octets** The total number of frames (including bad frames) received that were 64 octets in length (excluding framing bits but including FCS octets). MSTAT Counter Write Address = 0x13
215D	Mid	
215E	High	
2160	Low	**ReceiveFrames65to127Octets** The total number of frames (including bad frames) received that were between
2161	Mid	

Downloaded by Content Team of Parts Group Inc on Wednesday, 7 February 2007 09:09:32 PM

MSTAT Counter Registers		
2162	High	65 and 127 octets in length inclusive (excluding framing bits but including FCS octets). MSTAT Counter Write Address = 0x14
2164	Low	**ReceiveFrames128to255Octets** The total number of frames (including bad frames) received that were between 128 and 255 octets in length inclusive (excluding framing bits but including FCS octets). MSTAT Counter Write Address = 0x15
2165	Mid	
2166	High	
2168	Low	**ReceiveFrames256to511Octets** The total number of frames (including bad frames) received that were between 256 and 511 octets in length inclusive (excluding framing bits but including FCS octets). MSTAT Counter Write Address = 0x16
2169	Mid	
216A	High	
216C	Low	**ReceiveFrames512to1023Octets** The total number of frames (including bad frames) received that were between 512 and 1023 octets in length inclusive (excluding framing bits but including FCS octets). MSTAT Counter Write Address = 0x17
216D	Mid	
216E	High	
2170	Low	**ReceiveFrames1024to1518Octets** The total number of frames (including bad frames) received that were between 1024 and (1518 octets for untagged frames and 1522 octets for VLAN tagged frames) in length inclusive (excluding framing bits but including FCS octets). MSTAT Counter Write Address = 0x18
2171	Mid	
2172	High	
2174	Low	**ReceiveFrames1519toMAXOctets** The total number of frames (including bad frames) received that were between the maximum normal frame lengths (1518 octets for untagged frames and 1522 octets for tagged frames) and maximum Jumbo frame lengths (i.e. 9600 octets) (excluding framing bits but including FCS octets). MSTAT Counter Write Address = 0x19
2175	Mid	
2176	High	
2178	Low	**JumboOctetsReceivedOK** The total number of octets (excluding bad frames) received that were between the maximum normal frame lengths (1518 octets for untagged frames and 1522 octets for tagged frames) and maximum Jumbo frame lengths (i.e. up to MaxFrameSize) (excluding framing bits but including FCS octets). MSTAT Counter Write Address = 0x1A
2179	Mid	
217A	High	
217C	Low	**FilteredOctets** The total number of octets that would normally be passed to the link that are dropped because of filtering rules. MSTAT Counter Write Address = 0x1B
217D	Mid	
217E	High	
2180	Low	**FilteredUnicastFrames** The total number of Unicast classified frames that would normally be passed to the link that are dropped because of filtering rules. MSTAT Counter Write Address = 0x1C
2181	Mid	
2182	High	
2184	Low	**FilteredMulticastFrames** The total number of Multicast frames that would normally be passed to the link that are dropped because of filtering rules. MSTAT Counter Write Address = 0x1D
2185	Mid	
2186	High	

Downloaded by Content Team of Part Miner on Thursday, 01 February 2007 08:39:32 PM

MSTAT Counter Registers		
2188	Low	**FilteredBroadcastFrames** The total number of Broadcast frames that would normally be passed to the link that are dropped because of filtering rules. MSTAT Counter Write Address = 0x1E
2189	Mid	
218A	High	
2190	Low	**FramesTransmittedOK** Contains the count of frames that are successfully transmitted over the MAC interface. MSTAT Counter Write Address = 0x20
2191	Mid	
2192	High	
2194	Low	**OctetsTransmittedOK** Contains a count of data and padding (excluding preamble, SFD, destination/source address, length/type field, Q-Tag prefix, and FCS) octets of frames that are successfully transmitted over the MAC interface. ifOutOctets (MIB-II) can be computed using the following: ifOutOctets = OctetsTransmittedOK + (18 * FramesTransmittedOK) ifOutOctets includes the count of data, padding, destination/source address, length/type field, Q-Tag prefix, and FCS. (excludes preamble and SFD). MSTAT Counter Write Address = 0x21
2195	Mid	
2196	High	
2198	Low	**OctetsTransmitted** Contains a count of data and padding (excluding preamble, SFD, destination/source address, length/type field, Q-Tag prefix, and FCS) octets of frames that are attempted to be transmitted over the MAC interface. MSTAT Counter Write Address = 0x22
2199	Mid	
219A	High	
219C	Low	**FramesLostDueToInternalMACTransmissionError** Contains a count of frames that would otherwise be transmitted by the device, but because of a MAC FIFO underrun could not be sent correctly. If this counter is incremented, then none of the other error counters in this section are incremented. MSTAT Counter Write Address = 0x23
219D	Mid	
219E	High	
21A0	Low	**TransmitSystemError** Contains a count of frames that would otherwise be transmitted by the device, but could not be sent due to an indication from the POS-PHY Level 3 TERR signal being asserted, an oversize frame being transmitted, or an internal CRC error discovered that was generated from the upstream device. If this counter is incremented, then none of the other error counters in this section are incremented. MSTAT Counter Write Address = 0x24
21A1	Mid	
21A2	High	
21A4	Low	**UnicastFramesTransmittedAttempted** Contains a count of frames that are requested to be transmitted to a group unicast destination address. This count includes those frames that were discarded or not sent. MSTAT Counter Write Address = 0x25
21A5	Mid	
21A6	High	
21A8	Low	**UnicastFramesTransmittedOK** Contains a count of frames that are successfully transmitted via the MAC interface to a group unicast destination address. MSTAT Counter Write Address = 0x26
21A9	Mid	
21AA	High	
21AC	Low	**MulticastFramesTransmittedAttempted**

Downloaded by Content Team of Parts-i-e Inc on Monday, February 05, 2007 06:59:32 PM

MSTAT Counter Registers		
21AD	Mid	Contains a count of frames that are requested to be transmitted to a group multicast destination address. This count includes those frames that were discarded or not sent. This count is not updated by broadcast frame transmission. MSTAT Counter Write Address = 0x27
21AE	High	
21B0	Low	**MulticastFramesTransmittedOK** Contains a count of frames that are successfully transmitted to a group multicast destination. This count is not updated by broadcast frame transmission. MSTAT Counter Write Address = 0x28
21B1	Mid	
21B2	High	
21B4	Low	**BroadcastFramesTransmittedAttempted** Contains a count of the frames that were requested to be transmitted to a broadcast address. This count includes those frames that were discarded or not sent. This count is not updated by multicast frame transmission. MSTAT Counter Write Address = 0x29
21B5	Mid	
21B6	High	
21B8	Low	**BroadcastFramesTransmittedOK** Contains a count of the frames that were successfully transmitted to the broadcast address. This count is not updated by multicast frame transmission. MSTAT Counter Write Address = 0x2A
21B9	Mid	
21BA	High	
21BC	Low	**PAUSEMACCTRLFramesTransmitted** Contains a count of PAUSE frames passed to the MAC sub-layer for transmission. This counter is incremented when a request to send the PAUSE control frame is generated. MSTAT Counter Write Address = 0x2B
21BD	Mid	
21BE	High	
21C0	Low	**MACCTRLFramesTransmitted** Contains a count of frames passed to the MAC sub-layer for transmission. This counter is incremented when a control frame is transmitted out of the MAC. MSTAT Counter Write Address = 0x2C
21C1	Mid	
21C2	High	
21C4	Low	**TransmittedFrames64Octets** The total number of frames (including bad frames) transmitted that were 64 octets in length (excluding framing bits but including FCS octets). MSTAT Counter Write Address = 0x2D
21C5	Mid	
21C6	High	
21C8	Low	**TransmittedFrames65to127Octets** The total number of frames (including bad frames) transmitted that were between 65 and 127 octets in length inclusive (excluding framing bits but including FCS octets). MSTAT Counter Write Address = 0x2E
21C9	Mid	
21CA	High	
21CC	Low	**TransmittedFrames128to255Octets** The total number of frames (including bad frames) transmitted that were between 128 and 255 octets in length inclusive (excluding framing bits but including FCS octets). MSTAT Counter Write Address = 0x2F
21CD	Mid	
21CE	High	
21D0	Low	**TransmittedFrames256to511Octets** The total number of frames (including bad frames) transmitted that were
21D1	Mid	

Downloaded by Content Team of Parts Direct on Wednesday, 7 February, 2007 06:59:32 PM

MSTAT Counter Registers		
21D2	High	between 256 and 511 octets in length inclusive (excluding framing bits but including FCS octets). MSTAT Counter Write Address = 0x30
21D4	Low	**TransmittedFrames512to1023Octets** The total number of frames (including bad frames) transmitted that were between 512 and 1023 octets in length inclusive (excluding framing bits but including FCS octets). MSTAT Counter Write Address = 0x31
21D5	Mid	
21D6	High	
21D8	Low	**TransmittedFrames1024to1518Octets** The total number of frames (including bad frames) transmitted that were between 1024 and (1518 octets for untagged frames and 1522 octets for VLAN tagged frames) in length inclusive (excluding framing bits but including FCS octets). MSTAT Counter Write Address = 0x32
21D9	Mid	
21DA	High	
21DC	Low	**TransmittedFrames1519toMAXOctets** The total number of frames (including bad frames) transmitted that were between the normal maximum length (1518 octets for un-tagged frames and 1522 octets for tagged frames) and the max Jumbo frame length (i.e. up to MaxFrameSize) (excluding framing bits but including FCS octets). MSTAT Counter Write Address = 0x33
21DD	Mid	
21DE	High	
21E0	Low	**JumboOctetsTransmittedOK** The total number of octets (excluding bad frames) transmitted that were between the normal maximum length (1518 octets for un-tagged frames and 1522 octets for tagged frames) and the max Jumbo frame length (i.e. up to MaxFrameSize) (excluding framing bits but including FCS octets). MSTAT Counter Write Address = 0x34
21E1	Mid	
21E2	High	
21E4	Low	**TaggedFramesTransmittedOK** Contains a count of Tagged frames that are successfully transmitted. This does not include Tagged frames transmitted that contain errors such as FramesLostDueToInternalMACTransmissionError or TransmitSystemError. MSTAT Counter Write Address = 0x35
21E5	Mid	
21E6	High	

Downloaded by Content Team of Partsim.com Pursuant to Terms and Conditions 2007 09:49:32 PM

12.24 Ingress Flexible FIFO (IFLX)

Register 2200H: IFLX Global Configuration Register

Bit	Type	Function	Default
Bit 15	R/W	IRCU_ENABLE	0
Bit 14	R/W	IDSWT_ENABLE	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

IRCU_ENABLE

The ENABLE bit must be set to enable the operation of the IRCU block. Clearing this bit causes the entire IRCU block to freeze and stop processing requests from either the write data path or the system scheduler.

IDSWT_ENABLE

The ENABLE bit must be set to enable the operation of the IDSWT block. Clearing this bit causes the entire IDSWT block to freeze and stop processing requests from either the write data path or the system scheduler.

This bit should be set high under normal operation. To disable traffic flow to the PL4 interface, either set the IRCU_ENABLE low, or set all the Channel PROV bits low.
To disable selected channels, set the appropriate Channel PROV bit low whilst keeping the IRCU_ENABLE and IDSWT_ENABLE bits high.

Downloaded by Conexant Department on Wednesday, 07 February 2007 06:59:32 PM

Register 2201H: IFLX Channel Provision

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	PROV[3]	0
Bit 2	R/W	PROV[2]	0
Bit 1	R/W	PROV[1]	0
Bit 0	R/W	PROV[0]	0

PROV[3:0]

The channel provision (PROV[3:0]) bits specify the active status of the channels being accessed. When PROV[n] is asserted high, channel[n] is active. When PROV[n] is asserted low, channel[n] is inactive and is not used. The PROV[3:0] bits are used for enabling and disabling available channels within the IFLX, as well as to initialize the data and tag RAM read/write addresses. A transition from channel[n] being active (PROV[n] is logic 1) to inactive (PROV[n] is logic 0) will reset the associated rate adaptation buffer, the frame buffer and freeze the associated logical FIFO. A transition from channel[n] being inactive (PROV[n] is logic 0) to active (PROV[n] is logic 1) will reset the associated logical FIFO read/write pointers to an empty state and begin to process data independent of other provisioned channels.

Reserved

The Reserved bits must be set to default logic states as indicated for proper operation of the S/UNI 9953.

Downloaded by Content Team on Behalf of PMC on Wednesday, 07 February 2007 06:59:32 PM

Register 2202H: IFLX Global Status Register

Bit	Type	Function	Default
Bit 15	R	TPPROC	X
Bit 14	R	SOF_ERR	X
Bit 13	R	EOF_ERR	X
Bit 12	—	Unused	X
Bit 11	R	OVF_ERR	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

TPPROC

If set, indicates that the tag processor is currently processing a command. It is normal for this bit to be read as a ‘1’ from time to time when requests are processed from the system scheduler.

SOF_ERR

When SOF_ERR is asserted, the IFLX has detected two or more start-of-frames without an end-of-frame for one of the active channels. This bit serves as a global error indication for all the logical FIFOs, signaling that the host must read the status from the FIFO SOF Error Indication Register to determine which channel suffered the error. The SOF_ERR status bit is cleared when the offending channel status is read.

EOF_ERR

When EOF_ERR is asserted, the IFLX has detected two or more end-of-frames without a start-of-frame for one of the active channels. This bit serves as a global error indication for all the logical FIFOs, signaling that the host must read the status from the FIFO EOF Error Indication Register to determine which channel suffered the error. The EOF_ERR status bit is cleared when the offending channel status is read.

Downloaded by Content Team @ Container Inc @ Wednesday, 07 February 2007 06:59:32 PM

OVF_ERR

When OVR_ERR is asserted, one of the address register and FIFO flag units detected an overflow (i.e., a write to a FIFO that could not be performed because the FIFO was completely full). This bit serves as a global error indication for all the logical FIFOs, signaling that the host must read the FIFO Overflow Error Indication Register to determine which channel suffered the error. The OVF_ERR status bit is cleared when the offending channel status is read.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 00:00:32 PM

Register 2203H: IFLX SOF Error Enable

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	SOF_ERRE[3]	0
Bit 2	R/W	SOF_ERRE[2]	0
Bit 1	R/W	SOF_ERRE[1]	0
Bit 0	R/W	SOF_ERRE[0]	0

SOF_ERRE[3:0]

Start of frame error enable (SOF_ERRE[3:0]) bits enable the generation of an interrupt due to a SOF error for any of the channels. When SOF_ERRE[n] is set to logic 1, an SOF_ERRI[n] assertion causes an interrupt (INTB) to be generated. When SOF_ERRE[n] is set to logic 0, an SOF_ERRI[n] assertion does not generate an interrupt.

Reserved

The Reserved bits must be set to default logic states as indicated for proper operation of the S/UNI 9953.

Downloaded by Content Team of Partminer on Wednesday, 07 February, 2007 06:59:32 PM

Register 2204H: IFLX SOF Error Interrupt

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R	SOF_ERRI[3]	X
Bit 2	R	SOF_ERRI[2]	X
Bit 1	R	SOF_ERRI[1]	X
Bit 0	R	SOF_ERRI[0]	X

If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, these interrupt status bits are cleared on write with a logic 1. Otherwise, these interrupt status bits are cleared on read as per register bit description.

SOF_ERRI[3:0]

Start of frame error interrupt (SOF_ERRI[3:0]) bits indicate a framing error has occurred with respect to SOF for a particular channel. When SOF_ERRI[n] is read as logic one, an SOF error has occurred on the channel corresponding to channel [n]. When SOF_ERRI[n] is zero, no SOF error has occurred on channel [n]. All SOF_ERRI[3:0] bits are cleared to logic 0 immediately after a read to this register.

Downloaded by Content Team of Pericom Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 2205H: IFLX EOF Error Enable

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	EOF_ERRE[3]	0
Bit 2	R/W	EOF_ERRE[2]	0
Bit 1	R/W	EOF_ERRE[1]	0
Bit 0	R/W	EOF_ERRE[0]	0

EOF_ERRE[3:0]

End of frame error enable (EOF_ERR[3:0]) bits enable the generation of an interrupt due to an EOF error for any of the channels. When EOF_ERRE[n] is set to logic 1, an EOF_ERRI[n] assertion causes an interrupt (INTB) to be generated. When EOF_ERRE[n] is set to logic 0, an EOF_ERRI[n] assertion does not generate an interrupt.

Reserved

The Reserved bits must be set to default logic states as indicated for proper operation of the S/UNI 9953.

Downloaded by Content Team of Partminer on Wednesday, 07 February 2007 06:59:32 PM

Register 2206H: IFLX EOF Error Interrupt

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R	EOF_ERRI[3]	X
Bit 2	R	EOF_ERRI[2]	X
Bit 1	R	EOF_ERRI[1]	X
Bit 0	R	EOF_ERRI[0]	X

If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, these interrupt status bits are cleared on write with a logic 1. Otherwise, these interrupt status bits are cleared on read as per register bit description.

EOF_ERRI[3:0]

End of frame error interrupt (EOF_ERRI[3:0]) bits indicate a framing error has occurred with respect to EOF for a particular channel. When EOF_ERRI[n] is read as logic one, an EOF error has occurred on the channel corresponding to channel [n]. When EOF_ERRI[n] is zero, no EOF error has occurred on channel [n]. All EOF_ERRI[3:0] bits are cleared to logic 0 immediately after a read to this register.

Downloaded by Content Team of Pericom Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 2209H: IFLX Rate Adaptation Buffer Overflow Enable

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	OVFE[3]	0
Bit 2	R/W	OVFE[2]	0
Bit 1	R/W	OVFE[1]	0
Bit 0	R/W	OVFE[0]	0

OVFE[3:0]

Overflow enable (OVFE[3:0]) bits enable the generation of an interrupt due to a rate adaptation buffer overflow for any of the channels. When OVFE[n] is set to logic 1, a OVFI[n] assertion causes an interrupt (INTB) to be generated. When OVFE[n] is set to logic 0, a OVFI[n] assertion does not generate an interrupt.

Reserved

The Reserved bits must be set to default logic states as indicated for proper operation of the S/UNI 9953.

Downloaded by Content Team of Partminer on Wednesday, 07 February 2007 06:59:32 PM

Register 220AH: IFLX Rate Adaptation Buffer Overflow Interrupt

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R	OVFI[3]	X
Bit 2	R	OVFI[2]	X
Bit 1	R	OVFI[1]	X
Bit 0	R	OVFI[0]	X

If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, these interrupt status bits are cleared on write with a logic 1. Otherwise, these interrupt status bits are cleared on read as per register bit description.

OVFI[3:0]

Overflow interrupt (OVFI[3:0]) bits indicate an overflow has occurred on a particular rate adaptation buffer. When OVFI[n] is read as logic one, an overflow occurred on the FIFO corresponding to channel [n]. When OVFI[n] is zero, no overflow has occurred on channel [n]. All OVFI[3:0] bits are cleared to logic 0 immediately after a read to this register.

Downloaded by Content Team of Parts Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 220DH: IFLX Indirect Channel Address

Bit	Type	Function	Default
Bit 15	R	BUSY	0
Bit 14	R/W	RWB	1
Bit 13	—	Unused	0
Bit 12	—	Unused	0
Bit 11	—	Unused	0
Bit 10	—	Unused	0
Bit 9	—	Unused	0
Bit 8	—	Unused	0
Bit 7	—	Unused	0
Bit 6	—	Unused	0
Bit 5	—	Unused	0
Bit 4	—	Unused	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	CHAN[1]	0
Bit 0	R/W	CHAN[0]	0

CHAN[1:0]

The indirect channel number bits (CHAN[1:0]) indicate the channel to be updated or queried in the indirect access.

RWB

The read/write bar (RWB) bit selects between an update operation (write) and a query operation (read). Writing logic 0 to RWB triggers the update operation of the channel specified by CHAN[1:0] with the information in Indirect Registers 220EH through 2211H. Writing a logic 1 to RWB triggers a query of the channel specified by CHAN[1:0] and the information is placed in all of the Indirect Registers.

BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set high when a write to the Indirect Channel Select register triggers an indirect access and will stay high until the access is complete. This register should be polled to determine when data from an indirect read operation is available in all the Indirect Data registers or to determine when a new indirect write operation may commence.

Downloaded by Cortina Team of Partner Inc on Wednesday, 07 February, 2007 06:59:32 PM

Reserved

The Reserved bits must be set to default logic states as indicated for proper operation of the S/UNI 9953.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 220EH: IFLX Indirect Logical FIFO Low Limit & Provision

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	LOLIM[6]	0
Bit 5	R/W	LOLIM[5]	0
Bit 4	R/W	LOLIM[4]	0
Bit 3	R/W	LOLIM[3]	0
Bit 2	R/W	LOLIM[2]	0
Bit 1	R/W	LOLIM[1]	0
Bit 0	R/W	LOLIM[0]	0

LOLIM[6:0]

The lower address boundary (LOLIM[6:0]) specifies the lower address limit in the ring buffer for the logical FIFO defined in the Indirect Channel Address Register. The address value specified is in units of 256 bytes, or 16 128-bit words, and must point to the first byte of the first location in the RAM that belongs to the FIFO. For example, to set up a logical FIFO with 4096 bytes of space lying between locations 256 and 511 128-bit words (inclusive) in the RAM, the LOLIM[6:0] field must be set to 16 decimal.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007, 06:59:32 PM

Register 220FH: IFLX Indirect Logical FIFO High Limit

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	HILIM[6]	0
Bit 5	R/W	HILIM[5]	0
Bit 4	R/W	HILIM[4]	0
Bit 3	R/W	HILIM[3]	0
Bit 2	R/W	HILIM[2]	0
Bit 1	R/W	HILIM[1]	0
Bit 0	R/W	HILIM[0]	0

HILIM[6:0]

The upper address boundary, (HILIM[6:0]) specifies the upper address limit in the ring buffer for the logical FIFO defined in the Indirect Channel Address Register. HILIM[6:0] is specified in units of 256 bytes, or 16 128-bit words, and must point to the first byte *after* the last RAM location for the FIFO. For example, to set up a logical FIFO with 4096 bytes of space lying between locations 256 and 511 128-bit words (inclusive) in the RAM, the HILIM[6:0] field must be set to 32 decimal.

As the physical size of the IFLX RAM is 16,384 bytes, the maximum value of HILIM[6:0] would be 64 decimal. This would typically be for the single channel case.

Downloaded by Content Team of Parmiter on Wednesday, 07 February, 2007, 06:59:32 PM

Register 2210H: IFLX Indirect Full/Almost Full Status & Limit

Bit	Type	Function	Default
Bit 15	R	FULL	X
Bit 14	R	AFULL	X
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	AFTH[10]	0
Bit 9	R/W	AFTH[9]	0
Bit 8	R/W	AFTH[8]	0
Bit 7	R/W	AFTH[7]	0
Bit 6	R/W	AFTH[6]	0
Bit 5	R/W	AFTH[5]	0
Bit 4	R/W	AFTH[4]	0
Bit 3	R/W	AFTH[3]	0
Bit 2	R/W	AFTH[2]	0
Bit 1	R/W	AFTH[1]	0
Bit 0	R/W	AFTH[0]	0

AFTH [10:0]

The almost full threshold field (AFTH[10:0]) is the number of 128-bit words that can be held in the logical FIFO before the AFULL signal is asserted for the specified channel in the Indirect Channel Address Register. The AFULL status is reported to the upstream block. When the number of 128-bit words held in this FIFO (as measured by the word counter) is greater than AFTH[10:0], the AFULL status is asserted. Otherwise, AFULL status is de-asserted. It is recommended that AFTH[10:0] be written only at initialization time.

When used in conjunction with the TXXG for Ethernet modes, a PAUSE frame is triggered when the AFTH[10:0] threshold setting is crossed. It is recommended to set the AFTH[10:0] to at most 16 words (128-bit) less than the maximum logical FIFO size, as determined by the HILIM setting.

AFULL

The almost full status bit (AFULL) is set when the number of words within the logical FIFO is greater than the AFTH[10:0] value. This status information is provided for diagnostic purposes.

FULL

The full status bit (FULL) is set when the logical FIFO is reporting a full status to the upstream block. This status information is provided for diagnostic purposes.

Downloaded by Content Team on Wednesday, 07 February 2007 06:59:32 PM

Register 2211H: IFLX Indirect Empty/Almost Empty Status & Limit

Bit	Type	Function	Default
Bit 15	R	EMPTY	X
Bit 14	R	AEMPTY	X
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	AETH[10]	0
Bit 9	R/W	AETH[9]	0
Bit 8	R/W	AETH[8]	0
Bit 7	R/W	AETH[7]	0
Bit 6	R/W	AETH[6]	0
Bit 5	R/W	AETH[5]	0
Bit 4	R/W	AETH[4]	0
Bit 3	R/W	AETH[3]	0
Bit 2	R/W	AETH[2]	0
Bit 1	R/W	AETH[1]	0
Bit 0	R/W	AETH[0]	0

AETH [10:0]

The almost empty threshold field (AETH[10:0]) is the number of 128-bit words that are held in the logical FIFO before the AEMPTY signal is asserted for the specified channel in the Indirect Channel Address Register. The AEMPTY status is reported to the upstream block. When the number of 128-bit words held in this FIFO (as measured by the word counter) is equal to or less than AETH[10:0], the AEMPTY status is asserted. where n is the indirect channel. Otherwise, the AEMPTY status is de-asserted. It is recommended that AETH[10:0] be written only at initialization time.

AEMPTY

The almost empty status bit (AEMPTY) is set when the number of words within the logical FIFO is less than or equal to the AETH[10:0] value. This status information is provided for diagnostic purposes.

EMPTY

The empty status bit (EMPTY) is set whenever the logical FIFO is completely empty. This flag is provided for diagnostic purposes.

Downloaded by Content Team of Parthus on Wednesday, 07 February 2007 06:59:32 PM

12.25 PL4 Multi-Channel Output Scheduler (PL4MOS)

Register 2240H: PL4MOS Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	RE_INIT	0
Bit 2	R/W	PL4MOS_EN	0
Bit 1	R/W	NO_STATUS	0
Bit 0	R/W	ENABLE_FAIRNESS	1

ENABLE_FAIRNESS

The ENABLE_FAIRNESS bit must be set to enable the fairness controller. In the case of one channel system (TOP_CHAN=0), this bit is neglected and fairness controller is disabled. ENABLE_FAIRNESS bit should be updated before enabling the PL4MOS (PL4MOS_EN).

NO_STATUS

The NO_STATUS bit is set to 1 to indicate that status information is not available. In this case, each logical channel is assigned an infinite credit. When NO_STATUS bit is set to 0, the PL4 status information is available and the PL4MOS may use it to implement the credit based scheduling algorithm. The NO_STATUS mode is completely independent of the fairness scheme. So, fairness may be enabled/disabled in the NO_STATUS mode. NO_STATUS bit should be updated before enabling the PL4MOS (PL4MOS_EN).

Downloaded by Content Dept. of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

PL4MOS_EN

When the PL4MOS_EN bit is set low, the PL4MOS is disabled and no requests are sent to the IFLX (Ingress FIFO) block. When the PL4MOS_EN bit is set high, the PL4MOS operates in normal mode. Changing this bit does not affect the internal status or counters of the PL4MOS. This bit should be set high after the FIFO and upstream (payload processing) blocks have been initialized. If the FIFO or upstream blocks have to be reconfigured during normal operation, the PL4MOS_EN bit should be low and the RE_INIT bit should be held high to clear all the internal counters and previous status. If reconfiguring the IFLX, then it is recommended to disable the IFLX prior to disabling the PL4MOS to avoid data corruption. For diagnostic purposes, this bit should be set low to disable the PL4MOS before reading the internal status registers. This guarantees the consistency of the data read.

RE_INIT

RE_INIT bit is used to clear all the internal status registers. It does not affect the configuration registers. When the RE_INIT bit is set high, all the internal counters and status calendar are reset to 0. When it is set low, the PL4MOS operates in normal mode. This bit is ORed with OUT_DIS status from the PL4IO block. The OUT_DIS status is asserted when the PL4 Interface is not in frequency lock with the input reference (REFCLK) or the PL4 peer.

Downloaded by Content Team of Partminer Inc on Wednesday 01 February 2017 09:32 AM

Register 2241H: PL4MOS Mask

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	CHANNEL_MASK[3]	0
Bit 2	R/W	CHANNEL_MASK[2]	0
Bit 1	R/W	CHANNEL_MASK[1]	0
Bit 0	R/W	CHANNEL_MASK[0]	0

CHANNEL_MASK[3:0]

The CHANNEL_MASK register is used to selectively disable service to logical channels. When CHANNEL_MASK[n] is set to 1, the PL4MOS will not issue service requests for channel n. To re-enable the service for channel n, the bit CHANNEL_MASK[n] should be set to 0. PL4MOS_EN bit should be deasserted before writing to this register.

Reserved

The Reserved bits must be set to default logic states as indicated for proper operation of the S/UNI 9953.

Downloaded by Content Team of Partminer on Wednesday, 07 February 2007 06:59:32 PM

Register 2242H: PL4MOS Fairness Masking

Bit	Type	Function	Default
Bit 15	R/W	Reserved	1
Bit 14	R/W	Reserved	1
Bit 13	R/W	Reserved	1
Bit 12	R/W	Reserved	1
Bit 11	R/W	Reserved	1
Bit 10	R/W	Reserved	1
Bit 9	R/W	Reserved	1
Bit 8	R/W	Reserved	1
Bit 7	R/W	Reserved	1
Bit 6	R/W	Reserved	1
Bit 5	R/W	Reserved	1
Bit 4	R/W	Reserved	1
Bit 3	R/W	FAIR_CHAN[3]	1
Bit 2	R/W	FAIR_CHAN[2]	1
Bit 1	R/W	FAIR_CHAN[1]	1
Bit 0	R/W	FAIR_CHAN[0]	1

FAIR_CHAN[3:0]

The FAIR_CHAN register is used to enable or disable the fairness algorithm for the various logical channels. When FAIR_CHAN[n] is set to 0, the fairness algorithm will not be implemented on channel n and this channel will be allowed to transfer any amount of data. It means that the blocking status of the channel will be masked and the channel will be assigned normal/bonus requests irrespective of its blocking status. When FAIR_CHAN[n] is set to 1, the fairness algorithm is implemented and channel n bandwidth will be limited to avoid slowing down other channels. PL4MOS_EN bit should be deasserted before writing to this register.

Reserved

The Reserved bits must be set to default logic states as indicated for proper operation of the S/UNI 9953.

Downloaded by Content Team of Partsim.com on Wednesday, 07 February 2007 06:59:32 PM

Register 2243H: PL4MOS MaxBurst1 Register

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	MAX_BURST1[11]	0
Bit 10	R/W	MAX_BURST1[10]	0
Bit 9	R/W	MAX_BURST1[9]	0
Bit 8	R/W	MAX_BURST1[8]	0
Bit 7	R/W	MAX_BURST1[7]	0
Bit 6	R/W	MAX_BURST1[6]	0
Bit 5	R/W	MAX_BURST1[5]	0
Bit 4	R/W	MAX_BURST1[4]	0
Bit 3	R/W	MAX_BURST1[3]	1
Bit 2	R/W	MAX_BURST1[2]	0
Bit 1	R	MAX_BURST1[1]	0
Bit 0	R	MAX_BURST1[0]	0

MAX_BURST1

MAX_BURST1 defines the amount of credit, in 128-bit words, granted for a starving channel. This value depends on the system latency and architecture.

The following inequalities should be maintained:

MAX_BURST1 >= MAX_TRANSFER
MAX_BURST1 >= MAX_BURST2

Note: the lower 2 bits are forced to zero in order to constrain MAX_BURST1 to modulo 4 values. The default value is 8 words; i.e. 128 bytes. PL4MOS_EN bit should be deasserted before writing to this register.

Downloaded by Content Team at Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 2244H: PL4MOS MaxBurst2 Register

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	MAX_BURST2[11]	0
Bit 10	R/W	MAX_BURST2[10]	0
Bit 9	R/W	MAX_BURST2[9]	0
Bit 8	R/W	MAX_BURST2[8]	0
Bit 7	R/W	MAX_BURST2[7]	0
Bit 6	R/W	MAX_BURST2[6]	0
Bit 5	R/W	MAX_BURST2[5]	0
Bit 4	R/W	MAX_BURST2[4]	0
Bit 3	R/W	MAX_BURST2[3]	1
Bit 2	R/W	MAX_BURST2[2]	0
Bit 1	R	MAX_BURST2[1]	0
Bit 0	R	MAX_BURST2[0]	0

MAX_BURST2

MAX_BURST2 defines the amount of credit, in 128-bit words, granted for a hungry channel. This value depends on the system latency and architecture. The following inequalities should be maintained:

MAX_BURST2 >= MAX_TRANSFER
MAX_BURST1 >= MAX_BURST2

Note that the lower 2 bits are forced to zero in order to constrain MAX_BURST2 to modulo 4 values. The default value is 8 words; i.e. 128 bytes. PL4MOS_EN bit should be deasserted before writing to this register.

Downloaded by Content Team of Electronics Inc. on Wednesday, 07 February, 2007 06:59:32 PM

Register 2245H: PL4MOS Transfer Size Register

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	MAX_TRANSFER[7]	0
Bit 6	R/W	MAX_TRANSFER[6]	0
Bit 5	R/W	MAX_TRANSFER[5]	0
Bit 4	R/W	MAX_TRANSFER[4]	0
Bit 3	R/W	MAX_TRANSFER[3]	1
Bit 2	R/W	MAX_TRANSFER[2]	0
Bit 1	R	MAX_TRANSFER[1]	0
Bit 0	R	MAX_TRANSFER[0]	0

MAX_TRANSFER

MAX_TRANSFER defines the maximum number of 128-bit words that may be transferred during one service request. This value depends on the system latency and architecture. Note that the lower 2 bits are forced to zero in order to constrain MAX_TRANSFER to modulo 4 values. PL4MOS_EN bit should be deasserted before writing to this register.

Downloaded by Content Team of Partminer on Wednesday, 07 February, 2007 06:59:32 PM

12.26 PL4 Output Data Packer (PL4ODP)

Register 2280H: PL4ODP Configuration

Bit	Type	Function	Default
Bit 15	R/W	REPEAT_T[3]	0
Bit 14	R/W	REPEAT_T[2]	0
Bit 13	R/W	REPEAT_T[1]	0
Bit 12	R/W	REPEAT_T[0]	0
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	R/W	SOP_RULE	1
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R/W	Reserved	0
Bit 1	R/W	EN_PORTS	0
Bit 0	R/W	EN_DFWD	0

EN_DFWD

Enable Data Forward. This bit is used to allow PL4 data words at the input FIFO interface to be forwarded to the output PL4 interface. When '1', all PL4 data words will be forwarded regardless of validity. When '0', the PL4ODP block operates normally and forward only valid PL4 data words. The assertion and deassertion of this signal is not synchronized to a given port state, so modifying this register bit during packet data reception can result in partial packets detected at the input FIFO interface.

EN_PORTS

Enable Port State machine. This bit is used as a simple global qualifier to allow the per-channel Port State to leave the Port INACTIVE state. When '1', the Port State can transition out of Port INACTIVE. When '0', the Port State on a per-channel basis will not transition out of Port INACTIVE. Modifying this register bit during packet data reception will not result in partial packets to be written to the output PL4 interface.

Reserved

The Reserved bit must be set to default logic state as indicated for proper operation of the S/UNI 9953.

Downloaded by Connection of Pacific Inc on Wednesday, 07 February, 2007 06:59:32 PM

SOP_RULE

The value of SOP_RULE determines the minimum number of PL4 Bus cycles between successive Start-Of-Packet control words.

SOP_RULE	Minimum SOP spacing (in terms of PL4 Bus cycles)
0	2
1	8

REPEAT_T[3:0]

REPEAT_T is the PL4 Bus configuration parameter defining how many back-to-back training patterns define a training sequence. The value of this input is actually the number of training patterns plus one. A value of REPEAT_T of 0x0 means that a single 20-cycle (PL4 Bus cycle) training pattern defines a training sequence. A value of 0xF for REPEAT_T implies that the training sequence will be 320-cycles, with the 20-cycle training pattern repeated 16 times consecutively. REPEAT_T corresponds to the quantity α (alpha) used in the description of the training sequence in the PL4 specification.

Downloaded by Content Team of Partminer Inc on Wednesday, 31 October, 2007, 06:59:32 PM

Register 2282H: PL4ODP Interrupt Mask

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	PPE_EOPEOBE	0
Bit 6	R/W	PPE_ERREOPE	0
Bit 5	R/W	DBSIZE8NE	0
Bit 4	R/W	ICHANAE	0
Bit 3	R/W	PPE_MEOPE	0
Bit 2	R/W	PPE_MSOPE	0
Bit 1	R/W	ES_OVRE	0
Bit 0	R/W	OUT_DISE	0

OUT_DISE

The OUT_DISE bit enables the generation of an interrupt due to the OUT_DIS status being asserted by the PL4IO block. The OUT_DIS status is asserted when the PL4 Interface is not in frequency lock with the input reference (REFCLK) or the PL4 peer.

ES_OVRE

The ES_OVRE bit enables the generation of an interrupt due to the occurrence of an overrun condition in the PL4ODP Elastic Store.

PPE_MSOPE

Packet Protocol Error, Missing SOP case, Enable bit. This bit enables the generation of an interrupt due to a Packet Protocol Error of type “Missing SOP.”

PPE_MEOPE

Packet Protocol Error, Missing EOP case, Enable bit. This bit enables the generation of an interrupt due to a Packet Protocol Error of type “Missing EOP.”

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:59:32 PM

ICHANAE

Illegal Channel Address Enable bit. This bit enables the generation of an interrupt due to an Illegal Channel address field being detected in the data stream from the upstream Ingress FIFO block.

DBSIZE8NE

Illegal Size Enable bit. This bit enables the generation of an interrupt due to a size violation detected in the data stream from the upstream Ingress FIFO block (if not End-of-Packet then PL4 Data Burst must be a multiple of 16 bytes).

PPE_ERREOPE

Packet Protocol Error, ERR without EOP, Enable bit. This bit enables the generation of an interrupt due to a packet protocol error where ERR is asserted without EOP being asserted.

PPE_EOPEOBE

Packet Protocol Error, EOP without EOB, Enable bit. This bit enables the generation of an interrupt due to a packet protocol error where EOP is asserted without EOB being asserted.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 AM

Register 2283H: PL4ODP Interrupt

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	PPE_EOPEOBI	X
Bit 6	R	PPE_ERREOPI	X
Bit 5	R	DBSIZE8NI	X
Bit 4	R	ICHANAI	X
Bit 3	R	PPE_MEOPI	X
Bit 2	R	PPE_MSOPI	X
Bit 1	R	ES_OVRI	X
Bit 0	R	OUT_DISI	X

If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, these interrupt status bits are cleared on write with a logic 1. Otherwise, these interrupt status bits are cleared on read.

OUT_DISI

The OUT_DISI bit will be set when the OUT_DIS status is asserted by PL4IO. If OUT_DISE is '1' in the PL4ODP Interrupt Mask register, an interrupt will also be generated (INTB output asserted). The OUT_DIS status is asserted when the PL4 Interface is not in frequency lock with the input reference (REFCLK) or the PL4 peer.

ES_OVRI

The ES_OVRI bit will be set when the PL4ODP Elastic Store overruns. This register bit shall not become set in normal device operation since it is used to indicate that data within the PL4ODP has been discarded. If ES_OVRE is '1' in the PL4ODP Interrupt Mask register, an interrupt will also be generated.

PPE_MSOPI

Packet Protocol Error, Missing SOP case. This bit will be set when a Packet Protocol Error of type "Missing SOP" is detected on data written by the incoming FIFO interface.

Downloaded by Content Team of Parts Life Inc on Wednesday, 07 February, 2007 06:59:32 PM

PPE_MEOPI

Packet Protocol Error, Missing EOP case. This bit will be set when a Packet Protocol Error of type “Missing EOP” is detected on data written by the incoming FIFO interface.

ICHANAI

Illegal Channel Address. This bit will be set when an Illegal Channel Address is detected on data written by the incoming FIFO interface.

DBSIZE8NI

Illegal Size. This bit will be set when an Illegal Size is detected on data written by the incoming FIFO interface: if not End-of-Packet then PL4 Data Burst must be a multiple of 16 bytes.

PPE_ERREOPI

Packet Protocol Error, ERR without EOP. This bit will be set due to a packet protocol error where ERR is asserted without EOP being asserted.

PPE_EOPEOBI

Packet Protocol Error, EOP without EOB. This bit will be set due to a packet protocol error where EOP is asserted without EOB being asserted.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 Febuary, 2007 06:59:32 PM

Register 2284H: PL4ODP Configuration MAX_T Register

Bit	Type	Function	Default
Bit 15	R/W	MAX_T[15]	0
Bit 14	R/W	MAX_T[14]	0
Bit 13	R/W	MAX_T[13]	0
Bit 12	R/W	MAX_T[12]	0
Bit 11	R/W	MAX_T[11]	0
Bit 10	R/W	MAX_T[10]	0
Bit 9	R/W	MAX_T[9]	0
Bit 8	R/W	MAX_T[8]	0
Bit 7	R/W	MAX_T[7]	0
Bit 6	R/W	MAX_T[6]	0
Bit 5	R/W	MAX_T[5]	0
Bit 4	R/W	MAX_T[4]	1
Bit 3	R/W	MAX_T[3]	0
Bit 2	R/W	MAX_T[2]	0
Bit 1	R/W	MAX_T[1]	0
Bit 0	R/W	MAX_T[0]	0

MAX_T[15:0]

MAX_T defines the bounded interval in time over which the PL4 training sequence is to be sent. The time value of MAX_T is given in terms of 16 internal CLK cycles. MAX_T setting of 0x0000 has a special meaning.

A value of 0x0000 for MAX_T will result in disabling the timer associated with the sending of training patterns. When the MAX_T register is set to 0x0000, and the OUT_DIS status in the PL4IO block is set to low, no training patterns will be sent from the PL4ODP. If OUT_DIS status is set to high, the PL4ODP transmits training patterns regardless of the value of MAX_T.

The maximum value in time defined by MAX_T for a PL4 cycle frequency of *f* MHz is: (2**16)*(16 CLK cycles)*(4/*f* MHz per CLK cycle) microseconds.

Default value of 16 in MAX_T for a PL4 cycle frequency of 700 MHz means that a training sequence will occur every (16)*(16 CLK cycles)*(4/700 MHz per CLK cycle) = 1.46 µS

Downloaded by Content Team of Pantronics Inc. on Wednesday, 07 February, 2007 06:59:32 PM

Register 2285H: PL4ODP Elastic Store Limit

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	AE_LIM [3]	1
Bit 6	R/W	AE_LIM [2]	0
Bit 5	R//W	AE_LIM [1]	1
Bit 4	R/W	AE_LIM[0]	0
Bit 3	R/W	AF_LIM [3]	1
Bit 2	R/W	AF_LIM [2]	0
Bit 1	R/W	AF_LIM [1]	1
Bit 0	R/W	AF_LIM[0]	1

AF_LIM[3:0]

Defines an almost-full limit on the Elastic Store. The setting of this register affects the data transfer from the Ingress FIFO block. AF_LIM[3:0] sets an almost full limit on the Elastic Store FIFO in terms of 16 byte data elements, with almost-full being true if the FIFO word count (also in terms of 16 byte data elements) is greater than or equal to the AF_LIM[3:0] value.

AE_LIM[3:0]

Defines an almost-empty limit on the Elastic Store. The setting of this register affects the data transfer from the Ingress FIFO block. AF_LIM[3:0] sets an almost empty limit on the Elastic Store FIFO in terms of 16 byte data elements, with almost-empty being true if the FIFO word count (also in terms of 16 byte data elements) is less than or equal to the AE_LIM[3:0] value.

Notes:

AF_LIM[3:0] must be programmed to be greater or equal in value to AE_LIM[3:0].

Data transfer from the Ingress FIFO block is disabled whenever the Elastic Store FIFO word count is greater than AF_LIM (conditional on having the OUT_DIS status in PL4IO block set low). Data transfer is enabled whenever the Elastic Store FIFO word count is less than or equal to AE_LIM or if OUT_DIS status is set high.

Downloaded by Content Team of Chartminer.co.in on Wednesday, 07 February, 2007 06:59:32 PM

Both watermarks are 4-bit values, even though the FIFO has 24 entries. It is not possible to set the AE_LIM or AF_LIM to greater than 15.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

12.27 PL4 Input and Output Interface (PL4IO)

Register 2300H: PL4IO Lock Detect Status

Bit	Type	Function	Default
Bit 15	R	OUT_ROOLV	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	R	IS_ROOLV	X
Bit 11	R	DIP2_ERRV	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	R	ID_ROOLV	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R	IS_DOOLV	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R	ID_DOOLV	X

The current Reference Out Of Lock (ROOL) and Data Out Of Lock (DOOL) conditions.

ID_DOOLV

Depending on the setting of the DLSEL bit in the PL4IO Configuration register, either the input data FIFOs are not aligned to the incoming PL4 transmit data stream (in normal operation) or a valid PRBS pattern is not being received in the input data FIFOs (in serial data link testing).
IS_DOOLV

The PL4 receive status input stream (RSTAT) is not properly synchronized.

ID_ROOLV

The incoming PL4 transmit data clock (TDCLK) or one or more of the PL4 transmit data streams (TDAT[15:0]) are not trained to the local synthesized clock. The PL4 transmit data interface is normally disabled when ID_ROOLV is asserted.

DIP2_ERRV

A DIP2 error occurred on the FIFO status input stream.

Downloaded by Comset Team of Partner Inc on Wednesday, 07 February, 2007 06:59:32 PM

IS_ROOLV

The PL4 receive status clock (RSCLK) frequency exceeds ¼ the frequency of RDCLK. The PL4 receive status interface is normally disabled when IS_ROOLV is asserted.

OUT_ROOLV

The local synthesized clock is not trained to the reference frequency. The PL4 data and status output interfaces (RCTL/RDAT and TSTAT respectively) are normally disabled when OUT_ROOLV is asserted.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 2301H: PL4IO Lock Detect Change

Bit	Type	Function	Default
Bit 15	R	OUT_ROOLI	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	R	IS_ROOLI	X
Bit 11	R	DIP2_ERRI	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	R	ID_ROOLI	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R	IS_DOOLI	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R	ID_DOOLI	X

Indicates whether any of the Reference Out Of Lock (ROOL) or Data Out Of Lock (DOOL) conditions have changed since the previous read from the Lock Detect Change register. An interrupt will be asserted when any pair of corresponding bits in the Lock Detect Change and Lock Detect Mask registers are both set to logic "1". If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, these interrupt status bits are cleared on write with a logic 1. Otherwise, these interrupt status bits are cleared on read.

ID_DOOLI

The Input Data Out Of Lock condition has changed.

ID_DOOLI is set to logic "1" when the value of the ID_DOOLV condition changes.

IS_DOOLI

The Input Status Out Of Lock condition has changed.

IS_DOOLI is set to logic "1" when the value of the IS_DOOLV condition changes.

ID_ROOLI

The Input Data Reference Out Of Lock condition has changed.

ID_ROOLI is set to logic "1" when the value of the ID_ROOLV condition changes.

Downloaded by Content Team of Datasheet Directory, Wednesday, 07 February, 2007, 06:59:32 PM

DIP2_ERRI

The DIP2_ERRV status condition has changed.

DIP2_ERRI is set to logic "1" when the value of the DIP2_ERRV condition changes.

IS_ROOLI

The Input Status Reference Out Of Lock condition has changed.

IS_ROOLI is set to logic "1" when the value of the IS_ROOLV condition changes.

OUT_ROOLI

The Output Reference Out Of Lock condition has changed.

OUT_ROOLI is set to logic "1" when the value of the OUT_ROOLV condition changes.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 2302H: PL4IO Lock Detect Mask

Bit	Type	Function	Default
Bit 15	R/W	OUT_ROOLE	0
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	R/W	IS_ROOLE	0
Bit 11	R/W	DIP2_ERRE	0
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	R/W	ID_ROOLE	0
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R/W	IS_DOOLE	0
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R/W	ID_DOOLE	0

Arms the PL4IO interrupt when any pair of corresponding bits in the Lock Detect Change and Lock Detect Mask registers are both set to logic "1".

ID_DOOLE

Enables the assertion of interrupt. Interrupt is asserted when the ID_DOOLI bit in the Lock Detect Change register and the ID_DOOLE bit are both set to logic "1".

IS_DOOLE

Enables the assertion of interrupt. Interrupt is asserted when the IS_DOOLI bit in the Lock Detect Change register and the IS_DOOLE bit are both set to logic "1".

ID_ROOLE

Enables the assertion of interrupt. Interrupt is asserted when the ID_ROOLI bit in the Lock Detect Change register and the ID_ROOLE bit are both set to logic "1".

DIP2_ERRE

Enables the assertion of interrupt. Interrupt is asserted when the DIP2_ERRI bit in the Lock Detect Change register and the DIP2_ERRE bit are both set to logic "1".

Downloaded by ContentTeam of Hartmine Inc on Wednesday, 07 February, 2007 06:59:32 PM

IS_ROOLE

Enables the assertion of interrupt. Interrupt is asserted when the IS_ROOLI bit in the Lock Detect Change register and the IS_ROOLE bit are both set to logic "1".

OUT_ROOLE

Enables the assertion of interrupt. Interrupt is asserted when the OUT_ROOLI bit in the Lock Detect Change register and the OUT_ROOLE bit are both set to logic "1".

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 2303H: PL4IO Lock Detect Limits

Bit	Type	Function	Default
Bit 15	R/W	REF_LIMIT[7]	0
Bit 14	R/W	REF_LIMIT[6]	0
Bit 13	R/W	REF_LIMIT[5]	0
Bit 12	R/W	REF_LIMIT[4]	0
Bit 11	R/W	REF_LIMIT[3]	0
Bit 10	R/W	REF_LIMIT[2]	0
Bit 9	R/W	REF_LIMIT[1]	0
Bit 8	R/W	REF_LIMIT[0]	1
Bit 7	R/W	TRAN_LIMIT[7]	0
Bit 6	R/W	TRAN _LIMIT[6]	0
Bit 5	R/W	TRAN _LIMIT[5]	1
Bit 4	R/W	TRAN _LIMIT[4]	1
Bit 3	R/W	TRAN _LIMIT[3]	1
Bit 2	R/W	TRAN _LIMIT[2]	1
Bit 1	R/W	TRAN _LIMIT[1]	1
Bit 0	R/W	TRAN _LIMIT[0]	1

This register is for diagnostic purposes only, and would not normally be programmed from the defaults.

Specifies the permitted range of measured clock frequency deviation, relative to the selected reference clock.

REF_LIMIT[7:0]

The maximum permitted deviation for any clock derived from the reference clock, in multiples of 30 ppm (nominal - 30.773 ppm actual).

REF_LIMIT always applies to the CSU and to the PL4 transmit data clock (TDCLK).

REF_LIMIT is set to logic "0000_0001" (30 ppm nominal) when digital core reset is asserted. This value may need to be increased to “0000_0100” when operating in master mode with a peer PL4 interface whose clock system does not propagate low frequency jitter from RDCLK to TDCLK.

Downloaded by Content Mgmt of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

TRAN_LIMIT[7:0]

The minimum number of input data transition events (in multiples of 16) required to synchronize the DRU to the incoming data stream.

TRAN_LIMIT applies to the DRUs.

TRAN_LIMIT is set to logic "0011_1111" (1024 transitions) when digital core reset is asserted.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 6:59:32 PM

Register 2304H: PL4IO Calendar Repetitions

Bit	Type	Function	Default
Bit 15	R/W	IN_MUL[7]	0
Bit 14	R/W	IN_MUL[6]	0
Bit 13	R/W	IN_MUL[5]	0
Bit 12	R/W	IN_MUL[4]	0
Bit 11	R/W	IN_MUL[3]	0
Bit 10	R/W	IN_MUL[2]	0
Bit 9	R/W	IN_MUL[1]	0
Bit 8	R/W	IN_MUL[0]	0
Bit 7	R/W	OUT_MUL[7]	0
Bit 6	R/W	OUT_MUL[6]	0
Bit 5	R/W	OUT_MUL[5]	0
Bit 4	R/W	OUT_MUL[4]	0
Bit 3	R/W	OUT_MUL[3]	0
Bit 2	R/W	OUT_MUL[2]	0
Bit 1	R/W	OUT_MUL[1]	0
Bit 0	R/W	OUT_MUL[0]	0

Specifies the number of repetitions in the PL4 interface FIFO status calendars.

IN_MUL[7:0]

The number of repetitions of the input FIFO status (RSTAT) channels within a complete status calendar sequence. The PL4 input status parameter CALENDAR_M = IN_MUL + 1. The total length of the input status calendar sequence = CALENDAR_LEN x CALENDAR_M.

IN_MUL should only be changed while the input status interface (RSTAT) is disabled in the PL4IO Configuration register. The result of changing IN_MUL while the status interface is enabled is unspecified.

OUT_MUL[7:0]

The number of repetitions of the output FIFO status (TSTAT) channels within a complete status calendar sequence. The PL4 output status parameter CALENDAR_M = OUT_MUL + 1. The total length of the output status calendar sequence = CALENDAR_LEN x CALENDAR_M.

OUT_MUL should only be changed while the output status interface (TSTAT) is disabled in the PL4IO Configuration register. The result of changing OUT_MUL while the status interface is enabled is unspecified.

Downloaded by Content Team of Examiner 01 on Wednesday, 07 February, 2007 06:59:32 PM

Register 2305H: PL4IO Configuration

Bit	Type	Function	Default
Bit 15	R/W	DIP2_ERR_CHK	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	ENABLE	1
Bit 11	R/W	ODAT_DIS	X
Bit 10	R/W	TRAIN_DIS	X
Bit 9	R/W	OSTAT_DIS	1
Bit 8	R/W	ISTAT_DIS	1
Bit 7	R/W	NO_ISTAT	0
Bit 6	R/W	STAT_OUTSEL	0
Bit 5	R/W	INSEL	0
Bit 4	R/W	DLSEL	0
Bit 3	R/W	INV_RSCLK	0
Bit 2	R/W	INV_TSCLK	0
Bit 1	R/W	OUTSEL[1]	0
Bit 0	R/W	OUTSEL[0]	1

Specifies the requested configuration of the PL4IO interface. In normal operation the PL4IO control logic will sequence the internal PL4IO components toward this configuration.

OUTSEL[1:0]

Selects the source of the receive data stream for the PISOs.

00	None
01	Packer output data stream (normal operation)
10	PRBS generate data stream – used for PL4 data link testing
11	FIFO read data stream – enables PL4-side (remote) loop back.

OUTSEL = “11” implies data is looped-back from the device TCTL and TDAT[15:0] input pins to the RCTL and RDAT[15:0] output pins.

OUTSEL is set to logic "01" when digital core reset is asserted.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:09:32 PM

INV_TSCLK

When this bit is set to 1, the output status clock TSCLK is inverted before being output. This results in non-PL4 compliant timing of the output status bus, but it may allow for an easier board design due to the non-symettric PL4 specification of this interface. When INV_TSCLK is set to default value 0, the output status bus operates according to the PL4 timing specification.

INV_RSCLK

When this bit is set to 1, the input status clock RSCLK is inverted before being used for sampling the RSTAT[1:0] inputs. This requires non-PL4 compliant timing of the input status bus, but it may allow for an easier board design due to the non-symettric PL4 specification of this interface. When INV_RSCLK is set to default value 0, the input status bus must meet the PL4 timing specification for correct operation.

DLSEL

Selects the source for the Input Data Out Of Lock (ID_DOOL) condition.

0 – The input data FIFOs are not aligned to the transmit data stream

– used for normal parallel data link operation

1 – A valid PRBS pattern is not being received in the input data FIFOs
– used for serial data link testing

INSEL

Selects the source of the data stream for the Unpacker together with related handshake signals.

0 – DRU input data stream
1 – Packer output data stream
– enables device-side (local) loopback

If PL4IO INSEL is logic 1 (remote loopback from PL4ODP to PL4IDU) and PL4IO OUTSEL[1:0] is b01 (normal operation) data will be impressed on the PL4 RDAT[15:0], RCTL pins. If the user would like to disable the transfer of data on the PL4 RDAT[15:0],RCTL interface pins then the following can be done:

STEP_1: program PL4IO OUTSEL[1:0] to b00. This will result in the RDAT[15:0],RCTL pins being driven to a logic 0.

STEP_2: PL4IO INSEL can be programmed to logic 1 to configure the PL4 interface for remote loopback.

Downloaded by Conta Team of Partminer Inc on Wednesday, 07 February 2007 06:58:02 PM

NOTE:

When INSEL is set to 1 the PL4 interface must be in Master mode and have a valid reference clock for the loopback operation to work properly. The PL4IO lock status logic continues to check the lock status on the device's PL4 interface pins. This will not effect the remote loopback operation even if the PL4IO reports IS/ID ROOL/DOOL out-of-lock, it means the PL4 partner is not configured or present.

STAT_OUTSEL

Selects the source of the output status impressed on the device TSTAT[1:0] output pins.

0 – PL4IO output status state machine (normal operation)
1 – RSTAT input pins (PL4 local loopback operation)

STAT_OUTSEL is set to logic 0 when digital core reset is asserted.

NO_ISTAT

When NO_ISTAT is cleared to logic "0" the input FIFO status (RSTAT) channel operates normally. When NO_ISTAT is set to logic "1" the input FIFO status channel is disabled and the RSTAT pins are ignored. The PL4 receive data path (RCTL/RDAT) can operate normally while NO_ISTAT is set to logic "1" and ISTAT_DIS is cleared to logic "0".

This bit should not be set until the PL4 receive data path has been configured for normal operation.

ISTAT_DIS

When ISTAT_DIS is cleared to logic "0" the input FIFO status (RSTAT) channel operates normally. When ISTAT_DIS is set to logic "1" the input FIFO status channel is disabled and the RSTAT pins are ignored. Neither the PL4 receive data path (RCTL/RDAT) nor the PL4 receive status path (RSTAT) will operate normally while ISTAT_DIS is set to logic "1".

ISTAT_DIS is set to logic "1" when digital core reset is asserted. This bit should not be cleared until the PL4 receive data path (RCTL/RDAT) and status path (RSTAT) have been configured for normal operation. This bit should not be cleared in slave mode until the PL4 Transmit Data Clock (TDCLK) is valid.

Downloaded by Content Portal of Gartner Inc on Wednesday, 07 February, 2007 06:58:32 PM

OSTAT_DIS

When OSTAT_DIS is cleared to logic "0" the output FIFO status channel operates normally. When OSTAT_DIS is set to logic "1" the output FIFO status channel is disabled and the PL4 TSTAT[1:0] pins are driven high. The input data path (device pins TDAT[15:0], TCTL and RSTAT[1:0]) can operate normally while OSTAT_DIS is set to logic "1".

OSTAT_DIS is set to logic "1" when digital core reset is asserted. This bit should not be cleared until the input data path and output status path have been configured for normal operation. This bit should not be cleared in slave mode until the PL4 Transmit Data Clock (TDCLK) is valid.

TRAIN_DIS

When TRAIN_DIS is cleared to logic "0" the PL4 transmit data (TCTL/TDAT) deskew function operates normally. When TRAIN_DIS is set to logic "1" the transmit data deskew function is disabled and the PL4 training pattern is ignored. Neither the transmit data path nor the transmit status (TSTAT) path will operate normally while TRAIN_DIS is set to logic "1".

TRAIN_DIS is cleared to logic "0" when digital core reset is asserted while REFSEL[0] is high (master mode). TRAIN_DIS is loaded from REFSEL[1] when digital core reset is asserted while REFSEL[0] is low (slave mode). This bit should not be cleared in slave mode until the PL4 Transmit Data Clock (TDCLK) is valid.

ODAT_DIS

When ODAT_DIS is cleared to logic "0" the receive data bus (RCTL/RDAT) operates normally. When ODAT_DIS is set to logic "1" the receive data bus is disabled and the PL4 RCTL / RDAT pins are driven low. The receive status (RSTAT) path can operate normally while ODAT_DIS is set to logic "1".

ODAT_DIS is cleared to logic "0" when digital core reset is asserted while REFSEL[0] is high (master mode). ODAT_DIS is loaded from REFSEL[1] when digital core reset is asserted while REFSEL[0] is low (slave mode). This bit should not be cleared in slave mode until the PL4 Transmit Data Clock (TDCLK) is valid.

ENABLE

When ENABLE is set to logic "1" normal operation of the PL4IO is enabled. When ENABLE is cleared to logic "0" the PL4IO is disabled and all PL4 interface analog blocks (ABCs) also are disabled to minimize power consumption.

ENABLE is set to logic "1" when digital core reset is asserted.

Downloaded by Content Team Chartwell Yorke on Wednesday, 06 February, 2013 6:39:32 PM

DIP2_ERR_CHK

When DIP2_ERR_CHK is set to logic ‘1’ the receive status state machine will go out of lock when an error occurs in consecutive frames. An error is defined as a dip2 error, a ‘11’ channel status, or missing an expected sync pattern. After one error is detected, the state machine will return to the HOLD state after two end of calendar are found without another error.

When DIP2_ERR_CHK is set to logic ‘0’ the receive status state machine will return to the HOLD state when an error occurs in consecutive frames. Thus the state machine will not lose lock in the case of constant invalid DIP2 fields.

It is recommended to set this bit high for improved error robustnous.

Reserved

The Reserved bits must be set to default logic states as indicated for proper operation of the S/UNI 9953.

Downloaded by Content Team of Partminer Inc on Wednesday, 01 February, 2017 06:53:32 PM

Register 2307H: PL4IO Reference Mode

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R	Reserved	X
Bit 12	R/W	Reserved	1
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R/W	Reserved	1
Bit 1	R	REFSEL[1]	X
Bit 0	R	REFSEL[0]	X

Specifies the requested configuration of the PL4IO interface. In normal operation the PL4IO control logic will sequence the internal PL4IO components toward this configuration.

REFSEL[1:0]

Read-only status of the corresponding REFSEL[1:0] pins setting.

Reserved

The Reserved bits must be set to default logic states as indicated for proper operation of the S/UNI 9953.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

12.28 APS Analog Wrapper (CSTR)

Register 2380H: CSTR Control

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	1
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	CSU_ENB	0
Bit 3	R/W	Reserved	1
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R/W	Reserved	1

Except for the CSU_ENB register bit, the other register bits are used for manufacturing test purposes only. They are not required for normal operations.

Reserved

The Reserved bits should be set to their default values for normal operation.

CSU_ENB

The CSU enable control signal (CSU_ENB) bit forces the CSU into low power configuration. The CSU is disabled when CSU_ENB is logic 1. The CSU is enabled when CSU_ENB is logic 0. This bit must be set to logic 0 for normal operation.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:39:32 PM

Register 2381H: CSTR Interrupt Enable and CSU Lock Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 1	—	Unused	X
Bit 1	R	CSU_LOCKV	X
Bit 0	R/W	CSU_LOCKE	0

CSU_LOCKE

The CSU lock interrupt enable bit (CSU_LOCKE) enables the assertion of a hardware interrupt on INTB when the CSU lock status changes. When CSU_LOCKE is logic 1, the hardware interrupt is enabled. When CSU_LOCKE is logic 0, the hardware interrupt is disabled.

CSU_LOCKV

The CSU lock status (CSU_LOCKV) indicates the current state of the CSU. When CSU_LOCKV is logic 1, the CSU has locked on to the IAPSFPCLK reference and is operating normally. When CSU_LOCKV is logic 0, the CSU has not locked onto the IAPSFPCLK reference and is not in normal operating mode.

Downloaded by Content Team of Datminer Inc. on Wednesday, 07 February, 2007 06:59:32 PM

Register 2382H: CSTR CSU Lock Interrupt Indication

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 1	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R	CSU_LOCKI	X

If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, these interrupt status bits are cleared on write with a logic 1. Otherwise, these interrupt status bits are cleared on read as per register bit description.

CSU_LOCKI

The CSU lock interrupt indication bit (CSU_LOCKI) reports changes in the CSU lock status. CSU_LOCKI is logic 1 when the CSU transitions to or out of lock state. CSU_LOCKI is cleared when this register is read.

Downloaded by Content Team of Partsbase Inc on Wednesday, 07 February, 2007 06:59:32 PM

12.29 Ingress FIFO RAM (IRAM)

Register 2400H: IRAM Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R	TAG_PERRI	X
Bit 3	R	DATA_PERRI[3]	X
Bit 2	R	DATA_PERRI[2]	X
Bit 1	R	DATA_PERRI[1]	X
Bit 0	R	DATA_PERRI[0]	X

This register and its corresponding interrupt enable register, may be used to optionally identify any parity errors that have occurred within the FIFO RAM. This feature would normally be used for diagnostic purposes. If using this feature, the interrupts should only be enabled after data has first been flushed through the FIFO, otherwise false parity interrupts will be generated due to the uninitialized RAM.

If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, these interrupt status bits are cleared on write with a logic 1. Otherwise, these interrupt status bits are cleared on read as per register bit description.

DATA_PERRI[3:0]

The Data Parity Error Interrupt indicates a parity error occurred during a data RAM read. The bit asserted indicates which part of the data word contained the parity error:

Bit	Bit Range
Bit 3	127:96
Bit 2	95:64
Bit 1	63:32
Bit 0	31:0

Downloaded by Company Item of Partner Site (Wednesday, 07 February, 2007 06:59:32 PM

TAG_PERRI

The Tag Parity Error Interrupt indicates a parity error occurred during a tag RAM read.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 2401H: IRAM Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R/W	TAG_PERRE	0
Bit 3	R/W	DATA_PERRE[3]	0
Bit 2	R/W	DATA_PERRE[2]	0
Bit 1	R/W	DATA_PERRE[1]	0
Bit 0	R/W	DATA_PERRE[0]	0

DATA_PERRE[3:0]

The Data Parity Error Interrupt Enable is set to enable the assertion of the interrupt when the corresponding DATA_PERRI bit is asserted.

TAG_PERRE

The Tag Parity Error Interrupt Enable is set to enable the assertion of the interrupt when the TAG_PERRI bit is asserted.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

12.30 Transmit Cell Frame Processor (OC-192) (TCFP-9953)

Register 3020H: TCFP-9953 General Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	EHDR_LEN[5]	0
Bit 13	R/W	EHDR_LEN[4]	0
Bit 12	R/W	EHDR_LEN[3]	0
Bit 11	R/W	EHDR_LEN[2]	0
Bit 10	R/W	EHDR_LEN[1]	0
Bit 9	R/W	EHDR_LEN[0]	0
Bit 8	R/W	MODE[1]	0
Bit 7	R/W	MODE[0]	0
Bit 6	R/W	CORE_DC	0
Bit 5	R/W	FLAG_IDLE[3]	0
Bit 4	R/W	FLAG_IDLE[2]	0
Bit 3	R/W	FLAG_IDLE[1]	0
Bit 2	R/W	FLAG_IDLE[0]	0
Bit 1	R/W	SCRAMBLE	1
Bit 0	R/W	PROV	0

PROV

The processor provision bit (PROV) is used to enable the TCFP_9953. When PROV is logic 0, the TCFP-9953 ATM, POS (including DELINDIS) and GFP processors are disabled and will not request data from the FIFO interface and will respond to data requests with invalid data. When PROV is logic 1, the TCFP-9953 ATM/POS/GFP processor is enabled and will respond to data requests with valid data after requesting and processing data from the FIFO interface.

SCRAMBLE

The SCRAMBLE bit controls the scrambling of the ATM cell payload, POS and DELINDIS data streams or GFP frame payload area including FCS. When SCRAMBLE is a logic 1, scrambling is enabled. When SCRAMBLE is a logic 0, all scrambling is disabled. This bit is valid in all modes.

FLAG_IDLE[3:0]

The flag/idle-frame insertion control (FLAG_IDLE[3:0]) configures the minimum number of: flag bytes inserted between packets in POS mode, and idle frames inserted between frames in GFP mode. FLAG_IDLE[3:0] is only used when in either POS or GFP mode. Table 30 shows the FLAG_IDLE[3:0] decoding.

Downloaded by Content Team of Parts Search on Wednesday, 07 February, 2007 06:59:32 PM

Table 30 FLAG_IDLE[3:0] Decoding

FLAG_IDLE[3:0]	Min Number	
	POS Flag-bytes	GFP Idle-frames
0000	1	0
0001	2	1
0010	4	2
0011	8	4
0100	16	8
0101	32	16
0110	64	32
0111	128	64
1000	256	128
1001	512	256
1010	1024	512
1011	2048	1024
1100	4096	0
1101	8192	0
1110	16384	0
1111	32768	0

CORE_DC

The GFP Core Header DC Balance (CORE_DC) bit controls whether the transmitted GFP Core Header is DC balanced. When CORE_DC is set to logic one, the GFP Core Header (prior to scrambling) is logically XORed with the value 0xB6AB31E0. When CORE_DC is set to logic zero the Core Header field is unmodified.

MODE[1:0]

The mode select (MODE[1:0]) bits control the operational mode of the TCFP_9953.

Table 31 Operational Mode

MODE[1:0]	Operational Mode
00	DELINDIS
01	ATM
10	POS
11	GFP

Downloaded by Content Team of Hartmine on Wednesday, 07 February, 2007 06:59:32 PM

DELINDIS (POS Delineation Disable) mode enables the carriage of unmodified POS data.

ATM mode enables the processing of an ATM cell stream.

POS mode enables the processing of a POS packet stream.

GFP mode enables the processing of a GFP frame stream.

EHDR_LEN[5:0]

When the TCFP-9953 is in GFP mode, the Extended Header Length (EHDR_LEN[5:0]) bits specify the length of the GFP frame extended header. Valid values are in the range 0 to 60. An eHEC is not inserted for values less than three.Reserved

The Reserved bits must be set to the default value as shown for proper operation of the S/UNI 9953.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 06:59:32 PM

Register 3021H: TCFP-9953 CRC Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	1
Bit 6	R/W	Reserved	1
Bit 5	R/W	CHEC	1
Bit 4	R/W	THEC	1
Bit 3	R/W	EHEC	1
Bit 2	R/W	SHEC	1
Bit 1	R/W	FCS	1
Bit 0	R/W	COSET	1

COSET

The COSET bit determines whether the ATM coset polynomial is applied to the HEC field. When set to a logic one, the coset polynomial is applied to the HEC. When set to logic zero, the HEC is untouched. This bit is only valid in ATM mode.

FCS

The FCS bit determines whether the FCS field is calculated and inserted/overwritten. When set to logic one, the FCS is calculated and inserted in POS mode, and calculated and overwritten in GFP mode. When set to logic zero, no FCS calculation or insertion is performed in POS mode, and no FCS calculation or overwriting is performed in GFP mode. This bit is only valid in POS and GFP modes.

Reserved

The Reserved bits must be set to the default value as shown for proper operation of the S/UNI 9953.

SHEC

The SHEC bit determines whether the Special GFP Control Message HEC is calculated. When set to logic one, the sHEC field is calculated and written into the GFP frame. When set to logic zero the existing sHEC field is untouched. This bit is only valid in GFP mode.

Downloaded by Content Team at Container Int'l on Wednesday, 07 February, 2007 06:59:32 PM

EHEC

The EHEC bit determines whether the GFP Extended Header HEC is calculated. When set to logic one, the eHEC field is calculated and written into the GFP frame. When set to logic zero the existing eHEC field is untouched. This bit is only valid in GFP mode.

THEC

The THEC bit determines whether the GFP Type Header HEC is calculated. When set to logic one, the tHEC field is calculated and written into the GFP frame. When set to logic zero the existing tHEC field is untouched. This bit is only valid in GFP mode.

CHEC

The CHEC bit determines whether the Core Header HEC is calculated. When set to logic one, the cHEC field is calculated and written into the GFP frame. When set to logic zero the existing cHEC field is untouched. This bit is only valid in GFP mode.

Downloaded by Content Team of Partminer Inc on Wednesday, 08 February, 2017 06:59:32 AM

Register 3022H: TCFP-9953 Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	FIFO_ERRI	X
Bit 14	R	FIFO_UDRI	X
Bit 13	R	XFERI	X
Bit 12	R	LEN_ERRI	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

Note that all of the TCFP-9953 interrupts are set to logic one when an event occurs.

If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, these interrupt status bits are cleared on write with a logic 1. Otherwise, these interrupt status bits are cleared on read.

LEN_ERRI

The LEN_ERRI bit is set high when a mode specific length error occurs. In ATM mode, the interrupt is asserted when a cell length other than 52 bytes is detected. In POS mode no length checking is performed. In GFP mode, the interrupt is not used.

XFERI

The XFERI bit indicates that a transfer of accumulated counter data has occurred. A logic 1 in this bit position indicates that the transmitted cell/packet/frame counter, transmitted byte counter, and aborted packet counter holding registers have been updated. This update is initiated by writing to one of the counter register locations, or by a microprocessor write to the S/UNI 9953 Identity and Global Performance Monitor Update register (0000H).

FIFO_UDRI

The FIFO_UDRI (FIFO Under-run Interrupt) bit is set high when the FIFO Interface under-runs. This would be caused by transmission from EFLX stopping in the middle of a cell/packet/frame. This is considered a system error.

Downloaded by Cost to Cost of Polytrainer Inc. on Wednesday, 07 February, 2007 06:59:32 PM

FIFO_ERRI

This bit is set high when a FIFO Interface error is detected. Four failure modes are detected:

FIFO_ERR[15:0] not all-zero (POS mode only).

Breakdown in alternating SOP-EOP sequence.

Valid byte(s) between EOP and SOP.

FIFO Interface buffer overrun.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 3023H: TCFP-9953 Interrupt Enable

Bit	Type	Function	Default
Bit 15	R/W	FIFO_ERRE	0
Bit 14	R/W	FIFO_UDRE	0
Bit 13	R/W	XFERE	0
Bit 12	R/W	LEN_ERRE	0
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

LEN_ERRE

The LEN_ERRE bit enables the generation of an interrupt due to an ATM cell length error appearing on the FIFO Interface. When LEN_ERRE is set to logic 1, the interrupt is enabled. In GFP mode, the interrupt is not used.

XFERE

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the transmitted cell/packet/frame counter, transmitted byte counter, and aborted packet counter holding registers. When XFERE is set to logic 1, the interrupt is enabled.

FIFO_UDRE

The FIFO_UDRE bit enables the generation of an interrupt due to a FIFO under-run. When FIFO_UDRE is set to logic 1, the interrupt is enabled and the signal INTB will be set to logic 1 whenever FIFO_UNRI is set to logic 1.

FIFO_ERRE

The FIFO_ERRE bit enables the generation of an interrupt due to a FIFO error. When FIFO_ERRE is set to logic 1, the interrupt is enabled and the signal INTB will be set to logic 1 whenever FIFO_ERRI is set to logic 1.

Downloaded by Cortex Team of Raytheon Inc. on Wednesday, 07 February, 2007 06:59:32 PM

Register 3024H: TCFP-9953 ATM Idle Cell Format

Bit	Type	Function	Default
Bit 15	R/W	GFC[3]	0
Bit 14	R/W	GFC[2]	0
Bit 13	R/W	GFC[1]	0
Bit 12	R/W	GFC[0]	0
Bit 11	R/W	PTI[2]	0
Bit 10	R/W	PTI[1]	0
Bit 9	R/W	PTI[0]	0
Bit 8	R/W	CLP	1
Bit 7	R/W	PAYLD[7]	0
Bit 6	R/W	PAYLD[6]	1
Bit 5	R/W	PAYLD[5]	1
Bit 4	R/W	PAYLD[4]	0
Bit 3	R/W	PAYLD[3]	1
Bit 2	R/W	PAYLD[2]	0
Bit 1	R/W	PAYLD[1]	1
Bit 0	R/W	PAYLD[0]	0

The contents of this register are only used in ATM mode.

PAYLD[7:0]

When the TCFP-9953 is in ATM mode, the PAYLD[7:0] (ATM Cell Payload) bits contain the data pattern which will be used to fill the payload of idle/unassigned cells in ATM mode.

CLP

In ATM mode, the CLP (Cell Loss Priority) bit contains the eighth bit position of the fourth octet of the idle/unassigned cell pattern.

PTI[2:0]

In ATM mode, the PTI[2:0] (Payload Type) bits contain the fifth, sixth, and seventh bit positions of the fourth octet of the idle/unassigned cell pattern.

GFC[3:0]

In ATM mode, the GFC[3:0] (Generic Flow Control) bits contain the first, second, third, and fourth bit positions of the first octet of the idle/unassigned cell pattern.

Downloaded by Conten Team of Datasheet Miner Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 3025H: TCFP-9953 CRC Diagnostics

Bit	Type	Function	Default
Bit 15	R/W	DCRC[15]	0
Bit 14	R/W	DCRC[14]	0
Bit 13	R/W	DCRC[13]	0
Bit 12	R/W	DCRC[12]	0
Bit 11	R/W	DCRC[11]	0
Bit 10	R/W	DCRC[10]	0
Bit 9	R/W	DCRC[9]	0
Bit 8	R/W	DCRC[8]	0
Bit 7	R/W	DCRC[7]	0
Bit 6	R/W	DCRC[6]	0
Bit 5	R/W	DCRC[5]	0
Bit 4	R/W	DCRC[4]	0
Bit 3	R/W	DCRC[3]	0
Bit 2	R/W	DCRC[2]	0
Bit 1	R/W	DCRC[1]	0
Bit 0	R/W	DCRC[0]	0

DCRC[15:0]

The diagnostic CRC word (DCRC[15:0]) controls the logical inversion of bits in the inserted CRC on the outgoing data stream for diagnostic purposes.

In ATM modes, the DCRC[7:0] value is bit-wise XORed with the calculated CRC result before insertion into the transmission stream.

In POS mode the DCRC[7:0] value is bit-wise XORed with all four bytes of the FCS field before insertion into the transmission stream.

In GFP mode, the DCRC[15:0] value is bit-wise XORed with any of the three HECs when the associated HEC_CRPT_EN configuration parameter is set to logic one. Similarly, The DCRC[7:0] value is bitwise XORed with all four bytes of the GFP FCS field when the FCS_CRPT_EN configuration parameter is set to a logic one.

Downloaded by Content Team Partsinfo.com on Wednesday, 07 February, 2007 06:59:32 PM

Register 3026H: TCFP-9953 General Diagnostics

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	CHEC_CRPT_EN	0
Bit 9	R/W	THEC_CRPT_EN	0
Bit 8	R/W	EHEC_CRPT_EN	0
Bit 7	R/W	SHEC_CRPT_EN	0
Bit 6	R/W	FCS_CRPT_EN	0
Bit 5	R/W	TX_BYTE_MODE	0
Bit 4	R/W	XOFF	0
Bit 3	R/W	INVERT	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

INVERT

The data inversion bit (INVERT) configures the ATM/POS/GFP processor to logically invert the outgoing data stream. When INVERT is set to logic 1, the outgoing data stream is logically inverted. The outgoing data stream is not inverted when INVERT is set to logic 0. This bit is valid in all modes.

XOFF

The XOFF serves as a transmission enable bit. When XOFF is set to logic 0, cells/packet/frames are transmitted normally. When XOFF is set to logic 1, the cell/packet/frame being transmitted is completed and then transmission is suspended. When XOFF is set to logic 1, the TCFP-9953 will not request data. ATM Idle cells/POS flags/GFP idle frames, will be sent on the TCFP-9953 egress interface. This bit is valid in all modes.

Downloaded by Content Tools of Partminer Inc. on Wednesday, 07 February, 2007 06:59:32 PM

TX_BYTE_MODE

The transmit byte counter mode (TX_BYTE_MODE) bit is used to select the mode in which the TX_BYTE[39:0] counters work. When TX_BYTE_MODE is logic 0, TX_BYTE[39:0] will count all bytes in transmitted packets (including FCS and Aborted EOP bytes) before the byte stuffing operation. When TX_BYTE_MODE is logic 1, TX_BYTE[39:0] will count all bytes in transmitted packets (including FCS, Aborted EOP, and stuff bytes) after the byte stuffing operation. Flag bytes will not be counted in either case. The TX_BYTE_MODE bit is only valid when working in POS mode.

Reserved

The Reserved bits must be set to the default value as shown for proper operation of the S/UNI 9953.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 02:52 PM

Register 3027H: TCFP-9953 Transmit Cell/Packet/Frame Counter (LSB)

Bit	Type	Function	Default
Bit 15	R	TX_CPF[15]	X
Bit 14	R	TX_CPF[14]	X
Bit 13	R	TX_CPF[13]	X
Bit 12	R	TX_CPF[12]	X
Bit 11	R	TX_CPF[11]	X
Bit 10	R	TX_CPF[10]	X
Bit 9	R	TX_CPF[9]	X
Bit 8	R	TX_CPF[8]	X
Bit 7	R	TX_CPF[7]	X
Bit 6	R	TX_CPF[6]	X
Bit 5	R	TX_CPF[5]	X
Bit 4	R	TX_CPF[4]	X
Bit 3	R	TX_CPF[3]	X
Bit 2	R	TX_CPF[2]	X
Bit 1	R	TX_CPF[1]	X
Bit 0	R	TX_CPF[0]	X

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 3028H: TCFP-9953 Transmit Cell/Packet/Frame Counter (MSB)

Bit	Type	Function	Default
Bit 15	R	TX_CPF[31]	X
Bit 14	R	TX_CPF[30]	X
Bit 13	R	TX_CPF[29]	X
Bit 12	R	TX_CPF[28]	X
Bit 11	R	TX_CPF[27]	X
Bit 10	R	TX_CPF[26]	X
Bit 9	R	TX_CPF[25]	X
Bit 8	R	TX_CPF[24]	X
Bit 7	R	TX_CPF[23]	X
Bit 6	R	TX_CPF[22]	X
Bit 5	R	TX_CPF[21]	X
Bit 4	R	TX_CPF[20]	X
Bit 3	R	TX_CPF[19]	X
Bit 2	R	TX_CPF[18]	X
Bit 1	R	TX_CPF[17]	X
Bit 0	R	TX_CPF[16]	X

TX_CPF[31:0]

The TX_CPF[31:0] bits indicate the number of cells/frames or non-aborted packets transmitted to the TCFP-9953 egress stream during the last accumulation interval. ATM Idle cells, POS flag bursts and GFP Idle frames inserted into the transmission stream are not counted.

A write to any one of the TCFP-9953 statistics counter registers (TX_CPF, TX_BYTE, TX_ABRT and TX_IDLE) loads the registers with the current counter value and resets the internal 32 bit counter. The counter reset value is dependent on the number of count events during the transfer. The counter should be polled regularly to avoid saturating. The contents of these registers are valid three TCLK cycles after a transfer is triggered by a write to any of the TCFP-9953 statistics counter registers.

This counter can also be loaded by a microprocessor write to the S/UNI 9953 Identity and Global Performance Monitor Update register (0000H).

Downloaded by Content Team at Data Sheet Direct Wednesday, 07 February, 2007 06:59:32 PM

Register 3029H: TCFP-9953 Transmit Byte Counter (LSB)

Bit	Type	Function	Default
Bit 15	R	TX_BYTE[15]	X
Bit 14	R	TX_BYTE[14]	X
Bit 13	R	TX_BYTE[13]	X
Bit 12	R	TX_BYTE[12]	X
Bit 11	R	TX_BYTE[11]	X
Bit 10	R	TX_BYTE[10]	X
Bit 9	R	TX_BYTE[9]	X
Bit 8	R	TX_BYTE[8]	X
Bit 7	R	TX_BYTE[7]	X
Bit 6	R	TX_BYTE[6]	X
Bit 5	R	TX_BYTE[5]	X
Bit 4	R	TX_BYTE[4]	X
Bit 3	R	TX_BYTE[3]	X
Bit 2	R	TX_BYTE[2]	X
Bit 1	R	TX_BYTE[1]	X
Bit 0	R	TX_BYTE[0]	X

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 302AH: TCFP-9953 Transmit BYTE Counter (ISB)

Bit	Type	Function	Default
Bit 15	R	TX_BYTE[31]	X
Bit 14	R	TX_BYTE[30]	X
Bit 13	R	TX_BYTE[29]	X
Bit 12	R	TX_BYTE[28]	X
Bit 11	R	TX_BYTE[27]	X
Bit 10	R	TX_BYTE[26]	X
Bit 9	R	TX_BYTE[25]	X
Bit 8	R	TX_BYTE[24]	X
Bit 7	R	TX_BYTE[23]	X
Bit 6	R	TX_BYTE[22]	X
Bit 5	R	TX_BYTE[21]	X
Bit 4	R	TX_BYTE[20]	X
Bit 3	R	TX_BYTE[19]	X
Bit 2	R	TX_BYTE[18]	X
Bit 1	R	TX_BYTE[17]	X
Bit 0	R	TX_BYTE[16]	X

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 302BH: TCFP-9953 Transmit BYTE Counter (MSB)

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	TX_BYTE[39]	X
Bit 6	R	TX_BYTE[38]	X
Bit 5	R	TX_BYTE[37]	X
Bit 4	R	TX_BYTE[36]	X
Bit 3	R	TX_BYTE[35]	X
Bit 2	R	TX_BYTE[34]	X
Bit 1	R	TX_BYTE[33]	X
Bit 0	R	TX_BYTE[32]	X

TX_BYTE[39:0]

In POS mode, the TX_BYTE[39:0] bits indicate the number of bytes in packets transmitted to the TCFP-9953 egress stream during the last accumulation interval. The byte counts include all user payload bytes, FCS bytes, and aborted EOP bytes. Inclusion of POS stuff bytes is controlled by the TX_BYTE_MODE register bit. HDLC flags are not counted. Note that the additional POS flag byte inserted after the aborted EOP byte is not counted.

In DELINDIS mode, the TX_BYTE[39:0] bits indicate the number of valid bytes read from the FIFO Interface and inserted into the transmission stream.

The TX_BYTE[39:0] count is only valid in POS or DELINDIS mode.

A write to any one of the TCFP-9953 statistics counter registers (TX_CPF, TX_BYTE, TX_ABRT and TX_IDLE) loads the register with the current counter value and resets the internal 40 bit counter. The counter reset value is dependent on the number of count events during the transfer. The counter should be polled regularly to avoid saturating. The contents of these registers are valid three TCLK cycles after a transfer is triggered by a write to any of the TCFP-9953 statistics counter registers.

This counter can also be loaded by a microprocessor write to the S/UNI 9953 Identity and Global Performance Monitor Update register (0000H).

Downloaded by Connie Tsen of Pan Jit on Wednesday, 07 February, 2007 06:59:32 PM

Register 302CH: TCFP-9953 Aborted Packet Counter

Bit	Type	Function	Default
Bit 15	R	TX_ABRT[15]	X
Bit 14	R	TX_ABRT[14]	X
Bit 13	R	TX_ABRT[13]	X
Bit 12	R	TX_ABRT[12]	X
Bit 11	R	TX_ABRT[11]	X
Bit 10	R	TX_ABRT[10]	X
Bit 9	R	TX_ABRT[9]	X
Bit 8	R	TX_ABRT[8]	X
Bit 7	R	TX_ABRT[7]	X
Bit 6	R	TX_ABRT[6]	X
Bit 5	R	TX_ABRT[5]	X
Bit 4	R	TX_ABRT[4]	X
Bit 3	R	TX_ABRT[3]	X
Bit 2	R	TX_ABRT[2]	X
Bit 1	R	TX_ABRT[1]	X
Bit 0	R	TX_ABRT[0]	X

TX_ABRT[15:0]

The TX_ABRT[15:0] bits indicate the number of aborted packets transmitted to the TCFP-9953 egress stream during the last accumulation interval.

These counters are only valid when POS mode is selected.

A write to any one of the TCFP-9953 statistics counter registers (TX_CPF, TX_BYTE, TX_ABRT and TX_IDLE) loads the register with the current counter value and resets the internal 16 bit counter. The counter reset value is dependent on the number of count events during the transfer. The counter should be polled regularly to avoid saturating. The contents of these registers are valid three TCLK cycles after a transfer is triggered by a write to any of the TCFP-9953 statistics counter registers.

This counter can also be loaded by a microprocessor write to the S/UNI 9953 Identity and Global Performance Monitor Update register (0000H).

Downloaded by Content Team at Datasheet inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 302DH: TCFP-9953 Transmit Idle Frame Counter (LSB)

Bit	Type	Function	Default
Bit 15	R	TX_IDLE[15]	X
Bit 14	R	TX_IDLE [14]	X
Bit 13	R	TX_IDLE [13]	X
Bit 12	R	TX_IDLE [12]	X
Bit 11	R	TX_IDLE [11]	X
Bit 10	R	TX_IDLE [10]	X
Bit 9	R	TX_IDLE [9]	X
Bit 8	R	TX_IDLE [8]	X
Bit 7	R	TX_IDLE [7]	X
Bit 6	R	TX_IDLE [6]	X
Bit 5	R	TX_IDLE [5]	X
Bit 4	R	TX_IDLE [4]	X
Bit 3	R	TX_IDLE [3]	X
Bit 2	R	TX_IDLE [2]	X
Bit 1	R	TX_IDLE [1]	X
Bit 0	R	TX_IDLE [0]	X

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 302EH: TCFP-9953 Transmit Idle Frame Counter (MSB)

Bit	Type	Function	Default
Bit 15	R	TX_IDLE[31]	X
Bit 14	R	TX_IDLE [30]	X
Bit 13	R	TX_IDLE [29]	X
Bit 12	R	TX_IDLE [28]	X
Bit 11	R	TX_IDLE [27]	X
Bit 10	R	TX_IDLE [26]	X
Bit 9	R	TX_IDLE [25]	X
Bit 8	R	TX_IDLE [24]	X
Bit 7	R	TX_IDLE [23]	X
Bit 6	R	TX_IDLE [22]	X
Bit 5	R	TX_IDLE [21]	X
Bit 4	R	TX_IDLE [20]	X
Bit 3	R	TX_IDLE [19]	X
Bit 2	R	TX_IDLE [18]	X
Bit 1	R	TX_IDLE [17]	X
Bit 0	R	TX_IDLE [16]	X

TX_IDLE[31:0]

The TX_IDLE[31:0] bits indicate the number of GFP idle frames inserted into the transmission stream during the last accumulation interval.

These counters are only valid when GFP mode is selected.

A write to any one of the TCFP-9953 statistics counter registers (TX_CPF, TX_BYTE, TX_ABRT and TX_IDLE) loads the register with the current counter value and resets the internal 32 bit counter. The counter reset value is dependent on the number of count events during the transfer. The counter should be polled regularly to avoid saturating. The contents of these registers are valid three TCLK cycles after a transfer is triggered by a write to any of the TCFP-9953 statistics counter registers.

This counter can also be loaded by a microprocessor write to the S/UNI 9953 Identity and Global Performance Monitor Update register (0000H).

Downloaded by Content Team at Datasheet Inc. on Wednesday, 07 February, 2007 06:59:32 PM

12.31 Transmit Ethernet Processor 10 Gigabits (TXXG)

Register 3040H: TXXG Configuration 1

Bit	Type	Function	Default
Bit 15	R/W	TXEN0	0
Bit 14	—	Unused	X
Bit 13	R/W	HOSTPAUSE	0
Bit 12	R/W	IPGT[5]	0
Bit 11	R/W	IPGT[4]	0
Bit 10	R/W	IPGT[3]	1
Bit 9	R/W	IPGT[2]	1
Bit 8	R/W	IPGT[1]	0
Bit 7	R/W	IPGT[0]	0
Bit 6	—	Unused	X
Bit 5	R/W	32BIT_ALIGN	0
Bit 4	R/W	CRCEN	0
Bit 3	R/W	FCTX	0
Bit 2	R/W	FCRX	0
Bit 1	R/W	PADEN	0
Bit 0	R/W	Reserved	0

PADEN

If set, the TXXG will pad all IEEE 802.3 transmitted frames that are less than the minimum size up to the minimum size for a valid 802.3 frame. The minimum size is set by the Transmit Min Frame Size Register. Padding is done by inserting zero-filled octets between the end of the payload and the Start of the FCS field. Note that only IEEE 802.3 frames (those with Length/Type fields set to 0x05DC or less) are padded; Ethernet V2.0 frames with Length/Type fields greater than 0x05DC are never padded, regardless of the setting of PADEN. If an IEEE 802.3 frame has a VLAN tag inserted, it will be padded to the minimum size + 4 bytes.

FCRX

If set, the TXXG will respond to transmit pausing requests input on the RPAUSET[15:0] and PAUSE signals; otherwise, the TXXG ignores these signals and never interrupts the outgoing transmit stream.

FCTX

If set, the TXXG will respond to PAUSE frame transmit requests that are input on PAUSESEND[1:0]; otherwise, the TXXG ignores these signals and never injects PAUSE frames into the transmit stream.

Downloaded by Control Team of Petrolink Inc on Wednesday, 07 February 2007 06:59:32 PM

CRCEN

If CRCEN is set then all frames transmitted will have a 4 byte CRC appended. If CRCEN is not set, frames transmitted will not have a CRC appended. Note: MAC Control Pause Packets generated internally will always have a valid CRC appended, regardless of the setting of CRCEN. Corrupt packets [error bit set] will always have a corrupt CRC appended, regardless of the setting of CRCEN.

32BIT_ALIGN

The default value of logic zero must be over-written to logic 1 for normal operation of the device.

IPGT [5:0]

Back-to-Back Transmit IPG. This is a programmable field representing the IPG between back-to-back packets. This is the IPG parameter used in Full-Duplex mode. Set this field to the number of octets of IPG desired. A setting of 12 decimal represents the minimum IPG of 0.0096µs. The IPG setting is a average setting due to the 32-bit alignment requirement. The IPG may be +/- 3 bytes from the programmed IPG, and on average the IPG is the programmed value. Because of the 32-bit alignment requirement the minimum programmed IPG that will not cause errors is 8 bytes +/- 3 bytes. So the minimum allowed setting of IPGT is 0x08.

HOSTPAUSE

HOSTPAUSE enable bit. When this bit is set to a 1 the TXXG will send PAUSE Control Frames based on the PAUSE timer and PAUSE interval registers. The operation of HOSTPAUSE is masked by FCTX.

TXEN0

This bit must be set to enable TXXG to transmit packets from the System Interface or from the internal Outgoing Flow Control block. All TXXG programming should be performed before setting this bit. If this bit is cleared during packet transmission, the current packet transmit will proceed to completion, and no new packet transmission initiated.

Downloaded by Content Technology Partmill Inc on Wednesday, 14 February, 2007 06:58:32 AM

Register 3041H: TXXG Configuration 2

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 06:59:32 PM

Register 3042H: TXXG Configuration 3

Bit	Type	Function	Default
Bit 15	R/W	FIFO_ERRE	0
Bit 14	R/W	FIFO_UDRE	0
Bit 13	R/W	MAX_LERRE	0
Bit 12	R/W	MIN_LERRE	0
Bit 11	R/W	XFERE	0
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

XFERE

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the filter error counter holding register. When XFERE is set to logic 1, the interrupt is enabled.

MIN_LERRE

The MIN_LERRE bit enables the generation of an interrupt due to a packet sourced from the System interface being less than the minimum frame size programmed in the Transmit Min Frame Size Register.

MAX_LERRE

The MAX_LERRE bit enables the generation of an interrupt due to a packet sourced from the System interface exceeding the maximum frame size programmed in the Transmit Max Frame Size Register.

FIFO_UDRE

The FIFO_UDRE bit enables the generation of an interrupt due to a FIFO underrun event. When the FIFO_ERRE bit is set to logic 1, an underrun event will cause the FIFO_UDRI bit to be set in the Interrupt register.

Downloaded by Contents Mgmt of Raytheon Inc. on Wednesday, 07 February, 2007 06:59:32 PM

FIFO_ERRE

The FIFO_ERRE bit enables the generation of an interrupt due to a FIFO error event. When the FIFO_ERRE bit is set to logic 1, a FIFO error event will cause the FIFO_ERRI bit to be set in the Interrupt register. FIFO error events are:

(1) FIFO_ERR asserted with FIFO_EOP.
(2) Invalid SOP/ EOP sequence.
(3) Invalid gapping during data transfer.
(4) Frame length less than 9 bytes.
(5) FIFO overrun.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 3043H: TXXG Interrupt

Bit	Type	Function	Default
Bit 15	R	FIFO_ERRI	X
Bit 14	R	FIFO_UDRI	X
Bit 13	R	MAX_LERRI	X
Bit 12	R	MIN_LERRI	X
Bit 11	R	XFERI	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, these interrupt status bits are cleared on write with a logic 1. Otherwise, these interrupt status bits are cleared on read as per register bit description.

XFERI

The XFERI bit indicates that a transfer of accumulated counter data has occurred. A logic 1 in this bit position indicates that the filter error counter holding register has been updated. This update is initiated by writing to one of the counter register locations, or by a microprocessor write to the S/UNI 9953 Identity and Global Performance Monitor Update register (0000H). If XFERE is set in Configuration Register 2, then an interrupt will also be generated (INTB output asserted). This bit is cleared to logic 0 when register is read.

MIN_LERRI

The MIN_LERRI bit is set when the packet sourced from the FIFO is less than the value programmed in the Transmit Min Frame Size Register. If MIN_LERRE is set in Configuration Register 2, then an interrupt will also be generated (INTB output asserted). This bit is cleared to logic 0 when register is read.

Downloaded by Conexant Systems Inc on Wednesday, 07 February, 2007 06:59:32 PM

MAX_LERRI

The MAX_LERRI bit is set when the packet sourced from the FIFO exceeds the value programmed in the Transmit Max Frame Size Register. If MAX_LERRE is set in Configuration Register 2, then an interrupt will also be generated (INTB output asserted). This bit is cleared to logic 0 when register is read.

FIFO_UDRI

The FIFO_UDRI bit is set when a FIFO underrun event occurs. An underrun condition exists if the TXXG is in the middle of transmitting a packet and no additional data is available to be transmitted. If FIFO_UDRE is set in Configuration Register 2, then an interrupt will also be generated (INTB output asserted). This bit is cleared to logic 0 when register is read.

FIFO_ERRI

The FIFO_ERRI bit is set when a FIFO error event occurs. FIFO error events are

(1) FIFO_ERR asserted with FIFO_EOP.
(2) Invalid SOP/ EOP sequence.
(3) Invalid gapping during data transfer.
(4) Frame length less than 9 bytes.
(5) FIFO overrun.

If FIFO_ERRE is set in TXXG Configuration Register 2, then an interrupt will also be generated (INTB output asserted). This bit is cleared to logic 0 when register is read.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 06:59:32 PM

Register 3044H: TXXG Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R	TXACTIVE	0
Bit 0	R	PAUSED	0

PAUSED

When set, indicates that the PAUSE timer is non-zero. This will happen whenever the RXXG interface transfers a non-zero pause value, or the CPU test mode loads a non-zero value, and the timer has not yet decremented to 0.

TXACTIVE

When set, indicates that the MAC Core is currently in the process of transmitting a packet from the System interface to the Line interface, or from the MAC Outgoing Flow Control block to the Line interface.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:59:32 PM

Register 3045H: TXXG TX_MAXFR - Transmit Max Frame Size

Bit	Type	Function	Default
Bit 15	R/W	TX_MAXFR[15]	0
Bit 14	R/W	TX_MAXFR[14]	0
Bit 13	R/W	TX_MAXFR[13]	0
Bit 12	R/W	TX_MAXFR[12]	0
Bit 11	R/W	TX_MAXFR[11]	0
Bit 10	R/W	TX_MAXFR[10]	1
Bit 9	R/W	TX_MAXFR[9]	0
Bit 8	R/W	TX_MAXFR[8]	1
Bit 7	R/W	TX_MAXFR[7]	1
Bit 6	R/W	TX_MAXFR[6]	1
Bit 5	R/W	TX_MAXFR[5]	1
Bit 4	R/W	TX_MAXFR[4]	0
Bit 3	R/W	TX_MAXFR[3]	1
Bit 2	R/W	TX_MAXFR[2]	1
Bit 1	R/W	TX_MAXFR[1]	1
Bit 0	R/W	TX_MAXFR[0]	0

TX_MAXFR[15:0]

TX_MAXFR[15:0] places an upper bound on a transmitted Ethernet frame, in octets. The length is measured from the first byte of the destination address to the last byte of the FCS field. The default is 0x05EE, corresponding to the Standard setting of 1518 bytes. If the pre-set frame length is exceeded by the frame source, the TXXG unit will truncate the outgoing frame, force a CRC error, and discard all subsequently received bytes until the next SOF.

Downloaded by Content Team of Partminer on Wednesday, 07 February, 2007 06:59:32 PM

Register 3046H: TXXG TX_MINFR - Transmit Min Frame Size

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	TX_MINFR[7]	0
Bit 6	R/W	TX_MINFR[6]	0
Bit 5	R/W	TX_MINFR[5]	1
Bit 4	R/W	TX_MINFR[4]	1
Bit 3	R/W	TX_MINFR[3]	1
Bit 2	R/W	TX_MINFR[2]	1
Bit 1	R/W	TX_MINFR[1]	0
Bit 0	R/W	TX_MINFR[0]	0

TX_MINFR[7:0]

The TX_MINFR[7:0] field is used to set a lower limit on the size of a transmitted Ethernet frame. The length is measured from the first byte of the destination address to the last byte of the payload, excluding the 4-byte FCS field. The default is set to 60 decimal, corresponding to the nominal 64-byte minimum-size frame. If the TXXG receives an IEEE 802.3 frame (i.e., with the Length/ Type field set to 0x05DC or less) that is smaller than TX_MINFR[7:0], and the PADEN bit is set in the Configuration Register 1, it will pad the frame to TX_MINFR[7:0] with zeros.

Downloaded by Content Team of Parts Life Co. Wednesday, 07 February, 2007 06:59:32 PM

Register 3047H: TXXG SA[15:0] - Station Address

Bit	Type	Function	Default
Bit 15	R/W	SA[15]	0
Bit 14	R/W	SA[14]	0
Bit 13	R/W	SA[13]	0
Bit 12	R/W	SA[12]	0
Bit 11	R/W	SA[11]	0
Bit 10	R/W	SA[10]	0
Bit 9	R/W	SA[9]	0
Bit 8	R/W	SA[8]	0
Bit 7	R/W	SA[7]	0
Bit 6	R/W	SA[6]	0
Bit 5	R/W	SA[5]	0
Bit 4	R/W	SA[4]	0
Bit 3	R/W	SA[3]	0
Bit 2	R/W	SA[2]	0
Bit 1	R/W	SA[1]	0
Bit 0	R/W	SA[0]	0

SA[15:0]

The SA[15:0] register sets the low 16 bits of the 48-bit Station address used for PAUSE frame generation.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 3048H: TXXG SA[31:16] - Station Address

Bit	Type	Function	Default
Bit 15	R/W	SA[31]	0
Bit 14	R/W	SA[30]	0
Bit 13	R/W	SA[29]	0
Bit 12	R/W	SA[28]	0
Bit 11	R/W	SA[27]	0
Bit 10	R/W	SA[26]	0
Bit 9	R/W	SA[25]	0
Bit 8	R/W	SA[24]	0
Bit 7	R/W	SA[23]	0
Bit 6	R/W	SA[22]	0
Bit 5	R/W	SA[21]	0
Bit 4	R/W	SA[20]	0
Bit 3	R/W	SA[19]	0
Bit 2	R/W	SA[18]	0
Bit 1	R/W	SA[17]	0
Bit 0	R/W	SA[16]	0

SA[31:16]

The SA[31:16] register sets the middle 16 bits of the 48-bit Station address used for PAUSE frame generation.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 3049H: TXXG SA[47:32] - Station Address

Bit	Type	Function	Default
Bit 15	R/W	SA[47]	0
Bit 14	R/W	SA[46]	0
Bit 13	R/W	SA[45]	0
Bit 12	R/W	SA[44]	0
Bit 11	R/W	SA[43]	0
Bit 10	R/W	SA[42]	0
Bit 9	R/W	SA[41]	0
Bit 8	R/W	SA[40]	0
Bit 7	R/W	SA[39]	0
Bit 6	R/W	SA[38]	0
Bit 5	R/W	SA[37]	0
Bit 4	R/W	SA[36]	0
Bit 3	R/W	SA[35]	0
Bit 2	R/W	SA[34]	0
Bit 1	R/W	SA[33]	0
Bit 0	R/W	SA[32]	0

SA[47:32]

The SA[47:32] register sets the high 16 bits of the 48-bit Station address used for PAUSE frame generation.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 304AH: TXXG Diagnostic 1

Bit	Type	Function	Default
Bit 15	R/W	HOST_EXT_BYTE[7]	0
Bit 14	R/W	HOST_EXT_BYTE[6]	0
Bit 13	R/W	HOST_EXT_BYTE[5]	0
Bit 12	R/W	HOST_EXT_BYTE[4]	0
Bit 11	R/W	HOST_EXT_BYTE[3]	0
Bit 10	R/W	HOST_EXT_BYTE[2]	0
Bit 9	R/W	HOST_EXT_BYTE[1]	0
Bit 8	R/W	HOST_EXT_BYTE[0]	0
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R/W	LDPAUSETMR	0
Bit 1	R/W	RPAUSETST	0
Bit 0	R/W	DIAG_HOSTPAUSE	0

DIAG_HOSTPAUSE

DIAG_HOSTPAUSE enable bit. When set to a 1 the TXXG will send PAUSE Control Frames based on the PAUSE timer and PAUSE interval registers. When this operation has been completed, the DIAG_HOSTPAUSEDONE event bit will be set in the TXXG Diagnostic Status Register. Setting the bit to a 0 will cause the TXXG to no longer send PAUSE Control Frames. This is provided for system diagnostic purposes only.

LDPAUSETMR

When this bit is toggled from 0 to 1, the TXXG Incoming MAC Control block will load the pause timer with the value programmed in TXXG Diagnostic Register 2. This is provided for system diagnostic purposes only.

RPAUSETST

When this bit is set, the unit of decrement (pause quanta value) for the incoming pause timer is TCLKx2. When this bit is clear (normal mode), the unit of decrement is dependent on the value programmed in FC_PAUSE_QNTM[7:0] in the TXXG Pause Quantum Value Configuration Register. If the value programmed is 7 [default], the unit of decrement will be TCLKx2/8 [512 bit times].

Downloaded by Corinet Teamcenter Partmint on Wednesday, 07 February, 2007 06:59:32 PM

HOST_EXT_BYTE[7:0]

HOST_EXT_BYTE [7:0] contains the number of extra pad bytes that TXXG will append to an outgoing flow control packet in diagnostic mode. In normal mode, HOST_EXT_BYTE [7:0] will be set to 0x00.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 304BH: TXXG Diagnostic 2

Bit	Type	Function	Default
Bit 15	R/W	TSTRPAUSE[15]	0
Bit 14	R/W	TSTRPAUSE[14]	0
Bit 13	R/W	TSTRPAUSE[13]	0
Bit 12	R/W	TSTRPAUSE[12]	0
Bit 11	R/W	TSTRPAUSE[11]	0
Bit 10	R/W	TSTRPAUSE[10]	0
Bit 9	R/W	TSTRPAUSE[9]	0
Bit 8	R/W	TSTRPAUSE[8]	0
Bit 7	R/W	TSTRPAUSE[7]	0
Bit 6	R/W	TSTRPAUSE[6]	0
Bit 5	R/W	TSTRPAUSE[5]	0
Bit 4	R/W	TSTRPAUSE[4]	0
Bit 3	R/W	TSTRPAUSE[3]	0
Bit 2	R/W	TSTRPAUSE[2]	0
Bit 1	R/W	TSTRPAUSE[1]	0
Bit 0	R/W	TSTRPAUSE[0]	0

TSTRPAUSE[15:0]

The TSTRPAUSE[15:0] register works in conjunction with the LDPAUSETMR bit in TXXG Diagnostic Register 1. This register must be programmed before LDPAUSETMR is toggled from 0 to 1.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 304CH: TXXG Diagnostic Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R	DIAG_HOSTPAUSEDONE	0

DIAG_HOSTPAUSEDONE

This Status bit will be set in response to the DIAG_HOSTPAUSE bit being set in TXXG Diagnostic 1 Register, when the MAC Flow Control packet has been successfully transmitted.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 304DH: TXXG PAUSE_TIME – PAUSE TIMER

Bit	Type	Function	Default
Bit 15	R/W	PAUSE_TIME[15]	1
Bit 14	R/W	PAUSE_TIME [14]	1
Bit 13	R/W	PAUSE_TIME [13]	1
Bit 12	R/W	PAUSE_TIME [12]	1
Bit 11	R/W	PAUSE_TIME [11]	1
Bit 10	R/W	PAUSE_TIME [10]	1
Bit 9	R/W	PAUSE_TIME [9]	1
Bit 8	R/W	PAUSE_TIME [8]	1
Bit 7	R/W	PAUSE_TIME [7]	1
Bit 6	R/W	PAUSE_TIME [6]	1
Bit 5	R/W	PAUSE_TIME [5]	1
Bit 4	R/W	PAUSE_TIME [4]	1
Bit 3	R/W	PAUSE_TIME [3]	1
Bit 2	R/W	PAUSE_TIME [2]	1
Bit 1	R/W	PAUSE_TIME [1]	1
Bit 0	R/W	PAUSE_TIME [0]	1

PAUSE_TIME [15:0}

This register contains the PAUSE timer value that is used on the PAUSE Control Frames that are sent to the Line Interface. The default is 0xFFFF for an XON/XOFF type of protocol. In diagnostic mode, this register must be programmed before DIAG_HOSTPAUSE is toggled from 0 to 1. In normal mode, this register must be programmed before HOSTPAUSE is toggled from 0 to 1.

Downloaded by Content Team of Partminer on Wednesday, 07 February, 2007 06:59:32 PM

Register 304EH: TXXG PAUSE_IVAL – PAUSE Timer Interval

Bit	Type	Function	Default
Bit 15	R/W	PAUSE_IVAL[15]	1
Bit 14	R/W	PAUSE_ IVAL [14]	1
Bit 13	R/W	PAUSE_ IVAL [13]	0
Bit 12	R/W	PAUSE_ IVAL[12]	0
Bit 11	R/W	PAUSE_ IVAL [11]	1
Bit 10	R/W	PAUSE_ IVAL [10]	1
Bit 9	R/W	PAUSE_ IVAL [9]	1
Bit 8	R/W	PAUSE_ IVAL [8]	1
Bit 7	R/W	PAUSE_ IVAL [7]	1
Bit 6	R/W	PAUSE_ IVAL [6]	1
Bit 5	R/W	PAUSE_ IVAL [5]	1
Bit 4	R/W	PAUSE_ IVAL [4]	1
Bit 3	R/W	PAUSE_ IVAL [3]	1
Bit 2	R/W	PAUSE_ IVAL [2]	1
Bit 1	R/W	PAUSE_ IVAL [1]	1
Bit 0	R/W	PAUSE_ IVAL [0]	1

PAUSE_ IVAL [15:0]

This register contains the Pause Timer Interval value that is used by the PAUSE Generation Logic to control how often a PAUSE Control frame is sent. The default value is 0xCFFF. In diagnostic mode, this register must be programmed before DIAG_HOSTPAUSE is toggled from 0 to 1. In normal mode, this register must be programmed before HOSTPAUSE is toggled from 0 to 1.

Downloaded by Content Team of Partminer on Wednesday, 07 February, 2007 06:59:32 PM

Register 304FH: TXXG Packet Statistics (Lower 14 bits)

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R	TXSTAT[13]	0
Bit 12	R	TXSTAT [12]	0
Bit 11	R	TXSTAT [11]	0
Bit 10	R	TXSTAT [10]	0
Bit 9	R	TXSTAT [9]	0
Bit 8	R	TXSTAT [8]	0
Bit 7	R	TXSTAT [7]	0
Bit 6	R	TXSTAT [6]	0
Bit 5	R	TXSTAT [5]	0
Bit 4	R	TXSTAT [4]	0
Bit 3	R	TXSTAT [3]	0
Bit 2	R	TXSTAT [2]	0
Bit 1	R	TXSTAT [1]	0
Bit 0	R	TXSTAT [0]	0

TXSTAT[13:0]

These register bits are reserved for PMC debug purposes only.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 3050H: TXXG Packet Statistics (Upper 15 bits)

Bit	Type	Function	Default
Bit 15	R	TXSTAT [29]	0
Bit 14	R	TXSTAT [28]	0
Bit 13	R	TXSTAT [27]	0
Bit 12	R	TXSTAT [26]	0
Bit 11	R	TXSTAT [25]	0
Bit 10	R	TXSTAT [24]	0
Bit 9	R	TXSTAT [23]	0
Bit 8	R	TXSTAT [22]	0
Bit 7	R	TXSTAT [21]	0
Bit 6	R	TXSTAT [20]	0
Bit 5	R	TXSTAT [19]	0
Bit 4	R	TXSTAT [18]	0
Bit 3	R	TXSTAT [17]	0
Bit 2	R	TXSTAT [16]	0
Bit 1	R	TXSTAT [15]	0
Bit 0	R	TXSTAT [14]	0

TXSTAT[28:14]

These register bits are reserved for PMC debug purposes only.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 3051H: TXXG Filter Error Counter

Bit	Type	Function	Default
Bit 15	R	FILTER_ERROR[15]	0
Bit 14	R	FILTER_ERROR[14]	0
Bit 13	R	FILTER_ERROR[13]	0
Bit 12	R	FILTER_ERROR[12]	0
Bit 11	R	FILTER_ERROR[11]	0
Bit 10	R	FILTER_ERROR[10]	0
Bit 9	R	FILTER_ERROR[9]	0
Bit 8	R	FILTER_ERROR[8]	0
Bit 7	R	FILTER_ERROR[7]	0
Bit 6	R	FILTER_ERROR[6]	0
Bit 5	R	FILTER_ERROR[5]	0
Bit 4	R	FILTER_ERROR[4]	0
Bit 3	R	FILTER_ERROR[3]	0
Bit 2	R	FILTER_ERROR[2]	0
Bit 1	R	FILTER_ERROR[1]	0
Bit 0	R	FILTER_ERROR[0]	0

FILTER_ERROR[15:0]

The FILTER_ERROR[15:0] register indicates the number of packets that were filtered by the Tx System Interface during the last accumulation interval.

A write to any one of the bits in this register loads the register with the current filter error counter value and resets the internal 16 bit counter. The counter reset value is dependent on the number of count events during the transfer. The counter should be polled regularly to avoid saturating. The contents of this register are valid three TCLK cycles after a transfer is triggered by a write to any of the bits in the register.

This counter can also be loaded by a microprocessor write to the S/UNI 9953 Identity and Global Performance Monitor Update register (0000H).

Downloaded by Content Team on Patton Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 3052H: TXXG Pause Quantum Value Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	R/W	FC_PHY_PACE_EN	0
Bit 7	R/W	FC_PAUSE_QNTM [7]	0
Bit 6	R/W	FC_PAUSE_QNTM [6]	0
Bit 5	R/W	FC_PAUSE_QNTM [5]	0
Bit 4	R/W	FC_PAUSE_QNTM [4]	0
Bit 3	R/W	FC_PAUSE_QNTM [3]	0
Bit 2	R/W	FC_PAUSE_QNTM [2]	1
Bit 1	R/W	FC_PAUSE_QNTM [1]	1
Bit 0	R/W	FC_PAUSE_QNTM [0]	1

FC_PAUSE_QNTM [7:0]

The FC_PAUSE_QNTM [15:0] register indicates the number of TCLKx2 cycles that are to be used for scaling the pause_quantum value (minus 1). A value of 7 means that every 8 TCLKx2 cycles, the local pause timer value decrements by 1. The local pause timer acquires its value from the RXXG when a PAUSE frame is received.

FC_PHY_PACE_EN

If FC_PHY_PACE_EN is set, the local pause timer will stall the decrement operation once in every 33 TCLKx2 cycles.

Downloaded by Content Team of Westminer on Wednesday, February, 2007 06:59:32 PM

12.32 Transmit 64B/66B Processor (T64B66B)

Register 3080H: T64B66B Configuration

Bit	Type	Function	Default
Bit 15	R	~~Reserved~~TIP	0
Bit 14	R/W	SWAVE_LEN[2]	0
Bit 13	R/W	SWAVE_LEN[1]	0
Bit 12	R/W	SWAVE_LEN[0]	0
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	R/W	JDAT_PAT_SEL	0
Bit 7	R/W	JTST_PAT_SEL	0
Bit 6	R/W	JITT_PAT_EN	0
Bit 5	R/W	RXERR_DIS	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	1
Bit 1	R/W	INT_EN	0
Bit 0	R/W	Reserved	1

INT_EN

When ‘1’, the Interrupts are enabled.

When ‘0’, the Interrupts are disabled.

Setting this bit to a logic 1 allows the propagation of the interrupt to the Master Payload Interrupt Status register (0010H).

RXERR_DIS

When ‘1’, The T64B66B Block will ignore all of the receiver detected error events: Loss Of Signal (LOS), Remote Fault (RF), and Local Fault (LF). All data received from the upstream device will be processed as normal. The associated interrupts (RX_LFI, RX_RFI and RX_LOSI) will still assert even if the RX_ERRDIS bit is set to ‘1’.

When ‘0’, The T64B66B Block will NOT ignore the receiver detected error events: Loss Of Signal (LOS), Remote Fault (RF), Local Fault (LF). All data received from the upstream device will be processed as normal only if the receiver is not indicating any error(s).

Downloaded by Content Team of Pasternack Inc. on Wednesday, 07 February, 2007 06:59:32 PM

JITT_PAT_EN

When ‘1’, the T64B66B block will ignore all input data and transmit a jitter test pattern using the scrambler and the data defined by the JDAT_PAT_SEL bit.

When ‘0’ the T64BT66B transmits data normally.

JTST_PAT_SEL

When ‘1’ the square wave test pattern is used for jitter testing. In this mode the T64BT66B transmits a square wave which consists of 4 – 11 alternating series of 1’s and 0’s where the 4 – 11 is defined by the SWAVE_LEN bits.

When ‘0’ the pseudo random test pattern is used for jitter testing. The input to the scrambler is then defined by JDAT_PAT_SEL and the seeds used are defined by the JITTER TEST SEED registers.

JDAT_PAT_SEL

When ‘1’ the zeros data pattern is used for jitter testing. If in pseudo random test pattern mode also, the input to the scrambler is all zeros.

When ‘0’ the LF ordered set is used for jitter testing. When JITT_PAT_EN is ‘1’ also the input to the scrambler is a constant LF.

SWAVE_LEN[2:0]

Number of consecutive 0’s and 1’s that constitute the square wave generated when in square wave test pattern mode. The value is offset by 4 so that the range is from 4 – 11 i.e. SWAVE_LEN[2:0]=000 implies 4 0’s and 1’s.

TIP

Writing a ‘1’ to this bit copies the current value of register 0x3083 to a shadow register. When this bit is read as ‘1’ the transfer is still in progress. When this bit is read as ‘0’, the transfer is complete.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 3083H: T64B66B Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R	RX_LF	X
Bit 5	R	RX_RF	X
Bit 4	R	RX_LOS	X
Bit 3	R	FIFO_UDRFL	X
Bit 2	R	FIFO_OVRFL	X
Bit 1	R	SEQ_ERR	X
Bit 0	R	SOP_ERR	X

SOP_ERR

This register bit is reserved for PMC debug purposes only.

SEQ_ERR

This register bit is reserved for PMC debug purposes only.

FIFO_OVRFL

This register bit is reserved for PMC debug purposes only.

FIFO_UDRFL

This register bit is reserved for PMC debug purposes only.

RX_LOS

This register bit is reserved for PMC debug purposes only.

RX_RF

This register bit is reserved for PMC debug purposes only.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

RX_LF

This register bit is reserved for PMC debug purposes only.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 3084H: T64B66B FIFO STORE THRESHOLD

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	1
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	0

Reserved

These register bits are reserved for PMC debug purposes only, and must be left in their default setting for proper operation of the S/UNI 9953.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 06:59:32 PM

Register 0x3085H: Jitter Test Seed A 3

Bit	Type	Function	Default
Bit 15	R	Unused	X
Bit 14	R	Unused	X
Bit 13	R	Unused	X
Bit 12	R	Unused	X
Bit 11	R	Unused	X
Bit 10	R	Unused	X
Bit 9	R/W	JITT_SEED_A[57]	0
Bit 8	R/W	JITT_SEED_A[56]	0
Bit 7	R/W	JITT_SEED_A[55]	0
Bit 6	R/W	JITT_SEED_A[54]	0
Bit 5	R/W	JITT_SEED_A[53]	0
Bit 4	R/W	JITT_SEED_A[52]	0
Bit 3	R/W	JITT_SEED_A[51]	0
Bit 2	R/W	JITT_SEED_A[50]	0
Bit 1	R/W	JITT_SEED_A[49]	0
Bit 0	R/W	JITT_SEED_A[48]	0

JITT_SEED_A[57:48]

Contains bits 57 down to 48 of the 58 bit pseudo random jitter test pattern seed A.

NOTE: These bits can only be written when jitter pattern generation is turned off, i.e. JITT_PAT_EN is written low.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:59:32 PM

Register 0x3086H: Jitter Test Seed A 2

Bit	Type	Function	Default
Bit 15	R/W	JITT_SEED_A[47]	1
Bit 14	R/W	JITT_SEED_A[46]	1
Bit 13	R/W	JITT_SEED_A[45]	1
Bit 12	R/W	JITT_SEED_A[44]	1
Bit 11	R/W	JITT_SEED_A[43]	1
Bit 10	R/W	JITT_SEED_A[42]	1
Bit 9	R/W	JITT_SEED_A[41]	1
Bit 8	R/W	JITT_SEED_A[40]	1
Bit 7	R/W	JITT_SEED_A[39]	1
Bit 6	R/W	JITT_SEED_A[38]	1
Bit 5	R/W	JITT_SEED_A[37]	1
Bit 4	R/W	JITT_SEED_A[36]	1
Bit 3	R/W	JITT_SEED_A[35]	1
Bit 2	R/W	JITT_SEED_A[34]	1
Bit 1	R/W	JITT_SEED_A[33]	1
Bit 0	R/W	JITT_SEED_A[32]	1

JITT_SEED_A[47:32]

Contains bits 47 down to 32 of the 58 bit pseudo random jitter test pattern seed A.

NOTE: These bits can only be written when jitter pattern generation is turned off, i.e. JITT_PAT_EN is written low.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:59:32 PM

Register 0x3087H: Jitter Test Seed A 1

Bit	Type	Function	Default
Bit 15	R/W	JITT_SEED_A[31]	1
Bit 14	R/W	JITT_SEED_A[30]	1
Bit 13	R/W	JITT_SEED_A[29]	1
Bit 12	R/W	JITT_SEED_A[28]	1
Bit 11	R/W	JITT_SEED_A[27]	1
Bit 10	R/W	JITT_SEED_A[26]	1
Bit 9	R/W	JITT_SEED_A[25]	1
Bit 8	R/W	JITT_SEED_A[24]	1
Bit 7	R/W	JITT_SEED_A[23]	1
Bit 6	R/W	JITT_SEED_A[22]	1
Bit 5	R/W	JITT_SEED_A[21]	1
Bit 4	R/W	JITT_SEED_A[20]	1
Bit 3	R/W	JITT_SEED_A[19]	1
Bit 2	R/W	JITT_SEED_A[18]	1
Bit 1	R/W	JITT_SEED_A[17]	1
Bit 0	R/W	JITT_SEED_A[16]	1

JITT_SEED_A[31:16]

Contains bits 31 down to 16 of the 58 bit pseudo random jitter test pattern seed A.

NOTE: These bits can only be written when jitter pattern generation is turned off, i.e. JITT_PAT_EN is written low.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:59:32 PM

Register 0x3088H: Jitter Test Seed A 0

Bit	Type	Function	Default
Bit 15	R/W	JITT_SEED_A[15]	1
Bit 14	R/W	JITT_SEED_A[14]	1
Bit 13	R/W	JITT_SEED_A[13]	1
Bit 12	R/W	JITT_SEED_A[12]	1
Bit 11	R/W	JITT_SEED_A[11]	1
Bit 10	R/W	JITT_SEED_A[10]	1
Bit 9	R/W	JITT_SEED_A[9]	1
Bit 8	R/W	JITT_SEED_A[8]	1
Bit 7	R/W	JITT_SEED_A[7]	1
Bit 6	R/W	JITT_SEED_A[6]	1
Bit 5	R/W	JITT_SEED_A[5]	1
Bit 4	R/W	JITT_SEED_A[4]	1
Bit 3	R/W	JITT_SEED_A[3]	1
Bit 2	R/W	JITT_SEED_A[2]	1
Bit 1	R/W	JITT_SEED_A[1]	1
Bit 0	R/W	JITT_SEED_A[0]	1

JITT_SEED_A[15:0]

Contains bits 15 down to 0 of the 58 bit pseudo random jitter test pattern seed A.

NOTE: These bits can only be written when jitter pattern generation is turned off, i.e. JITT_PAT_EN is written low.

Downloaded by Content Team of Partminer.com on Wednesday, 07 February, 2007 06:59:32 PM

Register 0x3089H: Jitter Test Seed B 3

Bit	Type	Function	Default
Bit 15	R/W	Unused	X
Bit 14	R	Unused	X
Bit 13	R	Unused	X
Bit 12	R	Unused	X
Bit 11	R	Unused	X
Bit 10	R	Unused	X
Bit 9	R/W	JITT_SEED_B[57]	0
Bit 8	R/W	JITT_SEED_B[56]	0
Bit 7	R/W	JITT_SEED_B[55]	0
Bit 6	R/W	JITT_SEED_B[54]	0
Bit 5	R/W	JITT_SEED_B[53]	0
Bit 4	R/W	JITT_SEED_B[52]	0
Bit 3	R/W	JITT_SEED_B[51]	0
Bit 2	R/W	JITT_SEED_B[50]	0
Bit 1	R/W	JITT_SEED_B[49]	0
Bit 0	R/W	JITT_SEED_B[48]	0

JITT_SEED_B[57:48]

Contains bits 57 down to 48 of the 58 bit pseudo random jitter test pattern seed B.

NOTE: These bits can only be written when jitter pattern generation is turned off, i.e. JITT_PAT_EN is written low.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:59:32 PM

Register 0x308AH: Jitter Test Seed B 2

Bit	Type	Function	Default
Bit 15	R/W	JITT_SEED_B[47]	1
Bit 14	R/W	JITT_SEED_B[46]	1
Bit 13	R/W	JITT_SEED_B[45]	1
Bit 12	R/W	JITT_SEED_B[44]	1
Bit 11	R/W	JITT_SEED_B[43]	1
Bit 10	R/W	JITT_SEED_B[42]	1
Bit 9	R/W	JITT_SEED_B[41]	1
Bit 8	R/W	JITT_SEED_B[40]	1
Bit 7	R/W	JITT_SEED_B[39]	1
Bit 6	R/W	JITT_SEED_B[38]	1
Bit 5	R/W	JITT_SEED_B[37]	1
Bit 4	R/W	JITT_SEED_B[36]	1
Bit 3	R/W	JITT_SEED_B[35]	1
Bit 2	R/W	JITT_SEED_B[34]	1
Bit 1	R/W	JITT_SEED_B[33]	1
Bit 0	R/W	JITT_SEED_B[32]	1

JITT_SEED_B[47:32]

Contains bits 47 down to 32 of the 58 bit pseudo random jitter test pattern seed B.

NOTE: These bits can only be written when jitter pattern generation is turned off, i.e. JITT_PAT_EN is written low.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:59:32 PM

Register 0x308BH: Jitter Test Seed B 1

Bit	Type	Function	Default
Bit 15	R/W	JITT_SEED_B[31]	1
Bit 14	R/W	JITT_SEED_B[30]	1
Bit 13	R/W	JITT_SEED_B[29]	1
Bit 12	R/W	JITT_SEED_B[28]	1
Bit 11	R/W	JITT_SEED_B[27]	1
Bit 10	R/W	JITT_SEED_B[26]	1
Bit 9	R/W	JITT_SEED_B[25]	1
Bit 8	R/W	JITT_SEED_B[24]	1
Bit 7	R/W	JITT_SEED_B[23]	1
Bit 6	R/W	JITT_SEED_B[22]	1
Bit 5	R/W	JITT_SEED_B[21]	1
Bit 4	R/W	JITT_SEED_B[20]	1
Bit 3	R/W	JITT_SEED_B[19]	1
Bit 2	R/W	JITT_SEED_B[18]	1
Bit 1	R/W	JITT_SEED_B[17]	1
Bit 0	R/W	JITT_SEED_B[16]	1

JITT_SEED_B[31:16]

Contains bits 31 down to 16 of the 58 bit pseudo random jitter test pattern seed B.

NOTE: These bits can only be written when jitter pattern generation is turned off, i.e. JITT_PAT_EN is written low.

Downloaded by Content Team of Partminer.com on Wednesday, 07 February, 2007 06:59:32 PM

Register 0x308CH: Jitter Test Seed B 0

Bit	Type	Function	Default
Bit 15	R/W	JITT_SEED_B[15]	1
Bit 14	R/W	JITT_SEED_B[14]	1
Bit 13	R/W	JITT_SEED_B[13]	1
Bit 12	R/W	JITT_SEED_B[12]	1
Bit 11	R/W	JITT_SEED_B[11]	1
Bit 10	R/W	JITT_SEED_B[10]	1
Bit 9	R/W	JITT_SEED_B[9]	1
Bit 8	R/W	JITT_SEED_B[8]	1
Bit 7	R/W	JITT_SEED_B[7]	1
Bit 6	R/W	JITT_SEED_B[6]	1
Bit 5	R/W	JITT_SEED_B[5]	1
Bit 4	R/W	JITT_SEED_B[4]	1
Bit 3	R/W	JITT_SEED_B[3]	1
Bit 2	R/W	JITT_SEED_B[2]	1
Bit 1	R/W	JITT_SEED_B[1]	1
Bit 0	R/W	JITT_SEED_B[0]	1

JITT_SEED_B[15:0]

Contains bits 15 down to 0 of the 58 bit pseudo random jitter test pattern seed B.

NOTE: These bits can only be written when jitter pattern generation is turned off, i.e. JITT_PAT_EN is written low.

Downloaded by Content Team of Partminer.com on Wednesday, 07 February, 2007 06:59:32 PM

12.33 Egress Flexible FIFO (EFLX)

Register 3200H: EFLX ERCU Global Configuration

Bit	Type	Function	Default
Bit 15	R/W	ERCU_EN	0
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	EDSWT_EN	0
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

ERCU_EN

The ERCU_EN bit must be set before the ERCU block will begin normal operation. Clearing this bit causes the entire ERCU block to freeze and stop processing requests from either the write data path or the system bus controller. The TOP_CHAN[3:0] bits (Register 0002H: S/UNI 9953 System-side Configuration) and SSMODE[1:0] bits (Register 0001H: S/UNI 9953 Master Reset and Configuration) should be modified only when ERCU_EN is low.

EDSWT_EN

The EDSWT_EN bit must be set before the EDSWT block will begin normal operation. Clearing this bit causes the entire EDSWT block to freeze. The TOP_CHAN[3:0] bits (Register 0002H: S/UNI 9953 System-side Configuration) and SSMODE[1:0] bits (Register 0001H: S/UNI 9953 Master Reset and Configuration) should be modified only when ERCU_EN is low. This bit is intended solely for diagnostic purposes.

Downloaded by Connection of Participants on Wednesday, 07 February, 2007, 06:59:32 PM

Register 3201H: EFLX ERCU Global Status

Bit	Type	Function	Default
Bit 15	R	Reserved	X
Bit 14	R	Reserved	X
Bit 13	R	OVF_ERR	X
Bit 12	R	Reserved	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

OVF_ERR

When OVR_ERR is asserted, one of the address register and FIFO flag units detected an overflow (i.e., a write to a FIFO that could not be performed because the FIFO was completely full). This bit serves as a global error indication for all the logical FIFOs, signaling that the host must read the FIFO Overflow Error Indication Register to determine which channel suffered the error. The OVF_ERR*[n]* status bit is cleared when the offending channel status is read.

Downloaded by Content Team of Partminer on Wednesday, 07 February 2007 06:09:32 PM

Register 3202H: EFLX Indirect Channel Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	1
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	CHAN [1]	0
Bit 0	R/W	CHAN [0]	0

CHAN[1:0]

The CHAN[1:0] extends registers 3203H – 3207H across all possible channels used, up to 4 active channels. The value of CHAN[1:0] will be used when reading or writing to these registers to configure or get status on the current selected channel. A write should be performed to this register before any access to the aforementioned registers to ensure data is correctly interpreted.

Reserved

These register bits are reserved for PMC debug purposes only, and must be left in their default setting for proper operation of the S/UNI 9953.

RWB

The read/write bar (RWB) bit selects between an update operation (write) and a query operation (read). Writing logic 0 to RWB triggers the update operation of the channel specified by CHAN[1:0] with the information in Registers 3203H – 3207H. Writing a logic 1 to RWB triggers a query of the channel specified by CHAN[1:0] and the information is placed in all of the Indirect Registers.

Downloaded by Content Team of Chartminer at Wednesday, 07 February 2007 06:09:32 PM

BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set high when a write to the Indirect Channel Select register triggers an indirect access and will stay high until the access is complete. This register should be polled to determine when data from an indirect read operation is available in all the Indirect Data registers or to determine when a new indirect write operation may commence.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:58:32 PM

Register 3203H: EFLX Indirect Logical FIFO Low Limit and Provision

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	LOLIM[6]	0
Bit 5	R/W	LOLIM[5]	0
Bit 4	R/W	LOLIM[4]	0
Bit 3	R/W	LOLIM[3]	0
Bit 2	R/W	LOLIM[2]	0
Bit 1	R/W	LOLIM[1]	0
Bit 0	R/W	LOLIM[0]	0

LOLIM[6:0]

The lower address boundary of the ring buffer for the logical FIFO referenced by the Indirect Channel Address Register is given by this field. The address value specified is also in units of 256 bytes, and must point to the first byte of the first location in the RAM that belongs to a given FIFO. For example, to set up a logical FIFO with 4096 bytes of space lying between locations 256 and 511 128-bit words (inclusive) in the RAM, the LOLIM[6:0] field must be set to 16 decimal.

To be more precise, due to additional internal caching within the EFLX, the actual FIFO size in bytes is represented by the formula:

FIFO_SIZE = 256*(HILIM-LOLIM) – 16

Thus in the example above, the FIFO size would be 4080 bytes.

Downloaded by Content Team of Parmiter on Wednesday, 07 February 2007 06:09:32 PM

Register 3204H: EFLX Indirect Logical FIFO High Limit

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	HILIM[6]	0
Bit 5	R/W	HILIM[5]	0
Bit 4	R/W	HILIM[4]	0
Bit 3	R/W	HILIM[3]	0
Bit 2	R/W	HILIM[2]	0
Bit 1	R/W	HILIM[1]	0
Bit 0	R/W	HILIM[0]	0

HILIM[6:0]

The upper address boundary, in units of 256 bytes, of the ring buffer for the logical FIFO specified in the Indirect Channel Address Register is given by this field. HILIM[6:0] must point to the first byte *after* the last RAM location for the given FIFO. For example, to set up a logical FIFO with 4096 bytes of space lying between locations 256 and 511 128-bit words (inclusive) in the RAM, the HILIM[6:0] field must be set to 32 decimal.

To be more precise, due to additional internal caching within the EFLX, the actual FIFO size in bytes is represented by the formula:

FIFO_SIZE = 256*(HILIM-LOLIM) – 16

Thus in the example above, the FIFO size would be 4080 bytes.

As the physical size of the EFLX RAM is 20,480 bytes, the maximum value of HILIM[6:0] would be 80 decimal. This would typically be for the single channel case.

Downloaded by Content Team of Partinic on Wednesday, 07 February 2007 06:09:32 PM

Register 3205H: EFLX Indirect Full/Almost-Full Status and Limit

Bit	Type	Function	Default
Bit 15	R	FULL	X
Bit 14	R	AFULL	X
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved AFTH[11]	0
Bit 10	R/W	AFTH [10]	0
Bit 9	R/W	AFTH [9]	0
Bit 8	R/W	AFTH [8]	0
Bit 7	R/W	AFTH [7]	0
Bit 6	R/W	AFTH [6]	0
Bit 5	R/W	AFTH [5]	0
Bit 4	R/W	AFTH [4]	0
Bit 3	R/W	AFTH [3]	0
Bit 2	R/W	AFTH [2]	0
Bit 1	R/W	AFTH [1]	0
Bit 0	R/W	AFTH [0]	0

AFTH [10:0]

The AFTH [10:0] field holds the threshold, in terms number of 128-bit words currently present in the logical FIFO referenced by Indirect Channel Address Register, before an almost-full status is reported. AFTH [10:0] should be written at initialization time (ERCUEN = '0') with the total number of words allocated to the logical FIFO, minus the required amount for the round trip latency to the system bus controller. It is not changed by the ERCU. The minimum value of AFTH[10:0] is 13 decimal.

Due to additional internal caching within the EFLX , the AFTH value used for transition from HUNGRY to SATISFIED state is the value in the AFTH register value minus 13.

AFULL

The almost full status bit (AFULL) is set when the number of words within the logical FIFO is greater than the AFTH[10:0] value. This status information is provided for diagnostic purposes.

FULL

The full status bit (FULL) is set when the logical FIFO is reporting a full status to the upstream write data path. This status information is provided for diagnostic purposes.

Downloaded by Content Team of Parmir on Wednesday, 07 February 2007 06:09:32 PM

Register 3206H: EFLX Indirect Empty/Almost-Empty Status and Limit

Bit	Type	Function	Default
Bit 15	R	EMPTY	X
Bit 14	R	AEMPTY	X
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	AETH [10]	0
Bit 9	R/W	AETH [9]	0
Bit 8	R/W	AETH [8]	0
Bit 7	R/W	AETH [7]	0
Bit 6	R/W	AETH [6]	0
Bit 5	R/W	AETH [5]	0
Bit 4	R/W	AETH [4]	0
Bit 3	R/W	AETH [3]	0
Bit 2	R/W	AETH [2]	0
Bit 1	R/W	AETH [1]	0
Bit 0	R/W	AETH [0]	0

AETH [10:0]

The AETH [10:0] field holds the threshold, in terms number of 128-bit words currently present in the logical FIFO referenced by Indirect Channel Address Register, before an almost-empty status is reported. AETH [10:0] should be written at initialization time (ERCUEN = '0') with a value greater than 12 decimal, but less than the total number of words allocated to the logical FIFO. It is not changed by the ERCU.

Due to additional internal caching within the EFLX, the AETH value used for transition from HUNGRY to STARVING state is the value in the AETH register value minus 12.

AEMPTY

The almost empty status bit (AEMPTY) is set when the number of words within the logical FIFO is less than or equal to the AETH[10:0] value. This status information is provided for diagnostic purposes.

EMPTY

The empty status bit (EMPTY) is set whenever the logical FIFO is completely empty. This flag is provided for diagnostic purposes.

Downloaded by Content Team of Parwinder on Wednesday, 07 February 2007 06:09:32 PM

Register 3207H: EFLX Indirect FIFO Cut-Through Threshold

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	CUT_THRU [10]	0
Bit 9	R/W	CUT_THRU [9]	0
Bit 8	R/W	CUT_THRU [8]	0
Bit 7	R/W	CUT_THRU [7]	0
Bit 6	R/W	CUT_THRU [6]	0
Bit 5	R/W	CUT_THRU [5]	0
Bit 4	R/W	CUT_THRU [4]	0
Bit 3	R/W	CUT_THRU [3]	0
Bit 2	R/W	CUT_THRU [2]	0
Bit 1	R/W	CUT_THRU [1]	0
Bit 0	R/W	CUT_THRU [0]	0

CUT_THRU [10:0]

The CUT_THRU [10:0] field holds the threshold, in terms of the number of 128-bit words currently present in the logical FIFO referenced by Indirect Channel Address Register, before a frame is released. It should be written at initialization time (ERCU_EN = '0' or PROV[*n*] = '1') with the total number of words of a given frame that should be written for a given logical FIFO before reads are issued on the line side to minimize the probability of an underflow situation. It is not changed by the ERCU. The minimum value of CUT_THRU[10:0] is 13 decimal.

Due to additional internal caching within the EFLX, the actual point of cut through is the CUT_THRU register value minus 12.

Downloaded by Content Team of Purchase Dept on Wednesday, 07 February 2007 06:09:32 PM

Register 3208H: EFLX FIFO SOF Error Enable

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 06:09:32 PM

Register 3209H: EFLX FIFO SOF Error Indication

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 06:09:32 PM

Register 320AH: EFLX FIFO EOF Error Enable

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 06:09:32 PM

Register 320BH: EFLX FIFO EOF Error Indication

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 06:09:32 PM

Register 320CH: EFLX FIFO Overflow Error Enable

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	OVFE[3]	0
Bit 2	R/W	OVFE[2]	0
Bit 1	R/W	OVFE[1]	0
Bit 0	R/W	OVFE[0]	0

OVFE[3:0]

The overflow interrupt enable controls the assertion of the INTB output when OVFI*[n]* is high on any given channel. When OVFE*[n]* is set high, an interrupt is generated upon assertion event of the OVFI*[n]* register. When OVFE*[n]* is set low, changes in the OVFI*[n]* status do not generate an interrupt.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:59:32 PM

Register 320DH: EFLX FIFO Overflow Error Indication

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R	OVFI[3]	X
Bit 2	R	OVFI[2]	X
Bit 1	R	OVFI[1]	X
Bit 0	R	OVFI[0]	X

If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, these interrupt status bits are cleared on write with a logic 1. Otherwise, these interrupt status bits are cleared on read.

OVFI[3:0]

The OVFI*[n]* interrupt flag is set whenever an overflow (i.e., an attempted write to a completely full FIFO) is detected on the referenced logical FIFO. The OVFI*[n]* register bit is cleared immediately after it is read (WCIMODE = '0') or written (WCIMODE = '1'), thus acknowledging the event has been recorded.

Downloaded by Content Team of Parts-IC Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 320EH: EFLX Invalid Channel Error Enable

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	INVCHANE[3]	0
Bit 2	R/W	INVCHANE[2]	0
Bit 1	R/W	INVCHANE[1]	0
Bit 0	R/W	INVCHANE[0]	0

INVCHANE[3:0]

The invalid channel interrupt enable controls the assertion of the INTB output when INVCHANI*[n]* is high on any given channel. When INVCHANE*[n]* is set high, an interrupt is generated upon assertion event of the INVCHANI*[n]* register. When INVCHANE*[n]* is set low, changes in the INVCHANI*[n]* status do not generate an interrupt.

Downloaded by Content Team of Partminer on Wednesday, 07 February, 2007 06:59:32 PM

Register 320FH: EFLX Invalid Channel Error Indication

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R	INVCHANI[3]	X
Bit 2	R	INVCHANI[2]	X
Bit 1	R	INVCHANI[1]	X
Bit 0	R	INVCHANI[0]	X

If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, these interrupt status bits are cleared on write with a logic 1. Otherwise, these interrupt status bits are cleared on read.

INVCHANI[3:0]

The INVCHANI*[n]* interrupt flag is set whenever an attempt was made by the system bus controller to write to an unprovisioned channel (as determined by the TOP_CHAN[3:0] bits in the S/UNI 9953 System-side Configuration Register (Register 0002H). The INVCHANI*[n]* register bit is cleared immediately after it is read (WCIMODE=’0’) or (WCIMODE = ‘1’), thus acknowledging the event has been recorded.

Downloaded by Content Team of PMC-Sierra Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 3210H: EFLX Channel Provision

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	PROV [3]	0
Bit 2	R/W	PROV [2]	0
Bit 1	R/W	PROV [1]	0
Bit 0	R/W	PROV [0]	0

PROV[3:0]

The channel provision (PROV[3:0]) bits specify the active status of the channels being accessed. When PROV[n] is asserted high, channel[n] is active. When PROV[n] is asserted low, channel[n] is inactive and is not used. The PROV[3:0] bits are used for enabling and disabling available channels within the EFLX, as well as to initialize the data and tag RAM read/write addresses. A transition from channel[n] being active (PROV[n] is logic 1) to inactive (PROV[n] is logic 0) will reset the associated rate adaptation buffer and freeze the associated logical FIFO. A transition from channel[n] being inactive (PROV[n] is logic 0) to active (PROV[n] is logic 1) will latch in the LOLIM[6:0], HILIM[6:0], AFTH[10:0], AETH[10:0] and CUT_THRU[10:0] to the associated logical FIFO and begin to process data independent of other provisioned channels.

Note that is is recommended to reset or reprovision any downstream blocks (eg TCFP or TCFP-9953) after re-provisioning the EFLX, to avoid initial spurious data from being transmitted.

Downloaded by Content Team on Wednesday, 07 February, 2007 06:59:32 PM

12.34 PL4 Input Data Unpacker (PL4IDU)

Register 3280H: PL4IDU Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	1
Bit 1	R/W	EN_PORTS	0
Bit 0	R/W	EN_DFWD	0

EN_DFWD

Enable Data Forward. This bit is used to allow PL4 data words to be forwarded to the output FIFO interface: it is used as a simple qualifier on the CMDWE term of the output FIFO interface. When '1', data will be forwarded. When '0', CMDWE will not be asserted. The assertion and deassertion of this signal is not synchronized to a given port state, so modifying this register bit during packet data reception can result in partial packets to be written to the output FIFO interface. Port Statistics are incremented only if EN_DFWD is a '1'.

EN_PORTS

Enable Port State machine. This bit is used to allow PL4 data words to be forwarded to the output FIFO interface: it is used as a simple global qualifier to allow the per-channel Port State to leave the Port INACTIVE state. When '1', the Port State can transition out of Port INACTIVE. When '0', the Port State on a per-channel basis will not transition out of Port INACTIVE. Modifying this register bit during packet data reception will not result in partial packets to be written to the output FIFO interface. Port Statistics are incremented based on the per-channel Port state being either Port ACTIVE or Port PAUSED; hence the assertion and deassertion of EN_PORTS affects the port statistics only at packet boundaries.

Downloaded by Conexant Cam of Radiyalabs on Wednesday, 07 February, 2007 06:59:32 PM

Register 3282H: PL4IDU Interrupt Mask

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	DIP4E	0
Bit 0	R/W	Reserved	0

DIP4E

The DIP4E bit enables the generation of an interrupt due to a DIP4 check error on a PL4 control word. The DIP4 checking is only done if the primary input signal IND_VALID is asserted on the PL4 input interface.

Reserved

These register bits are reserved for PMC debug purposes only, and must be left in their default setting for proper operation of the S/UNI 9953.

Downloaded by Content Team of Pbminer Nicon Wednesday, 07 February, 2007 06:59:32 PM

Register 3283H: PL4IDU Interrupt

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	DIP4I	X
Bit 0	R	Reserved	X

If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, these interrupt status bits are cleared on write with a logic 1. Otherwise, these interrupt status bits are cleared on read as per register bit description.

DIP4I

The DIP4I bit will be set when there is a DIP4 check error. The DIP4 checking is only done if the primary input signal IND_VALID is asserted on the PL4 input interface. If DIP4E is '1' in the PL4IDU Interrupt Mask register, an interrupt will also be generated (INTB output asserted).

Reserved

These register bits are reserved for PMC debug purposes only, and must be left in their default setting for proper operation of the S/UNI 9953.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

12.35 Egress FIFO RAM (ERAM)

Register 3400H: ERAM Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R	TAG_PERRI	X
Bit 3	R	DATA_PERRI[3]	X
Bit 2	R	DATA_PERRI[2]	X
Bit 1	R	DATA_PERRI[1]	X
Bit 0	R	DATA_PERRI[0]	X

This register and its corresponding interrupt enable register, may be used to optionally identify any parity errors that have occurred within the FIFO RAM. This feature would normally be used for diagnostic purposes. If using this feature, the interrupts should only be enabled after data has first been flushed through the FIFO, otherwise false parity interrupts will be generated due to the uninitialized RAM.

If the WCIMODE bit in the S/UNI 9953 Master Reset and Configuration Register (Register 0001H) is set high, these interrupt status bits are cleared on write with a logic 1. Otherwise, these interrupt status bits are cleared on read as per register bit description.

DATA_PERRI[3:0]

The Data Parity Error Interrupt indicates a parity error occurred during a data RAM read. The bit asserted indicates which part of the data word contained the parity error:

Bit	Bit Range
Bit 3	127:96
Bit 2	95:64
Bit 1	63:32
Bit 0	31:0

Downloaded by Company Item of Partner Site at Wednesday, 07 February, 2007 06:59:32 PM

TAG_PERRI

The Tag Parity Error Interrupt indicates a parity error occurred during a tag RAM read.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 3401H: ERAM Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R/W	TAG_PERRE	0
Bit 3	R/W	DATA_PERRE[3]	0
Bit 2	R/W	DATA_PERRE[2]	0
Bit 1	R/W	DATA_PERRE[1]	0
Bit 0	R/W	DATA_PERRE[0]	0

DATA_PERRE[3:0]

The Data Parity Error Interrupt Enable is set to enable the assertion of the interrupt when the corresponding DATA_PERRI bit is asserted.

TAG_PERRE

The Tag Parity Error Interrupt Enable is set to enable the assertion of the interrupt when the TAG_PERRI bit is asserted.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

12.36 Line Side PRBS Generator/Monitor (RLMPGM, TLMPGM)

Register 0n28H: S/UNI 9953 Receive Line MPGM Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R/W	MPGM_EN_REG	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

MPGM_EN_REG

The MPGM Enable Register (MPGM_EN_REG) bit is used to enable/disable the MPGM. When the MPGM_EN_REG bit is set to high the MPGM is enabled and when it is low, it is disabled.

Downloaded by Content Team of Partminer, Inc. on Wednesday, 07 February, 2007 06:39:32 PM

Note that each of the 16 registers (0x0n28) defined by "n", where n = 0 to F, maps to the receive line interface pins (RXDATA) according to the following for the given value of n:

0 : RXDATA4[3]
1 : RXDATA4[2]
2 : RXDATA4[1]
3 : RXDATA4[0]
4 : RXDATA3[3]
5 : RXDATA3[2]
6 : RXDATA3[1]
7 : RXDATA3[0]
8 : RXDATA2[3]
9 : RXDATA2[2]
A : RXDATA2[1]
B : RXDATA2[0]
C : RXDATA1[3]
D : RXDATA1[2]
E : RXDATA1[1]
F : RXDATA1[0]

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0n29H: S/UNI 9953 Receive Line MPGM Monitor Sync

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R	OOLV	X
Bit 2	R/W	OOLE	0
Bit 1	R	LOCKI	X
Bit 0	R	OOLI	X

Note: The clear mode of the interrupts OOLI and LOCKI depends on the WCIMODE input value. When WCIMODE is zero, the interrupts are cleared when it is read. When WCIMODE is one, the interrupts are cleared only if logic one is being written to it.

OOLI

The Out of Lock Interrupt (OOLI) indicates when the state machine goes from Lock to Out Of Lock State. Whenever the state machine goes from Lock to Out Of Lock State OOLI is set high. This bit is independent of OOLE.

LOCKI

The Lock Interrupt (LOCKI) indicates when the state machine goes from Out Of Lock to Lock State. Whenever the state machine goes from Out Of Lock to Lock State LOCKI is set high. This bit is independent of OOLE.

OOLE

The Out Of Lock interrupt Enable (OOLE) bit allows the monitor synchronization interrupt to generate an external interrupt on INT. When OOLE is set high, whenever the monitor goes into Out of Lock State or Lock State an interrupt is generated on INT.

Downloaded by Content Team of Partner1 Inc on Wednesday, 07 February, 2007 06:39:32 PM

OOLV

The Out of Lock Status (OOLV) reflects the state of the monitor's state machine. When OOLV is set high, the monitor's state machine is in the Out of Locked State. When OOLV is low, the monitor is in Lock State.

Note that each of the 16 registers (0x0n29) defined by "n", where n = 0 to F, maps to the receive line interface pins (RXDATA) according to the following for the given value of n:

0 : RXDATA4[3]
1 : RXDATA4[2]
2 : RXDATA4[1]
3 : RXDATA4[0]
4 : RXDATA3[3]
5 : RXDATA3[2]
6 : RXDATA3[1]
7 : RXDATA3[0]
8 : RXDATA2[3]
9 : RXDATA2[2]
A : RXDATA2[1]
B : RXDATA2[0]
C : RXDATA1[3]
D : RXDATA1[2]
E : RXDATA1[1]
F : RXDATA1[0]

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 @ 09:59:32 AM

Register 1n28H: S/UNI 9953 Transmit Line MPGM Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R/W	MPGM_EN_REG	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

MPGM_EN_REG

The MPGM Enable Register (MPGM_EN_REG) bit is used to enable/disable the MPGM. When the MPGM_EN_REG bit is set to high the MPGM is enabled and when it is low, it is disabled.

Note that each of the 16 registers (0x1n28) defined by "n", where n = 0 to F, maps to the transmit line interface pins (TXDATA) according to the following for the given value of n:

0 : TXDATA4[3]
1 : TXDATA4[2]
2 : TXDATA4[1]
3 : TXDATA4[0]
4 : TXDATA3[3]
5 : TXDATA3[2]
6 : TXDATA3[1]
7 : TXDATA3[0]
8 : TXDATA2[3]
9 : TXDATA2[2]
A : TXDATA2[1]
B : TXDATA2[0]
C : TXDATA1[3]
D : TXDATA1[2]
E : TXDATA1[1]
F : TXDATA1[0]

Downloaded by Cornell University, Department of Inc on Wednesday, 07 February, 2007 06:39:32 PM

12.37 APS Port PRBS Generator/Monitor (IAMPGM, OAMPGM)

Register 0nA8H: S/UNI 9953 Input APS MPGM Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R/W	MPGM_EN_REG	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

MPGM_EN_REG

The MPGM Enable Register (MPGM_EN_REG) bit is used to enable/disable the MPGM. When the MPGM_EN_REG bit is set to high the MPGM is enabled and when it is low, it is disabled.

Downloaded by Content Team of Partminer, Inc. on Wednesday, 07 February, 2007 06:39:32 PM

Note that each of the 16 registers (0x0nA8) defined by "n", where n = 0 to F, maps to the input APS interface pins (IAPS) according to the following for the given value of n:

0 : IAPS1[0]
1 : IAPS1[1]
2 : IAPS1[2]
3 : IAPS1[3]
4 : IAPS2[0]
5 : IAPS2[1]
6 : IAPS2[2]
7 : IAPS2[3]
8 : IAPS3[0]
9 : IAPS3[1]
A : IAPS3[2]
B : IAPS3[3]
C : IAPS4[0]
D : IAPS4[1]
E : IAPS4[2]
F : IAPS4[3]

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Register 0nA9H: S/UNI 9953 Input APS MPGM Monitor Sync

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R	OOLV	X
Bit 2	R/W	OOLE	0
Bit 1	R	LOCKI	X
Bit 0	R	OOLI	X

Note: The clear mode of the interrupts OOLI and LOCKI depends on the WCIMODE input value. When WCIMODE is zero, the interrupts are cleared when it is read. When WCIMODE is one, the interrupts are cleared only if logic one is being written to it.

OOLI

The Out of Lock Interrupt (OOLI) indicates when the state machine goes from Lock to Out Of Lock State. Whenever the state machine goes from Lock to Out Of Lock State OOLI is set high. This bit is independent of OOLE.

LOCKI

The Lock Interrupt (LOCKI) indicates when the state machine goes from Out Of Lock to Lock State. Whenever the state machine goes from Out Of Lock to Lock State LOCKI is set high. This bit is independent of OOLE.

OOLE

The Out Of Lock interrupt Enable (OOLE) bit allows the monitor synchronization interrupt to generate an external interrupt on INT. When OOLE is set high, whenever the monitor goes into Out of Lock State or Lock State an interrupt is generated on INT.

Downloaded by Content Team of Partner1 Inc on Wednesday, 07 February, 2007 06:39:32 PM

OOLV

The Out of Lock Status (OOLV) reflects the state of the monitor's state machine. When OOLV is set high, the monitor's state machine is in the Out of Locked State. When OOLV is low, the monitor is in Lock State.

Note that each of the 16 registers (0x0nA9) defined by "n", where n = 0 to F, maps to the input APS interface pins (IAPS) according to the following for the given value of n:

0 : IAPS1[0]
1 : IAPS1[1]
2 : IAPS1[2]
3 : IAPS1[3]
4 : IAPS2[0]
5 : IAPS2[1]
6 : IAPS2[2]
7 : IAPS2[3]
8 : IAPS3[0]
9 : IAPS3[1]
A : IAPS3[2]
B : IAPS3[3]
C : IAPS4[0]
D : IAPS4[1]
E : IAPS4[2]
F : IAPS4[3]

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 @ 09:59:32 AM

Register 1nA8H: S/UNI 9953 Output APS MPGM Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R/W	MPGM_EN_REG	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

MPGM_EN_REG

The MPGM Enable Register (MPGM_EN_REG) bit is used to enable/disable the MPGM. When the MPGM_EN_REG bit is set to high the MPGM is enabled and when it is low, it is disabled.

Note that each of the 16 registers (0x1nA8) defined by “n”, where n = 0 to F, maps to the output APS interface pins (OAPS) according to the following for the given value of n:

0 : OAPS1[0]
1 : OAPS1[1]
2 : OAPS1[2]
3 : OAPS1[3]
4 : OAPS2[0]
5 : OAPS2[1]
6 : OAPS2[2]
7 : OAPS2[3]
8 : OAPS3[0]
9 : OAPS3[1]
A : OAPS3[2]
B : OAPS3[3]
C : OAPS4[0]
D : OAPS4[1]
E : OAPS4[2]
F : OAPS4[3]

Downloaded by Conexant Systems Partmiss Inc on Wednesday, 07 February, 2007 06:39:32 PM

13 Test Features Description

Simultaneously asserting (low) the CSB, RDB and WRB inputs causes all digital output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the S/UNI 9953. Test mode registers (as opposed to normal mode registers) are selected when TRS (A[14]) is high.

Test mode registers may also be used for board testing. When all of the TSBs within the S/UNI 9953 are placed in test mode 0, digital device inputs may be read and digital device outputs may be forced via the microprocessor interface.

Test registers are normally not required to be accessed from a customer level.

In addition, the S/UNI 9953 also supports a standard IEEE 1149.1 five-signal JTAG boundary scan test port for use in board testing. All digital device inputs may be read and all digital device outputs may be forced via the JTAG test port.

Table 32 Test Mode Register Memory Map

Address	Register
0000H-3FFFH	Normal Mode Registers
4000	Master Test Register
4001	Test Mode Address Force Enable
4002	Test Mode Address Force Value
4003	Line / System Analog Test
4004	VCLK SONET Test Clock Select
4005	VCLK PL4 Test Clock Select
4006	ROHI Control Test Points
4007	ROHI Observe Test Points
4008	TOHI Control Test Points
4009	TOHI Observe Test Points
400AH-7FFFH	Reserved For Test

13.1 Master Test and Test Configuration Registers

Notes on Test Mode Register Bits

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.

2. Writeable test mode register bits are not initialized upon reset unless otherwise noted.

Downloaded by Content Team of Pa... on Wednesday, 07 February 2007 06:59:12 PM

Register 4000H: S/UNI 9953 Master Test

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R/W	Reserved	X
Bit 5	R/W	PMCATST	X
Bit 4	R/W	PMCTST	X
Bit 3	R/W	DBCTRL	0
Bit 2	R/W	IOTST	0
Bit 1	R/W	HIZDATA	0
Bit 0	R/W	HIZIO	0

This register is used to enable S/UNI 9953 test features. All bits, except PMCTST and PMCATST are reset to zero by a reset of the S/UNI 9953 using the RSTB input. PMCTST and PMCATST are reset when CSB is logic 1. PMCTST, and PMCATST can also be reset by writing a logic 0 to the corresponding register bit.

Both PMCATST and PMCTST (bit 4 and 5) in this register must be set to high for analog test.

Access to this register is not affected by the Test Mode Address Force functions in registers 4001H and 4002H.

HIZIO, HIZDATA

The HIZIO and HIZDATA bits control the tri-state modes of the S/UNI 9953. While the HIZIO bit is a logic one, all digital output pins of the S/UNI 9953 except the data bus and output TDO are held tri-state. The microprocessor interface is still active. While the HIZDATA bit is a logic one, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles. The HIZDATA bit is overridden by the DBCTRL bit.

IOTST

The IOTST bit is used to allow normal microprocessor access to the top-level test registers and control or observe the top-level digital device inputs/outputs for board level testing. When IOTST is a logic 1, all digital device inputs/outputs can be observed/controlled via test registers.

Downloaded by Content Part of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

DBCTRL

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic one and IOTST is set to logic one, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the S/UNI 9953 to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

PMCTST

The PMCTST bit is used to configure the S/UNI 9953 for PMC's manufacturing tests. When PMCTST is set to logic one, the S/UNI 9953 microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors. The PMCTST can be cleared by setting CSB to logic one or by writing logic zero to the bit.

Both PMCATST and PMCTST (bit 4 and 5) in this register must be set to high for analog test.

PMCATST

The PMCATST bit is used to configure the analog portion of the S/UNI 9953 for PMC's manufacturing tests. The PMCATST can be cleared by setting CSB to logic one or by writing logic zero to the bit.

Both PMCATST and PMCTST (bit 4 and 5) in this register must be set to high for analog test.

Reserved

The reserved bit should be set to logic 0 for normal tests. They have no effect on the operation of the device when PMCTST is logic 0.

Downloaded by Content Team of Pacdriver Inc on Wednesday, 07 February 2007 06:52:32 PM

Register 400AH – 7FFFH: S/UNI 9953 Reserved for Test

Bit	Type	Function	Default
Bit 15	R	Reserved	X
Bit 14	R	Reserved	X
Bit 13	R	Reserved	X
Bit 12	R	Reserved	X
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

These registers are Reserved for future enhancements.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

13.2 JTAG Test Port

The S/UNI 9953 JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more generic details on the JTAG port, please refer to the Application Note, PMC-2021518, "JTAG Test Features Description".

Table 33 Instruction Register (Length - 3 bits)

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Table 34 Identification Register

Length	32 bits
Version Number	0H (for Rev A, 1H for Rev B, 2H for Rev C)
Part Number	5390H
Manufacturer's Identification Code	0CDH
Device Identification (Revision A)	053900CDH
Device Identification (Revision B)	153900CDH
Device Identification (Revision C)	253900CDH

Note that the first 4 bits scanned out of the JTAG Boundary Register detailed below represent the 4-bit Revision ID, and thus will vary depending on the device revision, as indicated in the Identification Register above.

Downloaded by Content Team of Element14 INC on Wednesday, 07 February 2007 08:53:17 PM

Table 35 Boundary Scan Register (RevC)

Name	Register Bit	Cell Type	Device ID
ALE	376	IN_CELL	L
CSB	375	IN_CELL	L
RDB	374	IN_CELL	H
WRB	373	IN_CELL	L
OEB_INTB	372	OUT_CELL	L
INTB	371	OUT_CELL	H
RSTB	370	IN_CELL	L
OEB_D[12]	369	OUT_CELL	H
D[12]	368	IO_CELL	L
OEB_D[13]	367	OUT_CELL	L
D[13]	366	IO_CELL	H
OEB_D[14]	365	OUT_CELL	H
D[14]	364	IO_CELL	H
OEB_D[15]	363	OUT_CELL	L
D[15]	362	IO_CELL	L
OEB_D[8]	361	OUT_CELL	H
D[8]	360	IO_CELL	L
OEB_D[9]	359	OUT_CELL	L
D[9]	358	IO_CELL	L
OEB_D[10]	357	OUT_CELL	L
D[10]	356	IO_CELL	L
OEB_D[11]	355	OUT_CELL	L
D[11]	354	IO_CELL	L
OEB_D[4]	353	OUT_CELL	L
D[4]	352	IO_CELL	H
OEB_D[5]	351	OUT_CELL	H
D[5]	350	IO_CELL	L
OEB_D[6]	349	OUT_CELL	L
D[6]	348	IO_CELL	H
OEB_D[7]	347	OUT_CELL	H
D[7]	346	IO_CELL	L
OEB_D[0]	345	OUT_CELL	H
D[0]	344	IO_CELL	—
OEB_D[1]	343	OUT_CELL	—
D[1]	342	IO_CELL	—
OEB_D[2]	341	OUT_CELL	—
D[2]	340	IO_CELL	—
OEB_D[3]	339	OUT_CELL	—
D[3]	338	IO_CELL	—

Downloaded by Intel Team of Partnineers on Wednesday, February 21, 2007 06:59:32 PM

Name	Register Bit	Cell Type	Device ID
A[12]	337	IN_CELL	—
A[13]	336	IN_CELL	—
A[14]	335	IN_CELL	—
A[8]	334	IN_CELL	—
A[9]	333	IN_CELL	—
A[10]	332	IN_CELL	—
A[11]	331	IN_CELL	—
A[4]	330	IN_CELL	—
A[5]	329	IN_CELL	—
A[6]	328	IN_CELL	—
A[7]	327	IN_CELL	—
A[0]	326	IN_CELL	—
A[1]	325	IN_CELL	—
A[2]	324	IN_CELL	—
A[3]	323	IN_CELL	—
BTEST	322	IN_CELL	—
QUAD2488	321	IN_CELL	—
LAN	320	IN_CELL	—
OEB_PAUSED	319	OUT_CELL	—
PAUSED	318	OUT_CELL	—
PAUSE	317	IN_CELL	—
REFSEL[0]	316	IN_CELL	—
REFSEL[1]	315	IN_CELL	—
RSTAT[0]	314	IN_CELL	—
RSTAT[1]	313	IN_CELL	—
RSCLK	312	IN_CELL	—
REFCLK	311	IN_CELL	—
TDAT[0]	310	IN_CELL	—
TDAT[2]	309	IN_CELL	—
TDAT[4]	308	IN_CELL	—
TDAT[6]	307	IN_CELL	—
TDAT[8]	306	IN_CELL	—
TDAT[9]	305	IN_CELL	—
TDAT[11]	304	IN_CELL	—
TDAT[13]	303	IN_CELL	—
TDAT[15]	302	IN_CELL	—
TDAT[1]	301	IN_CELL	—
TDAT[3]	300	IN_CELL	—
TDAT[5]	299	IN_CELL	—
TDAT[7]	298	IN_CELL	—

Downloaded by [illegible] Team of Partminer Inc. on Wednesday, February 21, 2007 06:59:32 PM

Name	Register Bit	Cell Type	Device ID
TDCLK	297	IN_CELL	—
TDAT[10]	296	IN_CELL	—
TDAT[12]	295	IN_CELL	—
TDAT[14]	294	IN_CELL	—
TCTL	293	IN_CELL	—
RDAT[1]	292	OUT_CELL	—
RDAT[0]	291	OUT_CELL	—
RDAT[3]	290	OUT_CELL	—
RDAT[2]	289	OUT_CELL	—
RDAT[5]	288	OUT_CELL	—
RDAT[4]	287	OUT_CELL	—
RDAT[7]	286	OUT_CELL	—
RDAT[6]	285	OUT_CELL	—
RCTL	284	OUT_CELL	—
RDAT[8]	283	OUT_CELL	—
RDAT[9]	282	OUT_CELL	—
RDCLK	281	OUT_CELL	—
RDAT[11]	280	OUT_CELL	—
RDAT[10]	279	OUT_CELL	—
RDAT[13]	278	OUT_CELL	—
RDAT[12]	277	OUT_CELL	—
RDAT[15]	276	OUT_CELL	—
RDAT[14]	275	OUT_CELL	—
OEB_TSTAT[0]	274	OUT_CELL	—
TSTAT[0]	273	OUT_CELL	—
OEB_TSTAT[1]	272	OUT_CELL	—
TSTAT[1]	271	OUT_CELL	—
OEB_TSCLK	270	OUT_CELL	—
TSCLK	269	OUT_CELL	—
DTRB	268	IN_CELL	—
OEB_TTOHCLK[1]	267	OUT_CELL	—
TTOHCLK[1]	266	OUT_CELL	—
OEB_TTOHCLK[2]	265	OUT_CELL	—
TTOHCLK[2]	264	OUT_CELL	—
OEB_TTOHCLK[3]	263	OUT_CELL	—
TTOHCLK[3]	262	OUT_CELL	—
OEB_TTOHCLK[4]	261	OUT_CELL	—
TTOHCLK[4]	260	OUT_CELL	—
OEB_TTOHFP[1]	259	OUT_CELL	—
TTOHFP[1]	258	OUT_CELL	—

Downloaded by [illegible] pursuant to License Agreement. No further reproduction or distribution is permitted. Wednesday, February 21, 2007 06:59:32 PM

Name	Register Bit	Cell Type	Device ID
OEB_TTOHFP[2]	257	OUT_CELL	—
TTOHFP[2]	256	OUT_CELL	—
OEB_TTOHFP[3]	255	OUT_CELL	—
TTOHFP[3]	254	OUT_CELL	—
OEB_TTOHFP[4]	253	OUT_CELL	—
TTOHFP[4]	252	OUT_CELL	—
TTOH[1]	251	IN_CELL	—
TTOH[2]	250	IN_CELL	—
TTOH[3]	249	IN_CELL	—
TTOH[4]	248	IN_CELL	—
TTOHEN[1]	247	IN_CELL	—
TTOHEN[2]	246	IN_CELL	—
TTOHEN[3]	245	IN_CELL	—
TTOHEN[4]	244	IN_CELL	—
OEB_TPOHCLK[1]	243	OUT_CELL	—
TPOHCLK[1]	242	OUT_CELL	—
OEB_TPOHCLK[2]	241	OUT_CELL	—
TPOHCLK[2]	240	OUT_CELL	—
OEB_TPOHCLK[3]	239	OUT_CELL	—
TPOHCLK[3]	238	OUT_CELL	—
OEB_TPOHCLK[4]	237	OUT_CELL	—
TPOHCLK[4]	236	OUT_CELL	—
OEB_TPOHFP[1]	235	OUT_CELL	—
TPOHFP[1]	234	OUT_CELL	—
OEB_TPOHFP[2]	233	OUT_CELL	—
TPOHFP[2]	232	OUT_CELL	—
OEB_TPOHFP[3]	231	OUT_CELL	—
TPOHFP[3]	230	OUT_CELL	—
OEB_TPOHFP[4]	229	OUT_CELL	—
TPOHFP[4]	228	OUT_CELL	—
TPOH[1]	227	IN_CELL	—
TPOH[2]	226	IN_CELL	—
TPOH[3]	225	IN_CELL	—
TPOH[4]	224	IN_CELL	—
TPOHEN[1]	223	IN_CELL	—
TPOHEN[2]	222	IN_CELL	—
TPOHEN[3]	221	IN_CELL	—
TPOHEN[4]	220	IN_CELL	—
OEB_TPOHRDY[1]	219	OUT_CELL	—
TPOHRDY[1]	218	OUT_CELL	—

Downloaded by [illegible] Team of Partnerships on Wednesday, February 21, 2007 06:59:32 PM

Name	Register Bit	Cell Type	Device ID
OEB_TPOHRDY[2]	217	OUT_CELL	—
TPOHRDY[2]	216	OUT_CELL	—
OEB_TPOHRDY[3]	215	OUT_CELL	—
TPOHRDY[3]	214	OUT_CELL	—
OEB_TPOHRDY[4]	213	OUT_CELL	—
TPOHRDY[4]	212	OUT_CELL	—
OEB_SALM[1]	211	OUT_CELL	—
SALM[1]	210	OUT_CELL	—
OEB_SALM[2]	209	OUT_CELL	—
SALM[2]	208	OUT_CELL	—
OEB_SALM[3]	207	OUT_CELL	—
SALM[3]	206	OUT_CELL	—
OEB_SALM[4]	205	OUT_CELL	—
SALM[4]	204	OUT_CELL	—
OEB_RALM[1]	203	OUT_CELL	—
RALM[1]	202	OUT_CELL	—
OEB_RALM[2]	201	OUT_CELL	—
RALM[2]	200	OUT_CELL	—
OEB_RALM[3]	199	OUT_CELL	—
RALM[3]	198	OUT_CELL	—
OEB_RALM[4]	197	OUT_CELL	—
RALM[4]	196	OUT_CELL	—
OEB_TCLK[1]	195	OUT_CELL	—
TCLK[1]	194	OUT_CELL	—
OEB_TCLK[2]	193	OUT_CELL	—
TCLK[2]	192	OUT_CELL	—
OEB_TCLK[3]	191	OUT_CELL	—
TCLK[3]	190	OUT_CELL	—
OEB_TCLK[4]	189	OUT_CELL	—
TCLK[4]	188	OUT_CELL	—
OEB_PGMTCLK[1]	187	OUT_CELL	—
PGMTCLK[1]	186	OUT_CELL	—
OEB_PGMTCLK[2]	185	OUT_CELL	—
PGMTCLK[2]	184	OUT_CELL	—
OEB_PGMTCLK[3]	183	OUT_CELL	—
PGMTCLK[3]	182	OUT_CELL	—
OEB_PGMTCLK[4]	181	OUT_CELL	—
PGMTCLK[4]	180	OUT_CELL	—
OEB_MDC	179	OUT_CELL	—
MDC	178	OUT_CELL	—

Downloaded by [illegible] on behalf of Partninet SA on Wednesday, 28 February 2007 06:59:32 PM

Name	Register Bit	Cell Type	Device ID
OEB_MDIO	177	OUT_CELL	—
MDIO	176	IO_CELL	—
SYNC_ERR1	175	IN_CELL	—
SYNC_ERR2	174	IN_CELL	—
SYNC_ERR3	173	IN_CELL	—
SYNC_ERR4	172	IN_CELL	—
PHASE_ERR1	171	IN_CELL	—
PHASE_ERR2	170	IN_CELL	—
PHASE_ERR3	169	IN_CELL	—
PHASE_ERR4	168	IN_CELL	—
OEB_PHASE_INIT1	167	OUT_CELL	—
PHASE_INIT1	166	OUT_CELL	—
OEB_PHASE_INIT2	165	OUT_CELL	—
PHASE_INIT2	164	OUT_CELL	—
OEB_PHASE_INIT3	163	OUT_CELL	—
PHASE_INIT3	162	OUT_CELL	—
OEB_PHASE_INIT4	161	OUT_CELL	—
PHASE_INIT4	160	OUT_CELL	—
TXDATA4[3]	159	OUT_CELL	—
TXDATA4[1]	158	OUT_CELL	—
TXDATA4[2]	157	OUT_CELL	—
TXDATA4[0]	156	OUT_CELL	—
TXCLK4	155	OUT_CELL	—
TXCLK_SRC4	154	IN_CELL	—
TXDATA3[3]	153	OUT_CELL	—
TXDATA3[1]	152	OUT_CELL	—
TXDATA3[2]	151	OUT_CELL	—
TXDATA3[0]	150	OUT_CELL	—
TXCLK3	149	OUT_CELL	—
TXCLK_SRC3	148	IN_CELL	—
TXCLK2	147	OUT_CELL	—
TXCLK_SRC2	146	IN_CELL	—
TXDATA2[3]	145	OUT_CELL	—
TXDATA2[1]	144	OUT_CELL	—
TXDATA2[2]	143	OUT_CELL	—
TXDATA2[0]	142	OUT_CELL	—
TXCLK1	141	OUT_CELL	—
TXCLK_SRC1	140	IN_CELL	—
TXDATA1[3]	139	OUT_CELL	—
TXDATA1[1]	138	OUT_CELL	—

Downloaded by [illegible] team of Partminer on Wednesday, February 21, 2007 06:59:32 PM

Name	Register Bit	Cell Type	Device ID
TXDATA1[2]	137	OUT_CELL	—
TXDATA1[0]	136	OUT_CELL	—
RXDATA4[3]	135	IN_CELL	—
RXDATA4[1]	134	IN_CELL	—
RXDATA4[2]	133	IN_CELL	—
RXDATA4[0]	132	IN_CELL	—
RXDATA3[3]	131	IN_CELL	—
RXCLK4	130	IN_CELL	—
RXDATA3[2]	129	IN_CELL	—
RXDATA3[0]	128	IN_CELL	—
RXDATA3[1]	127	IN_CELL	—
RXCLK3	126	IN_CELL	—
RXDATA2[3]	125	IN_CELL	—
RXCLK2	124	IN_CELL	—
RXDATA2[2]	123	IN_CELL	—
RXDATA2[0]	122	IN_CELL	—
RXDATA2[1]	121	IN_CELL	—
RXCLK1	120	IN_CELL	—
RXDATA1[3]	119	IN_CELL	—
RXDATA1[1]	118	IN_CELL	—
RXDATA1[2]	117	IN_CELL	—
RXDATA1[0]	116	IN_CELL	—
IAPS1[1]	115	IN_CELL	—
IAPS1[0]	114	IN_CELL	—
IAPS1[3]	113	IN_CELL	—
IAPS1[2]	112	IN_CELL	—
OAPS1[1]	111	OUT_CELL	—
OAPS1[0]	110	OUT_CELL	—
OAPS1[3]	109	OUT_CELL	—
OAPS1[2]	108	OUT_CELL	—
IAPS2[1]	107	IN_CELL	—
IAPS2[0]	106	IN_CELL	—
IAPS2[3]	105	IN_CELL	—
IAPS2[2]	104	IN_CELL	—
OAPS2[1]	103	OUT_CELL	—
OAPS2[0]	102	OUT_CELL	—
OAPS2[3]	101	OUT_CELL	—
OAPS2[2]	100	OUT_CELL	—
IAPS3[1]	99	IN_CELL	—
IAPS3[0]	98	IN_CELL	—

Downloaded by [illegible] Team of Partminer on Wednesday, February 21, 2007 06:59:32 PM

Name	Register Bit	Cell Type	Device ID
IAPS3[3]	97	IN_CELL	—
IAPS3[2]	96	IN_CELL	—
OAPS3[1]	95	OUT_CELL	—
OAPS3[0]	94	OUT_CELL	—
OAPS3[3]	93	OUT_CELL	—
OAPS3[2]	92	OUT_CELL	—
IAPS4[1]	91	IN_CELL	—
IAPS4[0]	90	IN_CELL	—
IAPS4[3]	89	IN_CELL	—
IAPS4[2]	88	IN_CELL	—
OAPS4[1]	87	OUT_CELL	—
OAPS4[0]	86	OUT_CELL	—
OAPS4[3]	85	OUT_CELL	—
OAPS4[2]	84	OUT_CELL	—
OEB_OAPSFP	83	OUT_CELL	—
OAPSFP	82	OUT_CELL	—
IAPSFP	81	IN_CELL	—
IAPSFPCLK	80	IN_CELL	—
OEB_RTOHCLK[1]	79	OUT_CELL	—
RTOHCLK[1]	78	OUT_CELL	—
OEB_RTOHCLK[2]	77	OUT_CELL	—
RTOHCLK[2]	76	OUT_CELL	—
OEB_RTOHCLK[3]	75	OUT_CELL	—
RTOHCLK[3]	74	OUT_CELL	—
OEB_RTOHCLK[4]	73	OUT_CELL	—
RTOHCLK[4]	72	OUT_CELL	—
OEB_RTOHFP[1]	71	OUT_CELL	—
RTOHFP[1]	70	OUT_CELL	—
OEB_RTOHFP[2]	69	OUT_CELL	—
RTOHFP[2]	68	OUT_CELL	—
OEB_RTOHFP[3]	67	OUT_CELL	—
RTOHFP[3]	66	OUT_CELL	—
OEB_RTOHFP[4]	65	OUT_CELL	—
RTOHFP[4]	64	OUT_CELL	—
OEB_RTOH[1]	63	OUT_CELL	—
RTOH[1]	62	OUT_CELL	—
OEB_RTOH[2]	61	OUT_CELL	—
RTOH[2]	60	OUT_CELL	—
OEB_RTOH[3]	59	OUT_CELL	—
RTOH[3]	58	OUT_CELL	—

Downloaded by [illegible] on Wednesday, February 21, 2007 06:59:32 PM

Name	Register Bit	Cell Type	Device ID
OEB_RTOH[4]	57	OUT_CELL	—
RTOH[4]	56	OUT_CELL	—
OEB_RPOHCLK[1]	55	OUT_CELL	—
RPOHCLK[1]	54	OUT_CELL	—
OEB_RPOHCLK[2]	53	OUT_CELL	—
RPOHCLK[2]	52	OUT_CELL	—
OEB_RPOHCLK[3]	51	OUT_CELL	—
RPOHCLK[3]	50	OUT_CELL	—
OEB_RPOHCLK[4]	49	OUT_CELL	—
RPOHCLK[4]	48	OUT_CELL	—
OEB_RPOHFP[1]	47	OUT_CELL	—
RPOHFP[1]	46	OUT_CELL	—
OEB_RPOHFP[2]	45	OUT_CELL	—
RPOHFP[2]	44	OUT_CELL	—
OEB_RPOHFP[3]	43	OUT_CELL	—
RPOHFP[3]	42	OUT_CELL	—
OEB_RPOHFP[4]	41	OUT_CELL	—
RPOHFP[4]	40	OUT_CELL	—
OEB_RPOH[1]	39	OUT_CELL	—
RPOH[1]	38	OUT_CELL	—
OEB_RPOH[2]	37	OUT_CELL	—
RPOH[2]	36	OUT_CELL	—
OEB_RPOH[3]	35	OUT_CELL	—
RPOH[3]	34	OUT_CELL	—
OEB_RPOH[4]	33	OUT_CELL	—
RPOH[4]	32	OUT_CELL	—
OEB_RPOHEN[1]	31	OUT_CELL	—
RPOHEN[1]	30	OUT_CELL	—
OEB_RPOHEN[2]	29	OUT_CELL	—
RPOHEN[2]	28	OUT_CELL	—
OEB_RPOHEN[3]	27	OUT_CELL	—
RPOHEN[3]	26	OUT_CELL	—
OEB_RPOHEN[4]	25	OUT_CELL	—
RPOHEN[4]	24	OUT_CELL	—
OEB_B3E[1]	23	OUT_CELL	—
B3E[1]	22	OUT_CELL	—
OEB_B3E[2]	21	OUT_CELL	—
B3E[2]	20	OUT_CELL	—
OEB_B3E[3]	19	OUT_CELL	—
B3E[3]	18	OUT_CELL	—

Downloaded by [illegible] on Wednesday, February 21, 2007 06:59:32 PM

Name	Register Bit	Cell Type	Device ID
OEB_B3E[4]	17	OUT_CELL	—
B3E[4]	16	OUT_CELL	—
OEB_RCLK[1]	15	OUT_CELL	—
RCLK[1]	14	OUT_CELL	—
OEB_RCLK[2]	13	OUT_CELL	—
RCLK[2]	12	OUT_CELL	—
OEB_RCLK[3]	11	OUT_CELL	—
RCLK[3]	10	OUT_CELL	—
OEB_RCLK[4]	9	OUT_CELL	—
RCLK[4]	8	OUT_CELL	—
OEB_PGMRCLK[1]	7	OUT_CELL	—
PGMRCLK[1]	6	OUT_CELL	—
OEB_PGMRCLK[2]	5	OUT_CELL	—
PGMRCLK[2]	4	OUT_CELL	—
OEB_PGMRCLK[3]	3	OUT_CELL	—
PGMRCLK[3]	2	OUT_CELL	—
OEB_PGMRCLK[4]	1	OUT_CELL	—
PGMRCLK[4]	0	OUT_CELL	—

Notes

1. When set high, INTB will be set to high impedance.
2. Each output cell has its own output enable (OEB_*), except for the differential outputs.
3. PGMRCLK[4] is the first bit in the boundary scan chain, and ALE is the first bit out of the boundary scan chain.
4. It is assumed that the differential I/O will drive or will be driven differentially. A logic 1 being driven on a differential output via the JTAG scan chain will cause a logic 1 to be driven onto "positive" or "_P" pin, and a logic 0 to be driven onto the "negative" or "_N" pin. A similar convention is true for differential inputs.

Downloaded by Content Team of Partmi Inc on Wednesday, February 21, 2007 06:59:32 PM

14 Operation

14.1 Device Reset

The reset pin of the PM5390 device (RSTB – active low) should be asserted for at least 1 ms to initiate a complete initialization, or re-initialization, of the device. While RSTB is held low (logic 0) both the digital and the analog portions of the chip are being reset.

After de-assertion of the RSTB pin the device will continue to hold its internal digital reset asserted until an internal timer expires after 10 to 14 ms.. This will allow the analog clock synthesizers (CSUs) for the high-speed device interfaces (OIFS or line side, APS and PL4) to stabilize to their selected reference frequencies before allowing the digital portions of the device to operate.

Software may elect to reset the PM5390 via register bits. This is accomplished by writing to the PM5390 Master Reset and Configuration register. The software should set the ARESET_OIF, ARESET_APS, ARESET_PL4 and DRESET register bits to logic 1 to perform a software reset of the device. The software must pause no less than 1ms (there is no upper limit) before de-asserting analog reset by setting the ARESET_OIF, ARESET_APS and ARESET_PL4 bits to logic 0. After de-asserting analog reset, the software must wait no less than 10ms (there is no upper limit) before de-asserting digital core reset by setting the DRESET bit to logic 0. As with assertion of the RSTB pin, the software must also insure that the REFSEL[1:0] pins are in a stable state and that all clocks for the device are present for a minimum of 1ms prior to initiating a software reset sequence. Note that the internal 10ms digital reset delay timer is only initiated after an appropriate RSTB pin reset sequence. Asserting software reset via ARESET or DRESET register bits will not properly sequence the delay timer.

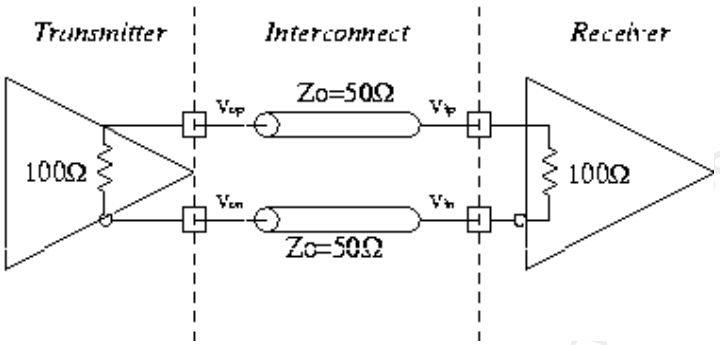
14.2 Line-Side LVDS Interface Overview

The LVDS family of cells allows the implementation of 622 Mbit/s LVDS links. Four 622 Mbit/s LVDS form a set of high-speed serial data links for passing an STS-48 aggregate data stream. Sixteen 622 Mbit/s LVDS form a set for passing an STS-192 aggregate data stream.

A generic LVDS link according to IEEE 1596.3-1996 is illustrated below. The transmitter drives a differential signal through a pair of 50Ω characteristic interconnects, such as board traces, backplane traces, or short lengths of cable. The receiver presents a 100Ω differential termination impedance to terminate the lines. Included in the standard is sufficient common-mode range for the receiver to accommodate as much as 925mV of common-mode ground difference.

Downloaded by Content from Parthiber Inc at Wednesday, February 14, 2007 08:39:32 PM

Figure 31 Generic LVDS Link Block Diagram



14.3 Line-Side Receivers and SIPO

The LVDS Receiver (RXLV) converts LVDS signaling levels to CMOS digital bit-serial data. A total of twenty RXLV blocks are instantiated in the S/UNI 9953 line receive section. In single STS-192/STM-64 mode, the LVDS receive block supports a 16-bit 622.08 MHz differential LVDS line side interface for direct connection to external clock recovery, clock synthesis and serializer-deserializer components. In quad STS-48/STM-16 mode, the LVDS receive block supports four independent 4-bit 622.08 MHz LVDS line side interface for direct connection to external clock recovery, clock synthesis and serializer-deserializer components.

Note: In both modes, an external Serial to Parallel Converter (SIPO) must be used. If the SIPO supports A1/A2 framing, it must be disabled by negating its out-of-frame (OOF) input port.

This bit-serial data is fed to a serial-in-parallel-out (SIPO) block. The SIPO block divides the 622MHz receive clock by 8 and generates a parallel 8-bit (running at 77.76MHz) data bus for each bit-serial data. Thus a total of sixteen parallel 8-bit busses running at 77.76MHz are fed to the SRLI block.

14.4 Programming the S/UNI 9953 Master Configuration Registers

The S/UNI 9953 Receive and Transmit data-paths are configured mainly via the SSMODE[1:0] bits in the S/UNI 9953 Master Reset and Configuration (0001H) register. These bits allow the configuration of the device to support an STS-192c/STM-64c or four STS-48c/STM-16c streams in OC-192 mode and four STS-48c/STM-16c streams in quad OC-48 mode.

The TOP_CHAN[1:0] bits in the S/UNI 9953 System-side Configuration (0002H) register needs to be set to b’00 for single STS-192c/STM-64c stream processing and to b’11 for four STS-48c/STM-16c streams processing. The PL4/FIFO functional blocks must be configured and enabled after TOP_CHAN[1:0] has been set. The R10GEEN and T10GEEN bits in this register should also be set appropriately to enable top-level configuration of data-paths to support ATM cell, POS packet or 10 Gigabit Ethernet frame processing. Individual payload processors (e.g. RCFP-9953, TCFP-9953) should then be configured and enabled as required. This should be followed by the configuration and enabling of the Ingress and Egress FIFO (IFLX, EFLX) blocks.

Downloaded by [illegible] on Tuesday, 6 February [illegible] 6:59:32 PM

Initialization and configuration sequence of the individual PL4 functional (PL4IO, PL4ODP, PL4IDU, PL4MOS) blocks will be described in the POS-PHY Level 4 related subsections in the Operation section.

14.5 SONET/SDH Streams and PL4 Logical Channels Mapping

In the S/UNI 9953, the single transmit/receive STS-192c/STM-64c stream in OC-192 mode is mapped to the single egress/ingress PL4/FIFO logical channel #0 as shown in Table 36.

Table 36 STS-192c/STM-64c Stream to Logical Channel Mapping

Transmit/Receive SONET/SDH OC-192/STS-192c/STM-64c	Egress/Ingress PL4/FIFO Logical Channel
1	0

The mapping of the four STS-48c/STM-16c streams to corresponding PL4/FIFO logical channels are shown in Table 37. Column 1 lists the four STS-48c/STM-16c streams when the S/UNI 9953 is configured to support channelized OC-192/STS-192/STM-64 SONET/SDH stream. Column 2 lists the four STS-48c/STM-16c streams when the S/UNI 9953 is configured to support quad OC-48/STS-48c/STM-16c SONET/SDH streams. Column 3 lists the corresponding PL4/FIFO logical channels for the STS-48c/STM-16c streams. Transmit streams are mapped to Egress channels and Receive streams are mapped to Ingress channels.

Table 37 STS-48c/STM-16c Streams to Logical Channels Mapping

Transmit/Receive SONET/SDH OC-192/STS-48c/STM-16c	Transmit/Receive SONET/SDH OC-48/STS-48c/STM-16c	Egress/Ingress PL4/FIFO Logical Channel
1	1	3
2	2	2
3	3	1
4	4	0

14.6 Interrupt Service Routine

The S/UNI 9953 will assert INTB to logic 0 when a condition that is configured to produce an interrupt occurs. To find which condition caused this interrupt to occur, use the procedure outlined below:

1. Read the registers 0010H, 0011H, 0020H and 0021H to find the functional block(s) which caused the interrupt.

2. Find the register address of the corresponding block that caused the interrupt and read its Interrupt Status registers. The interrupt functional block and interrupt source identification register bits from step 1 are cleared once these register(s) have been read and the interrupt(s) identified.

Downloaded by Content Team of Partminer Networks on February, 2007 @ 5:59:32 PM

3. Service the interrupt(s).

4. If the INTB pin is still logic 0, then there are still interrupts to be serviced and steps 1 to 3 need to be repeated. Otherwise, all interrupts have been serviced. Wait for the next assertion of INTB.

Note:

- Interrupts from individual functional blocks will only be asserted via INTB device interrupt pin if their corresponding group interrupt enable register bits (INTE) in registers 0010H, 0011H, 0020H and 0021H are set to logic 1. Otherwise, only the block interrupt status is available for polling.

14.7 Accessing Indirect Registers

Indirect registers are used to conserve address space in the S/UNI 9953.

Use the following steps for writing to indirect registers:

1. Read the BUSY (or equivalent) bit. If it is equal to logic 0, continue to step 2. Otherwise, continue polling the BUSY (or equivalent) bit.

2. Write the desired configurations for the channel into the indirect data registers.

3. Write the channel number (indirect address) to the indirect address register with RWB set to logic 0.

4. Read BUSY. Once it equals 0, the indirect write has been completed.

Use the following steps for reading indirect registers:

1. Read the BUSY (or equivalent) bit. If it is equal to logic 0, continue to step 2. Otherwise, continue polling the BUSY (equivalent) bit.

2. Write the channel number (indirect address) to the indirect address register with RWB set to logic 1.

3. Read the BUSY bit. If it is equal to logic 0, continue to 4. Otherwise, continue polling the BUSY bit.

4. Read the indirect data registers to find the state of the register bits for the selected channel number.

14.8 Using the Performance Monitoring Features

The performance monitor counters within the different blocks are provided for performance monitoring purposes. All performance monitor counters have been sized to not saturate if polled every second. Except for the MSTAT block, the counters will saturate and not roll over if they reach their maximum value. The MSTAT block can be configured to provide an interrupt on counter roll over.

Downloaded by Content Team of Partminer.C on Wednesday, 07 February, 2001 5:59:32 PM

Writing to the S/UNI 9953 Identity, and Global Performance Monitor Update (0000H) register will initiate a global update of all the counters in every functional blocks. The TIP bit in this register can be polled to determine when all the counter values have been transferred and are ready to be read.

In order to update the performance counters in the R64B66B block, the local TIP bit must be set. This is register 2080h, bit 13. Similarly, in order to obtain the status register of the T64B66B, the local TIP bit must be set. This is register 3080h, bit 15.

14.9 Using The Line Bit Error Rate Monitoring Features

The Bit Error Rate Monitor (SBER) block counts and monitors line BIP (B2) errors over programmable periods of time (window size). It can monitor to declare an alarm or to clear it if the alarm is already set. A different threshold must be used to declare or clear the alarm, whether or not those two operations are performed at the same BER. The following tables list the recommended content of the SBER registers for different speeds (STS-N) and error rates (BER). Both SF/SD BER Monitor blocks in SBER are equivalent and are programmed similarly. In a normal application they would be set to monitor different BER.

When the SF/SD CMODE bit is 1, clearing monitoring will be performed using a window size that is 8 times longer than the declaration window size. When the SF/SD CMODE bit is 0, clearing monitoring will be performed using a window size equal to the declaration window size. In all cases the clearing threshold is calculated for a BER that is 10 times lower than the declaration BER, as required in the references. The tables indicate the declare BER, the evaluation period and the recommended CMODE and associated thresholds.

The Saturation threshold is not listed in the table. It is programmed with the value 0xFFFFFF by default, deactivating saturation. Saturation capabilities are provided to allow the user to address issues associated with error bursts. It enables the user to determine a ceiling value at which the error counters will saturate, letting error bursts pass through within a frame or sub window period.

Since the monitoring algorithm is based on a pseudo-sliding window containing 8 sub intervals, the time required to declare or clear an alarm can take up to 9 sub accumulation periods (SAP). The following tables thus consider that each SAP must take a value lower or equal to $1/9^{th}$ of the timing constraint, in frames.

Table 38 Recommended SBER Settings for Different Data and BER Rates, Meeting Telcordia Objectives

STS	Monitored Declare BER	Objective met for Switching Time (s)	SF/SD CMODE	SF/SD SAP (hex)	SF/SD DECTH (hex)	SF/SD CLRTH (hex)
48	10^{-3}	0.008	0	00000007	002116	000677
48	10^{-4}	0.008	0	00000007	0005F8	0000C1
48	10^{-5}	0.008	0	00000007	000095	000019
48	10^{-6}	0.063	0	00000037	000074	000014

Downloaded by [illegible] from Components Direct on Wednesday, 07 Feb 2007 06:20:32 PM

STS	Monitored Declare BER	Objective met for Switching Time (s)	SF/SD CMODE	SF/SD SAP (hex)	SF/SD DECTH (hex)	SF/SD CLRTH (hex)
48	10^{-7}	0.625	0	0000022B	000075	000014
48	10^{-8}	5.200	0	0000120E	000060	000011
48	10^{-9}	42.000	0	000091D5	00004C	00000F
192	10^{-3}	0.008	0	00000007	008547	00195E
192	10^{-4}	0.008	0	00000007	001860	0002D7
192	10^{-5}	0.008	0	00000007	000280	000053
192	10^{-6}	0.016	0	0000000E	000076	000014
192	10^{-7}	0.156	0	0000008A	000074	000014
192	10^{-8}	1.300	0	00000483	000060	000011
192	10^{-9}	10.400	0	0000241C	00004B	00000F

Table 39 Recommended SBER Settings for Different Data and BER Rates, Meeting Telcordia and ITU Requirements

STS	Monitored Declare BER	Requirement met for Switching Time (s)	SF/SD CMODE	SF/SD SAP (hex)	SF/SD DECTH (hex)	SF/SD CLRTH (hex)
48	10^{-3}	0.01	0	00000008	0025A5	00077B
48	10^{-4}	0.10	0	0000002B	002554	000465
48	10^{-5}	1.00	0	00000192	00256F	000426
48	10^{-6}	10.00	0	00000F98	002570	000420
48	10^{-7}	100.00	0	00009BD6	002571	00041F
48	10^{-8}	1,000.00	0	00061647	002571	00041F
48	10^{-9}	10,000.00	0	003CDEAD	002571	00041F
192	10^{-3}	0.01	0	00000008	0097FA	001D2C
192	10^{-4}	0.10	0	0000002B	00970C	0010FD
192	10^{-5}	1.00	0	00000192	009789	001004
192	10^{-6}	10.00	0	00000F98	00978F	000FEB
192	10^{-7}	100.00	0	00009BD6	009792	000FE9
192	10^{-8}	1,000.00	0	00061647	009793	000FE9
192	10^{-9}	10,000.00	0	003CDEAD	009793	000FE9

Important Notice:

The user should NOT use CMODE = 1 mode when working with Telcordia or ITU requirements for the evaluation periods. In that case, the clearing time (8 times declare time) would not be conform to the requirements (where clearing time requirement = declare time requirement). For the same reason, the user should also avoid using CMODE = 1 with Telcordia objectives when dealing with STS-1 or any detection threshold = 10^{-3}.

Downloaded by Content Team of PMC-Sierra Inc on Wednesday, 07 February 2007 06:

The user should note that a probability of 99% was assumed as the probability that the switch initiation time (declaring) is below the Telcordia requirement. Since the Telcordia specification is vague regarding this issue (“must be very close to 1.0”), the approximation with 0.99 is sufficient and lets the Telcordia requirements be identical to the ITU requirements.

The user should also note that the Telcordia objectives are stricter than Telcordia and ITU requirements upon detection and clearing times. But Telcordia and ITU requirements are stricter than Telcordia objectives upon detection and clearing probability for a given BER (99% vs. 95% for Telcordia objectives).

14.10 Using The Receive Trail Trace Processor Features

The RTTP monitors a one byte, 16 bytes or 64 bytes trail trace message. To monitor a one-byte message, ALGO register bits must be set to 11 (algo3). The trail trace byte is captured at address 40H. To monitor a 16 byte message, ALGO register bits must be set to 01/10 (algo1/2) and LENGTH16 register bit must be set to logic one. The trail trace message is captured between RTTP indirect addresses 40H and 4FH. To monitor a 64 byte message, ALGO register bits must be set to 01/10 (algo1/2) and LENGTH16 register bit must be set to logic zero. The trail trace message is captured between RTTP indirect addresses 40H and 7FH.

When SYNC_CRLF is low, the synchronization is based on the MSB of the trail trace byte. Only one of the bytes has its MSB set high. The byte with its MSB set high is the first byte of the message. When SYNC_CRLF is high, the synchronization is based on the CR/LF (CR = 0Dh, LF = 0Ah) characters of the trail trace message. The byte following the CR/LF bytes is the first byte of the message.

Figure 32 One-byte Trail Trace Message

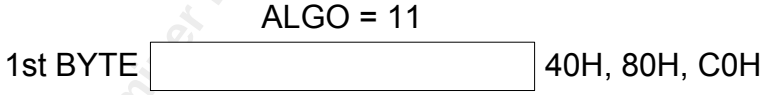


Figure 33 16-byte Trail Trace Message, Sync on MSB

Downloaded by Content Team of Partminer Inc on Wednesday, 21 February, 2007 06:09:32 PM

Figure 34 16-byte Trail Trace Message, Sync on CR/LF

ALGO = 01/10 , LENGTH16 = 1 , SYNC_CRLF = 1

1st BYTE		40H, 80H, C0H
2nd BYTE		41H, 81H, C1H
...		...
15th BYTE	CR	4EH, 8EH, CEH
16th BYTE	LF	4FH, 8FH, CFH

Figure 35 64-byte Trail Trace Message, Sync on MSB

ALGO = 01/10 , LENGTH16 = 0 , SYNC_CRLF = 0

1st BYTE	MSB SET HIGH	40H, 80H, C0H
2nd BYTE		41H, 81H, C1H
...		...
63th BYTE		7EH, BEH, FEH
64th BYTE		7FH, BFH, FFH

Figure 36 64-byte Trail Trace Message, Sync on CR/LF

ALGO = 01/10 , LENGTH16 = 0 , SYNC_CRLF = 1

1st BYTE		40H, 80H, C0H
2nd BYTE		41H, 81H, C1H
...		...
63th BYTE	CR	7EH, BEH, FEH
64th BYTE	LF	7FH, BFH, FFH

To avoid declaring an unstable/mismatch defect when the transmitter updates the trail trace message, the RTTP considers an all zeros message to be matched. An all zeros captured message in algorithm 1 and an all zeros accepted message in algorithm 2 are not validated against the expected message but are considered match, i.e. a match is declared when the captured or accepted message is all zeros regardless of the expected message. This feature can be turned off by setting the ZEROEN register bit to logic one.

Note

- The transmitter is required to force an all zeros trail trace message when the trail trace message is updated.

Downloaded by [illegible] Team of Partners Inc on We[illegible] February, 2001 06:59:32 PM

14.11 Using the Transmit Trail Trace Processor

The TTTP generates a one, 16 or 64 byte trail trace message. To generate a one-byte message, the BYTEEN register bit must be set to logic one. The trail trace byte is placed at TTTP indirect address 40H. To generate a 16 byte message, the BYTEEN register bit must be set to logic zero and LENGTH16 register bit must be set to logic one. The trail trace message is placed between TTTP indirect addresses 40H and 4FH. To generate a 64 byte message, both BYTEEN and LENGTH16 register bits must be set to logic zero. The trail trace message is placed between TTTP indirect addresses 40H and 7FH.

The trail trace message must include synchronization because the TTTP does not add synchronization to the message. The synchronization mechanism is different for a 16 byte message and for a 64 byte message. When the message is 16 bytes, the synchronization is based on the MSB of the trail trace byte. Only one of the 16 bytes has MSB set high. The byte with its MSB set high is the first byte of the message. When the message is 64 bytes, the synchronization is based on the CR/LF (CR = 0Dh, LF = 0Ah) characters of the trail trace message. The byte following the CR/LF bytes is the first byte of the message.

Figure 37 One-byte Trail Trace Message

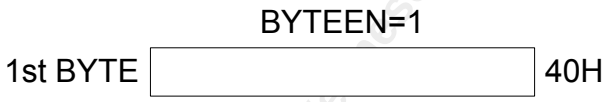
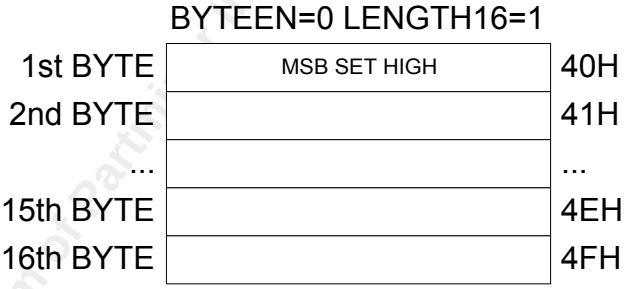
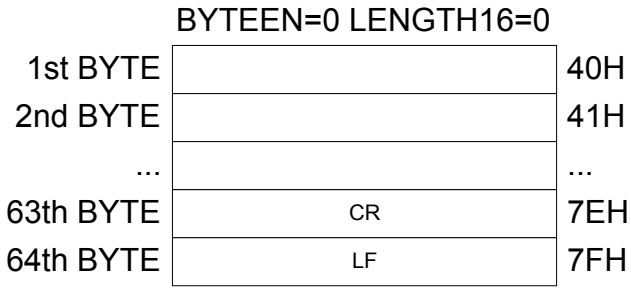


Figure 38 16-byte Trail Trace Message



Downloaded by Content Team of Parts Inc on Wednesday, 07 [illegible] 2007 08:[illegible] PM

Figure 39 64-bytes Trail Trace Message



To avoid generating an unstable/mismatch message, the TTTP can be configured (with the ZEROEN register bit) to generate an all zeros trail trace message while the microprocessor updates the internal message. The enabling and disabling of the all zeros message is not done on message boundary since the receiver is required to perform filtering on the message.

14.12 Configuring the SONET/SDH Alarm Controller

14.12.1 Received Section and Line Alarms (OC-192/STS-192,OC-48/STS-48c)

The Received Section and Line Alarm (SARC) block process all the section and line defects detected by the overhead processors (RRMP, SBER, Section RTTP) and generates the consequential action indications for an OC-192/STS-192/STM-64 or OC-48/STS-48c/STM-16c SONET/SDH data stream. Three consequential action indications are defined: receive section alarm (RSALM), receive line AIS insertion (RLAISINS) and transmit line RDI insertion (TLRDIINS) indications.

Equation 1:

Alarm = (OOF AND OOFEN) OR
(LOF AND LOFEN) OR
(LOS AND LOSEN) OR
(LAIS AND LAISEN) OR
(LRDI AND LRDIEN) OR
(APSBF AND APSBFEN) OR
(STIU AND STIUEN) OR
(STIM AND STIMEN) OR
(SDBER AND SDBEREN) OR
(SFBER AND SFBEREN) OR
(SYNC_ERR AND SYNC_ERREN)

The RSALM indication is defined by Equation 1. OOFEN to SYNC_ERREN are register configuration bits that individually enable or disable each defect. The RSALM indication is provided at the corresponding SALM device pin.

Downloaded by Content Team (Farnell Inc on Wednesday, 7 February, 2007 06:59:32 PM

The RLAISINS indication is defined by Equation 1. OOFEN to SYNC_ERREN are register configuration bits that individually enable or disable each defect. The RLAISINS indication is provided to the corresponding master RRMP block to enable Line AIS insertion in the receive data stream.

The TLRDIINS indication is defined by Equation 1. OOFEN to SYNC_ERREN are register configuration bits that individually enable or disable each defect. The TLRDIINS indication is provided to the corresponding master TRMP block to enable Line RDI insertion in the transmit data stream.

The TLREIINS indication is the receive Line BIP (B2) errors accumulated by the SARC block. This indication is provided to the corresponding master TRMP block to enable Line REI insertion in the transmit data stream.

14.12.2 Received Path Alarms (OC-192/STS-192,OC-48/STS-48c)

The Received Path Alarm (SARC) block process all the path defects detected by the overhead and payload processors (RHPP, Path RTTP, RCFP, RCFP-9953, R64B66B) and generates the consequential action indications for an OC-192/STS-192/STM-64 or OC-48/STS-48c/STM-16c SONET/SDH data stream. Three consequential action indications are defined: receive path alarm (RPALM), receive path AIS insertion (RPAISINS) and transmit path ERDI insertion (TPERDIINS[2:0]) indications.

The first step to the generation of the consequential action indications is to monitor the PLOP, PLOPC, PAIS, PAISC and ALLPAISC signals in order to generate the PAISPTR and PLOPTR defects.

Equation 2:

PLOPTR = PLOP PLOPTRCFG[1:0] = 00

PLOPTR = PLOP or PLOPC PLOPTRCFG[1:0] = 01

PLOPTR = PLOP or PLOPC or PAIS or PAISC PLOPTRCFG[1:0] = 10

PLOPTR = ‘0’ PLOPTRCFG[1:0] = 11

PLOPTRCFG[1:0] are SARC register configuration bits that defines the PLOPTR defect. A path loss of pointer defect is declared when the selected Equation 2 is true. A path loss of pointer defect is removed when the selected Equation 2 is false. An interrupt is generated when a PLOPTR defect is declared and also when a PLOPTR defect is removed. Optionally, the PLOPTR defect can be terminated by a PAISPTR defect (selectable with the PLOPTREND register configuration bit).

Equation 3:

PAISPTR = PAIS PAISPTRCFG[1:0] = 00

PAISPTR = PAIS or PAISC PAISPTRCFG[1:0] = 01

Downloaded by Cortina Systems c/o Partner Inc on Wednesday, February 21, 2007 06:50:32 PM

PAISPTR = PAIS and ALLPAISC PAISPTRCFG[1:0] = 10

PAISPTR = '0' PAISPTRCFG[1:0] = 11

PAISPTRCFG[1:0] are SARC register configuration bits that defines the PAISPTR defect. A path alarm indication signal defect is declared when the selected Equation 3 is true. A path alarm indication signal defect is removed when the selected Equation 3 is false. An interrupt is generated when a PAISPTR defect is declared and also when a PAISPTR defect is removed.

With the PLOPTR and the PAISPTR defects, we can define the receive path alarm (RPALM), the receive path AIS insertion (RPAISINS) and the transmit path ERDI insertion (TPERDIINS[2:0]) indications.

The PPLU, PPLM, PUNEQ, PPDI, PRDI, PERDI, PTIU and PTIM signals are alarms from RRMP, RHPP, Path RTTP blocks and the LCD signal is an alarm from the payload processors (RCFP, RCFP-9953, R64B66B).

Equation 4:

Alarm = (RSALM AND RSALMEN) OR
(PLOPTR AND PLOPTREN) OR
(PAISPTR AND PAISPTREN) OR
(PPLU AND PPLUEN) OR
(PPLM AND PPLMEN) OR
(PUNEQ AND PUNEQEN) OR
(PPDI AND PPDIEN) OR
(PRDI AND PRDIEN) OR
(PERDI AND PERDIEN) OR
(PTIU AND PTIUEN) OR
(PTIM AND PTIMEN) OR

(PGROWTH AND PGROWTHEN) OR

(LCD AND LCDEN)

The RPALM indication is defined by Equation 4. RSALMEN to PGROWTHEN are SARC register configuration bits that individually enable or disable each defect. The RPALM indication is provided at the corresponding RALM device pin.

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:02:2 PM

Equation 5:

Alarm = (RLAISINS AND RLAISINSEN) OR
(PLOPTR AND PLOPTREN) OR
(PAISPTR AND PAISPTREN) OR
(PPLU AND PPLUEN) OR
(PPLM AND PPLMEN) OR
(PUNEQ AND PUNEQEN) OR
(PPDI AND PPDIEN) OR
(PRDI AND PRDIEN) OR
(PERDI AND PERDIEN) OR
(PTIU AND PTIUEN) OR
(PTIM AND PTIMEN) OR

(PGROWTH AND PGROWTHEN]) OR

(LCD AND LCDEN)

The RPAISINS indication is defined by Equation 5. RLAISINSEN to PGROWTHEN are SARC register configuration bits that individually enable or disable each defect. The RPAISINS indication is provided to the corresponding SVCAs to enable Path AIS insertion in the receive data stream.

Table 40 ERDI-P Encoding (PRDIEN = 0)

DEFECT	PRIORITY	ERDI-P[2:0]
PLOPTR or PAISPTR	1	101
PUNEQ, PTIU or PTIM	2	110
PPLU, PPLM or LCD	3	010
None	4	001

Table 41 ERDI-P Encoding (PRDIEN = 1)

DEFECT	ERDI-P[2:0]
None	000
PLOPTR or PAISPTR	100

The TPERDIINS[2:0] indication is defined by Table 40 when the PRDIEN register configuration bit in SARC is logic zero and by Table 41 when PRDIEN is logic one. The TPERDIINS[2:0] indication is provided to the corresponding master THPP block to enable Path/Enhanced Path RDI insertion in the transmit data stream.

The TPREIINS indication is the receive Path BIP (B3) errors accumulated by the SARC block. This indication is provided to the corresponding master THPP block to enable Path REI insertion in the transmit data stream.

Downloaded by Content Team of Partsim Inc on Wednesday, 07 February, 2007 06:59:32 PM

14.13 Input APS Port "IAPSFP" Synchronization

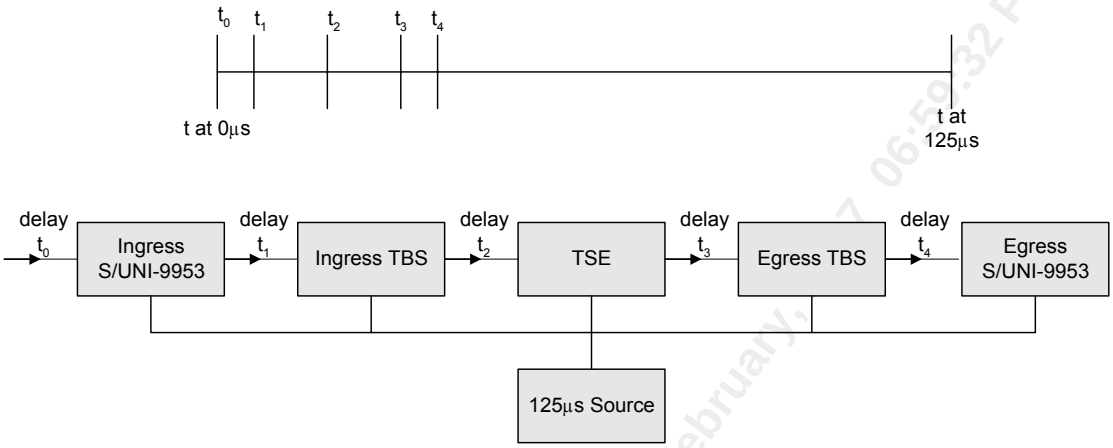
Any TSE/TBS/SPECTRA/SUNI fabric based on the CHESS™ SET can be viewed as a collection of "columns" of devices. A TST switch (see Figure 40) has five columns: one column consisting of the ingress flow from the load devices (e.g., a SUNI-9953); one column consisting of the ingress flow through the TBS devices; a column consisting of the TSE devices; and one column consisting of the egress flow through the load devices (e.g. a S/UNI 9953). Note that the devices in columns 0 and 4 (1 and 3) are the same devices. The dual column references refer to their two separate simplex flows. STS-12/STM-4 frames are pipelined through this structure in a regular fashion, under control of a single clock frequency (77.76 MHz). There are latencies between these columns, and these latencies may vary from path to path. The following design is used to accommodate these latencies.

A timing pulse for SONET frames (8kHz, 125 µs) is generated and fed to each member of the CHESS™ SET. Each CHESS™ chip has a *FrameDelay* register (AIJ0DLY[13:0] in the S/UNI 9953 APS Input TelecomBus Synchronization Delay) which contains the count of 77.76 MHz clock ticks that device should delay from the timing pulse before expecting the framing character of the STS-12 frame. The base timing pulse is called t. The delays from t based on the settings of the AIJ0DLY[13:0] or equivalent in the successive columns of CHESS™ chips are called $t_0, \ldots t_4$. The first signal, t_0, determines the start of an STS-12/STM-4 frame. This signal is used to instruct the ingress load devices to start emitting an STS-12/STM-4 frame (with its special "J0" control character) at that time. t_i is determined by the customer, based on device and wiring delays to be approximately the earliest time that all "J0" characters will have arrived in the ingress FIFOs of the t_i column of devices. t_i is selected to provide assurance that all "J0" characters have arrived. The i^{th} column of devices use the t_i signal to synchronize emission of the STS-12/STM-4 frames.

The ingress FIFOs permit a variable latency in IAPSFP arrival of up to 16 clock cycles. That is, the largest tolerable delay between the slowest and fastest LVDS is 16 bytes. Consequently, the external system must ensure that the relative delays between all the 16 receive LVDS links be less than 16 bytes. The minimum value for the internal programmable delay (AIJ0DLY[13:0]) is the delay to the last (slowest) J0 character plus 20 bytes. The maximum value is the delay to the first (fastest) J0 character plus 36 bytes. The actual programmed delay should be based on the delay of the "slowest" of the 16 links – the link in which J0 arrives last plus a small safety margin of 1 or 2 words. The magnitude of the clock cycle delay is bounded by two parameters. First, the programmed delay register AIJ0DLY is 14 bits. This implies that a clock cycle delay of 214 –1 or 16,383 clock cycles can be programmed. However, the second parameter, the frame rate (125 µs), bounds the delay to one STS-12 frame or 9719 (9720 unique values but 0 is the value for no delay) clock cycles (125 µs x 77.76 MHz), after which the next SONET frame begins.

Downloaded by Content Delivery on Thursday, 7 February, 2013 3:37 PM

Figure 40 "IAPSFP" Synchronization Control



14.14 Configuring the Receive APS for Path Termination

When the device is used as a working protect, it is typical to send the incoming APS data directly to the payload termination blocks (RCFP, RCFP-9953). This is illustrated in Figure 6. There may be occasions where a regeneration of the path is required prior to payload processing. Thus, the receive APS data would need to be redirected to the RHPP blocks in order to do this. This is illustrated in Figure 8. All of the APS datapaths are controlled by the APSMUXCTRL control bits in registers 0x0007 – 0x000A. Note that if the APS data is being sent to the RHPPs (APSMUX0CTL=1), then the RCFP blocks must receive data from the SVCA blocks (APSMUX1CTL=0) instead of the normal APS mux setting of logic 1.

14.15 Receive PCS - R64B66B

The R64B66B performs the required functionality for the PCS layer when the PM5390 is configured to support 10 Gigabit Ethernet LAN/WAN PHY operation. The block will align to the proper sync characters of '10' or '01' as encoded on the receive data stream. The R64B66B will decode the embedded sync until sync is achieved. Once sync has been achieved, the block will also monitor for improper sync. If the block has synchronized and detects 16 improper sync types within 64 66-bit blocks, the logic will be forced into a re-synchronization state. The re-initialization will assert a loss of code group sync status to the T64B66B block, forcing the remote fault message to be transmitted on the line interface.

Downloaded by Content Team on Attachmate Corporation, Thursday, 07 February, 2008 06:50:32 PM

The R64B66B block will also support fault signaling through the use of ordered sets defined as remote fault and local fault. When four fault messages are detected, the R64B66B will signal to the T64B66B transmit block either remote fault or local fault. Local fault assertion to the T64BT66B block will cause idles alternating with a remote fault message to be sent to the line. Remote fault assertion to the T64B66B block will cause idles to be sent to the line. The R64B66B will need sixty four 66-bit valid blocks without the fault message to return to a normal state. The logic will also act upon a pin level SYNC_ERR from the optical module or receive alarm from the WIS (SONET/SDH) layer. When driven high, or asserted, a loss of code group sync will be signaled to the transmit logic (T64B66B) by the R64B66B and it will also enter an initialization state.

The R64B66B will also monitor for a high bit error state. If the logic receives 16 bit errors within a 125us window, HI_BER interrupt will be asserted. Once a high bit error condition has been detected, the logic will be forced to re-initialize to obtain sync.

The R64B66B provides Ethernet frame delineation before passing the frame data to the RXXG. The logic expects data to be on 32-bit boundaries for alignment. Control and data fields are determined by the sync type decoded from the data stream. A 2 bit sync type field is pulled from the data word every 64 bits. For a sync type of “10”, the packet is defined as control and data type. When the sync type is “01”, the packet is defined as data only. There are only 2 valid SOP control types defined, 0x78 and 0x33. The R64B66B will decode proper frame delineation and begin sending the frame to the RXXG. The logic will also expect proper termination of the frame with an EOP. If an EOP is not present, the frame will be indicated as errored as it is being sent to the RXXG. If during reception of a frame a fault condition occurs, the R64B66B will error the current frame and process the pending fault. The R64B66B will not terminate a frame. It will however mark the frame to be in error with EOP.

14.16 Receive PCS Layer Error Handling

This section describes the behavior of the RX PCS during error conditions and during a fault condition. The RX PCS conforms to the 802.3ae standard for all error and fault conditions as described in Clauses 49 and 46 of the 802.3ae standard. All errors that the RX PCS encounters are communicated to the RX MAC by latching the error condition until the end of packet is received. All fault conditions are terminated in the RX PCS block (i.e. will not be propagated to the system interface).

The possible error conditions that exist are: Receive State Machine Errors, Invalid 66-bit blocks, Error control code, Loss of sync, Bit Error State Machine.

The possible fault conditions are Local Fault or Remote Fault.

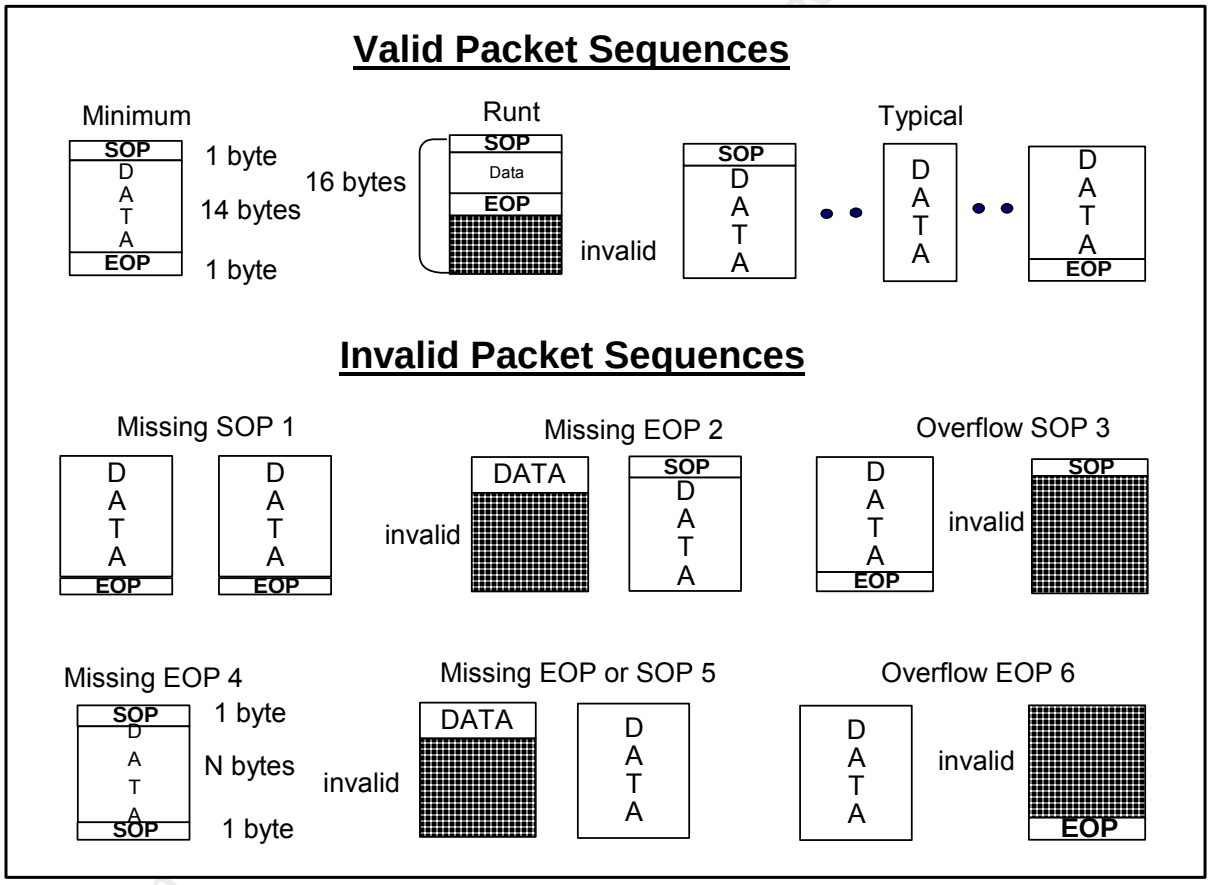
The sections to follow will describe that details of the error conditions and the fault conditions.

Downloaded by Content Team of Chinaaet.com for internal use only on Thursday, February 01, 2007 3:56:27 PM

14.16.1 Receive State Machine Errors

The RX PCS follows the Receive State Machine in Figure 49-14 of 802.3ae. When the Receive State Machine transitions to RX_E (Error state), the RX PCS will replace the payload with all 0's, but still drive the byte valid signals for all 8 bytes. The RX PCS will latch the error condition and when a good end-of-frame occurs, will drive the appropriate PCS layer error signal to the RX MAC.

Figure 41 Expected Packet Formats



14.16.2 Invalid 66-Bit Blocks

There are three types of invalid 66-bit blocks:

- The sync field has a value of 00 or 11
- The type field contains a reserved value
- Any control character contains a value not in Table 49-1 of 802.3ae

Downloaded by ComentTeam

When the RX PCS encounters an invalid 66-bit block the Receive State Machine will transition to the RX_E(Error) state.

14.16.3 Error Control Code

The 802.3ae defines an Error control code to be eight control characters and its first character is an Error control code (0x1e). This condition can only occur when the type field is 0x1e and the first control code (C0[6:0]) is 0x1e and the rest of the control codes (C1-C7) are either 0x0 or 0x1e. When this is encountered the Receive State Machine will transition to the RX_E(Error) state.

14.16.4 Loss Of Sync

Once the RX PCS has achieved the initial synchronization there are two ways for the RX PCS to lose sync. If within receiving 64 66-bit blocks there are 32 or more invalid sync fields(00,11) or if the SYNC_ERR signal is asserted

When a Loss of sync occurs, the RX PCS will terminate and error any packet that is being transferred across the system interface and assert the RX_LOS status signal and LOS status bit. The assertion of the LOS status bit can cause an interrupt to be generated if enabled.

If the Loss of sync is due to the assertion of SYNC_ERR a sync_err status bit will also be asserted. The assertion of the sync_err status bit can cause an interrupt to be generated if enabled.

14.16.5 Bit Error State Machine

The RX PCS monitors bit errors in the sync field. The Bit Error State Machine is defined in Figure 49-12 of 802.3ae. The Bit Error State Machine uses an 125us timer to give a window for a high bit error indication. A high bit error is defined as 16 bit errors within an 125us window. When a high bit error occurs the hi_ber status bit will be asserted, this can cause an interrupt to be generated if enabled. When the BER State Machine goes into a HI_BER state the Receive State Machine will jump to the RX_INIT state causing no data to be transferred to the RX MAC. The Receive State Machine will remain in the RX_INIT state until the HI_BER state is cleared.

The 125us timer is a 14-bit counter that rolls over to 0 when the counter reaches the default done value. The default done value on reset is 20162 or 0x4EC2. The calculation for the 125us timer is 125us/6.2ns.

14.16.6 Fault Conditions

Fault signaling is communicated by using the defined Sequence Ordered Set in 802.3ae The RX PCS also includes part of the RS layer, therefore the section in clause 46 Link fault signaling also applies.

Downloaded by Content Team of Parts Engine on Wednesday, 21 February, 2007 10:50:32 PM

Local Fault

A Local Fault(LF) is defined as being one of the Order Set Type Control codes defined in figure 49-7 of 802.3ae with the D3 or D7 byte field being 0x01. When at least 4 LF messages are received within the 802.3ae defined window, the RX PCS will assert the RX_LF status signal and assert the Link Fail status bit. The assertion of the RX_LF status signal or Link Fail status bit can cause an interrupt to be generated if enabled. After achieving a Local Fault state, when there is an absence of Local Fault messages for at least 64 clocks (@6.2ns) the RX PCS will de-assert RX_LF status signal and the Link Fail status bit. The Local Fault messages are terminated in the RX PCS, only IDLE's are passed to the RX MAC.

Remote Fault

A Remote Fault(RF) is defined as being one of the Order Set Type Control codes defined in figure 49-7 of 802.3ae with the D3 or D7 byte field being 0x02. When at least 4 RF messages are received the RX PCS will assert the RX_RF status signal. The assertion of the RX_RF status signal can cause an interrupt to be generated if enabled. After achieving a Remote Fault state, when there is an absence of Remote Fault messages for at least 64 clocks (@6.2ns) the RX PCS will de-assert RX_RF status signal. The Remote Fault messages are terminated in the RX PCS, only IDLE's are passed to the RX MAC.

14.17 Controlling Ethernet Frame Reception and Transmission

The reception and transmission of Ethernet frames within the PM5390 can be halted or enabled under software control. The TXEN0 and RXEN0 bits within the transmit and receive MACs (TXXG and RXXG) Configuration register enables and disables the transmit and receive data flows respectively. In addition, the FCTX, FCRX and PARF bits determine the response of the PM5390 to MAC Control frames.

14.17.1 Enabling and Disabling Reception

When the RXEN0 bit is deasserted (logic 0), the channel will cease data reception of both MAC Data frames and MAC Control frames at the next frame boundary (that is, during the inter-frame gap). If the channel is in the middle of receiving a frame, the frame reception will complete. All further frames, both MAC Data frames and MAC Control frames, that ingress at the RXXG line side interface will be ignored. All frames that have been received prior to halting and are buffered within either the RXXG receive FIFO or the IFLX FIFO for this channel will continue to ingress. These frames will be transferred across the PM5390 device RDAT[15:0] pins as per the PL4 Bus protocol. By default the PM5390 comes out of reset with the RXEN0 bit logic 0 (i.e. reception disabled)

It is possible to select whether a MAC Control frame is forwarded to the system side PL4 interface. The PARF bit of the **RXXG Configuration 1** register controls this feature. By default, MAC Control frames are not forwarded.

The FCRX bit in the **TXXG Configuration 1** register determines whether the MAC Control sub-layer for this channel will respond to a received MAC PAUSE Control frame. If FCRX is a logic 1 and a MAC PAUSE Control frame is received, the pause timer counter will be loaded with the PAUSE_TIME value of the received frame. If FCRX is a logic 0, the load of the pause timer counter is inhibited and the transmit of MAC Data frames from this channel is not paused.

Downloaded by Cirrcuit Tree Electronic on Wednesday, 07 May, 2007 07:53 PM

14.17.2 Enabling and Disabling MAC Transmission

The Ethernet MAC transmit interface will be disabled if the TXEN0 bit of the **TXXG Configuration 1** register is logic 0. TXEN0 is logic 0 when the PM5390 comes out of reset. To enable the MAC interface to transmit either MAC Data or MAC Control frames, TXEN0 must be logic 1. The TXEN0 is used to enabled and disable the transmission of MAC Data frames and MAC Control frames.

When the TXEN0 bit is set to logic 0, the TXXG will cease data transfer for the transmit or egress direction on the PM5390 device. If the TXXG is in the middle of sending a frame, that frame will be finished without error. The PM5390 will then cease to transmit further MAC Data frames. If the system-side source device continues to transfer data to the PM5390 for this channel (over the PL4 TDAT[15:0] pins), the data will be buffered until all egress buffer resources have been used on the EFLX FIFO. The egress buffer resource levels are reported to the system source device using the PL4 Bus FIFO status signals over the TSTAT[1:0] pins.

14.18 Ten Gigabit Ethernet InterFrameGap Support

The PM5390 operates on frames having a range of InterFrameGap (IFG) at the Ten Gigabit Ethernet MAC interface. The receive IFG setting is fixed whereas the transmit IFG spacing is programmable.

14.18.1 Ten Gigabit Ethernet Receive IFG

The PM5390 can receive frames continuously with an IFG of equal to or greater than 40 bit times or 5 bytes. The normal receive interval is specified as the time between the last octet of the FrameCheckSequence on the previous frame and the sampling of the Start of Frame Delimiter (SFD). Note that the 9.6 ns minimum receive interval encompasses the time required for the inter-frame gap, preamble octets and start frame delimiter.

14.18.2 Ten Gigabit Ethernet Transmit IFG

For transmit or egress traffic the PM5390 will insert a minimum IFG of 12 bytes or 9.6 ns by default. The transmit IFG can also be programmed to allow a minimum IFG or 8~~5~~ bytes~~ or 4 ns~~. The IPGT[5:0] field in the **TXXG Configuration 1** register defines the back-to-back IFG between frames and can be set to one of the non-reserved values as per the table below.

Table 42 Transmit InterPacket Gap Encoding

IPGT[5:0]	IPG (In Bytes)	Comment
08h	8	
09h	9	
0Ah	10	
0Bh	11	
0Ch	**12**	**Default value**
10h	16	
14h	20	
18h	24	

Downloaded by Content Team of Datasheet Inc. on Wednesday, 07 February 2007, 06:55 PM

IPGT[5:0]	IPG (In Bytes)	Comment
1Ch	28	
20h	32	
24h	36	
28h	40	
2Ch	44	
30h	48	
34h	52	
38h	56	
3Ch	60	
Any other value	—	Reserved

To ensure 32-bit alignment while transmitting back-to-back frames with minimum IFG, the TXXG does the following:

- The 32BIT_ALIGN bit in the **TXXG configuration 1** register needs to be set. This will cause the MAC to then insert and delete Gaps in the data stream to maintain 32bit alignment and to maintain, on average, the programmed IFG for all frames sizes.

In all cases, back-to-back frames will be sent with a transmit interval from the last octet of the FCS of the previous frame to the first octet of data in the next MAC frame of 160 bit-times (which is 96 + 64) if the IPGT encoding is 0x0C; in the case that the IPGT encoding is 0x0B, the transmit interval is 152 bit-times and so on as per the above table.

14.19 Ten Gigabit Ethernet Preamble Support

14.19.1 Transmit Preamble

On Ethernet transmit frames, the TXXG will always insert the 802.3ae specified preamble: the preamble is 7 bytes, aligned on 32-bit boundaries having the octet value 0x55 (serialized bit stream of 10101010 with serial transmission occurring from left to right). The 7-byte preamble is followed by a one-byte StartOfFrameDelimiter, SFD: having the octet value 0xD5 (serialized bit stream of 10101011 with serial transmission occurring from left to right).

14.19.2 Receive Preamble

The RXXG includes configurable options on how it will interpret the preamble and StartOfFrame delimiter (SFD) at the reconciliation sub-layer. This is done through the **RXXG - Configuration 1** register: PUREP and LONGP.

Preamble checking of the content of the preamble field of the packet, ensuring a data pattern of 0x55, is done only if PUREP is a logic 1. If PUREP is a logic 0, then the data pattern during the preamble is not checked. In either case, PUREP does not affect any length check on the preamble. The 802.3ae specification for full duplex operation does not require that PUREP be set to logic 1. Note that the default mode of this register bit is logic 0

Downloaded by Stefan Team of Polaris Inc on Wednesday, 07 February, 2007 06:59:32 PM

The ability of the MAC receive process to ignore frames based on the length of the preamble is controlled by the LONGP register bit. If set to logic 1, the MAC receive process will accept frames having preambles greater than 11 Bytes in length. If LONGP is set to logic 0, packets with preambles greater than 12 bytes will be ignored. The 802.3ae specification for full duplex operation does not require that LONGP is ever set to logic 1. Note that the default mode of this register bit is logic 0: by convention Ethernet frames having preambles of greater than 11 bytes are ignored.

The preamble and SFD are stripped on every received frame, converting the physical packet to an Ethernet Frame. Only the DATA octets from the internal reconciliation frame stream are transferred:

Internal reconciliation frame stream:

<Inter-frame><preamble><sfd><DATA><efd>

Ethernet Frame as transferred on PL4 Bus system interface:

<DATA>

14.20 Ten Gigabit Ethernet MAC Transmit Padding and CRC Generation

The TXXG can pad a frame for transmission that is forwarded from the PL4 system interface and is greater-than-or-equal-to 14 bytes. This is accomplished only if the PADEN and CRCEN bits are set in the **TXXG Configuration 1** register. The frame is padded with data octets having the value 0x0 to 60 bytes if not tagged or 64 bytes if tagged; a 4 octet FCS is appended to the frame prior to transmit.

The PM5390 can append a proper four-octet FCS to each and every frame prior to transmission if the CRCEN bit within the **TXXG Configuration 1** register is set.

As previously described, frames without an error indicator having a length of at least 9 bytes to 14 bytes and if the PADEN bit is set will be padded to 60 bytes and then a bad CRC is appended to the frame and the Error flag is also asserted to the PCS layer to guarantee that the frame is properly marked as bad. 14 bytes are required for the Ethernet frame destination address (6 octets), source address (6 octets), and LENGTH/TYPE field (2 octets).

Frames that are less than 9 bytes will be discarded and an internal debug counter will count the number of times a packet is discarded due to less than 9 bytes.

Table 43 PM5390 Minimum Transmit Frame Size Padding

Frame Length at internal Transmit MAC interface	Frame Type	PADEN State	CRCEN State	Pad Action	CRC Action
<9 bytes	Normal or tagged	X	X	Frame discarded by Transmit MAC control logic and debug counter incremented	

Downloaded by Content Team at Document Inc on Wednesday, 07 February, 2007 06:53:32 PM

Frame Length at internal Transmit MAC interface	Frame Type	PADEN State	CRCEN State	Pad Action	CRC Action
9 to < TX MIN Frame Size Reg.	Normal	0	0	No Pad	Append 4 byte CRC with ERROR[1]
9 to < TX MIN Frame Size Reg	Normal	0	1	No Pad	Append 4 byte CRC with ERROR
9 to < TX MIN Frame Size Reg	Normal	1	0	Pad with 0's to TX MIN Frame Size Reg value	Append 4 byte CRC with ERROR[2]
9 to < TX MIN Frame Size Reg	Normal	1	1	Pad with 0's to TX MIN Frame Size Reg value[3]	Append 4 byte CRC
>= TX MIN Frame Size Reg.	Normal	0	0	No Pad	No CRC Append
>= TX MIN Frame Size Reg.	Normal	0	1	No Pad	Append 4 byte CRC
>= TX MIN Frame Size Reg.	Normal	1	0	No Pad	No CRC Append
>= TX MIN Frame Size Reg.	Normal	1	1	No Pad	Append 4 byte CRC

14.21 Ethernet Frame Transmit Errors

The PM5390 device will use the 64-bit Error Block as defined in Table 49-1 in the 802.3ae standard, to indicate a transmission error to its peer entity across the Ethernet media.

14.21.1 Transmit Frame Error Catalysts

The minimum frame length at the transmit system interface of the TXXG for propagating an error indication is 9 bytes. Any frame indication forwarded by the PL4 system side via the EFLX that has a length less than 9 bytes will be discarded by the transmit control logic internal to the TXXG: hence, no external MAC carrier event will be signaled.

The catalysts for frame transmission with error are listed below. At least one catalyst needs to be true for asserting a frame transmit error on the Ethernet media:

1. If the PL4 system sourcing device asserts an End-Of-Packet status of ABORT during egress frame transfer (PM5390 device pins TDAT[15:0]+/-, TCTL+/-). This error indication is forwarded on to the internal TXXG transmit interface.

[1] Packet is less than the minimum frame size. Transmit MAC will assert and Error to the Transmit PCS at the End of Packet and add a Corrupt CRC to guarantee a downstream receiver will discard this packet.
[2] Same comment as above.
[3] If Frame is VLAN tagged the Pad will increase by 4 bytes.

Downloaded by Content Team of Datasheet.in on Wednesday, 07 February, 2007 12:12:15 PM

2. If the PL4 incoming data word parser (in the PL4IDU logic) indicates that the packet should be aborted. This could be either because a PL4 Bus error occurred (case EOP ABORT) or because a PL4 Bus error was detected (case EOP ABORT). This error indication is forwarded on to the internal TXXG transmit interface.

3. If the egress frame is considered short (see note below), long, or having an internal transmit MAC error (i.e. transmit underrun). Another way of stating this is that the frame is transmit with an error indication if the MAC sub-layer within the TXXG detects a transmit frame having a status that will be interpreted by the peer device across the Ethernet link as erred. NOTE: Short frames at the TXXG internal transmit system interface will assert the Error Propagation character only if the following register settings are in effect:
   - The PADEN bit is set to logic 0

Note that detection of an error in the FrameCheckSequence (FCS) field of a frame during transmission does not result in a transmit error indication on the Ethernet media for the given channel. Restated, an FCS error detected during frame transmission is not a catalyst for asserting the Error_Propagation character. The frame is expected to be detected during the frame receive process on the peer entity across the Ethernet media.

Transmit Underrun

An internal transmit MAC error is detected if the Transmit FIFO internal to the TXXG at the EFLX interface underruns: that is, the FIFO goes empty before an internal End-Of-Packet indicator is read. In a typical system application transmit underrun will not occur as long as the peer device that is sourcing traffic on the PL4 Bus is able to maintain an adequate rate of data transfers. As previously described, the egress FIFO interface on the PM5390 device maintains a cut-through threshold that is used for determining whether data is to be forwarded on to the TXXG for transmission on the Ethernet media. For a system application that is operating on standard Ethernet sized frames (those having a maximum length of 1522 bytes), the cut-through threshold can be set for 1536 bytes (see **EFLX Cut-Through Threshold** register), thereby guaranteeing that frames will not be transferred from the egress FIFO to the TXXG until the complete frame is buffered. Internal to the PM5390 device, the rate of data transfer from the TXXG for transmit data is limited by the 645 MHz device reference clocks, with one octet of data being transferred every reference clock period. The difference in internal clock rates between the TXXG transmit interface and the egress FIFO accounts for at most a two-byte contribution to the transmit underrun calculation:

9600 bytes * 8-bits/byte * 200 ppm = 15.4 bit-times

Therefore, for a system application that is transferring Ethernet frames of 9600 bytes the requirement to prevent underrun is, on a frame-by-frame basis that the traffic sourcing device must transfer the remaining (frame_length – cut-through) number of data bytes within the amount of time that it takes to impress the frame data on the Ethernet media, not counting the inserted IFG and preamble times.

Downloaded by Conseil Fean of Parliament (no) on Wednesday, 07 February, 2018, 6:39:32 PM

For example, to guarantee that transmit underrun does not occur on a frame of 9600 bytes - assuming [1] that the 645 MHz reference clock has an approximate 1.5 ns period; [2] that the EFLX cut-through threshold is set for 1536 bytes; [3] that there are no errors detected on the PL4 Bus incoming word stream at the PL4IDU block of the PM5390 device - the system interface egress device must transfer the last 8604 (i.e. 9600-1536) bytes of the frame on the PL4 Bus within a 12 us (8064 * 1.5 ns) time window starting from the time that the 1536th byte was transferred on the PL4 Bus.

The response of the TXXG to transmit underrun is:

1. All bytes that had been forwarded to the TXXG at the time the underrun occurred will be impressed on the XSBI pins as long as the underrun condition occurs after the 9th byte of the frame (if before 9 bytes, the data is discarded as described previously since there is not a valid Ethernet DA, SA, and IEEE/TYPE field in the frame)

2. At the point of underrun, the error is signaled on the XSBI pins using the Ethernet Transmit Frame Error protocol described below

3. All subsequent data sent by the EFLX to the TXXG will be discarded until the next valid Start-Of-Packet flag is set.

14.21.2 Ethernet Transmit Frame Error Protocol

All frames that are transferred by the MAC interface with a transmit error calculation exhibit the following behavior:

- A 64-bit Control block is formed with the ERROR Control code as defined in Table 49-1 in 802.3ae, all eight character locations.

In the event that the frame being transmit is detected as having an error at the input transmit control interface of the TXXG and prior to an End-Of-Frame indicator, the frame will be truncated by the transmit control logic and the MAC layer will be signaled to assert transmit error. The following transmit errors are detectable at the TXXG transmit control interface and can result in truncation during transmission:

1. An EOP ABORT status is detected on the PL4 system interface. This EOP ABORT could have been indicated on the PL4 Bus as an End-Of-Packet status of ABORT or it could be the result of the PL4IDU logic detecting a word parsing error.

2. Transmit underrun is detected

3. TX Max Frame length is violated

14.22 Frame Length Support

The PM5390 supports a programmable maximum threshold for MAC frame length and a programmable forwarding threshold; the thresholds in both the ingress and egress directions are fully independent and programmable. In addition, there is a minimum fixed size of a frame that is supported in each direction; frames of less than this fixed size are always discarded.

Downloaded by Content Team Parts Direct, Inc. on Wednesday, 07 February, 2007 06:53:32 PM

The PM5390 supports jumbo frames up to 9600 bytes in both the ingress and egress directions.

14.22.1 Ingress (Ethernet Receive) Frame Length

The RXXG supports a minimum ingress frame fragment size of 9 bytes (fixed) and a programmable maximum ingress frame size of up to 9600 bytes.

The minimum frame fragment size requirement is the result of supporting address filtering: any received frame that has less than 9 bytes will be not be forwarded on from the RXXG. If a frame fragment of less than 9 bytes is received it will be filtered and the proper receive statistics information on the frame recorded.

The **RXXG Minimum Receive Frame Length** register control the minimum size of the ingress frame. If the frame is less than the programmed Min frame length the frame will be treated as a Short or Runt frame depending on if the frame had a non-erred or erred FCS respectively. The Short or Runt frame is then filtered and the appropriate status vector is generated for the frame to update the Ethernet Statistics.

The **RXXG Maximum Receive Frame Length** register controls the maximum size of the ingress frame. If the frame is greater than the programmed size the frame will be treated as a long or jabber frame, depending on if the frame had a non-erred or erred FCS respectively. If the length of the received frame is greater than the **RXXG Receive Maximum Frame Length** then the incoming frame is truncated to the length programmed in that register and the frame is flagged as erred.

The **RXXG Receive FIFO Threshold** register sets the forwarding threshold used for ingress frame gathering and error reporting. Frames are passed from the RXXG to the PL4 ingress FIFO if an end-of-frame indication has been received by the RXXG or if the number of bytes received by the RXXG is greater than the **RXXG Receive FIFO Threshold** register. Ethernet MAC frames that are received as erred and that are forwarded on to the system interface (the POS-PHY Level 4 interface) cause the affected packet to have an End-of-Packet status of ABORT in the PL4 Payload Control word following the last byte of the Ethernet frame that is in the PL4 Data word.

This mechanism provides for two different frame error reporting capabilities. First if the forwarding threshold is set higher than the received frame size the RXXG will drop and not forward erred frames. Second if the forwarding threshold is set lower than the received frame size the RXXG will immediately start passing the incoming frame as soon as the threshold is reached. In this case the RXXG passes the state of the ReceiveError flag to the downstream logic and the PM5390 will assert an End-Of-Packet status of ABORT during data transfer on the PL4 bus.

There is no additional frame forwarding threshold register in the ingress data path of the PM5390 device other than the RXXG **Receive FIFO Threshold** register.

Downloaded by Content Department (Guiyang) on Wednesday, 07 February, 2007 16:59:32 PM

14.22.2 Receive Frame Length Checking

The PM5390 device supports frame length checking based on the value of the sixteen bit Length/Type field in the received frame. Receive frame length checking is enabled by setting the FLCHK bit of the **RXXG Configuration 1** register**,** to a logic 1. If FLCHK is set to a logic 1, a received frame will fail the frame length check if the Length/Type field of the frame has a Length interpretation and the number of received octets in the data frame less 18 (Length field indicates the number of MAC client data octets and does not count the 6 octets of destination address nor 6 octets of source address nor 2 octets of Length/Type field itself nor 4 octets of FCS) is GREATER than the numeric value of the Length/Type field. The Length/Type field of a receive frame has a Length interpretation on the PM5390 device if the Ethernet frame is untagged (as per 802.3 standard, clause 3.5.4- "The Length/Type field of a tagged MAC frame always uses the Type interpretation") and the Length/Type field is greater than or equal to 0 decimal and less than or equal to 1500 decimal.

14.22.3 Egress (Ethernet Transmit) Frame Length

The **EFLX FIFO Cut-Through Threshold** register sets the forwarding threshold used for egress frame gathering on a per-channel basis. Packets passed to the PM5390 on the PL4 bus will be gathered in the egress FIFO until an end of packet indication or until the number of bytes transferred to the PM5390 and present in the egress buffer are greater than or equal to the **EFLX FIFO Cut-Through Threshold** register (this register counts in terms of 16-byte data blocks). This forwarding threshold allows frame buffering required to ensure that a frame will not underrun once frame transmission begins on the Ethernet link.

The TXXG supports a minimum frame length of 9 bytes (fixed) at the transmit system interface. The programmable maximum egress frame size is 9600 bytes. A frame that is received with a length of less than 9 bytes, from the PL4 system side (i.e. via the EFLX) will be discarded, regardless as to the setting of the PADEN and CRCEN mode bits. Frames having a length of 9 or more bytes at the system interface will always be transferred by the Ethernet MAC and impressed on the PM5390 XSBI pins.

In order to aid diagnostics, a count of frames that are discarded in the TXXG transmit interface because they had a length of less than 9 bytes is maintained in the **TXXG Filter Error Count** register.

The minimum frame size on the egress channel for MAC frames after any optional padding or FCS appending is 64 bytes: this is a fixed limit. If a frame is transferred to the TXXG transmit interface having a length of between 9 and 64 bytes after any optional padding or FCS appending, then the frame will be transmit as a short erred frame: the error control block will be sent at the end of the frame.

Downloaded by Content Group of Parsing Only Wednesday, February 16, 2005 10:52 PM

The **TXXG Transmit Max Frame Length** register controls the maximum size of the egress frame. The **Transmit Max Frame Length** register specifies the maximum number of bytes transmitted before truncation in an outgoing non-tagged Ethernet frame (in the 802.3-2000 specification, this parameter is termed maxUntaggedFrameSize). The default setting of this register is 0x05EE (1518 decimal), which results in a maximum frame size before frame truncation of 1518 bytes if untagged and 1522 bytes if VLAN tagged. Frames that have exceeded the setting of **Transmit Max Frame Length** are truncated and have the error control block impressed at the End-Of-Packet. VLAN tagged frames have a 4 byte offset (i.e. 1522 bytes by default) before being considered as violating the frame length setting.

The length of the frame as transmit by the Ethernet MAC is determined by the length of the frame transferred by the egress FIFO, the setting of the PADEN and CRCEN mode bits (as described in the section "MAC Transmit Padding and CRC Generation"), and the value of the **TXXG Transmit Max Frame Length** register.

14.23 Frame Data and Byte Format

The PM5390 transfers octets of Ethernet Data Frames in the same order as they are transmitted and received on the Ethernet media. As noted in the IEEE Std 802-1990 (Local and Metropolitan Area Networks: Overview and Architecture):

1. The transmission of data for IEEE 802.3 occurs LSB (Least Significant Bit) first. This is true for the entire packet, LAN MAC address fields (source and destination), MAC-specific fields (e.g. length/type field in IEEE 802.3 LANs) and the MAC Information Field. (See also 802.3 standard, clause 3.3).

2. The 48-bit address (universal or local) is represented as a string of six octets. The octets are displayed from left to right, in the order that they are transmitted on the LAN medium, separated by hyphens. Each octet of the address is displayed as two hexadecimal digits. The bits within the octets are transmitted from left to right as shown below. In the display of octets, the first bit transmitted of each octet on the LAN medium is the LSB of that octet (e.g. I/G address Bit is LSB of octet 0). The Organizationally Unique Identifier is contained in octets 0,1,2 with octets 3,4,5 being administered by the assignee. The example given in Std 802-1990 is:

Table 44 Std 802-1990, Figure 5-3 Universal Address

Octet	0	1	2	3	4	5
	0011_0101	0111_1011	0001_0010	0000_0000	0000_0000	0000_0001
	^					

First bit transmitted on the LAN medium (also the I/G Address Bit).

The hexadecimal representation of this example is: AC-DE-48-00-00-80

This hexadecimal representation is often referred to as the canonical format.

For the purposes of the PM5390, the address example given above in the Std 802-1990 is represented as follows:

Downloaded by Content Team of Parts Life on Wednesday, 07 February, 2007 6:53:24 PM

DA[0] is the 1st bit on the LAN medium: 0
DA[1] is the 2nd bit on the LAN medium: 0
DA[2] is the 3rd bit on the LAN medium: 1
DA[3] is the 4th bit on the LAN medium: 1
DA[4] is the 5th bit on the LAN medium: 0
DA[5] is the 6th bit on the LAN medium: 1
DA[6] is the 7th bit on the LAN medium: 0
DA[7] is the 8th bit on the LAN medium: 1

DA[8] is the 9th bit on the LAN medium: 0
DA[9] is the 10th bit on the LAN medium: 1
DA[10] is the 11th bit on the LAN medium: 1
DA[11] is the 12th bit on the LAN medium: 1
DA[12] is the 13th bit on the LAN medium: 1
DA[13] is the 14th bit on the LAN medium: 0
DA[14] is the 15th bit on the LAN medium: 1
DA[15] is the 16th bit on the LAN medium: 1
And so forth

DA[40] is the 41st bit on the LAN medium: 0
DA[41] is the 42nd bit on the LAN medium: 0
DA[42] is the 43rd bit on the LAN medium: 0
DA[43] is the 44th bit on the LAN medium: 0
DA[44] is the 45th bit on the LAN medium: 0
DA[45] is the 46th bit on the LAN medium: 0
DA[46] is the 47th bit on the LAN medium: 0
DA[47] is the 48th bit on the LAN medium: 1

The PM5390 will represent the address shown above (example in Figure 5-3 of Std 802-1990: AC-DE-48-00-00-80) as

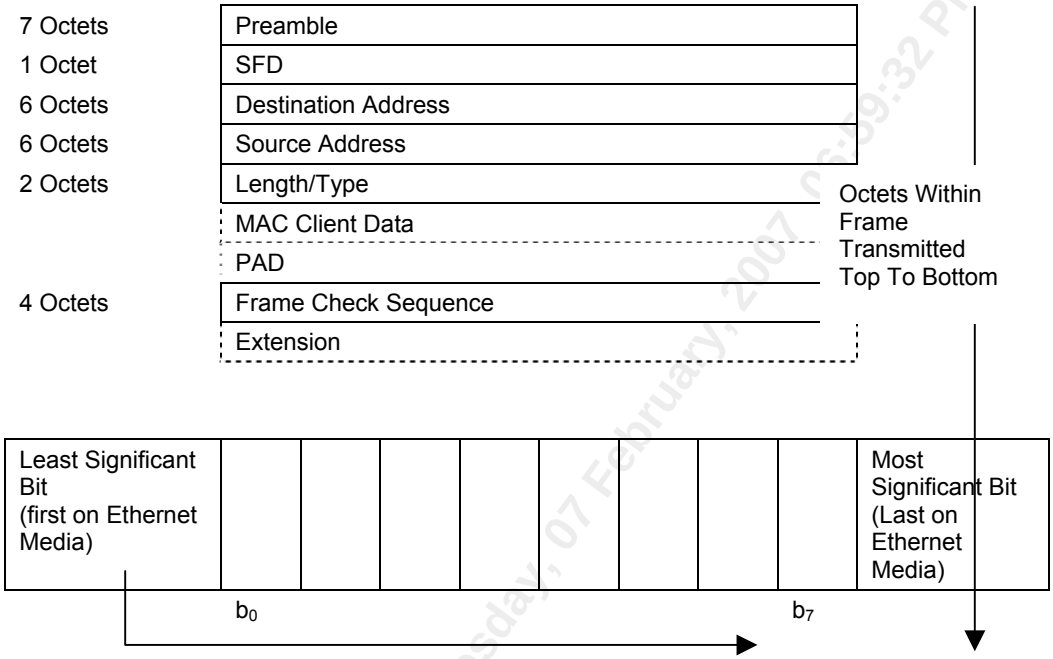
DA[7:0] = AC
DA[15:8] = DE
DA[23:16] = 48
DA[31:24] = 00
DA[39:32] = 00
DA[47:40] = 80

14.23.1 Frame Data and Byte Format On Ethernet Line Side

Bit-in-byte ordering in the 802.3 Ethernet standard is bit 0 (Least Significant Bit) to bit 7 (Most Significant Bit) with bit 0 being the first bit transferred on the Ethernet media. Ethernet data is always transmitted and received via the MAC line side in the following format. Bits are transmitted and received from the top to bottom and from left to right. For example, for the destination address (DA[47:0]), bit DA[0] is transmitted first and bit DA[47] is transmitted last.

Downloaded by Circuit Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Table 45 MAC Frame Format



14.23.2 Frame Data and Byte Format At PL4 Interface

Bit in Byte Ordering within the entire PL4 data path is from bit 7 (Most Significant Bit) to bit 0 (Least Significant Bit). In the ingress direction, the first byte of the frame that is received on the Ethernet line side is impressed on the PL4 RDAT[15:8] byte lane, with the most significant bit aligned to RDAT[15]. Likewise in the egress direction, the first byte of the frame that is to be transmit on the Ethernet line side is impressed on the PL4 TDAT[15:8] byte lane, with the most significant bit aligned to TDAT[15].

Two examples are provided: one for a non-VLAN tagged Ethernet frame having a length of 1518 bytes (so the IEEE correct Length/Type field of the frame is 05-DC) and one for a VLAN tagged Ethernet frame.

Table 46 PM5390 Data Order On PL4 Interface, Non-VLAN Ethernet Frame

Bits 15:8	Bits 7:0
DA[7:0]	DA[15:8]
DA[23:16]	DA[31:24]
DA[39:32]	DA[47:40]
SA[7:0]	SA[15:8]
SA[23:16]	SA[31:24]
SA[39:32]	SA[47:40]
Length/Type[7:0]: 0x05	Length/Type[15:8] 0xDC
Data[7:0]	Data[15:8]

Downloaded by [illegible] Team of Part Time Students on Wednesday, 07 February, 2007 06:39:32 PM

Bits 15:8	Bits 7:0
Data[23:16]	…
…	…
FCS[24:31] 1st octet of **FRAME CHECK SEQUENCE** as received on Ethernet media. As per 802.3 clause 3.2.8, the FCS is impressed on the media with bit x31 first, bit x30 2nd, and so on with bit x0 being transmit last, RDAT[15:8] corresponds to bits [x24,x25,x26,x27,x28,x29,x30,x31].	FCS[16:23] 2nd octet of **FRAME CHECK SEQUENCE** as received on Ethernet media. As per 802.3 clause 3.2.8, the FCS is impressed on the media with bit x31 first, bit x30 2nd, and so on with bit x0 being transmit last, RDAT[7:0] corresponds to bits [x16,x17,x18,x19,x20,x21,x22,x23].
FCS[8:15] 3rd octet of **FRAME CHECK SEQUENCE** as received on Ethernet media. As per 802.3 clause 3.2.8, the FCS is impressed on the media with bit x31 first, bit x30 2nd, and so on with bit x0 being transmit last, RDAT[15:8] corresponds to bits [x08,x09,x10,x11,x12,x13,x14,x15].	FCS[0:7] 1st octet of **FRAME CHECK SEQUENCE** as received on Ethernet media. As per 802.3 clause 3.2.8, the FCS is impressed on the media with bit x31 first, bit x30 2nd, and so on with bit x0 being transmit last, RDAT[15:8] corresponds to bits [x00,x01,x02,x03,x04,x05,x06,x07].

Downloaded by Content Team of Partminer Inc on Wednesday, 01 August 2007 10:32 PM

Table 47 PM5390 Data Order On PL4 Interface, VLAN Ethernet Frame Type

Bits 15:8	Bits 7:0	Comment
DA[7:0]	DA[15:8]	Octets 1,2
DA[23:16]	DA[31:24]	Octets 3,4
DA[39:32]	DA[47:40]	Octets 5,6
SA[7:0]	SA[15:8]	Octets 7,8
SA[23:16]	SA[31:24]	Octets 9,10
SA[39:32]	SA[47:40]	Octets 11,12
0x81	0x00	VLAN Qtag Prefix
TAG_CONTROL [7:0]	TAG_CONTROL [15:8]	Where the 12 bit VID field is given by the most significant 12 bits of TAG_CONTROL; CFI bit is TAG_CONTROL[4], and USER_PRIORITYis TAG_CONTROL[7:5].
Length/Type[7:0]	Length/Type[15:8]	MAC Client Length/Type
Data[7:0]	Data[15:8]	Octets 19,20
Data[23:16]	…	Octets 21,22
…	…	…
FCS[24:31]	FCS[16:23]	FCS[24:31] is the first octet of FCS impressed on the Ethernet media
FCS[8:15]	FCS[0:7]	FCS[0:7] is the fourth octet of FCS impressed on the Ethernet media

14.23.3 Ethernet Frame Segmentation On The PL4 Bus System Interface

The PM5390 device in the ingress direction makes efficient usage of PL4 Bus transfers from the ingress FIFO logic. Scheduling by the PL4MOS is not guaranteed to be done at a frame boundary. The PM5390 device in the ingress direction cannot be programmed to guarantee that entire Ethernet frames will be transmit contiguously.

Note that in the case that the RXXG marked the ingress Ethernet frame with an err delimiter, then the frame will be transferred on the PL4 Bus and terminated with a EOPS[1:0] status of EOP_ABORT). Because of the encoding of the EOP by the PL4 Bus specification in this manner, it is impossible for the PL4 peer entity to determine the delimited length of the erred frame to within one byte. That is, the PL4 peer entity does not know whether one or two bytes of the frame terminated with EOP_ABORT were received at the RXXG link interface.

14.23.4 Example of Data Representation, From Ethernet Physical Packet To PL4 Bus Interface

The following example shows how a Physical Packet corresponding to a 64 byte MAC Data Frame would appear on the Ethernet media and when transferred on the PL4 Bus interface. This holds true for the ingress direction (Ethernet receive media to PL4 RDAT[15:0], RCTL pins) and egress direction (PL4 TDAT[15:0], TCTL pins to Ethernet transmit media).

This example utilizes a 64-byte Ethernet Data Frame that is represented in canonical format as:

Downloaded by Content Team Document Solutions on Wednesday, 21 March 2007 06:59:32 PM

DA = 12-34-56-78-9A-BC
SA = 01-23-45-67-89-AB

LENGTH/TYPE field = 0C-0D (so type interpretation)

MAC CLIENT DATA = 0E-0F-10-11-12-13-14-15-

16-17-18-19-1A-1B-1C-1D-
1E-1F-20-21-22-23-24-25-
26-27-28-29-2A-2B-2C-2D-
2E-2F-30-31-32-33-34-35-
36-37-38-39-3A-3B

FrameCheckSequence field = FD-C9-0F-E2

Table 48 Ten Gigabit Ethernet Frame Example

Ethernet Media Serial Bit Stream (first -> last)	PM5390 Octet Internal Representation	PL4 Bus DAT[] pins and DataBurst cycle	PM5390 Interpretation
/S/ Start_Of_Packet	Internal PCS replaces /S/ with the first preamble octet: 0101_0101	Not transferred	Start_Of_Packet: Physical packet only so not transferred on PL4 Bus
10101010	0101_0101	Not transferred	2nd octet of preamble
10101010	0101_0101	Not transferred	3rd octet of preamble
10101010	0101_0101	Not transferred	4th octet of preamble
10101010	0101_0101	Not transferred	5th octet of preamble
10101010	0101_0101	Not transferred	6th octet of preamble
10101010	0101_0101	Not transferred	7th octet of preamble
10101011	1101_0101	Not transferred	SFD (Start Frame Delimiter) Physical packet only so not transferred on PL4 Bus
01001000	0001_0010	DAT[15:8], cycle 1	Destination Address [7:0]
00101100	0011_0100	DAT[7:0], cycle 1	Destination Address [15:8]
01101010	0101_0110	DAT[15:8], cycle 2	Destination Address [23:16]
00011110	0111_1000	DAT[7:0], cycle 2	Destination Address [31:24]
01011001	1001_1010	DAT[15:8], cycle 3	Destination Address [39:32]
00111101	1011_1100	DAT[7:0], cycle 3	Destination Address [47:40]
10000000	0000_0001	DAT[15:8], cycle 4	Source Address [7:0]
11000100	0010_0011_	DAT[7:0], cycle 4	Source Address [15:8]
10100010	0100_0101	DAT[15:8], cycle 5	Source Address [23:16]
11100110	0110_0111	DAT[7:0], cycle 5	Source Address [31:24]
10010001	1000_1001	DAT[15:8], cycle 6	Source Address [39:32]
11010101	1010_1011	DAT[7:0], cycle 6	Source Address [47:40]
00110000	0000_1100	DAT[15:8], cycle 7	Length/Type Field [7:0]

Downloaded by [illegible] Team of Portman Inc on Wednesday, 07 February, 2007 06:59:32 PM

Ethernet Media Serial Bit Stream (first -> last)	PM5390 Octet Internal Representation	PL4 Bus DAT[] pins and DataBurst cycle	PM5390 Interpretation
00110000	0000_1100	DAT[15:8], cycle 7	Length/Type Field [7:0]
10110000	0000_1101	DAT[7:0], cycle 7	Length/Type Field [15:8] Canonical Format of Length/Type Field is 0C-0D
01110000	0000_1110	DAT[15:8], cycle 8	MAC Client Data, 1st octet
11110000	0000_1111	DAT[7:0], cycle 8	MAC Client Data, 2nd octet
00001000	0001_0000	DAT[15:8], cycle 9	MAC Client Data, 3rd octet
10001000	0001_0001	DAT[7:0], cycle 9	MAC Client Data, 4th octet
……	……	……	……
01011100	0011_1010	DAT[15:8], cycle 30	MAC Client Data, 45th octet
11011100	0011_1011	DAT[7:0], cycle 30	MAC Client Data, 46th octet
10111111	1111_1101	DAT[7:0], cycle 31	FrameCheckSequence, 1st octet
10010011	1100_1001	DAT[7:0], cycle 31	FrameCheckSequence, 2nd octet
11110000	0000_1111	DAT[7:0], cycle 32	FrameCheckSequence, 3rd octet
01000111	1110_0010	DAT[7:0], cycle 32	FrameCheckSequence, 4th octet Canonical Format of FrameCheckSequence Field is FD-C9-0F-E2
/T/ End_Of_Packet	Internal PCS appends /T/ on transmit, strips on receive	Not transferred	End_Of_Packet: Physical packet only so not transferred on PL4 Bus

14.24 Frame Filtering

The PM5390 has simple programmable options to filter or forward ingress frames to the upstream link device. The PM5390 Receive Address Filtering Logic consists of eight exact-match MAC/VID filters, one 64-bin hash based multicast filter and four address filtering control registers that control the state of the forwarding for each filter. Each exact match filter includes one 48-bit MAC Address register and one 12-bit VID register that can be programmed through the microprocessor interface to the appropriate values. The filter logic is controlled by the four RXXG Address Filter Control registers. The host microprocessor has complete programmable access to all filtering features. Each address filter option is per-port independently programmable.

Downloaded by Content Team of Datasheet Inc on Wednesday, 07 October 2015 6:46:02 PM

14.24.1 Group Multicast Address Filtering

In parallel with the exact address match, the PM5390 performs multicast filter lookups. Within the PM5390 there resides a 64-bin hash based multicast filter consisting of one 64-bit mask register that is programmable from the Microprocessor interface (**RXXG Multicast Hash** register). This register is used in conjunction with a 6-bit value which is derived from bits [28:23] of the 32-bit CRC computed over the Destination Address. This 6-bit CRC value is used to index into the 64-bit mask register. The 64-bit mask register is used to determine if a multicast address that hashes to a given bin will be accepted for forwarding The 64-bin hash based multicast filtering is enabled by the MHASH_EN bit in the **RXXG Address Control 2** register. If the MHASH_EN bit is 0 then there is no hash based multicast filtering, however if MHASH_EN is 1 then hash based multicast filtering is enabled.

The multicast hash filter operation operates only on multicast-type frames: those with the IEEE Group/Functional bit set in the DA of the frame (least significant bit of the most significant byte of the MAC DA. The final forward versus filter decision for a frame is a combination of both the Group Multicast address filter result and the results from the eight possible exact match filter operations.

The 48-bit destination address of the received frame is passed through the standard 802.3 CRC function in the same order in which the destination address octets are received. Making reference to the 802.3 specification, section 3.2.8 Frame Check Sequence field, the CRC function generating polynomial and function is:

$$G(x) = x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^{8}+x^{7}+x^{5}+x^{4}+x^{2}+x^{1}+1$$

1. The first 32-bits of the frame (which is the first 32-bits of the destination address received) are complemented.

2. The 48 bits of the destination address are then considered to be the coefficients of a polynomial M(x) of degree 47

3. M(x) is multiplied by x^{32} and divided by G(x), producing a remainder R(x) of degree <= 31.

4. The coefficients of R(x) are considered to be a 32-bit sequence.

Bits [28:23] of the resultant 32-bit CRC remainder (call this crc_rem[28:23]) are used as the index into the MHASH[63:0] register. The result of the Group Multicast address filter is logically represented by the variable MHASH_ACCEPT:

MHASH_ACCEPT = (MHASH_EN == 1) & (MHASH[crc_rem[28:23]] ==1);

14.24.2 Exact Match Filter Operation

Each of the eight exact match filters on the RXXG has four bits of associated configuration. These are found in the Address Filter Control 1 register:

1. ADRFILT_CTRL[0] enables the exact match operation. If this bit is a logic 0 then the EXACT_MATCH operation returns a logic 0.

Downloaded by Content Team of Datasheet Inc on Wednesday, 07 February, 2018 - 6:57:16 PM

2. ADRFILT_CTRL[1] selects whether the source address or destination address of the received frame is used as the address for matching.

3. ADRFILT_CTRL2] enables the match function to also compare the VLAN Tag VID[11:0] field of the receive frame if the two bytes following the receive frame source address are equal to the VLAN Tag ID register

4. ADRFILT_CTRL[3] is a configuration bit that determines whether an exact match will affect the variable ACCEPT or DISCARD.

The exact match filter operation is a two-step process. The first step is to determine whether the address match criteria is logically true:

- EXACT_MATCH is logic 1 if the exact match filter is enabled and the selected frame address (and optional VID field of a VLAN tagged frame) are equal; otherwise, EXACT_MATCH is logic 0.

The second step is to set the EXACT_MATCH_ACCEPT or EXACT_MATCH_DISCARD variable for the given (one of eight) exact match filters based on the setting of ADRFILT_CTRL[3]:

- EXACT_MATCH_ACCEPT = EXACT_MATCH & (ADRFILT_CTRL[3] == 1);
- EXACT_MATCH_DISCARD = EXACT_MATCH & (ADRFILT_CTRL[3] == 0);

14.24.3 Address Filter ACCEPT / DISCARD Evaluation

The final result of the address filter function is a single filter versus forward decision. The result of the Group Multicast Address filter is combined with the result of the eight possible exact match filter operations to determine a final filter versus forward decision. The address filter logic can be configured so that a frame has a higher priority for being forwarded or filtered: this decision is based on the configuration bit PMODE in the Address Filter Control 2 register.

The results of the above filter operations are logically ORed together and then evaluated based on PMODE. Let EXACT_MATCH_ACCEPT[7:0] and EXACT_MATCH_DISCARD[7:0] represent the ACCEPT and DISCARD variables for the eight independent exact match filters respectively. The final combined value of ACCEPT and DISCARD for all address filters is logically:

- ACCEPT = (EXACT_MATCH_ACCEPT[7:0] != 0) | MHASH_ACCEPT;
- DISCARD = (EXACT_MATCH_DISCARD[7:0] != 0);

14.24.4 Address Filtering in Non-Promiscuous Mode

DISCARD has priority over ACCEPT in non-Promiscuous mode (PMODE a logic 0). A frame will be filtered only if ACCEPT is true and DISCARD is false. This is shown in the following table. It should be noted that if all filters are disabled, then all frames are filtered.

Downloaded by Content Team Engineering on Wednesday, 07 February, 2007 06:59:12 PM

Table 49 Address Filter Result in Non-Promiscuous Mode

PMODE	Discard	Accept	Result of Address Filter Function
0	0	0	Filter frame
0	0	1	Forward frame
0	1	0	Filter frame
0	1	1	Filter frame

14.24.5 Address Filtering in Promiscuous Mode

ACCEPT has priority over DISCARD in Promiscuous mode (PMODE a logic 1). A frame will be filtered only if DISCARD is true and ACCEPT is false. This is shown in the following table. It should be noted that if all filters are disabled, then all frames are accepted. See clause 5.2.4.3 of 802.3 standard, function LayerMgmtRecognizeAddress, for a reference to “promiscuous”.

Table 50 Address Filter in Promiscuous Mode

PMODE	Discard	Accept	Result of Address Filter Function
1	0	0	Forward frame
1	0	1	Forward frame
1	1	0	Filter frame
1	1	1	Forward frame

14.24.6 Address Filter Programming

The PM5390 frame filtering is programmed in the following manner.

1. Disable receive Ethernet traffic by setting RXEN0 bit to 0 in the RXXG Configuration Register.

   Note: When RXEN0 is set to 0 there is a possible wait time for a frame to complete being received since the disable is a graceful disable and will only disable the port during an IFG period.

2. Set the ADRFILT_CTL[0] to 0 (disable state) for all exact match filters that need to be programmed or changed, including the MHASH_EN if programming or changing the Multicast Hash Filters.

3. Program all desired filters with the desired contents.
   - Program the **RXXG Exact Match Address** and **RXXG Match VID** registers and respective **RXXG Address Control 0** or **RXXG Address Control 1** registers for the desired Exact match options.
   - Program the **RXXG Multicast Hash** register with the desired bit mask and enable by programming the **RXXG Address Filter Control 2** register.

4. Set the ADRFILT_CTL[0] to 1 (enable state) for all exact match filters that need to be enabled, including the MHASH_EN if enabling the Multicast Hash Filters.

Downloaded by ContentTeam of Chartmaster Inc on Wednesday, 07 February 2007 06:59:32 PM

5. Enable receive Ethernet traffic be setting RXEN0 bit to 1 in the RXXG Configuration Register

14.24.7 Receive Address Frame Filtering Byte Order

The address filtering registers are programmed a certain way to achieve an exact match on the DA or SA.

Assume a DA[47:0] = 0x01 0x02 0x03 0x04 0x05 0x06 where bit 40 of the DA[47:0] is the multicast bit.

The address filter register is broken up into three 16-bit registers labeled as HIGH[15:0], MID[15:0], and LOW[15:0].

A byte swap needs to be performed when programming the address filter registers. Hence:

HIGH[15:0] = 0x0605

MID[15:0] = 0x0403

LOW[15:0] = 0x0201

14.25 PAUSE Flow Control

The PM5390 allows 802.3 PAUSE frames to be transmitted out the egress MAC port based on three separate PAUSE frame catalysts. These conditions are discussed further in this section but first a general description of the PM5390 PAUSE frame generation is provided.

The Transmit PAUSE Control Frame logic responds to a Transmit PAUSE Control Request caused by one of these three catalysts:

- Internal ingress FIFO flow control (pause request based on IFLX FIFO fill level)
- External side-band PAUSE Request using the PAUSE and PAUSED pins.
- External host based PAUSE Request.

Each of the three catalysts, if enabled, are logically ORed together to form a transmit PAUSE control request to the TXXG associated with a specific channel.

The PM5390 responds by entering a Transmit PAUSE Frame State. After waiting for any current frame transmission to end, a MAC PAUSE control frame will be transmitted. The PAUSE control frame is formatted as follows:

Table 51 PAUSE Control Frame Format

Octets	Frame Field	Source of Information
7 Octets	Preamble	Auto-generated
1 Octet	SFD	Auto-generated

Downloaded by Content Team of Portonics on Wednesday, 07 February, 2007 06:53:32 PM

Octets	Frame Field	Source of Information
6 Octets	Destination Address	Auto-generated (01-80-c2-00-00-01) Note that DA[7:0] = 0x01, DA[15:8] = 0x80…etc.
6 Octets	Source Address	**TXXG Station Address** register. User defined (TXXG Station Address Registers 3047H, 3048H, 3049H)
2 Octets	Length/Type Field	Auto-generated (88-08)
2 Octets	Opcode Field	Auto-generated (00-01)
2 Octets	PAUSETimer Field	**TXXG PAUSE Timer** register: By default FF-FF. Defined by PAUSE_TIME[0..15], register 304DH.
42 Octets	PAD	Auto-generated
4 Octets	FCS	Auto-generated

The PAUSE frame is stitched together using register-based information and a series of auto-generated fields. As long as the PM5390 is in the Transmit PAUSE Frame State the TXXG will continually send PAUSE control frames every time the internal **TXXG PAUSE Timer Interval** (PAUSE_IVAL[15..0], register 304EH) counts down to zero. In this fashion the egress data-pipe will not be blocked for normal egress data traffic. The **TXXG PAUSE Timer** and **TXXG PAUSE Timer Interval** registers are both programmable. By default the **TXXG PAUSE Timer** register defaults to 0xFFFF and the **TXXG PAUSE Timer Interval** register defaults to 0xCFFF. Both are representative of the number of PAUSE Quanta used in the system. Note that PAUSE Quanta is defined as 512 bit times. The **TXXG PAUSE Timer Interval** will reload to the programmed state when it reaches zero. It is the responsibility of the PAUSE catalyst to hold the input to the TXXG until normal ingress traffic can be resumed. When the catalyst removes the request for PAUSE the TXXG will send out a PAUSE Control frame with the PAUSE timer value of zero.

The three different PAUSE frame catalysts are discussed in more detail below.

14.25.1 Internal Ingress FIFO Flow Control

The POS-PHY ingress FIFO logic (IFLX) has a per-channel, programmable almost-full threshold: register **IFLX Indirect Full/Almost Full Status & Limit** (indirect register 2210H) . When the ingress FIFO fill level for the logical FIFO exceeds the programmed almost-full threshold value an ***internal*** PAUSE flow control request signal is asserted to the TXXG. The TXXG can be programmed to accept POS-PHY ingress FIFO PAUSE flow control requests for egress traffic if the **FCTX** bit is set in the **TXXG Configuration register 1** (register 3040H). When enabled and the internal FIFO PAUSE flow control signal is asserted the TXXG will commence sending 802.3 PAUSE frames. The IFLX logic continues to hold the internal FIFO PAUSE flow control request signal to the TXXG until the FIFO fill level for the logical FIFO of that channel is below the almost-empty threshold value programmed in the **IFLX Indirect Empty/Almost Empty Status & Limit** register (indirect register 2211H). At this time the internal FIFO PAUSE flow control request signal is de-asserted informing the TXXG to cease PAUSE frame flow control by sending a PAUSE Control frame with the PAUSE timer value of zero.

The almost full threshold field (AFTH[9:0]) and almost empty threshold field (AETH[9:0]) in the IFLX registers are in terms of the number of 128-bit words that can be held in the logical FIFO.

Downloaded by [illegible] on Wednesday, 01 February, 2006, 06:52:[illegible] PM

14.25.2 External Side-Band PAUSE Request

The PM5390 has a sideband PAUSE request signal or PAUSE pin. Asserting the PAUSE signal (active high) places the TXXG into a Transmit PAUSE Frame State. The PAUSE signal is to be asserted and held as long as MAC Control PAUSE frames are required to be transmitted from the TXXG. When normal frame reception is desired the PAUSE signal is de-asserted. Upon de-assertion a MAC Control frame with the PAUSE timer value of zero will be transmitted.

The PL4 Bus protocol and implementation of the output scheduling done by the PM5390 device using the PL4MOS does not require intervention by an external agent to support low-level flow control and support of non-blocking operation. The PAUSE signal is provided to allow an external agent to indicate a "coarse" level of flow control independent of that provided by the internal ingress FIFO flow control mechanism.

14.25.3 External Host Based PAUSE Request

The PM5390 allows an external microprocessor to set a register bit to initiate a PAUSE flow control request on a per-channel basis. This is done via the **HOSTPAUSE** bit in the **TXXG Configuration 1 register**, (register 3040H). When the **HOSTPAUSE** bit is set to logic 1 the TXXG is placed in a Transmit PAUSE Frame State. When normal frame reception is desired the HOSTPAUSE register bit is de-asserted by setting it to logic 0. Pause frames are formatted based on the PAUSE_TIME[15..0] value (register 304DH) and the PAUSE_IVAL[15..0] value (register 304EH). Upon de-assertion of HOSTPAUSE a MAC Control frame with the PAUSE timer value of zero will be transmitted.

The PL4 Bus protocol and implementation of the output scheduling done by the PM5390 device using the PL4MOS does not require intervention by an external agent to support low-level flow control and support of non-blocking operation. The HOSTPAUSE register bit is provided to allow an external agent to indicate a "coarse" level of flow control independent of that provided by the internal ingress FIFO flow control mechanism.

14.25.4 Reception of 802.3 PAUSE Frames

As per the 802.3-2000 standard a valid PAUSE frame shall contain following for the PM5390 to respond to the received PAUSE MAC Control Frame:

1. The globally assigned 48-bit multicast address (01-80-C2-00-00-01) or the unicast station address of the MAC.

2. The LENGTH/TYPE field = 8808

3. The PAUSE Opcode of 0001

4. A non-zero value in the PAUSE timer field

As per the 802.3-2000 standard only the LENGTH/TYPE field and the Opcode is needed to increment the PAUSEMACCtrlFramesReceived, regardless of the DA field.

Downloaded by Content Team of PMC-Sierra, Inc. on Wednesday, 27 February, 2008 06:51:17 PM

The PM5390 can be programmed to handle ingress PAUSE control frames in the manner as outlined below. This programming is done via the **PARF** bit in the **RXXG Configuration 1 register** (register 2040H) and the **FCRX** bit in the **TXXG Configuration 1** register (register 3040H). The **PARF** bit programs whether or not control frames are passed to the upper layer device. The **FCRX** bit allows the MAC Control sub-layer to respond to a received PAUSE Control frames by pausing the transmitter from transmitting data frames (this response is referred to as "executed" in the following table).

Table 52 PAUSE Frame Programmable Control

PARF	FCRX	PM5390 Action
0	0	PAUSE Frames are ignored and dropped at the PM5390 level.
0	1	PAUSE Frames are executed but are not passed to the upper layer.
1	X	PAUSE Frames are ignored and forwarded to the upper layer device.

Please note as per 802.3-2000 that if the PM5390 is currently executing reception of a PAUSE frame and is currently blocking the data-path from transmission of MAC Data frames (i.e. normal data traffic) that MAC Control PAUSE frames can still be sent. While the TXXG has PAUSED transmission of data frames, the PAUSED pin will be asserted high.

14.26 Ethernet MAC Receive FIFO Overrun Condition

The 802.3 specification defined MAC Control PAUSE frames to inhibit transmission of MAC Data frames between two full-duplex peer Ethernet devices across the Ethernet media. However, support of Ethernet MAC Control PAUSE frames by a device that is a peer of the PM5390 device is an optional feature and so is not guaranteed to be supported on the peer device. In addition, a given application may use the PM5390 device in a manner that does not guarantee loss-less flow control (as described elsewhere in the Operation section, loss-less flow control is a function of the round-trip length of the fiber between the peer Ethernet devices, the maximum frame size of the application, the provisioned amount of buffer space in the PM5390 device for the channel, and the response time of the peer device to the PAUSE frame request and subsequent cessation of frame transmission). This section describes the behavior of the PM5390 Ethernet MAC (RXXG) to a receive FIFO overrun condition.

The response of the Ethernet MAC receive FIFO to a overrun condition depends upon whether any of the data from the frame has been transferred to the downstream ingress FIFO. As mentioned earlier, frame data transfer from the RXXG receive FIFO can start either at an End-Of-Frame indication or when the number of bytes in the frame exceeds the **RXXG Receive FIFO Threshold**.

An Ethernet MAC receive FIFO overrun condition occurs if the FIFO is full and data continues to be received from the XSBI interface(this would be data from within an Ethernet MAC Data frame). The actual FIFO buffer used by the RXXG receive logic does not overflow: the internal pointers used for determining the location in the FIFO to read and write are prevented from actually overrunning. Instead frame data is discarded until there is sufficient buffer space in the receive FIFO for the next frame and reception of subsequent frames resumes on a Start-Of-Frame boundary.

Downloaded by Circuit Test Services Pty Ltd (circuittest@ozemail.com.au) on 07 August 2007 06:50:07 AM

Frame Data Transfer To Ingress FIFO Had Not Started When Ethernet MAC Receive FIFO Overrun Occurs

The receive control logic in the RXXG is responsible for the detection and recovery from a receive FIFO overrun condition. If the overrun is detected before any data from the frame is transferred to the ingress FIFO (which will always be the case if the received frame size is less than the **RXXG Receive FIFO Threshold)** the receive control logic will flag the frame as an overrun frame and it will be discarded in its entirety without being transferred to the ingress FIFO. This is a countable event in the MSTATS receive counter FramesLostDueToInternalMACError. The RXXG will re-synchronize to the next start of a physical packet (preamble/SFD delimiter) and continue Ethernet frame reception. If a receive FIFO overrun condition occurs again, the response of the RXXG is identical to that described above until there is sufficient buffer space to accept either the entire frame or until the number of bytes of the received frame exceeds the **RXXG Receive FIFO Threshold.** Note that reception resumes on a Start-Of-Frame boundary.

Frame Data Transfer To Ingress FIFO Started When Ethernet MAC Receive FIFO Overrun Occurs

In the case that the receive FIFO has started transferring data when the overrun condition occurs, the receive control logic will flag the frame in transfer as an overrun frame and discard all subsequent data from the frame until the next Start-Of-Frame boundary is detected. The frame in transfer when the overrun condition occurs (which is after the **RXXG Receive FIFO Threshold** has been exceeded), will assert an internal receive error status signal to the ingress FIFO. On the PL4 Bus output interface (device pins RDAT[15:0]+/-, RCTL+/-) the frame will be truncated at the location that the overrun occurred within the RXXG receiver and the frame will be marked as erred by having a PL4 End-Of-Packet status of ABORT.

As discussed previously, this is a countable event in the MSTATS receive counter FramesLostDueToInternalMACError. The RXXG will re-synchronize to the next start of a physical packet (preamble/SFD delimiter) and continue Ethernet frame reception. If a receive FIFO overrun condition occurs again, the response of the RXXG is identical to that described above until there is sufficient buffer space to accept either the entire frame or until the number of bytes of the received frame exceeds the **RXXG Receive FIFO Threshold.** Note that reception resumes on a Start-Of-Frame boundary.

14.27 Transmit PCS - T64B66B

14.27.1 Initialization

The T64B66B will leave the reset state on de-assertion of the RSTB input. During reset, all state-machines are initialized and the internal FIFO read and write pointers are reset. Any information that was held in the FIFO is unreliable and unusable. All programmable registers are initialized to their default value.

~~14.27.2 Monitoring~~

~~Error status will be indicated in the **T64B66B Interrupt Status** register. Also transmit activity can be read from the **T64B66B Status** register.~~

Downloaded by Cortex Team of PMC-Sierra on Wednesday, 07 February 2007 05:51:02PM

14.28 Transmit PCS Layer Error Handling

This section describes the behavior of the TX PCS during error conditions and during a fault condition. The TX PCS conforms to the 802.3ae standard for all error and fault conditions as described in Clauses 49 and 46 of the 802.3ae standard.

The possible error conditions that exist are: Transmit State Machine Errors, MAC transmit errors, Loss of sync from the RX PCS, HI_BER from the RX PCS.

The possible fault conditions are Local Fault or Remote Fault.

The sections to follow will describe that details of the error conditions and the fault conditions.

14.28.1 Receive State Machine Errors

The TX PCS follows the Transmit State Machine in Figure 49-14 of 802.3ae. When the Transmit State Machine transitions to TX_E (Error state), the TX PCS will insert the 66-bit ERROR code as defined by the 802.3ae.

14.28.2 MAC Transmit Errors

The TX PCS will also insert the 66-bit ERROR code when the TX MAC asserts the SYSTEM_ERROR signal. The SYSTEM_ERROR signal is asserted when the TX MAC has encountered an error.

14.28.3 Loss of Sync From The RX PCS

When the RX PCS encounters a loss of sync the TX PCS will treat this as a Local Fault condition. When in a Local Fault condition the TX PCS will hold off data from the TX MAC and stream out the Remote Fault code alternating between IDLE's and Remote Fault until the Local Fault condition is cleared.

14.28.4 HI BER From The RX PCS

When the RX PCS encounters a High Bit ERROR the TX PCS will treat this as a Local Fault condition. When in a Local Fault condition the TX PCS will hold off data from the TX MAC and stream out the Remote Fault code alternating between IDLE's and Remote Fault until the Local Fault condition is cleared.

14.28.5 Local Fault Received From The RX PCS

When the RX PCS receives the Local Fault code the TX PCS will treat this as a Local Fault condition. When in a Local Fault condition the TX PCS will hold off data from the TX MAC and stream out the Remote Fault code alternating between IDLE's and Remote Fault until the Local Fault condition is cleared.

Downloaded by Circuit Team Northwest on Wednesday, 07 February 2007 00:59:37 PM

14.28.6 Remote Fault Received From The RX PCS

When the RX PCS receives the Remote Fault code the TX PCS will treat this as a Remote Fault condition. When in a Remote Fault condition the TX PCS will hold off data from the TX MAC and stream out IDLE's until the Remote Fault condition is cleared.

14.29 POS-PHY Level 4 Introduction

The PM5390 device, one of PMC-Sierra's 10 Gigabit physical layer devices, utilizes the POS-PHY Level 4 system interface to provide a common interface across multiple devices supporting various protocols and rates with an aggregate throughput 9.953 or 10 Gbit/s.

The POS-PHY Level 4 system interface consists of a pair of 16 bit data paths and a pair of 2 bit FIFO status paths. For a detailed description of this interface please refer to the POS-PHY Level 4 specification.

PMC-Sierra's POS-PHY Level 4 interface data paths typically operate at 622 to 700 Mbit/s with LVDS I/O. Both transmit and receive data paths operate at the same frequency (*i.e.* RDCLK frequency = TDCLK frequency).

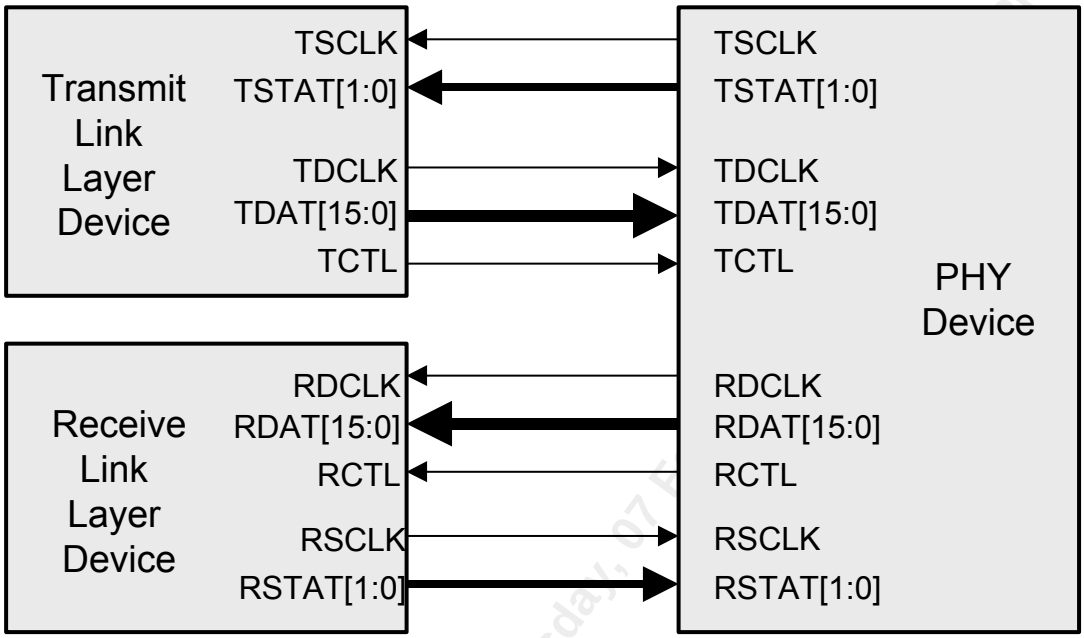
PMC-Sierra's POS-PHY Level 4 interface FIFO status paths typically operate at $1/8^{th}$ the data path-rate with LVTTL I/O. The transmit FIFO status path can operate at any speed up to $1/8^{th}$ the data path rate. The receive FIFO status path operates at $1/8^{th}$ the data path rate.

The terms 'egress', 'transmit', 'ingress' and 'receive' denote the system relative flow of status or data across the POS-PHY Level 4 interfaces whereas the terms 'in', 'input', 'out' and 'output' denote the device relative flow of status or data across the device interfaces.

Figure 42 shows the relationships between devices communicating via the POS-PHY Level 4 interface. On the PM5390, the transmit interface consists of TSCLK / TSTAT outputs and TDCLK / TCTL / TDAT inputs, and the receive interface consists of RSCLK / RSTAT inputs and RDCLK / RCTL / RDAT outputs. For link layer devices the transmit interface consists of TSCLK / TSTAT inputs and TDCLK / TCTL / TDAT outputs, and the receive interface consists of (optional) RSCLK / RSTAT outputs and RDCLK / RCTL / RDAT inputs.

Downloaded by Content Team of Parts Group LLC on Monday, 07 February, 2011 06:59:32 PM

Figure 42 POS-PHY Level 4 Interfaces



14.30 POS-PHY Level 4 Clocking

14.30.1 POS-PHY Level 4 Clocking Modes

PMC-Sierra's POS-PHY Level 4 interface supports two data path-clocking modes: a master and a slave mode. In master mode, the PMC-Sierra physical layer device (PHY) derives the PL4 clock from reference input (REFCLK) and provides clocking to the customer ASIC. In slave mode, the PHY derives the PL4 clock from the transmit data clock (TDCLK) received from the customer ASIC.

The choice between master and slave clocking modes depends on board design considerations and the jitter performance expected on the customer ASIC device.

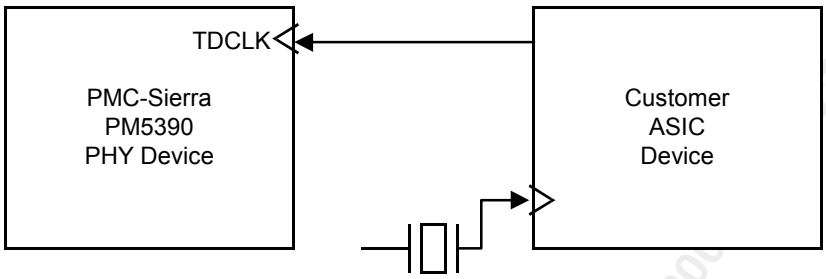
14.30.2 Slave Clocking Mode

When in Slave clocking mode the PMC-Sierra PHY derives its data clocks from the transmit data clock (TDCLK) received from the customer ASIC device.

Figure 43 shows a PMC-Sierra PHY device connected to a customer ASIC device in slave clocking mode.

Downloaded by Content Team of Partminer.com on Wednesday, 07 F

Figure 43 POS-PHY Level 4 Slave Clocking

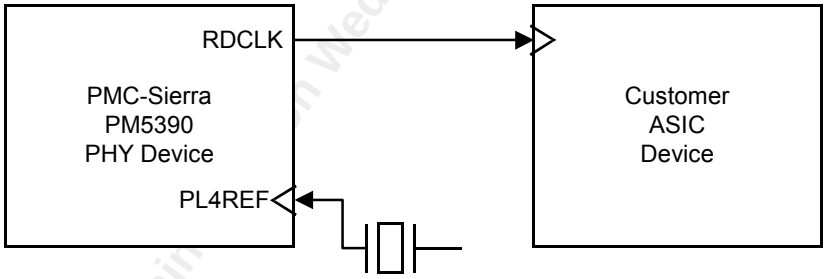


Master Clocking Mode

When in Master clocking mode the PMC-Sierra PHY derives its data clocks directly from an external reference clock (REFCLK) and provides a frequency reference to the customer ASIC device via the receive data clock (RDCLK).

Figure 44 shows a PMC-Sierra PHY device connected to a customer ASIC device in master clocking mode.

Figure 44 POS-PHY Level 4 Master Clocking Mode



14.30.3 POS-PHY Level 4 Clock Mode Configuration

This section describes how to configure the clocking mode for PMC-Sierra's POS-PHY Level 4 interface.

The choice of clocking mode is indicated to the PMC PHY device by the REFSEL[0] input pin on the device as follows:

0 = Slave mode (TDCLK is the frequency reference)

1 = Master mode (REFCLK is the frequency reference)

In slave mode the availability of the transmit data clock (TDCLK) is indicated to the PMC PHY device by the REFSEL[1] input pin on the device as follows:

Downloaded by Content Team @ Portmin... on Wednesday, 17 February, 200... 2:32 PM

0 = TDCLK is valid when the RSTB pin is de-asserted (immediate mode) Clock initialization proceeds automatically.

1 = TDCLK is not valid when the RSTB pin is de-asserted (deferred mode) Software intervention is required to complete clock initialization.

In master mode the frequency of the reference clock (REFCLK) is indicated to the PMC PHY device by the REFSEL[1] input pin on the device as follows:

0 = ½ the data rate (311.04 to 350 MHz)

1 = ¼ the data rate (155.52 to 175 MHz)

In master mode the REFCLK must be available when the RSTB pin is de-asserted (*i.e.* there is no deferred master mode).

The REFSEL settings must not change after the RSTB pin is de-asserted.

PL4 Data Alignment modes (Dynamic versus Static)

The input data path of the PM5390 (TCTL+/- and TDAT[15:0]+/- pins) only supports the PL4 Bus specification dynamic alignment mode. This requires that the peer PL4 device must send the PL4 training sequence at a certain minimum rate. The minimum rate is TBD and will be discussed in a referenced application note. It is also required that the peer PL4 device comply to the dynamic mode jitter specifications that will also be referenced in the application note.

14.31 POS-PHY Level 4 Initialization

Initialization of PMC-Sierra's POS-PHY Level 4 interface proceeds in several phases:

1. Device reset (previously discussed)
2. Clock acquisition
3. Training
4. Configuration
5. Enabling

These phases represent the conceptual initialization sequence. Depending on the configured mode of operation there may be some overlap between phases.

14.31.1 Clock Acquisition

Clock acquisition begins during device reset with the de-assertion of the RSTB pin. In immediate (master or slave) mode the selected reference clock (REFCLK or TDCLK) should be valid at this point, and the CSU will begin training to the supplied reference frequency.

Downloaded by Content Team of Partminer Inc. on Wednesday, 07 February, 2007 06:59:32 PM

In deferred (slave) mode the transmit data clock (TDCLK) input should be active but may not be operating at the correct frequency, *e.g.* because it is being driven from a CSU which is still in frequency acquisition. In this case the training of the slave CSU should track the training of the master CSU with a moderate amount of time lag.

Completion of clock acquisition is determined by monitoring the frequency of the CSU relative to the transmit data clock (TDCLK) in both slave and master modes, and relative to the reference clock (REFCLK) in master mode only. In immediate (master or slave) mode the frequency lock detection functions are enabled immediately upon de-assertion of the device internal digital reset. At this point the CSU should be properly trained to the selected reference frequency. The frequency lock detection functions should indicate reference in-lock within 500ms after the device internal digital reset is de-asserted.

In deferred (slave) mode the output of the lock detect function must be ignored until the master device is driving a valid frequency reference (TDCLK) into the slave device, and the slave CSU has had time to acquire frequency lock. This is accomplished by automatically setting two configuration flags (TRAIN_DIS and ODAT_DIS) at reset time when REFSEL[1:0] = 10, and delaying the training phase until software clears these flags, as described below.

14.31.2 Training

Both the transmit data path (TCTL / TDAT) and the receive data path (RCTL / RDAT) are de-skewed during this phase. During training the output end of the data path continuously sends the training pattern defined in the POS-PHY Level 4 standard (10 Training Control Words / 10 Training Data Words) to the input end.

Training proceeds somewhat independently in each direction. Transmit data path training begins when the TRAIN_DIS flag is cleared (by the device in immediate mode or by software in deferred mode) and the frequency lock detect function indicates that the CSU is locked to the transmit data clock (TDCLK), and in master mode only to the reference clock (REFCLK). During training the input data de-skew function aligns the 17 parallel bit lanes of the transmit data interface to each other. The transmit data alignment function should indicate data in-lock within 6 µs after transmit data path training begins when a valid training pattern is present at the transmit data interface (TCTL / TDAT). Transmit data path training continues until the transmit data path is enabled, as described below.

Receive data path training begins when the ODAT_DIS flag is cleared (by the device in immediate mode or by software in deferred mode) and the frequency lock detect function indicates that the CSU is locked to the selected frequency reference (TDCLK or REFCLK). During training the device continuously generates the training pattern at the receive data interface (RCTL / RDAT) to allow the input end of the interface in the peer device to properly de-skew. Receive data path training continues until the receive data path is enabled, as described below.

14.31.3 Configuration

The operation of PMC-Sierra's POS-PHY Level 4 interface requires several configuration parameters, including:

1. Highest channel number used by the device (Calender_Len)

Downloaded by Conrad Electronic Wednesday, 07 February, 2007, 16:09:32

2. Transmit and receive FIFO allocations and thresholds for each channel.

3. Receive data scheduling parameters (Max_Burst1, Max_Burst2, Max_Transfer)

4. Receive training scheduling parameters (Data_Max_T, Alpha)

5. Optional disabling of receive FIFO status channel (NO_STATUS flag)

It is recommended that parameters be configured in the order shown to avoid anomalous behavior. Rules for setting the PL4 Bus configuration parameters is described in a later section.

14.31.4 Enabling

Enabling proceeds somewhat independently in each direction. After configuring all transmit interface parameters software must clear the OSTAT_DIS flag. (As described in the training phase, the TRAIN_DIS flag must also have been cleared automatically or by software.) Normal operation of the transmit FIFO status and data interfaces commences when the OSTAT_DIS flag is cleared and the transmit data alignment function indicates data in-lock.

After configuring all receive interface parameters software must either set the NO_STATUS flag or clear the ISTAT_DIS flag. (As described in the training phase, the ODAT_DIS flag must also have been cleared automatically or by software.) Normal operation of the receive FIFO status interface commences when the ISTAT_DIS flag is cleared and the receive status alignment function indicates status in-lock. Normal operation of the receive data interface commences when the NO_STATUS flag is set or the receive status alignment function indicates status in-lock.

14.31.5 PL4 Bus Configuration Parameters

The PL4 Bus specification specifies a number of startup parameters that are configurable, either on a per-channel basis or on a per-interface basis. All of the PL4 Bus configuration parameters can be accessed via the microprocessor interface of the PM5390 device.

PL4 Bus CALENDAR_LEN

The PL4 Bus CALENDAR_LEN parameter is represented by the TOP_CHAN[3:0] field (plus 1) of the **PM5390 System-side Configuration** register. The PM5390 device supports 1 or 4 internal pipes, and TOP_CHAN[3:0] is set to 0 or 3 respectively, thus CALENDAR_LEN will be 1 or 4.

PL4 Bus MaxBurst1 and MaxBurst2 for Receive

The PL4 Bus MaxBurst1 parameter is held in the **PL4MOS MaxBurst1** register. On the PM5390 device **PL4MOS MaxBurst1** can take the value 8 to 4095 and represents a credit amount in blocks of 16 bytes.

Likewise, the PL4 Bus MaxBurst2 parameter is held in the **PL4MOS MaxBurst2** register and can take the value 8 to 4095. It also represents a credit amount in blocks of 16 bytes.

Downloaded by Content Team Chairman Group on Wednesday, 01 February, 2006, 06:59:32 PM

As per the PL4 Bus specification, MaxBurst1 is to be programmed to be either higher than or equal to the value than MaxBurst2. On the PM5390 device there is no hardware bounds checking to ensure that this configuration requirement is met.

The selection of MaxBurst1 and MaxBurst2 in a system application is related to the size of the receive buffering.

PL4 Bus Maximum Burst Length (MAX_TRANSFER)

MAX_TRANSFER determines the maximum length of a PL4 data burst. The Maximum DataBurst Length parameter for output data (PM5390 device RDAT[15:0] and RCTL) is held in the **PL4MOS Transfer Size** register as MAX_TRANSFER[7:0]. MAX_TRANSFER defines the maximum size in a PL4 DataBurst in terms of 16-byte data blocks for the single pipe. The register is implemented so that the low two bits are read-only and hardwired to 2'b00, thereby constraining the configurable size to be modulo 4 (or at a 64-byte boundary). For example, a MAX_TRANSFER value of 8 limits the PL4 DataBurst to transfers of at most 128 bytes or, equivalently, 64 PL4 Bus cycles.

The Maximum Burst Length parameter for incoming data (device pins TDAT[15:0] and TCTL) is not held on the PM5390 and there is no requirement that the value of the parameter in the ingress and egress directions be the same. The Maximum Burst Length parameter for incoming data can range from 32 to 1024 bytes, in increments of 32 bytes.

Note that for ATM cell transfer across the PL4 interface, the recommended value of MAX_TRANSFER[7:0] is 4, not the default of 8. Changing this default reduces the amount of lost credit during each cell. MAX_BURST1 and MAX_BURST2 should be left at 8.

PL4 FIFO Threshold Issues

Appendix C of the PL4 Bus specification discusses the FIFO status bandwidth requirements and FIFO threshold issues. Further details are provided below as they apply to the PM5390 device.

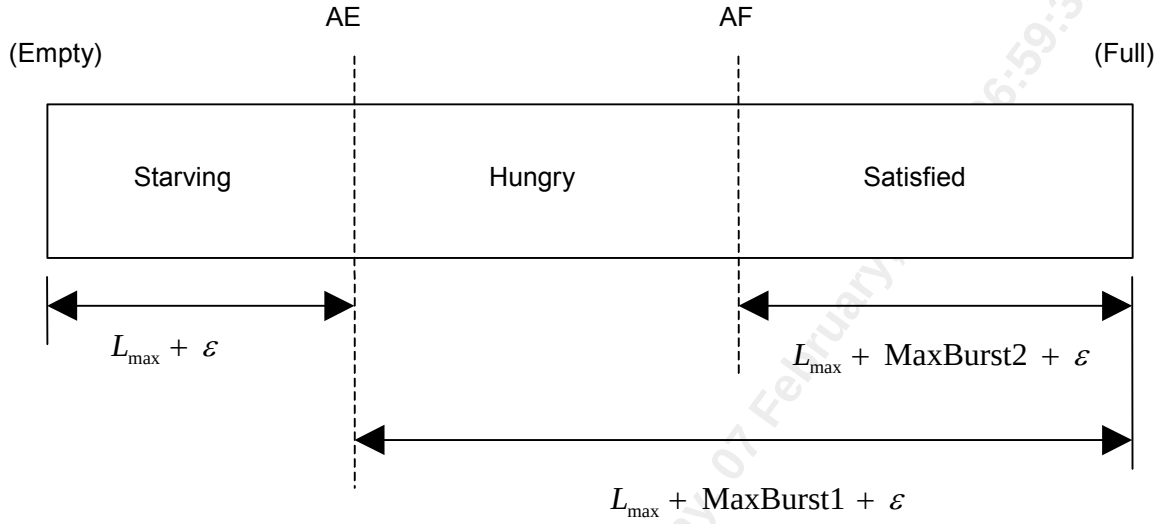
The thresholds for STARVING and HUNGRY in the peer PL4 device are set such that the peer FIFO can accept at least MaxBurst1 and MaxBurst2 (16-byte) blocks respectively, plus an additional amount to account for feedback-response delay. In order to guard against potential buffer underflow (which could affect total receive throughput if the sink device is unable to drain its FIFO at a rate greater than the line rate), the lowest threshold must be set high enough to allow the other end to respond to transitions to the state of lowest FIFO occupancy in a reasonable length of time (to the order of the status update interval, plus scheduler response time). MaxBurst2 and MaxBurst1 (if applicable) must be provisioned to allow adequate utilization of transfer bandwidth between status updates for the given port.

Figure 45 shows one possible way for relating worst-case FIFO thresholds to MaxBurst1 and MaxBurst2 as well as the response latency. For receive the receive and transmit directions, Lmax and epsilon can take different value. Lmax corresponds to the worst-case response time, starting from the delay in receiving a status update over the FIFO status channel, and observing the reaction to that update on the corresponding data path. The margin, epsilon, is an implementation-specific quantity that accounts for differences between the calculated/designed and actual Lmax. The actual Lmax number will be determined and specified be for release.

Downloaded by Element14 (Farnell Inc) on Mon Feb 27 2017 06:59:22 PM

Figure 45 Sample FIFO Thresholds

(AE = Almost Empty waterline, AF = Almost Full waterline)



The contribution to Lmax by the PM5390 device in the receive direction (data flow on RDAT pins) is approximately (2*MAX_TRANSFER + 512 bytes).

PL4 Bus SOP-to-SOP Spacing Rule

The PL4 Bus parameter that specifies the Start-Of-Packet to Start-Of-Packet spacing rule for output data is held in the **PL4ODP Configuration** register SOP_RULE field. The PM5390 supports a configurable minimum SOP-to-SOP spacing of 2 or 8 PL4 Bus cycles on the output data (PM5390 device RDAT[15:0] and RCTL).

For PL4 Bus input data (TDAT[15:0] and TCTL) the PM5390 device requires a minimum SOP-to-SOP spacing rule of 4. There is no register on the PM5390 device that holds this parameter in the input data direction.

PL4 Bus MaxBurst1 and MaxBurst2 for Transmit

The MaxBurst1 and MaxBurst2 parameters for input data are not held on the PM5390 device. These parameters are required to be implemented either as a programmable or fixed value on the peer PL4 device that sources data on the PL4 Bus TDAT[15:0] pins.

The value of MaxBurst1 and MaxBurst2 for input data and output data do not have to be equal.

PL4 Bus CALENDAR_M

The PL4 Bus CALENDAR_M parameter is represented by the IN_MUL[7:0] and OUT_MUL[7:0] fields of the **PL4IO Calendar Repetitions** register.

Downloaded by Content Management Portal on Wednesday, 07 February, 2007 6:59:32 PM

The number of repetitions of the input FIFO status channels (impressed on PM5390 device input pins RSTAT[1:0]) within a complete status calendar sequence is controlled by IN_MUL. The PL4 input status parameter CALENDAR_M = IN_MUL + 1. The total length of the input status calendar sequence = CALENDAR_LEN x CALENDAR_M. IN_MUL must be changed while the input status interface is disabled in the **PL4IO Configuration** register. The result of changing IN_MUL while the status interface is enabled is unspecified. IN_MUL can take the value 1 to 255 if the input FIFO status channel is enabled. As per the PL4 Bus specification, the input FIFO status channel is optional, but will only reflect a single channel status on the PM5390.

The number of repetitions of the output FIFO status channels (impressed on the PM5390 device output pins TSTAT[1:0]) within a complete status calendar sequence is controlled by OUT_MUL. The PL4 output status parameter CALENDAR_M = OUT_MUL + 1. The total length of the output status calendar sequence = CALENDAR_LEN x CALENDAR_M. OUT_MUL must be changed while the output status interface is disabled in the **PL4IO Configuration** register. The result of changing OUT_MUL while the status interface is enabled is unspecified. OUT_MUL can take the value 1 to 255.

Note that for single channel operation with small data transfers such as ATM cells, then it is recommended to use calendar repetition value of greater than 1 (i.e. OUT_MUL = IN_MUL = 2, or more). This will improve the overall efficiency of the interface.

PL4 Bus MAX_CALENDAR_LEN

The maximum supported value for MAX_CALENDAR_LEN follows from the maximum supported value of both CALENDAR_LEN and CALENDAR_M:

MAX_CALENDAR_LEN= max(CALENDAR_LEN) x max(CALENDAR_M);

= 10 x 256 = 2560;

PL4 Bus FIFO_MAX_T

The PL4 Bus parameter FIFO_MAX_T is the product of CALENDAR_LEN and CALENDAR_M.

PL4 Bus DATA_MAX_T

As per the PL4 Bus specification, “For the data path de-skew procedure, DATA_MAX_T is configured only on the sending side of the data paths on the transmit and receive interfaces. DATA_MAX_T need not be identical over both interfaces.”

The PL4 Bus DATA_MAX_T parameter for the output data path is held in the **PL4ODP MAX_T** register. MAX_T[11:0] defines the bounded time interval over which the PL4 training sequence is to be sent. The value of MAX_T is in terms of 1024 PL4 Bus cycles. A value of 0 in the MAX_T register disables the sending of the training sequence (no training patterns sent).

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 6:09:32 PM

Although any integer value of MAX_T can be programmed, in order to maintain the non-blocking operation of the PM5390 a maximum of 0.1% of the PL4 bus cycles should contain a forced training data pattern or training control pattern. This limits the lowest practical value for which MAX_T can be programmed (if non-zero) to 16; for a α value of 1, this would imply that at a minimum the 20 cycle training pattern would be sent every 1000 - 4000 PL4 Bus cycles.

PL4 Bus Data Training Sequence Repetitions (α)

The PL4 Bus parameter α that specifies the number of back-to-back training patterns that define a training sequence for outgoing data (PM5390 device RDAT[15:0] and RCTL) is held in the **PL4ODP Configuration** register REPEAT_T[3:0] field. Numerically:

$$\alpha = \text{REPEAT\_T} + 1;$$

where α can take the value of 1 to 16.

For incoming data (PM5390 device TDAT[15:0] and TCTL) the value of α is not held. For correct operation of the PM5390 input deskew logic, α can take on any value greater than or equal to 1.

Operation with PL4 Bus Receive FIFO Status Unimplemented

The PM5390 device supports the PL4 Bus specification requirement that the receive FIFO status is optional. In the event that the peer PL4 sink device does not implement the receive FIFO status, the NO_STATUS bit in the **PL4MOS Configuration** register is to be written to a logic 1 prior to enabling the PL4MOS (which is done by writing PL4MOS_EN to a logic 1). In this case, each of the channels in the PM5390 is assigned an infinite credit. The scheduler on the PL4MOS works as previously described but with an implied FIFO status of HUN (hungry) for all enabled channels. In addition, the NO_ISTAT bit in the PL4IO Configuration register is to be written to a logic 1 after initial configuration.

14.32 ATM, POS, 10 Gigabit Ethernet Format on Line and PL4 Interfaces

The bit/byte transmission/reception order for ATM cell, POS packet or 10 Gigabit Ethernet Frame payload on the Line and PL4 interfaces are described in Application Notes, PMC-2010559, “S/UNI 9953 and S/UNI-1x10GE Frequently Asked Questions”.

14.33 Management Data Interface (MDIO)

A master MDIO interface is implemented in the PM5390. MDIO operation is driven via the following PM5390 registers:

Downloaded by Content Team (Partnernet) on Wednesday, 07 February, 2007 06:59:32 PM

S/UNI 9953 MDIO Command (0018H)
S/UNI 9953 MMD PHY Address (0019H)
S/UNI 9953 MMD Control Address Data (001AH)
S/UNI 9953 MDIO Read Status Data (001BH)
S/UNI 9953 PCS/LAN/MDIO Interrupt Enable and Control (001CH)
S/UNI 9953 PCS/LAN/MDIO Interrupt Status (001DH)
S/UNI 9953 PCS/LAN/MDIO Status (001EH)

When a load write data command (LCTLD), load address command (LCTLA), Read Status Command (RSTAT) or a Read Increment (RDINC) is detected from the host via programming of the S/UNI 9953 MDIO Command register, the corresponding MDIO sequence is initiated.

Before initiating an MDIO read/write sequence, the relevant port address and device address of the target MMD PHY must be programmed via the S/UNI 9953 MMD PHY Address register. For a write operation, the control address or data must also be setup in the S/UNI 9953 MMD Control Address Data register prior to sequence initiation.

Upon receiving a write or read command, the MDIO interface issues a BUSY signal (setting MDIO_BUSY bit in the S/UNI 9953 PCS/LAN/MDIO Status register high) to inform the host to insert wait states while the write or read operation is in progress. The BUSY signal is de-asserted when the write or read operation is completed. The host may chose to be informed by polling the BUSY signal (MDIO_BUSY bit) or via interrupt by setting the MDIO_BUSYE bit in the S/UNI 9953 PCS/LAN/MDIO Interrupt Enable and Control register. After the completion of a read sequence, the host may access the result via the S/UNI 9953 MDIO Read Status Data register.

14.34 WAN Interface Sub-layer (WIS) Test Patterns

The generator can transmit a square wave pattern (over the entire SONET frame), a mixed frequency test pattern, or a continuous PRBS-23 pattern in the SPE depending on the register configuration. The pattern checker verifies the B1, B2, B3 bytes in the mixed frequency test pattern frame and the continuous PRBS-23 pattern frame, and also monitors a continuous PRBS-23 pattern in the SPE.

When using the WIS test pattern generator, TREQ_ADVANCE[6:0] in the S/UNI 9953 Transmit Control and Clock Enable Register 0004H should be set to 72 decimal.

14.34.1 Test Pattern Generation

The test pattern to be generated is selected using the S/UNI 9953 System-side Configuration register 0002H.

The square wave test pattern consists of 8 logic zero bits followed by 8 logic one bits. The SONET blocks do not perform any framing and the square wave pattern is transmitted by the XSBI interface.

Downloaded by Intel Team of Parcil Inc on Wed Feb 15, 2017 06:59:32 PM

The mixed frequency test pattern and the continuous PRBS-23 pattern consist of a PRBS generator and a SONET transmit frame counter. In the mixed frequency test pattern mode, a Test Signal Structure (TSS) that consists of 2 consecutive WIS STS-192c frames is generated. The SPE payload capacity of the TSS is filled with a PRBS-23 pattern. The sequence is generated in a 23 stage shift register whose 18th and 23rd stage outputs are added in a modulo-two addition stage, and the result is fed back to the input of the first stage. The shift register is loaded with all 1s at the start of each payload capacity.

The WIS transmit frame counter generates a STS-192c stream with valid H1, H2, H3 and Z0 pointer bytes. The frame counter can also insert an alternating pattern in the last 9 Z0 bytes of the section overhead. All other section, line and path overhead, and the fixed stuff bytes are generated by the SONET subsystem. The J1 byte of the path overhead may be programmed to a fixed value that provides optimal stress or be programmed to 0x89 if not used for that purpose.

14.34.2 Test Pattern Checking

The WIS checker consists of the existing SONET subsystem and a PRBS monitor. The SONET subsystem will verify the mixed frequency test pattern frame and the continuous PRBS-23 pattern frame by verifying the B1, B2, B3 bytes in each frame. The PRBS-23 monitor monitors the received data stream for a continuous PRBS-23 pattern in the SPE. The number of PRBS mismatches can be read from the S/UNI 9953 PRBS-23 Pattern Mismatch Counter register 0026H and 0027H. A top-level interrupt can be asserted if a mismatch is found. The interrupt is enabled through the S/UNI 9953 PCS/LAN/MDIO Interrupt Enable and Control register 001CH.

14.35 JTAG Support

Generic JTAG support in the S/UNI 9953 is described in Application Note, PMC-2021518, “JTAG Test Features Description”.

14.36 Board Design Recommendations

14.36.1 Power Supply Filtering Recommendations

Circuitry necessary to provide adequate power filtering and de-coupling for both the analog and digital circuits in the S/UNI 9953 is described in Application Note, PMC-2010770, “Power Supply Filtering Recommendations”.

14.36.2 Quad OC-48 Reference Design

Basic design guidelines for applications using the S/UNI 9953 in quad OC-48 mode is described in Application Note, PMC-2011381, “S/UNI 9953 4XOC-48 Line Card Reference Design”.

14.36.3 Static Alignment Design Considerations for PL4 Interface

Design considerations for applications implementing PL4 static alignment operation using S/UNI 9953 as the PHY device is described in PMC-2010476, “POS-PHY Level 4 Static Alignment Design Considerations Application Note”.

Downloaded by Control Team Parminder Nelson Wednesday, February 14, 2007 06:59:32 PM

14.36.4 Line Interface Design Considerations

Design recommendations for interfacing the S/UNI 9953 to an SFI-4/XSBI compliant optics/SERDES is described in Application Note, PMC-2011046, “Interfacing to SFI-4 on PMC-Sierra’s Xenon Chipset”.

14.37 Line and APS Interface PRBS Support

The PM5390 device has integrated PRBS generator and monitor blocks that may used for board level debug. The PRBS pattern is defined by the polynomial $1 + x^6 + x^7$.

Each of the 16 transmit data pins on the line interface (TXDATAx[y]) have their own independent PRBS generator. Similarly, each of the 16 receive data pins on the line interface (RXDATAx[y]) have their own independent PRBS monitor.

Each of the 16 transmit data pins on the APS interface (OAPSx[y]) have their own independent PRBS generator. Similarly, each of the 16 receive data pins on the line side interface (IAPSx[y]) have their own independent PRBS monitor.

Note that the PRBS data is injected on each serial stream just prior to being converted from the parallel to the serial stream. No payload framing is involved. Similarly, received PRBS data is checked immediately after being converted from the serial stream to an internal parallel stream. The purpose of the PRBS data is user specific, but could be used to determine the quality of the high-speed serial links.

The mapping of the control/status register to the relevant device pins is described in the appropriate register descriptions.

The configuration of the device for this mode is relatively simple. After configuring the device for normal mode of operation, simply enable both the generator and monitor by setting the MPGM_EN_REG bit in the appropriate configuration registers (0x0n28, 0x1n28, 0x0nA8, 0x1nA8) . Assuming the appropriate interrupt bits are enabled, then interrupts will be generated by the monitor when either LOCK is achieved or lost.

14.38 Power Management

The PM5390 device has multiple modes of operation and as such, some portions of the device are not be required for certain modes. Powering down these unused sections will assist in overall power management. Many of these power down functions are provided automaically depending on the mode of operation. In Revision C of the PM5390 device, an additional register has been added to further control the powering down of various sections. This is under full control of the user, as some features may or may not be required in various modes. This is controlled by register 0x0024. In addition, registers 0x0022 and 0x0023 have been added to disable the Transport and Path Overhead ports (RTOH and RPOH). These are described later.

In general, there are 3 areas where power consumption may be minimized:

- Mode dependent functions
- Unused Interfaces

Downloaded by Control Parts Group Inc on Wednesday, 07 February, 2007 06:59:32 PM

- Unused analog circuitry

14.38.1 Mode Dependent

Top-level register 0x0024 (S/UNI 9953 Power Down Configuration) controls the power down of various sections of the device. In this case, powering down will disable the clock to that section.

Table 53 Functional Mode Power Management

Operational Mode		Mode 1	Mode 2	Mode 3	Mode 4	Mode 5
Register 0x0024		STS-192c POS/ATM	STS-192 POS/ATM	STS-48c POS/ATM	10GE WAN	10GE LAN
Bit	Function					
Bit 15	APS_PD	X	X	X	X	1
Bit 14	STSI_PD	0	0	0	0	1
Bit 13	TTTP_PATH_PD	X	X	X	X	X*
Bit 12	RTTP_PATH_PD	X	X	X	X	X*
Bit 11	TTTP_SECTION_PD	X	X	X	X	X*
Bit 10	RTTP_SECTION_PD	X	X	X	X	X*
Bit 9	SARC_PD	0~~1~~	0	0	0~~1~~	X*
Bit 8	MSTAT_PD	1	1	1	X	X~~1~~
Bit 7	T64B66B_PD	1	1	1	0	0
Bit 6	R64B66B_PD	1	1	1	0	0
Bit 5	TXXG_PD	1	1	1	0	0
Bit 4	RXXG_PD	1	1	1	0	0
Bit 3	TCFP9953_PD	0	1	1	1	1
Bit 2	RCFP9953_PD	0	1	1	1	1
Bit 1	TCFP_PD	1	0	0	1	1
Bit 0	RCFP_PD	1	0	0	1	1

Key to the table

- 1: the block should be powered down in this mode
- 0: the block must not be powered down in this mode
- X: the block may be powered down in this mode if this feature is not required
- X*: powered down by default when LAN mode selected, thus these are redundant in this mode

14.38.2 Unused Interfaces

Transport and Path Overhead Insert/Extract

If interfaces are not being used, then they should be disabled to save power. Top-level registers 0x0022 and 0x0023 (S/UNI 9953 Overhead and DCC Configuration 1 &2) may be used to disable the clock and data activity on the overhead extraction and insertion ports. Control can be applied independently for each of the 4 STS-48 interfaces, and also for the receive/transmit and transport/path (ie RTOH, RPOH, TTOH, TPOH). This can achieved by setting each of the overhead select bits to “01”.

Downloaded by Content Search Department Inc on Wednesday, 21 February 2007 06:59:32 PM

Thus, to power down all overhead ports (transmit and receive, transport and path):

- Set register 0x0022 = 0x5555
- Set register 0x0023 = 0x5555

Output Clocks RCLK[4:1] and TCLK[4:1]

The 77.76MHz clock outputs RCLK[4:1] and TCLK[4:1] may be disabled. Note that by default these are disbled. Control is provided in register 0x0004 (S/UNI 9953 Transmit Control and Clock Enable).

Output Clocks PGMRCLK[4:1] and PGMTCLK[4:1]

The programmable clock outputs PGMRCLK[4:1] and PGMTCLK[4:1] may be disabled. Note that by default these are disbled. Control is provided in register 0x1031 (STLI Programmable Clock Configuration) and register 0x003C (SRLI Programmable Clock Configuration).

14.38.3 Analog Circuitry

The PM5390 device contains 3 major areas of analog circuitry. These being the line side SFI4.1 (XSBI) interface, the SPI4.2 (PL4) interface, and the APS interface.

APS Power Down

If the APS interfaces are not being used, then the associated digital and analog circuitry may be disabled. The digital is powered down by the APS_PD bit described above in the mode dependent section. The analog circuitry is powered down by disabling all 16 transmitters and receivers, and also the associated CSU block.

This is achieved as follows (where n = 0 through F):

- Set register 0x0nA3 = 0xF402 (R8TD #1-16)
- Set register 0x1nA5 = 0x0187 (T8TE #1-16)
- Set register 0x2380 = 0x0419 (CSTRI)

PL4 Power Down

Under normal operation, the PL4 interface would not be powered down. However, if the device is used as a protect APS mate, then its PL4 interface would not be required. In this case, the PL4 CSU can be powered down. This will also remove all the clocks to the PL4 digital circuitry, the PL4 FIFO, and the packet/cell/frame processing blocks. If this is done, then the blocks providing a transfer in progress (TIP) signal back to the main microprocessor TIP bit (register 0x0000) would not be able to clear their own local TIP signal, as they have no clocks to do so. This would cause the TIP bit to stay asserted, and twould thus “hang” any process polling it. To avoid this situation, the TIP from blocks that have been powered down by setting the PL4 disable bit must disabled. This is done by setting the PL4_TIP_DIS bit in register 0x001F.

This is achieved as follows:

- Set PL4_TIP_DIS bit in register 0x001F to logic 1.

Downloaded by [redacted] on Palmwinter Inc on Wednesday, 07 February, 2007, 06:59:32 PM

- Set ENABLE bit in register 0x2305 to logic 0.

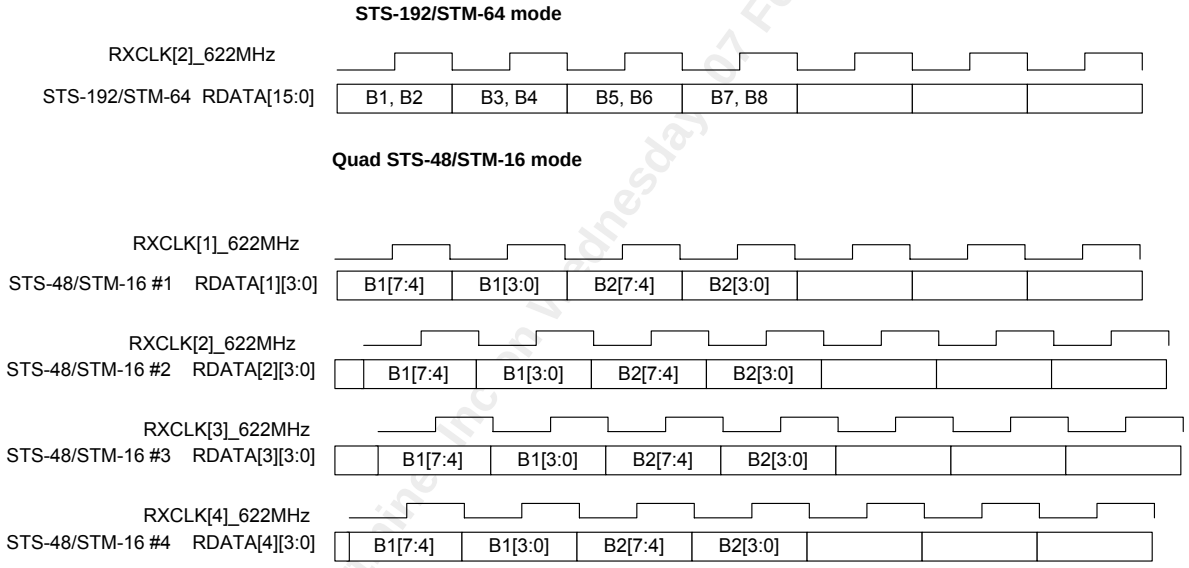
Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

15 Functional Timing

15.1 Line Interface Functional Timing

The S/UNI 9953 line interface complies with the OIF OC-192 SERDES Interface Revision 3.1. When the device is used to process an STS-192/STM-64 SONET/SDH stream, the RXDATA/TXDATA bus carries two bytes and is sampled/updated on the rising edge of the RXCLK[2]/TXCLK[2]. When four STS-48/STM-16 are processed, each RXDATA[N][3:0]/TXDATA[N][3:0] carries a nibble and is sampled/updated on the rising edge of the RXCLK[N]/TXCLK[N]. Figure 46 shows the functional timing of the receive line interface.

Figure 46 Line Interface Functional Timing



15.2 Receive Overhead Port Timing

The RTOH and RPOH ports may be configured to extract either section or line DCC bytes, in addition to the full overhead bytes. This is configured using the S/UNI 9953 Overhead and DCC Configuration1 and 2 registers (0022H and 0023H). The following sections describe the interface functional timing when used in the different modes of operation.

15.2.1 Receive Transport Full Overhead Byte Access (RTOH)

This is the default mode of operation for the overhead ports.

Downloaded by Content Part Line Inc on Wednesday, 07 February, 2007 10:30:32 PM

Figure 47 shows the functional timing of the receive transport overhead (RTOH) port when extracting all the overhead bytes. RTOHCLK[1:4] is a nominal 82.94MHz clock generated by gapping a 103.68MHz clock. 10368 bits (9x3x48 bytes) are output on each RTOH[N] between two RTOHFP assertion. All RTOH outputs (RTOH[N], RTOHFP[N]) are updated on the rising edge of RTOHCLK[N]. The rising edge of RTOHCLK[N] should be used to sample RTOH[N] and RTOHFP[N] . Sampling RTOHFP[N] high identifies the MSB of the first A1 Byte on RTOH. Refer to the multiplexing structure described in the functional description section for more details on how the serial bit stream is formatted.

The S/UNI 9953 extracts and serially outputs all the transport overhead bytes (defined and undefined) on the RTOH ports. 10368 bits (9x3x48 bytes) are output on each RTOH[N] between two RTOHFP assertion. Figure 47 shows the receive transport overhead (RTOH) functional timings. RTOHCLK[1:4] is a nominal 82.94MHz clock generated by gapping a 103.68MHz clock. The gapping occurs after the fourth bit 7 has been serialized out on the RTOH port for each group of 4 bytes. This gap is eight 103.68 MHz clock periods wide. All RTOH outputs (RTOH[N], RTOHFP[N]) are updated on the rising edge of RTOHCLK[N]. The rising edge of RTOHCLK[N] should be used to sample RTOH[N] and RTOHFP[N]. Sampling RTOHFP[N] high identifies the MSB of the first A1 Byte on RTOH.

When processing an STS-192/STM-64 or a quad STS-48/STM-16 data stream, the following multiplexing structure is used :

RTOH[1] bit-wise multiplexes the transport overhead bytes from [STM-16 #1, STM-4 #N] data streams as follows: [1,1] [1,2] [1,3] [1,4].

RTOH[2] bit-wise multiplexes the transport overhead bytes from [STM-16 #2, STM-4 #N] data streams as follows: [2,1] [2,2] [2,3] [2,4].

RTOH[3] bit-wise multiplexes the transport overhead bytes from [STM-16 #3, STM-4 #N] data streams as follows: [3,1] [3,2] [3,3] [3,4].

RTOH[4] bit-wise multiplexes the transport overhead bytes from [STM-16 #4, STM-4 #N] data streams as follows: [4,1] [4,2] [4,3] [4,4].

Downloaded by Content Team of Parliament TV on Wednesday, 07 March 2007 06:30:07 IST

Figure 47 RTOH Port Functional Timing (all OH bytes)

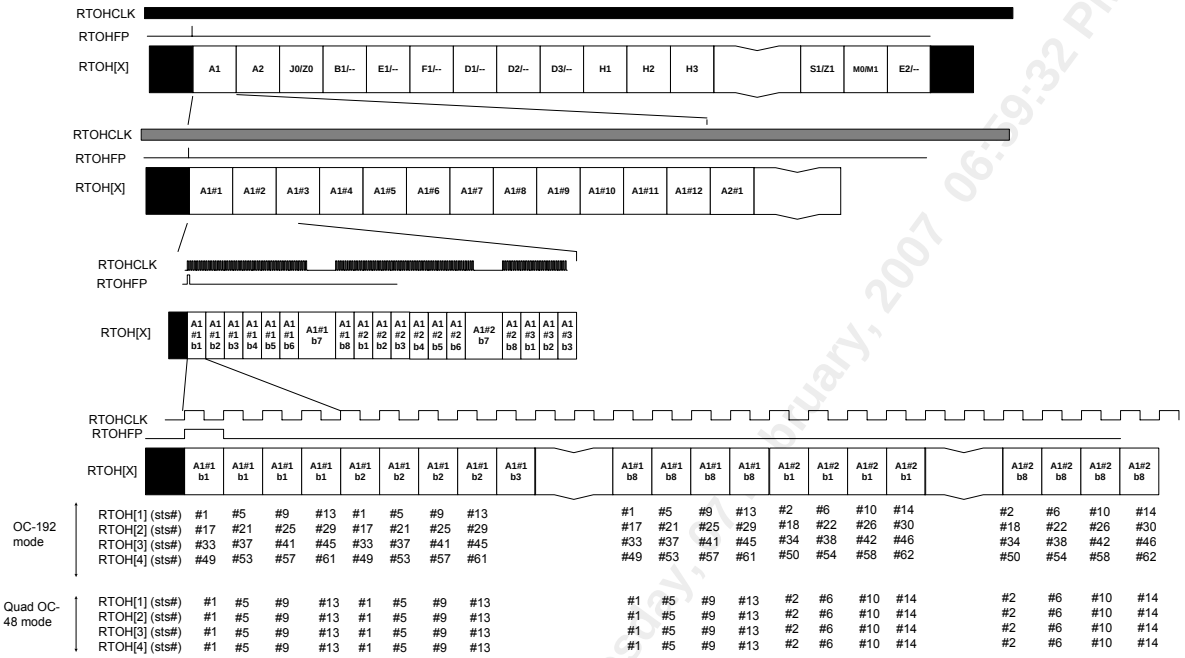


Table 54 show the transport overhead (byte/bit) streaming orders on the RTOH ports for STS-192/STM-64 operation. Column 1 contains the constituent STS-48/STM-16 data stream numbers #1 to #4 and the corresponding transport overhead bytes are serialized out on RTOH port #1 to #4 respectively. Column 2 contains the constituent STS-12/STM-4 data stream numbers #1 to #4 within each STS-48/STM-16. Columns 3 to 14 contain STS-1/STM-0 time-slot numbers within the STS-192/STM-64 according to the receive order from the line. The first A1 byte in the STS-192/STM-64 belongs to the STS-1/STM-0 time-slot #1 (high-lighted in table) which is part of STS-48/STM-16 #1, STS-12/STM-4 #1 data stream. The last Z0 byte in the STS-192/STM-64 belongs to the STS-1/STM-0 time-slot #192 (high-lighted in table) which is part of STS-48/STM-16 #4, STS-12/STM-4 #4 data stream. For RTOH[1], the transport overhead bytes (SONET/SDH serial words) from STS-1/STM-0 #1, #5, #9 and #13 are the first to be serialized out in a bit interleave manner starting with b1 and ending with b8 (where b1 is the first bit received for each serial word) as shown in Figure 47. The second set of four transport overhead bytes will be from STS-1/STM-0 #2, #6, #10 and #14 and so on. STS-1/STM-0 #132, #136, #140 and #144 provide the last set of four transport overhead bytes to be serialized on RTOH[1]. Similar transport overhead byte order for RTOH[4:2] can be looked up in Table 54.

Table 54 RTOH Port Transport Overhead Multiplexing for STS-192/STM-64

STM-16 (RTOH) #	STM-4 #	Transport Byte/Bit Streaming Order on RTOH →											
		b1..b8	b1..b8	b1..b8	b1..b8	b1..b8	b1..b8	b1..b8	b1..b8	b1..b8	b1..b8	b1..b8	b1..b8
1	1	**1**	2	3	4	65	66	67	68	129	130	131	132
	2	5	6	7	8	69	70	71	72	133	134	135	136
	3	9	10	11	12	73	74	75	76	137	138	139	140

Downloaded by Content Library at 13:59:32 PM, Wednesday, 07 February, 2007

STM-16 (RTOH) #	STM-4 #	Transport Byte/Bit Streaming Order on RTOH →											
		b1..b8	b1..b8	b1..b8	b1..b8	b1..b8	b1..b8	b1..b8	b1..b8	b1..b8	b1..b8	b1..b8	b1..b8
	4	13	14	15	16	77	78	79	80	141	142	143	144
2	1	17	18	19	20	81	82	83	84	145	146	147	148
	2	21	22	23	24	85	86	87	88	149	150	151	152
	3	25	26	27	28	89	90	91	92	153	154	155	156
	4	29	30	31	32	93	94	95	96	157	158	159	160
3	1	33	34	35	36	97	98	99	100	161	162	163	164
	2	37	38	39	40	101	102	103	104	165	166	167	168
	3	41	42	42	44	105	106	107	108	169	170	171	172
	4	45	46	47	48	109	110	111	112	173	174	175	176
4	1	49	50	51	52	113	114	115	116	177	178	179	180
	2	53	54	55	56	117	118	119	120	181	182	183	184
	3	57	58	59	60	121	122	123	124	185	186	187	188
	4	61	62	63	64	125	126	127	128	189	190	191	**192**

Table 55 shows the transport overhead (byte/bit) streaming orders on the RTOH ports for quad STS-48/STM-16 operation. Column 1 contains the STS-48/STM-16 data stream numbers #1 to #4 and the corresponding transport overhead bytes are serialized out on RTOH port #1 to #4 respectively. Column 2 contains the constituent STS-12/STM-4 data stream numbers #1 to #4 within each STS-48/STM-16. Columns 3 to 14 contain STS-1/STM-0 time-slot numbers within the STS-48/STM-16 according to the receive order from the line. The first A1 byte in the STS-48/STM-16 belongs to the STS-1/STM-0 time-slot #1 (high-lighted in table) which is part of STS-12/STM-4 #1 data stream. The last Z0 byte in the STS-48/STM-16 belongs to the STS-1/STM-0 time-slot #48 (high-lighted in table) which is part of STS-12/STM-4 #4 data stream. For RTOH[N], the transport overhead bytes (SONET/SDH serial words) from STS-1/STM-0 #1, #5, #9 and #13 are the first to be serialized out in a bit interleave manner starting with b1 and ending with b8 (where b1 is the first bit received for each serial word) as shown in Figure 47. The second set of four transport overhead bytes will be from STS-1/STM-0 #2, #6, #10 and #14 and so on. STS-1/STM-0 #36, #40, #44 and #48 provide the last set of four transport overhead bytes to be serialized on RTOH[N].

Table 55 RTOH Port Transport Overhead Multiplexing for Quad STS-48/STM-16

STM-16 (RTOH) #	STM-4 #	Transport Byte/Bit Streaming Order on RTOH →											
		b1..b8	b1..b8	b1..b8	b1..b8	b1..b8	b1..b8	b1..b8	b1..b8	b1..b8	b1..b8	b1..b8	b1..b8
1	1	**1**	2	3	4	17	18	19	20	33	34	35	36
	2	5	6	7	8	21	22	23	24	37	38	39	40
	3	9	10	11	12	25	26	27	28	41	42	43	44
	4	13	14	15	16	29	30	31	32	45	46	47	**48**
2	1	**1**	2	3	4	17	18	19	20	33	34	35	36
	2	5	6	7	8	21	22	23	24	37	38	39	40
	3	9	10	11	12	25	26	27	28	41	42	43	44
	4	13	14	15	16	29	30	31	32	45	46	47	**48**
3	1	**1**	2	3	4	17	18	19	20	33	34	35	36
	2	5	6	7	8	21	22	23	24	37	38	39	40

Downloaded by Content Team (Content Team) on 06-Jun-2007 from IHS, 2007/06/06 16:52:21

STM-16 (RTOH) #	STM-4 #	Transport Byte/Bit Streaming Order on RTOH →											
		b1..b8	b1..b8	b1..b8	b1..b8	b1..b8	b1..b8	b1..b8	b1..b8	b1..b8	b1..b8	b1..b8	b1..b8
	3	9	10	11	12	25	26	27	28	41	42	43	44
	4	13	14	15	16	29	30	31	32	45	46	47	**48**
4	1	**1**	2	3	4	17	18	19	20	33	34	35	36
	2	5	6	7	8	21	22	23	24	37	38	39	40
	3	9	10	11	12	25	26	27	28	41	42	43	44
	4	13	14	15	16	29	30	31	32	45	46	47	**48**

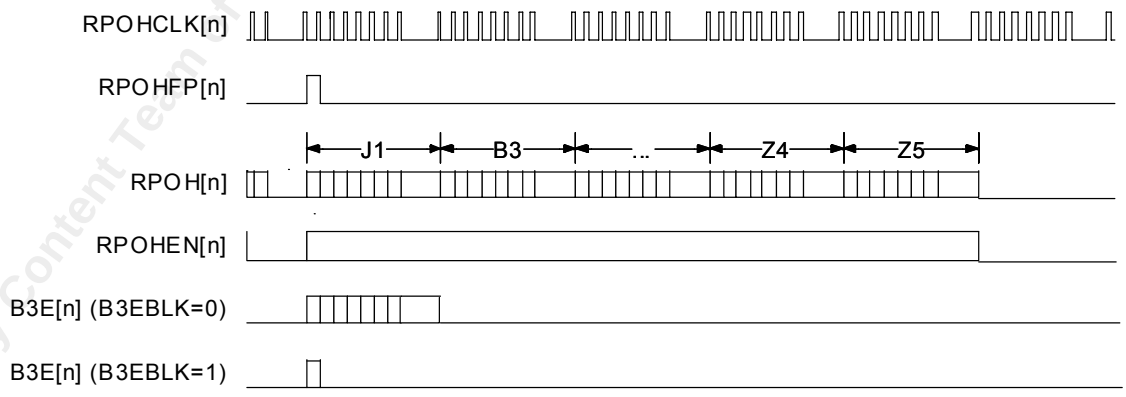
15.2.2 Receive Path Full Overhead Byte Access (RPOH)

Figure 48 shows the receive path overhead port functional timing when extracting all the overhead bytes. RPOHCLK[4:1] are 20.736 MHz clocks generated by gapping down 25.92 MHz clocks (RCLK[4:1] divided by 3). RPOHFP[4:1] are updated on the falling edge of corresponding RPOHCLK[4:1]. This guarantees a proper setup and hold time for sampling RPOHFP[4:1] externally with the rising edge of RPOHCLK[4:1]. Similarly, RPOH[4:1], RPOHEN[4:1] and B3E[4:1] are updated on the falling edge of corresponding RPOHCLK[4:1].

The RPOH port #n (RPOHFP[n], RPOH[n], RPOHEN[n], B3E[n]) is used to output the POH bytes of the STS (VC) payloads and the path BIP-8 errors for the corresponding STS-48c (STM-16c) #n data stream in quad OC-48 mode. Sampling RPOHFP[n] high identifies the MSB of the path trace byte of STS-48c (STM-16c) #n on RPOH[n] and the first possible path BIP-8 error on B3E[n]. For STS-192c (STM-64c) data stream, only RPOH port #1 carries valid POH bytes and BIP-8 errors.

The POH bytes are output on RPOH[n] MSB first in the same order that they are received. Since RPOHFP[n] is synchronized on the transport frame, zero, one or two-path overhead can be output per path per frame. RPOHEN[n] is used to indicate new POH bytes on RPOH[n]. RPOHEN[n] is either asserted or de-asserted for the nine POH bytes. The path BIP-8 errors are output on B3E[n] at the same time the path trace byte is output on RPOH[n]. Optionally, block BIP-8 errors can be output on B3E[n].

Figure 48 RPOH Port Functional Timing (all OH bytes)



Downloaded by Content Team of Partminer.com on Wednesday, 07 February 2007 10:50:52 PM

15.2.3 Receive DCC Byte Access (RTOH and RPOH)

Either the RTOH or RPOH ports may be configured to serially output the section (D1-D3) or line (D4-D12) DCC bytes. The RRMP RSLDSEL register bit selects which of the two sources is multiplexed out onto the interfaces.

RTOHCLK[1:4]/RPOHCLK[1:4] are the generated output clocks used to provide timing for the RTOH/RPOH interfaces. If the interface carries the line DCC, the clocks are a nominal 576 kHz clock or if the interface carries the section DCC, the clocks are a nominal 192 kHz clock.

Sampling RTOHFP/RPOHFP high identifies the MSB of the first DCC byte on RTOH/RPOH interface.

RTOH/RPOH data are generated on the falling edge of RTOHCLK[1:4]/RPOHCLK[1:4] and should be sampled on the rising edge of RTOHCLK[1:4]/RPOHCLK[1:4].

RTOHFP/RPOHFP data are generated on the rising edge of RTOHCLK[1:4]/RPOHCLK[1:4] and should be sampled on the falling edge of RTOHCLK[1:4]/RPOHCLK[1:4].

Note that when STS-192/STM-64 mode is enabled RTOH/RPOH ports 2-4 should be ignored.

Figure 49 shows the RTOH/RPOH port functional timings when extracting section DCC (D1-D3).

Figure 49 shows the RTOH/RPOH port functional timings when extracting line DCC (D4-D12).

Figure 49 RTOH/RPOH Port Functional Timing (D1-D3 OH bytes)

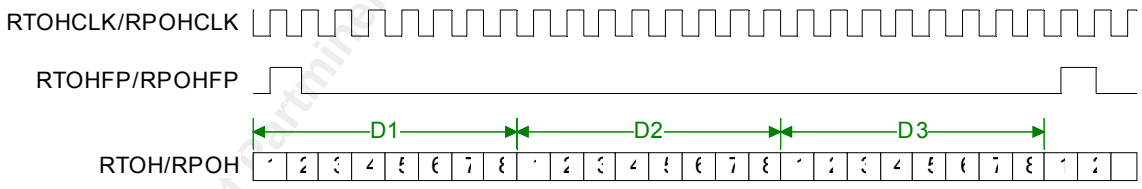
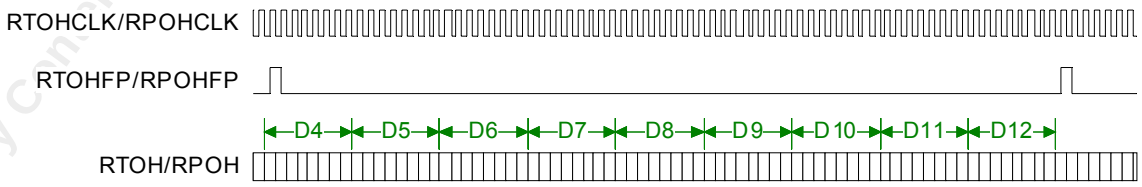


Figure 50 RTOH/RPOH Port Functional Timing (D4-D12 OH bytes)



Downloaded by Component Team of Earthlink Inc on Wednesday, 07 February, 2007 09:59:32 PM

15.3 Transmit Overhead Port Timing

The TTOH and TPOH ports may be configured to insert either section or line DCC bytes, in addition to the full overhead bytes. This is configured using the S/UNI 9953 Overhead and DCC Configuration1 and 2 registers (0022H and 0023H). The following sections describe the interface functional timing when used in the different modes of operation.

15.3.1 Transmit Transport Full Overhead Byte Access (TTOH)

This is the default mode of operation for the overhead ports.

The TOH bytes must be serially presented to TTOH[4:1] in the same order that they are transmitted (A1, A2, J0/Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, S1/Z1, Z2/M1/Z2 and E2). The multiplexing structure is the same as the RTOH port (Refer to Figure 47, Table 54, Table 55). TTOHCLK[4:1] are the generated output clocks used to provide timing for the TTOH[4:1] inputs, the TTOHEN[4:1] inputs and the TTOHFP[4:1] outputs. TTOHCLK[N] is a nominal 82.94MHz clock generated by gapping a 103.68MHz clock. Sampling TTOHFP[N] high with the rising edge of TTOHCLK[N] identifies the MSB of the first A1 byte on TTOH[N]. TTOHEN[N] is used to validate, on a byte basis, the byte insertion via TTOH[N]. When TTOHEN[N] is sampled high on the serial byte, the serial byte is to be inserted. When TTOHEN[N] is sampled low on the serial byte, the serial byte is discarded. TTOHEN[N] must be high on all the bits in order to insert the byte and must be low on all the bits to discard the byte.

15.3.2 Transmit Path Full Overhead Byte Access (TPOH)

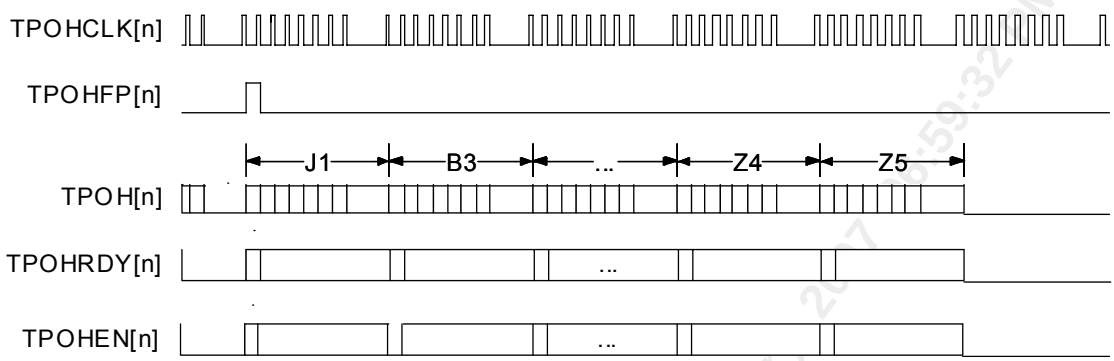
Figure 51 shows the transmit path overhead port functional timing when inserting all the overhead bytes. TPOHCLK[4:1] are 20.736 MHz clocks generated by gapping 25.92 MHz clocks (TCLK[4:1] divided by 3). TPOHFP[4:1] and TPOHRDY[4:1] are updated on the falling edge of corresponding TPOHCLK[4:1]. TPOHFP[4:1] and TPOHRDY[4:1] must be sampled externally on the rising edge of TPOHCLK[4:1] for a proper setup and hold time. TPOH[4:1] and TPOHEN[4:1] are sampled by device on the rising edge of the corresponding TPOHCLK[4:1].

The TPOH port #n (TPOHFP[n], TPOH[n], TPOHEN[n], TPOHRDY[n]) is used to insert the POH bytes of the STS (VC) payloads for the corresponding STS-48c (STM-16c) #n data stream in quad OC-48 mode. For STS-192c (STM-64c) data stream, only TPOH port #1 carries valid POH bytes.

A logic one on TPOHFP[n] identifies the MSB of the first J1 byte on TPOH[n]. The POH bytes are sampled on TPOH[n] MSB first in the same order that they are transmitted. TPOHRDY[n] is asserted to indicate to external circuitry that the device is ready to accept data. TPOHRDY[n] is only asserted when the device is capable of receiving all 9 path overhead bytes for the corresponding data streams. TPOHEN[n] is used to validate the insertion of the corresponding byte on TPOH[n]. When TPOHRDY[n] is logic high and TPOHEN[n] is sampled high on the MSB of the byte, the byte will be inserted in the path overhead of the transmit stream. When TPOHRDY[n] is logic high and TPOHEN[n] is sampled low on the MSB of the byte, the byte is not inserted in the transmit stream.

Downloaded by [illegible] on Wednesday, February 14, 2007 06:59:17 PM

Figure 51 TPOH Port Functional Timing (all OH bytes)



15.3.3 Transmit DCC Byte Access (TTOH and TPOH)

Either the TTOH or TPOH ports may be configured to serially input the section (D1-D3) or line (D4-D12) DCC bytes. The TRMP TSLDSEL register bit selects which of the DCC bytes (section or line) are multiplexed into the interfaces, and thus the frequency of the output clock (192KHz or 576KHz).

TTOHCLK[1:4]/TPOHCLK[1:4] are the generated output clocks used to provide timing for the TTOH/TPOH output. If the interface carries the line DCC, the clocks are a nominal 576 kHz clock or if the interface carries the section DCC, the clocks are a nominal 192 kHz clock.

Sampling TTOHFP/TPOHFP high identifies the MSB of the first DCC byte on TTOH/TPOH interface.

TTOH/TPOH data are sampled on the rising edge of TTOHCLK[1:4]/TPOHCLK[1:4] and should be generated on the falling edge of TTOHCLK[1:4]/TPOHCLK[1:4].

TTOHFP/TPOHFP data are generated on the rising edge of TTOHCLK[1:4]/TPOHCLK[1:4] and should be sampled on the falling edge of TTOHCLK[1:4]/TPOHCLK[1:4].

Note that when STS-192/STM-64 mode is enabled TTOH/TPOH ports 2-4 should be ignored.

Figure 52 shows the TTOH/TPOH port functional timings when inserting section DCC (D1-D3).

Figure 53 shows the TTOH/TPOH port functional timings when inserting line DCC (D4-D12).

Downloaded by Content Team of Harte-Hanks on Wednesday, 07 February, 2007 10:59:32 AM

Figure 52 TTOH/TPOH Functional Timing (D1-D3 OH bytes)

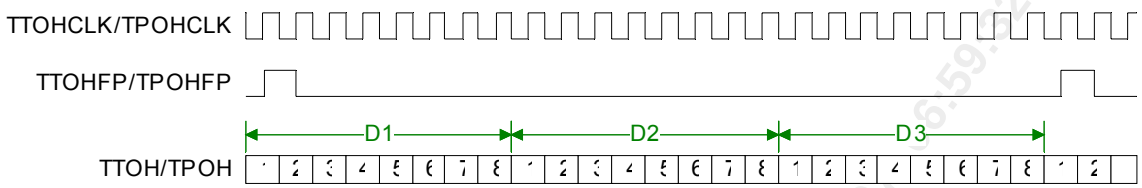
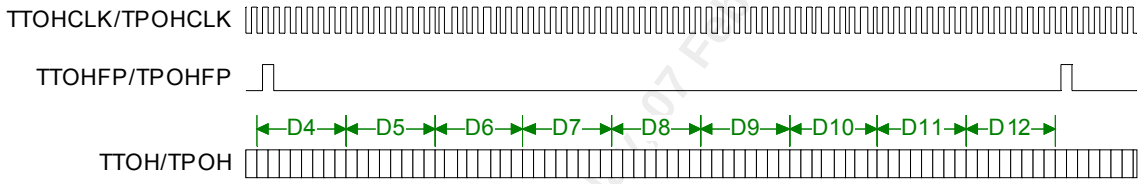


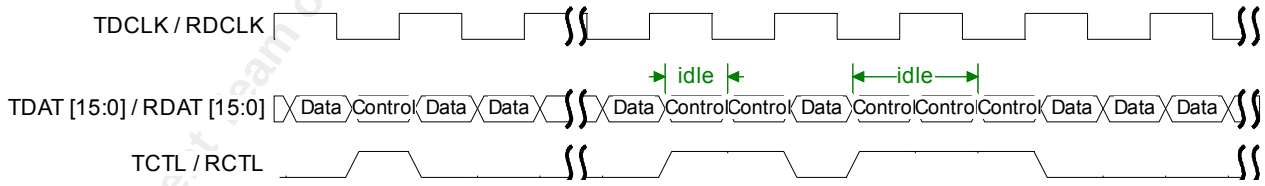
Figure 53 TTOH/TPOH Functional Timing (D4-D12 OH bytes)



15.4 PL4 Interface Data Path and FIFO Status Timing

A timing diagram of the PL4 interface data path signals is shown in Figure 54. This diagram is applicable to either the transmit or the receive interface. TCTL/RCTL is high when TDAT[15:0]/RDAT[15:0] contains control words. Idle periods correspond to back-to-back control words. Data and control words are updated on both the rising and falling edges of the TDCLK/RDCLK. The actual clock rate used in practice is determined by the application at hand (up to a maximum of 700 MHz data rate divide by 2).

Figure 54 PL4 Interface Data Path Functional Timing



Complete packets or shorter bursts (fragment of larger packets) may be transferred. The maximum configured payload data transfer size must be a multiple of 16 bytes. Control words are inserted only between burst transfers; once a transfer has begun, data words are sent uninterrupted until end-of-packet or the burst transfer size is reached, whichever comes first. The interval between the end of a given transfer and the next payload control word (marking the start of another transfer) consists of zero or more idle control words.

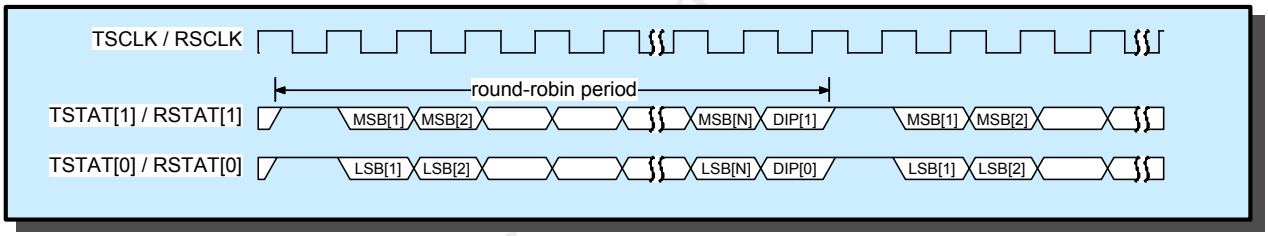
Downloaded by Content Team of Partline (K) Limited on Wednesday, 07 February, 2007 6:59:12 PM

The minimum and maximum supported packet lengths are determined by the application. For ease of implementation however, successive start-of-packets must occur not less than 8 cycles apart, where a cycle is one control or data word. The gap between shorter packets is filled with idle control words.

Payload data bytes are transferred over the interface in the same order as they would be transmitted or received on the line side. The most significant bits (MSBs) of the constituent bytes correspond to bits 15 and 7. The byte with MSB at bit 15 is transmitted or received first on the line side relative to the byte with MSB at bit 7. On payload transfers that do not end on an even byte boundary, the unused byte (after the last valid byte) is set to all zeroes.

Figure 55 shows the PL4 Interface FIFO Status functional timing for the S/UNI 9953 device. FIFO status information is sent periodically over TSTAT[1:0] from the S/UNI 9953 to the Link Layer device, and over the RSTAT[1:0] from the Link Layer to the S/UNI 9953. The transmit and receive status channels operate independently of each other. TSTAT[1:0]/RSTAT[1:0] is updated on the rising edge of TSCLK/RSCLK. TSCLK/RSCLK runs at a nominal rate of 1/8th the data rate of the PL4 transmit/receive interface.

Figure 55 PL4 Interface FIFO Status Functional Timing



The FIFO status of each port is encoded in a 2-bit data structure as per PL4 specification. The port sequences on the transmit and receive interfaces may be configured differently from each other. The “1 1” pattern is reserved for in-band framing; it must be sent once prior to the start of the FIFO status sequence. A DIP-2 odd parity checksum is sent at the end of each complete sequence, immediately before the “1 1” framing pattern. The DIP-2 code is computed over all preceding FIFO status indications sent after the last “1 1” framing pattern as per PL4 specification. A continuous stream of repeated “1 1” framing patterns may be sent to indicate an error condition.

Downloaded by Content Team @ Document Inc

16 Absolute Maximum Ratings

Maximum rating are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

Table 56 Absolute Maximum Ratings

Storage Temperature	-40°C to +125°C
Supply Voltage (3.3V)	-0.3V to 4.6V
Supply Voltage (1.8V)	-0.3V to 2.4V
Voltage on Any Digital Pin	-0.3V to V_{VDDO}+0.3V
Static Discharge Voltage	±1000 V
Latch-Up Current	±100 Ma
DC Input Current	±20 Ma
Ball Temperature	+225°C
Absolute Maximum Junction Temperature	+125°C

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 06:59:32 PM

17 Normal Operating Conditions

Unless otherwise specified, all DC and AC specifications in this data sheet are valid for the following voltage and temperature ranges.

	Operating Range[1]		Typical[2]
Operating Temperature	T_A = -40 °C to T_J =125~~05~~ °C		T_J = 60 °C
Supply Voltages	**Minimum (V)**	**Typical (V)**	**Maximum (V)**
1.8V Supply Voltage (VDDI)	1.71	1.80	1.89
3.3V Supply Voltage (VDDO)	3.14	3.30	3.46
1.8V Analog Supply Voltage (AVDL)	1.71	1.80	1.89
3.3V Analog Supply Voltage (AVDH)	3.14	3.30	3.46

Notes

1. Power supply, D.C. characteristics, and A.C. timing are characterized across these operating ranges, unless otherwise stated
2. Where typical measurements are given, these parameter values will be used, unless otherwise stated

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2018 10:30:32 PM

18 Power Information

18.1 Power Requirements

Conditions	Parameter	Typ[1,3]	High[4]	Max[2]	Units
OC-192c POS Mode APS Enabled	IDDOP (1.8V)	4.84	—	5.70	A
	IDDOP (3.3 V)	0.55	—	0.95	A
	Total Power	10.53	12.99	—	W
OC-192c POS Mode APS Disabled[5]	IDDOP (1.8V)	4.46	—	5.24	A
	IDDOP (3.3 V)	0.39	—	0.95	A
	Total Power	9.32	12.12	—	W
4xOC-48c POS Mode APS Enabled	IDDOP (1.8V)	4.75	—	5.30	A
	IDDOP (3.3 V)	0.55	—	1.11	A
	Total Power	10.36	12.79	—	W
4xOC-48c POS Mode APS Disabled[5]	IDDOP (1.8V)	4.37	—	4.92	A
	IDDOP (3.3 V)	0.39	—	0.96	A
	Total Power	9.16	11.56	—	W
10GbE WAN Mode APS Disabled	IDDOP (1.8V)	4.38	—	5.10	A
	IDDOP (3.3 V)	0.39	—	0.96	A
	Total Power	9.19	11.89	—	W
10GbE LAN Mode APS Disabled	IDDOP (1.8V)	3.09	—	3.81	A
	IDDOP (3.3 V)	0.39	—	0.86	A
	Total Power	6.87	9.12	—	W

Notes

1. Typical IDD values are calculated as the mean value of current under the following conditions: typically processed silicon, nominal supply voltage, T_J=60 °C, outputs loaded with 30 pF (if not otherwise specified), and a normal amount of traffic or signal activity. These values are suitable for evaluating typical device performance in a system
2. Max IDD values are currents guaranteed by the production test program and/or characterization over process for operating currents at the maximum operating voltage and operating temperature that yields the highest current (including outputs loaded to 30 pF, unless otherwise specified)
3. Typical power values are calculated using the formula:

   Power = ∑i(VDDNomi x IDDTypi)

   Where i denotes all the various power supplies on the device, VDDNomi is the nominal voltage for supply i, and IDDTypi is the typical current for supply i (as defined in note 1 above). These values are suitable for evaluating typical device performance in a system
4. High power values are a “normal high power” estimate and are calculated using the formula:

   Power = ∑i(VDDMaxi x IDDHighi)

   Where i denotes all the various power supplies on the device, VDDMaxi is the maximum operating voltage for supply i, and IDDHighi is the current for supply i. IDDHigh values are calculated as the mean value plus two sigmas (2σ) of measured current under the following conditions: T_J=105° C, outputs loaded with 30 pF (if not otherwise specified). These values are suitable for evaluating board and device thermal characteristics

Downloaded by Conti Temic microelectronic Inc on Monday, 07 January, 2007 10:39:32 PM

5. To disable the APS port, the following register bits should be written:

Block	Control Register (hex)	Setting (hex)
R8TD #1-16	0nA3h : R8TD APS Analog Control #1 where n = 0 through F	F402h
T8TE #1-16	1nA5h : T8TE APS Analog Control where n = 0 through F	0187h
CSTRI	2380h : CSTR Control	0419h

6. The Typical numbers are measured in the lab using Revision C of the device. The device is fully operational and passing PRBS-23 or similar data patterns within the payload. Use of the power management features are employed during the measurements, which optionally disables the various parts of the logic not required for a particular. This is detailed in the Power Management section 14.38 of this document.

18.2 Power Sequencing

Due to ESD protection structures in the pads it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions, incorrect power sequencing may damage these ESD protection devices or trigger latch up.

The recommended power supply sequencing is as follows:

1. VDDO power must be supplied either before VDDI or simultaneously with VDDI.

2. AVDH can be applied either before or after VDDO, but must be applied either before or simultaneously with VDDI. In operation, the differential voltage measured between AVDH supplies and VDDO must be less than 0.5 volt. The relative power sequencing of the multiple AVDH power supplies is not important.

3. AVDL must be applied after AVDH and VDDO, and either before or after VDDI. Or, AVDL can be applied simultaneously with VDDO, AVDH, and VDDI.

4. I/Os get driven after all the supplies have been powered. Otherwise, the I/Os must be current limited to 20 mA.

5. Power down the device in the reverse sequence.

18.3 Power Supply Filtering

Circuitry necessary to provide adequate power filtering and de-coupling for both the analog and digital circuits in the S/UNI 9953 is described in Application Note, PMC-2010770, “Power Supply Filtering Recommendations”.

Downloaded by Control Team of Paknin Inc (ctl@paknin.com), Wednesday, 21 February, 2007 06:59:32 PM

19 D.C. Characteristics

Table 57 D.C. Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{IL}	Input Low Voltage	—	—	0.8	Volts	Guaranteed Input Low Voltage
V_{IH}	Input High Voltage	2.0	—	—	Volts	Guaranteed Input High Voltage
V_{OL}	Output Or Bi-Directional Low Voltage	—	0.1	0.4	Volts	Guaranteed Output Low Voltage At V_{VDDO}=2.97V And I_{OL}=Maximum Rated For Pad.
V_{OH}	Output Or Bi-Directional High Voltage	2.4	2.7	—	Volts	Guaranteed Output Low Voltage At V_{VDDO}=2.97V And I_{OL}=Maximum Rated For Pad.
V_{T-}	Schmidt Input Low Voltage	—	—	0.8	Volts	Applies To All Schmidt Inputs.
V_{T+}	Schmidt Input High Voltage	2.2	—	—	Volts	Applies To All Schmidt Inputs.
V_{TH}	Schmidt Input Hysteresis	—	0.5	—	Volts	Applies To All Schmidt Inputs.
I_{ILPU}	Input Low Current	-200	-50	-4	µA	V_{IL} = GND. NOTES 1 AND 3.
I_{IHPU}	Input High Current	-10	0	+10	µA	$V_{IH} = V_{VDDO}$. NOTES 1 AND 3.
I_{IL}	Input Low Current	-10	0	+10	µA	V_{IL} = GND. NOTES 2 AND 3.
I_{IH}	Input High Current	-10	0	+10	µA	$V_{IH} = V_{VDDO}$. NOTES 2 AND 3.
C_{IN}	Input Capacitance	—	5	—	pF	—
C_{OUT}	Output Capacitance	—	5	—	pF	—
C_{IO}	Bi-Directional Capacitance	—	5	—	pF	—
I_{DDOP1}	Operating Current	—	—	—	mA	SEE NOTE 4
V_{ICM}	LVDS Input Common-Mode Range	0	—	2.4	V	—
$\|V_{IDM}\|$	LVDS Input Differential Sensitivity	—	—	100	mV	—

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2001 06:30:32 PM

Symbol	Parameter	Min	Typ	Max	Units	Conditions
R_{IN}	LVDS Differential Input Impedance	85	100	115	Ω	—
V_{LOH}	LVDS Output Voltage High	—	1375	1475	mV	R_{LOAD}=100Ω ±1%
V_{LOL}	LVDS Output Voltage Low	925	1025	—	mV	R_{LOAD}=100Ω ±1%
V_{ODM}	LVDS Output Differential Voltage	300	350	400	mV	R_{LOAD}=100Ω ±1%
V_{OCM}	LVDS Output Common-Mode Voltage	1125	1200	1275	mV	R_{LOAD}=100Ω ±1%
R_O	LVDS Output Impedance, Differential	85	110	115	Ω	—
$\|V_{ODM}\|$	Change In $\|V_{ODM}\|$ Between "0" And "1"	—	—	25	mV	R_{LOAD}=100Ω ±1%
$\|V_{OCM}\|$	Change In $\|V_{OCM}\|$ Between "0" And "1"	—	—	25	mV	R_{LOAD}=100Ω ±1%
I_{SP}, I_{SN}	LVDS Short-Circuit Output Current	—	—	10	mA	Drivers Shorted To Ground
I_{SPN}	LVDS Short-Circuit Output Current	—	—	10	mA	Drivers Shorted Together
$V_{IL,}$ DC PECL	Input Low Voltage	V_{VDDO} – 1.81	—	V_{VDDO} – 1.475	Volts	Applies to REFCLK+/- inputs only.
$V_{IH,}$ DC PECL	Input High Voltage	V_{VDDO} – 1.165	—	V_{VDDO} – 0.88	Volts	Applies to REFCLK+/- inputs only.
$V_{IDV,}$ AC PECL	PECL Input Differential Voltage	0.4	—	2.00	Vppd	100Ω differential AC termination

Notes on D.C. Characteristics

1. Input pin or bi-directional pin with internal pull-up resistor.
2. Input pin or bi-directional pin without internal pull-up resistor.
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).

Downloaded by Content Team Chartmiter INC on Wednesday, 01 February 2007 06:59:32 PM

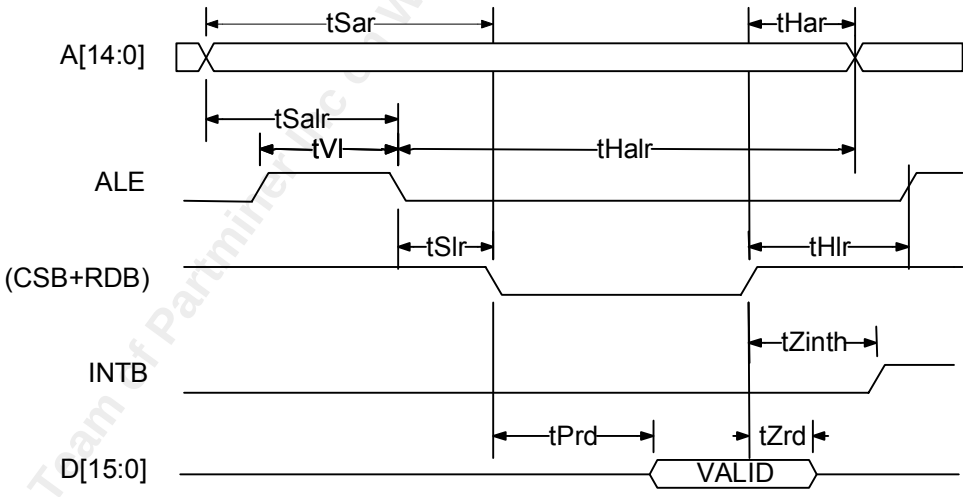
20 A.C. Timing Characteristics

20.1 Microprocessor Interface

Table 58 Microprocessor Interface Read Timing (Figure 56)

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	10	—	ns
tH_{AR}	Address to Valid Read Hold Time	5	—	ns
tS_{ALR}	Address to Latch Set-up Time	10	—	ns
tH_{ALR}	Address to Latch Hold Time	10	—	ns
tV_{L}	Valid Latch Pulse Width	5	—	ns
tS_{LR}	Latch to Read Set-up	0	—	ns
tH_{LR}	Latch to Read Hold	5	—	ns
tP_{RD}	Valid Read to Valid Data Propagation Delay	—	70	ns
tZ_{RD}	Valid Read Negated to Output Tri-state	—	20	ns
tZ_{INTH}	Valid Read Negated to INTB High	—	50	ns

Figure 56 Intel Microprocessor Interface Read Timing



Downloaded by Content Team of Partminer Inc on Wednesday, 07 February 2007 06:59:32 PM

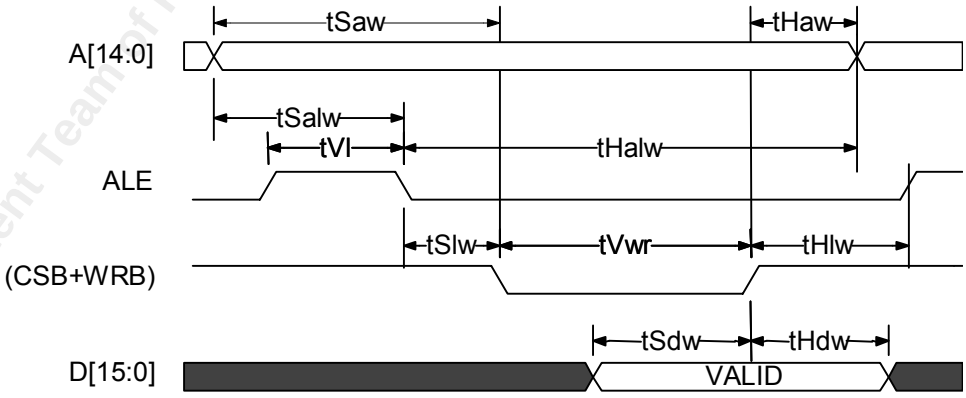
Notes on Microprocessor Interface Read Timing

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[15:0]).
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALR}, tH_{ALR}, tV_L, tS_{LR}, and tH_{LR} are not applicable.
5. Parameter tH_{AR} is not applicable if address latching is used.
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Table 59 Microprocessor Interface Write Timing (Figure 57)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	10	—	ns
tS_{DW}	Data to Valid Write Set-up Time	20	—	ns
tS_{ALW}	Address to Latch Set-up Time	10	—	ns
tH_{ALW}	Address to Latch Hold Time	10	—	ns
tV_L	Valid Latch Pulse Width	5	—	ns
tS_{LW}	Latch to Write Set-up	0	—	ns
tH_{LW}	Latch to Write Hold	5	—	ns
tH_{DW}	Data to Valid Write Hold Time	6~~5~~	—	ns
tH_{AW}	Address to Valid Write Hold Time	5.5~~5~~	—	ns
tV_{WR}	Valid Write Pulse Width	40	—	ns

Figure 57 Intel Microprocessor Interface Write Timing



Downloaded by Content Team of Partsim.com on Wednesday, 07 February 2007 06:59:52 PM

Notes on Microprocessor Interface Write Timing

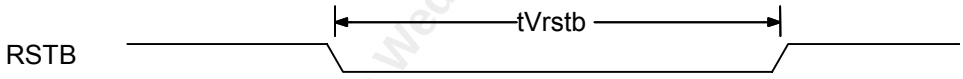
1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.
2. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALW}, tH_{ALW}, tV_L, tS_{LW}, and tH_{LW} are not applicable.
3. Parameter tH_{AW} is not applicable if address latching is used.
4. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
5. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the

20.2 System Miscellaneous Timing

Table 60 System Miscellaneous Timing (Figure 58)

Symbol	Description	Min	Max	Units
tV_{RSTB}	RSTB input pulse width	1	—	ms

Figure 58 System Miscellaneous Timing Diagram Timing



20.3 Line Interface Timing

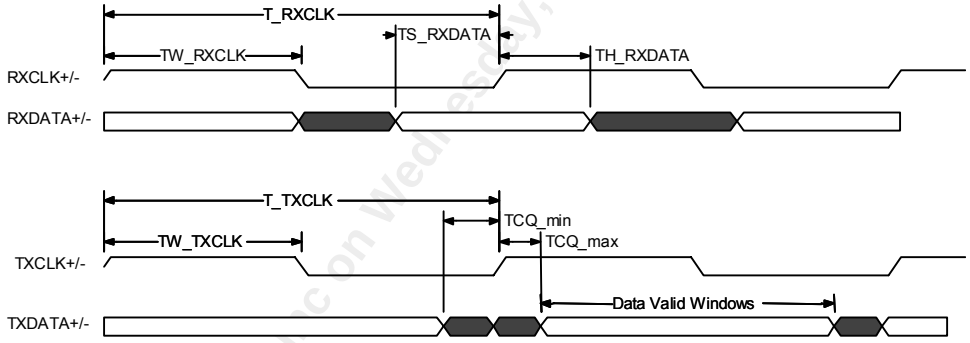
Table 61 Line Interface Timing (Figure 59)

Symbol	Description	Min	Max	Units
f_{RXCLK}	**RXCLK** Frequency* 622.08 MHz +/-100ppm (SFI-4 Line I/F) 644.53125 MHz +/-100ppm (XSBI Line I/F)	—	—	MHz
T_{RXCLK}	RXCLK period nominally 1.60751 ns (SFI-4 Line I/F) nominally 1.55151 ns (XSBI Line I/F)	—	—	ns
TW_{RXCLK}	RXCLK duty cycle	45	55	%
TR_{RXCLK}	RXCLK rise time (20%-80%)	100	400	ps
TF_{RXCLK}	RXCLK fall time (20%-80%)	100	400	ps
TS_{RXCLK}	RXDATA Setup time	300	—	ps
TH_{RXCLK}	RXDATA hold time	300	—	ps
f_{TXCLK_SRC}	**TXCLK_SRC** Frequency 622.08 MHz +/-100ppm (SFI-4 Line I/F) 644.53125 MHz +/-100ppm (XSBI Line I/F)	—	—	MHz

Downloaded by Document Team from Datasheet Engine Inc on Wednesday, 07 February, 2007 06:59:32 PM

Symbol	Description	Min	Max	Units
f_{TXCLK}	**TXCLK** Frequency (TXCLK is a buffered version of the corresponding TXCLK_SRC and is nominally 622.08 MHz or 644.53125 MHz.)			MHz
T_{TXCLK}	TXCLK period nominally 1.60751 ns (SFI-4 Line I/F) nominally 1.55151 ns (XSBI Line I/F)			ns
TW_{TXCLK}	TXCLK duty cycle	40	60	%
TR_{TXCLK}	TXCLK rise time (20%-80%)	100	250	ps
TF_{TXCLK}	TXCLK fall time (20%-80%)	100	250	ps
TCQ_{TXCLK}	TXDATA propagation delay	-200	200	ps
* During Loss of Signal or Out of Lock condition at the optic module/SERDES, up to +/-2500ppm deviation from nominal operating frequency is tolerated. TR_{TXCLK} and TF_{TXCLK} assume a load of 1pF.				

Figure 59 Line Interface Timing



PMC-Sierra's LVDS I/Os operate according to IEEE 1596.3-1996. The transmitter drives a differential signal through a pair of 50 Ω characteristic interconnects, such as board traces, backplane traces, or short lengths of cable. The receiver presents a 100 Ω differential termination impedance to terminate the lines. Included in the standard is sufficient common-mode range for the receiver to accommodate as much as 925 mV of common-mode ground difference.

20.4 APS Port Timing

Table 62 APS Port Timing

Symbol	Description	Min	Typ	Max	Units
f_{APS}	**IAPSFPCLK** Frequency (IAPSFPCLK is nominally 77.76 MHz)	—	—	—	MHz

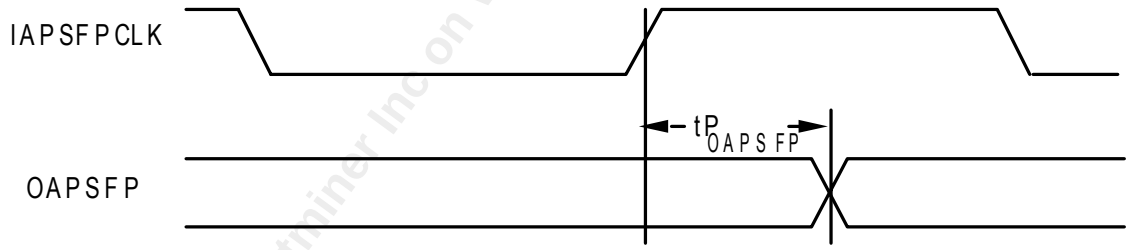
Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Symbol	Description	Min	Typ	Max	Units
	IAPSFPCLK duty cycle	40	—	60	%
	IAPSFPCLK rise time (20%-80%)	200	—	400	ps
	IAPSFPCLK fall time (20%-80%)	200	—	400	ps
f_{IOLVDS}	IAPS[4:1][3:0]+/-, OAPS[4:1][3:0]+/- Bit-rate	$10*f_{APS}$ – 100 ppm	$10*f_{APS}$	$10*f_{APS}$ + 100 ppm	—
	IAPS+/-, OAPS+/- Differential Skew	—	—	50	ps
tP_{OAPSFP}	IAPSFPCLK rising edge to OAPSFP valid	3	12	ns	—

The minimum and maximum fIOLVDS specification is to accommodate transients between generated clocks. The mean data rate on the input and output APS ports must be exactly 10*fAPS. FIFO overrun/underrun in the R8TD and T8TE blocks will result if the mean data rate differs from 10*fAPS. A common system clock (IAPSFPCLK) needs to be used for all devices with serial TelecomBus interfaces.

PMC-Sierra's LVDS I/Os operate according to IEEE 1596.3-1996. The transmitter drives a differential signal through a pair of 50 Ω characteristic interconnects, such as board traces, backplane traces, or short lengths of cable. The receiver presents a 100 Ω differential termination impedance to terminate the lines. Included in the standard is sufficient common-mode range for the receiver to accommodate as much as 925 mV of common-mode ground difference.

Figure 60 OAPSFP Output Timing



20.5 Receive Overhead Port Timing

Table 63 RTOHCLK1-4 Output Timing (Full TOH Bytes) (Figure 61)

Symbol	Description	Min	Max	Units
	RTOHCLK[4:1] (RTOHCLK is nominally 82.94 MHz and is generated by gapping an internal 103.68 MHz receive line clock)	—	—	—
	RTOHCLK[4:1] Duty Cycle (for consecutive transitions of the gapped clock)	3040	7060	%
tP_{RTOHFP}	RTOHCLK1-4 rising edge to RTOHFP1-4 valid	1	5	ns
tP_{RTOH}	RTOHCLK1-4 rising edge to RTOH1-4 valid	1	5	ns

Downloaded by Content Team of Partminer Inc on Wednesday 07 February 2007 at 08:32:10

Figure 61 RTOHCLK1-4 Output Timing (Full TOH Bytes)

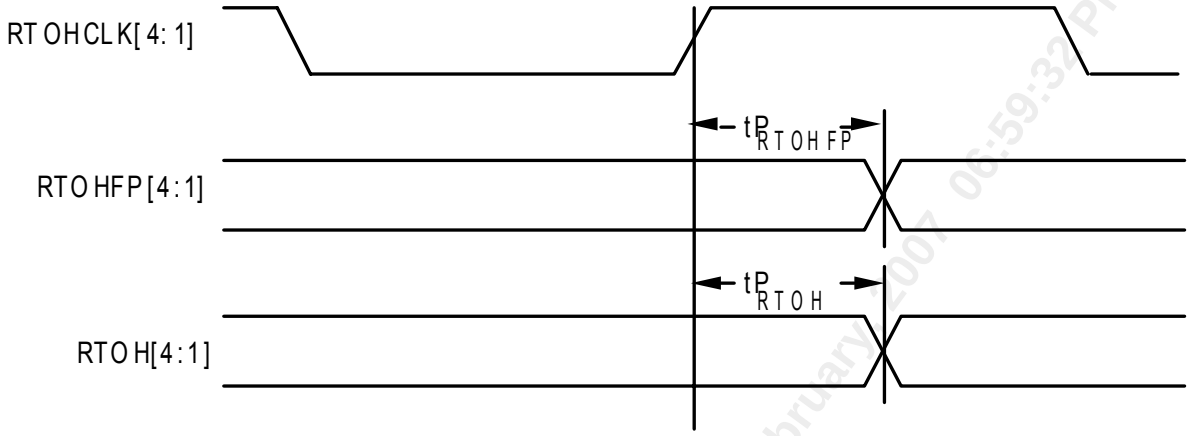


Table 64 RTOHCLK1-4/RPOHCLK1-4 Output Timing (DCC Bytes) (Figure 62)

Symbol	Description	Min	Max	Units
$F_{RTOHCLK/RPOHCLK}$	RTOHCLK/RPOHCLK Frequency in DCC mode	192 or 576		KHz
$tP_{RTOH/RPOH}$	RTOHCLK/RPOHCLK falling edge to RTOH/RPOH valid	-250	0	ns
$tP_{RTOHFP/RPOHFP}$	ROHFP output setup time to RSLDCLK rising edge	-250	0	ns

Figure 62 RTOHCLK1-4/RPOHCLK1-4 Output Timing (DCC Bytes)

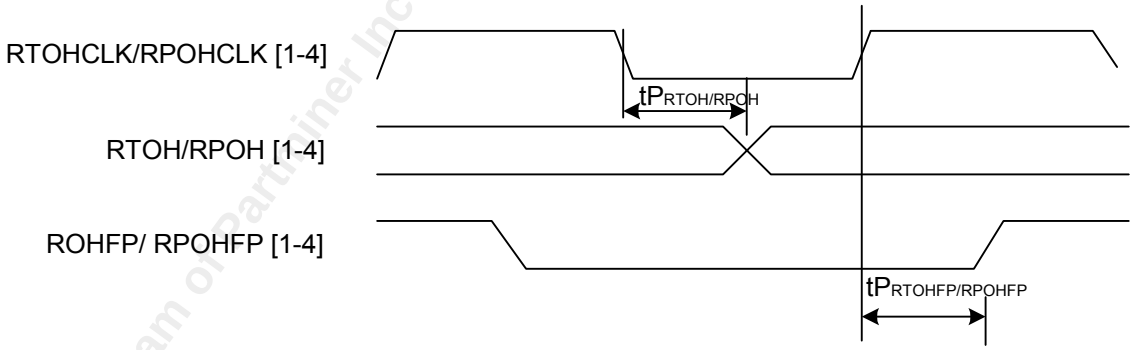


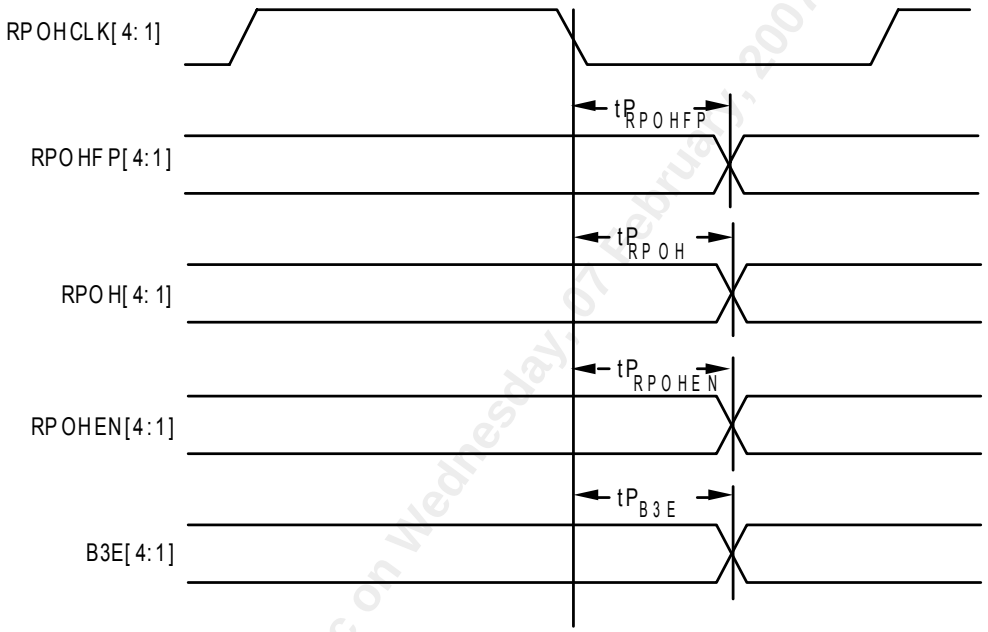
Table 65 RPOHCLK1-4 Output Timing (Full POH Bytes) (Figure 63)

Symbol	Description	Min	Max	Units
	RPOHCLK[4:1] (RPOHCLK is nominally 20.736 MHz and is generated by gapping an internal 25.92 MHz receive line clock)	—	—	—
	RPOHCLK[4:1] Duty Cycle (for consecutive transitions of the gapped clock)	30	70	%

Downloaded by Element Team of Partminer Inc on Wednesday, 07 February 2007 06:59:32 PM

Symbol	Description	Min	Max	Units
tP_{RPOHFP}	RPOHCLK1-4 falling edge to RPOHFP1-4 valid	-6	6	ns
tP_{RPOH}	RPOHCLK1-4 falling edge to RPOH1-4 valid	-6	6	ns
tP_{RPOHEN}	RPOHCLK1-4 falling edge to RPOHEN1-4 valid	-6	6	ns
tP_{B3E}	RPOHCLK1-4 falling edge to B3E1-4 valid	-6	6	ns

Figure 63 RPOHCLK1-4 Output Timing (Full POH Bytes)



20.6 Transmit Overhead Port Timing

Table 66 TTOHCLK1-4 Input Timing (Full TOH Bytes) (Figure 64)

Symbol	Description	Min	Max	Units
	TTOHCLK[4:1] (TTOHCLK is nominally 82.94 MHz and is generated by gapping an internal 103.68 MHz transmit line clock)	—	—	—
	TTOHCLK[4:1] Duty Cycle (for consecutive transitions of the gapped clock)	30~~40~~	70~~60~~	%
tS_{TTOH}	TTOH1-4 Set-up time to TTOHCLK1-4 rising edge	3.5	—	ns
tH_{TTOH}	TTOH1-4 Hold time to TTOHCLK1-4 rising edge	0	—	ns
tS_{TTOHEN}	TTOHEN1-4 Set-up time to TTOHCLK1-4 rising edge	3.5	—	ns
tH_{TTOHEN}	TTOHEN1-4 Hold time to TTOHCLK1-4 rising edge	0	—	ns

Downloaded by Content Technologies Singapore Inc on Wednesday, 07 February, 2007 06:59:32 PM

Figure 64 TTOHCLK1-4 Input Timing (Full TOH Bytes)

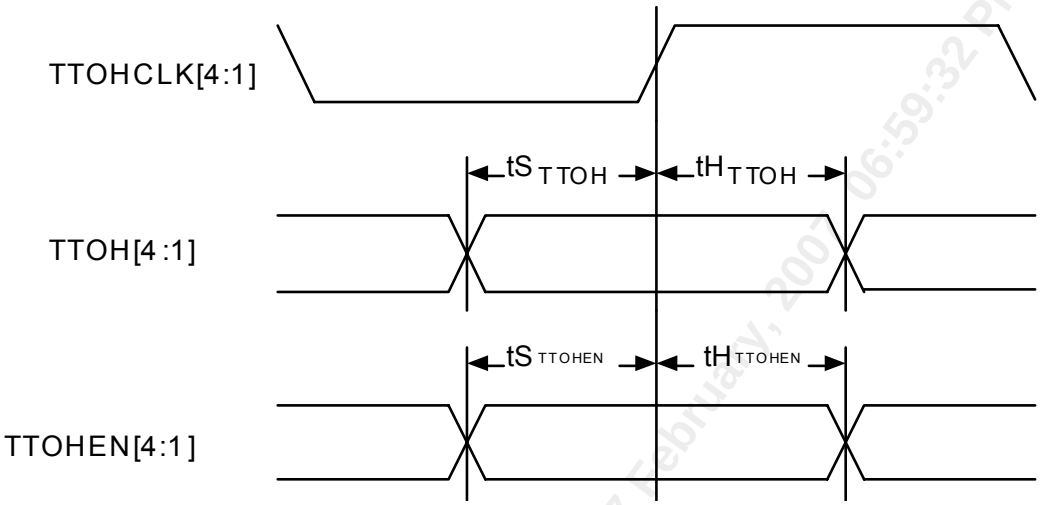


Table 67 TTOHCLK1-4 Output Timing (Full TOH Bytes) (Figure 65)

Symbol	Description	Min	Max	Units
tP_{TTOHFP}	TTOHCLK1-4 rising edge to TTOHFP1-4 valid	1	5	ns

Figure 65 TTOHCLK1-4 Output Timing (Full TOH Bytes)

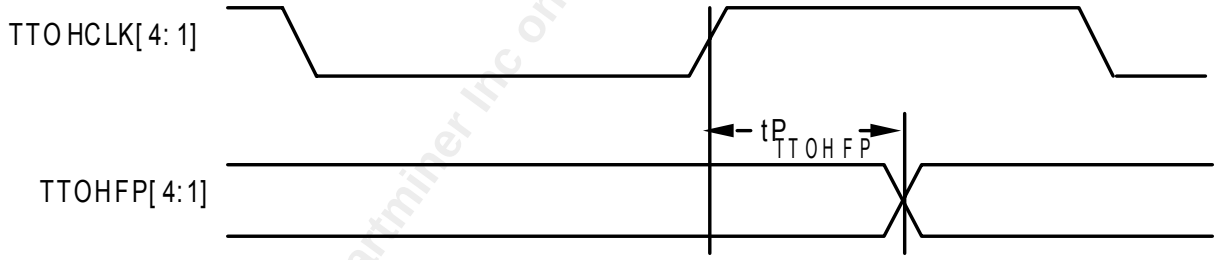


Table 68 TTOHCLK1-4/TPOHCLK1-4 Input/Output Timing (DCC Bytes) (Figure 66)

Symbol	Description	Min	Max	Units
$F_{TTOHCLK/TPOHCLK}$	TTOHCLK/TPOHCLK Frequency	192 or 576		KHz
$tS_{TTOH/TPOH}$	TTOH/TPOH Set-up time to TTOHCLK/TPOHCLK rising edge	50		ns
$tH_{TTOH/TPOH}$	TTOH/TPOH Hold time to TTOHCLK/TPOHCLK rising edge	250		ns
$tP_{TTOHFP/TPOHFP}$	TTOHFP/TPOHFP output setup time to TTOHCLK/TPOHCLK rising edge	-250	0	ns

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

Figure 66 TTOHCLK1-4/TPOHCLK1-4 Input /Output Timing (DCC Bytes)

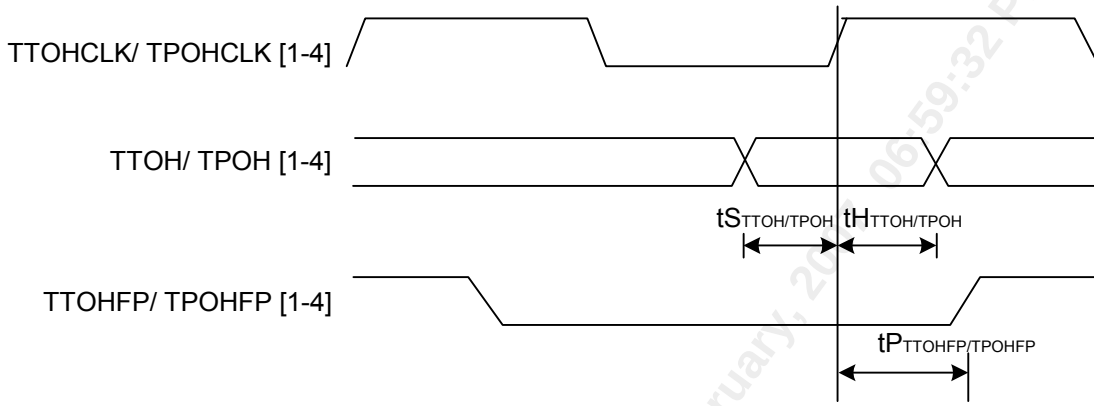
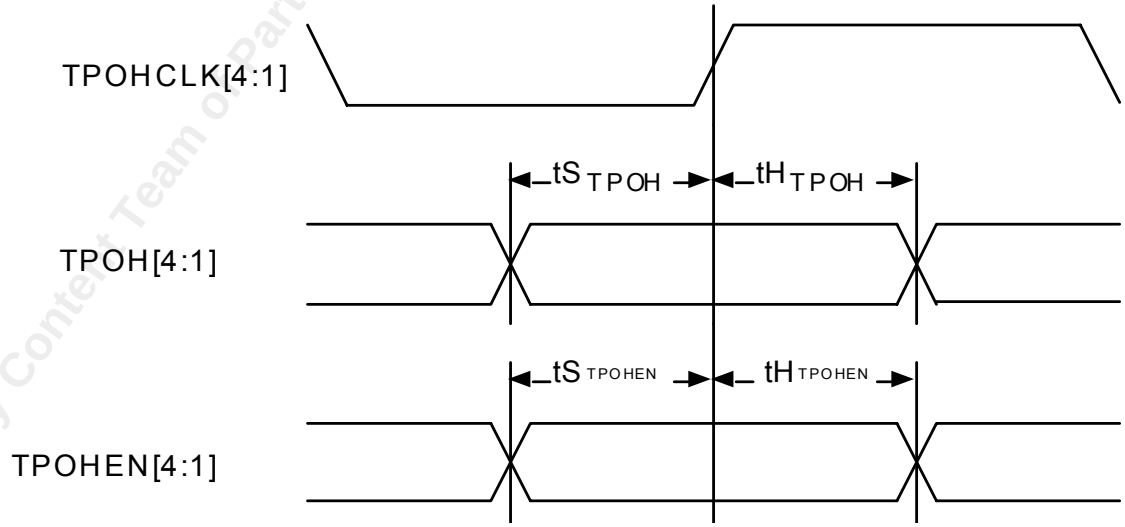


Table 69 TPOHCLK1-4 Input Timing (Full POH Bytes) (Figure 67)

Symbol	Description	Min	Max	Units
	TPOHCLK[4:1] (TPOHCLK is nominally 20.736 MHz and is generated by gapping an internal 25.92 MHz transmit line clock)	—	—	—
	TPOHCLK[4:1] Duty Cycle (for consecutive transitions of the gapped clock)	30	70	%
tS_{TPOH}	TPOH1-4 Set-up time to TPOHCLK1-4 rising edge	12	—	ns
tH_{TPOH}	TPOH1-4 Hold time to TPOHCLK1-4 rising edge	0	—	ns
tS_{TPOHEN}	TPOHEN1-4 Set-up time to TPOHCLK1-4 rising edge	10	—	ns
tH_{TPOHEN}	TPOHEN1-4 Hold time to TPOHCLK1-4 rising edge	0	—	ns

Figure 67 TPOHCLK1-4 Input Timing (Full POH Bytes)

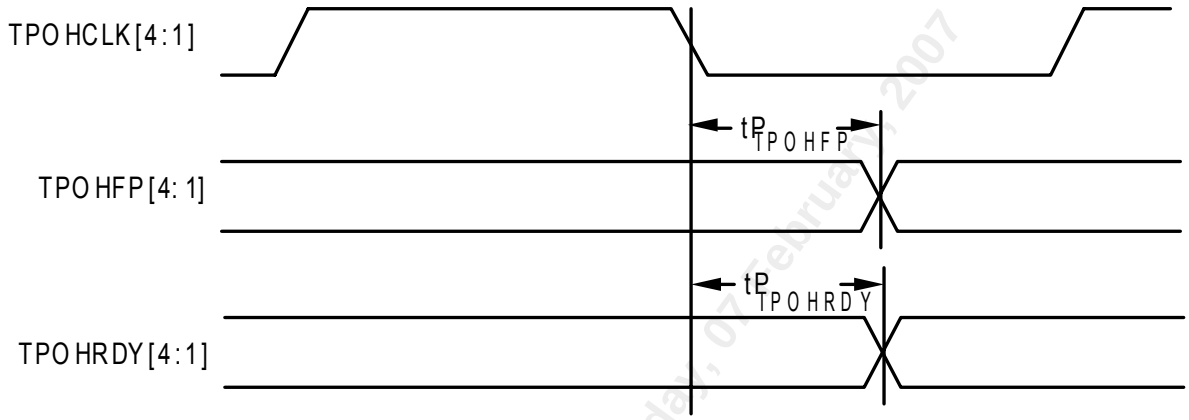


Downloaded by Content Team of Partmaster Online Tuesday, 27 February, 2007 06:59:32 PM

Table 70 TPOHCLK1-4 Output Timing (Full POH Bytes) (Figure 68)

Symbol	Description	Min	Max	Units
tP_{TPOHFP}	TPOHCLK1-4 falling edge to TPOHFP1-4 valid	-6	6	ns
$tP_{TPOHRDY}$	TPOHCLK1-4 falling edge to TPOHRDY1-4 valid	-6	6	ns

Figure 68 TPOHCLK1-4 Output Timing (Full POH Bytes)



20.7 PL4 Interface Timing

20.7.1 Interpretation of the SPI-4-II/PL4 Standards for LVDS Electrical, Jitter and Skew Specifications

This section provides clarification and supplemental information regarding the Electrical Specifications of PMC-Sierra's POS-PHY Level 4 interface implemented on the Xenon Family of devices. The information provided in this section is specific to PMC-Sierra's implementation of the PL4/SPI-4 Phase II standard and provides additional clarification of performance specifications outlined in the standards that are ambiguous or incomplete.

LVDS Electrical

The LVDS electrical specifications for the PMC PL4/SPI-4-II interfaces are given in Table 45. It should be noted that the PL4/SPI-4-II standards just reference the IEEE and TIA LVDS standards for the LVDS electrical specifications. In some cases these two standards differ, as well as being different than the SFI-4-I standard.

Table 71 LVDS Electrical Specifications

Symbol	Parameter	Comments	TYP	Units
t_R, t_F	Input 20%-80% Rise & Fall Times	See Notes 1 & 2	0.36	UI
t_R, t_F	Output 20%-80% Rise & Fall Times	—	175	ps

Downloaded by [illegible] on Wednesday, 07 February, 2007 06:59:32 PM

Notes

1. Same as the PL4/SPI-4-II standards.
2. Rise/fall times are measured from the 20% to 80% thresholds

20.7.2 Reference Clock Interface

The data in Table 72 and Table 73 is for the reference clock when in Master mode. This data is not part of the PL4/SPI-4-II standards (no specifications are given for refclk input).

Table 72 Reference Clock Timing Specifications for divBy2 (PL4_REFCLK)

Symbol	Parameter	Min	Typ	Max	Units	Comments
fD	Reference Clock Frequency	311	—	350	MHz	Not in the PL4/SPI-4-II standards
DCref	Reference Clock Duty Cycle	40	—	60	%	
DJref	Reference Clock Deterministic Jitter (pk-to-pk between fD/1000 & 8MHz) (pk-to-pk between fD/1000 & fD)	—	—	 0.01 0.05	 UI UI	
TJref	Reference Clock Total Jitter (pk-to-pk between fD/1000 & fD)	—	—	0.10	UI	
tRFref	Reference Clock Rise / Fall Times		1.0	—	ns	

Notes on Reference Clock Timing

1. Master Mode and divBy2 (REFSEL[0] = "1" & REFSEL[1] = “0”).
2. The Unit Interval (UI) is the reciprocal of the symbol rate.
3. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
4. Values are measured with each PECL/LVDS input DC coupled into a 50 Ohm impedance (100 Ohms differential impedance).
5. Rise time is measured from the 10% threshold of the reference signal to the 90% threshold of the reference signal.
6. Fall time is measured from the 90% threshold of the reference signal to the 10% threshold of the reference signal.
7. Duty cycle and jitter are specified between differential crossings of the 50% threshold of the reference signal.

Table 73 Reference Clock Timing Specifications for divBy4 (PL4_REFCLK)

Symbol	Parameter	Min	Typ	Max	Units	Comments
fD	Reference Clock Frequency	155.5		175	MHz	Not in the PL4/SPI-4-II standards
DCref	Reference Clock Duty Cycle	40		60	%	
DJref	Reference Clock Deterministic Jitter (pk-to-pk between fD/500 & 8MHz) (pk-to-pk between fD/500 & 2*fD)			 0.01 0.05	 UI UI	
TJref	Reference Clock Total Jitter (pk-to-pk between fD/500 & 2*fD)			0.10	UI	
tRFref	Reference Clock Rise / Fall Times		1.0		ns	

Notes on Reference Clock Timing

1. Master Mode divBy4 (REFSEL[0] = "1" & REFSEL[1] = “1”).

Downloaded by Content Team of Partminer Incon Wednesday, 07 February 2007 10:59:32 PM

2. The Unit Interval (UI) is the reciprocal of the symbol rate.
3. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
4. Values are measured with each PECL/LVDS input DC coupled into a 50 Ohm impedance (100 Ohms differential impedance).
5. Rise time is measured from the 10% threshold of the reference signal to the 90% threshold of the reference signal.
6. Fall time is measured from the 90% threshold of the reference signal to the 10% threshold of the reference signal.
7. Duty cycle and jitter are specified between differential crossings of the 50% threshold of the reference signal.

20.7.3 Data Interface

The data in Table 74 and Table 75 give output and input specifications for the data and clock lanes.

Table 74 Output Data Timing (RDCLK, RCTL, RDAT)

Symbol	Parameter	Min	Typ	Max	Units	Comments
Dcoc	Output Clock Duty Cycle	45	—	55	%	—
fD	Output Clock Frequency	311	—	350	MHz	Max is not in the PL4/SPI-4-II standards
TJoc	Output Clock Total Jitter (pk-to-pk between fD/1000 & fD)	—	—	0.10	UI	With max allowed jitter on PL4_REFCLK/TDCLK
DJod	Output Data Deterministic Jitter (pk-to-pk between fD/1000 & fD)	—	—	0.12	UI	Not in the PL4/SPI-4-II standards With max allowed jitter on PL4_REFCLK/TDCLK
TJod	Output Data Total Jitter (pk-to-pk between fD/1000 & fD)	—	—	0.19	UI	PL4/SPI-4-II standards give a max of 0.24UI With max allowed jitter on PL4_REFCLK/TDCLK
tCDSout	Output Clock lane to any Data lane Skew	—	—	±280	ps	
tDSout	Output Differential Skew	—	±20	—	ps	—

Notes on Output Timing

1. The Unit Interval (UI) is the reciprocal of the symbol rate for both clock and data.
2. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.

Downloaded by Content Team of Chartmineral on Wednesday, 07 February, 2007 06:39:39 PM

3. Values are measured with each LVDS output DC coupled into a 50 Ohm impedance (100 Ohms differential impedance).
4. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

Table 75 Input Data Timing (TDCLK, TCTL, TDAT)

Symbol	Parameter	Min	Typ	Max	Units	Comments
Dcic	Input Clock Duty Cycle	40	—	60	%	See note #1
fD	Input Clock Frequency	311	—	350	MHz	
DJic	Input Clock Deterministic Jitter (pk-to-pk between fD/1000 & 8MHz) (pk-to-pk between fD/1000 & fD)	—	—	0.01 0.10	UI UI	See note #1 Max not in the PL4/SPI-4-II standards
TJic	Input Clock Total Jitter (pk-to-pk between fD/1000 & fD)	—	—	0.17	UI	
DJid	Input Data Deterministic Jitter (pk-to-pk between fD/1000 & fD, and no jitter on PL4_REFCLK/TDCLK)	—	—	0.36	UI	See note #2 Not in the PL4/SPI-4-II standards
TJid	Input Data Total Jitter (pk-to-pk between fD/1000 & fD, and no jitter on PL4_REFCLK/TDCLK)	—	—	0.65	UI	
tDDSin	Input Data to Data Skew (any pair of data signals)	—	—	±1.0	UI	—
tDSin	Input Differential Skew	—	±60	—	ps	—

Notes on Input Timing

1. Spec's on TDCLK (Dcoc, fD, DJic & TJic) only valid when in Slave Mode (REFSEL[0] = "0" & REFSEL[1] = "0"), as TDCLK is not required when in either Master mode.
2. When in Master Mode and divBy4, the "fD" in DJid & TJid is twice value of the PL4_REFCLK frequency. When in Master Mode and divBy2, the "fD" in DJid & TJid is the same as the PL4_REFCLK frequency.
3. The Unit Interval (UI) is the reciprocal of the symbol rate for both clock and data.
4. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
5. Values are measured with each LVDS input DC coupled into a 50 Ohm impedance (100 Ohms differential impedance).
6. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

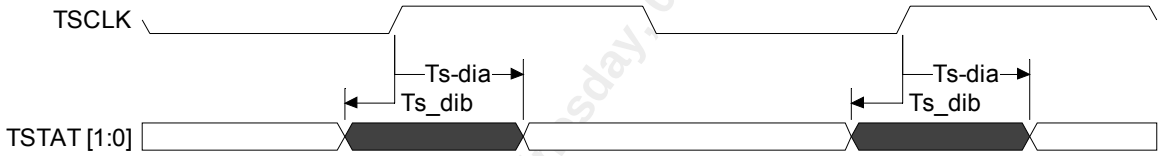
Downloaded by Conexant Systems Inc on Wednesday, 07 February, 2007 16:59:32 PM

20.7.4 PL4 FIFO Status Interface

Table 76 Output Status Timing (TSCLK, TSTAT[1:0])

Symbol	Parameter	Min	Typ	Max	Units
PL4_Fos	TSCLK Frequency	1/4	—	1/4	See Note #1
PL4_Dcos	TSCLK Duty Cycle	40	—	60	%
—	—	—	—	—	—
PL4_Ts_dib	TSTAT[1:0] Invalid Window Before Rising Edge of TSCLK (at PM5390 pins)	—	—	1.0	ns
PL4_Ts_dia	TSTAT[1:0] Invalid Window After Rising Edge of TSCLK (at PM5390 pins)	—	—	2.5	ns

Figure 69 PL4 Bus Output Status AC Timing Diagram



Notes on PL4 Output Status Timing

1. The TSCLK frequency is one-quarter of the TDCLK frequency.
2. Assumes a load of 30 pF on the TSCLK and TSTAT[1:0] outputs.
3. Rise time is measured from the 0.8 Volt threshold of the reference signal to the 2.0 Volt threshold of the reference signal.
4. Fall time is measured from the 2.0 Volt threshold of the reference signal to the 0.8 Volt threshold of the reference signal.
5. Duty cycle and skew are specified between crossings of the 1.4 Volt threshold of the reference signal.

Table 77 Input Status Timing (RSCLK, RSTAT[1:0])

Symbol	Parameter	Min	Typ	Max	Units
PL4_Fis	RSCLK Frequency	—	—	1/4	See Note #1
PL4_DCis	RSCLK Duty Cycle	35	—	65	%
—	—	—	—	—	—
PL4_tSis	RSTAT[1:0] to Rising Edge RSCLK Setup (at PM5390 pins)	2.0	—	—	ns
PL4_tHis	RSTAT[1:0] to Rising Edge RSCLK Hold (at PM5390 pins)	0.5	—	—	ns

Downloaded by Content Team of Datasheet Inc. on Wednesday, 07 February 2007 06:39:39 PM

Figure 70 PL4 Bus Input Status AC Timing Diagram

Notes on PL4 Input StatusTiming

1. The maximum RSCLK frequency shall not exceed one-quarter of the RDCLK frequency.
2. Rise time is measured from the 0.8 Volt threshold of the reference signal to the 2.0 Volt threshold of the reference signal.
3. Fall time is measured from the 2.0 Volt threshold of the reference signal to the 0.8 Volt threshold of the reference signal.
4. Duty cycle, setup and hold are specified between crossings of the 1.4 Volt threshold of the reference signal.

20.8 System Clock Output Timing

Table 78 RCLK1-4, PGMRCLK1-4, TCLK1-4 and PGMTCLK1-4 Output Timing

Symbol	Description	Min	Max	Units
	RCLK[4:1] (RCLK is a divide-by-8 of the corresponding receive line clock. For quad OC-48 operation, RCLK[N] is a divided version of the receive line clock, RXCLK[N]+/-. For OC-192 or 10 Gigabit Ethernet LAN PHY operation, RCLK[N] is a divided version of the receive line clock, RXCLK2+/-. For quad OC-48 or OC-192 operation, RCLK is a nominally 77.76 MHz, 50% duty cycle clock. For 10 Gigabit Ethernet LAN PHY operation, RCLK is a nominally 80.57 MHz, 50% duty cycle clock.)	—	—	—
	RCLK[4:1] Duty Cycle	45	55	%
	PGMRCLK[4:1] (PGMRCLK is derived by dividing down the corresponding receive line clock when operating in SONET/SDH mode. For quad OC-48 mode, PGMRCLK[N] is a divided version of the receive clock, RXCLK[N]+/-. For OC-192 mode, PGMRCLK[N] is a divided version of the receive clock, RXCLK2+/-. PGMRCLK[N] can be programmed to be a nominal 8 kHz, 19.44 MHz or 77.76 MHz, 50% duty cycle clock or forced to low by setting the PGMRCLKSEL[N][1:0] bits in SRLI Programmable Clock Configuration register. PGMRCLK[4:1] are also forced to low in 10 Gigabit Ethernet LAN PHY mode.)	—	—	—
	PGMRCLK[4:1] Duty Cycle	45	55	%
	TCLK[4:1] (TCLK is a divide-by-8 of the corresponding transmit line clock. For quad OC-48 operation, TCLK[N] is a divided version of the transmit source clock, TXCLK_SRC[N]+/-.	—	—	—

Downloaded by Content Team, Engineering, Wednesday, 07 February 2007 09:59:32 PM

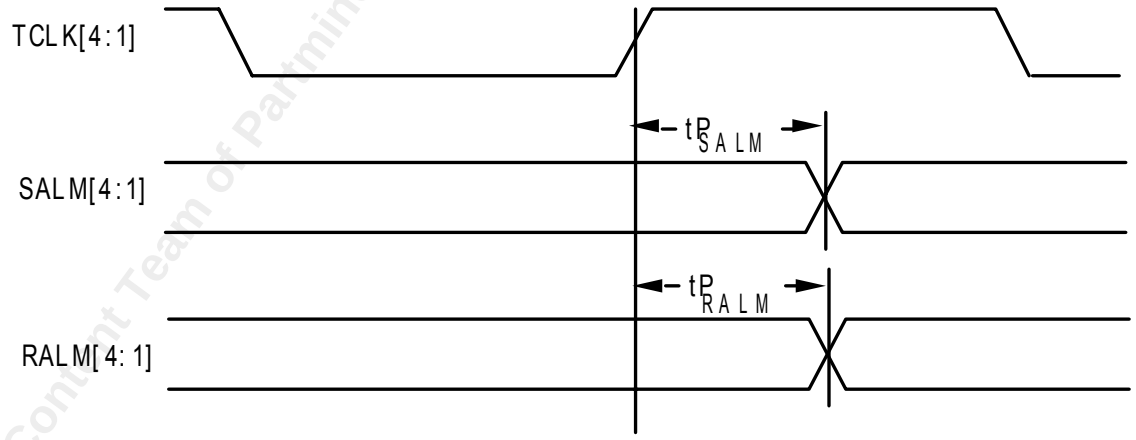
Symbol	Description	Min	Max	Units
	For OC-192 or 10 Gigabit Ethernet LAN PHY operation, TCLK[N] is a divided version of the transmit source clock, TXCLK_SRC2+/-. For quad OC-48 or OC-192 operation, TCLK is a nominally 77.76 MHz, 50% duty cycle clock. For 10 Gigabit Ethernet LAN PHY operation, TCLK is a nominally 80.57 MHz, 50% duty cycle clock.)			
	TCLK[4:1] Duty Cycle	45	55	%
	PGMTCLK[4:1] (PGMTCLK is derived by dividing down the corresponding transmit line clock when operating in SONET/SDH mode. For quad OC-48 operation, PGMTCLK[N] is a divided version of the transmit source clock, TXCLK_SRC[N]+/-. For OC-192 operation, PGMTCLK[N] is a divided version of the transmit source clock, TXCLK_SRC2+/-. PGMTCLK[N] can be programmed to be a nominal 8 kHz, 19.44 MHz or 77.76 MHz, 50% duty cycle clock or forced to low by setting the PGMTCLKSEL[N][1:0] bits in STLI PGM Clock Configuration register. PGMTCLK[4:1] are also forced to low in 10 Gigabit Ethernet LAN PHY mode.)	—	—	—
	PGMTCLK[4:1] Duty Cycle	45	55	%

20.9 Receive Alarm Output Timing

Table 79 SALM1-4 and RALM1-4 Output Timing (Figure 71)

Symbol	Description	Min	Max	Units
tP_{SALM}	TCLK1-4 rising edge to SALM1-4 valid	1	6.5	ns
tP_{RALM}	TCLK1-4 rising edge to RALM1-4 valid	1	6.5	ns

Figure 71 SALM1-4 and RALM1-4 Output Timing



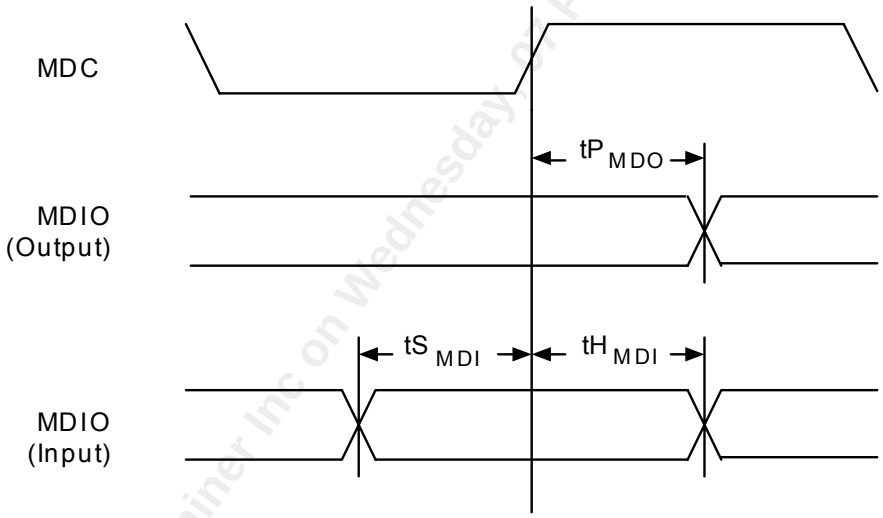
Downloaded by Content Team of Partminer on Wednesday, 07-February, 2007 05:59:32 PM

20.10 MDIO Port Timing

Table 80 MDIO Port Timing (Figure 72)

Symbol	Description	Min	Max	Units
	MDC Frequency (MDC is a CPREF_CLK/32 MHz nominally 50% duty cycle clock.)	—	—	MHz
	MDC Duty Cycle	45	55	%
tS_{MDI}	MDIO Set-up time to MDC rising edge	25	—	ns
tH_{MDI}	MDIO Hold time to MDC rising edge	0	—	ns
tP_{MDO}	MDC rising edge to MDIO Valid	10	40	ns

Figure 72 MDIO Port Timing



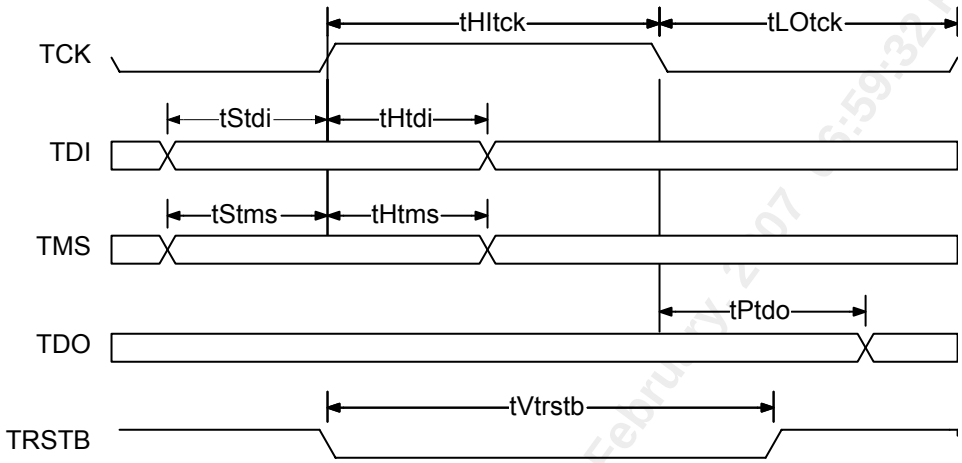
20.11 JTAG Port Timing

Table 81 JTAG Port Interface (Figure 73)

Symbol	Description	Min	Max	Units
f_{TCK}	TCK Frequency	—	4	MHz
tHI_{TCK}	TCK HI Pulse Width	100	—	ns
tLO_{TCK}	TCK LO Pulse Width	100	—	ns
tS_{TMS}	TMS Set-up time to TCK	25	—	ns
tH_{TMS}	TMS Hold time to TCK	25	—	ns
tS_{TDI}	TDI Set-up time to TCK	25	—	ns
tH_{TDI}	TDI Hold time to TCK	25	—	ns
tP_{TDO}	TCK Low to TDO Valid	2	25	ns
tV_{TRSTB}	TRSTB Pulse Width	100	—	ns

Downloaded by Department Team of Portminer Inc on Wednesday 07 February 2007 06:59:22 PM

Figure 73 JTAG Port Interface Timing



Notes on Input Timing

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on Output Timing

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum output propagation delays are measured with an 80 pF load on the outputs at the Microprocessor, MDIO and the JTAG interfaces.
3. Maximum output propagation delays are measured with a 30 pF load on the outputs except when otherwise specified.

Downloaded by Content Team of Partminer.com Wednesday, 07 February 2007 06:59:32 PM

21 Thermal Information

This product is designed to operate over a wide temperature range when used with a heat sink and is suited for outside plant equipment[1].

Table 82 Outside Plant Thermal Information

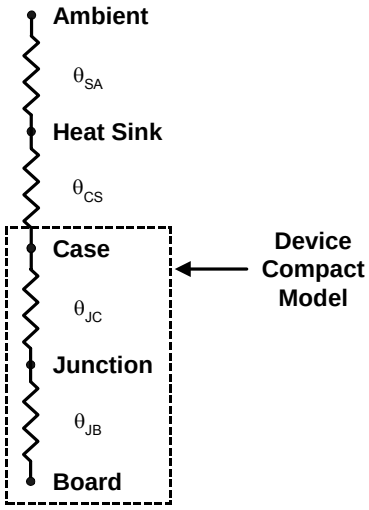
Maximum long-term operating junction temperature (T_J) to ensure adequate long-term life.	105 °C
Maximum junction temperature (T_J) for short-term excursions with guaranteed continued functional performance[2]. This condition will typically be reached when the local ambient temperature reaches 85 °C.	125 °C
Minimum ambient temperature (T_A)	-40 °C

Table 83 Device Compact Model[3]

Junction-to-Case Thermal Resistance, θ_{JC}	0.19 °C/W
Junction-to-Board Thermal Resistance, θ_{JB}	3.5 °C/W

Table 84 Heat Sink Requirements

$\theta_{SA}+\theta_{CS}$[4]	The sum of θ_{SA} + θ_{CS} must be less than or equal to: $[[(105 - T_A) / P_D] - \theta_{JC}]$ °C/W where: T_A is the ambient temperature at the heat sink location P_D is the operating power dissipated in the package
	θ_{SA} and θ_{CS} are required for long-term operation



Power depends upon the operating mode. To obtain power information, refer to 'High' power values in section 18.1 Power Requirements.

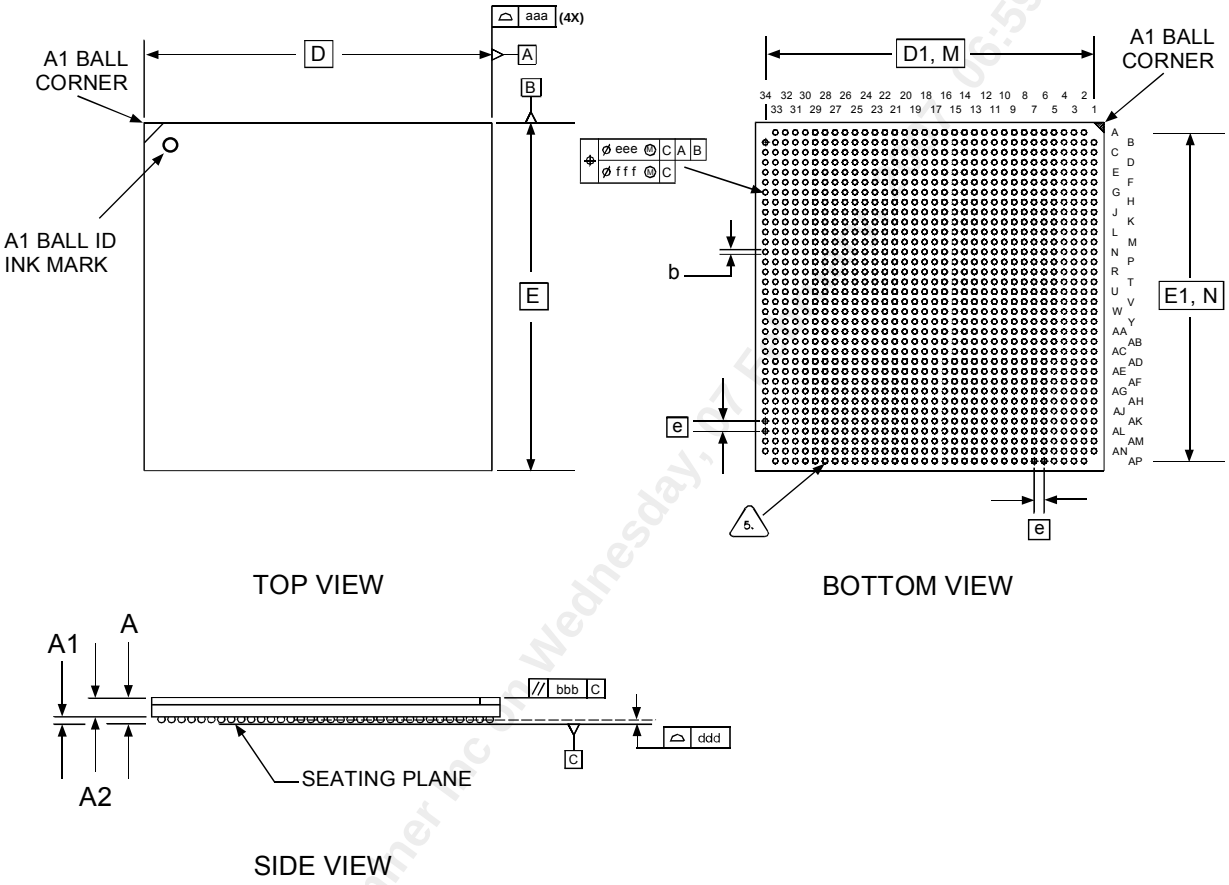
Notes

1. The minimum ambient temperature requirement for Outside Plant Equipment meets the minimum ambient temperature requirement for Industrial Equipment
2. Short-term is used as defined in Telcordia Technologies Generic Requirements GR-63-Core Core; for more information about this standard, see [35]
3. θ_{JC}, the junction-to-case thermal resistance, is a measured nominal value plus two sigma. θ_{JB}, the junction-to-board thermal resistance, is obtained by simulating conditions described in JEDEC Standard JESD 51-8; for more information about this standard, see [34]
4. θ_{SA} is the thermal resistance of the heat sink to ambient. θ_{CS} is the thermal resistance of the heat sink attached material. The maximum θ_{SA} required for the airspeed at the location of the device in the system with all components in place

Downloaded by Component Control of Perminer Inc. on Wednesday, 07 February, 2007 06:59:32 PM

22 Mechanical Information

Figure 74 1152 PIN FCBGA – 35x35 MM BODY – 3M VERSION

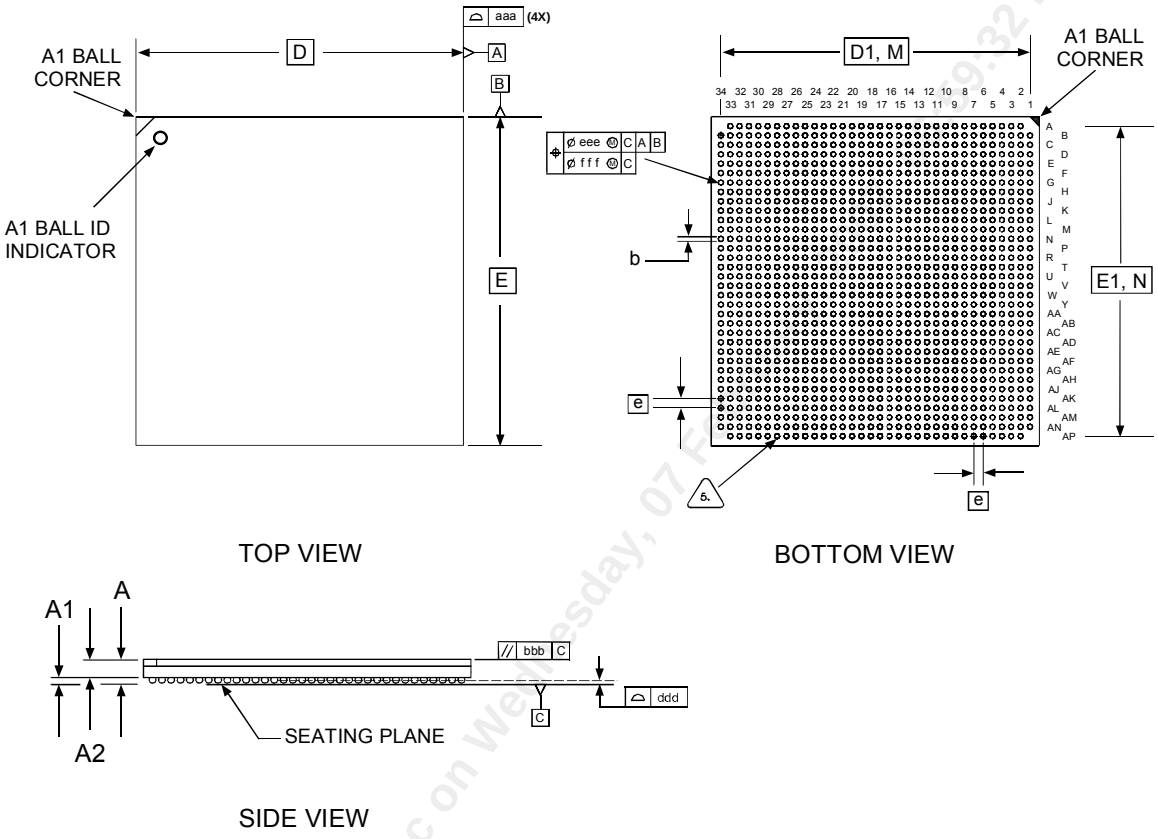


NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES PACKAGE BODY PROFILE.
3) DIMENSION bbb DENOTES PARALLEL.
4) DIMENSION ddd DENOTES COPLANARITY.
5) DIAMETER OF SOLDER MASK OPENING IS 0.530 MM (SMD).

PACKAGE TYPE : 1152 FLIP CHIP BALL GRID ARRAY - FCBGA																
BODY SIZE : 35 x 35 x 2.39 MM (7 LAYERS)																
Dim.	A	A_1	A_2	D	D_1	E	E_1	M,N	b	e	aaa	bbb	ddd	eee	f f f	S
Min.	2.11	0.40	1.71	-	-	-	-	-	0.48	-	-	-	-	-	-	-
Nom.	2.39	0.50	1.89	35.00 BSC	33.00 BSC	35.00 BSC	33.00 BSC	34x34	0.64	1.00 BSC	-	-	-	-	-	-
Max.	2.67	0.60	2.07	-	-	-	-	-	0.76	-	0.20	0.25	0.20	0.30	0.15	

Downloaded by [illegible] Features Partnumber Inc on Wednesday, 17 [illegible] 06:59:32 PM

Figure 75 1152 PIN FCBGA – 35x35 MM BODY – HDBU Substrate



NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES PACKAGE BODY PROFILE.
3) DIMENSION bbb DENOTES PARALLEL.
4) DIMENSION ddd DENOTES COPLANARITY.
5) DIAMETER OF SOLDER MASK OPENING IS 0.530 MM (SMD).
6) PACKAGE COMPLIANT TO JEDEC REGISTERED OUTLINE MS-034, VARIATION AAR-1.

PACKAGE TYPE : 1152 FLIP CHIP BALL GRID ARRAY - FCBGA (HDBU 3_2_3)															
BODY SIZE : 35 x 35 x 3.04 MM															
Dim.	A	A_1	A_2	D	D_1	E	E_1	M,N	b	e	aaa	bbb	ddd	eee	f f f
Min.	2.76	0.40	2.36	-	-	-	-	-	0.50	-	-	-	-	-	-
Nom.	3.04	0.50	2.54	35.00 BSC	33.00 BSC	35.00 BSC	33.00 BSC	34x34	0.64	1.00 BSC	-	-	-	-	-
Max.	3.32	0.60	2.72	-	-	-	-	-	0.70	-	0.20	0.25	0.20	0.25	0.10

Downloaded by Conexant Systems Inc on Wednesday, 07 Feb 2007 09:32 PM

23 Ordering Information

Table 85 Ordering Information

Part	Description
PM5390-FI	S/UNI® 9953 1152-Pin FCBGA (3M Substrate)
PM5390H-FI	S/UNI® 9953 1152-Pin FCBGA (HDBU Substrate)
PM5390-FGI	S/UNI® 9953 1152-Pin FCBGA (HDBU Substrate, RoHS-Compliant)

Downloaded by Content Team of Partminer Inc on Wednesday, 07 February, 2007 06:59:32 PM

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Telecom Interface ICs ***category:***

Click to view products by Microchip ***manufacturer:***

Other Similar products are found below :

MT8888CP1 MT88E45BS1 MT9174AN1 MT88E39ASR1 MT9074AL1 MT9122AP1 PEB4266TV12 S LL62 DS3150TNC1+ DS26334GN+ MT88E46AS1 MT8963AE1 DS26324GNA3+ PM4351-RI PEF41068FV11 S LL8T PEF41068VV12 S LL8U LE58QL022BVC LE58QL022BVCT LE88286DLC LE88276DLCT LE79252BTC RTL8019AS W7100A-S2E-100LQFP M100EVO-LITE HE910NAR206T701 XRT86VL38IB CMX631AD4 XD8870 82V2084PFG CPC5620A CPC5620ATR CPC5621A CPC5621ATR CPC5622A CPC5622ATR DS21455+ DS21348G+ DS2148TN+ CMX673E3 LE88506DVC MT88E39AS1 LE89810BSCT LE89810BSC CMX673D4 CMX683D4 CMX602BD4 MT8967AS1 HC55185AIMZ MT8952BP1 DS3150QN+ DS2149Q+