Frame Engine and Datalink Manager

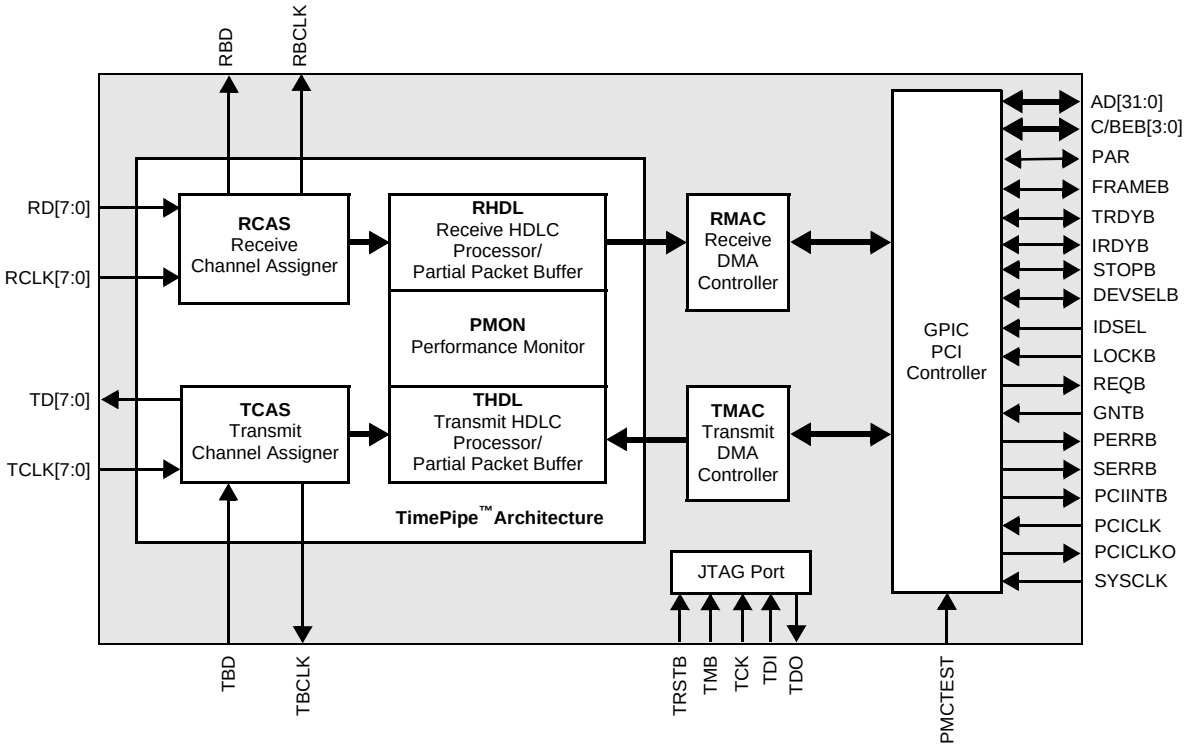
FEATURES

- High density HDLC controller ideal for Internet access, Frame Relay, and DSLAM equipment supporting rates ranging from 56 Kbit/s to 52 Mbit/s.
- Supports eight full-duplex and independently-timed links.
- Supports 128 full-duplex HDLC or transparent channels.
- Supports a TimePipe™ architecture that enables any physical link to be flexibly mapped to one or more HDLC channels.
- Provides 8 KB partial packet FIFO in each transmit and receive direction to compensate for PCI bus latency during data transfers. The 8 KB partial packet FIFO is arranged as 512 blocks of 16-byte buffers.
- The TimePipe architecture supports programmable assignment of partial packet buffers to HDLC channels.
- Two physical links can support up to 52 Mbit/s; the remaining six physical links can individually support up to 10 Mbit/s.
- Supports a mix of channelized and unchannelized links.
- The maximum aggregate clock rate is 64 MHz. When the device is interfaced to two T3 or HSSI links, the maximum aggregate clock rate is 104 MHz.
- For channelized operation, the channel assignment supports up to 24 timeslots for a T1 link and 31 timeslots for an E1 link. Timeslots assigned to a common HDLC channel can be noncontiguous.
- Performs flag delineation, bit de-stuffing, CRC verification using either CRC-32 or CRC-CCITT algorithm, and length checking on receive HDLC channels.
- Performs flag insertion, bit stuffing, and FCS calculation using either CRC-32 or CRC-CCITT algorithm and length checking on transmit HDLC channels.
- On the system side, provides a 33 MHz, 32-bit PCI 2.1-compliant bus interface.
- Implements efficient transmit and receive DMA controllers to support burst data transfers between partial packet FIFO and packet memory.
- Supports scatter-gather capabilities whereby a packet can span multiple buffers.
- Supports line-side loopback on a per-link basis and system-side loopback on a per-HDLC channel basis.
- Pin-compatible and software-compatible with the PM7364 FREEDM-32™.
- Provides a standard 5-signal P1149.1 JTAG test port for boundary scan test board purposes.
- Implemented in low power 3.3 V CMOS technology with 5 V-tolerant inputs.
- Packaged in a 256-pin Ball Grid Array (BGA) package.

APPLICATIONS

- Ideal for applications requiring HDLC, PPP, and transparent protocol processing for physical links, such as T1, E1, T3, E3, xDSL, and HSSI.
- Frame-Based Interfaces for Internet Access and DSLAM equipment.
- FUNI or Frame Relay service interworking interfaces for ATM switches and multiplexers.

BLOCK DIAGRAM



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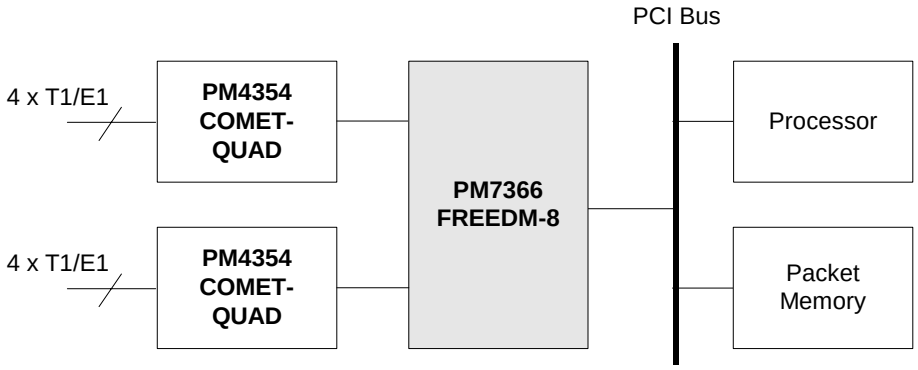
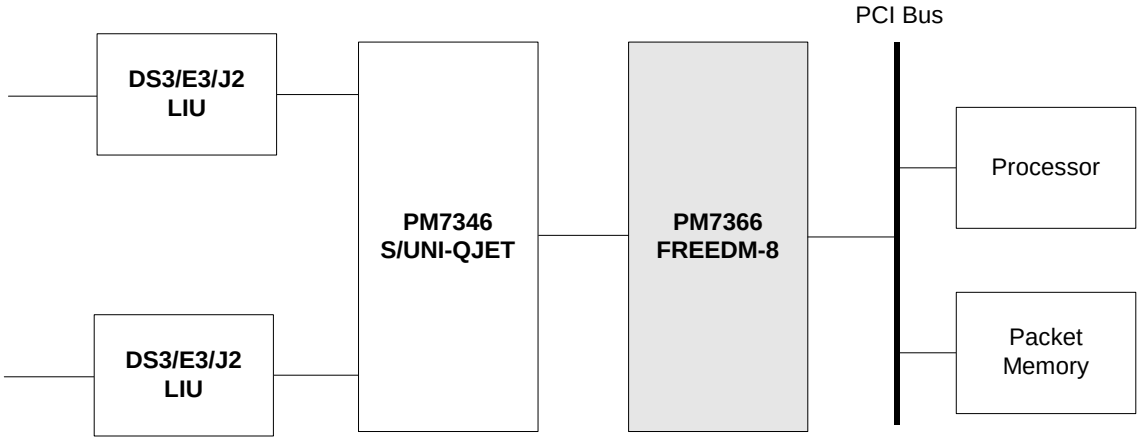
TYPICAL APPLICATIONS

HIGH DENSITY CHANNELIZED AND UNCHANNELIZED T1/E1 INTERFACES



DS3/E3/J2 UPLINK INTERFACES



Head Office:
PMC-Sierra, Inc.
8555 Baxter Place
Burnaby, B.C. V5A 4V7
Canada
Tel: 604.415.6000
Fax: 604.415.6200

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