

**PM8611**

**SBSLITE**

**SBI Bus Serializer**

**Data Sheet**

**Proprietary and Confidential**

**Released**

**Issue No. 6: December 2005**

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## Revision History

Issue No.	Issue Date	Details of Change
6	December 2005	Updated ordering information including RoHS-compliant device details.
5	June 2002	Changed document status to Released.
4	May 2002	Created Issue 4 of the data sheet. General pre-production review and update. Updated SBI336 and SBI structure tables and cleaned up framing format tables. Added AMODE requirement in TelecomBus mode. Added a note pertaining to analog power filtering requirements, and corrected these requirements. Removed OPA section and replaced it with a reference to the application notes. Documented RX_INV bit in registers 0C0 and 0C8. Updated power requirements. Added latency and J1/V1 insertion sections to Operations section (section 13.12). Updated thermal information based on new simulation data.
3	February 2002	Created Issue 3 of the data sheet.
2	May 2001	Replaced all references to SBS-lite to SBSLITE for trademark purposes
1	May 2001	Created document.

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## 1 Features

- SBI converter and TDM SBI switch
- Byte wide 77.76MHz SBI336 bus to 777.6MHz serial SBI336S converter.
- DS0, NxDS0, T1, E1, TVT1.5, TVT2, DS3 and E3 granular SBI336 to serial SBI336S switch. Supports sub-rate link switching with the restriction that sub-rate links must be symmetric in both the transmit and receive directions.
- VT/TU channelized TelecomBus to TelecomBus converter and TDM switch.
- Byte wide 77.76MHz TelecomBus to serial 777.6MHz TelecomBus converter.
- VT/TU, STS/AU 77.76MHz TelecomBus to serial TelecomBus switch.
- With the Narrowband Switch Element, NSE, the SBSLITE can be used to implement a DS0 granularity SBI Memory:Space:Memory switch scaleable to 20Gb/s. In TelecomBus mode a 20Gb/s VT/TU granularity Memory:Space:Memory switch can be implemented.
- Integrates two independent DS0 granularity Memory Switches. One switch is placed between the incoming 77.76MHz byte wide SBI336 bus and the transmit working and protect Serial SBI336S link. The transmit working and protect links transmit the same data. The other switch is placed between the receive working or protect Serial SBI336S link and the outgoing 77.76MHz byte wide SBI336 bus.
- Nominal latency through the SBSLITE in DS0 mode is 125uS. Channel Associated Signaling (CAS) latency through the SBSLITE in DS0 mode is two T1 multi-frame (6mS) or two E1 multi-frame (4mS).
- In TelecomBus mode or SBI mode without DS0 level switching nominal latency through the SBSLITE is <15uS.
- The Memory Switch permits any receive or incoming byte from an input port to be mapped to any outgoing or transmit byte, respectively, on the associated output port
- Supports redundant working and protect serial SBI336S links in support of a redundant Memory:Space:Memory switch with the NSE.
- Encodes and decodes byte wide SBI336 bus control signals for all SBI supported link types and clock modes for transport over the serial SBI336S interface.
- Encodes data from the Incoming SBI336 bus or TelecomBus stream to a working and protect 777.6Mbps LVDS serial links with 8B/10B-based encoding.
- Decodes data from a working and protect 777.6MHz LVDS serial links with 8B/10B-based encoding to the Outgoing SBI336 bus or TelecomBus stream.
- In SBI mode switches Channel Associated Signaling bits, CAS, with all DS0 data.
- Uses 8B/10B-based line coding protocol on the serial links to provide transition density guarantee and DC balance and to offer a greater control character vocabulary than the standard 8B/10B protocol.



- Provides optional PRBS generation for each outgoing LVDS serial data link for off-line link verification. PRBS can be inserted with STS/AU granularity.
- Provides PRBS detection for each incoming LVDS serial link for off-line link verification. PRBS is verified with STS/AU granularity.
- Provides pins to coordinate updating of the connection map of the memory switch blocks in the local device, peer SBSLITE devices and companion NSE switch device.
- Can communicate with the NSE switch device over an in-band communications channel in the LVDS links. This channel includes mechanisms for central control and configuration.
- Derives all internal timing from a single 77.76MHz system clock.
- Implemented in 1.8V/3.3V 0.18 $\mu$ m CMOS and packaged in a 160 ball 15mmx15mm PBGA.
- Low power consumption of 0.95W (typical).

## 2 Applications

- T1/E1 SONET/SDH Cross-connects
- T1/E1 SONET/SDH Add-Drop Multiplexers
- Multi-service Access Multiplexers
- Multi-Service Switches (MSS)
- Multi-service Provisioning Platforms (MSPP)
- Serial Backplane Board Interconnect
- Shelf to Shelf Cabled Serial Interconnect
- Voice/Media Gateways

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5. Bell Communications Research - SONET Transport Systems: Common Generic Criteria, GR-253-CORE, Issue 2, Revision 2, January 1999.
6. ITU, Recommendation G.707 - "Digital Transmission Systems – Terminal equipments - General", March 1996.
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## 4 Application Examples

The voice/media gateways, softswitches and wireless voice gateways (MSC) may require a DS-0 cross-connect to groom the TDM traffic among the line cards and the voice/data processing cards. Figure 1 illustrates a typical voice/media gateway implementation. A small FPGA is required to interconnect the SBI and H-MVIP interfaces on the voice/data processing cards. The code for the FPGA (SHB) is available from PMC-Sierra under the license agreement.

**Figure 1 Voice/Media Gateway DS-0 TDM Switch Fabric Solution**

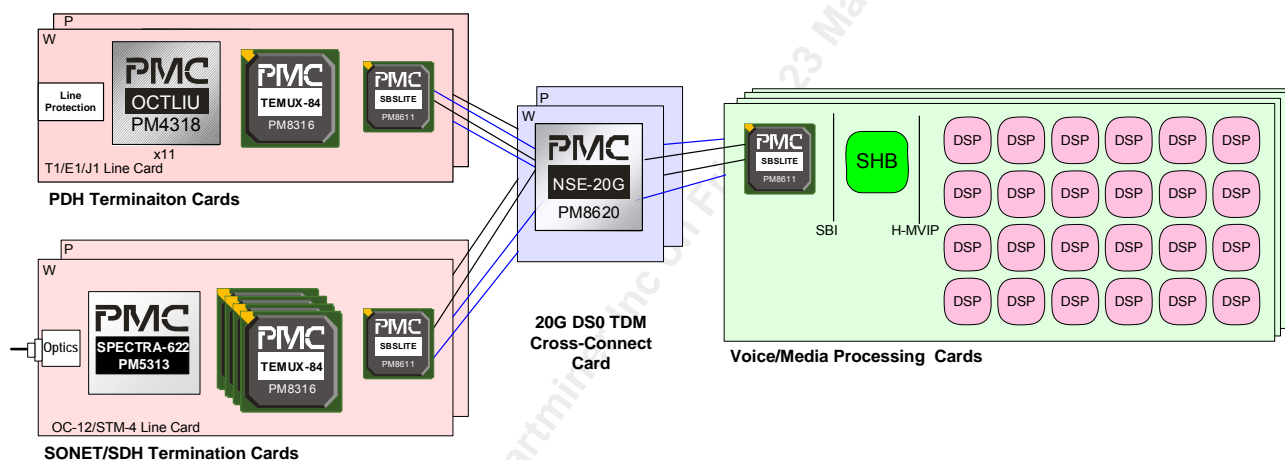
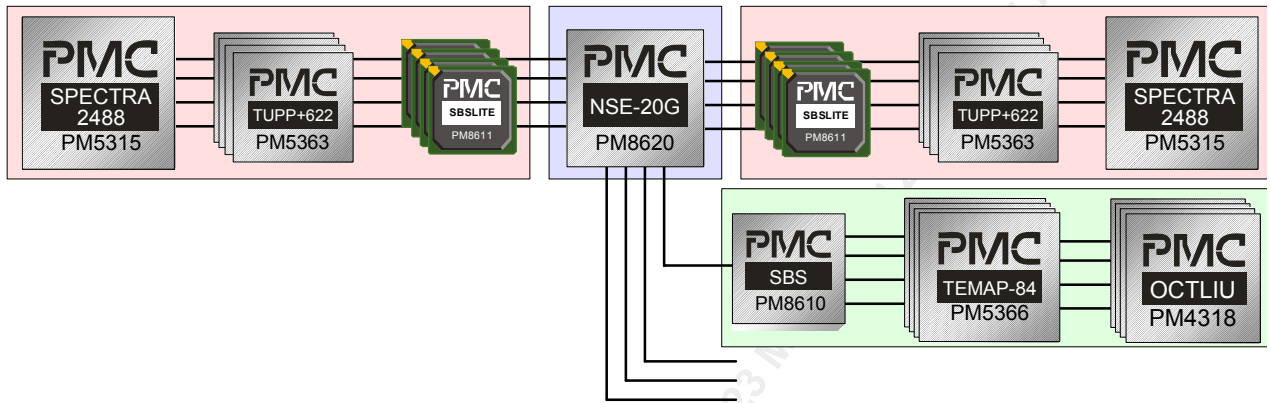


Figure 2 illustrates a possible T1/E1 add/drop multiplexer (ADM) architecture. In this example the SBSLITE and the NSE-20G operate in the TelecomBus mode. For locked STS/AUs, the SBSLITE requires all path pointer justifications to be translated into tributary pointer movements so that J1 is fixed to the location following C1 or H3. The TUPP+622 performs the J1.

**Figure 2 OC-48 T1/E1 ADM (Individually Drop/Add any T1/E1 in STS-48)**



To provide customers with a cost-effective way to groom some or all of the STS-1/AU-3 granularity traffic at the VT/TU level, equipment vendors may consider adding one-armed narrowband cross-connect cards as part of their access, metro edge, and metro core product offerings. Figure 3 illustrates a possible architecture that integrates CHES-II and CHES-NB family devices.

**Figure 3 10G VT/TU One-Armed Cross-Connect**

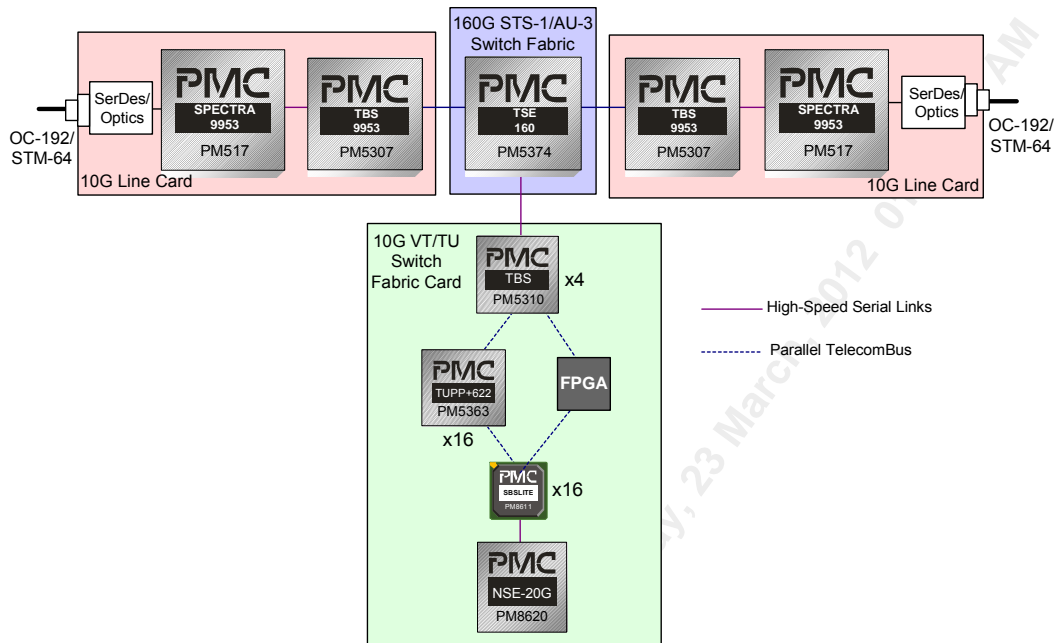
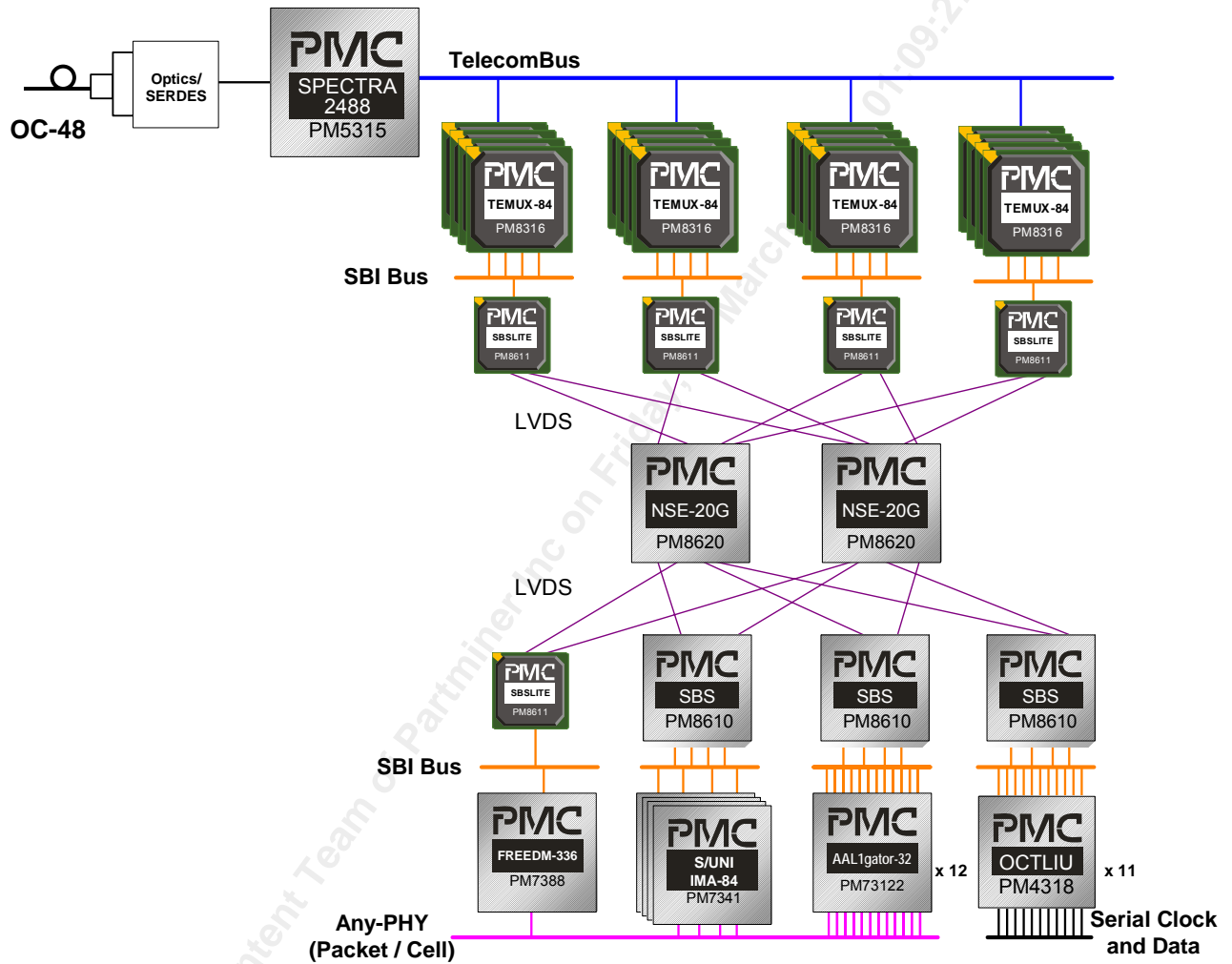


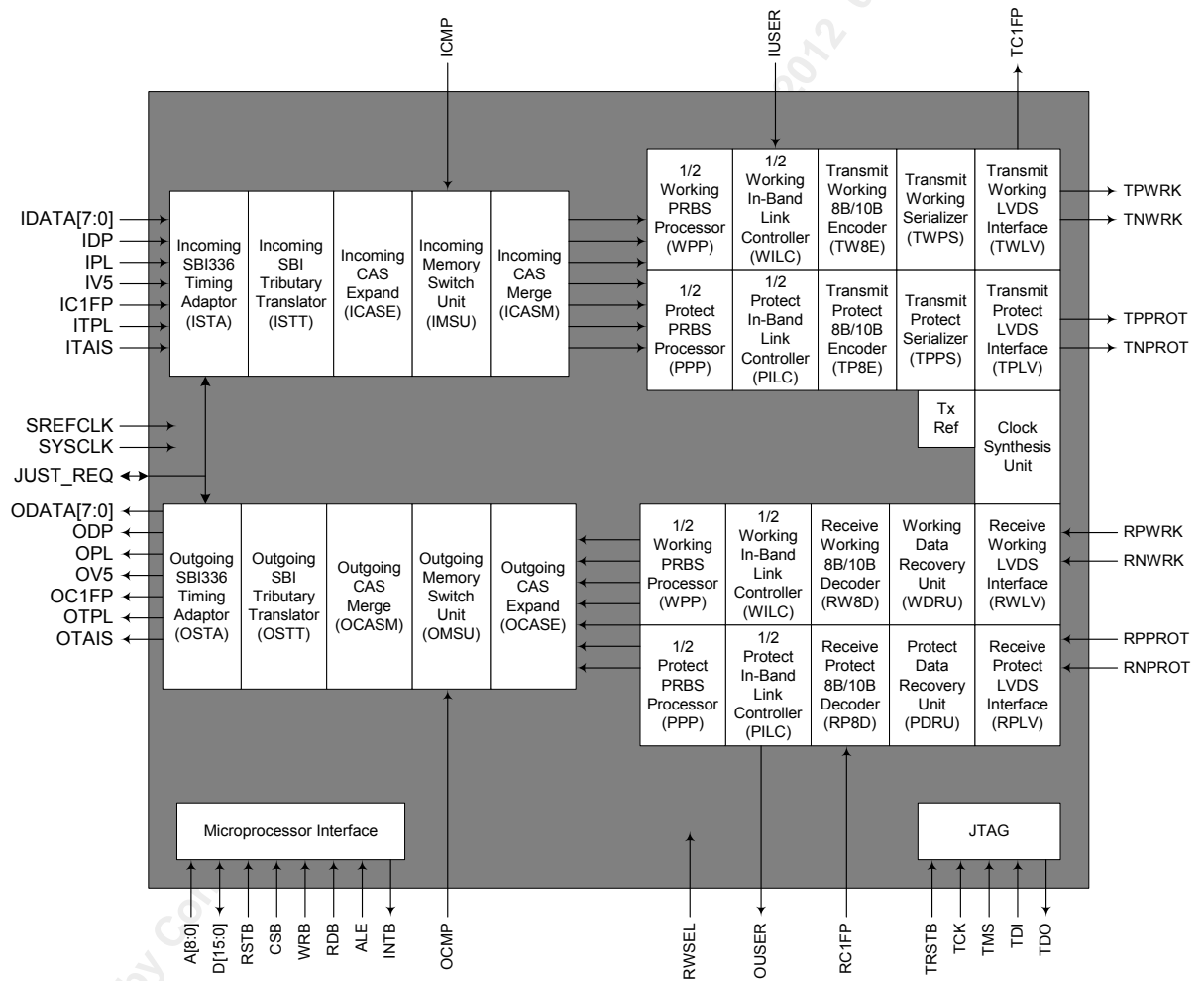
Figure 4 illustrates a DS0/NxDS0/T1/E1/VT/TU/STS-1-capable OC-48/STM-16 Any-Service-Any-Port (ASAP) architecture. The high-capacity optical streams are channelized down to the DS0 level and groomed to a variety of service cards. T1s, E1s, Transparent VTs, E3, DS3 and sub-rate rate links can be switched between the physical layer and layer 2 devices using the SBS, SBSLITE and NSE-20G devices.

**Figure 4 DS-0/NxDS0T1/E1/VT/TU/STS-1-Capable OC-48/STM-16 Any-Service-Any-Port (ASAP) Architecture**



## 5 Block Diagram

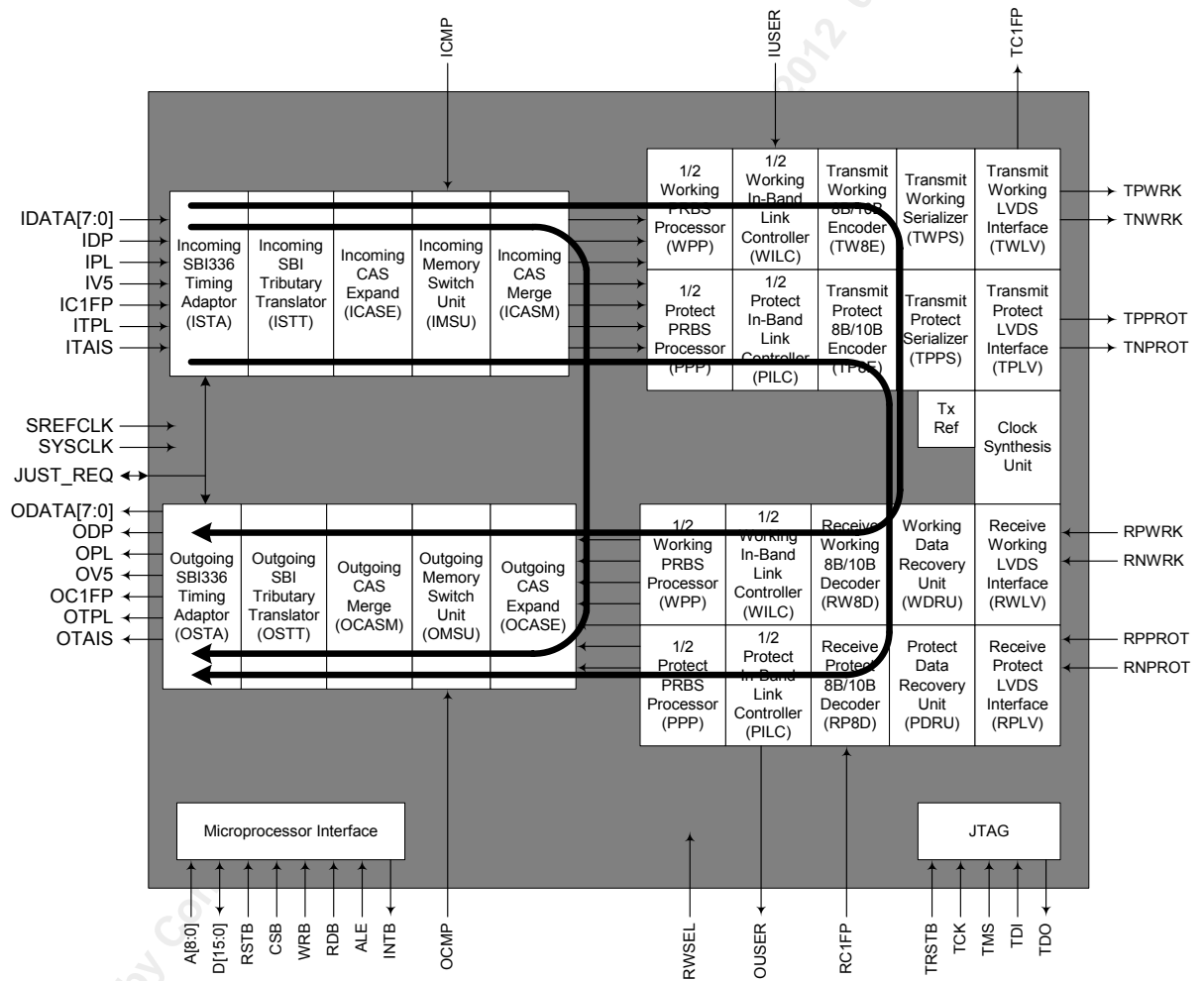
Figure 5 SBSLITE Block Diagram





## 6 Loop Back Configurations

Figure 6 Loop Back Block Diagram



## 7 Description

The PM8611 SBI336 Bus Serializer, SBSLITE, is a monolithic integrated circuit that implements conversion between a byte-serial 77.76MHz SBI336 bus and redundant 777.6Mbps bit-serial 8B/10B-base SBI336S bus. In TelecomBus mode the SBSLITE implements conversion between a 77.76MHz TelecomBus format and redundant 777.6Mbps bit-serial 8B/10B-base serial TelecomBus format. In line with the bus conversion is a DS0 granular switch allowing any input DS0 to be output on any output DS0.

The SBSLITE can be used to connect and switch high-density T1/E1 framer devices supporting an SBI bus with link layer devices supporting an SBI bus over a serial backplane. Putting the Narrowband Switch Element, NSE, between the framer and link layer devices allows construction of up to 20Gb/s NxDS0 switches.

In the ingress direction, the SBSLITE connects an incoming 77.76MHz SBI336 stream to a pair of redundant serial SBI336S LVDS links through a DS0 memory switch. In TelecomBus mode an incoming 77.76MHz TelecomBus that has the J1 path fixed and all high order pointer justifications converted to tributary pointer justifications can be switched through a VT/TU granular switch to a pair of redundant serial LVDS TelecomBus format links. The incoming data is encoded into an extended set of 8B/10B characters and transferred onto two redundant 777.6 Mbps serial LVDS links. SBI or TelecomBus frame boundaries, pointer justification events and master timing controls are marked by 8B/10B control characters. Incoming SPEs may be optionally overwritten with the locally generated  $X^{23} + X^{18} + 1$  PRBS pattern for diagnosis of downstream equipment. The PRBS processor is configurable to handle any combination of SPEs and can be inserted independently into either of the redundant LVDS links. A DS0 memory switch provides arbitrary mapping of streams on the incoming SBI336 bus stream to the working and protect LVDS links at DS0 granularity. In TelecomBus mode a VT/TU memory switch provides arbitrary mapping of tributaries on the incoming TelecomBus stream to the working and protect LVDS links. Multi-cast is supported.

In the egress direction, the SBSLITE connects two independent 777.6 Mbps serial LVDS links to an outgoing SBI336 Bus. Each link contains a constituent SBI336S stream. Bytes on the links are carried as 8B/10B characters. The SBSLITE decodes the characters into data and control signals for a single 77.76MHz SBI336 bus. Alternatively the SBSLITE decodes two independent 777.6 Mbps TelecomBus formatted serial LVDS links characters into a single 77.76MHz TelecomBus. A pseudo-random bit sequence (PRBS) processor is provided to monitor the decoded payload for the  $X^{23} + X^{18} + 1$  pattern in each SPE. The PRBS processor is configurable to handle any combination of SPEs in the serial LVDS link. Data on the outgoing SBI336 bus stream may be sourced from either of the LVDS links.

An In-band signaling link over the serial LVDS links allows this device to be controlled by a companion-switching device, the Narrowband Switching Element, NSE20G. This link can be used as communication link between a central processor and the local microprocessor.

Two loop backs are provided on the SBSLITE. The transmit 8b/10b to receive 8b/10b loop back allows data entering on the incoming bus to be looped back from the output of the TW8E and TP8E to the input of the RW8D and RP8D, respectively. Only the data looped back on the active link (working or protection) will make it back to the outgoing bus. The transmit to receive loop back allows data entering on the incoming bus to be looped back from the output of the ICASM to the input of the OCASE and then returned to the outgoing bus.

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## 8 Pin Diagram

The SBSLITE is packaged in a 160-pin PBGA package having a body size of 15mm by 15mm and a ball pitch of 1mm.

**Figure 7 Pin Diagram (Bottom View)**

	14	13	12	11	10	9	8	7	6	5	4	3	2	1			
A		DVDDO	SYSCLK	DVDDI	VSS	DVDDO	OTPL	VSS	ODATA[4]	DVDDI	ODATA[0]	DVDDO	DVDDO		A		
B	IDATA[0]	VSS	SREFCLK	VSS	ICMP	VSS	OV5	ODATA[6]	VSS	ODATA[2]	VSS	VSS	RESK	VSS	B		
C	IDATA[3]	IDATA[1]	IDATA[2]	VSS	DVDDQ	OC1FP	DVDDO	ODATA[7]	DVDDO	VSS	ODP	TC1FP	RES	AVDH[2]	C		
D	IDATA[6]	IDATA[4]	IDATA[5]	OCMP	VSS	OPL	OTAI5	ODATA[5]	ODATA[3]	ODATA[1]	AVDH[1]	VSS	TNPROT	TPPROT	D		
E	IDP	DVDDO	VSS	IDATA[7]							VSS	AVDH[0]	TPWRK	TNWRK	E		
F	IPL	IV5	IC1FP	ITPL							ATB0	ATB1	RPWRK	RNWRK	F		
G	VSS	DVDDI	INTB	ITAI5							GND	GND	AVDL	VSS	RPPROT	RNPROT	G
H	DVDDO	TCK	TDO	VSS							GND	GND	CSU_AVD L	AVDQ	VSS	CSU_AVD H	H
J	TDI	DVDDQ	TRSTB	TMS	CSU_AVD L	CSU_AVD L	VSS	VSS	J								
K	OUUSER2	NC	JUST_RE Q	VSS	VSS	VSS	DVDDI	VSS	K								
L	A[1]	DVDDI	VSS	A[0]	D[2]	D[6]	VSS	VSS	D[10]	IUSER2	D[15]	VSS	ALE	DVDDI	L		
M	A[2]	A[3]	A[6]	D[0]	D[4]	VSS	D[8]	VSS	D[11]	VSS	DVDDO	WRB	CSB	RDB	M		
N	A[4]	A[5]	VSS	A[8]	D[3]	DVDDO	D[7]	D[9]	D[13]	D[14]	RC1FP	RWSEL	DVDDO	DVDDO	N		
P		DVDDO	A[7]	D[1]	D[5]	DVDDI	DVDDQ	DVDDO	D[12]	DVDDI	VSS	RSTB	VSS		P		
	14	13	12	11	10	9	8	7	6	5	4	3	2	1			

## 9 Pin Description

Pin Name	Type	Pin No.	Function
<b>Receive Serial Data Interface (5 Signals)</b>			
RPWRK RNWRK	Analog LVDS Input	F2 F1	<p><b>Receive Working Serial Data.</b> In SBI336 mode, the differential receive working serial data link (RPWRK/RNWRK) carries the receive 77.76MHz SBI336 data from an upstream working source, in bit serial format, SBI336S.</p> <p>In TelecomBus mode, RPWRK/RNWRK carries the receive 77.76MHz TelecomBus from an upstream working source, in bit serial format.</p> <p>Data on RPWRK/RNWRK is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is transmitted first and the bit 'j' is transmitted last.</p> <p>RPWRK/RNWRK are nominally 777.6 Mbps data streams.</p> <p>If this serial link is unused, the LVDS inputs RPWRK/RNWRK may be left floating or the inputs may be grounded. In either case the analog blocks (RWLV and WDRU) can be disabled to reduce power consumption. Tying one pin high and the other pin low will apply voltage across the internal termination resistor, which will increase system power consumption.</p>
RPPROT RNPROT	Analog LVDS Input	G2 G1	<p><b>Receive Protect Serial Data.</b> In SBI336 mode, the differential receive protect serial data link (RPPROT/RNPROT) carries the receive 77.76MHz SBI336 data from an upstream protect source, in bit serial format, SBI336S.</p> <p>In TelecomBus mode, RPPROT/RNPROT carries the receive 77.76MHz TelecomBus from an upstream protection source, in bit serial format.</p> <p>Data on RPPROT/RNPROT is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is transmitted first and the bit 'j' is transmitted last.</p> <p>RPPROT/RNPROT are nominally 777.6 Mbps data streams.</p> <p>If this serial link is unused, the LVDS inputs RPPROT/RNPROT may be left floating or the inputs may be grounded. In either case the analog blocks (RWLV and WDRU) can be disabled to reduce power consumption. Tying one pin high and the other pin low will apply voltage across the internal termination resistor, which will increase system power consumption.</p>
RC1FP	Input	N4	<p><b>Receive Serial Frame Pulse.</b> The receive serial SBI336S frame pulse signal (RC1FP) provides system timing of the receive serial interface.</p> <p>When using the receive serial interface, RC1FP is set high for one SYSCLK cycle once every multi-frame (4</p>

Pin Name	Type	Pin No.	Function
			frames for SBI without CAS, 48 frames for SBI with CAS, and 4 frames for TelecomBus), or multiple thereof. The RC1FP_DLY[13:0] bits (register 007H) are used to align the C1 frame boundary 8B/10B character on the receive serial interface (RPWRK/RNWRK and RPPROT/RNPROT) with RC1FP.  RC1FP is sampled on the rising edge of SYSCCLK.
<b>Outgoing SBI Bus (68 Signals)</b>			
OC1FP	Tristate Output	C9	<b>Outgoing C1 Frame Pulse (OC1FP).</b> This signal indicates the first C1 octet on the outgoing SBI or TelecomBus.  <u>In SBI336 mode:</u>  This signal also indicates multi-frame alignment which occurs every 4 frames, therefore this signal is pulsed every fourth C1 octet to produce a 2KHz multi-frame signal.  When using the SBI bus in synchronous mode the OC1FP signal indicates T1 and E1 signaling multi-frame alignment by pulsing on 48 SBI frame boundaries. This must be done if CAS is to be switched along with the data.  <u>In TelecomBus mode:</u>  This signal may also be pulsed to indicate the J1 byte position and the byte following J1. For locked STS/AUs, the J1 byte position is locked to an offset of either 0 or 522. The byte following J1 is used to indicate multi-frame alignment and is only pulsed once every 4 frames marking the frame with the V1s.  OC1FP is updated on the rising edge of SREFCLK.
ODATA[7] ODATA[6] ODATA[5] ODATA[4] ODATA[3] ODATA[2] ODATA[1] ODATA[0]	Tristate Output	C7 B7 D7 A6 D6 B5 D5 A4	<b>Outgoing Data (ODATA[7:0]).</b> The Outgoing Data bus, ODATA[7:0], is a time division multiplexed buses which transport tributaries by assigning them to fixed octets within the SBI or TelecomBus structure.  ODATA[7:0] are updated on the rising edge of SREFCLK.
ODP	Tristate Output	C4	<b>Outgoing Bus Data Parity (ODP).</b> The outgoing data parity signal carries the even or odd parity for the outgoing bus. In SBI336 modes, the parity calculation for ODP encompasses the ODATA[7:0], OPL and OV5 signals. In TelecomBus mode, the parity calculation encompasses the ODATA[7:0] and optionally the OC1FP and OPL signals.  ODP is updated on the rising edge of SREFCLK.
OPL	Tristate Output	D9	<b>Outgoing Bus Payload (OPL).</b> The outgoing payload signal, OPL, indicates valid tributary data within the SBI bus. In TelecomBus mode, this signal indicates valid path payload.  <u>In SBI336 mode:</u>

Pin Name	Type	Pin No.	Function
			<p>This active high signal is asserted during all octets making up a tributary which includes all octets shaded gray in the framing format tables. This signal goes high during the V3 or H3 octet within a tributary to accommodate negative timing adjustments between the tributary rate and the fixed SBI bus structure. This signal goes low during the octet after the V3 or H3 octet within a tributary to accommodate positive timing adjustments between the tributary rate and the fixed SBI bus structure. For fractional rate links this signal indicates that the current octet is carrying valid data when high.</p> <p>In locked TVT mode, this signal must be driven in the same manner as for floating TVTs.</p> <p><u>In TelecomBus mode:</u></p> <p>This signal distinguishes between transport overhead bytes and synchronous payload bytes. OPL is set high to mark each payload byte on ODATA[7:0] and is set low to mark each transport overhead byte.</p> <p>OPL is updated on the rising edge of SREFCLK.</p>
OV5	Tristate Output	B8	<p><b>Outgoing Bus Payload Indicator (OV5).</b> The active high signal, OV5, locates the position of the floating payload for each tributary within the outgoing SBI336 or TelecomBuses.</p> <p><u>In SBI336 mode:</u></p> <p>This active high signal locates the position of the floating payloads for each tributary within the SBI336 structure. Timing differences between the port timing and the bus timing are indicated by adjustments of this payload indicator relative to the fixed bus structure. All movements indicated by this signal must be accompanied by appropriate adjustments in the OPL signal.</p> <p>In locked TVT mode or fractional rate link mode this signal may be driven but must be ignored by the receiving device.</p> <p><u>In TelecomBus mode:</u></p> <p>This signal identifies tributary payload frame boundaries on the outgoing data bus. OV5 is set high to mark the V5 bytes on the bus.</p> <p>OV5 is updated on the rising edge of SREFCLK.</p>

Pin Name	Type	Pin No.	Function
JUST_REQ	Bidir	K12	<p><b>Shared Bus Justification Request (JUST_REQ).</b> The SBI Bus Justification Request signal, JUST_REQ, is used to speed up, slow down or maintain the minimal rate of a slave timed SBI device.</p> <p>When the SBSLITE is configured to be connected to a physical layer device, JUST_REQ is an input aligned with the incoming bus.</p> <p>When the SBSLITE is configured to be connected to a link layer device, JUST_REQ is an output aligned with the outgoing bus.</p> <p>This active high signal, JUST_REQ, indicates negative timing adjustments on the SBI bus when asserted high during the V3 or H3 octet, depending on the tributary type. In response to this the slave timed SBI device should send an extra byte in the V3 or H3 octet of the next frame along with a valid payload signal indicating a negative justification.</p> <p>This signal indicates positive timing adjustments on the corresponding SBI bus when asserted high during the octet following the V3 or H3 octet, depending on the tributary type. The slave timed SBI device should respond to this by not sending an octet during the V3 or H3 octet of the next frame along with a valid payload signal indicating a positive justification.</p> <p>For fractional rate links this signal is asserted high during any available information byte to indicate to the slave timed SBI device that the timing master device is able to accept another byte of data. For every byte that this signal is asserted high the slave device is expected to send a valid byte of data.</p> <p>All timing adjustments from the slave timed device in response to the justification request must still set the payload and payload indicators appropriately for timing adjustments.</p> <p>JUST_REQ is not used when configured for TelecomBus mode.</p> <p>JUST_REQ is asserted or sampled on the rising edge of SREFCLK.</p>
OTPL	Tristate Output	A8	<p><b>Outgoing Tributary Payload (OTPL).</b> This signal is used to indicate tributary payload when configured for TelecomBus and is held low when configured for an SBI336 bus.</p> <p>OTPL is set high during valid VC11 and VC12 bytes of the Outgoing bus. OTPL is set low for all transport overhead bytes, high order path overhead bytes, fixed stuff column bytes and tributary transport overhead bytes (V1,V2,V3,V4).</p> <p>OTPL is updated on the rising edge of SREFCLK.</p>
OTAIS	Tristate Output	D8	<p><b>Outgoing Tributary Alarm Indication Signal (OTAIS).</b> This signal indicates tributaries in low order path AIS state for the Outgoing TelecomBus and is held low</p>



Pin Name	Type	Pin No.	Function
			<p>when configured for an SBI336 bus.</p> <p>OT AIS is set high when the tributary on the Outgoing bus is in AIS state and is set low when the tributary is out of AIS state.</p> <p>OT AIS is updated on the rising edge of SREFCLK.</p>
<b>Incoming SBI Bus (56 Signals)</b>			
IC1FP	Input	F12	<p><b>Incoming C1 Frame Pulse (IC1FP).</b> This signal pulses high for one SREFCLK cycle to indicate the first C1 octet on the incoming SBI336 or TelecomBus.</p> <p><u>In SBI336 mode:</u></p> <p>This signal also indicates multi-frame alignment which occurs every 4 frames, therefore this signal is pulsed every fourth C1 octet to produce a 2KHz multi-frame signal. The frame pulse does not need to be repeated every 2KHz as the SBSLITE will flywheel in its absence.</p> <p>When using the SBI bus in synchronous mode the IC1FP signal can be used to indicate T1 and E1 multi-frame alignment by pulsing on 48 SBI frame boundaries. This must be done if CAS is to be switched along with the data.</p> <p><u>In TelecomBus mode:</u></p> <p>This signal may also be pulsed to indicate the J1 byte position and the byte following J1. For locked STS/AUs, the J1 byte position must be locked to an offset of either 0 or 522. The byte following J1 is used to indicate multi-frame alignment and should only pulse once every 4 frames marking the frame with the V1s.</p> <p>IC1FP is sampled on the rising edge of SREFCLK.</p>
IDATA[7] IDATA[6] IDATA[5] IDATA[4] IDATA[3] IDATA[2] IDATA[1] IDATA[0]	Input	E11 D14 D12 D13 C14 C12 C13 B14	<p><b>Incoming Bus Data (IDATA[7:0]).</b> The Incoming data bus, IDATA[7:0], is a time division multiplexed buses which transports tributaries by assigning them to fixed octets within the SBI336 or TelecomBus structure.</p> <p>Multiple SBI336 devices can drive this bus at uniquely assigned tributary columns within the SBI/SBI336 bus structure.</p> <p>IDATA[7:0] is sampled on the rising edge of SREFCLK.</p>
IDP	Input	E14	<p><b>Incoming Bus Data Parity (IDP).</b> The Incoming data parity signal carries the even or odd parity for the Incoming bus. In SBI336 modes, the parity calculation encompasses the IDATA[7:0], IPL and IV5 signals. In TelecomBus mode, the parity calculation encompasses the IDATA[7:0] and optionally the IC1FP and IPL signals.</p> <p>Multiple SBI336 devices can drive this signal at uniquely assigned tributary columns within the SBI336 bus structure. This parity signal is intended to detect multiple sources in the column assignment.</p> <p>IDP is sampled on the rising edge of SREFCLK.</p>
IPL	Input	F14	<p><b>Incoming Bus Payload (IPL).</b> The Incoming Payload</p>

Pin Name	Type	Pin No.	Function
			<p>signal, IPL, indicates valid tributary data within the SBI336 bus. In TelecomBus mode, this signal indicates valid path payload.</p> <p><u>In SBI336 mode:</u></p> <p>This active high signal is asserted during all octets making up a tributary which includes all octets shaded gray in the framing format tables. This signal goes high during the V3 or H3 octet within a tributary to accommodate negative timing adjustments between the tributary rate and the fixed SBI336 structure. This signal goes low during the octet following the V3 or H3 octet within a tributary to accommodate positive timing adjustments between the tributary rate and the fixed SBI336 structure. For fractional rate links this signal indicates that the current octet is carrying valid data when high.</p> <p>Multiple SBI336 devices can drive this signal at uniquely assigned tributary columns within the SBI336 structure.</p> <p>For locked TVTs, this signal must be driven in the same manner as for floating TVTs.</p> <p><u>In TelecomBus mode:</u></p> <p>This signal distinguishes between transport overhead bytes and the synchronous payload bytes. IPL is set high to mark each payload byte on IDATA[7:0] and is set low to mark each transport overhead byte..</p> <p>IPL is sampled on the rising edge of SREFCLK.</p>
IV5	Input	F13	<p><b>Incoming Bus Payload Indicator (IV5).</b> This signal locates the position of the floating payload for each tributary of the incoming SBI336 or TelecomBuses.</p> <p><u>In SBI336 mode:</u></p> <p>This active high signal locates the position of the floating payloads for each tributary within the SBI336 structure. Timing differences between the port timing and the bus timing are indicated by adjustments of this payload indicator relative to the fixed bus structure. All movements indicated by this signal must be accompanied by appropriate adjustments in the IPL signal.</p> <p>Multiple SBI336 devices can drive this signal at uniquely assigned tributary columns within the SBI336 structure.</p> <p>For locked TVTs, this signal must either be driven in the same manner as for floating TVTs or held low.</p> <p><u>In TelecomBus mode:</u></p> <p>This signal identifies tributary payload frame boundaries on the incoming data bus. IV5 is set high to mark the V5 bytes on the bus.</p> <p>IV5 is sampled on the rising edge of SREFCLK.</p>
ITPL	Input	F11	<p><b>Incoming Tributary Payload (ITPL).</b> This signal is</p>

Pin Name	Type	Pin No.	Function
			<p>used to indicate tributary payload when configured for TelecomBus and is unused when configured for an SBI336 bus.</p> <p>ITPL is set high during valid VC11 and VC12 bytes of the Incoming bus. ITPL is set low for all transport overhead bytes, high order path overhead bytes, fixed stuff column bytes and tributary transport overhead bytes (V1,V2,V3,V4).</p> <p>ITPL is sampled on the rising edge of SREFCLK.</p>
ITAIS	Input	G11	<p><b>Incoming Tributary Alarm Indication Signal (ITAIS).</b> This signal indicates tributaries in low order path AIS state for the Incoming TelecomBus and is unused when configured for an SBI336 bus.</p> <p>ITAIS is set high when the tributary on the Incoming bus is in AIS state and is set low when the tributary is out of AIS state.</p> <p>ITAIS is sampled on the rising edge of SREFCLK.</p>
<b>Transmit Serial Data Interface (5 Signals)</b>			
TPWRK TNWRK	Analog LVDS Output	E2 E1	<p><b>Transmit Working Serial Data.</b> In SBI336 mode, the differential transmit working serial data link (TPWRK/TNWRK) carries a transmit 77.76Mhz SBI336 data stream to a downstream working sink, in bit serial format, SBI336S.</p> <p>In TelecomBus mode, TPWRK/TNWRK carries the transmit 77.76MHz TelecomBus data stream to a downstream working sink, in bit serial format.</p> <p>Data on TPWRK/TNWRK is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is transmitted first and the bit 'j' is transmitted last.</p> <p>TPWRK/TNWRK are nominally 777.6 Mbps data streams.</p>
TPPROT TNPROT	Analog LVDS Output	D1 D2	<p><b>Transmit Protect Serial Data.</b> In SBI336 mode, the differential transmit protect serial data link (TPPROT/TNPROT) carries a transmit 77.76Mhz SBI336 data stream to a downstream protect sink, in bit serial format, SBI336S.</p> <p>In TelecomBus mode, TPPROT/TNPROT carries the transmit 77.76MHz TelecomBus data stream to a downstream protection sink, in bit serial format.</p> <p>Data on TPPROT/TNPROT is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is transmitted first and the bit 'j' is transmitted last.</p> <p>TPPROT/TNPROT are nominally 777.6 Mbps data streams.</p>
TC1FP	Output	C3	<p><b>Transmit Serial SBI Frame Pulse.</b> The transmit serial SBI frame pulse signal (TC1FP) provides system timing of the transmit serial interface.</p> <p>TC1FP is set high to indicate that the C1 frame</p>

Pin Name	Type	Pin No.	Function
			boundary 8B/10B character has been serialized out on the transmit working serial data link (TPWRK/TNWRK) and the transmit protection serial data link (TPPROT/TNPROT). TC1FP is output every 4 frame for SBI mode without CAS and for TelecomBus mode. TC1FP is output every 48 frames for SBI mode with CAS. TC1FP is updated on the rising edge of SYSCLK.
<b>Microprocessor Interface (30 Signals)</b>			
CSB	Input	M2	<b>Chip Select Bar.</b> The active low chip select signal (CSB) controls microprocessor access to registers in the SBSLITE device. CSB is set low during SBSLITE Microprocessor Interface Port register accesses. CSB is set high to disable microprocessor accesses.  If CSB is not required (i.e. register accesses controlled using RDB and WRB signals only), CSB should be connected to an inverted version of the RSTB input.
RDB	Input	M1	<b>Read Enable Bar.</b> The active low read enable bar signal (RDB) controls microprocessor read accesses to registers in the SBSLITE device. RDB is set low and CSB is also set low during SBSLITE Microprocessor Interface Port register read accesses. The SBSLITE drives the D[15:0] bus with the contents of the addressed register while RDB and CSB are low.
WRB	Input	M3	<b>Write Enable Bar.</b> The active low write enable bar signal (WRB) controls microprocessor write accesses to registers in the SBSLITE device. WRB is set low and CSB is also set low during SBSLITE Microprocessor Interface Port register write accesses. The contents of D[15:0] are clocked into the addressed register on the rising edge of WRB while CSB is low.
D[15] D[14] D[13] D[12] D[11] D[10] D[9] D[8] D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O	L4 N5 N6 P6 M6 L6 N7 M8 N8 L9 P10 M10 N10 L10 P11 M11	<b>Microprocessor Data Bus.</b> The bi-directional data bus, D[15:0] is used during SBSLITE Microprocessor Interface Port register reads and write accesses. D[15] is the most significant bit of the data words and D[0] is the least significant bit.
A[8]/TRS A[7] A[6] A[5] A[4] A[3] A[2]	Input	N11 P12 M12 N13 N14 M13 M14	<b>Microprocessor Address Bus.</b> The microprocessor address bus (A[8:0]) selects specific Microprocessor Interface Port registers during SBSLITE register accesses.  A[8] is also the Test Register Select (TRS) address pin and selects between normal and test mode register

Pin Name	Type	Pin No.	Function
A[1] A[0]		L14 L11	accesses. TRS is set high during test mode register accesses, and is set low during normal mode register accesses.
ALE	Input	L2	<b>Address Latch Enable.</b> The address latch enable signal (ALE) is active high and latches the address bus (A[11:0]) when it is set low. The internal address latches are transparent when ALE is set high. ALE allows the SBSLITE to interface to a multiplexed address/data bus. ALE has an integral pull up resistor.
INTB	Open Drain Output	G12	<b>Interrupt Request Bar.</b> The active low interrupt enable signal (INTB) output goes low when an SBSLITE interrupt source is active and that source is unmasked. INTB returns high when the interrupt is acknowledged via an appropriate register access. INTB is an open drain output.
<b>General Function (9 Signals)</b>			
SYSCLK	Input	A12	<b>SBI System Clock.</b> The 77MHz SBI reference clock signal, SYSCLK, is the master clock for the SBSLITE device. SYSCLK is a 77.76 MHz clock, with a nominal 50% duty cycle. RC1FP, OCMP and RWSEL are sampled on the rising edge of SYSCLK. TC1FP is updated on the rising edge of SYSCLK.
SREFCLK	Input	B12	<b>SBI Reference Clock.</b> The SBI reference clock, SREFCLK, is a reference for the incoming and outgoing SBI bus and TelecomBus interfaces. SREFCLK is a 77.76MHz clock with a nominal 50% duty cycle. IC1FP, IDATA[7:0], IDP, IPL, IV5, ITPL, ITAIS, JUST_REQ and ICMP are sampled on the rising edge of SREFCLK. OC1FP, ODATA[7:0], ODP, OPL, OV5, OTPL, OTAIS and JUST_REQ are updated on the rising edge of SREFCLK.  This signal should be tied to SYSCLK.
ICMP	Input	B10	<b>Incoming Connection Memory Page.</b> The incoming connection memory page select signal, ICMP, controls the selection of the connection memory page in the Incoming Memory Switch Unit, IMSU. When ICMP is set high, connection memory page 1 is selected. When ICMP is set low, connection memory page 0 is selected.  The byte location during which ICMP is sampled is dependant on the mode of operation. <u>4-Frame SBI336 mode:</u>  ICMP is sampled at the C1 byte position of the incoming bus on the first frame of the 4-frame multi-frame (marked by IC1FP). Changes to the connection memory page selection is synchronized to the frame boundary of the next four-frame multi-frame. <u>48-Frame SBI336 mode:</u>  ICMP is sampled at the C1 byte position of the incoming bus on the first frame of the 48-frame multi-frame (marked by IC1FP). Changes to the connection memory page selection is synchronized to the frame

Pin Name	Type	Pin No.	Function
			<p>boundary of the next 48-frame multi-frame.</p> <p><u>TelecomBus mode:</u></p> <p>ICMP is sampled at the C1 byte position of every frame on the incoming bus (marked by IC1FP). Changes to the connection memory page selection are synchronized to the frame boundary of the next frame.</p> <p>ICMP is sampled on the rising edge of SREFCLK.</p>
OCMP	Input	D11	<p><b>Outgoing Connection Memory Page.</b> The outgoing connection memory page select signal, OCMP, controls the selection of the connection memory page in the Outgoing Memory Switch Unit, OMSU. When OCMP is set high, connection memory page 1 is selected. When OCMP is set low, connection memory page 0 is selected.</p> <p>The byte location during which OCMP is sampled is dependant on the mode of operation.</p> <p><u>4-Frame SBI336 mode:</u></p> <p>OCMP is sampled at the C1 byte position of the receive bus on the first frame of the 4-frame multi-frame (marked by RC1FP). Changes to the connection memory page selection is synchronized to the frame boundary of the next four-frame multi-frame.</p> <p><u>48-Frame SBI336 mode:</u></p> <p>OCMP is sampled at the C1 byte position of the receive bus on the first frame of the 48-frame multi-frame (marked by RC1FP). Changes to the connection memory page selection is synchronized to the frame boundary of the next 48-frame multi-frame.</p> <p><u>TelecomBus mode:</u></p> <p>OCMP is sampled at the C1 byte position of every frame on the receive bus (marked by RC1FP). Changes to the connection memory page selection are synchronized to the frame boundary of the next frame.</p> <p>OCMP is sampled on the rising edge of SYSCLK.</p>
RWSEL	Input	N3	<p><b>Receive Working Serial Data Select.</b> The receive working serial data select signal, RWSEL, selects between sourcing outgoing data, ODATA[7:0], from the receive working serial data link, RPWRK/RNWRK, or the receive protect serial data link, RPPROT/RNPROT. When RWSEL is set high, the working serial bus is selected. When RWSEL is set low, the protect serial bus is selected. RWSEL is sampled at the C1 byte location as defined by the receive serial interface frame pulse signal, RC1FP. Changes to the selection of the working and protect serial streams are synchronized to the SBI frame boundary of the next frame.</p> <p>RWSEL is sampled on the rising edge of SYSCLK.</p>
IUSER2	Input	L5	<p><b>Input In-band Link User Signal.</b> The input in-band link user signal, IUSER2, provides external control over one of the bits in the in-band link. The USER[2] bit in the</p>

Pin Name	Type	Pin No.	Function
			header of the in-band signaling channel of both the working and protection serial links will reflect the state of this input.  IUSER2 an asynchronous signal and is internally synchronized to SYSCLK.
OUSER2	Output	K14	<b>Output In-Band Link User Signal.</b> The output in-band link user signal, OUSER2, reflects the state of the USER[2] bit in the header of the in-band signaling channel of either the working or the protection serial link, whichever is active.  OUSER2 is an asynchronous output.
RSTB	Input	P3	<b>Reset Enable Bar.</b> The active low reset signal, RSTB, provides an asynchronous SBSLITE reset. RSTB is a Schmitt triggered input with an integral pull-up resistor.  When performing a reset of the SBSLITE, this pin should be held low for a minimum of 1ms to properly reset the CSU. Alternatively, the ARESET bit in register 000H must be set for a minimum of 1ms after the SBSLITE is reset by RSTB.
<b>JTAG Interface (5 Signals)</b>			
TCK	Input	H13	<b>Test Clock.</b> The JTAG test clock signal, TCK, provides timing for test operations that are carried out using the IEEE P1149.1 test access port.
TMS	Input	J11	<b>Test Mode Select.</b> The JTAG test mode select signal, TMS, controls the test operations that are carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull-up resistor.
TDI	Input	J14	<b>Test Data Input.</b> The JTAG test data input signal, TDI, carries test data into the SBSLITE via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull-up resistor.
TDO	Tristate	H12	<b>Test Data Output.</b> The JTAG test data output signal, TDO, carries test data out of the SBSLITE via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output which is inactive except when scanning of data is in progress.
TRSTB	Input	J12	<b>Test Reset Bar.</b> The active low JTAG test reset signal, TRSTB, provides an asynchronous SBSLITE test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an integral pull-up resistor.  Note that when TRSTB is not being used, it must be connected to the RSTB input.
<b>Analog Reference Resistors (2 Signals)</b>			
RES	Analog Input	C2	<b>Reference Resistor Connection (RES).</b> An off-chip 3.16kΩ ±1% resistor is connected between this positive resistor reference pin, RES, and a Kelvin ground pin, RESK. An on-chip negative feedback path will force the 0.8V VREF voltage onto RES, therefore forcing 252uA

Pin Name	Type	Pin No.	Function
			of current to flow through the resistor.
RESK	Analog Input	B2	<b>Reference Resistor Connection (RESK).</b> An off-chip 3.16kΩ ±1% resistor is connected between the positive resistor reference pin, RES, and this Kelvin ground pin, RESK. An on-chip negative feedback path will force the 0.8V VREF voltage onto RESK, therefore forcing 252uA of current to flow through the resistor.
<b>Analog Test Bus (2 Signals)</b>			
ATB0	Analog	F4	<b>Analog test pin (ATB0).</b> This pin is used for PMC validation and testing. This pin must be grounded.
ATB1	Analog	F3	<b>Analog test pin (ATB1).</b> This pin is used for PMC validation and testing. This pin must be grounded.
<b>Analog High Voltage Power (5 Signals)</b>			
CSU_AVDH	Power	H1	<b>CSU Analog Power (CSU_AVDH).</b> This pin should be connected to a well-decoupled +3.3V ± 5% DC supply.
AVDH[2] AVDH[1] AVDH[0]	Power	C1 D4 E3	<b>Analog Power (AVDH[2:0]).</b> These pins should be connected to a well-decoupled +3.3V ± 5% DC supply.
AVDQ	Power	H3	<b>Analog Quiet Power (AVDQ).</b> This pin should be connected to a well decoupled +3.3V ± 5% DC supply.
<b>Analog Low Voltage Power (4 Signals)</b>			
CSU_AVDL[2] CSU_AVDL[1] CSU_AVDL[0]	Power	H4 J3 J4	<b>CSU Analog Power (CSU_AVDL[2:0]).</b> These pins should be connected to a well-decoupled +1.8V ± 5% DC supply. Each CSU_AVDL pin requires individual filtering.
AVDL	Power	G4	<b>Analog Power (AVDL[2:0]).</b> This pin should be connected to a well-decoupled +1.8V ± 5% DC supply.
<b>Digital Core Power (8 Signals)</b>			
DVDDI[7] DVDDI[6] DVDDI[5] DVDDI[4] DVDDI[3] DVDDI[2] DVDDI[1] DVDDI[0]	Power	K2 L1 P5 P9 L13 G13 A11 A5	<b>Digital Core Power (DVDDI[7:0]).</b> The digital core power pins should be connected to a well-decoupled +1.8V ± 5% DC supply.
<b>Digital I/O Power (14 Signals)</b>			
DVDDO[13] DVDDO[12] DVDDO[11] DVDDO[10] DVDDO[9] DVDDO[8] DVDDO[7] DVDDO[6] DVDDO[5] DVDDO[4] DVDDO[3] DVDDO[2]	Power	N1 N2 M4 P7 N9 P13 H14 E13 A13 A9 C8 C6	<b>Digital I/O Power (DVDDO[13:0]).</b> The digital I/O power pins should be connected to a well-decoupled +3.3V ± 5% DC supply.



Pin Name	Type	Pin No.	Function
DVDDO[1] DVDDO[0]		A3 A2	
<b>Digital I/O Quiet Power (3 Signals)</b>			
DVDDQ[2:0]	Power	P8 J13 C10	<b>Digital I/O Quiet Power (DVDDQ[2:0]).</b> The digital I/O quiet power pins should be connected to a well-decoupled +3.3V ± 5% DC supply.
<b>Ground (35 Signals)</b>			
VSS[34] VSS[33] VSS[32] VSS[31] VSS[30] VSS[29] VSS[28] VSS[27] VSS[26] VSS[25] VSS[24] VSS[23] VSS[22] VSS[21] VSS[20] VSS[19] VSS[18] VSS[17] VSS[16] VSS[15] VSS[14] VSS[13] VSS[12] VSS[11] VSS[10] VSS[9] VSS[8] VSS[7] VSS[6] VSS[5] VSS[4] VSS[3] VSS[2] VSS[1] VSS[0]	Ground	B1 D3 E4 G3 H2 J1 J2 K1 K3 K4 L3 P2 P4 M5 L7 M7 L8 M9 N12 L12 K11 H11 G14 E12 B13 B11 C11 A10 D10 B9 A7 B6 C5 B4 B3	<b>Ground (VSS[34:0]).</b> The ground pins, VSS[34:0], should be connected to GND.
GND	Thermal Vias	G7 G8 H7 H8	The Thermal Vias (GND) pins are used to improve thermal conductance of the device package. They should be connected to the PCB ground plane. The GND pins are not electrically connected to the other ground pins of the package.
NC	No Connect	K13	The No Connect pin must be left floating.

**Notes on Pin Description:**

- All SBSLITE inputs and bi-directionals except the LVDS links present minimum capacitive loading and operate at TTL (V<sub>dd</sub> reference) logic levels.
- Inputs RSTB, ALE, TMS, TDI and TRSTB have internal pull-up resistors.

3. All SBSLITE outputs have 20mA drive capability except for JUST\_REQ, D[15:0], TDO and INTB which have 12mA drive capability.
4. The DVDDI, CSU\_AVDL and AVDL power pins are not internally connected to each other. Failure to connect these pins externally may cause malfunction or damage to the SBSLITE.
5. The AVDH, AVDQ, CSU\_AVDH, DVDDO and DVDDQ power pins are not internally connected to each other. Failure to connect these pins externally may cause malfunction or damage to the SBSLITE.
6. The DVDDI, DVDDO, DVDDQ, AVDH, AVDQ, CSU\_AVDH, CSU\_AVDL and AVDL power pins all share a common ground.
7. See section 16.2 for information on power sequencing.
8. See section 16.3 for information on analog power filtering recommendations.

## 10 Functional Description

### 10.1 SBI Bus Data Formats

While the SBSLITE does not interface to the 19.44MHz SBI bus, this bus is described below for illustrative purposes. The SBSLITE does interface to a 77.76MHz SBI336 bus which is equivalent to four byte interleaved 19.44MHz SBI buses.

#### 10.1.1 SBI Multiplexing Structure

The SBI structure uses a locked SONET/SDH structure fixing the position of the TU-3 relative to the STS-3/STM-1. The SBI is also of fixed frequency and alignment as determined by the reference clock and frame indicator signal (IC1FP). Frequency deviations are compensated by adjusting the location of the T1/E1/DS3/E3/TVT1.5/TVT2 channels using floating tributaries as determined by the V5 indicator and payload signals (IV5[x] and IPL[x]). TVTs also allow for synchronous operation where SONET/SDH tributary pointers are carried within the SBI structure in place of the V5 indicator and payload signals (IV5[x] and IPL[x]). Fractional links use as many bytes as required within a given synchronous payload envelope (SPE) using the payload signals to indicate bytes carrying valid data.

Table 1 shows the bus structure for carrying T1, E1, TVT1.5, TVT2, DS3, E3 and Fractional tributaries in a SDH STM-1 like format. Up to 84 T1s, 63 E1s, 84 TVT1.5s, 63 TVT2s, 3 DS3s, 3 E3s or 3 Fractional rate links are carried within the octets labeled SPE1, SPE2 and SPE3 in columns 16-270. All other octets are unused and are of fixed position. The frame signal (IC1FP) occurs during the octet labeled C1 in Row 1 column 7.

The multiplexed links are separated into three Synchronous Payload Envelopes called SPE1, SPE2 and SPE3. Each envelope carries up to 28 T1s, 21 E1, 28 TVT1.5s, 21 TVT2s, a DS3, an E3 or a Fractional link. SPE1 carries the T1s numbered 1,1 through 1,28, E1s numbered 1,1 through 1,21, DS3 number 1,1, E3 number 1,1 or Fractional link 1,1. SPE2 carries T1s numbered 2,1 through 2,28, E1s numbered 2,1 through 2,21, DS3 number 2,1, E3 number 2,1 or Fractional link 2,1. SPE3 carries T1s numbered 3,1 through 3,28, E1s numbered 3,1 through 3,21, DS3 number 3,1, E3 number 3,1 or Fractional link 3,1. TVT1.5s are numbered the same as T1 tributaries and TVT2s are numbered the same as E1 tributaries.

**Table 1 Structure for Carrying Multiplexed Links**

		SBI Column														
		1	6	7	8	15	16	17	18	19	268	269	270			
Row	1	-	...	-	C1	-	...	-	SPE1	SPE2	SPE3	SPE1	...	SPE1	SPE2	SPE3
	2	-	...	-	-	-	...	-	SPE1	SPE2	SPE3	SPE1	...	SPE1	SPE2	SPE3
	9	-	-	-	-	-	SPE1	SPE2	SPE3	SPE1				SPE1	SPE2	SPE3
		1	2	3	3	5	6	6	6	7	90	90	90			
														SPE Column		

The mappings for each link type are rigidly defined, however the mix of links transported across the bus at any one time is flexible. Each synchronous payload envelope, comprising 85 columns numbered 6 through 90, operates independently allowing a mix of T1s, E1s, TVT1.5s, TVT2s, DS3s, E3s or Fractional links. For example, SPE1 could transport a single DS3, SPE2 could transport a single E3 and SPE3 could transport either 28 T1s or 21 E1s. Each SPE is restricted to carrying a single tributary type. SBI columns 16-18 are unused for T1, E1, TVT1.5 and TVT2 tributaries.

**Tributary Numbering**

Tributary numbering for T1 and E1 uses the SPE number, followed by the Tributary number within that SPE and are numbered sequentially. Table 2 and Table 3 show the T1 and E1 column numbering and relates the tributary number to the SPE column numbers and overall SBI column structure. Numbering for DS3 or E3 follows the same naming convention even though there is only one DS3 or E3 per SPE. TVT1.5s and TVT2s follow the same numbering conventions as T1 and E1 tributaries respectively. SBI columns 16-18 are unused for T1, E1, TVT1.5 and TVT2 tributaries.

**Table 2 T1/TVT1.5 Tributary Column Numbering**

T1#	SPE1 Column	SPE2 Column	SPE3 Column	SBI Column
1,1	7,35,63			19,103,187
2,1		7,35,63		20,104,188
3,1			7,35,63	21,105,189
1,2	8,36,64			22,106,190
2,2		8,36,64		23,107,191
...				
1,28	34,62,90			100,184,268
2,28		34,62,90		101,185,269
3,28			34,62,90	102,186,270

**Table 3 E1/TVT2 Tributary Column Numbering**

E1#	SPE1 Column	SPE2 Column	SPE3 Column	SBI Column
1,1	7,28,49,70			19,82,145,208
2,1		7,28,49,70		20,83,146,209
3,1			7,28,49,70	21,84,147,210
1,2	8,29,50,71			22,85,148,211
2,2		8,29,50,71		23,86,149,212
•••				
1,21	27,48,69,90			79,142,205,268
2,21		27,48,69,90		80,143,206,269
3,21			27,48,69,90	81,144,207,270

### 10.1.2 SBI Timing Master Modes

The Scaleable Bandwidth Interconnect is a synchronous bus which is timed to a reference 19.44MHz clock and a 2KHz frame pulse (8KHz is easily derived from the 2KHz and 19.44MHz clock). All sources and sinks of data on this bus are timed to the reference clock and frame pulse.

The data format on the data bus allows for compensating between clock differences on the PHY, SBI and Link Layer devices. This is achieved by floating data structures within the SBI format.

Timing is communicated across the SBI bus by floating data structures within the bus. Payload indicator signals in the SBI control the position of the floating data structure and therefore the timing. When sources are running faster than the SBI the floating payload structure is advanced by an octet by passing an extra octet in the V3 octet locations (H3 octet for DS3 and E3 mappings). When the source is slower than the SBI the floating payload is retarded by leaving the octet after the V3 or H3 octet unused. Both these rate adjustments are indicated by the SBI control signals.

On the DROP BUS all timing is sourced from the PHY and is passed onto the Link Layer device by the arrival rate of data over the SBI.

On the ADD BUS timing can be controlled by either the PHY or the Link Layer device by controlling the payload and by making justification requests. When the Link Layer device is the timing master the PHY device gets its transmit timing information from the arrival rate of data across the SBI. When the PHY device is the timing master it signals the Link Layer device to speed up or slow down with justification request signals. The PHY timing master indicates a speedup request to the Link Layer by asserting the justification request signal high during the V3 or H3 octet. When this is detected by the Link Layer it will advance the channel by inserting data in the next V3 or H3 octet as described above. The PHY timing master indicates a slowdown request to the Link Layer by asserting the justification request signal high during the octet after the V3 or H3 octet. When detected by the Link Layer it will retard the channel by leaving the octet following the next V3 or H3 octet unused. Both advance and retard rate adjustments take place in the frame or multi-frame following the justification request.

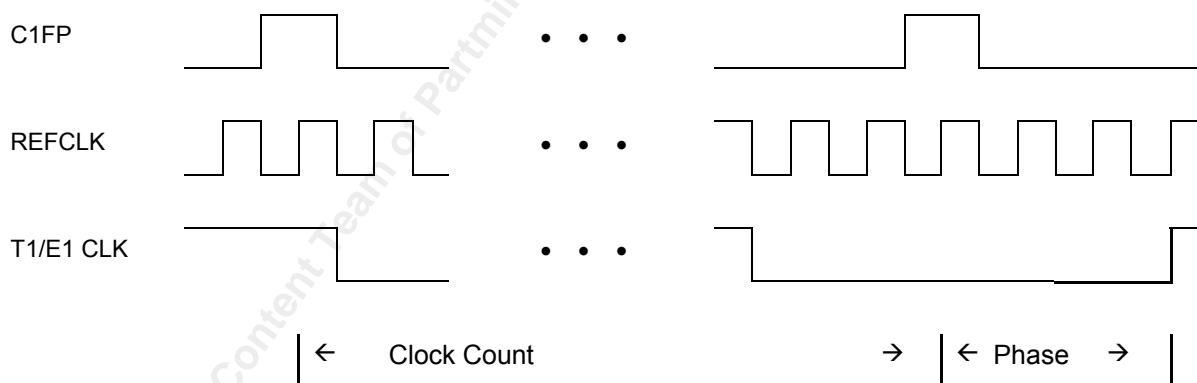
The SBI bus supports a synchronous SBI mode for T1 and E1 links. In this mode the DS0s or timeslots within the T1 or E1 tributaries are fixed to the locations shown in the T1 and E1 mappings. Effectively synchronous mode locks the V5 in the octet following the V1 octet and does not allow the tributaries to float relative to the reference clock.

### 10.1.3 SBI Link Rate Information

The SBI bus provides a method for carrying link rate information. This is optional on a per channel basis. Two methods are specified, one for T1 and E1 channels and the second for DS3 and E3 channels. Link rate information is not available for TVTs. These methods use the reference 19.44MHz SBI clock and the IC1FP frame synchronization signal to measure channel clock ticks and clock phase for transport across the bus.

The T1 and E1 method allows for a count of the number of T1 or E1 rising clock edges between two IC1FP frame pulses. This count is encoded in ClkRate[1:0] to indicate that the nominal number of clocks, one more than nominal or one less than nominal should be generated during the IC1FP period. This method also counts the number of 19.44MHz clock rising edges after sampling IC1FP high to the next rising edge of the T1 or E1 clock, giving the ability to control the phase of the generated clock. The link rate information passed across the SBI bus via the V4 octet and is shown in Table 4. Table 5 shows the encoding of the clock count, ClkRate[1:0], passed in the link rate octet.

**Table 4 T1/E1 Link Rate Information**



Link Rate Octet	Bit #	7	6	5:4	3:0
T1/E1 Format		ALM	0	ClkRate[1:0]	Phase[3:0]

**Table 5 T1/E1 Clock Rate Encoding**

ClkRate[1:0]	T1 Clocks / 2KHz	E1 Clocks / 2 KHz
"00" – Nominal	772	1024
"01" – Fast	773	1025
"1x" – Slow	771	1023

The DS3 and E3 method for transferring link rate information across the SBI passes the encoded count of DS3/E3 clocks between C1FP pulses in the same method used for T1/E1 tributaries, but does not pass any phase information. The other difference from T1/E1 link rate is that ClkRate[1:0] indicates whether the nominal number of clocks are generated or if four fewer or four extra clocks are generated during the C1FP period. The format of the DS3/E3 link rate octet is shown in Table 6. This is passed across the SBI via the Linkrate octet which follows the H3 octet in the column, see Table 12 and Table 15. Table 7 shows the encoding of the clock count, ClkRate[1:0], passed in the link rate octet.

**Table 6 DS3/E3 Link Rate Information**

Link Rate Octet	Bit #	7	6	5:4	3:0
DS3/E3 Format		ALM	0	ClkRate[1:0]	Unused

**Table 7 DS3/E3 Clock Rate Encoding**

ClkRate[1:0]	DS3 Clocks / 2KHz	E3 Clocks / 2 KHz
"00" – Nominal	22368	17184
"01" – Fast	22372	17188
"1x" – Slow	22364	17180

#### 10.1.4 Alarms

This specification provides a method for transferring alarm conditions across the SBI bus. This is optional on a per tributary basis and is valid for T1, E1, DS3, and E3 tributaries but not valid for transparent VTs nor Fractional links.

Table 4 and Table 6 show the alarm indication bit, ALM, as bit 7 of the Link Rate Octet. Devices which do not support alarm indications should set this bit to 0. When not enabled the value of this bit must be ignored by the receiving device.

The presence of an alarm condition is indicated by the ALM bit set high in the Link Rate Octet. The absence of an alarm condition is indicated by the ALM bit set low in the Link Rate Octet. The ALM bit is transparent to the SBS.

### 10.1.5 T1 Tributary Mapping

Table 8 shows the format for mapping 84 T1s within the SPE octets. The DS0s and framing bits within each T1 are easily located within this mapping for channelized T1 applications. It is acceptable for the framing bit to not carry a valid framing bit on the Add Bus since the physical layer device will provide this information. Unframed T1s use the exact same format for mapping 84 T1s into the SBI except that the T1 tributaries need not align with the frame bit and DS0 locations. The V1,V2 and V4 octets are not used to carry T1 data and are either reserved or used for control across the interface. When enabled, the V4 octet is the Link Rate octet of Tables 1 and 3. It carries alarm and clock phase information across the SBI bus. The V1 and V2 octets are unused and should be ignored by devices listening to the SBI bus. The V5 and R octets do not carry any information and are fixed to a zero value. The V3 octet carries a T1 data octet but only during rate adjustments as indicated by the V5 indicator signals, IV5 and OV5, and payload signals, IPL and OPL. The PPSSSSFR octets carry channel associated signaling (CAS) bits and the T1 framing overhead. The DS0 octets are the 24 DS0 channels making up the T1 link.

The V1,V2,V3 and V4 octets are fixed to the locations shown. All the other octets, shown shaded for T1#1,1, float within the allocated columns maintaining the same order and moving a maximum of one octet per 2KHz multi-frame. The position of the floating T1 is identified via the V5 Indicator signals, IV5 and OV5, which locate the V5 octet. When the T1 tributary rate is faster than the SBI nominal T1 tributary rate, the T1 tributary is shifted ahead by one octet which is compensated by sending an extra octet in the V3 location. When the T1 tributary rate is slower than the nominal SBI tributary rate the T1 tributary is shifted by one octet which is compensated by inserting a stuff octet in the octet immediately following the V3 octet and delaying the octet that was originally in that position.

**Table 8 T1 Framing Format**

ROW #	COL #	T1#1,1	T1#2,1-3,28	T1#1,1	T1#2,1-3,28	T1#1,1	T1#2,1-3,28
	1-18	19	20-102	103	104-186	187	188-270
1	Unused	V1	V1	V5	-	PPSSSSFR	-
2	Unused	DS0#1	-	DS0#2	-	DS0#3	-
3	Unused	DS0#4	-	DS0#5	-	DS0#6	-
4	Unused	DS0#7	-	DS0#8	-	DS0#9	-
5	Unused	DS0#10	-	DS0#11	-	DS0#12	-
6	Unused	DS0#13	-	DS0#14	-	DS0#15	-
7	Unused	DS0#16	-	DS0#17	-	DS0#18	-
8	Unused	DS0#19	-	DS0#20	-	DS0#21	-
9	Unused	DS0#22	-	DS0#23	-	DS0#24	-
1	Unused	V2	V2	R	-	PPSSSSFR	-
2	Unused	DS0#1	-	DS0#2	-	DS0#3	-
3	Unused	DS0#4	-	DS0#5	-	DS0#6	-
4	Unused	DS0#7	-	DS0#8	-	DS0#9	-



ROW #	COL #	T1#1,1	T1#2,1-3,28	T1#1,1	T1#2,1-3,28	T1#1,1	T1#2,1-3,28
	1-18	19	20-102	103	104-186	187	188-270
5	Unused	DS0#10	-	DS0#11	-	DS0#12	-
6	Unused	DS0#13	-	DS0#14	-	DS0#15	-
7	Unused	DS0#16	-	DS0#17	-	DS0#18	-
8	Unused	DS0#19	-	DS0#20	-	DS0#21	-
9	Unused	DS0#22	-	DS0#23	-	DS0#24	-
1	Unused	V3	V3	R	-	PPSSSSFR	-
2	Unused	DS0#1	-	DS0#2	-	DS0#3	-
3	Unused	DS0#4	-	DS0#5	-	DS0#6	-
4	Unused	DS0#7	-	DS0#8	-	DS0#9	-
5	Unused	DS0#10	-	DS0#11	-	DS0#12	-
6	Unused	DS0#13	-	DS0#14	-	DS0#15	-
7	Unused	DS0#16	-	DS0#17	-	DS0#18	-
8	Unused	DS0#19	-	DS0#20	-	DS0#21	-
9	Unused	DS0#22	-	DS0#23	-	DS0#24	-
1	Unused	V4	V4	R	-	PPSSSSFR	-
2	Unused	DS0#1	-	DS0#2	-	DS0#3	-
3	Unused	DS0#4	-	DS0#5	-	DS0#6	-
4	Unused	DS0#7	-	DS0#8	-	DS0#9	-
5	Unused	DS0#10	-	DS0#11	-	DS0#12	-
6	Unused	DS0#13	-	DS0#14	-	DS0#15	-
7	Unused	DS0#16	-	DS0#17	-	DS0#18	-
8	Unused	DS0#19	-	DS0#20	-	DS0#21	-
9	Unused	DS0#22	-	DS0#23	-	DS0#24	-

The P<sub>1</sub>P<sub>0</sub>S<sub>1</sub>S<sub>2</sub>S<sub>3</sub>S<sub>4</sub>FR octet carries T1 framing in the F bit and channel associated signaling in the P<sub>1</sub>P<sub>0</sub> and S<sub>1</sub>S<sub>2</sub>S<sub>3</sub>S<sub>4</sub> bits. Channel associated signaling is optional. The R bit is reserved and is set to 0. The P<sub>1</sub>P<sub>0</sub> bits are used to indicate the phase of the channel associated signaling and the S<sub>1</sub>S<sub>2</sub>S<sub>3</sub>S<sub>4</sub> bits are the channel associated signaling bits for the 24 DS0 channels in the T1. Table 9 shows the channel associated signaling bit mapping and how the phase bits locate the sixteen state CAS mapping as well as T1 frame alignment for super frame and extended superframe formats. When using four state CAS then the signaling bits are A1-A24, B1-B24, A1-B24, B1-B24 in place of are A1-A24, B1-B24, C1-C24, D1-D24. When using 2 state CAS there are only A1-A24 signaling bits.

**Table 9 T1 Channel Associated Signaling bits**

				SF	ESF	
S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	S <sub>4</sub>	F	F	P <sub>1</sub> P <sub>0</sub>
A1	A2	A3	A4	F1	M1	00

				SF	ESF	
S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	S <sub>4</sub>	F	F	P <sub>1</sub> P <sub>0</sub>
A5	A6	A7	A8	S1	C1	00
A9	A10	A11	A12	F2	M2	00
A13	A14	A15	A16	S2	F1	00
A17	A18	A19	A20	F3	M3	00
A21	A22	A23	A24	S3	C2	00
B1	B2	B3	B4	F4	M4	01
B5	B6	B7	B8	S4	F2	01
B9	B10	B11	B12	F5	M5	01
B13	B14	B15	B16	S5	C3	01
B17	B18	B19	B20	F6	M6	01
B21	B22	B23	B24	S6	F3	01
C1	C2	C3	C4	F1	M7	10
C5	C6	C7	C8	S1	C4	10
C9	C10	C11	C12	F2	M8	10
C13	C14	C15	C16	S2	F4	10
C17	C18	C19	C20	F3	M9	10
C21	C22	C23	C24	S3	C5	10
D1	D2	D3	D4	F4	M10	11
D5	D6	D7	D8	S4	F5	11
D9	D10	D11	D12	F5	M11	11
D13	D14	D15	D16	S5	C6	11
D17	D18	D19	D20	F6	M12	11
D21	D22	D23	D24	S6	F6	11

T1 tributary asynchronous timing is compensated via the V3 octet as described in section 10.1.2. T1 tributary link rate adjustments are optionally passed across the SBI via the V4 octet as described in section 10.1.3. T1 tributary alarm conditions are optionally passed across the SBI bus via the link rate octet in the V4 location as described in section 10.1.3 and 10.1.4.

The SBI bus allows for a synchronous T1 mode of operation. In this mode the T1 tributary mapping is fixed to that shown in Table 8 and rate justifications are not possible using the V3 octet. The clock rate information within the link rate octet in the V4 location is not used in synchronous mode.

### 10.1.6 E1 Tributary Mapping

Table 10 shows the format for mapping 63 E1s within the SPE octets. The timeslots and framing bits within each E1 are easily located within this mapping for channelized E1 applications. It is acceptable for the framing bits to not carry valid framing information on the Add Bus since the physical layer device will provide this information. Unframed E1s use the exact same format for mapping 63 E1s into the SBI except that the E1 tributaries need not align with the timeslot locations associated with channelized E1 applications. The V1,V2 and V4 octets are not used to carry E1 data and are either reserved used for control information across the interface. When enabled, the V4 octet carries clock phase information across the SBI. The V1 and V2 octets are unused and should be ignored by devices listening to the SBI bus. The V5 and R octets do not carry any information and are fixed to a zero value. The V3 octet carries an E1 data octet but only during rate adjustments as indicated by the V5 indicator signals, IV5 and OV5, and payload signals, IPL and OPL. The PP octets carry channel associated signaling phase information and E1 frame alignment. TS#0 through TS#31 make up the E1 channel.

The V1,V2,V3 and V4 octets are fixed to the locations shown. All the other octets, shown shaded for E1#1,1, float within the allocated columns maintaining the same order and moving a maximum of one octet per 2KHz multi-frame. The position of the floating E1 is identified via the V5 Indicator signals, IV5 and OV5, which locate the V5 octet. When the E1 tributary rate is faster than the E1 tributary nominal rate, the E1 tributary is shifted ahead by one octet which is compensated by sending an extra octet in the V3 location. When the E1 tributary rate is slower than the nominal rate the E1 tributary is shifted by one octet which is compensated by inserting a stuff octet in the octet immediately following the V3 octet and delaying the octet that was originally in that position.

**Table 10 E1 Framing Format**

ROW	COL #	E1#1,1	#2,1-3,21	E1#1,1	#2,1-3,21	E1#1,1	#2,1-3,21	E1#1,1	#2,1-
	1-18	19	20-81	82	83-144	145	146-207	208	209-270
1	Unused	V1	V1	V5	-	PP	-	TS#0	-
2	Unused	TS#1	-	TS#2	-	TS#3	-	TS#4	-
3	Unused	TS#5	-	TS#6	-	TS#7	-	TS#8	-
4	Unused	TS#9	-	TS#10	-	TS#11	-	TS#12	-
5	Unused	TS#13	-	TS#14	-	TS#15	-	TS#16	-
6	Unused	TS#17	-	TS#18	-	TS#19	-	TS#20	-
7	Unused	TS#21	-	TS#22	-	TS#23	-	TS#24	-
8	Unused	TS#25	-	TS#26	-	TS#27	-	TS#28	-
9	Unused	TS#29	-	TS#30	-	TS#31	-	R	-
1	Unused	V2	V2	R	-	PP	-	TS#0	-
2	Unused	TS#1	-	TS#2	-	TS#3	-	TS#4	-
3	Unused	TS#5	-	TS#6	-	TS#7	-	TS#8	-
4	Unused	TS#9	-	TS#10	-	TS#11	-	TS#12	-
5	Unused	TS#13	-	TS#14	-	TS#15	-	TS#16	-

ROW	COL #	E1#1,1	#2,1-3,21	E1#1,1	#2,1-3,21	E1#1,1	#2,1-3,21	E1#1,1	#2,1-
	1-18	19	20-81	82	83-144	145	146-207	208	209-270
6	Unused	TS#17	-	TS#18	-	TS#19	-	TS#20	-
7	Unused	TS#21	-	TS#22	-	TS#23	-	TS#24	-
8	Unused	TS#25	-	TS#26	-	TS#27	-	TS#28	-
9	Unused	TS#29	-	TS#30	-	TS#31	-	R	-
1	Unused	V3	V3	R	-	PP	-	TS#0	-
2	Unused	TS#1	-	TS#2	-	TS#3	-	TS#4	-
3	Unused	TS#5	-	TS#6	-	TS#7	-	TS#8	-
4	Unused	TS#9	-	TS#10	-	TS#11	-	TS#12	-
5	Unused	TS#13	-	TS#14	-	TS#15	-	TS#16	-
6	Unused	TS#17	-	TS#18	-	TS#19	-	TS#20	-
7	Unused	TS#21	-	TS#22	-	TS#23	-	TS#24	-
8	Unused	TS#25	-	TS#26	-	TS#27	-	TS#28	-
9	Unused	TS#29	-	TS#30	-	TS#31	-	R	-
1	Unused	V4	V4	R	-	PP	-	TS#0	-
2	Unused	TS#1	-	TS#2	-	TS#3	-	TS#4	-
3	Unused	TS#5	-	TS#6	-	TS#7	-	TS#8	-
4	Unused	TS#9	-	TS#10	-	TS#11	-	TS#12	-
5	Unused	TS#13	-	TS#14	-	TS#15	-	TS#16	-
6	Unused	TS#17	-	TS#18	-	TS#19	-	TS#20	-
7	Unused	TS#21	-	TS#22	-	TS#23	-	TS#24	-
8	Unused	TS#25	-	TS#26	-	TS#27	-	TS#28	-
9	Unused	TS#29	-	TS#30	-	TS#31	-	R	-

When using channel associated signaling (CAS) TS#16 carries the ABCD signaling bits and the timeslots 17 through 31 are renumbered 16 through 30. The PP octet is 0h for all frames except for the frame which carries the CAS for timeslots 15/30 at which time the PP octet is C0h. The first octet of the CAS multi-frame, RRRRRRRR, is reserved and should be ignored by the receiver when CAS signaling is enabled. Table 11 shows the format of timeslot 16 when carrying channel associated signaling.

**Table 11 E1 Channel Associated Signaling bits**

TS#16[7:4]	TS#16[3:0]	PP
RRRR	RRRR	00
ABCD1	ABCD16	00
ABCD2	ABCD17	00
ABCD3	ABCD18	00
ABCD4	ABCD19	00
ABCD5	ABCD20	00
ABCD6	ABCD21	00
ABCD7	ABCD22	00
ABCD8	ABCD23	00
ABCD9	ABCD24	00
ABCD10	ABCD25	00
ABCD11	ABCD26	00
ABCD12	ABCD27	00
ABCD13	ABCD28	00
ABCD14	ABCD29	00
ABCD15	ABCD30	C0

E1 tributary asynchronous timing is compensated via the V3 octet as described in section 10.1.2. E1 tributary link rate adjustments are optionally passed across the SBI via the V4 octet as described in section 10.1.3. E1 tributary alarm conditions are optionally passed across the SBI bus via the link rate octet in the V4 location as described in section 10.1.3 and 10.1.4.

The SBI bus allows for a synchronous E1 mode of operation. In this mode the E1 tributary mapping is fixed to that shown in Table 10 and rate justifications are not possible using the V3 octet. The clock rate information within the link rate octet in the V4 location is not used in synchronous mode.

### 10.1.7 DS3 Tributary Mapping

Table 12 shows a DS3 tributary mapped within the first synchronous payload envelope SPE1. The V5 indicator pulse identifies the V5 octet. The DS3 framing format does not follow an 8KHz frame period so the floating DS3 multi-frame located by the V5 indicator, shown in heavy border gray region in Table 12, will jump around relative to the H1 frame on every pass. In fact the V5 indicator will often be asserted twice per H1 frame, as is shown by the second V5 octet in Table 12. The V5 indicator and payload signals indicate negative and positive rate adjustments which are carried out by either putting a data byte in the H3 octet or leaving empty the octet after the H3 octet.

**Table 12 DS3 Framing Format**

	SPE COL#		DS3 1	DS3 2-56	DS3 57	DS3 58-84	DS3 85
ROW	SBI COL# 1,4,7,10	13	16	...	184	...	268
1	Unused	H1	V5	DS3	DS3	DS3	DS3
2	Unused	H2	DS3	DS3	DS3	DS3	DS3
3	Unused	H3	DS3	DS3	DS3	DS3	DS3
4	Unused	Linkrate	DS3	DS3	DS3	DS3	DS3
5	Unused	Unused	DS3	DS3	DS3	DS3	DS3
6	Unused	Unused	DS3	DS3	DS3	DS3	DS3
7	Unused	Unused	DS3	DS3	DS3	DS3	DS3
8	Unused	Unused	DS3	DS3	V5	DS3	DS3
9	Unused	Unused	DS3	DS3	DS3	DS3	DS3

Because the DS3 tributary rate is less than the rate of the gray region, padding octets are interleaved with the DS3 tributary to make up the difference in rate. Interleaved with every DS3 multi-frame are 35 stuff octets, one of which is the V5 octet. These 35 stuff octets are spread evenly across seven DS3 subframes. Each DS3 subframe is eight blocks of 85 bits. The 85 bits making up a DS3 block are padded out to be 11 octets. Table 13 shows the DS3 block 11 octet format where R indicates a stuff bit, F indicates a DS3 framing bit and I indicates DS3 information bits. Table 14 shows the DS3 multi-frame format that is packed into the gray region of Table 12. In this table V5 indicates the V5 octet which is also a stuff octet, R indicates a stuff octet and B indicates the 11 octet DS3 block. Each row in Table 14 is a DS3 multi-frame. The DS3 multi-frame stuffing format is identical for 5 multi-frames and then an extra stuff octet after the V5 octet is added every sixth frame.

**Table 13 DS3 Block Format**

Octet #	1	2	3	4	5	6	7	8	9	10	11
Data	RRRFIIII	8*I	8*I	8*I	8*I	8*I	8*I	8*I	8*I	8*I	8*I

**Table 14 DS3 Multi-frame Stuffing Format**

V5	4*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B
V5	4*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B
V5	4*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B
V5	4*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B
V5	4*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B
V5	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B

DS3 asynchronous timing is compensated via the H3 octet as described in section 10.1.2. DS3 link rate adjustments are optionally passed across the SBI via the Linkrate octet as described in section 10.1.3. DS3 alarm conditions are optionally passed across the SBI bus via the Linkrate octet as described in section 10.1.3 and 10.1.4.

### 10.1.8 E3 Tributary Mapping

Table 15 shows a E3 tributary mapped within the first synchronous payload envelope SPE1. The V5 indicator pulse identifies the V5 octet. The E3 framing format does not follow an 8KHz frame period so the floating frame located by the V5 indicator and shown in gray in Table 15, will jump around relative to the H1 frame on every pass. In fact the V5 indicator will be asserted two or three times per H1 frame, as is shown by the second and third V5 octet in Table 15. The V5 indicator and payload signals indicate negative and positive rate adjustments which are carried out by either putting a data byte in the H3 octet or leaving empty the octet after the H3 octet.

**Table 15 E3 Framing Format**

	SPE COL#		E3 1	E3 2-18	E3 19	E3 20-38	E3 39	E3 40-84	E3 85
ROW	SBI COL# 1,4,7,10	13	16	...	70	...	130	...	268
1	Unused	H1	V5	E3	E3	E3	E3	E3	E3
2	Unused	H2	E3	E3	E3	E3	E3	E3	E3
3	Unused	H3	E3	E3	E3	E3	E3	E3	E3
4	Unused	Linkrate	E3	E3	V5	E3	E3	E3	E3
5	Unused	Unused	E3	E3	E3	E3	E3	E3	E3
6	Unused	Unused	E3	E3	E3	E3	E3	E3	E3
7	Unused	Unused	E3	E3	E3	E3	V5	E3	E3
8	Unused	Unused	E3	E3	E3	E3	E3	E3	E3
9	Unused	Unused	E3	E3	E3	E3	E3	E3	E3

Because the E3 tributary rate is less than the rate of the gray region, padding octets are interleaved with the E3 tributary to make up the difference in rate. Interleaved with every E3 frame is an alternating pattern of 81 and 82 stuff octets, one of which is the V5 octet. These 81 or 82 stuff octets are spread evenly across the E3 frame. Each E3 subframe is 48 octet which is further broken into 4 equal blocks of 12 octets each. Table 16 shows the alternating E3 frame stuffing format that is packed into the gray region of Table 15. Note that there are 6 stuff octets after the V5 octet in one frame and 5 stuff octets after the V5 octet in the next frame. In this table V5 indicates the V5 octet which is also a stuff octet, R indicates a stuff octet, D indicates an E3 data octet, FAS indicates the first byte of the 10 bit E3 Frame Alignment Signal.

**Table 16 E3 Frame Stuffing Format**

V5	6*R	FAS	11*D	5*R	12*D	5*R	12*D	5*R	12*D
	5*R	FAS	11*D	5*R	12*D	5*R	12*D	5*R	12*D
	5*R	FAS	11*D	5*R	12*D	5*R	12*D	5*R	12*D
	5*R	FAS	11*D	5*R	12*D	5*R	12*D	5*R	12*D
V5	5*R	FAS	11*D	5*R	12*D	5*R	12*D	5*R	12*D
	5*R	FAS	11*D	5*R	12*D	5*R	12*D	5*R	12*D
	5*R	FAS	11*D	5*R	12*D	5*R	12*D	5*R	12*D
	5*R	FAS	11*D	5*R	12*D	5*R	12*D	5*R	12*D

E3 asynchronous timing is compensated via the H3 octet as described in section 10.1.2. E3 link rate adjustments are optionally passed across the SBI via the Linkrate octet as described in section 10.1.3. E3 alarm conditions are optionally passed across the SBI bus via the Linkrate octet as described in section 10.1.3 and 10.1.4.

### 10.1.9 Transparent VT1.5/TU11 Mapping

VT1.5 and TU11 virtual tributaries, TVT1.5s, are transported across the SBI bus in a similar manner to the T1 tributary mapping. Table 17 shows the transparent structure where “I” is used to indicate information bytes. There are two options when carrying virtual tributaries on the SBI bus, the primary difference being how the floating V5 payload is located.

The first option is locked TVT mode which carries the entire VT1.5/TU11 virtual tributary indicated by the shaded region in Table 17. Locked is used to indicate that the location of the V1,V2 pointer is locked. The virtual tributary must have a valid V1,V2 pointer to locate the V5 payload. In this mode the V5 indicator and payload signals, IV5, OV5, IPL and OPL, may be generated but must be ignored by the receiving device. In locked mode timing is always sourced by the transmitting side, therefore justification requests are not used and the JUST\_REQ signal is ignored. Other than the V1 and V2 octets which must carry valid pointers, all octets can carry data in any format. The location of the V1,V2,V3 and V4 octets is fixed to the locations shown in Table 17.

The second option is floating TVT mode which carries the payload comprised of the V5 and I octets within the shaded region of Table 17. In this mode the V1,V2 pointers are still in a fixed location and may be valid but are ignored by the receiving device. The V5 indicator and payload signals, IV5, OV5, IPL and OPL, must be valid and are used to locate the floating payload. The justification request signal can be used to control the timing on the add bus. The V3 octets are used to accommodate justification requests. The location of the V1,V2,V3 and V4 octets is fixed to the locations shown in Table 17.

**Table 17 Transparent VT1.5/TU11 Format**

ROW #	COL #	VT1.5#1,1	#2,1-3,28	VT1.5#1,1	#2,1-3,28	VT1.5#1,1	#2,1-3,28
	1-18	19	20-102	103	104-186	187	188-270
1	Unused	V1	V1	V5	-	I	-



ROW #	COL #	VT1.5#1,1	#2,1-3,28	VT1.5#1,1	#2,1-3,28	VT1.5#1,1	#2,1-3,28
	1-18	19	20-102	103	104-186	187	188-270
2	Unused		-		-		-
3	Unused		-		-		-
4	Unused		-		-		-
5	Unused		-		-		-
6	Unused		-		-		-
7	Unused		-		-		-
8	Unused		-		-		-
9	Unused		-		-		-
1	Unused	V2	V2		-		-
2	Unused		-		-		-
3	Unused		-		-		-
4	Unused		-		-		-
5	Unused		-		-		-
6	Unused		-		-		-
7	Unused		-		-		-
8	Unused		-		-		-
9	Unused		-		-		-
1	Unused	V3	V3		-		-
2	Unused		-		-		-
3	Unused		-		-		-
4	Unused		-		-		-
5	Unused		-		-		-
6	Unused		-		-		-
7	Unused		-		-		-
8	Unused		-		-		-
9	Unused		-		-		-
1	Unused	V4	V4		-		-
2	Unused		-		-		-
3	Unused		-		-		-
4	Unused		-		-		-
5	Unused		-		-		-
6	Unused		-		-		-
7	Unused		-		-		-
8	Unused		-		-		-
9	Unused		-		-		-

### 10.1.10 Transparent VT2/TU12 Mapping

VT2 and TU12 virtual tributaries, TTV2s, are transported across the SBI bus in a similar manner to the E1 tributary mapping. Table 18 shows the transparent structure where “I” is used to indicate information bytes. There are two options when carrying virtual tributaries on the SBI bus, the primary difference being how the floating V5 payload is located.

The first option is locked TTV mode which carries the entire VT2/TU12 virtual tributary indicated by the shaded region in Table 18. Locked is used to indicate that the location of the V1,V2 pointer is locked. The virtual tributary must have a valid V1,V2 pointer to locate the V5 payload. In this mode the V5 indicator and payload signals, IV5, OV5, IPL and OPL, are optionally generated but must be ignored by the receiving device. In locked mode timing is always sourced by the transmitting side, therefore justification requests are not used and the JUST\_REQ signal is ignored. Other than the V1 and V2 octets which are carrying valid pointers, all octets can carry data in any format. The location of the V1,V2,V3 and V4 octets is fixed to the locations shown in Table 18.

The second option is floating TTV mode which carries the payload comprised of the V5 and I octets within the shaded region of Table 18. In this mode the V1,V2 pointers are still in a fixed location and may be valid but are ignored by the receiving device. The V5 indicator and payload signals, IV5, OV5, IPL and OPL, must be valid and are used to locate the floating payload. The justification request signal can be used to control the timing on the add bus. The V3 octet is used to accommodate justification requests. The location of the V1,V2,V3 and V4 octets is fixed to the locations shown in Table 18.

**Table 18 Transparent VT2/TU12 Format**

COL #	E1#1,1	#2,1-3,21	E1#1,1	#2,1-3,21	E1#1,1	#2,1-3,21	E1#1,1	#2,1-
1-18	19	20-81	82	83-144	145	146-207	208	209-270
1	Unused	V1	V1	V5	-	I	-	I
2	Unused	I	-	I	-	I	-	I
3	Unused	I	-	I	-	I	-	I
4	Unused	I	-	I	-	I	-	I
5	Unused	I	-	I	-	I	-	I
6	Unused	I	-	I	-	I	-	I
7	Unused	I	-	I	-	I	-	I
8	Unused	I	-	I	-	I	-	I
9	Unused	I	-	I	-	I	-	I
1	Unused	V2	V2	I	-	I	-	I
2	Unused	I	-	I	-	I	-	I
3	Unused	I	-	I	-	I	-	I
4	Unused	I	-	I	-	I	-	I
5	Unused	I	-	I	-	I	-	I
6	Unused	I	-	I	-	I	-	I

ROW	COL #	E1#1,1	#2,1-3,21	E1#1,1	#2,1-3,21	E1#1,1	#2,1-3,21	E1#1,1	#2,1-
	1-18	19	20-81	82	83-144	145	146-207	208	209-270
7	Unused	I	-	I	-	I	-	I	-
8	Unused	I	-	I	-	I	-	I	-
9	Unused	I	-	I	-	I	-	I	-
1	Unused	V3	V3	I	-	I	-	I	-
2	Unused	I	-	I	-	I	-	I	-
3	Unused	I	-	I	-	I	-	I	-
4	Unused	I	-	I	-	I	-	I	-
5	Unused	I	-	I	-	I	-	I	-
6	Unused	I	-	I	-	I	-	I	-
7	Unused	I	-	I	-	I	-	I	-
8	Unused	I	-	I	-	I	-	I	-
9	Unused	I	-	I	-	I	-	I	-
1	Unused	V4	V4	I	-	I	-	I	-
2	Unused	I	-	I	-	I	-	I	-
3	Unused	I	-	I	-	I	-	I	-
4	Unused	I	-	I	-	I	-	I	-
5	Unused	I	-	I	-	I	-	I	-
6	Unused	I	-	I	-	I	-	I	-
7	Unused	I	-	I	-	I	-	I	-
8	Unused	I	-	I	-	I	-	I	-
9	Unused	I	-	I	-	I	-	I	-

### 10.1.11 Fractional Rate Tributary Mapping

The Fractional Rate SBI mapping is intended for support of data services over fractional DS3 or similar links. A fractional rate link is mapped into any SPE octet as defined in Table 1. Table 19 shows all the available information (I) octets useable for carrying a Fractional rate link mapped to a single SPE. There are no V1 to V5 bytes nor frame alignment signals in a fractional rate link. The Add bus and Drop bus payload signals, IPL and OPL, indicate when a fractional rate information byte contains valid data or is empty. The fractional rate link Add bus can have the timing master be either the PHY or the Link Layer device. When the PHY is the timing master the JUST\_REQ signal from the PHY communicates the transmit rate to the Link Layer device. The JUST\_REQ signal is asserted during any of the available fractional rate link octets to indicate that the PHY can accept another byte of data. For every byte that is marked with the JUST\_REQ signal the Link Layer device should respond with a valid byte to the PHY within a short time. The PHY accepts data from the Link Layer device whenever it sees valid data as indicated by the IPL or OPL signal, whether it is timing master or slave.

**Table 19 Fractional Rate Format**

	SPE COL#	Fractional 1	Fractional 2-84	Fractional 85
ROW	SBI COL# 1,4,7,10,13	16	...	268
1	Unused			
2	Unused			
3	Unused			
4	Unused			
5	Unused			
6	Unused			
7	Unused			
8	Unused			
9	Unused			

**10.1.12 SBI336 Bus Format**

The interface on the SBSLITE is a 77.76MHz SBI336 bus. The 77.76MHz SBI336 bus is exactly four interleaved 19.44MHz SBI buses. There are some slight differences between the two formats to accommodate the increased clock rate. The differences are:

The JUST\_REQ signal is referenced to the Drop bus C1FP alignment rather than the common Add/Drop C1FP alignment of the SBI bus. This aids 77.76MHz bus timing by allowing buffering and retiming logic to be put between SBI336 devices. This change also aids construction of larger SBI cross connect systems using smaller buffers between devices by controlling the C1 frame alignment independently in each direction.

**10.1.13 SBI336 Multiplexing Structure**

**Table 20 Structure for Carrying Multiplexed Links in SBI336**

		SBI Column																		
		1	24	25	26	60	61	62	63	64	65	66	67	68	1078	1079	1080			
Row	1	-	...	-	C1	-	...	-	1,SPE1	2,SPE1	3,SPE1	4,SPE1	1,SPE2	2,SPE2	3,SPE2	4,SPE2	...	2,SPE3	3,SPE3	4,SPE3
	2	-	...	-	-	-	...	-	1,SPE1	2,SPE1	3,SPE1	4,SPE1	1,SPE2	2,SPE2	3,SPE2	4,SPE2	...	2,SPE3	3,SPE3	4,SPE3
		⋮																		
	9	-	-	-	-	-	-	-	1,SPE1	2,SPE1	3,SPE1	4,SPE1	1,SPE2	2,SPE2	3,SPE2	4,SPE2	...	2,SPE3	3,SPE3	4,SPE3
		1	2	3	3	5	6	6	6	6	6	6	6	6	6	6	6	90	90	90
		SPE Column																		

Table 20 shows how 12 SPEs are multiplexed into a 77.76MHz SBI336 bus. The structure is exactly the same as byte interleaving four 19.44MHz SBI buses. 1,SPE1 identifies SPE1 from the first SBI equivalent bus, 2,SPE1 identifies SPE1 from the second SBI equivalent bus, and so on. All tributary mapping formats are exactly the same as for the 19.44MHz SBI bus with the only difference that there are four times the number of tributaries. Tributary numbering appends the equivalent SBI number to the original SBI numbering. For example, the first T1 in a SBI bus would be numbered T1 #1,1 whereas the first T1 in a SBI336 bus would be numbered T1 #1,1,1. Likewise the second T1 in a SBI bus would be T1 #2,1 whereas the second T1 in a SBI336 bus would be T1 #2,1,1.

## 10.2 Incoming SBI336 Timing Adapter

The Incoming SBI336 Timing Adapter, ISTA, provides parity checking of the incoming 77.76MHz SBI336 or TelecomBus. Parity can be configured to be either even or odd. In SBI336 mode, the parity calculation encompasses the IDATA[7:0], IPL and IV5 signals. In 77.76MHz TelecomBus mode, the parity calculation encompasses the IDATA[7:0] signals and optionally the IC1FP and IPL signals. If enabled, an interrupt can be generated whenever a parity error is detected.

## 10.3 CAS Expanders

The Channel Associated Signaling Expander blocks, ICASE and OCASE, pull the CAS information from the SBI336 formatted bus on a tributary basis so that it can be switched through the memory switch with the DS0 data. For tributaries enabled for DS0 switching the Channel Associated Signaling bits (CAS bits) are double buffered on a signaling multi-frame boundary and repeated along side the tributary data for the duration of the multi-frame. This block can be used for T1 and E1 tributaries simultaneously across different SBI SPEs. This block adds one T1 multi-frame (24 frames) or one E1 multi-frame (16 frames) of latency to the CAS bits.

## 10.4 Memory Switch Units

The Memory Switch Unit blocks, IMSU and OMSU, provide DS0 or column switching of the SBI336 or 77.76MHz TelecomBus. Any input byte (or column) can be switched to any output byte (or column). Four bits of Channel Associated Signaling (CAS) and three or four bits of control information are switched along with the data byte. In SBI336 mode, the control signals are PL, V5 and JUST\_REQ. In TelecomBus mode, the control signals are PL, TPL, V5 and TAIS.

In DS0 switch mode, the data entering the MSU is stored in two alternating pages of memory. Each page contains one complete frame (9720 bytes) of data. One of these alternating pages is currently filling while the other is currently full. Data exiting the MSU is extracted from the currently full page. As a consequence, the MSU imposes a nominal switching latency of 1 frame (125us). The selection of bytes to fill each output port requires a switching connection memory. Control is required for each of the 9720 bytes in the output SBI336 frame. Complete specification of an output byte requires 14 bits to specify which of the 9720 input bytes to use. Dual copies of this control memory are required to provide hitless frame boundary switchover.

In column switch mode, the same switching principle described above is used, but less memory is required. Data entering the MSU is stored in two alternating pages of memory. Each page contains one row (1080 bytes) of data. In this mode, the nominal latency is 1 row if a frame (<15 us). The switching connection memory for the output port requires control for each of the 1080 columns in the frame. Complete specification of an output column requires 11 bits to specify which of the 1080 input columns to use. Dual copies of this control memory are required to provide hitless frame boundary switchover.

Each MSU can be independently bypassed for reduced latency or debugging purposes.

#### 10.4.1 Data Buffer

The Data Buffer block contains a double buffer structure for each frame consisting of a data byte, 4-bits of Channel Associated Signaling information and 4 bits of control information necessary for identifying valid data and timing.

#### 10.4.2 Connection Memory

The Connection Memory sub-block contains two pages of mapping configuration, page 0 and page 1. One page is designated the active page and the other the stand-by page. Selection between which page is to be active and which is to be stand-by is controlled by the ICMP signal (for the IMSU) and OCMP signal (for the OMSU). The Connection Memory sub-block samples the value on the ICMP signal at the C1 byte position as defined by the incoming frame pulse signal, IC1FP. The Connection Memory sub-block samples the value on the OCMP signal at the C1 byte position as defined by the receive serial interface frame pulse signal, RC1FP. Swaps between the active/standby status of the two pages are synchronized to the first A1 byte of the next frame or multi-frame. This arrangement allows all devices in a cross-connect system to be updated in a coordinated fashion. Consequently, DS0 streams or tributaries not being assigned new positions are unaffected by page swaps.

The CMP input signals can be overridden by register configuration or by the SBI336S in-band link channel.

### 10.5 CAS Merging

The Channel Associated Signaling Merge blocks, ICASM and OCASM, insert the CAS signaling information into the SBI bus on a tributary basis. CAS signaling channels within the SBI bus are constructed out of the available CAS bits for T1 and E1 SBI tributaries that are enabled for CAS signaling. The resulting CAS signaling channel replaces the octets of the SBI bus where the new CAS signaling is to be inserted. This function is enabled on a per-tributary basis and can be used for T1 and E1 tributaries simultaneously across different SBI SPEs. This block adds one T1 multi-frame (24 frames) or one E1 multi-frame (16 frames) of latency to the CAS bits.

## 10.6 Incoming SBI336 Tributary Translator

The Incoming SBI336 Tributary Translator block, ISTT, translates all SBI336 timing and Channel Associated Signaling information for all tributaries into SBI336S format. The output from this block is a 77.76MHz SBI336 stream with all tributaries and control signals encoded into an internal format that closely resembles the serial SBI336S format.

This block translates all tributary types into a form that is easy for the 8B/10B encoder to handle in a more generic form. A control RAM keeps the current configuration for each of the incoming SBI bus tributaries so that it can perform the translation function.

Common to all tributaries is identification of the first C1 byte. There are unique mappings of the 8B/10B codes for the supported SBI and SBI336 bus link types: Asynchronous T1/E1, Synchronous (locked) T1/E1, Transparent VT1.5/VT2, DS3/E3 and Fractional rate links. Much of the identification and mapping of a link into serial SBI format is based on the C1 frame pulse and a tributaries location relative to that C1 pulse. In addition to the C1FP identification this block identifies multi-frame alignment, valid payload, pointer movements for floating tributaries and timing control for encoding into the 8B/10B serial SBI format.

This block is transparent in TelecomBus mode.

## 10.7 PRBS Processors

The Working and Protection PRBS Processor blocks, WPP and PPP, provides in-service and off-line PRBS generation and detection for diagnostics of the equipment downstream of the two LVDS links. Each PRBS Processor has the capacity to source and monitor PRBS data for the associated Working or Protection Serial SBI336S stream with a granularity of unchannelized SBI SPEs of TelecomBus STS/AUs.

### 10.7.1 PRBS Generator

The PRBS generator sub-block optionally overwrites the data originating from the incoming data streams, IDATA[4:1][7:0]. When enabled, the PRBS generator sub-block inserts synchronous payload envelope, SPE bytes into the serial transmit links. The inserted data is derived from an internal linear feedback shift register (LFSR) with a polynomial of  $X^{23} + X^{18} + 1$ .

## 10.7.2 PRBS Detector

The PRBS detector sub-block monitors the synchronous payload envelope, SPE, bytes in the incoming data stream. The incoming data is compared against the expected value derived from an internal linear feedback shift register (LFSR) with a polynomial of  $X^{23} + X^{18} + 1$ . If the incoming data fails to match the expected value for three consecutive bytes, the PRBS detector sub-block will enter out-of-synchronization (OOS) state. The LFSR will be re-initialized using the incoming data bytes. The new LFSR seed is confirmed by comparison with subsequent incoming data bytes. The PRBS detector sub-block will exit the OOS state when the incoming data matches the LFSR output for three consecutive bytes. The PRBS detector sub-block will remain in the OOS state and re-load the LFSR if confirmation failed. The PRBS sub-block counts PRBS byte errors and optionally generates interrupts when it enters and exits the OOS state.

## 10.8 Transmit 8B/10B Encoders

The Transmit 8B/10B Encoder blocks, TW8E and TP8E, construct an 8B/10B character stream from an incoming translated SBI336 bus or TelecomBus carrying an STS-12/STM-4 equivalent stream.

In SBI mode, these blocks encode the SBI336S stream as shown in Table 21. When configured for Synchronous mode for DS0 switching, the 8B/10B encoder transmits CAS signaling multi-frame alignment across the SBI336S interface by generating a C1FP character every 48 frame times. When not configured for DS0 switching the C1FP character is sent every 4 frames.

### 10.8.1 SBI336S 8B/10B Character Encoding

Table 21 shows the mapping of SBI336S bus control bytes and signals into 8B/10B control characters. The linkrate octet in location V4, V1 and V2, the in-band programming channel, the V3 octet when it contains data are all carried as data. Justification requests for master timing are carried in the V5 character so there are three V5 characters used, nominal, negative timing adjustment request, and positive timing adjustment request.

**Table 21 SBI336S Character Encoding**

Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Encoded Signals Description
Common to All Link Types			
K28.5	001111 1010	110000 0101	IC1FP='b1 C1FP frame and multi-frame alignment
K23.7-	111010 1000	-	Overhead Bytes (columns 1-60 or 1-72 except for C1 and in-band programming channel), V3 or H3 byte except during negative justification, byte after V3 or H3 byte during positive justification, unused bytes in fraction rate links
Asynchronous T1/E1 Links			
K27.7-	110110 1000	-	V5 byte, no justification request



Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Encoded Signals Description
K28.7-	001111 1000	-	V5 byte, negative justification request
K29.7-	101110 1000	-	V5 byte, positive justification request
Synchronous T1/E1 Links			
K27.7-	110110 1000	-	V5 byte
Asynchronous DS3/E3 Links			
K27.7-	110110 1000	-	V5 byte, no justification request
K28.7-	001111 1000	-	V5 byte, negative justification request*
K29.7-	101110 1000	-	V5 byte, positive justification request*
Fractional Rate Links			
K28.7-	001111 1000	-	V5 byte, send one extra byte request**
K29.7-	101110 1000	-	V5 byte, send one less byte request**
Floating Transparent Virtual Tributaries			
K27.7-	110110 1000	-	V5 byte IV5=1, IDATA[0,4] = ERDI[1:0] = 'b00, IDATA[5] = REI = 'b0
K27.7+	-	001001 0111	V5 byte IV5=1, IDATA[0,4] = ERDI[1:0] = 'b00, IDATA[5] = REI = 'b1
K28.7-	001111 1000	-	V5 byte IV5=1, IDATA[0,4] = ERDI[1:0] = 'b01, IDATA[5] = REI = 'b0
K28.7+	-	110000 0111	V5 byte IV5=1, IDATA[0,4] = ERDI[1:0] = 'b01, IDATA[5] = REI = 'b1
K29.7-	101110 1000	-	V5 byte IV5=1, IDATA[0,4] = ERDI[1:0] = 'b10, IDATA[5] = REI = 'b0
K29.7+	-	010001 0111	V5 byte IV5=1, IDATA[0,4] = ERDI[1:0] = 'b10, IDATA[5] = REI = 'b1
K30.7-	011110 1000	-	V5 byte IV5=1, IDATA[0,4] = ERDI[1:0] = 'b11, IDATA[5] = REI = 'b0
K30.7+	-	100001 0111	V5 byte IV5=1, IDATA[0,4] = ERDI[1:0] = 'b11, IDATA[5] = REI = 'b1

\* Note there can be multiple V5s per SBI frame when in DS3 or E3 mode but only one justification can occur per SBI frame. Positive and negative justification request through V5 required by the SBI336S interface should be limited to one per frame.

\*\* Note fractional rate links are symmetric in the transmit and receive direction over SBI336S. When using clock slave mode with a fractional rate link the clock master makes single byte adjustments to the slave's rate once per frame.

## 10.8.2 Serial TelecomBus 8B/10B Character Encoding

Table 22 shows the mapping of TelecomBus control bytes and signals into 8B/10B control characters. When the TelecomBus control signals conflict each other, the 8B/10B control characters are generated according to the sequence of the table, with the characters at the top of the table taking precedence over those lower in the table.

**Table 22 Serial TelecomBus Character Encoding**

Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Encoded Signals Description
Multiplex Section Termination (MST) Mode			
K28.5	001111 1010	110000 0101	IC1FP='b1 IPL='b0 C1FP frame and multi-frame alignment
High Order Path Termination (HPT) Mode			
K28.0-	001111 0100	-	IPL='b0 High-order path H3 byte position, no negative justification event.
K28.0+	-	110000 1011	IPL='b0 High-order path PSO byte position, positive justification event.
K28.6	001111 0110	110000 1001	IC1FP='b1, IPL='b1 High-order path frame alignment (J1).
Low Order Path Termination (LPT) Mode			
K28.4+	-	110000 1101	IT AIS='b1 Low-order path AIS.
K27.7-	110110 1000	-	IV5='b1, IDATA[0,4] = ERDI[1:0] = 'b00, IDATA[5] = REI = 'b0 Low order path frame alignment. ERDI and REI are encoded in the V5 byte.
K27.7+	-	001001 0111	IV5='b1, IDATA[0,4] = ERDI[1:0] = 'b00, IDATA[5] = REI = 'b1 Low order path frame alignment. ERDI and REI are encoded in the V5 byte.
K28.7-	001111 1000	-	IV5='b1, IDATA[0,4] = ERDI[1:0] = 'b01, IDATA[5] =

Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Encoded Signals Description
			REI = 'b0 Low order path frame alignment. ERDI and REI are encoded in the V5 byte.
K28.7+	-	110000 0111	IV5='b1, IDATA[0,4] = ERDI[1:0] = 'b01, IDATA[5] = REI = 'b1 Low order path frame alignment. ERDI and REI are encoded in the V5 byte.
K29.7-	101110 1000	-	IV5='b1, IDATA[0,4] = ERDI[1:0] = 'b10, IDATA[5] = REI = 'b0 Low order path frame alignment. ERDI and REI are encoded in the V5 byte.
K29.7+	-	010001 0111	IV5='b1, IDATA[0,4] = ERDI[1:0] = 'b10, IDATA[5] = REI = 'b1 Low order path frame alignment. ERDI and REI are encoded in the V5 byte.
K30.7-	011110 1000	-	IV5='b1, IDATA[0,4] = ERDI[1:0] = 'b11, IDATA[5] = REI = 'b0 Low order path frame alignment. ERDI and REI are encoded in the V5 byte.
K30.7+	-	100001 0111	IV5='b1, IDATA[0,4] = ERDI[1:0] = 'b11, IDATA[5] = REI = 'b1 Low order path frame alignment. ERDI and REI are encoded in the V5 byte.
K23.7-	111010 1000	000101 0111	ITPL='b0 Non low-order path payload bytes.

## 10.9 Transmit Serializer

The Transmit Serializer blocks, TWPS and TPPS, convert 8B/10B characters to bit-serial format. The Transmit Working Serializer, TWPS, generates a serial stream for the working transmit LVDS link, TPWRK/TNWRK. The Transmit Protect Serializer, TPPS, generates a serial stream for the protect transmit LVDS link, TPPROT/TNPROT.

## 10.10 LVDS Transmitters

The LVDS Transmitters, TWLV and TPLV, convert 8B/10B encoded digital bit-serial streams to LVDS signaling levels. The Transmit Working LVDS Interface, TWLV, drives the working transmit LVDS links, TPWRK/TNWRK. The Transmit Protect LVDS Interface block, TPLV, drives the protect transmit LVDS link, TPPROT/TNPROT.

## 10.11 Clock Synthesis Unit

The Clock Synthesis Unit, CSU, block generates the 777.6 MHz clock for the transmit and receive LVDS links. To ensure proper operation of the CSU, it must be reset for a minimum of 1ms. This can be accomplished by either holding RSTB low for 1ms or by setting the ARESET bit in register 000H for 1ms.

## 10.12 Transmit Reference Generator

The Transmit Voltage Reference Generator block generates bias voltages and currents for the LVDS Transmitters.

## 10.13 LVDS Receivers

The LVDS Receivers, RWLV and RPLV, convert LVDS signaling levels to 8B/10B encoded digital bit-serial. The Receive Working LVDS Interface block, RWLV, connects to the working receive LVDS links, RPWRK/RNWRK. The Receive Protect LVDS Interface block, RPLV, connects to the protect receive LVDS link RPPROT/RNPROT.

## 10.14 Data Recovery Units

The Data Recovery Units, WDRU and PDRU, monitor the receive LVDS link for transitions to determine the extent of bit cycles on the link. It then adjusts its internal timing to sample the link in the middle of the data "eye". WDRU retrieves data from the working receive LVDS link, RPWRK/RNWRK. PDRU processes the protect receive LVDS link, RPPROT/RNPROT.

The DRU block also converts the serial stream into 10-bit words. The words are constructed from ten consecutive received bits without regard to 8B/10B character boundaries.

## 10.15 Receive 8B/10B Decoders

The Receive 8B/10B serial SBI336S Bus decoders, RW8D and RP8D, frame to the receive stream to find 8B/10B character boundaries. It also contains a FIFO to bridge between the timing domain of the receive LVDS links and the system clock timing domain. The RW8D block performs framing and elastic store functions on data retrieved from the working receive LVDS link, RPWRK/RNWRK. The RP8D block processes data on the protect receive LVDS link, RPPROT/RNPROT.

### 10.15.1 FIFO Buffer

The FIFO buffer sub-block provides isolation between the timing domain of the associated receive LVDS link and that of the system clock, SYSCLK. The FIFO also provides a retiming function to allow individual links in a multi-SBS system to have varying interconnect delay. This eases timing distribution and synchronization in large systems. Data with arbitrary alignment to 8B/10B characters are written into a 10-bit by 24-word deep FIFO at the link clock rate. Data is read from the FIFO at every SYSCLK cycle.

### 10.15.2 Serial SBI336S and TelecomBus Alignment

The alignment functionality performed by each receiver can be broken down into two parts, character alignment and frame alignment. Character alignment finds the 8B/10B character boundary in the arbitrarily aligned incoming data. Frame alignment finds SBI336S or TelecomBus frame and multi-frame boundaries within the Serial link.

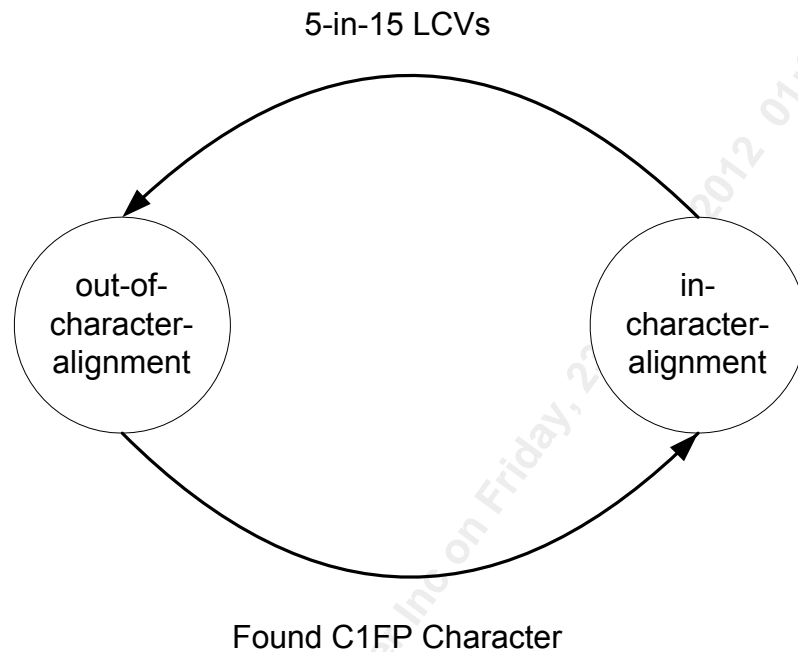
The character and frame alignment are expected to be robust enough for operation over a cabled interconnect.

### 10.15.3 Character Alignment Block

Character alignment locates character boundaries in the incoming 8B/10B data stream. The character alignment algorithm may be in one of two states, in-character-alignment state and out-of-character-alignment state. The two states of the character alignment algorithm is shown in Figure 8.

When the character alignment state machine is in the out-of-character-alignment state, it maintains the current alignment, while searching for a C1FP character. If it finds the C1FP character it will re-align to the C1FP character and move to the in-character-alignment state. The C1FP character is found by searching for the 8B/10B C1FP character, K28.5+ or K28.5-, simultaneously in ten possible bit locations. While in the in-character-alignment state, the state machine monitors LCVs. If 5 or more LCVs are detected within a 15 character window the character alignment state machine transitions to out-of-character-alignment state. The special characters listed in Table 21 and Table 22 are ignored for LCV purposes. Upon return to in-character-alignment state the LCV count is cleared.

**Figure 8 Character Alignment State Machine**



#### 10.15.4 Frame Alignment

Frame alignment locates SBI or TelecomBus frame and multi-frame boundaries in the incoming 8B/10B data stream. The frame alignment state machine may be in one of two states, in-frame-alignment state and out-of-frame-alignment state. Each SBI336S frame is 125uS in duration.

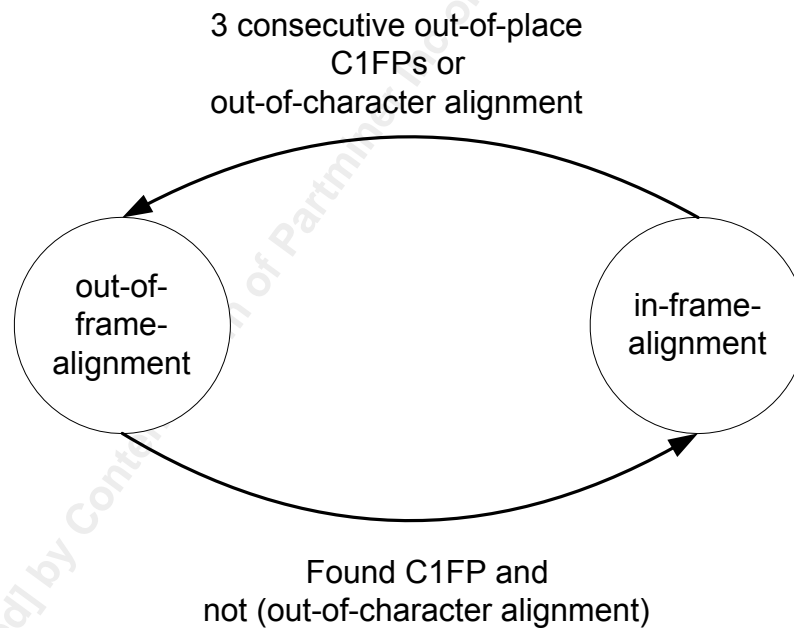
In SBI mode: Encoded over the SBI336S frame alignment is SBI336S multi-frame alignment which is every four SBI336S frames or 500uS. When carrying DS0 traffic in synchronous mode, signaling multi-frame alignment is also necessary and is also encoded over SBI336S alignment. Signaling multi-frame alignment is every 24 frames for T1 links and every 16 frames for E1 links, therefore signaling multi-frame alignment covering both T1 and E1 multi-frame alignment is every 48 SBI336S frames or 6ms. Therefore C1FP characters are sent every four or every 48 frames.

In TelecomBus mode: Encoded over the serial link is the tributary multi-frame alignment which is every 4 frames or 500uS. Multi-frame alignment is required so that a downstream device can extract the T1 or E1 data from the tributary. The multi-frame information is preserved by only sending out C1FP characters every four frames.

The frame alignment state machine establishes frame alignment over the link and is based on the frame and not the multi-frame alignments. When the frame alignment state machine is in the out-of-frame-alignment state, it maintains the current alignment, while searching for a C1FP character. When it finds the C1FP character the state machine transitions to the in-frame-alignment state. While in the in-frame-alignment state the state machine monitors out-of-place C1FP characters. Out-of-place C1FP characters are identified by maintaining a frame counter based on the C1FP character. The counter is initialized by the C1FP character when in the out-of-character-alignment state, and is unaffected in the in-character-alignment state. If 3 consecutive C1FPs have been found that do not agree with the expected location as defined by the frame counter, the state will change to out-of-frame-alignment state.

The frame alignment state machine is also sensitive to character alignment. When the character alignment state machine is in the out-of-character-alignment state, the frame alignment state machine is forced out-of-alignment, and is held in that state until the character alignment state machine transitions to the in-character alignment state.

**Figure 9 Frame Alignment State Machine**



### 10.15.5 SBI336S Multi-Frame Alignment

SBI336S multi-frame alignment is communicated across the link by controlling the frequency of the C1FP character. The most frequent transmission of the C1FP character is every four SBI336S frame times. This is the SBI336S multi-frame and is used when there are no synchronous tributaries requiring signaling multi-frame alignment on the SBI336S bus. When there are synchronous tributaries on the SBI336S bus the C1FP character is transmitted every 48 frame times. This is the CAS signaling multi-frame and is the lowest common multiple of the 24 frame T1 multi-frame and the 16 frame E1 multi-frame.

The SBI336S multi-frame and signaling multi-frame alignment is based a free running multi-frame counter that is reset with each C1FP character received. Under normal operating conditions each received C1FP character will coincide with the free running multi-frame counter. SBI336S multi-frame alignment is always required, SBI336S signaling multi-frame alignment is optional and only required when synchronous tributaries are supported with DS0 level switching.

### 10.16 Outgoing SBI336S Tributary Translator

The Outgoing SBI Tributary Translator block, OSTT, processes all timing information and Channel Associated Signaling information for the tributaries on the outgoing SBI Bus or buses. Input to this block is a 77MHz SBI stream with all tributaries encoded in an internal format that closely resembles the serial SBI format.

This block is transparent in TelecomBus mode.

#### 10.16.1 Outgoing SBI336S Translation

This block translates the generic internal SBI format to the external SBI format. A control RAM keeps the current configuration of the outgoing SBI bus(es) and the tributaries carried so that it can perform the translation function.

Common to all tributaries is identification of the first C1 byte. There are unique mappings of the 8B/10B codes for the supported SBI bus link types: Asynchronous T1/E1, Synchronous (locked) T1/E1, Transparent VT1.5/VT2, DS3/E3 and Fractional rate links. Much of the identification and mapping of a link from serial SBI format is based on the OC1FP frame pulse and a tributaries location relative to that C1 reference. In addition to the OC1FP identification this block identifies multi-frame alignment, valid payload, pointer movements for floating tributaries and timing control for decoding from the 8B/10B serial SBI format.

### 10.17 Outgoing SBI336 Timing Adapter

The Outgoing SBI336 Timing Adapter, OSTA, generates parity on the outgoing 77.76MHz SBI336 or TelecomBus. Parity can be configured to be either even or odd. In SBI336 mode, the parity calculation encompasses the ODATA[7:0], OPL and OV5 signals. In 77.76MHz TelecomBus mode, the parity calculation encompasses the ODATA[7:0] signals and optionally the OC1FP and OPL signals.



## 10.18 In-band Link Controller

In order to permit centralized control of distributed NSE/SBSLITE fabrics from the NSE microprocessor interface (for applications in which NSEs are located on fabric cards, and SBSLITEs are located on multiple line cards), an in-band signaling channel is provided between the NSE and the SBSLITE over the Serial interface. Each NSE can control up to 32 SBSLITEs which are attached by the LVDS links. The NSE/SBSLITE in-band channel is full duplex, but the NSE has active control of the link.

The SBSLITE contains two independent In-Band Link Controllers. One ILC is connected to the Working Transmit Serial LVDS Link and the other is connected to the Protection Transmit Serial LVDS Link.

The in-band channel is carried in the first 36 columns of four rows of the SBI or TelecomBus structure, rows 3, 6, 7 and 8. The overall in-band channel capacity is thus  $36 \times 4 \times 64 \text{ kb/s} = 9.216 \text{ Mb/s}$ . Each 36 bytes per row allocated to the in-band signaling channel is its own in-band message between the end points. Four bytes of each 36 byte in-band message are reserved for end-to-end control information and error protection, leaving  $8.192 \text{ Mb/s}$  available for user data transfer between the end points.

The data transferred between the end points has no fixed format, effectively providing a clear channel for packet transfer between the attached microprocessors at each of the LVDS link terminating devices. Using the microprocessor interface, the user is able to send and receive any packet up to 32 bytes in length. The first two bytes of each 36 byte message contains a header and the last two bytes of the message is a CRC-16 which detects errors in the message.

This in-band channel is expected to be used almost entirely to carry out switching control changes in the SBSLITEs. To configure a DS0 in an SBSLITE device most often requires a local microprocessor to write to one memory location consisting of a 16-bit address and a 16-bit data. Using this as a baseline and assuming an efficient use of the in-band channel bandwidth we can set a maximum of  $(32 \text{ bytes/row} \times 4 \text{ rows/frame} \times 8000 \text{ frames/sec} / 4 \text{ bytes/write})$  256,000 DS0 configurations per second.

Considering that configuring a T1 when switching DS0s requires 27 DS0 writes indicates that the in-band signaling channel bandwidth sets maximum limit of over 9000 T1 configurations per second. In real life these limits will not be achieved but this shows that the in-band link should not be the bottleneck. In TelecomBus mode this same configuration will require only 3 writes per T1 link.

In N+1 protected architectures it is likely that full configuration of a port card will be necessary during the switchover. This would require the entire connection memory be reconfigured. Assuming connections for overhead bytes are also reconfigured, the fastest that a complete reconfiguration can take place is  $9720 \text{ register writes}$  which equates to  $(9720 \text{ writes} \times 4 \text{ bytes/write} / (32 \text{ bytes/row} \times 4 \text{ rows/frame} \times 8000 \text{ frames/second}))$  38 milliseconds. It is also possible that the spare card could hold all the connection configurations for all the port cards it is protecting locally, for even faster switch over.

### 10.18.1 In-Band Signaling Channel Fixed Overhead

The In-Band Link Controller block generates and terminates two bytes of fixed header and a CRC-16 per every 36 byte in-band message. The two byte header provides control and status between devices at the ends of the LVDS link. The CRC-16 is calculated over the entire 34 byte in-band message and provides the terminating end the ability to detect errors in the in-band message. The format of the in-band message and header bytes is shown in Figure 10 and Figure 11.

**Figure 10 In-Band Signaling Channel Message Format**

1 byte	1 byte	32 bytes	2 bytes
Header1	Header2	Free Format Information	CRC-16

**Figure 11 In-Band Signaling Channel Header Format**

Header1							
Bit 7	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	Bit 0
Valid	Link[1:0]		Page[1:0]		User[2:0]		

Header2							
Bit 7	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	Bit 0
Aux[7:0]							

**Table 23 In-band Message Header Fields**

Field Name	Received by SBSLITE	Transmitted by SBSLITE
Valid	Message slot contains a valid message(1) or is empty(0). If empty this message will not be put into Rx Message FIFO (other header information processed as usual)	Message slot contains a valid message(1) or is empty(0). The header and CRC bytes are transmitted regardless of the state of this bit.
Link[1:0]#	Each bit indicates which Link to use, working(0) or Protect(1). Other algorithms are possible in indicate Working or Protect over these 2 bits.	Each bit shows current Link in use, working(0) or Protect(1). Other algorithms are possible in indicate Working or Protect over these 2 bits.  These bits are transmitted immediately.
Page[1:0]#	Each bit indicates which configuration page to use, page (1) or page (0) for the corresponding MSU. Page[1] controls the IMSU configuration page and Page[0] controls the OMSU configuration page.	Each bit shows current control page in use, page (1) or page (0) for the corresponding MSU. Page[1] indicates the IMSU configuration page and Page[0] indicates the OMSU configuration page  Only transmitted from the beginning of the first message of the frame
User[2:0]#	User defined bits which may be read through the microprocessor interface. User[2] is also output from the SBSLITE on the OUSER2 pin.	User defined bits. User[2] is sourced from the IUSER2 input to the SBSLITE. User[1:0] are sourced from an internal register.

Field Name	Received by SBSLITE	Transmitted by SBSLITE
		Transmitted immediately.
Aux[7:0]#	User defined auxiliary register indication.	User defined auxiliary register indication. Transmitted immediately.

#Change in these bits(received side) will not be processed if the received message CRC-16 indicates an error.

Interrupts can be generated when CRC errors are detected or the USER or LINK bits change state. There is no inherent flow control provided by the In-Band Link Controller. The attached microprocessor is able to provide flow control via interrupts when the in-band message FIFO overflows and via the USER bits in the header.

As each message arrives, the CRC-16 and valid bit is checked; if the valid bit is not set the message is discarded, if it fails the CRC check it is flagged as being in error and an interrupt is generated if enabled. If the CRC-16 is OK, regardless of the valid bit, the Page Link, User and Aux bits are passed on immediately. If the FIFO erroneously overflows, an interrupt is generated.

## 10.19 Microprocessor Interface

The Microprocessor Interface block provides normal and test mode registers, and logic required to connect to the microprocessor interface. The normal mode registers are required for normal operation, and test mode registers are used to enhance testability of the SBSLITE.

Address	Register
000H	SBSLITE Master Reset
001H	SBSLITE Master Configuration
002H	SBSLITE Revision/Part Number
003H	SBSLITE Part Number/Manufacturer ID
004H	SBSLITE Master Bypass
005H	SBSLITE Incoming SPE Control #1
006H	SBSLITE Incoming SPE Control #2
007H	SBSLITE Receive Synchronization Delay
008H	SBSLITE In-Band Link User Bits
009H – 00FH	SBSLITE Reserved
010H	SBSLITE Master Interrupt Source
011H	SBSLITE Interrupt Register
012H	SBSLITE Interrupt Enable Register
013H	SBSLITE Loop back Configuration
014H	SBSLITE Master Clock Monitor #1, Accumulation Trigger
015H	SBSLITE Master Clock Monitor #2
016H	SBSLITE Master Interrupt Enable Register
017H	SBSLITE Free User Register

Address	Register
018H	SBSLITE Outgoing SPE Control #1
019H	SBSLITE Outgoing SPE Control #2
01AH	SBSLITE Transmit SPE Control
01BH	SBSLITE Receive SPE Control
01CH – 01FH	Reserved
020H	ISTA Incoming Parity Configuration
021H	ISTA Incoming Parity Status
022H	ISTA TelecomBus Configuration
023H	ISTA Reserved
024H – 027H	Reserved
028H	IMSU Configuration
029H	IMSU Interrupt Status and Memory Page Update
02AH	IMSU Indirect Time Switch Address
02BH	IMSU Indirect Time Switch Data
02CH – 02FH	Reserved
030H	ICASM CAS Enable Indirect Address
031H	ICASM CAS Enable Indirect Control
032H	ICASM CAS Enable Indirect Data
033H	ICASM Reserved
034H – 037H	Reserved
038H	ISTT Control RAM Indirect Access Address Register
039H	ISTT Control RAM Indirect Access Control Register
03AH	ISTT Control RAM Indirect Access Data Register
03BH	ISTT Reserved
03CH – 03FH	Reserved
040H	OSTT Control RAM Indirect Access Address Register
041H	OSTT Control RAM Indirect Access Control Register
042H	OSTT Control RAM Indirect Access Data Register
043H	OSTT Reserved
044H – 047H	Reserved
048H	OMSU Configuration
049H	OMSU Interrupt Status and Memory Page Update
04AH	OMSU Indirect Time Switch Address
04BH	OMSU Indirect Time Switch Data
04CH – 04FH	Reserved
050H	OCASM Indirect Address
051H	OCASM Indirect Control
052H	OCASM Indirect Data
053H	OCASM Reserved
054H – 05FH	Reserved

Address	Register
060H	OSTA Outgoing Configuration and Parity
061H	OSTA Outgoing J1 Configuration
062H	OSTA Outgoing V1 Configuration
063H	OSTA H1-H2 Pointer Value
064H	OSTA Alternate H1-H2 Pointer Value
065H	OSTA H1-H2 Pointer Selection
066H – 06FH	OSTA Reserved
070H	WPP Indirect Address
071H	WPP Indirect Data
072H	WPP Generator Payload Configuration
073H	WPP Monitor Payload Configuration
074H	WPP Monitor Byte Error Interrupt Status
075H	WPP Monitor Byte Error Interrupt Enable
076H – 078H	WPP Reserved
079H	WPP Monitor Synchronization Interrupt Status
07AH	WPP Monitor Synchronization Interrupt Enable
07BH	WPP Monitor Synchronization State
07CH	WPP Performance Counters Transfer Trigger
07DH – 07FH	WPP Reserved
080H	PPP Indirect Address
081H	PPP Indirect Data
082H	PPP Generator Payload Configuration
083H	PPP Monitor Payload Configuration
084H	PPP Monitor Byte Error Interrupt Status
085H	PPP Monitor Byte Error Interrupt Enable
086H – 088H	Reserved
089H	PPP Monitor Synchronization Interrupt Status
08AH	PPP Monitor Synchronization Interrupt Enable
08BH	PPP Monitor Synchronization State
08CH	PPP Performance Counters Transfer Trigger
08DH – 08FH	PPP Reserved
090H	WILC Transmit Message FIFO Data High
091H	WILC Transmit Message FIFO Data Low
092H	WILC Reserved
093H	WILC Transmit Control
094H	WILC Reserved
095H	WILC Transmit Status and FIFO Synch
096H	WILC Receive Message FIFO Data High
097H	WILC Receive Message FIFO Data Low
098H	WILC Reserved

Address	Register
099H	WILC Receive Control
09AH	WILC Receive Auxiliary
09BH	WILC Receive Status and FIFO Synch
09CH	WILC Reserved
09DH	WILC Interrupt Enable and Control
09EH	WILC Reserved
09FH	WILC Interrupt Reason
0A0H	PILC Transmit Message FIFO Data High
0A1H	PILC Transmit Message FIFO Data Low
0A2H	PILC Reserved
0A3H	PILC Transmit Control
0A4H	PILC Reserved
0A5H	PILC Transmit Status and FIFO Synch
0A6H	PILC Receive Message FIFO Data High
0A7H	PILC Receive Message FIFO Data Low
0A8H	PILC Reserved
0A9H	PILC Receive Control
0AAH	PILC Receive Auxiliary
0ABH	PILC Receive Status and FIFO Synch
0ACH	PILC Reserved
0ADH	PILC Interrupt Enable and Control
0AEH	PILC Reserved
0AFH	PILC Interrupt Reason
0B0H	TW8E Control and Status
0B1H	TW8E Interrupt Status
0B2H	TW8E Time-slot Configuration #1
0B3H	TW8E Time-slot Configuration #2
0B4H	TW8E Test Pattern
0B5H	TW8E Analog Control
0B6H – 0B7H	TW8E Reserved
0B8H	TP8E Control and Status
0B9H	TP8E Interrupt Status
0BAH	TP8E Time-slot Configuration #1
0BBH	TP8E Time-slot Configuration #2
0BCH	TP8E Test Pattern
0BDH	TP8E Analog Control
0BEH – 0BFH	TP8E Reserved
0C0H	RW8D Control and Status
0C1H	RW8D Interrupt Status
0C2H	RW8D Line Code Violation Count

Address	Register
0C3H	RW8D Analog Control #1
0C4H – 0C7H	RW8D Reserved
0C8H	RP8D Control and Status
0C9H	RP8D Interrupt Status
0CAH	RP8D Line Code Violation Count
0CBH	RP8D Analog Control
0CCH – 0CFH	RP8D Reserved
0D0H	CSTR Control
0D1H	CSTR Interrupt Enable and Status
0D2H	CSTR Interrupt Indication
0D3H	CSTR Reserved
0D4H – 0DFH	Reserved
0E0H	REFDLL Configuration
0E1H	REFDLL Reserved
0E2H	REFDLL Reset
0E3H	REFDLL Control Status
0E4H – 0E7H	Reserved
0E8H	SYSDLL Configuration
0E9H	SYSDLL Reserved
0EAH	SYSDLL Reset
0EBH	SYSDLL Control Status
0ECH – 0FFH	Reserved
100H	SBSLITE Master Test
101H – 1FFH	Reserved for Test

For all register accesses, CSB must be set low.

## 11 Normal Mode Register Description

Normal mode registers are used to configure and monitor the operation of the SBSLITE. Normal mode registers (as opposed to test mode registers) are selected when A[8] is set low.

### Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of this product, unused register bits must be written with logic 0. Reading back unused bits can produce either a logic 1 or a logic 0; hence, unused register bits should be masked off by software when read.
2. All configuration bits that can be written into can also be read back. This allows the processor controlling the SBSLITE to determine the programming state of the block.
3. Writeable normal mode register bits are cleared to logic 0 upon reset unless otherwise noted.
4. Writing into read-only normal mode register bit locations does not affect SBSLITE operation unless otherwise noted.



**Register 000H: SBSLITE Master Reset**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7		Unused	0
Bit 6		Unused	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	ARESET	0
Bit 0	R/W	DRESET	0

**Reserved**

These bits must be set low for proper operation of the SBSLITE.

**ARESET**

The analogue reset bit (ARESET) allows the analogue circuitry in the SBSLITE to be reset and disabled under software control. When the ARESET bit is set high, all SBSLITE analogue circuitry is held in reset and disabled. This bit is not self-clearing. Therefore, it must be set low to bring the affected circuitry out of reset and enable it. Holding SBSLITE in analogue reset state places it into a low power, disabled mode. A hardware reset clears the ARESET bit, thus negating the analogue software reset.

This bit must be set for a minimum of 1ms after a hardware reset to properly reset the CSU. Alternatively, the hardware reset, RSTB, must be held low for a minimum of 1ms.

**DRESET**

The digital reset bit (DRESET) allows the digital circuitry in the SBSLITE to be reset under software control. When the DRESET bit is set high, all SBSLITE digital circuitry is held in reset with the exception of this register. This bit is not self-clearing. Therefore, it must be set low to bring the affected circuitry out of reset. Holding SBSLITE in digital reset state places it into a low power, digital stand-by mode. A hardware reset clears the DRESET bit, thus negating the digital software reset.

**Register 001H: SBSLITE Master Configuration**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14	R/W	ICMP_SRC[1]	0
Bit 13	R/W	ICMP_SRC[0]	0
Bit 12	R/W	ICMP_VAL	0
Bit 11		Unused	0
Bit 10	R/W	OCMP_SRC[1]	0
Bit 9	R/W	OCMP_SRC[0]	0
Bit 8	R/W	OCMP_VAL	0
Bit 7	R/W	RWSEL_SRC	0
Bit 6	R/W	RWSEL_VAL	1
Bit 5	R/W	Reserved[1]	0
Bit 4	R/W	COLUMN_MODE	0
Bit 3	R/W	PHY_SBI	1
Bit 2	R/W	MF_48	0
Bit 1	R/W	TELECOM_BUS	0
Bit 0	R/W	Reserved[0]	0

**ICMP\_SRC[1:0]**

The ICMP\_SRC[1:0] bits select the source for the incoming connection memory page information.

ICMP_SRC[1:0]	Source
00	ICMP_VAL register bit
01	ICMP input pin
10	PAGE bit from the active ILC (as determined by the RWSEL_VAL bit or RWSEL input)
11	Reserved

**ICMP\_VAL**

The ICMP\_VAL bit controls the selection of the connection memory page in each Incoming Memory Switch Unit, IMSU. When ICMP\_VAL is a logic 1, connection memory page 1 is selected. When ICMP\_VAL is a logic 0, connection memory page 0 is selected.

ICMP\_VAL is sampled at the C1 byte position as defined by the incoming frame pulse signal (IC1FP). Changes to the connection memory page selection are synchronized to the frame boundary of the next frame (in TelecomBus mode), 4 frame multi-frame (in SBI mode without CAS), or 48 frame multi-frame (in SBI mode with CAS). This bit is only used when ICMP\_SRC[1:0] = 'b00.

### OCMP\_SRC[1:0]

The OCMP\_SRC[1:0] bits select the source for the outgoing connection memory page information.

OCMP_SRC[1:0]	Source
00	OCMP_VAL register bit
01	OCMP input pin
10	PAGE bit from the active ILC (as determined by the RWSEL_VAL bit or RWSEL input)
11	Reserved

### OCMP\_VAL

The OCMP\_VAL bit controls the selection of the connection memory page in each Outgoing Memory Switch Unit, OMSU. When OCMP\_VAL is a logic 1, connection memory page 1 is selected. When OCMP\_VAL is a logic 0, connection memory page 0 is selected. OCMP\_VAL is sampled at the C1 byte position as defined by the receive frame pulse signal (RC1FP). Changes to the connection memory page selection are synchronized to the frame boundary of the next frame (in TelecomBus mode), 4 frame multi-frame (in SBI mode without CAS), or 48 frame multi-frame (in SBI mode with CAS). This bit is only used when OCMP\_SRC[1:0] = 'b00.

### RWSEL\_SRC

The RWSEL\_SRC bit selects the source for the selection of which link, the working or the protect, is active. When RWSEL\_SRC is a logic 0, the RWSEL\_VAL register bit is used as the source for selecting the active link. When RWSEL\_SRC is a logic 1, the RWSEL input is used as the source for selecting the active link.

### RWSEL\_VAL

The RWSEL\_VAL bit selects between the receive working and protect links when the RWSEL\_SRC is a logic 0. When RWSEL\_VAL is a logic 1, the working link is selected and the SBSLITE listens to the data from the RPWRK and RNWRK inputs. When RWSEL\_VAL is a logic 0, the protect link is selected and the SBSLITE listens to the data from the RPPROT and RNPROT inputs. This bit has no effect when the RWSEL\_SRC bit is a logic 1 or when the parallel interface is used (PARALLEL\_MODE = 'b1).

### Reserved[1]

This bit must be set to a logic 0 for correct operation of the SBSLITE.

## COLUMN\_MODE

The COLUMN\_MODE bit selects between column switching and DS0 switching. When COLUMN\_MODE is set to a logic 1, column switching is enabled and the SBSLITE is configured to switch columns within the SBI336 or TelecomBus. When COLUMN\_MODE is set to a logic 0, DS0 switching is enabled and the SBSLITE is configured to switch DS0's within the SBI336 bus. DS0 switching is not permitted in TelecomBus mode.

## PHY\_SBI

The PHY\_SBI bit configures the direction of the JUST\_REQ input/output signals on the incoming and outgoing buses. When PHY\_SBI is set to a logic 1, the SBSLITE is configured to be connected to a PHY device and the JUST\_REQ signal is an input. When PHY\_SBI is set to a logic 0, the SBSLITE is configured to be connected to a Link layer device and the JUST\_REQ signal is an output.

## MF\_48

The MF\_48 bit selects between 4 frame multi-frame mode or 48 frame multi-frame mode on the SBI336 bus. When MF\_48 is a logic 1, 48 frame mode is selected. IC1FP is expected once every 48 frames and OC1FP is output every 48 frames, indicating CAS signaling multi-frame alignment. When MF\_48 is a logic 0, 4 frame mode is selected. IC1FP is expected once every 4 frames and OC1FP is output every 4 frames. This bit has no effect when in TelecomBus mode (TELECOM\_BUS = 'b1) or when in column switching mode (COLUMN\_MODE = 'b1).

## TELECOM\_BUS

The TELECOM\_BUS bit selects between TelecomBus and SBI bus modes on the incoming and outgoing buses. When TELECOM\_BUS is set to a logic 1, TelecomBus mode is selected and all frame pulses must mark C1J1V1 positions. When TELECOM\_BUS is set to a logic 0, SBI bus mode is selected and the all frame pulses only mark the C1 position.

## Reserved[0]

This bit must be set to a logic 1 for proper operation of the SBSLITE.

**Note:** Whenever this bit is changed from a logic 0 to a logic 1, the REFDLL must be reset by writing to register 0E2H.

**Register 002H: SBSLITE Version/Part Number**

Bit	Type	Function	Default
Bit 15	R	VERSION[3]	0
Bit 14	R	VERSION[2]	0
Bit 13	R	VERSION[1]	0
Bit 12	R	VERSION[0]	1
Bit 11	R	PART_NUMBER[15]	1
Bit 10	R	PART_NUMBER[14]	0
Bit 9	R	PART_NUMBER[13]	0
Bit 8	R	PART_NUMBER[12]	0
Bit 7	R	PART_NUMBER[11]	0
Bit 6	R	PART_NUMBER[10]	1
Bit 5	R	PART_NUMBER[9]	1
Bit 4	R	PART_NUMBER[8]	0
Bit 3	R	PART_NUMBER[7]	0
Bit 2	R	PART_NUMBER[6]	0
Bit 1	R	PART_NUMBER[5]	0
Bit 0	R	PART_NUMBER[4]	1

**VERSION[3:0]**

The VERSION[3:0] bits report the binary revision number of the SBSLITE silicon.  
VERSION[3:0] = 'b0001 for revision B of the SBSLITE.

**PART\_NUMBER[15:4]**

The PART NUMBER[15:4] bits represent the 12 most significant bits of the part number of the SBSLITE device.

**Register 003H: SBSLITE Part Number/Manufacturer ID**

Bit	Type	Function	Default
Bit 15	R	PART_NUMBER[3]	0
Bit 14	R	PART_NUMBER[2]	0
Bit 13	R	PART_NUMBER[1]	0
Bit 12	R	PART_NUMBER[0]	1
Bit 11	R	MANUFACTURER_ID[10]	0
Bit 10	R	MANUFACTURER_ID[9]	0
Bit 9	R	MANUFACTURER_ID[8]	0
Bit 8	R	MANUFACTURER_ID[7]	0
Bit 7	R	MANUFACTURER_ID[6]	1
Bit 6	R	MANUFACTURER_ID[5]	1
Bit 5	R	MANUFACTURER_ID[4]	0
Bit 4	R	MANUFACTURER_ID[3]	0
Bit 3	R	MANUFACTURER_ID[2]	1
Bit 2	R	MANUFACTURER_ID[1]	1
Bit 1	R	MANUFACTURER_ID[0]	0
Bit 0	R	JID	1

**PART\_NUMBER[3:0]**

The PART\_NUMBER[3:0] bits represent the 4 least significant bits of the part number of the SBSLITE device.

**MANUFACTURER\_ID[10:0]**

The MANUFACTURER\_ID[10:0] bits represent the 11 bit manufacturer's code assigned to PMC-Sierra, Inc. for inclusion in the JTAG Boundary Scan Identification Code. For more information on JTAG Boundary Scan, refer to Section 12.

**JID**

The JID bit is bit 0 in the JTAG identification code.

**Register 004H: SBSLITE Master Bypass Register**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7		Unused	0
Bit 6		Unused	0
Bit 5	R/W	IMSU_BYPASS	0
Bit 4	R/W	ICASE_BYPASS	0
Bit 3	R/W	ICASM_BYPASS	0
Bit 2	R/W	OMSU_BYPASS	0
Bit 1	R/W	OCASE_BYPASS	0
Bit 0	R/W	OCASM_BYPASS	0

**IMSU\_BYPASS**

The IMSU\_BYPASS bit is used to bypass the functionality of the IMSU block. When IMSU\_BYPASS is a logic 1, the incoming memory switch is bypassed and the incoming data bus is passed to the transmit data bus unmodified. This eliminates the one frame delay through the IMSU and places the IMSU in a low power mode. When IMSU\_BYPASS is a logic 0, the IMSU is not bypassed and must be configured.

**ICASE\_BYPASS**

The ICASE\_BYPASS bit is used to bypass the functionality of the ICASE block. When ICASE\_BYPASS is a logic 1, the incoming CAS extractor is bypassed and the CAS bits are not extracted from the SBI336 bus. This places the ICASE block in a low power mode. When ICASE\_BYPASS is a logic 0, the ICASE is not bypassed and the CAS bits are extracted from the SBI336 bus.

**ICASM\_BYPASS**

The ICASM\_BYPASS bit is used to bypass the functionality of the ICASM block. When ICASM\_BYPASS is a logic 1, the incoming CAS merge block is bypassed and the CAS bits are not inserted into the SBI336 bus. This places the ICASM block in a low power mode. When ICASM\_BYPASS is a logic 0, the ICASM is not bypassed and the CAS bits are inserted into the SBI336 bus.

### OMSU\_BYPASS

The OMSU\_BYPASS bit is used to bypass the functionality of the OMSU block. When OMSU\_BYPASS is a logic 1, the outgoing memory switch is bypassed and the receive data bus is passed to the outgoing data bus unmodified. This eliminates the one frame delay through the OMSU and places the OMSU in a low power mode. When OMSU\_BYPASS is a logic 0, the OMSU is not bypassed and must be configured.

### OCASE\_BYPASS

The OCASE\_BYPASS bit is used to bypass the functionality of the OCASE block. When OCASE\_BYPASS is a logic 1, the transmit CAS extractor is bypassed and the CAS bits are not extracted from the SBI336 bus. This places the OCASE block in a low power mode. When OCASE\_BYPASS is a logic 0, the OCASE is not bypassed and the CAS bits are extracted from the SBI336 bus.

### OCASM\_BYPASS

The OCASM\_BYPASS bit is used to bypass the functionality of the OCASM block. When OCASM\_BYPASS is a logic 1, the transmit CAS merge block is bypassed and the CAS bits are not inserted into the SBI336 bus. This places the OCASM block in a low power mode. When OCASM\_BYPASS is a logic 0, the OCASM is not bypassed and the CAS bits are inserted into the SBI336 bus.



**Register 005H: SBSLITE Incoming SPE Control #1**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7	R/W	ISBI4_SPE3_TYP[1] / ISTS1_TYP[12]	0
Bit 6	R/W	ISBI4_SPE3_TYP[0]	0
Bit 5	R/W	ISBI3_SPE3_TYP[1] / ISTS1_TYP[11]	0
Bit 4	R/W	ISBI3_SPE3_TYP[0]	0
Bit 3	R/W	ISBI2_SPE3_TYP[1] / ISTS1_TYP[10]	0
Bit 2	R/W	ISBI2_SPE3_TYP[0]	0
Bit 1	R/W	ISBI1_SPE3_TYP[1] / ISTS1_TYP[9]	0
Bit 0	R/W	ISBI1_SPE3_TYP[0]	0

**Register 006H: SBSLITE Incoming SPE Control #2**

Bit	Type	Function	Default
Bit 15	R/W	ISBI4_SPE2_TYP[1] / ISTS1_TYP[8]	0
Bit 14	R/W	ISBI4_SPE2_TYP[0]	0
Bit 13	R/W	ISBI3_SPE2_TYP[1] / ISTS1_TYP[7]	0
Bit 12	R/W	ISBI3_SPE2_TYP[0]	0
Bit 11	R/W	ISBI2_SPE2_TYP[1] / ISTS1_TYP[6]	0
Bit 10	R/W	ISBI2_SPE2_TYP[0]	0
Bit 9	R/W	ISBI1_SPE2_TYP[1] / ISTS1_TYP[5]	0
Bit 8	R/W	ISBI1_SPE2_TYP[0]	0
Bit 7	R/W	ISBI4_SPE1_TYP[1] / ISTS1_TYP[4]	0
Bit 6	R/W	ISBI4_SPE1_TYP[0]	0
Bit 5	R/W	ISBI3_SPE1_TYP[1] / ISTS1_TYP[3]	0
Bit 4	R/W	ISBI3_SPE1_TYP[0]	0
Bit 3	R/W	ISBI2_SPE1_TYP[1] / ISTS1_TYP[2]	0
Bit 2	R/W	ISBI2_SPE1_TYP[0]	0
Bit 1	R/W	ISBI1_SPE1_TYP[1] / ISTS1_TYP[1]	0
Bit 0	R/W	ISBI1_SPE1_TYP[0]	0

**ISBIx\_SPEy\_TYP[1:0] (SBI mode only)**

In SBI mode (TELECOM\_BUS = 'b0), the ISBIx\_SPEy\_TYP[1:0] bits select the SPE type for the specified SPE within the specified Incoming SBI bus. The types for each SPE are independently configured with possible types being T1, E1, DS3/E3 and fractional rate links. In TelecomBus mode (TELECOM\_BUS = 'b1), the ISBIx\_SPEy\_TYP[0] bits are unused.

The setting for ISBIx\_SPEy\_TYP[1:0] are:

SBIx_SPEy_TYP[1:0]	Payload Type
00	T1
01	E1
10	DS3/E3
11	Fractional Rate

**ISTS1\_TYP[12:1] (TelecomBus mode only)**

In TelecomBus mode (TELECOM\_BUS = 'b1), the ISTS1\_TYP[12:1] bits select between floating and fixed STS/AUs on the Incoming bus. When ISTS1\_TYP[x] is a logic 1, the associated STS/AU is floating and may have high order pointer movements. When ISTS1\_TYP[x] is a logic 0, the associated STS/AU is fixed and cannot have high order pointer movements.

**Register 007H: SBSLITE Receive Synchronization Delay**

Bit	Type	Function	Default
Bit 15	R	TIP	0
Bit 14		Unused	0
Bit 13	R/W	RC1FPDLY[13]	0
Bit 12	R/W	RC1FPDLY[12]	0
Bit 11	R/W	RC1FPDLY[11]	0
Bit 10	R/W	RC1FPDLY[10]	0
Bit 9	R/W	RC1FPDLY[9]	0
Bit 8	R/W	RC1FPDLY[8]	0
Bit 7	R/W	RC1FPDLY[7]	0
Bit 6	R/W	RC1FPDLY[6]	0
Bit 5	R/W	RC1FPDLY[5]	0
Bit 4	R/W	RC1FPDLY[4]	0
Bit 3	R/W	RC1FPDLY[3]	0
Bit 2	R/W	RC1FPDLY[2]	0
Bit 1	R/W	RC1FPDLY[1]	0
Bit 0	R/W	RC1FPDLY[0]	0

**TIP**

The transfer in progress bit (TIP) reports the status of latching performance monitor counting into holding registers. TIP is set high when a transfer is initiated by a write access to the SBSLITE Master Signal Monitor #1, Accumulation Trigger Register (014H). It is set low when all the counters in the SBSLITE have transferred their values to holding registers. The updated counts are now available for reading at the designated registers. These registers are the WPP Monitor Error Count (Register 071H with IADDR = 4H), the PPP Monitor Error Count (Register 081H with IADDR = 4H), the RW8D LCV Count (Register 0C2H), and the RP8D LCV Count (Register 0CAH).

**RC1FPDLY[13:0]**

The receive transport frame delay bits (RC1FPDLY[13:0]) controls the delay, in SYSCLK cycles, inserted by the SBSLITE before processing the C1 characters delivered by the receive serial data links. RC1FPDLY should be set such that after the specified delay the active receive link should have delivered the C1 character. The relationships between RC1FP, RC1FPDLY and the receive serial links is described in the Functional Timing section.

**Register 008H: SBSLITE In-Bank Link User Bits**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7		Unused	0
Bit 6		Unused	0
Bit 5		Unused	0
Bit 4		Unused	0
Bit 3	R/W	TXWUSER[1]	0
Bit 2	R/W	TXWUSER[0]	0
Bit 1	R/W	TXPUSER[1]	0
Bit 0	R/W	TXPUSER[0]	0

**TXWUSER[1:0]**

The Transmit Working USER bits (TXWUSER[1:0]) contain the values to be inserted in the USER[1:0] bits in the header of the working in-band signaling channel.

**TXPUSER[1:0]**

The Transmit Protection USER bits (TXWUSER[1:0]) contain the values to be inserted in the USER[1:0] bits in the header of the protection in-band signaling channel.

**Register 010H: SBSLITE Master Interrupt Source**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14	R	SBS_INT	X
Bit 13	R	IMSU_INT	X
Bit 12	R	OMSU_INT	X
Bit 11	R	REFDLL_INT	X
Bit 10	R	SYSDLL_INT	X
Bit 9	R	CSTR_INT	X
Bit 8	R	TW8E_INT	X
Bit 7	R	TP8E_INT	X
Bit 6	R	RW8D_INT	X
Bit 5	R	RP8D_INT	X
Bit 4	R	WPP_INT	X
Bit 3	R	PPP_INT	X
Bit 2	R	WILC_INT	X
Bit 1	R	PILC_INT	X
Bit 0	R	ISTA_INT	X

**SBS\_INT**

If the SBS\_INT bit is a logic 1, an interrupt has been generated by the top level circuitry. The SBSLITE Interrupt register must be read to clear this interrupt.

**IMSU\_INT**

If the IMSU\_INT bit is a logic 1, an interrupt has been generated by the IMSU block. The IMSU Interrupt register must be read to clear this interrupt.

**OMSU\_INT**

If the OMSU\_INT bit is a logic 1, an interrupt has been generated by the OMSU block. The OMSU Interrupt register must be read to clear this interrupt.

**REFDLL\_INT**

If the REFDLL\_INT bit is a logic 1, an interrupt has been generated by the REFDLL block. The REFDLL Interrupt register must be read to clear this interrupt.

#### SYSDLL\_INT

If the SYSDLL\_INT bit is a logic 1, an interrupt has been generated by the SYSDLL block. The SYSDLL Interrupt register must be read to clear this interrupt.

#### CSTR\_INT

If the CSTR\_INT bit is a logic 1, an interrupt has been generated by the CSTR block. The CSTR Interrupt register must be read to clear this interrupt.

#### TW8E\_INT

If the TW8E\_INT bit is a logic 1, an interrupt has been generated by the TW8E block. The TW8E Interrupt register must be read to clear this interrupt.

#### TPPP\_INT

If the TP8E\_INT bit is a logic 1, an interrupt has been generated by the TP8E block. The TP8E Interrupt register must be read to clear this interrupt.

#### RW8D\_INT

If the RW8D\_INT bit is a logic 1, an interrupt has been generated by the RW8D block. The RW8D Interrupt register must be read to clear this interrupt.

#### RP8D\_INT

If the RP8D\_INT bit is a logic 1, an interrupt has been generated by the RP8D block. The RP8D Interrupt register must be read to clear this interrupt.

#### WPP\_INT

If the WPP\_INT bit is a logic 1, an interrupt has been generated by the WPP block. The WPP Interrupt register must be read to clear this interrupt.

#### PPP\_INT

If the PPP\_INT bit is a logic 1, an interrupt has been generated by the PPP block. The PPP Interrupt register must be read to clear this interrupt.

#### WILC\_INT

If the WILC\_INT bit is a logic 1, an interrupt has been generated by the WILC block. The WILC Interrupt register must be read to clear this interrupt.

#### PILC\_INT

If the PILC\_INT bit is a logic 1, an interrupt has been generated by the PILC block. The PILC Interrupt register must be read to clear this interrupt.

#### ISTA\_INT

If the ISTA\_INT bit is a logic 1, an interrupt has been generated by the ISTA block. The ISTA Interrupt register must be read to clear this interrupt.

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**Register 011H: SBSLITE Interrupt Register**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12	R	WRC1_EXP_INT	X
Bit 11	R	WRC1_EXTRA_INT	X
Bit 10	R	WRC1_MISS_INT	X
Bit 9	R	PRC1_EXP_INT	X
Bit 8	R	PRC1_EXTRA_INT	X
Bit 7	R	PRC1_MISS_INT	X
Bit 6	R	ICMP_INT	X
Bit 5	R	OCMP_INT	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

**WRC1\_EXP\_INT**

The WRC1\_EXP\_INT bit is set to a logic 1 when a C1 character is received on the receive working serial link in its expected position with respect to the RC1FP input. This interrupt is enabled with the WRC1\_EXPE bit in the SBSLITE Interrupt Enable register. This interrupt bit will be cleared when read.

**WRC1\_EXTRA\_INT**

The WRC1\_EXTRA\_INT bit is set to a logic 1 when a C1 character is received on the receive working serial link in an unexpected position with respect to the RC1FP input. This interrupt is enabled with the WRC1\_EXTRAE bit in the SBSLITE Interrupt Enable register. This interrupt bit will be cleared when read.

**WRC1\_MISS\_INT**

The WRC1\_MISS\_INT bit is set to a logic 1 when a C1 character is not received on the receive working serial link in its expected position with respect to the RC1FP input. This interrupt is enabled with the WRC1\_MISSE bit in the SBSLITE Interrupt Enable register. This interrupt bit will be cleared when read.



#### PRC1\_EXP\_INT

The PRC1\_EXP\_INT bit is set to a logic 1 when a C1 character is received on the receive protection serial link in its expected position with respect to the RC1FP input. This interrupt is enabled with the PRC1\_EXPE bit in the SBSLITE Interrupt Enable register. This interrupt bit will be cleared when read.

#### PRC1\_EXTRA\_INT

The PRC1\_EXTRA\_INT bit is set to a logic 1 when a C1 character is received on the receive protection serial link in an unexpected position with respect to the RC1FP input. This interrupt is enabled with the PRC1\_EXTRAE bit in the SBSLITE Interrupt Enable register. This interrupt bit will be cleared when read.

#### PRC1\_MISS\_INT

The PRC1\_MISS\_INT bit is set to a logic 1 when a C1 character is not received on the receive protection serial link in its expected position with respect to the RC1FP input. This interrupt is enabled with the PRC1\_MISSE bit in the SBSLITE Interrupt Enable register. This interrupt bit will be cleared when read.

#### ICMP\_INT

The ICMP\_INT bit is set to a logic 1 when the ICMP input is sampled by the SBSLITE. In TelecomBus mode, ICMP is sampled during the first C1 position of every frame, as marked by IC1FP. In SBI mode, ICMP is sampled during the first C1 position of every 4 or 48 frame multi-frame, as marked by IC1FP. This interrupt may be helpful in scheduling configuration page changes in the IMSU. This interrupt is enabled with the ICMPE bit in the SBSLITE Interrupt Enable register. This interrupt bit will be cleared when read.

#### OCMP\_INT

The OCMP\_INT bit is set to a logic 1 when the OCMP input is sampled by the SBSLITE. In TelecomBus mode, OCMP is sampled during the first C1 position of every frame, as marked by RC1FP. In SBI mode, OCMP is sampled during the first C1 position of every 4 or 48 frame multi-frame, as marked by RC1FP. This interrupt may be helpful in scheduling configuration page changes in the OMSU. This interrupt is enabled with the OCMPE bit in the SBSLITE Interrupt Enable register. This interrupt bit will be cleared when read.

#### Reserved

The Reserved bits should be ignored when this register is read.

**Register 012H: SBSLITE Interrupt Enable Register**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12	R/W	WRC1_EXPE	0
Bit 11	R/W	WRC1_EXTRAE	0
Bit 10	R/W	WRC1_MISSE	0
Bit 9	R/W	PRC1_EXPE	0
Bit 8	R/W	PRC1_EXTRAE	0
Bit 7	R/W	PRC1_MISSE	0
Bit 6	R/W	ICMPE	0
Bit 5	R/W	OCMPE	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

**WRC1\_EXPE**

The WRC1\_EXPE interrupt enable bit is an active high interrupt enable. When WRC1\_EXPE is set to a logic 1, an interrupt will be asserted on the INTB output when the WRC1\_EXP\_INT bit in register 011H is set high and the SBSE and INTE bits in register 016H are set high. When WRC1\_EXPE is set to a logic 0, The WRC1\_EXP\_INT bit will not cause an interrupt.

**WRC1\_EXTRAE**

The WRC1\_EXTRAE interrupt enable bit is an active high interrupt enable. When WRC1\_EXTRAE is set to a logic 1, an interrupt will be asserted on the INTB output when the WRC1\_EXTRA\_INT bit in register 011H is set high and the SBSE and INTE bits in register 016H are set high. When WRC1\_EXTRAE is set to a logic 0, The WRC1\_EXTRA\_INT bit will not cause an interrupt.

**WRC1\_MISSE**

The WRC1\_MISSE interrupt enable bit is an active high interrupt enable. When WRC1\_MISSE is set to a logic 1, an interrupt will be asserted on the INTB output when the WRC1\_MISS\_INT bit in register 011H is set high and the SBSE and INTE bits in register 016H are set high. When WRC1\_MISSE is set to a logic 0, The WRC1\_MISS\_INT bit will not cause an interrupt.

#### PRC1\_EXPE

The PRC1\_EXPE interrupt enable bit is an active high interrupt enable. When PRC1\_EXPE is set to a logic 1, an interrupt will be asserted on the INTB output when the PRC1\_EXP\_INT bit in register 011H is set high and the SBSE and INTE bits in register 016H are set high. When PRC1\_EXPE is set to a logic 0, The PRC1\_EXP\_INT bit will not cause an interrupt.

#### PRC1\_EXTRAE

The PRC1\_EXTRAE interrupt enable bit is an active high interrupt enable. When PRC1\_EXTRAE is set to a logic 1, an interrupt will be asserted on the INTB output when the PRC1\_EXTRA\_INT bit in register 011H is set high and the SBSE and INTE bits in register 016H are set high. When PRC1\_EXTRAE is set to a logic 0, The PRC1\_EXTRA\_INT bit will not cause an interrupt.

#### PRC1\_MISSE

The PRC1\_MISSE interrupt enable bit is an active high interrupt enable. When PRC1\_MISSE is set to a logic 1, an interrupt will be asserted on the INTB output when the PRC1\_MISS\_INT bit in register 011H is set high and the SBSE and INTE bits in register 016H are set high. When PRC1\_MISSE is set to a logic 0, The PRC1\_MISS\_INT bit will not cause an interrupt.

#### ICMPE

The ICMPE interrupt enable bit is an active high interrupt enable. When ICMPE is set to a logic 1, an interrupt will be asserted on the INTB output when the ICMP\_INT bit in register 011H is set high and the SBSE and INTE bits in register 016H are set high. When ICMPE is set to a logic 0, The ICMP\_INT bit will not cause an interrupt.

#### OCMPE

The OCMPE interrupt enable bit (OCMPE) is an active high interrupt enable. When OCMPE is set to a logic 1, an interrupt will be asserted on the INTB output when the OCMP\_INT bit in register 011H is set high and the SBSE and INTE bits in register 016H are set high. When OCMPE is set to a logic 0, The OCMP\_INT bit will not cause an interrupt.

#### Reserved

The Reserved bits must be set to a logic 0.

**Register 013H: SBSLITE Loop Back Configuration**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7		Unused	0
Bit 6		Unused	0
Bit 5		Unused	0
Bit 4		Unused	0
Bit 3		Unused	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	T82R8LOOP	0
Bit 0	R/W	T2RLOOP	0

**Reserved**

The Reserved bit must be set to a logic 0.

**T82R8LOOP**

The T82R8LOOP bit enables a diagnostic loop back from the transmit 8b/10b encoded bus to the receive 8b/10b encoded bus. When T82R8LOOP is a logic 1, the entire SBI336 or TelecomBus is looped back from the output of the TW8E and TP8E to the input of the RW8D and RP8D, respectively. When T82R8LOOP is a logic 0, no loop back is performed.

**T2RLOOP**

The T2RLOOP bit enables a diagnostic loop back from the transmit interface to the receive interface. When T2RLOOP is a logic 1, the entire SBI336 or TelecomBus is looped back from the output of the ICASM to the input of the OCASE. When T2RLOOP is a logic 0, no loop back is performed.

**Register 014H: SBSLITE Master Signal Monitor #1, Accumulation Trigger**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	RC1FPA	X
Bit 5	R	SYSCLKA	X
Bit 4	R	SREFCLKA	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	IC1FPA	X

This register provides activity monitoring on major SBSLITE inputs. When a monitored input makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the bits in this register are cleared. Bits that depend on multiple inputs making a low to high transition must have each input make a low to high transition between subsequent reads before the activity bit will be set high. The corresponding register bit reading low indicates a lack of transitions. This register should be read periodically to detect for stuck at conditions.

Writing to this register delimits the accumulation intervals in the various performance monitor accumulation registers. These registers are the WPP Monitor Error Count (Register 071H with IADDR = 4H), the PPP Monitor Error Count (Register 081H with IADDR = 4H), the RW8D LCV Count (Register 0C2H), and the RP8D LCV Count (Register 0CAH). Counts accumulated in those registers are transferred to holding registers where they can be read. The counters themselves are then cleared to begin accumulating events for a new accumulation interval. To prevent loss of data, accumulation intervals must be 1.0 second or shorter. The bits in this register are not affected by write accesses.

**Reserved**

The Reserved bits should be ignored when this register is read.

**RC1FPA**

The RC1FP active bit (RC1FPA) detects low to high transitions on the RC1FP input. RC1FPA is set high on a rising edge of RC1FP, and is set low when this register is read.

#### SYSCCLKA

The SYSCCLK active bit (SYSCCLKA) detects low to high transitions on the SYSCCLK input. SYSCCLKA is set high on a rising edge of SYSCCLK, and is set low when this register is read.

#### SREFCLKA

The SREFCLK active bit (SREFCLKA) detects low to high transitions on the SREFCLK input. SREFCLKA is set high on a rising edge of SREFCLK, and is set low when this register is read.

#### IC1FPA

The IC1FP active bit (IC1FPA) detects low to high transitions on the IC1FP input. IC1FPA is set high on a rising edge of IC1FP, and is set low when this register is read.

**Register 015H: SBSLITE Master Signal Monitor #2**

Bit	Type	Function	Default
Bit 15	R	Reserved	X
Bit 14	R	Reserved	X
Bit 13	R	Reserved	X
Bit 12	R	ITPLA	X
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	IV5A	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	IPLA	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	IDATAA	X

This register provides activity monitoring on major SBSLITE inputs. When a monitored input makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the bits in this register are cleared. Bits that depend on multiple inputs making a low to high transition must have each input make a low to high transition between subsequent reads before the activity bit will be set high. The corresponding register bit reading low indicates a lack of transitions. This register should be read periodically to detect for stuck at conditions.

**ITPLA**

The ITPL active bit (ITPLA) detects low to high transitions on the ITPL input. ITPLA is set high when a rising edge has been observed on the ITPL input, and is set low when this register is read.

**IV5A**

The IV5 active bit (IV5A) detects low to high transitions on the IV5 input. IV5A is set high when a rising edge has been observed on the IV5 input, and is set low when this register is read.

#### IPLA

The IPL active bit (IPLA) detects low to high transitions on the IPL input. IPLA is set high when a rising edge has been observed on the IPL input, and is set low when this register is read.

#### IDATAA

The IDATA active bit (IDATAA) detects low to high transitions on the IDATA input bus. IDATAA is set high when rising edges have been observed on all the signals on the IDATA[7:0] bus, and is set low when this register is read.

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**Register 016H: SBSLITE Master Interrupt Enable**

Bit	Type	Function	Default
Bit 15	R/W	INTE	0
Bit 14	R/W	SBSE	0
Bit 13	R/W	IMSUE	0
Bit 12	R/W	OMSUE	0
Bit 11	R/W	REFDLLE	0
Bit 10	R/W	SYSDLLE	0
Bit 9	R/W	CSTRE	0
Bit 8	R/W	TW8EE	0
Bit 7	R/W	TP8EE	0
Bit 6	R/W	RW8DE	0
Bit 5	R/W	RP8DE	0
Bit 4	R/W	WPPE	0
Bit 3	R/W	PPPE	0
Bit 2	R/W	WILCE	0
Bit 1	R/W	PILCE	0
Bit 0	R/W	ISTAE	0

**INTE**

The INTE bit is a global interrupt enable bit. When INTE is set to a logic 1, interrupts will be indicated on the INTB output. When INTE is set to a logic 0, the INTB output will be held high impedance

**SBSE**

The SBSE interrupt enable bit, when set to a logic 1, enables interrupts from the SBSLITE Interrupt Register (register 011H) to be propagated to the INTB output.

**IMSUE**

The IMSUE interrupt enable, when set to a logic 1, enables interrupts from the IMSU block to be propagated to the INTB output.

**OMSUE**

The OMSUE interrupt enable, when set to a logic 1, enables interrupts from the OMSU block to be propagated to the INTB output.

#### REFDLLE

The REFDLLE interrupt enable, when set to a logic 1, enables interrupts from the REFDLL block to be propagated to the INTB output.

#### SYSDLLE

The SYSDLLE interrupt enable, when set to a logic 1, enables interrupts from the SYSDLL block to be propagated to the INTB output.

#### CSTRE

The CSTRE interrupt enable, when set to a logic 1, enables interrupts from the CSTR block to be propagated to the INTB output.

#### TW8EE

The TW8EE interrupt enable, when set to a logic 1, enables interrupts from the TW8E block to be propagated to the INTB output.

#### TP8EE

The TP8EE interrupt enable, when set to a logic 1, enables interrupts from the TP8E block to be propagated to the INTB output.

#### RW8DE

The RW8DE interrupt enable, when set to a logic 1, enables interrupts from the RW8D block to be propagated to the INTB output.

#### RP8DE

The RP8DE interrupt enable, when set to a logic 1, enables interrupts from the RP8D block to be propagated to the INTB output.

#### WPPE

The WPPE interrupt enable, when set to a logic 1, enables interrupts from the WPP block to be propagated to the INTB output.

#### PPPE

The PPPE interrupt enable, when set to a logic 1, enables interrupts from the PPP block to be propagated to the INTB output.

#### WILCE

The WILCE interrupt enable, when set to a logic 1, enables interrupts from the WILC block to be propagated to the INTB output.

#### PILCE

The PILCE interrupt enable, when set to a logic 1, enables interrupts from the PILC block to be propagated to the INTB output.

#### ISTAE

The ISTAE interrupt enable, when set to a logic 1, enables interrupts from the ISTA block to be propagated to the INTB output.

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**Register 017H: SBSLITE Free User Register**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7	R/W	FREE[7]	0
Bit 6	R/W	FREE[6]	0
Bit 5	R/W	FREE[5]	0
Bit 4	R/W	FREE[4]	0
Bit 3	R/W	FREE[3]	0
Bit 2	R/W	FREE[2]	0
Bit 1	R/W	FREE[1]	0
Bit 0	R/W	FREE[0]	0

**FREE[7:0]**

The software ID register (FREE) holds whatever value is written into it. Reset clears the contents of this register. This register has no impact on the operation of the SBSLITE.

**Register 018H: SBSLITE Outgoing SPE Control #1**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7	R/W	OSBI4_SPE3_TYP[1]	0
Bit 6	R/W	OSBI4_SPE3_TYP[0]	0
Bit 5	R/W	OSBI3_SPE3_TYP[1]	0
Bit 4	R/W	OSBI3_SPE3_TYP[0]	0
Bit 3	R/W	OSBI2_SPE3_TYP[1]	0
Bit 2	R/W	OSBI2_SPE3_TYP[0]	0
Bit 1	R/W	OSBI1_SPE3_TYP[1]	0
Bit 0	R/W	OSBI1_SPE3_TYP[0]	0

**Register 019H: SBSLITE Outgoing SPE Control #2**

Bit	Type	Function	Default
Bit 15	R/W	OSBI4_SPE2_TYP[1]	0
Bit 14	R/W	OSBI4_SPE2_TYP[0]	0
Bit 13	R/W	OSBI3_SPE2_TYP[1]	0
Bit 12	R/W	OSBI3_SPE2_TYP[0]	0
Bit 11	R/W	OSBI2_SPE2_TYP[1]	0
Bit 10	R/W	OSBI2_SPE2_TYP[0]	0
Bit 9	R/W	OSBI1_SPE2_TYP[1]	0
Bit 8	R/W	OSBI1_SPE2_TYP[0]	0
Bit 7	R/W	OSBI4_SPE1_TYP[1]	0
Bit 6	R/W	OSBI4_SPE1_TYP[0]	0
Bit 5	R/W	OSBI3_SPE1_TYP[1]	0
Bit 4	R/W	OSBI3_SPE1_TYP[0]	0
Bit 3	R/W	OSBI2_SPE1_TYP[1]	0
Bit 2	R/W	OSBI2_SPE1_TYP[0]	0
Bit 1	R/W	OSBI1_SPE1_TYP[1]	0
Bit 0	R/W	OSBI1_SPE1_TYP[0]	0

**OSBIx\_SPEy\_TYP[1:0]**

The OSBIx\_SPEy\_TYP[1:0] bits select the SPE type for the specified SPE within the specified Outgoing SBI bus. The types for each SPE are independently configured with possible types being T1, E1, DS3/E3 and fractional rate links. In TelecomBus mode (TELECOM\_BUS = 'b1), the OSBIx\_SPEy\_TYP[1:0] bits are unused.

The setting for OSBIx\_SPEy\_TYP[1:0] are:

OSBIx_SPEy_TYP[1:0]	Payload Type
00	T1
01	E1
10	DS3/E3
11	Fractional Rate

**Register 01AH: SBSLITE Transmit SPE Control**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11	R/W	TSBI4_SPE3_TYP	0
Bit 10	R/W	TSBI3_SPE3_TYP	0
Bit 9	R/W	TSBI2_SPE3_TYP	0
Bit 8	R/W	TSBI1_SPE3_TYP	0
Bit 7	R/W	TSBI4_SPE2_TYP	0
Bit 6	R/W	TSBI3_SPE2_TYP	0
Bit 5	R/W	TSBI2_SPE2_TYP	0
Bit 4	R/W	TSBI1_SPE2_TYP	0
Bit 3	R/W	TSBI4_SPE1_TYP	0
Bit 2	R/W	TSBI3_SPE1_TYP	0
Bit 1	R/W	TSBI2_SPE1_TYP	0
Bit 0	R/W	TSBI1_SPE1_TYP	0

**TSBIx\_SPEy\_TYP**

The TSBIx\_SPEy\_TYP bits select the SPE type for the specified SPE within the Transmit SBI336S bus for the purpose of CAS merging by the ICASM block. The types for each SPE are independently configured to be either T1 or E1. When TSBIx\_SPEy\_TYP is a logic 0, the associated SPE is configured for T1. When TSBIx\_SPEy\_TYP is a logic 1, the associated SPE is configured for E1. If the SPE contains something other than T1 or E1, the TSBIx\_SPEy\_TYP bit is unused. In TelecomBus mode (TELECOM\_BUS = 'b1), the TSBIx\_SPEy\_TYP bits are unused.

**Register 01BH: SBSLITE Receive SPE Control**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11	R/W	RSBI4_SPE3_TYP	0
Bit 10	R/W	RSBI3_SPE3_TYP	0
Bit 9	R/W	RSBI2_SPE3_TYP	0
Bit 8	R/W	RSBI1_SPE3_TYP	0
Bit 7	R/W	RSBI4_SPE2_TYP	0
Bit 6	R/W	RSBI3_SPE2_TYP	0
Bit 5	R/W	RSBI2_SPE2_TYP	0
Bit 4	R/W	RSBI1_SPE2_TYP	0
Bit 3	R/W	RSBI4_SPE1_TYP	0
Bit 2	R/W	RSBI3_SPE1_TYP	0
Bit 1	R/W	RSBI2_SPE1_TYP	0
Bit 0	R/W	RSBI1_SPE1_TYP	0

**RSBIx\_SPEy\_TYP**

In SBI mode (TELECOM\_BUS = 'b0), the RSBIx\_SPEy\_TYP bits select the SPE type for the specified SPE within the Receive SBI336S bus for the purpose of expanding the CAS by the OCASE block. The types for each SPE are independently configured to be either T1 or E1. When RSBIx\_SPEy\_TYP is a logic 0, the associated SPE is configured for T1. When RSBIx\_SPEy\_TYP is a logic 1, the associated SPE is configured for E1. If the SPE contains something other than T1 or E1, the RSBIx\_SPEy\_TYP bit is unused. In TelecomBus mode (TELECOM\_BUS = 'b1), the RSBIx\_SPEy\_TYP bits are unused.



**Register 020H: ISTA Incoming Parity Configuration**

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	IPE	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	INCLIC1	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	INCLIPL	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	IOP	0

**Reserved**

The Reserved bits must be set to a logic 0.

**IPE**

The incoming parity interrupt enable bit (IPE) is an active high interrupt enable. When IPE is set to a logic 1, the occurrence of a parity error on the incoming bus will cause an interrupt to be asserted on the INTB output. When IPE is set to a logic 0, incoming parity errors will not cause and interrupt.

**INCLIPL**

The INCLIPL bit controls whether the IPL input signal participates in the incoming parity calculations. When INCLIPL is set to a logic 1, the parity signal includes the IPL input. When INCLIPL is set to a logic 0, parity is calculated without regard to the state of IPL. These bits only take effect when in TelecomBus mode.

## INCLIC1

The INCLIC1 bit controls whether the IC1FP input signal participates in the incoming parity calculations. When INCLIC1 is set to a logic 1, the parity signal includes the IC1FP input. When INCLIC1 is set to a logic 0, parity is calculated without regard to the state of IC1FP. These bits only take effect when in TelecomBus mode.

## IOP

The incoming odd parity bit (IOP) control the expected parity on the incoming bus. When IOP is set to a logic 1, the expected parity on the IDP input is odd. When IOP is set to a logic 0, the parity is even. In SBI bus mode, the parity calculation encompasses the IDATA[7:0], IPL and IV5 signals. In TelecomBus mode, the parity calculation encompasses the IDATA[7:0] and optionally IPL and IC1FP as determined by the INCLIPL and INCLIC1 bits.

**Register 021H: ISTA Incoming Parity Status**

Bit	Type	Function	Default
Bit 15	R	Reserved	X
Bit 14	R	Reserved	X
Bit 13	R	Reserved	X
Bit 12	R	IPI	X
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7		Unused	0
Bit 6		Unused	0
Bit 5		Unused	0
Bit 4		Unused	0
Bit 3		Unused	0
Bit 2		Unused	0
Bit 1		Unused	0
Bit 0		Unused	0

**Reserved**

The Reserved bits should be ignored when this register is read.

**IPI**

The incoming parity error indication bit (IPI) is set high when a parity error has occurred on the Incoming bus. This bit is cleared when this register is read.

**Register 022H: ISTA TelecomBus Configuration**

Bit	Type	Function	Default
Bit 15	R/W	ILOCK0	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7		Unused	0
Bit 6		Unused	0
Bit 5		Unused	0
Bit 4		Unused	0
Bit 3		Unused	0
Bit 2		Unused	0
Bit 1		Unused	0
Bit 0		Unused	0

**ILOCK0**

The ILOCK0 bit controls the position of the J1 byte in the Incoming TelecomBus. When ILOCK0 is a logic 1, the J1 byte is expected to be locked to an offset of 0 (the byte following H3). When ILOCK0 is a logic 0, the J1 byte is expected to be locked to an offset of 522 (the byte following C1). This bit is used to determine where to sample the IC1FP[4:1] input in order to find the byte following J1 which will indicate multi-frame alignment. This bit only has an effect when in TelecomBus mode (TELECOM\_BUS = 'b1 in the SBSLITE Master Configuration Register).

**Register 028H: IMSU Configuration**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7		Unused	0
Bit 6		Unused	0
Bit 5		Unused	0
Bit 4	R/W	AUTO_UPDATE	0
Bit 3	R/W	SWAP_PENDINGE	0
Bit 2	R/W	UPDATEE	0
Bit 1	R	SWAP_PENDINGV	0
Bit 0	R	UPDATEV	0

**AUTO\_UPDATE**

The AUTO\_UPDATE bit selects when an off-line page update is performed. When AUTO\_UPDATE is a logic 1, the on-line page is automatically copied into the off-line page whenever there is a change to the connection memory page. When AUTO\_UPDATE is a logic 0, the off-line page is not updated when there is a change to the connection memory page. A page update may still be performed by writing to the Interrupt Status and Memory Page Update Register.

**SWAP\_PENDINGE**

A logic 1 on the SWAP\_PENDINGE bit enables the generation of an interrupt on a change of state of SWAP\_PENDINGV.

**UPDATEE**

A logic 1 on the UPDATEE bit enables the generation of an interrupt on a change of state from high to low of UPDATEV.

#### SWAP\_PENDINGV

The SWAP\_PENDINGV bit contains the current state of the page swap circuitry. This bit is a logic 1 when a switch to the connection memory page (CMP) has been recognized but the page swap has not yet happened. This bit is a logic 0 when there is not a page swap pending.

#### UPDATEV

The UPDATEV bit contains the current state of the time switch ram off-line page update circuitry. This bit is a logic 1 when the on-line page is being copied to the offline page. This bit is a logic 0 when the on-line page is not being copied.

**Register 029H: IMSU Interrupt Status and Memory Page Update Register**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7		Unused	0
Bit 6		Unused	0
Bit 5		Unused	0
Bit 4		Unused	0
Bit 3		Unused	0
Bit 2		Unused	0
Bit 1	R	SWAP_PENDINGI	X
Bit 0	R	UPDATEI	X

Writing to this register initiates an update of the off-line page in the time switch ram. The contents of the on-line page are written to the off-line page. During this update, the time switch ram may not be accessed through the indirect registers.

**SWAP\_PENDINGI**

The page swap pending interrupt status bit, SWAP\_PENDINGI, reports and acknowledges a change of state of the SWAP\_PENDINGV bit of the MSU Configuration register. This bit is cleared when this register is read. When enabled by the SWAP\_PENDINGE bit, the INT output reflects the state of this bit.

**UPDATEI**

The off-line page update interrupt status bit, UPDATEI, reports and acknowledges a change of state from high to low of the UPDATEV bit of the MSU Configuration register. This bit is cleared when this register is read. When enabled by the UPDATEE bit, the INT output reflects the state of this bit.

**Register 02AH: IMSU Indirect Time Switch Address**

Bit	Type	Function	Default
Bit 15	R/W	RWB	0
Bit 14		Unused	0
Bit 13	R/W	OUT_BYTE[13]	0
Bit 12	R/W	OUT_BYTE[12]	0
Bit 11	R/W	OUT_BYTE[11]	0
Bit 10	R/W	OUT_BYTE[10]	0
Bit 9	R/W	OUT_BYTE[9]	0
Bit 8	R/W	OUT_BYTE[8]	0
Bit 7	R/W	OUT_BYTE[7]	0
Bit 6	R/W	OUT_BYTE[6]	0
Bit 5	R/W	OUT_BYTE[5]	0
Bit 4	R/W	OUT_BYTE[4]	0
Bit 3	R/W	OUT_BYTE[3]	0
Bit 2	R/W	OUT_BYTE[2]	0
Bit 1	R/W	OUT_BYTE[1]	0
Bit 0	R/W	OUT_BYTE[0]	0

This register provides the address and the read/write control for the time switch configuration ram. Writing to this register triggers a ram access. Note that when an indirect write access is to be performed, the Indirect Time Switch Data register must first be setup before writing to this register. There must be a minimum of 4 SYSCLK cycles between consecutive ram write accesses. For a ram read access, it will take a maximum of 8 SYSCLK cycles for the Indirect Time Switch Data Register to contain valid data.

**RWB**

The indirect access control bit (RWB) selects between a write or read access to the time switch configuration RAM. Writing a logic zero to RWB triggers an indirect write operation. Data to be written is taken from the Indirect Time Switch Data register. Writing a logic one to RWB triggers an indirect read operation. The read data can be found in the Indirect Time Switch Data Register.

**OUT\_BYTE[13:0]**

The OUT\_BYTE[13:0] bits indicate the ram address to be accessed. Each address in the ram corresponds to a location in the output data bus. The contents stored in each ram address points to the byte from the input data bus which is to be output. In DS0 mode, legal values are 000H to 25F7H (0 to 9719). In column mode, legal values are 000H to 437H (0 to 1079). The byte numbers of the output frame are shown in the following table:



Row

1	0	1	2	3	...	1077	1078	1079
2	1080	1081	1082	1083	...	2157	2158	2159
3								
4								
5								
6								
7								
8								
9	8640	8641	8642	8643	...	9717	9718	9719

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**Register 02BH: IMSU Indirect Time Switch Data**

Bit	Type	Function	Default
Bit 15	R	VALID	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	IN_BYTE[13]	0
Bit 12	R/W	IN_BYTE [12]	0
Bit 11	R/W	IN_BYTE [11]	0
Bit 10	R/W	IN_BYTE [10]	0
Bit 9	R/W	IN_BYTE [9]	0
Bit 8	R/W	IN_BYTE [8]	0
Bit 7	R/W	IN_BYTE [7]	0
Bit 6	R/W	IN_BYTE [6]	0
Bit 5	R/W	IN_BYTE [5]	0
Bit 4	R/W	IN_BYTE [4]	0
Bit 3	R/W	IN_BYTE [3]	0
Bit 2	R/W	IN_BYTE [2]	0
Bit 1	R/W	IN_BYTE [1]	0
Bit 0	R/W	IN_BYTE [0]	0

This register contains data read from the time switch RAM after an indirect read operation or data to be inserted into the time switch RAM during an indirect write operation. The value held in the ram indicates which byte of the input data bus is to be switched to the output.

**VALID**

The VALID bit reports the presence of valid data from an indirect read. VALID is set to logic 1 when indirect read access returns data from the off-line RAM and remains asserted until the next time Indirect Time Switch Data register is read.

**Reserved**

The reserved bit should not be modified.

**IN\_BYTE[13:0]**

The IN\_BYTE[13:0] bits indicate which byte in the input frame is to be switched to the output. In DS0 mode, legal values are 000H to 25F7H (0 to 9719). In column mode, legal values are 000H to 437H (0 to 1079).

**Register 030H: ICASM CAS Enable Indirect Access Address Register**

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R/W	SBI[2]	0
Bit 8	R/W	SBI[1]	0
Bit 7	R/W	SBI[0]	0
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

**TRIB[4:0], SPE[1:0] and SBI[2:0]**

The TRIB[4:0], SPE[1:0] and SBI[2:0] fields are used to fully specify which SBI336 CAS enable register the write or read operation will apply.

TRIB[4:0] specifies the tributary number within the SBI336 SPE as specified by the SPE[1:0] and SBI[2:0] fields. Legal values for TRIB[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'. Legal values for SBI[2:0] are b'001' through b'100'.

**Register 031H: ICASM CAS Enable Indirect Access Control Register**

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R	Unused	0
Bit 8	R	Unused	0
Bit 7	R	BUSY	0
Bit 6	R	HST_ADDR_ERR	0
Bit 5	R	Unused	0
Bit 4	R	Unused	0
Bit 3	R	Unused	0
Bit 2	R	Unused	0
Bit 1	R/W	RWB	0
Bit 0	R	Unused	0

**RWB**

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the CAS Enable register. Writing a '0' to RWB triggers an indirect write operation. Data to be written is taken from the CAS Enable Indirect Access Data register. Writing a '1' to RWB triggers an indirect read operation. The data read can be found in the CAS Enable Indirect Access Data register.

**HST\_ADDR\_ERR**

When set following a host read this bit indicates that an illegal host access was attempted. An illegal host access occurs when an attempt is made to access an out of range tributary. Out of range tributaries accesses occur when SBI[2:0] is not in the range 1-4, SPE[1:0] is not in the range 1-3 and TRIB[4:0] is not in the range 1-28 for T1s, not in the range 1-21 for E1s and not equal to 1 for the remaining tributary types. This bit is cleared when this register is read.

## BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set high when a write to the CAS Enable Indirect Access Control register triggers an indirect access and will stay high until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the CAS Enable Indirect Access Data register or to determine when a new indirect write operation may commence.

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**Register 032H: ICASM CAS Enable Indirect Access Data Register**

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R	Unused	0
Bit 8	R	Unused	0
Bit 7	R	Unused	0
Bit 6	R	Unused	0
Bit 5	R	Unused	0
Bit 4	R	Unused	0
Bit 3	R	Unused	0
Bit 2	R	Unused	0
Bit 1	R	Unused	0
Bit 0	R/W	CAS_EN	0

**CAS\_EN**

The CAS\_EN bit is used to enable the insertion of CAS into the proper location in the associated tributary. When CAS\_EN is a logic 1 and the associated tributary is a T1, the CAS bits and PP bits are inserted into the PPSSSSFR byte. When CAS\_EN is a logic 1 and the associated tributary is an E1, the CAS bits are inserted into TS#16 and proper data is placed in the PP byte. When CAS\_EN is a logic 0, both the CAS and PP bits are not inserted. This bit should only be set if operating in 48-frame mode.

When CAS insertion is enabled, the latency of the CAS bits through the SBSLITE is two multi-frames. For T1 tributaries, this is 48 frames or 6ms. For E1 tributaries, this is 32 frames or 4 ms.

**Register 038H: ISTT Tributary Translator Control RAM Indirect Access Address Register**

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R/W	SBI[2]	0
Bit 8	R/W	SBI[1]	0
Bit 7	R/W	SBI[0]	0
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

TRIB[4:0], SPE[1:0] and SBI[2:0]

The TRIB[4:0], SPE[1:0] and SBI[2:0] fields are used to fully specify which SBI336 tributary translator control register the write or read operation will apply.

TRIB[4:0] specifies the tributary number within the SBI336 SPE as specified by the SPE[1:0] and SBI[2:0] fields. Legal values for TRIB[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'. Legal values for SBI[2:0] are b'o01' through b'100'.

**Register 039H: ISTT Tributary Translator Control RAM Indirect Access Control Register**

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R	Unused	0
Bit 8	R	Unused	0
Bit 7	R	BUSY	0
Bit 6	R	HST_ADDR_ERR	0
Bit 5	R	Unused	0
Bit 4	R	Unused	0
Bit 3	R	Unused	0
Bit 2	R	Unused	0
Bit 1	R/W	RWB	0
Bit 0	R	Unused	0

**RWB**

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the tributary translator control RAM. Writing a '0' to RWB triggers an indirect write operation. Data to be written is taken from the Tributary Translator Control RAM Indirect Access Data Register. Writing a '1' to RWB triggers an indirect read operation. The data read can be found in the Tributary Translator Control RAM Indirect Access Data.

**HST\_ADDR\_ERR**

When set following a host read this bit indicates that an illegal host access was attempted. An illegal host access occurs when an attempt is made to access an out of range tributary. Out of range tributaries accesses occur when SBI[2:0] is not in the range 1-4, SPE[1:0] is not in the range 1-3 and TRIB[4:0] is not in the range 1-28 for T1s, not in the range 1-21 for E1s and not equal to 1 for the remaining tributary types. This bit is cleared when this register is read.



## BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set high when a write to the Tributary Translator Control RAM Indirect Access Control Register triggers an indirect access and will stay high until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the Indirect Tributary Translator Control RAM Indirect Access Data register or to determine when a new indirect write operation may commence.

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**Register 03AH: ISTT Tributary Translator Control RAM Indirect Access Data Register**

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R	Unused	0
Bit 8	R	Unused	0
Bit 7	R	Unused	0
Bit 6	R	Unused	0
Bit 5	R	Unused	0
Bit 4	R	Unused	0
Bit 3	R	Unused	0
Bit 2	R	Unused	0
Bit 1	R/W	TVT	0
Bit 0	R/W	JUST_REQ_EN	0

**JUST\_REQ\_EN**

The JUST\_REQ\_EN bit is used to enable T1, E1, DS3, E3 and Fractional rate justification request state machines to convert JUST\_REQ to V5, V5+ and V5- characters to be carried over the serial SBI336S link. When this bit is set to 1 the justification request state machines will convert JUST\_REQ signals to V5 characters. When this bit is set to 0 the state machines will not generate additional V5 characters for the specified link and will only pass existing V5 characters through as nominal rate V5 characters. This bit should be set to 1 when this device is being used in SBI mode and is connected to physical layer device which is clock master of the transmit tributary.

This bit should not be set if the TVT bit is set. This bit has no effect in TelecomBus mode.

**TVT**

The TVT bit configures a T1 or E1 tributary as a transparent virtual tributary. When TVT is set to 1 the T1 or E1 tributary is configured as a TVT and the ERDI and REI bits in the V5 byte are transmitted across the serial link in one of the V5 characters. When TVT is set to 0 the T1 or E1 tributary is configured as a standard T1 or E1 link.

This bit should not be set if the JUST\_REQ\_EN bit is set. This bit has no effect in TelecomBus mode or if the SPE is configured to something other than T1 or E1 data.

**Register 040H: OSTT Tributary Translator Control RAM Indirect Access Address Register**

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R/W	SBI[2]	0
Bit 8	R/W	SBI[1]	0
Bit 7	R/W	SBI[0]	0
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

**TRIB[4:0], SPE[1:0] and SBI[2:0]**

The TRIB[4:0], SPE[1:0] and SBI[2:0] fields are used to fully specify which SBI336 tributary translator control register the write or read operation will apply.

TRIB[4:0] specifies the tributary number within the SBI336 SPE as specified by the SPE[1:0] and SBI[2:0] fields. Legal values for TRIB[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'. Legal values for SBI[2:0] are b'001' through b'100'.

**Register 041H: OSTT Tributary Translator Control RAM Indirect Access Control Register**

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R	Unused	0
Bit 8	R	Unused	0
Bit 7	R	BUSY	0
Bit 6	R	HST_ADDR_ERR	0
Bit 5	R	Unused	0
Bit 4	R	Unused	0
Bit 3	R	Unused	0
Bit 2	R	Unused	0
Bit 1	R/W	RWB	0
Bit 0	R	Unused	0

**RWB**

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the tributary translator control RAM. Writing a '0' to RWB triggers an indirect write operation. Data to be written is taken from the Tributary Translator Control RAM Indirect Access Data Register. Writing a '1' to RWB triggers an indirect read operation. The data read can be found in the Tributary Translator Control RAM Indirect Access Data.

**HST\_ADDR\_ERR**

When set following a host read this bit indicates that an illegal host access was attempted. An illegal host access occurs when an attempt is made to access an out of range tributary. Out of range tributaries accesses occur when SBI[2:0] is not in the range 1-4, SPE[1:0] is not in the range 1-3 and TRIB[4:0] is not in the range 1-28 for T1s, not in the range 1-21 for E1s and not equal to 1 for the remaining tributary types. This bit is cleared when this register is read.

## BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set high when a write to the Tributary Translator Control RAM Indirect Access Control Register triggers an indirect access and will stay high until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the Indirect Tributary Translator Control RAM Indirect Access Data register or to determine when a new indirect write operation may commence.

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**Register 042H: OSTT Tributary Translator Control RAM Indirect Access Data Register**

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R	Unused	0
Bit 8	R	Unused	0
Bit 7	R	Unused	0
Bit 6	R	Unused	0
Bit 5	R	Unused	0
Bit 4	R	Unused	0
Bit 3	R	Unused	0
Bit 2	R	Unused	0
Bit 1	R/W	TVT	0
Bit 0	R/W	JUST_REQ_EN	0

**JUST\_REQ\_EN**

The JUST\_REQ\_EN bit is used to enable T1, E1, DS3, E3 and Fractional rate justification request state machines to convert V5, V5+ and V5- characters to JUST\_REQs. When this bit is set to 1 the justification request state machines will convert V5 characters to the JUST\_REQ signal. When this bit is set to 0 the state machines will not generate JUST\_REQ. This bit should be set to 1 when this device is being used in SBI mode and is connected to link layer device which is clock slave to the transmit tributary.

This bit should not be set if the TVT bit is set. This bit has no effect in TelecomBus mode.

**TVT**

The TVT bit configures a T1 or E1 tributary as a transparent virtual tributary. When TVT is set to 1 the T1 or E1 tributary is configured as a TVT. Being a TVT, the ERDI and REI bits are received from the serial link in one of the V5 characters and are output on ODATA during the V5 byte. When TVT is set to 0 the T1 or E1 tributary is configured as a standard T1 or E1 link.

This bit should not be set if the JUST\_REQ\_EN bit is set. This bit has no effect in TelecomBus mode or if the SPE is configured to something other than T1 or E1 data.

**Register 048H: OMSU Configuration**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7		Unused	0
Bit 6		Unused	0
Bit 5		Unused	0
Bit 4	R/W	AUTO_UPDATE	0
Bit 3	R/W	SWAP_PENDINGE	0
Bit 2	R/W	UPDATEE	0
Bit 1	R	SWAP_PENDINGV	0
Bit 0	R	UPDATEV	0

**AUTO\_UPDATE**

The AUTO\_UPDATE bit selects when an off-line page update is performed. When AUTO\_UPDATE is a logic 1, the on-line page is automatically copied into the off-line page whenever there is a change to the connection memory page. When AUTO\_UPDATE is a logic 0, the off-line page is not updated when there is a change to the connection memory page. A page update may still be performed by writing to the Interrupt Status and Memory Page Update Register.

**SWAP\_PENDINGE**

A logic 1 on the SWAP\_PENDINGE bit enables the generation of an interrupt on a change of state of SWAP\_PENDINGV.

**UPDATEE**

A logic 1 on the UPDATEE bit enables the generation of an interrupt on a change of state from high to low of UPDATEV.

#### SWAP\_PENDINGV

The SWAP\_PENDINGV bit contains the current state of the page swap circuitry. This bit is a logic 1 when a switch to the connection memory page (CMP) has been recognized but the page swap has not yet happened. This bit is a logic 0 when there is not a page swap pending.

#### UPDATEV

The UPDATEV bit contains the current state of the time switch ram off-line page update circuitry. This bit is a logic 1 when the on-line page is being copied to the offline page. This bit is a logic 0 when the on-line page is not being copied.

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**Register 049H: OMSU Interrupt Status and Memory Page Update Register**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7		Unused	0
Bit 6		Unused	0
Bit 5		Unused	0
Bit 4		Unused	0
Bit 3		Unused	0
Bit 2		Unused	0
Bit 1	R	SWAP_PENDINGI	X
Bit 0	R	UPDATEI	X

Writing to this register initiates an update of the off-line page in the time switch ram. The contents of the on-line page are written to the off-line page. During this update, the time switch ram may not be accessed through the indirect registers.

**SWAP\_PENDINGI**

The page swap pending interrupt status bit, SWAP\_PENDINGI, reports and acknowledges a change of state of the SWAP\_PENDINGV bit of the MSU Configuration register. This bit is cleared when this register is read. When enabled by the SWAP\_PENDINGE bit, the INT output reflects the state of this bit.

**UPDATEI**

The off-line page update interrupt status bit, UPDATEI, reports and acknowledges a change of state from high to low of the UPDATEV bit of the MSU Configuration register. This bit is cleared when this register is read. When enabled by the UPDATEE bit, the INT output reflects the state of this bit.

**Register 04AH: OMSU Indirect Time Switch Address**

Bit	Type	Function	Default
Bit 15	R/W	RWB	0
Bit 14		Unused	0
Bit 13	R/W	OUT_BYTE[13]	0
Bit 12	R/W	OUT_BYTE[12]	0
Bit 11	R/W	OUT_BYTE[11]	0
Bit 10	R/W	OUT_BYTE[10]	0
Bit 9	R/W	OUT_BYTE[9]	0
Bit 8	R/W	OUT_BYTE[8]	0
Bit 7	R/W	OUT_BYTE[7]	0
Bit 6	R/W	OUT_BYTE[6]	0
Bit 5	R/W	OUT_BYTE[5]	0
Bit 4	R/W	OUT_BYTE[4]	0
Bit 3	R/W	OUT_BYTE[3]	0
Bit 2	R/W	OUT_BYTE[2]	0
Bit 1	R/W	OUT_BYTE[1]	0
Bit 0	R/W	OUT_BYTE[0]	0

This register provides the address and the read/write control for the time switch configuration ram. Writing to this register triggers a ram access. Note that when an indirect write access is to be performed, the Indirect Time Switch Data register must first be setup before writing to this register. There must be a minimum of 4 SYSCLK cycles between consecutive ram accesses. For a ram read access, it will take a maximum of 8 SYSCLK cycles for the Indirect Time Switch Data Register to contain valid data.

**RWB**

The indirect access control bit (RWB) selects between a write or read access to the time switch configuration RAM. Writing a logic zero to RWB triggers an indirect write operation. Data to be written is taken from the Indirect Time Switch Data register. Writing a logic one to RWB triggers an indirect read operation. The read data can be found in the Indirect Time Switch Data Register.

OUT\_BYTE[13:0]

The OUT\_BYTE[13:0] bits indicate the ram address to be accessed. Each address in the ram corresponds to a location in the output data bus. The contents stored in each ram address points to the byte from the input data bus which is to be output. In DS0 mode, legal values are 000H to 25F7H (0 to 9719). In column mode, legal values are 000H to 437H (0 to 1079). The byte numbers of the output frame are shown in the following table.

**Row**

1	0	1	2	3	...	1077	1078	1079
2	1080	1081	1082	1083	...	2157	2158	2159
3								
4								
5								
6								
7								
8								
9	8640	8641	8642	8643	...	9717	9718	9719

**Register 04BH: OMSU Indirect Time Switch Data**

Bit	Type	Function	Default
Bit 15	R	VALID	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	IN_BYTE[13]	0
Bit 12	R/W	IN_BYTE [12]	0
Bit 11	R/W	IN_BYTE [11]	0
Bit 10	R/W	IN_BYTE [10]	0
Bit 9	R/W	IN_BYTE [9]	0
Bit 8	R/W	IN_BYTE [8]	0
Bit 7	R/W	IN_BYTE [7]	0
Bit 6	R/W	IN_BYTE [6]	0
Bit 5	R/W	IN_BYTE [5]	0
Bit 4	R/W	IN_BYTE [4]	0
Bit 3	R/W	IN_BYTE [3]	0
Bit 2	R/W	IN_BYTE [2]	0
Bit 1	R/W	IN_BYTE [1]	0
Bit 0	R/W	IN_BYTE [0]	0

This register contains data read from the time switch RAM after an indirect read operation or data to be inserted into the time switch RAM during an indirect write operation. The value held in the ram indicates which byte of the input data bus is to be switched to the output.

**VALID**

The VALID bit reports the presence of valid data from an indirect read. VALID is set to logic 1 when indirect read access returns data from the off-line RAM and remains asserted until the next time Indirect Time Switch Data register is read.

**Reserved**

The reserved bit should not be modified.

IN\_BYTE[13:0]

The IN\_BYTE[13:0] bits indicate which byte in the input frame is to be switched to the output. In DS0 mode, legal values are 000H to 25F7H (0 to 9719). In column mode, legal values are 000H to 437H (0 to 1079).

The MSU has the ability of overwrite the outputs when a value outside the range specified above is programmed. When IN\_BYTE[13:12] = 'b11, the value output on OPL, OTPL, OV5, OJ1, OTAIS and ODATA[7:0] is overwritten as shown in the following tables.

In Column Mode (TelecomBus):

IN_BYTE						
[13]	[12]	[11]	[10]	[9]	[8]	[7:0]
1	1	MODE[2]	MODE[1]	MODE[0]	OTAIS	ODATA[7:0]

Where

MODE[2:0]		Setting of Outputs				Special Setting
		OPL	OTPL	OC1FP (marking the J1 byte)	OV5	
000	Transport Overhead (TOH)	0	0	0	0	
001	J1 column	1	0	1 for 1st row, 0 for rows 2-9	0	ODATA is set to 11111CC at the H4 byte. CC indicates the frame number in the multi-frame.
010	Path level stuff columns	1	0	0	0	
011	Tributary Vx columns (V1, V2, V3, V4)	1	0 for 1st row, 1 for rows 2-9	0	0	
100	Tributary data columns	1	1	0	0	
101	Tributary data columns with V5	1	1	0	1 for 1st row in multi-frame, 0 otherwise	
110 – 111	Reserved					

In Column Mode (SBI bus):

IN_BYTE						
[13]	[12]	[11]	[10]	[9]	[8]	[7:0]
1	1	MODE[2]	MODE[1]	MODE[0]	Reserved	ODATA[7:0]

Where

MODE[2:0]		Setting of Outputs		
		OPL	OV5	Special Instructions
000	Transport Overhead (TOH)	0	0	Should be set for columns 0 to 35.
001	Reserved			Do not use
010	Path level stuff columns	0	0	Should be set for stuff columns > 35
011	Tributary Vx columns (V1, V2, V3, V4)	0 for 1st row, 1 for rows 2-9	0	Use for T1 and E1 tributaries only
100	Tributary data columns	1	0	Use for any data type
101	Tributary data columns with V5	1	1 for 1st row in multi-frame, 0 otherwise	Use for T1 and E1 tributaries only. Note that ODATA=00H for first row in multi-frame.
110 – 111	Reserved			Do not use

In DS0 Mode (SBI bus):

IN_BYTE						
[13]	[12]	[11]	[10]	[9]	[8]	[7:0]
1	1	Reserved	OPL	Reserved	Reserved	ODATA[7:0]

Note that for all modes, the Reserved bits should be set to a logic 0.

**Register 050H: OCASM CAS Enable Indirect Access Address Register**

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R/W	SBI[2]	0
Bit 8	R/W	SBI[1]	0
Bit 7	R/W	SBI[0]	0
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

TRIB[4:0], SPE[1:0] and SBI[2:0]

The TRIB[4:0], SPE[1:0] and SBI[2:0] fields are used to fully specify which SBI336 CAS enable register the write or read operation will apply.

TRIB[4:0] specifies the tributary number within the SBI336 SPE as specified by the SPE[1:0] and SBI[2:0] fields. Legal values for TRIB[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'. Legal values for SBI[2:0] are b'001' through b'100'.

**Register 051H: OCASM CAS Enable Indirect Access Control Register**

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 19	R	Unused	0
Bit 8	R	Unused	0
Bit 7	R	BUSY	0
Bit 6	R	HST_ADDR_ERR	0
Bit 5	R	Unused	0
Bit 4	R	Unused	0
Bit 3	R	Unused	0
Bit 2	R	Unused	0
Bit 1	R/W	RWB	0
Bit 0	R	Unused	0

**RWB**

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the CAS Enable register. Writing a '0' to RWB triggers an indirect write operation. Data to be written is taken from the CAS Enable Indirect Access Data register. Writing a '1' to RWB triggers an indirect read operation. The data read can be found in the CAS Enable Indirect Access Data register.

**HST\_ADDR\_ERR**

When set following a host read this bit indicates that an illegal host access was attempted. An illegal host access occurs when an attempt is made to access an out of range tributary. Out of range tributaries accesses occur when SBI[2:0] is not in the range 1-4, SPE[1:0] is not in the range 1-3 and TRIB[4:0] is not in the range 1-28 for T1s, not in the range 1-21 for E1s and not equal to 1 for the remaining tributary types. This bit is cleared when this register is read.



## BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set high when a write to the CAS Enable Indirect Access Control register triggers an indirect access and will stay high until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the CAS Enable Indirect Access Data register or to determine when a new indirect write operation may commence.

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**Register 052H: OCASM CAS Enable Indirect Access Data Register**

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 19	R	Unused	0
Bit 8	R	Unused	0
Bit 7	R	Unused	0
Bit 6	R	Unused	0
Bit 5	R	Unused	0
Bit 4	R	Unused	0
Bit 3	R	Unused	0
Bit 2	R	Unused	0
Bit 1	R	Unused	0
Bit 0	R/W	CAS_EN	0

**CAS\_EN**

The CAS\_EN bit is used to enable the insertion of CAS into the proper location in the associated tributary. When CAS\_EN is a logic 1 and the associated tributary is a T1, the CAS bits and PP bits are inserted into the PPSSSSFR byte. When CAS\_EN is a logic 1 and the associated tributary is an E1, the CAS bits are inserted into TS#16 and proper data is placed in the PP byte. When CAS\_EN is a logic 0, both the CAS and PP bits are not inserted. This bit should only be set if operating in 48-frame mode.

When CAS insertion is enabled, the latency of the CAS bits through the SBSLITE is two multi-frames. For T1 tributaries, this is 48 frames or 6ms. For E1 tributaries, this is 32 frames or 4 ms.

**Register 060H: OSTA Outgoing Configuration and Parity**

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	OLOCK0	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	INCLOC1FP	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	INCLOPL	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	OOP	0

Reserved

The Reserved bits must be set to a logic 0.

**OLOCK0**

The OLOCK0 bit controls the position of the J1 byte in the Outgoing TelecomBus. When OLOCK0 is a logic 1, the J1 byte is expected to be locked to an offset of 0 (the byte following H3). When OLOCK0 is a logic 0, the J1 byte is expected to be locked to an offset of 522 (the byte following C1). This bit is used to determine where to pulse the OC1FP output when any part of STS1\_OJ1EN[12:1] or STS1\_OV1EN[12:1] are set. This bit only has an effect when in TelecomBus mode (TELECOM\_BUS = 'b1 in the SBSLITE Master Configuration Register).

**INCLOC1FP**

The INCLOC1FP bit controls whether the OC1FP output signal participates in the outgoing bus parity calculations. When INCLOC1FP is set to a logic 1, the parity signal includes the OC1FP output. When INCLOC1FP is set to a logic 0, parity is calculated without regard to the state of OC1FP. These bits only take effect when in TelecomBus mode.

## INCLOPL

The INCLOPL bit controls whether the OPL output signal participates in the outgoing parity calculations. When INCLOPL is set to a logic 1, the parity signal includes the OPL output. When INCLOPL is set to a logic 0, parity is calculated without regard to the state of OPL[x]. These bits only take effect when in TelecomBus mode.

## OOP

The outgoing odd parity bit (OOP) controls the parity generated on the outgoing bus. When OOP is set to a logic 1, the parity on the ODP output is odd. When OOP is set to a logic 0, the parity is even. In SBI bus mode, the parity calculation encompasses the ODATA[7:0], OPL and OV5 signals. In TelecomBus mode, the parity calculation encompasses the ODATA[7:0] and optionally OPL and OC1FP as determined by the INCLOPL and INCLOC1FP bits.

**Register 061H: OSTA Outgoing J1 Configuration**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11	R/W	STS1_OJ1EN[12]	0
Bit 10	R/W	STS1_OJ1EN[11]	0
Bit 9	R/W	STS1_OJ1EN[10]	0
Bit 8	R/W	STS1_OJ1EN[9]	0
Bit 7	R/W	STS1_OJ1EN[8]	0
Bit 6	R/W	STS1_OJ1EN[7]	0
Bit 5	R/W	STS1_OJ1EN[6]	0
Bit 4	R/W	STS1_OJ1EN[5]	0
Bit 3	R/W	STS1_OJ1EN[4]	0
Bit 2	R/W	STS1_OJ1EN[3]	0
Bit 1	R/W	STS1_OJ1EN[2]	0
Bit 0	R/W	STS1_OJ1EN[1]	0

**STS1\_OJ1EN[12:1]**

The STS1\_OJ1EN[12:1] bits control the inclusion of the J1 byte identification on the OC1FP output for each of the 12 STS/AUs. When STS1\_OJ1EN[x] is a logic 1, the OC1FP output will pulse high during the J1 byte position of the associated STS/AU along with the usual C1 byte position. The position of the J1 byte relative to the C1 position is determined by the OLOCK0 bit. When STS1\_OJ1EN[x] is a logic 0, the OC1FP will not pulse high during the J1 byte position of the associated STS/AU. This bit only has an effect when in TelecomBus mode (TELECOM\_BUS = 'b1 in the SBSLITE Master Configuration Register). These register bits should not be set if the receive serial link contains J1 characters.

See section 13.12 for more information about J1/V1 insertion.

**Register 062H: OSTA Outgoing V1 Configuration**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11	R/W	STS1_OV1EN[12]	0
Bit 10	R/W	STS1_OV1EN[11]	0
Bit 9	R/W	STS1_OV1EN[10]	0
Bit 8	R/W	STS1_OV1EN[9]	0
Bit 7	R/W	STS1_OV1EN[8]	0
Bit 6	R/W	STS1_OV1EN[7]	0
Bit 5	R/W	STS1_OV1EN[6]	0
Bit 4	R/W	STS1_OV1EN[5]	0
Bit 3	R/W	STS1_OV1EN[4]	0
Bit 2	R/W	STS1_OV1EN[3]	0
Bit 1	R/W	STS1_OV1EN[2]	0
Bit 0	R/W	STS1_OV1EN[1]	0

**STS1\_OV1EN[12:1]**

The STS1\_OV1EN[12:1] bits control the inclusion of the byte following J1 identification on the OC1FP output for each of the 12 STS/AUs. When STS1\_OV1EN[x] is a logic 1, the OC1FP output will pulse high during the byte following the J1 position of the associated STS/AU along with the usual C1 byte position. The position of the J1 byte relative to the C1 position is determined by the OLOCK0 bit. When STS1\_OV1EN is a logic 0, the OC1FP will not pulse high during the byte following the J1 position of the associated STS/AU. This bit only has an effect when in TelecomBus mode (TELECOM\_BUS = 'b1 in the SBSLITE Master Configuration Register). These register bits should not be set if the receive serial link contains J1 characters.

See section 13.12 for more information about J1/V1 insertion.

**Register 063H: OSTA H1-H2 Pointer Value**

Bit	Type	Function	Default
Bit 15	R/W	H1[7]	0
Bit 14	R/W	H1[6]	0
Bit 13	R/W	H1[5]	0
Bit 12	R/W	H1[4]	0
Bit 11	R/W	H1[3]	0
Bit 10	R/W	H1[2]	0
Bit 9	R/W	H1[1]	0
Bit 8	R/W	H1[0]	0
Bit 7	R/W	H2[7]	0
Bit 6	R/W	H2[6]	0
Bit 5	R/W	H2[5]	0
Bit 4	R/W	H2[4]	0
Bit 3	R/W	H2[3]	0
Bit 2	R/W	H2[2]	0
Bit 1	R/W	H2[1]	0
Bit 0	R/W	H2[0]	0

**H1[7:0]**

The H1[7:0] bits contain the value to be output during the H1 position of the transport overhead of the Outgoing TelecomBus when the STS1\_PTR\_SEL[x] bit is a logic 0 and the OH1H2EN bit is set high. These bits have no effect when OH1H2EN is low or when in SBI mode (TELECOM\_BUS = 'b0 in the Master Configuration Register).

**H2[7:0]**

The H2[7:0] bits contain the value to be output during the H2 position of the transport overhead of the Outgoing TelecomBus when the STS1\_PTR\_SEL[x] bit is a logic 0 and the OH1H2EN bit is set high. These bits have no effect when OH1H2EN is low or when in SBI mode (TELECOM\_BUS = 'b0 in the Master Configuration Register).

**Register 064H: OSTA Alternate H1-H2 Pointer Value**

Bit	Type	Function	Default
Bit 15	R/W	H1_ALT[7]	0
Bit 14	R/W	H1_ALT[6]	0
Bit 13	R/W	H1_ALT[5]	0
Bit 12	R/W	H1_ALT[4]	0
Bit 11	R/W	H1_ALT[3]	0
Bit 10	R/W	H1_ALT[2]	0
Bit 9	R/W	H1_ALT[1]	0
Bit 8	R/W	H1_ALT[0]	0
Bit 7	R/W	H2_ALT[7]	0
Bit 6	R/W	H2_ALT[6]	0
Bit 5	R/W	H2_ALT[5]	0
Bit 4	R/W	H2_ALT[4]	0
Bit 3	R/W	H2_ALT[3]	0
Bit 2	R/W	H2_ALT[2]	0
Bit 1	R/W	H2_ALT[1]	0
Bit 0	R/W	H2_ALT[0]	0

**H1\_ALT[7:0]**

The H1\_ALT[7:0] bits contain the value to be output during the H1 position of the transport overhead of the Outgoing TelecomBus when the STS1\_PTR\_SEL[x] bit is a logic 1 and the OH1H2EN bit is set high. These bits have no effect when OH1H2EN is low or when in SBI mode (TELECOM\_BUS = 'b0 in the Master Configuration Register).

**H2\_ALT[7:0]**

The H2\_ALT[7:0] bits contain the value to be output during the H2 position of the transport overhead of the Outgoing TelecomBus when the STS1\_PTR\_SEL[x] bit is a logic 1 and the OH1H2EN bit is set high. These bits have no effect when OH1H2EN is low or when in SBI mode (TELECOM\_BUS = 'b0 in the Master Configuration Register).



**Register 065H: OSTA H1-H2 Pointer Selection**

Bit	Type	Function	Default
Bit 15	R/W	OH1H2EN	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11	R/W	STS1_PTR_SEL[12]	0
Bit 10	R/W	STS1_PTR_SEL[11]	0
Bit 9	R/W	STS1_PTR_SEL[10]	0
Bit 8	R/W	STS1_PTR_SEL[9]	0
Bit 7	R/W	STS1_PTR_SEL[8]	0
Bit 6	R/W	STS1_PTR_SEL[7]	0
Bit 5	R/W	STS1_PTR_SEL[6]	0
Bit 4	R/W	STS1_PTR_SEL[5]	0
Bit 3	R/W	STS1_PTR_SEL[4]	0
Bit 2	R/W	STS1_PTR_SEL[3]	0
Bit 1	R/W	STS1_PTR_SEL[2]	0
Bit 0	R/W	STS1_PTR_SEL[1]	0

**OH1H2EN**

The OH1H2EN bit enables the insertion of the H1 and H2 bytes in the transport overhead on the Outgoing TelecomBus. When OH1H2EN is a logic 1, the values in the internal registers is inserted into the H1 and H2 bytes of the Outgoing TelecomBus according to the STS1\_PTR\_SEL[12:1] bits. When OH1H2EN is a logic 0, the values from the internal registers is not inserted into the H1 and H2 bytes. This bit has no effect when in SBI mode (TELECOM\_BUS = 'b0 in the Master Configuration Register). This bit should not be set if any of the STS/AUs are floating.

**STS1\_PTR\_SEL[12:1]**

The STS1\_PTR\_SEL[12:1] bits select which of the two H1-H2 Pointer registers is used for each of the 12 STS/AUs output on the Outgoing TelecomBus when the OH1H2EN bit is set. When STS1\_PTR\_SEL[x] is a logic 0, the OSTA Transmit H1-H2 Pointer Value register is used for the associated STS/AU on the Outgoing bus. When STS1\_PTR\_SEL[x] is a logic 1, the OSTA Transmit Alternate H1-H2 Pointer Value register is used for the associated STS/AU on the Outgoing bus. These bits have no effect when OH1H2EN is low or when in SBI mode (TELECOM\_BUS = 'b0 in the Master Configuration Register).

**Register 070h: WPP Indirect Address**

Bit	Type	Function	Default
Bit 15	R	BUSY	0
Bit 14	R/W	RDWRB	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

This register provides selection of configuration pages and of the time-slots to be accessed in the WPP block. Writing to this register triggers an indirect register access.

**PATH[3:0]**

The PATH[3:0] bits select which time-multiplexed division is accessed by the current indirect transfer.

PATH[3:0]	Time Division #
0000	Invalid STS-1/STM-0 path
0001-1100	STS-1/STM-0 path #1 to STS-1/STM-0 path #12
1101-1111	Invalid STS-1/STM-0 path

**IADDR[3:0]**

The internal RAM page bits select which page of the internal RAM is access by the current indirect transfer. Six pages are defined for the monitor (IADDR[3] = '0') : the configuration page, the PRBS[22:7] page, the PRBS[6:0] page, the B1/E1 value page, the Monitor error count page and the received B1/E1 byte.

IADDR[3:0]	RAM page
0000	STS-1/STM-0 path Configuration page
0001	PRBS[22:7] page
0010	PRBS[6:0] page

IADDR[3:0]	RAM page
0011	Reserved
0100	Monitor error count page
0101	Reserved

Four pages are defined for the generator (IADDR [3] = '1') : the configuration page, the PRBS[22:7] page, the PRBS[6:0] page and the B1/E1 value.

IADDR[3:0]	RAM page
1000	STS-1/STM-0 path Configuration page
1001	PRBS[22:7] page
1010	PRBS[6:0] page
1011	Reserved

#### RDWRB

The active high read and active low write (RDWRB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RDWRB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transfer to the Indirect Data Register. When RDWRB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transfer to the addressed location in the internal RAM.

#### BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

**Register 071h: WPP Indirect Data**

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

This register contains the data read from the internal RAM after an indirect read operation or the data to be inserted into the internal RAM in an indirect write operation.

**DATA[15:0]**

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RDWRB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transfer to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RDWRB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which page of the internal RAM is being accessed.

**Register 071h (IADDR = 0h): WPP Monitor STS-1/STM-0 path Configuration**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	SEQ_PRBSB	0
Bit 5	R/W	Reserved	0
Bit 4		Unused	X
Bit 3	W	RESYNC	0
Bit 2	R/W	INV_PRBS	0
Bit 1	R/W	AMODE	0
Bit 0	R/W	MON_ENA	0

This register contains the definition of the WPP Indirect Data register (Register 071h) when accessing Indirect Address 0h (IADDR[3:0] is "0h" in register 070h).

For STS-Nc rates, only the first STS-1 has to be configured

**MON\_ENA**

Monitor Enable register bit, enables the PRBS monitor for the STS-1/STM-0 path specified in the PATH[3:0] of register 070h (WPP Indirect Address). If MON\_ENA is set to '1', a PRBS sequence is generated and compare to the incoming one inserted in the payload of the SONET/SDH frame. If MON\_ENA is low, the data at the input of the monitor is ignored.

**AMODE**

If AMODE is high, the monitor is in Autonomous mode, and the incoming SONET/SDH payload is compared to the internally generated one. In Autonomous mode, the beginning of the SPE is always place next to the H3 byte (zero offset), so the J1 pulses are ignored. When using the WPP in TelecomBus mode, this bit must be set high. When using the WPP in SBI mode, this bit must be set low.

**INV\_PRBS**

This sets the monitor to invert the PRBS before comparing it to the internally generated payload. When set high, the PRBS bytes will be inverted, else they will be compared unmodified.

#### RESYNC

This sets the monitor to re-initialize the PRBS sequence. When set high the monitor's state machine will be forced in the Out Of Sync state and automatically try to resynchronize to the incoming stream.

#### Reserved

The reserved bits must be set low for correct operation of the SBSLITE.

**Register 071h (IADDR = 1h): WPP Monitor PRBS[22:7] Accumulator**

Bit	Type	Function	Default
Bit 15	R/W	PRBS[22]	0
Bit 14	R/W	PRBS[21]	0
Bit 13	R/W	PRBS[20]	0
Bit 12	R/W	PRBS[19]	0
Bit 11	R/W	PRBS[18]	0
Bit 10	R/W	PRBS[17]	0
Bit 9	R/W	PRBS[16]	0
Bit 8	R/W	PRBS[15]	0
Bit 7	R/W	PRBS[14]	0
Bit 6	R/W	PRBS[13]	0
Bit 5	R/W	PRBS[12]	0
Bit 4	R/W	PRBS[11]	0
Bit 3	R/W	PRBS[10]	0
Bit 2	R/W	PRBS[9]	0
Bit 1	R/W	PRBS[8]	0
Bit 0	R/W	PRBS[7]	0

This register contains the definition of the WPP Indirect Data register (Register 071h) when accessing Indirect Address 1h (IADDR[3:0] is "1h" in register 070h).

For STS-Nc rates, only the first STS-1 has to be configured.

**PRBS[22:7]**

The PRBS[22:7] register are the 16 MSBs of the LFSR state of the STS-1/STM-0 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

**Register 071h (IADDR = 2h): WPP Monitor PRBS[6:0] Accumulator**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	PRBS[6]	0
Bit 5	R/W	PRBS[5]	0
Bit 4	R/W	PRBS[4]	0
Bit 3	R/W	PRBS[3]	0
Bit 2	R/W	PRBS[2]	0
Bit 1	R/W	PRBS[1]	0
Bit 0	R/W	PRBS[0]	0

This register contains the definition of the WPP Indirect Data register (Register 071h) when accessing Indirect Address 2h (IADDR[3:0] is “2h” in register 070h).

For STS-Nc rates, only the first STS-1 has to be configured.

**PRBS[6:0]**

The PRBS[6:0] register are the 7 LSBs of the LFSR state of the STS-1/STM-0 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.



**Register 071h (IADDR = 4h): WPP Monitor Error Count**

Bit	Type	Function	Default
Bit 15	R	ERR_CNT[15]	X
Bit 14	R	ERR_CNT[14]	X
Bit 13	R	ERR_CNT[13]	X
Bit 12	R	ERR_CNT[12]	X
Bit 11	R	ERR_CNT[11]	X
Bit 10	R	ERR_CNT[10]	X
Bit 9	R	ERR_CNT[9]	X
Bit 8	R	ERR_CNT[8]	X
Bit 7	R	ERR_CNT[7]	X
Bit 6	R	ERR_CNT[6]	X
Bit 5	R	ERR_CNT[5]	X
Bit 4	R	ERR_CNT[4]	X
Bit 3	R	ERR_CNT[3]	X
Bit 2	R	ERR_CNT[2]	X
Bit 1	R	ERR_CNT[1]	X
Bit 0	R	ERR_CNT[0]	X

This register contains the definition of the WPP Indirect Data register (Register 071h) when accessing Indirect Address 4h (IADDR[3:0] is “4h” in register 070h).

**ERR\_CNT[15:0]**

The ERR\_CNT[15:0] register contains the cumulative number of errors in the PRBS bytes since the last error reporting event. Errors are accumulated only when the monitor is in the synchronized state. Each PRBS byte will only contribute a single error, even if there are multiple errors within a single PRBS byte. The transfer of the error counter to this holding register is triggered by writing to the WPP Performance Counters Transfer Trigger Register (07CH) or writing the SBSLITE Master Signal Monitor #1, Accumulation Trigger Register (014H). The error counter is cleared and restarted after its value is transferred to the ERR\_CNT[15:0] holding register. No errors are missed during the transfer. The error counter will not wrap around after reaching FFFFh, it will saturate at this value.

**Register 071h (IADDR = 8h): WPP Generator STS-1/STM-0 Path Configuration**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	Reserved	0
Bit 12	R/W	LINKENA	0
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	Reserved	0
Bit 8	R/W	LINKENA	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	SEQ_PRBSB	0
Bit 4	R/W	Reserved	0
Bit 3	W	FORCE_ERR	0
Bit 2		Unused	
Bit 1	R/W	INV_PRBS	0
Bit 0	R/W	AMODE	0

This register contains the definition of the WPP Indirect Data register (Register 071h) when accessing Indirect Address 8h (IADDR[3:0] is "8h" in register 070h).

For STS-Nc rates, only the first STS-1 has to be configured.

**AMODE**

If AMODE is high, the generator is in Autonomous mode, and the SONET/SDH frame is generated using only the C1 pulse. The payload frame (J1) is at a fixed alignment as no pointer movements are generated. When using the WPP in TelecomBus mode, this bit must be set high. When using the WPP in SBI mode, this bit must be set low.

**INV\_PRBS**

Sets the generator to invert the PRBS before inserting it in the payload. When set high, the PRBS bytes will be inverted, else they will be inserted unmodified.

**FORCE\_ERR**

The Force Error bit is used to force bit errors in the inserted pattern. When a logic one is written, the MSB of the next byte will be inverted, inducing a single bit error. The register clears itself when the operation is complete.

#### SEQ\_PRBSB

This bit enables the insertion of a PRBS sequence or a sequential pattern in the payload. When low, the payload is filled with PRBS bytes, and when high, a sequential pattern is inserted.

#### LINKENA

These two bits specify if PRBS is to be inserted in the path through the TW8E. If LINKENA is high patterns are generated in the SONET/SDH frame to the TW8E, else no pattern is generated and the unmodified SONET/SDH input frame is passed to the TW8E.

#### Reserved

The reserved bits must be set low for correct operation of the SBSLITE.

**Register 071h (IADDR = 9h): WPP Generator PRBS[22:7] Accumulator**

Bit	Type	Function	Default
Bit 15	R/W	PRBS[22]	0
Bit 14	R/W	PRBS[21]	0
Bit 13	R/W	PRBS[20]	0
Bit 12	R/W	PRBS[19]	0
Bit 11	R/W	PRBS[18]	0
Bit 10	R/W	PRBS[17]	0
Bit 9	R/W	PRBS[16]	0
Bit 8	R/W	PRBS[15]	0
Bit 7	R/W	PRBS[14]	0
Bit 6	R/W	PRBS[13]	0
Bit 5	R/W	PRBS[12]	0
Bit 4	R/W	PRBS[11]	0
Bit 3	R/W	PRBS[10]	0
Bit 2	R/W	PRBS[9]	0
Bit 1	R/W	PRBS[8]	0
Bit 0	R/W	PRBS[7]	0

This register contains the definition of the WPP Indirect Data register (Register 071h) when accessing Indirect Address 9h (IADDR[3:0] is “9h” in register 070h).

For STS-Nc rates, only the first STS-1 has to be configured.

**PRBS[22:7]**

The PRBS[22:7] register are the 16 MSBs of the LFSR state of the STS-1/STM-0 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

**Register 071h (IADDR = Ah): WPP Generator PRBS[6:0] Accumulator**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	PRBS[6]	0
Bit 5	R/W	PRBS[5]	0
Bit 4	R/W	PRBS[4]	0
Bit 3	R/W	PRBS[3]	0
Bit 2	R/W	PRBS[2]	0
Bit 1	R/W	PRBS[1]	0
Bit 0	R/W	PRBS[0]	0

This register contains the definition of the WPP Indirect Data register (Register 071h) when accessing Indirect Address Ah (IADDR[3:0] is “Ah” in register 070h).

For STS-Nc rates, only the first STS-1 has to be configured.

**PRBS[6:0]**

The PRBS[6:0] register are the 7 LSBs of the LFSR state of the STS-1/STM-0 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

**Register 072h: WPP Generator Payload Configuration**

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	GEN_STS12C	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	GEN_STS3C[3]	0
Bit 2	R/W	GEN_STS3C[2]	0
Bit 1	R/W	GEN_STS3C[1]	0
Bit 0	R/W	GEN_STS3C[0]	0

This register configures the payload type of the time-slots in the Incoming bus for processing by the Working PRBS generator.

**GEN\_STS3C[0]**

The STS-3c/VC-4 payload configuration (GEN\_STS3C[0]) bit selects the payload configuration. When GEN\_STS3C[0] is set to logic 1, the STS-1/VC-3 paths #1, #5 and #9 are part of a STS-3c/VC-4 payload. When GEN\_STS3C[0] is set to logic 0, the paths are STS-1/VC-3 payloads. The GEN\_STS12C register bit has precedence over the GEN\_STS3C[0] register bit.

**GEN\_STS3C[1]**

The STS-3c/VC-4 payload configuration (GEN\_STS3C[1]) bit selects the payload configuration. When GEN\_STS3C[1] is set to logic 1, the STS-1/VC-3 paths #2, #6 and #10 are part of a STS-3c/VC-4 payload. When GEN\_STS3C[1] is set to logic 0, the paths are STS-1/VC-3 payloads. The GEN\_STS12C register bit has precedence over the GEN\_STS3C[1] register bit.

#### GEN\_STS3C[2]

The STS-3c/VC-4 payload configuration (GEN\_STS3C[2]) bit selects the payload configuration. When GEN\_STS3C[2] is set to logic 1, the STS-1/VC-3 paths #3, #7 and #11 are part of a STS-3c/VC-4 payload. When GEN\_STS3C[2] is set to logic 0, the paths are STS-1/VC-3 payloads. The GEN\_STS12C register bit has precedence over the GEN\_STS3C[2] register bit.

#### GEN\_STS3C[4]

The STS-3c/VC-4 payload configuration (GEN\_STS3C[3]) bit selects the payload configuration. When GEN\_STS3C[3] is set to logic 1, the STS-1/VC-3 paths #4, #8 and #12 are part of a STS-3c/VC-4 payload. When GEN\_STS3C[3] is set to logic 0, the paths are STS-1/VC-3 payloads. The GEN\_STS12C register bit has precedence over the GEN\_STS3C[3] register bit.

#### GEN\_STS12C

The STS-12c/VC-4-4c payload configuration (GEN\_STS12C) bit selects the payload configuration. When GEN\_STS12C is set to logic 1, the timeslots #1 to #12 are part of the same concatenated payload defined by GEN\_MSSLEN. When GEN\_STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the GEN\_STS3C[3:0] register bit. The GEN\_STS12C register bit has precedence over the GEN\_STS3C[3:0] register bit.

#### Reserved

The Reserved bits must be set low for correct operation of the SBSLITE.

**Register 073h: WPP Monitor Payload Configuration**

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	MON_STS12C	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	MON_STS3C[3]	0
Bit 2	R/W	MON_STS3C[2]	0
Bit 1	R/W	MON_STS3C[1]	0
Bit 0	R/W	MON_STS3C[0]	0

This register configures the payload type of the time-slots in the Receive Working Serial Link for processing by the PRBS monitor section.

**MON\_STS3C[0]**

The STS-3c/VC-4 payload configuration (MON\_STS3C[0]) bit selects the payload configuration. When MON\_STS3C[0] is set to logic 1, the STS-1/STM-0 paths #1, #5 and #9 are part of a STS-3c/VC-4 payload. When MON\_STS3C[0] is set to logic 0, the paths are STS-1/VC-3 payloads. The MON\_STS12C register bit has precedence over the MON\_STS3C[0] register bit.

**MON\_STS3C[1]**

The STS-3c/VC-4 payload configuration (MON\_STS3C[1]) bit selects the payload configuration. When MON\_STS3C[1] is set to logic 1, the STS-1/STM-0 paths #2, #6 and #10 are part of a STS-3c/VC-4 payload. When MON\_STS3C[1] is set to logic 0, the paths are STS-1/VC-3 payloads. The MON\_STS12C register bit has precedence over the MON\_STS3C[1] register bit.



**MON\_STS3C[2]**

The STS-3c/VC-4 payload configuration (MON\_STS3C[2]) bit selects the payload configuration. When MON\_STS3C[2] is set to logic 1, the STS-1/STM-0 paths #3, #7 and #11 are part of a MON\_STS-3c/VC-4 payload. When MON\_STS3C[2] is set to logic 0, the paths are STS-1 (VC-3) payloads. The MON\_STS12C register bit has precedence over the MON\_STS3C[2] register bit.

**MON\_STS3C[4]**

The STS-3c/VC-4 payload configuration (MON\_STS3C[3]) bit selects the payload configuration. When MON\_STS3C[3] is set to logic 1, the STS-1/STM-0 paths #4, #8 and #12 are part of a STS-3c/VC-4 payload. When MON\_STS3C[3] is set to logic 0, the paths are STS-1/VC-3 payloads. The MON\_STS12C register bit has precedence over the MON\_STS3C[3] register bit.

**Reserved**

The Reserved bits must be set low for correct operation of the SBSLITE.

**MON\_STS12C**

The STS-12c/VC-4-4c payload configuration (MON\_STS12C) bit selects the payload configuration. When MON\_STS12C is set to logic 1, the timeslots #1 to #12 are part of the same concatenated payload defined by MON\_MSSLEN. When MON\_STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the MON\_STS3C[3:0] register bit. The MON\_STS12C register bit has precedence over the MON\_STS3C[3:0] register bit.

**Register 074h: WPP Monitor Byte Error Interrupt Status**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_ERRI	X
Bit 10	R	MON11_ERRI	X
Bit 9	R	MON10_ERRI	X
Bit 8	R	MON9_ERRI	X
Bit 7	R	MON8_ERRI	X
Bit 6	R	MON7_ERRI	X
Bit 5	R	MON6_ERRI	X
Bit 4	R	MON5_ERRI	X
Bit 3	R	MON4_ERRI	X
Bit 2	R	MON3_ERRI	X
Bit 1	R	MON2_ERRI	X
Bit 0	R	MON1_ERRI	X

This register reports and acknowledges PRBS byte error interrupts for all the time-slots in the Receive Working Serial Link.

**MON<sub>x</sub>\_ERRI**

The Monitor Byte Error Interrupt Status register is the status of the interrupt generated by each of the 12 STS-1/STM-0 paths when an error has been detected. The MON<sub>x</sub>\_ERRI is set high when the monitor is in the synchronized state and when an error in a PRBS byte is detected in the STS-1/STM-0 path **x**. This bit is independent of MON<sub>x</sub>\_ERRE and is cleared after being read.

**Register 075h: WPP Monitor Byte Error Interrupt Enable**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	MON12_ERRE	0
Bit 10	R/W	MON11_ERRE	0
Bit 9	R/W	MON10_ERRE	0
Bit 8	R/W	MON9_ERRE	0
Bit 7	R/W	MON8_ERRE	0
Bit 6	R/W	MON7_ERRE	0
Bit 5	R/W	MON6_ERRE	0
Bit 4	R/W	MON5_ERRE	0
Bit 3	R/W	MON4_ERRE	0
Bit 2	R/W	MON3_ERRE	0
Bit 1	R/W	MON2_ERRE	0
Bit 0	R/W	MON1_ERRE	0

This register enables the assertion of PRBS byte error interrupts for all the time-slots in the Receive Working bus.

**MON<sub>x</sub>\_ERRE**

The Monitor Byte Error Interrupt Enable register enables the interrupt for each of the 12 STS-1/STM-0 paths. When MON<sub>x</sub>\_ERRE is set high it allows the Byte Error Interrupt to generate an external interrupt on INT.

**Register 079h: WPP Monitor Synchronization Interrupt Status**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_SYNCI	X
Bit 10	R	MON11_SYNCI	X
Bit 9	R	MON10_SYNCI	X
Bit 8	R	MON9_SYNCI	X
Bit 7	R	MON8_SYNCI	X
Bit 6	R	MON7_SYNCI	X
Bit 5	R	MON6_SYNCI	X
Bit 4	R	MON5_SYNCI	X
Bit 3	R	MON4_SYNCI	X
Bit 2	R	MON3_SYNCI	X
Bit 1	R	MON2_SYNCI	X
Bit 0	R	MON1_SYNCI	X

This register reports the PRBS monitor synchronization status change interrupts for all the time-slots in the Receive Working Serial Link.

**MON<sub>x</sub>\_SYNCI**

The Monitor Synchronization Interrupt Status register is set high when a change occurs in the monitor's synchronization status. Whenever a state machine of the **x** STS-1/STM-0 path goes from Synchronized to Out Of Synchronization state or vice-versa, the MON<sub>x</sub>\_SYNCI is set high. This bit is independent of MON<sub>x</sub>\_SYNCE and is cleared after it's been read.

**Register 07Ah: WPP Monitor Synchronization Interrupt Enable**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	MON12_SYNCE	0
Bit 10	R/W	MON11_SYNCE	0
Bit 9	R/W	MON10_SYNCE	0
Bit 8	R/W	MON9_SYNCE	0
Bit 7	R/W	MON8_SYNCE	0
Bit 6	R/W	MON7_SYNCE	0
Bit 5	R/W	MON6_SYNCE	0
Bit 4	R/W	MON5_SYNCE	0
Bit 3	R/W	MON4_SYNCE	0
Bit 2	R/W	MON3_SYNCE	0
Bit 1	R/W	MON2_SYNCE	0
Bit 0	R/W	MON1_SYNCE	0

This register enables the assertion of change of PRBS monitor synchronization status interrupts for all the time-slots in the Receive Working Serial Link.

**MON<sub>x</sub>\_SYNCE**

The Monitor Synchronization Interrupt Enable register allows each individual STS-1/STM-0 path to generate an external interrupt on INT. When MON<sub>x</sub>\_SYNCE is set high whenever a change occurs in the synchronization state of the monitor in STS-1/STM-0 path **x**, generates an interrupt on INT.

**Register 07Bh: WPP Monitor Synchronization State**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_SYNCV	X
Bit 10	R	MON11_SYNCV	X
Bit 9	R	MON10_SYNCV	X
Bit 8	R	MON9_SYNCV	X
Bit 7	R	MON8_SYNCV	X
Bit 6	R	MON7_SYNCV	X
Bit 5	R	MON6_SYNCV	X
Bit 4	R	MON5_SYNCV	X
Bit 3	R	MON4_SYNCV	X
Bit 2	R	MON3_SYNCV	X
Bit 1	R	MON2_SYNCV	X
Bit 0	R	MON1_SYNCV	X

This register reports the state of the PRBS monitors for all the time-slots in the Receive Working Serial Link.

**MON<sub>x</sub>\_SYNCV**

The Monitor Synchronization Status register reflects the state of the monitor's state machine. When MON<sub>x</sub>\_SYNCV is set high the monitor's state machine is in synchronization for the STS-1/STM-0 Path **x**. When MON<sub>x</sub>\_SYNCV is low the monitor is NOT in synchronization for the STS-1/STM-0 Path **x**.

When checking the state of MON<sub>x</sub>\_SYNCV, you must also check the state of the WPP Monitor PRBS Accumulator Registers (Register 071H with IADDR=1H and 2H) of the associated STS-1/STM-0. If the value of MON<sub>x</sub>\_SYNCV is a logic 1 and the value in the PRBS register is all zeros, then the associated STS-1/STM-0 path is NOT in synchronization. If the value of MON<sub>x</sub>\_SYNCV is a logic 1 and the value in the PRBS register is non-zero, then the associated STS-1/STM-0 path is IN synchronization.

**Register 07Ch: WPP Performance Counters Transfer Trigger**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	TIP	0

This register controls and monitors the reporting of the error counter registers.

A write in this register will trigger the transfer of the error counters to holding registers where they can be read. The value written in the register is not important. Once the transfer is initiated, the TIP bit is set high, and when the holding registers contain the value of the error counters, TIP is set low.

**TIP**

The Transfer In Progress bit reflects the state of the TIP output signal. When TIP is high, an error counter transfer has been initiated, but the counters are not transferred in the holding register yet. When TIP is low, the value of the error counters is available to be read in the holding registers. This bit can be poll after an error counters transfer request, to determine if the counters are ready to be read.

**Register 080h: PPP Indirect Address**

Bit	Type	Function	Default
Bit 15	R	BUSY	0
Bit 14	R/W	RDWRB	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

This register provides selection of configuration pages and of the time-slots to be accessed in the PPP block. Writing to this register triggers an indirect register access.

**PATH[3:0]**

The PATH[3:0] bits select which time-multiplexed division is accessed by the current indirect transfer.

PATH[3:0]	Time Division #
0000	Invalid STS-1/STM-0 path
0001-1100	STS-1/STM-0 path #1 to STS-1/STM-0 path #12
1101-1111	Invalid STS-1/STM-0 path

**IADDR[3:0]**

The internal RAM page bits select which page of the internal RAM is access by the current indirect transfer. Six pages are defined for the monitor (IADDR[3] = '0') : the configuration page, the PRBS[22:7] page, the PRBS[6:0] page, the B1/E1 value page, the Monitor error count page and the received B1/E1 byte.

IADDR[3:0]	RAM page
0000	STS-1/STM-0 path Configuration page
0001	PRBS[22:7] page



IADDR[3:0]	RAM page
0010	PRBS[6:0] page
0011	Reserved
0100	Monitor error count page
0101	Reserved

Four pages are defined for the generator (IADDR [3] = '1'): the configuration page, the PRBS[22:7] page, the PRBS[6:0] page and the B1/E1 value.

IADDR[3:0]	RAM page
1000	STS-1/STM-0 path Configuration page
1001	PRBS[22:7] page
1010	PRBS[6:0] page
1011	Reserved

#### RDWRB

The active high read and active low write (RDWRB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RDWRB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transfer to the Indirect Data Register. When RDWRB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transfer to the addressed location in the internal RAM.

#### BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

**Register 081h: PPP Indirect Data**

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

This register contains the data read from the internal RAM after an indirect read operation or the data to be inserted into the internal RAM in an indirect write operation.

**DATA[15:0]**

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RDWRB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transfer to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RDWRB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which page of the internal RAM is being accessed.

**Register 081h (IADDR = 0h): PPP Monitor STS-1/STM-0 path Configuration**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	SEQ_PRBSB	0
Bit 5	R/W	Reserved	0
Bit 4		Unused	X
Bit 3	W	RESYNC	0
Bit 2	R/W	INV_PRBS	0
Bit 1	R/W	AMODE	0
Bit 0	R/W	MON_ENA	0

This register contains the definition of the PPP Indirect Data register (Register 081h) when accessing Indirect Address 0h (IADDR[3:0] is "0h" in register 080h).

For STS-Nc rates, only the first STS-1 has to be configured

**MON\_ENA**

Monitor Enable register bit, enables the PRBS monitor for the STS-1/STM-0 path specified in the PATH[3:0] of register 050h (TPP Indirect Address). If MON\_ENA is set to '1', a PRBS sequence is generated and compare to the incoming one inserted in the payload of the SONET/SDH frame. If MON\_ENA is low, the data at the input of the monitor is ignored.

**AMODE**

If AMODE is high, the monitor is in Autonomous mode, and the incoming SONET/SDH payload is compared to the internally generated one. In Autonomous mode, the beginning of the SPE is always place next to the H3 byte (zero offset), so the J1 pulses are ignored. When using the PPP in TelecomBus mode, this bit must be set high. When using the PPP in SBI mode, this bit must be set low.

**INV\_PRBS**

This sets the monitor to invert the PRBS before comparing it to the internally generated payload. When set high, the PRBS bytes will be inverted, else they will be compared unmodified.

#### RESYNC

This sets the monitor to re-initialize the PRBS sequence. When set high the monitor's state machine will be forced in the Out Of Sync state and automatically try to resynchronize to the incoming stream.

#### SEQ\_PRBSB

This bit enables the monitoring of a PRBS or sequential pattern inserted in the payload. When low the payload contains PRBS bytes, and when high, a sequential pattern is monitored.

#### Reserved

The reserved bits must be set low for correct operation of the SBSLITE.

**Register 081h (IADDR = 1h): PPP Monitor PRBS[22:7] Accumulator**

Bit	Type	Function	Default
Bit 15	R/W	PRBS[22]	0
Bit 14	R/W	PRBS[21]	0
Bit 13	R/W	PRBS[20]	0
Bit 12	R/W	PRBS[19]	0
Bit 11	R/W	PRBS[18]	0
Bit 10	R/W	PRBS[17]	0
Bit 9	R/W	PRBS[16]	0
Bit 8	R/W	PRBS[15]	0
Bit 7	R/W	PRBS[14]	0
Bit 6	R/W	PRBS[13]	0
Bit 5	R/W	PRBS[12]	0
Bit 4	R/W	PRBS[11]	0
Bit 3	R/W	PRBS[10]	0
Bit 2	R/W	PRBS[9]	0
Bit 1	R/W	PRBS[8]	0
Bit 0	R/W	PRBS[7]	0

This register contains the definition of the PPP Indirect Data register (Register 081h) when accessing Indirect Address 1h (IADDR[3:0] is "1h" in register 080h).

For STS-Nc rates, only the first STS-1 has to be configured.

**PRBS[22:7]**

The PRBS[22:7] register are the 16 MSBs of the LFSR state of the STS-1/STM-0 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

**Register 081h (IADDR = 2h): PPP Monitor PRBS[6:0] Accumulator**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	PRBS[6]	0
Bit 5	R/W	PRBS[5]	0
Bit 4	R/W	PRBS[4]	0
Bit 3	R/W	PRBS[3]	0
Bit 2	R/W	PRBS[2]	0
Bit 1	R/W	PRBS[1]	0
Bit 0	R/W	PRBS[0]	0

This register contains the definition of the PPP Indirect Data register (Register 081h) when accessing Indirect Address 2h (IADDR[3:0] is “2h” in register 080h).

For STS-Nc rates, only the first STS-1 has to be configured.

**PRBS[6:0]**

The PRBS[6:0] register are the 7 LSBs of the LFSR state of the STS-1/STM-0 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

**Register 081h (IADDR = 4h): PPP Monitor Error count**

Bit	Type	Function	Default
Bit 15	R	ERR_CNT[15]	X
Bit 14	R	ERR_CNT[14]	X
Bit 13	R	ERR_CNT[13]	X
Bit 12	R	ERR_CNT[12]	X
Bit 11	R	ERR_CNT[11]	X
Bit 10	R	ERR_CNT[10]	X
Bit 9	R	ERR_CNT[9]	X
Bit 8	R	ERR_CNT[8]	X
Bit 7	R	ERR_CNT[7]	X
Bit 6	R	ERR_CNT[6]	X
Bit 5	R	ERR_CNT[5]	X
Bit 4	R	ERR_CNT[4]	X
Bit 3	R	ERR_CNT[3]	X
Bit 2	R	ERR_CNT[2]	X
Bit 1	R	ERR_CNT[1]	X
Bit 0	R	ERR_CNT[0]	X

This register contains the definition of the PPP Indirect Data register (Register 061h) when accessing Indirect Address 4h (IADDR[3:0] is “4h” in register 060h).

**ERR\_CNT[15:0]**

The ERR\_CNT[15:0] register contains the cumulative number of errors in the PRBS bytes since the last error reporting event. Errors are accumulated only when the monitor is in the synchronized state. Each PRBS byte will only contribute a single error, even if there are multiple errors within a single PRBS byte. The transfer of the error counter to this holding register is triggered by writing to the PPP Performance Counters Transfer Trigger Register (08CH) or by writing the SBSLITE Master Signal Monitor #1, Accumulation Trigger Register (014H). The error counter is cleared and restarted after its value is transferred to the ERR\_CNT[15:0] holding register. No errors are missed during the transfer. The error counter will not wrap around after reaching FFFFh, it will saturate at this value.

**Register 081h (IADDR = 8h): PPP Generator STS-1/STM-0 path Configuration**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	Reserved	0
Bit 12	R/W	LINKENA	0
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	Reserved	X
Bit 8	R/W	LINKENA	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	SEQ_PRBSB	0
Bit 4	R/W	Reserved	0
Bit 3	W	FORCE_ERR	0
Bit 2		Unused	
Bit 1	R/W	INV_PRBS	0
Bit 0	R/W	AMODE	0

This register contains the definition of the PPP Indirect Data register (Register 081h) when accessing Indirect Address 8h (IADDR[3:0] is “8h” in register 080h).

For STS-Nc rates, only the first STS-1 has to be configured.

**AMODE**

If AMODE is high, the generator is in Autonomous mode, and the SONET/SDH frame is generated using only the C1 pulse. The payload frame (J1) is at a fixed alignment as no pointer movements are generated. When using the PPP in TelecomBus mode, this bit must be set high. When using the PPP in SBI mode, this bit must be set low.

**INV\_PRBS**

Sets the generator to invert the PRBS before inserting it in the payload. When set high, the PRBS bytes will be inverted, else they will be inserted unmodified.

**FORCE\_ERR**

The Force Error bit is used to force bit errors in the inserted pattern. When a logic one is written, the MSB of the next byte will be inverted, inducing a single bit error. The register clears itself when the operation is complete.



#### SEQ\_PRBSB

This bit enables the insertion of a PRBS sequence or a sequential pattern in the payload. When low, the payload is filled with PRBS bytes, and when high, a sequential pattern is inserted.

#### LINKENA

These two bits specify if PRBS is to be inserted in the path through the TP8E. If LINKENA is high patterns are generated in the SONET/SDH frame to the TP8E, else no pattern is generated and the unmodified SONET/SDH input frame is passed to the TP8E.

#### Reserved

The reserved bits must be set low for correct operation of the SBSLITE.

**Register 081h (IADDR = 9h): PPP Generator PRBS[22:7] Accumulator**

Bit	Type	Function	Default
Bit 15	R/W	PRBS[22]	0
Bit 14	R/W	PRBS[21]	0
Bit 13	R/W	PRBS[20]	0
Bit 12	R/W	PRBS[19]	0
Bit 11	R/W	PRBS[18]	0
Bit 10	R/W	PRBS[17]	0
Bit 9	R/W	PRBS[16]	0
Bit 8	R/W	PRBS[15]	0
Bit 7	R/W	PRBS[14]	0
Bit 6	R/W	PRBS[13]	0
Bit 5	R/W	PRBS[12]	0
Bit 4	R/W	PRBS[11]	0
Bit 3	R/W	PRBS[10]	0
Bit 2	R/W	PRBS[9]	0
Bit 1	R/W	PRBS[8]	0
Bit 0	R/W	PRBS[7]	0

This register contains the definition of the PPP Indirect Data register (Register 081h) when accessing Indirect Address 9h (IADDR[3:0] is “9h” in register 080h).

For STS-Nc rates, only the first STS-1 has to be configured.

**PRBS[22:7]**

The PRBS[22:7] register are the 16 MSBs of the LFSR state of the STS-1/STM-0 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

**Register 081h (IADDR = Ah): PPP Generator PRBS[6:0] Accumulator**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	PRBS[6]	0
Bit 5	R/W	PRBS[5]	0
Bit 4	R/W	PRBS[4]	0
Bit 3	R/W	PRBS[3]	0
Bit 2	R/W	PRBS[2]	0
Bit 1	R/W	PRBS[1]	0
Bit 0	R/W	PRBS[0]	0

This register contains the definition of the PPP Indirect Data register (Register 081h) when accessing Indirect Address Ah (IADDR[3:0] is “Ah” in register 080h).

For STS-Nc rates, only the first STS-1 has to be configured.

**PRBS[6:0]**

The PRBS[6:0] register are the 7 LSBs of the LFSR state of the STS-1/STM-0 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

**Register 082h: PPP Generator Payload Configuration**

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	GEN_STS12C	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	GEN_STS3C[3]	0
Bit 2	R/W	GEN_STS3C[2]	0
Bit 1	R/W	GEN_STS3C[1]	0
Bit 0	R/W	GEN_STS3C[0]	0

This register configures the payload type of the time-slots in the Incoming bus for processing by the Protect PRBS generator.

**GEN\_STS3C[0]**

The STS-3c/VC-4 payload configuration (GEN\_STS3C[0]) bit selects the payload configuration. When GEN\_STS3C[0] is set to logic 1, the STS-1/VC-3 paths #1, #5 and #9 are part of a STS-3c/VC-4 payload. When GEN\_STS3C[0] is set to logic 0, the paths are STS-1/VC-3 payloads. The GEN\_STS12C register bit has precedence over the GEN\_STS3C[0] register bit.

**GEN\_STS3C[1]**

The STS-3c/VC-4 payload configuration (GEN\_STS3C[1]) bit selects the payload configuration. When GEN\_STS3C[1] is set to logic 1, the STS-1/VC-3 paths #2, #6 and #10 are part of a STS-3c/VC-4 payload. When GEN\_STS3C[1] is set to logic 0, the paths are STS-1/VC-3 payloads. The GEN\_STS12C register bit has precedence over the GEN\_STS3C[1] register bit.

#### GEN\_STS3C[2]

The STS-3c/VC-4 payload configuration (GEN\_STS3C[2]) bit selects the payload configuration. When GEN\_STS3C[2] is set to logic 1, the STS-1/VC-3 paths #3, #7 and #11 are part of a STS-3c/VC-4 payload. When GEN\_STS3C[2] is set to logic 0, the paths are STS-1/VC-3 payloads. The GEN\_STS12C register bit has precedence over the GEN\_STS3C[2] register bit.

#### GEN\_STS3C[4]

The STS-3c/VC-4 payload configuration (GEN\_STS3C[3]) bit selects the payload configuration. When GEN\_STS3C[3] is set to logic 1, the STS-1/VC-3 paths #4, #8 and #12 are part of a STS-3c/VC-4 payload. When GEN\_STS3C[3] is set to logic 0, the paths are STS-1/VC-3 payloads. The GEN\_STS12C register bit has precedence over the GEN\_STS3C[3] register bit.

#### GEN\_STS12C

The STS-12c/VC-4-4c payload configuration (GEN\_STS12C) bit selects the payload configuration. When GEN\_STS12C is set to logic 1, the timeslots #1 to #12 are part of the same concatenated payload defined by GEN\_MSSLEN. When GEN\_STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the GEN\_STS3C[3:0] register bit. The GEN\_STS12C register bit has precedence over the GEN\_STS3C[3:0] register bit.

#### Reserved

The Reserved bits must be set low for correct operation of the SBSLITE.

**Register 083h: PPP Monitor Payload Configuration**

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	MON_STS12C	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	MON_STS3C[3]	0
Bit 2	R/W	MON_STS3C[2]	0
Bit 1	R/W	MON_STS3C[1]	0
Bit 0	R/W	MON_STS3C[0]	0

This register configures the payload type of the time-slots in the Receive Protection Serial Link for processing by the PRBS monitor section.

**MON\_STS3C[0]**

The STS-3c/VC-4 payload configuration (MON\_STS3C[0]) bit selects the payload configuration. When MON\_STS3C[0] is set to logic 1, the STS-1/STM-0 paths #1, #5 and #9 are part of a STS-3c/VC-4 payload. When MON\_STS3C[0] is set to logic 0, the paths are STS-1/VC-3 payloads. The MON\_STS12C register bit has precedence over the MON\_STS3C[0] register bit.

**MON\_STS3C[1]**

The STS-3c/VC-4 payload configuration (MON\_STS3C[1]) bit selects the payload configuration. When MON\_STS3C[1] is set to logic 1, the STS-1/STM-0 paths #2, #6 and #10 are part of a STS-3c/VC-4 payload. When MON\_STS3C[1] is set to logic 0, the paths are STS-1/VC-3 payloads. The MON\_STS12C register bit has precedence over the MON\_STS3C[1] register bit.

**MON\_STS3C[2]**

The STS-3c/VC-4 payload configuration (MON\_STS3C[2]) bit selects the payload configuration. When MON\_STS3C[2] is set to logic 1, the STS-1/STM-0 paths #3, #7 and #11 are part of a MON\_STS-3c/VC-4 payload. When MON\_STS3C[2] is set to logic 0, the paths are STS-1 (VC-3) payloads. The MON\_STS12C register bit has precedence over the MON\_STS3C[2] register bit.

**MON\_STS3C[4]**

The STS-3c/VC-4 payload configuration (MON\_STS3C[3]) bit selects the payload configuration. When MON\_STS3C[3] is set to logic 1, the STS-1/STM-0 paths #4, #8 and #12 are part of a STS-3c/VC-4 payload. When MON\_STS3C[3] is set to logic 0, the paths are STS-1/VC-3 payloads. The MON\_STS12C register bit has precedence over the MON\_STS3C[3] register bit.

**MON\_STS12C**

The STS-12c/VC-4-4c payload configuration (MON\_STS12C) bit selects the payload configuration. When MON\_STS12C is set to logic 1, the timeslots #1 to #12 are part of the same concatenated payload defined by MON\_MSSLEN. When MON\_STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the MON\_STS3C[3:0] register bit. The MON\_STS12C register bit has precedence over the MON\_STS3C[3:0] register bit.

**Reserved**

The Reserved bits must be set low for correct operation of the SBSLITE.

**Register 084h: PPP Monitor Byte Error Interrupt Status**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_ERRI	X
Bit 10	R	MON11_ERRI	X
Bit 9	R	MON10_ERRI	X
Bit 8	R	MON9_ERRI	X
Bit 7	R	MON8_ERRI	X
Bit 6	R	MON7_ERRI	X
Bit 5	R	MON6_ERRI	X
Bit 4	R	MON5_ERRI	X
Bit 3	R	MON4_ERRI	X
Bit 2	R	MON3_ERRI	X
Bit 1	R	MON2_ERRI	X
Bit 0	R	MON1_ERRI	X

This register reports and acknowledges PRBS byte error interrupts for all the time-slots in the Receive Protection Serial Link.

**MON<sub>x</sub>\_ERRI**

The Monitor Byte Error Interrupt Status register is the status of the interrupt generated by each of the 12 STS-1/STM-0 paths when an error has been detected. The MON<sub>x</sub>\_ERRI is set high when the monitor is in the synchronized state and when an error in a PRBS byte is detected in the STS-1/STM-0 path **x**. This bit is independent of MON<sub>x</sub>\_ERRE and is cleared after being read.



**Register 085h: PPP Monitor Byte Error Interrupt Enable**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	MON12_ERRE	0
Bit 10	R/W	MON11_ERRE	0
Bit 9	R/W	MON10_ERRE	0
Bit 8	R/W	MON9_ERRE	0
Bit 7	R/W	MON8_ERRE	0
Bit 6	R/W	MON7_ERRE	0
Bit 5	R/W	MON6_ERRE	0
Bit 4	R/W	MON5_ERRE	0
Bit 3	R/W	MON4_ERRE	0
Bit 2	R/W	MON3_ERRE	0
Bit 1	R/W	MON2_ERRE	0
Bit 0	R/W	MON1_ERRE	0

This register enables the assertion of PRBS byte error interrupts for all the time-slots in the Receive Protection Serial Link.

**MON<sub>x</sub>\_ERRE**

The Monitor Byte Error Interrupt Enable register enables the interrupt for each of the 12 STS-1/STM-0 paths. When MON<sub>x</sub>\_ERRE is set high it allows the Byte Error Interrupt to generate an external interrupt on INT.

**Register 089h: PPP Monitor Synchronization Interrupt Status**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_SYNCI	X
Bit 10	R	MON11_SYNCI	X
Bit 9	R	MON10_SYNCI	X
Bit 8	R	MON9_SYNCI	X
Bit 7	R	MON8_SYNCI	X
Bit 6	R	MON7_SYNCI	X
Bit 5	R	MON6_SYNCI	X
Bit 4	R	MON5_SYNCI	X
Bit 3	R	MON4_SYNCI	X
Bit 2	R	MON3_SYNCI	X
Bit 1	R	MON2_SYNCI	X
Bit 0	R	MON1_SYNCI	X

This register reports the PRBS monitor synchronization status change interrupts for all the time-slots in the Receive Protection Serial Link.

**MON<sub>x</sub>\_SYNCI**

The Monitor Synchronization Interrupt Status register is set high when a change occurs in the monitor's synchronization status. Whenever a state machine of the **x** STS-1/STM-0 path goes from Synchronized to Out Of Synchronization state or vice-versa, the MON<sub>x</sub>\_SYNCI is set high. This bit is independent of MON<sub>x</sub>\_SYNCE and is cleared after it's been read.

**Register 08Ah: PPP Monitor Synchronization Interrupt Enable**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	MON12_SYNCE	0
Bit 10	R/W	MON11_SYNCE	0
Bit 9	R/W	MON10_SYNCE	0
Bit 8	R/W	MON9_SYNCE	0
Bit 7	R/W	MON8_SYNCE	0
Bit 6	R/W	MON7_SYNCE	0
Bit 5	R/W	MON6_SYNCE	0
Bit 4	R/W	MON5_SYNCE	0
Bit 3	R/W	MON4_SYNCE	0
Bit 2	R/W	MON3_SYNCE	0
Bit 1	R/W	MON2_SYNCE	0
Bit 0	R/W	MON1_SYNCE	0

This register enables the assertion of change of PRBS monitor synchronization status interrupts for all the time-slots in the Receive Protection Serial Link.

**MON<sub>x</sub>\_SYNCE**

The Monitor Synchronization Interrupt Enable register allows each individual STS-1/STM-0 path to generate an external interrupt on INT. When MON<sub>x</sub>\_SYNCE is set high whenever a change occurs in the synchronization state of the monitor in STS-1/STM-0 path **x**, generates an interrupt on INT.

**Register 08Bh: PPP Monitor Synchronization State**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_SYNCV	X
Bit 10	R	MON11_SYNCV	X
Bit 9	R	MON10_SYNCV	X
Bit 8	R	MON9_SYNCV	X
Bit 7	R	MON8_SYNCV	X
Bit 6	R	MON7_SYNCV	X
Bit 5	R	MON6_SYNCV	X
Bit 4	R	MON5_SYNCV	X
Bit 3	R	MON4_SYNCV	X
Bit 2	R	MON3_SYNCV	X
Bit 1	R	MON2_SYNCV	X
Bit 0	R	MON1_SYNCV	X

This register reports the state of the PRBS monitors for all the time-slots in the Receive Protection Serial Link.

**MON<sub>x</sub>\_SYNCV**

The Monitor Synchronization Status register reflects the state of the monitor's state machine. When MON<sub>x</sub>\_SYNCV is set high the monitor's state machine is in synchronization for the STS-1/STM-0 Path **x**. When MON<sub>x</sub>\_SYNCV is low the monitor is NOT in synchronization for the STS-1/STM-0 Path **x**.

When checking the state of MON<sub>x</sub>\_SYNCV, you must also check the state of the PPP Monitor PRBS Accumulator Registers (Register 081H with IADDR=1H and 2H) of the associated STS-1/STM-0. If the value of MON<sub>x</sub>\_SYNCV is a logic 1 and the value in the PRBS register is all zeros, then the associated STS-1/STM-0 path is NOT in synchronization. If the value of MON<sub>x</sub>\_SYNCV is a logic 1 and the value in the PRBS register is non-zero, then the associated STS-1/STM-0 path is IN synchronization.

**Register 08Ch: PPP Performance Counters Transfer Trigger**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	TIP	0

This register controls and monitors the reporting of the error counter registers.

A write in this register will trigger the transfer of the error counters to holding registers where they can be read. The value written in the register is not important. Once the transfer is initiated, the TIP bit is set high, and when the holding registers contain the value of the error counters, TIP is set low.

**TIP**

The Transfer In Progress bit reflects the state of the TIP output signal. When TIP is high, an error counter transfer has been initiated, but the counters are not transferred in the holding register yet. When TIP is low, the value of the error counters is available to be read in the holding registers. This bit can be poll after an error counters transfer request, to determine if the counters are ready to be read.

**Register 090H: WILC Transmit FIFO Data High**

Bit	Type	Function	Default
Bit 15	R/W	TDAT[31:16]	0
Bit 14	R/W	TDAT[31:16]	0
Bit 13	R/W	TDAT[31:16]	0
Bit 12	R/W	TDAT[31:16]	0
Bit 11	R/W	TDAT[31:16]	0
Bit 10	R/W	TDAT[31:16]	0
Bit 9	R/W	TDAT[31:16]	0
Bit 8	R/W	TDAT[31:16]	0
Bit 7	R/W	TDAT[31:16]	0
Bit 6	R/W	TDAT[31:16]	0
Bit 5	R/W	TDAT[31:16]	0
Bit 4	R/W	TDAT[31:16]	0
Bit 3	R/W	TDAT[31:16]	0
Bit 2	R/W	TDAT[31:16]	0
Bit 1	R/W	TDAT[31:16]	0
Bit 0	R/W	TDAT[31:16]	0

When writing data to the transmit FIFO, this register must be written to before register 091H.

**TDAT[31:16]**

TDAT[31:16] and TDAT[15:0] form the 32 bit wide data word to be written to the FIFO. The FIFO is organized as 32 bits wide and 64 words deep, giving a total of eight 32 byte messages.

**Register 091H: WILC Transmit FIFO Data Low**

Bit	Type	Function	Default
Bit 15	R/W	TDAT[15:0]	0
Bit 14	R/W	TDAT[15:0]	0
Bit 13	R/W	TDAT[15:0]	0
Bit 12	R/W	TDAT[15:0]	0
Bit 11	R/W	TDAT[15:0]	0
Bit 10	R/W	TDAT[15:0]	0
Bit 9	R/W	TDAT[15:0]	0
Bit 8	R/W	TDAT[15:0]	0
Bit 7	R/W	TDAT[15:0]	0
Bit 6	R/W	TDAT[15:0]	0
Bit 5	R/W	TDAT[15:0]	0
Bit 4	R/W	TDAT[15:0]	0
Bit 3	R/W	TDAT[15:0]	0
Bit 2	R/W	TDAT[15:0]	0
Bit 1	R/W	TDAT[15:0]	0
Bit 0	R/W	TDAT[15:0]	0

Writing to this register will initiate a transfer of TDAT[31:0] into the transmit FIFO.

**TDAT[15:0]**

TDAT[31:16] and TDAT[15:0] form the 32 bit wide data word to be written to the FIFO. The FIFO is organized as 32 bits wide and 64 words deep, giving a total of eight 32 byte messages.

**Register 093H: WILC Transmit Control Register**

Bit	Type	Function	Default
Bit 15	R/W	TX_AUX[7:0]	0
Bit 14	R/W	TX_AUX[7:0]	0
Bit 13	R/W	TX_AUX[7:0]	0
Bit 12	R/W	TX_AUX[7:0]	0
Bit 11	R/W	TX_AUX[7:0]	0
Bit 10	R/W	TX_AUX[7:0]	0
Bit 9	R/W	TX_AUX[7:0]	0
Bit 8	R/W	TX_AUX[7:0]	0
Bit 7	R	Unused	0
Bit 6	R	Unused	0
Bit 5	R/W	TX_LINK[1:0]	0
Bit 4	R/W	TX_LINK[1:0]	0
Bit 3	R	Unused	0
Bit 2	R	Unused	0
Bit 1	R/W	TX_CRC_SWIZ_EN	0
Bit 0	R/W	TX_BYPASS	0

**TX\_BYPASS**

When this bit is set to '1', the blocks message transmit functions are bypassed. No messages are inserted into the Transmit data. The transmit message FIFO RAM is disabled and thus message data writes are ignored.

**TX\_CRC\_SWIZ\_EN**

When this bit is set to '1', the calculated CRC-16 is bit reversed before being transmitted. This facility can be used for diagnostic testing of CRC-16 generation and checking functionality.

**TX\_LINK[1:0]**

These bits are transmitted in the LINK bits of the message header of the next available message. On reads these bit return the last written value.



### TX\_AUX[7:0]

These bits form the input to an Auxiliary channel between CPUs at each end of the link. Their use is at the Software developer's discretion. Data written to this register will be transmitted in the AUX header byte of each subsequent message to the other end of the in-band link. A new value of TX\_AUX will be transmitted at the next available message. Data read from this register will be the data previously written.

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**Register 095H: WILC Transmit Status and FIFO Synch Register**

Bit	Type	Function	Default
Bit 15	R	TX_MSG_LVL_VALID	X
Bit 14	R	TX_LINK[1:0]	0
Bit 13	R	TX_LINK[1:0]	0
Bit 12	R	IPAGE[1:0]	X
Bit 11	R	IPAGE[1:0]	X
Bit 10	R	IUSER[2:0]	X
Bit 9	R	IUSER[2:0]	0
Bit 8	R	IUSER[2:0]	0
Bit 7	R	Unused	0
Bit 6	R	Unused	0
Bit 5	R	TX_MSG_LVL[3:0]	0
Bit 4	R	TX_MSG_LVL[3:0]	0
Bit 3	R	TX_MSG_LVL[3:0]	0
Bit 2	R	TX_MSG_LVL[3:0]	0
Bit 1	R	TX_FI_BUSY	0
Bit 0	W	TX_XFER_SYNC	0

**TX\_XFER\_SYNC**

Writing '1' to this bit initializes the next write sequence to be to the beginning of the next message. After a '1' had been written successive writes to the Transmit FIFO will be to location zero of the next available slot. If a partial message has been written, TX\_XFER\_SYNC indicates that the current message is complete and that subsequent writes will be to the next message. If more than 32 bytes are written, the 33rd byte will be the first byte of the next message. The purpose of this bit is to unambiguously align the message boundaries. Another use would be to abandon the current write and move the write pointer to the beginning of the next message. (Previous message data will remain in the unwritten portion of the message being abandoned, which will have to be ignored by the receiving software).

If the message FIFO pointers are already at a message boundary then writing this bit to a '1' will have no affect.

On reads this bit is always returned as a '0'.

**TX\_FI\_BUSY**

This bit indicates that the internal hardware is transferring the data from the Transmit FIFO registers (TDAT) into the internal RAM. This bit need not be read by software if the time interval between successive 32 bit transfers is greater than 3 SYSCLK cycles.

### TX\_MSG\_LVL[3:0]

This indicates the current number of messages in the TXFIFO.

TX_MSG_LVL[3:0]	Number of Messages
0000	0
:	:
1000	8

Values greater than 1000 will not occur. The number of free messages available in the FIFO is given by  $8 - \text{TX\_MSG\_LVL}$ . The TX\_MSG\_LVL\_VALID bit must be polled before reading these bits.

### IUSER[2:0]

These bits are a reflection of the USER[2:0] bits output in the header of the in-band link on the Transmit Working Serial Link. IUSER[2] is sourced from the IUSER2 input to the SBSLITE. IUSER[1:0] is sourced from the TXWUSER[1:0] bits of register 008H.

### IPAGE[1:0]

These bits are a reflection of the PAGE[1:0] bits output in the header of the in-band link on the Transmit Working Serial Link. PAGE[1] reflects the current memory page used by the IMSU. PAGE[0] reflects the current memory page used by the OMSU.

### TX\_LINK[1:0]

These bits reflect the last written value of the TX\_LINK[1:0] field of the WILC Transmit Control Register. The upper byte of this register therefore reflects all of the configurable bits of the message Header1 byte.

### TX\_MSG\_LVL\_VALID

This bit indicates that the value of TX\_MSG\_LVL is valid. When read with a logic 0 this register should be re-read until TX\_MSG\_LVL\_VALID is a logic 1. This bit will be clear for only approximately 0.12% of the time. This bit must always be polled before reading the TX\_MSG\_LVL bits.

**Register 096H: WILC Receive FIFO Data High**

Bit	Type	Function	Default
Bit 15	R	RDAT[31:16]	0
Bit 14	R	RDAT[31:16]	0
Bit 13	R	RDAT[31:16]	0
Bit 12	R	RDAT[31:16]	0
Bit 11	R	RDAT[31:16]	0
Bit 10	R	RDAT[31:16]	0
Bit 9	R	RDAT[31:16]	0
Bit 8	R	RDAT[31:16]	0
Bit 7	R	RDAT[31:16]	0
Bit 6	R	RDAT[31:16]	0
Bit 5	R	RDAT[31:16]	0
Bit 4	R	RDAT[31:16]	0
Bit 3	R	RDAT[31:16]	0
Bit 2	R	RDAT[31:16]	0
Bit 1	R	RDAT[31:16]	0
Bit 0	R	RDAT[31:16]	0

When reading data out of the receive FIFO, this register must be read before register 097H.

**RDAT[31:16]**

RDAT[31:16] and RDAT[15:0] form the 32 bit wide data word read from the FIFO. The FIFO is organized as 32 bits wide and 64 words deep, giving a total of eight 32 byte messages. This register must be read before register 097H.

**Register 097H: WILC Receive FIFO Data Low**

Bit	Type	Function	Default
Bit 15	R	RDAT[15:0]	0
Bit 14	R	RDAT[15:0]	0
Bit 13	R	RDAT[15:0]	0
Bit 12	R	RDAT[15:0]	0
Bit 11	R	RDAT[15:0]	0
Bit 10	R	RDAT[15:0]	0
Bit 9	R	RDAT[15:0]	0
Bit 8	R	RDAT[15:0]	0
Bit 7	R	RDAT[15:0]	0
Bit 6	R	RDAT[15:0]	0
Bit 5	R	RDAT[15:0]	0
Bit 4	R	RDAT[15:0]	0
Bit 3	R	RDAT[15:0]	0
Bit 2	R	RDAT[15:0]	0
Bit 1	R	RDAT[15:0]	0
Bit 0	R	RDAT[15:0]	0

Reading this register initiates a read access to the next location in the receive FIFO.

**RDAT[15:0]**

RDAT[31:16] and RDAT[15:0] form the 32 bit wide data word read from the FIFO. The FIFO is organized as 32 bits wide and 64 words deep, giving a total of eight 32 byte messages.

**Register 099H: WILC Receive FIFO Control Register**

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R	Unused	0
Bit 8	R	Unused	0
Bit 7	R	Unused	0
Bit 6	R	Unused	0
Bit 5	R	Unused	0
Bit 4	R	Unused	0
Bit 3	R	Unused	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	RX_CRC_SWIZ_EN	0
Bit 0	R/W	RX_BYPASS	0

**RX\_BYPASS**

When this bit is set to a logic 1. The WILC's message receive functions are bypassed and no messages are extracted from the Receive Working Serial Link. The receive message FIFO RAM is disabled and thus message data reads will return undefined data.

**RX\_CRC\_SWIZ\_EN**

When this bit is set to a logic 1, the calculated CRC-16 is bit reversed before being compared with CRC-16 bytes of the received message. This facility can be used for diagnostic testing of CRC-16 generation and checking functionality

**Reserved:**

This bit should be set to a logic 1 for proper operation of the WILC.

**Register 09AH: WILC Receive Auxiliary Register**

Bit	Type	Function	Default
Bit 15	R	RX_STTS_VALID	X
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 19	R	Unused	0
Bit 8	R	Unused	0
Bit 7	R	RX_AUX[7:0]	0
Bit 6	R	RX_AUX[7:0]	0
Bit 5	R	RX_AUX[7:0]	0
Bit 4	R	RX_AUX[7:0]	0
Bit 3	R	RX_AUX[7:0]	0
Bit 2	R	RX_AUX[7:0]	0
Bit 1	R	RX_AUX[7:0]	0
Bit 0	R	RX_AUX[7:0]	0

**RX\_AUX[7:0]**

These bits constitute the output from an Auxiliary channel between CPUs at each end of the link. Their use is at the Software developers' discretion. A read from this register will return the AUX header byte of the last message received (without a CRC-16 error).

**RX\_STTS\_VALID**

This bit indicates that the value of RX\_AUX is valid. When read with a '0' this register should be re-read until RX\_STTS\_VALID is a '1'. This bit will be cleared for less than 0.15% of the time.

**Register 09BH: WILC Receive Status and FIFO Synch Register**

Bit	Type	Function	Default
Bit 15	R	RX_STTS_VALID	X
Bit 14	R	RX_LINK[1:0]	0
Bit 13	R	RX_LINK[1:0]	0
Bit 12	R	OPAGE[1:0]	0
Bit 11	R	OPAGE[1:0]	0
Bit 10	R	OUSER[2:0]	0
Bit 0	R	OUSER[2:0]	0
Bit 8	R	OUSER[2:0]	0
Bit 7	R	CRC_ERR	0
Bit 6	R	HDR_CRC_ERR	0
Bit 5	R	RX_MSG_LVL[3:0]	0
Bit 4	R	RX_MSG_LVL[3:0]	0
Bit 3	R	RX_MSG_LVL[3:0]	0
Bit 2	R	RX_MSG_LVL[3:0]	0
Bit 1	R	RX_FI_BUSY	0
Bit 0	R	RX_SYNC_DONE	X
Bit 0	W	RX_XFER_SYNC	0

When this register is read, it returns the status for the Receive Message Channel. When a logic 1 is written into bit 0 of this register, it is used to synchronize the Receive FIFO to the start of a message boundary or perform a message skip.



## RX\_XFER\_SYNC

Writing a logic 1 to this bit initiates a read sequence from the start of the next *unread* message. The hardware aligns the message read buffer address to the start of the next *unread* message and prefetches the first Dword from the *unread* message buffer so that it is ready to be read from the WILC Receive FIFO Data registers.

An *unread* message in this context means that the s/w has not read any of the message payload data by reading the WILC Receive FIFO Data registers.

After the RX XFER SYNC process has been completed successive reads from the Receive FIFO return the last Dword read from the Receive FIFO and prefetch the next Dword (when available).

This bit must be written to a logic 1 at the start of a message read sequence.

When multiple complete messages are being read (software knows that there is more than one message in the FIFO using the RX\_MSG\_LVL bits) this bit does not need to be written between individual message reads. It must be written for the 1<sup>st</sup> message.

When software uses a variable length message protocol it may want to abandon reading a message buffer before reading the entire message buffer of 8 DWords (16 Words). In this case this bit must be written with a '1' to move the message pointer to the start of the next message buffer before starting the read of that buffer.

After writing this bit with a logic 1 software should not start reading the FIFO until the RX\_FI\_BUSY bit has cleared. In the worst case this will take 4 SYSCLK cycles.

At this point the 1<sup>st</sup> DWORD of the message is available for reading and the CRC\_ERR bit is valid. Software may abandon a CRC errored message without reading the message buffer by writing this bit with a logic 1 again.

Whenever the RW8D block is not in frame or character alignment, the WILC will be receiving random data and the WILC receive message FIFO will be filled with this random data. Once the RW8D is in character alignment and in frame alignment (OCAV and OFAV in register 0C0H are low), this bit should be written to 16 times before attempting to use the WILC. This will flush out the receive message FIFO.

On reads this bit always returns the RX\_SYNC\_DONE status.

## RX\_SYNC\_DONE

This bit indicates the status of an RX\_XFER\_SYNC operation. When this bit is a logic 1 it indicates that an RX\_XFER\_SYNC has been done. S/W should check this bit at the start of a message read sequence or when attempting to perform a message skip sequence.

## RX\_FI\_BUSY

This bit indicates that the internal hardware is transferring data from the Receive FIFO RAM into the Receive FIFO registers. The bit is set following a write to this register with the RX\_XFER\_SYNC bit set or following a read from the WILC Receive FIFO Data Low register.

Following an RX\_XFER\_SYNC write this bit need not be read by software if

the time interval to the successive Receive FIFO DATA register read is greater than approximately 4 SYSCLK cycles.

This bit need not be read by software if the time interval between successive Receive FIFO DATA register reads greater than approximately 3 SYSCLK cycles.

This means between a read access from the WILC Received FIFO Data Low register and a read from the WILC Received FIFO Data High register. Note that there is no time restriction between a read accesses from the WILC Received FIFO Data High register and a read from the WILC Received FIFO Data Low register

## RX\_MSG\_LVL[3:0]

This indicates the current number of messages in the Receive FIFO.

RX_MSG_LVL[3:0]	Number of Messages
0000	0
:	:
1000	8

Values greater than 1000 will not occur.

## HDR\_CRC\_ERR

If this bit is set to a logic 1, the last message slot received was received with an errored CRC-16 field. This bits is updated every message slot. This bit is provided as status only.

## CRC\_ERR

If this bit it set to '1', the message at the head of the Receive FIFO has an errored CRC-16 field.

The usual sequence would be to read this register before reading the message buffer to check if the message buffer that will be read from next has been received with a CRC error. If a Receive FIFO Synchronization has been started the value of this bit is invalid until the RX\_XFER\_SYNC operation has completed. This bit is valid when RX\_FI\_BUSY is a logic 0 following a Receive FIFO Synchronization. The software must only check the status of this bit before reading the first word of a message from the receive FIFO.

#### OUSER[2:0]

These bits are a reflection of the USER[2:0] bits received in the message header of the latest received message (without a CRC-16 error) on the Working Serial Link. OUSER[2] is output from the SBSLITE on OUSER2 when the Working Serial Link is selected.

#### OPAGE[1:0]

These bits are a reflection of the PAGE[1:0] bits received in the message header of the latest received message (without a CRC-16 error) on the Working Serial Link. When the Working Serial Link is selected, OPAGE[1] controls the active page of the IMSU and OPAGE[0] controls the active page of the OMSU.

#### RX\_LINK[1:0]

These bits are a reflection of the LINK[1:0] bits received in the message header of the latest received message (without a CRC-16 error) on the Working Serial Link.

#### RX\_STTS\_VALID

This bit indicates that the values of RX\_MSG\_LVL , RX\_LINK, OPAGE, and OUSER are valid. When read with a logic 0 this register should be re-read until RX\_STTS\_VALID is a logic 1. This bit will be cleared for only approximately 0.15% of time.

**Register 09DH: WILC Interrupt Enable and Control Register.**

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 12	R/W	RX_TIMEOUT_VAL[1:0]	0
Bit 11	R/W	RX_TIMEOUT_VAL[1:0]	0
Bit 10	R/W	RX_THRESHOLD_VAL[2:0]	1
Bit 9	R/W	RX_THRESHOLD_VAL[2:0]	0
Bit 8	R/W	RX_THRESHOLD_VAL[2:0]	1
Bit 7	R	Unused	0
Bit 6	R/W	RX_TIMEOUTE	0
Bit 5	R/W	RX_THRSHLDE	0
Bit 4	R/W	RX_OVFLWE	0
Bit 3	R/W	RX_LINK_CHGE	0
Bit 2	R/W	OPAGE_CHGE[1:0]	0
Bit 1	R/W	OPAGE_CHGE[1:0]	0
Bit 0	R/W	OUUSER0_CHGE	0

**OUUSER0\_CHGE**

Writing a logic 1 to the RX\_OUUSER0\_CHGE bit enables the generation of an interrupt on a change of state from a logic 0 to a logic 1 of received message header bit OUSER[0].

**OPAGE\_CHGE[1:0]**

Writing a logic 1 to the OPAGE\_CHGE[n] bit enables the generation of an interrupt on a change of state of the received PAGE bits. The OPAGE bits that changed value are indicated by a logic 1 in the corresponding OPAGE\_CHGI[n].

**RX\_LINK\_CHGE**

Writing a logic 1 to the RX\_LINK\_CHGE bit enables the generation of an interrupt on a change of state of the received LINK bits. When either of the received LINK bits has changed value the RX\_LINK\_CHGI bit will be set to a logic 1.

**RX\_OVFLWE:**

Writing a logic 1 to the RX\_OVFLWE bit enables the generation of an interrupt when RX\_OVFLWI is a logic 1.

**RX\_THRSHLDE:**

Writing a logic 1 to the RX\_THRSHLDE bit enables the generation of an interrupt when RX\_THRSHLDI is a logic 1.

**RX\_TIMEOUTE:**

Writing a logic 1 to the RX\_TIMEOUTE bit enables the generation of an interrupt when RX\_TIMEOUTI is a logic 1.

**RX\_THRESHOLD\_VAL[2:0]:**

Variable Threshold dictates the minimum number of messages required to be in the RXFIFO before an interrupt is generated. '000' = 1 message '111' = 8 messages.

<b>RX_THRESHOLD_VAL[2:0]</b>	<b>Messages</b>
000	1
001	2
010	3
011	4
100	5
101	6
110	7
111	8

**RX\_TIMEOUT\_VAL[1:0]**

These bits specify a variable delay, relative to a read from the receive message FIFO, in steps of 125 us, before an interrupt is generated, if the Receive FIFO level is greater than 0. The objective is to stop stale messages collecting in the RXFIFO.

<b>RX_TIMEOUT_VAL[1:0]</b>	<b>Nominal Delay In Frames</b>	<b>Minimum Delay from Message Reception</b>	<b>Maximum Delay from Message Reception</b>	<b>Minimum Delay from FIFO read</b>	<b>Maximum Delay from FIFO read</b>
00	1	152µs	222µs	125µs	250µs
01	2	277µs	347µs	250µs	375µs
10	3	402µs	472µs	375µs	500µs
11	4	527µs	597µs	500µs	625µs

**Register 09FH: WILC Interrupt Reason Register**

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R	Unused	0
Bit 8	R	Unused	0
Bit 7	R	Unused	0
Bit 6	R	RX_TIMEOUTI	0
Bit 5	R	RX_THRSHLDI	0
Bit 4	R	RX_OVFLWI	0
Bit 3	R	RX_LINK_CHGI	0
Bit 2	R	OPAGE_CHGI[1:0]	0
Bit 1	R	OPAGE_CHGI[1:0]	0
Bit 0	R	OUSER0_CHGI	0

This register contains the status of events that may be enabled to generate interrupts..

All bits in this register are cleared on read.

**OUSER0\_CHGI**

A logic 1 in this bit indicates that the last received value of the OUSER[0] header bit has changed from a '0' to a '1' from the previously received values. This bit is cleared on a read.

**OPAGE\_CHGI[1:0]**

A logic 1 in these bits indicates that the last received value of the corresponding OPAGE[1:0] header bits has changed from the previously received values. These bits are cleared on read.

**RX\_LINK\_CHGI**

A logic 1 in this bit indicates that the last received value of the LINK[1:0] header bits has changed from the previously received values. This bit is cleared on a read.

RX\_OVFLWI

A logic 1 in this bit indicates that a Receive FIFO Overflow has occurred. This bit is cleared on a read.

RX\_THRSHLDI

A logic 1 in this bit indicates that the Receive FIFO Threshold has been reached. This bit is cleared on a read.

RX\_TIMEOUTI

A logic 1 in this bit indicates a Receive FIFO Timeout. This bit is cleared on read.

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**Register 0A0H: PILC Transmit FIFO Data High**

Bit	Type	Function	Default
Bit 15	R/W	TDAT[31:16]	0
Bit 14	R/W	TDAT[31:16]	0
Bit 13	R/W	TDAT[31:16]	0
Bit 12	R/W	TDAT[31:16]	0
Bit 11	R/W	TDAT[31:16]	0
Bit 10	R/W	TDAT[31:16]	0
Bit 9	R/W	TDAT[31:16]	0
Bit 8	R/W	TDAT[31:16]	0
Bit 7	R/W	TDAT[31:16]	0
Bit 6	R/W	TDAT[31:16]	0
Bit 5	R/W	TDAT[31:16]	0
Bit 4	R/W	TDAT[31:16]	0
Bit 3	R/W	TDAT[31:16]	0
Bit 2	R/W	TDAT[31:16]	0
Bit 1	R/W	TDAT[31:16]	0
Bit 0	R/W	TDAT[31:16]	0

When writing data to the transmit FIFO, this register must be written to before register 0A1H.

**TDAT[31:16]**

TDAT[31:16] and TDAT[15:0] form the 32 bit wide data word to be written to the FIFO. The FIFO is organized as 32 bits wide and 64 words deep, giving a total of eight 32 byte messages.



**Register 0A1H: PILC Transmit FIFO Data Low**

Bit	Type	Function	Default
Bit 15	R/W	TDAT[15:0]	0
Bit 14	R/W	TDAT[15:0]	0
Bit 13	R/W	TDAT[15:0]	0
Bit 12	R/W	TDAT[15:0]	0
Bit 11	R/W	TDAT[15:0]	0
Bit 10	R/W	TDAT[15:0]	0
Bit 9	R/W	TDAT[15:0]	0
Bit 8	R/W	TDAT[15:0]	0
Bit 7	R/W	TDAT[15:0]	0
Bit 6	R/W	TDAT[15:0]	0
Bit 5	R/W	TDAT[15:0]	0
Bit 4	R/W	TDAT[15:0]	0
Bit 3	R/W	TDAT[15:0]	0
Bit 2	R/W	TDAT[15:0]	0
Bit 1	R/W	TDAT[15:0]	0
Bit 0	R/W	TDAT[15:0]	0

Writing to this register will initiate a transfer of TDAT[31:0] into the transmit FIFO.

**TDAT[15:0]**

TDAT[31:16] and TDAT[15:0] form the 32 bit wide data word to be written to the FIFO. The FIFO is organized as 32 bits wide and 64 words deep, giving a total of eight 32 byte messages.

**Register 0A3H: PILC Transmit Control Register**

Bit	Type	Function	Default
Bit 15	R/W	TX_AUX[7:0]	0
Bit 14	R/W	TX_AUX[7:0]	0
Bit 13	R/W	TX_AUX[7:0]	0
Bit 12	R/W	TX_AUX[7:0]	0
Bit 11	R/W	TX_AUX[7:0]	0
Bit 10	R/W	TX_AUX[7:0]	0
Bit 9	R/W	TX_AUX[7:0]	0
Bit 8	R/W	TX_AUX[7:0]	0
Bit 7	R	Unused	0
Bit 6	R	Unused	0
Bit 5	R/W	TX_LINK[1:0]	0
Bit 4	R/W	TX_LINK[1:0]	0
Bit 3	R	Unused	0
Bit 2	R	Unused	0
Bit 1	R/W	TX_CRC_SWIZ_EN	0
Bit 0	R/W	TX_BYPASS	0

**TX\_BYPASS**

When this bit is set to '1', the blocks message transmit functions are bypassed. No messages are inserted into the Transmit data. The transmit message FIFO RAM is disabled and thus message data writes are ignored.

**TX\_CRC\_SWIZ\_EN**

When this bit is set to '1', the calculated CRC-16 is bit reversed before being transmitted. This facility can be used for diagnostic testing of CRC-16 generation and checking functionality.

**TX\_LINK[1:0]**

These bits are transmitted in the LINK bits of the message header of the next available message. On reads these bit return the last written value.

### TX\_AUX[7:0]

These bits form the input to an Auxiliary channel between CPUs at each end of the link. Their use is at the Software developer's discretion. Data written to this register will be transmitted in the AUX header byte of each subsequent message to the other end of the in-band link. A new value of TX\_AUX will be transmitted at the next available message. Data read from this register will be the data previously written.

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**Register 0A5H: PILC Transmit Status and FIFO Synch Register**

Bit	Type	Function	Default
Bit 15	R	TX_MSG_LVL_VALID	X
Bit 14	R	TX_LINK[1:0]	0
Bit 13	R	TX_LINK[1:0]	0
Bit 12	R	IPAGE[1:0]	X
Bit 11	R	IPAGE[1:0]	X
Bit 10	R	IUSER[2:0]	X
Bit 9	R	IUSER[2:0]	0
Bit 8	R	IUSER[2:0]	0
Bit 7	R	Unused	0
Bit 6	R	Unused	0
Bit 5	R	TX_MSG_LVL[3:0]	0
Bit 4	R	TX_MSG_LVL[3:0]	0
Bit 3	R	TX_MSG_LVL[3:0]	0
Bit 2	R	TX_MSG_LVL[3:0]	0
Bit 1	R	TX_FI_BUSY	0
Bit 0	W	TX_XFER_SYNC	0

**TX\_XFER\_SYNC**

Writing '1' to this bit initializes the next write sequence to be to the beginning of the next message. After a '1' had been written successive writes to the Transmit FIFO will be to location zero of the next available slot. If a partial message has been written, TX\_XFER\_SYNC indicates that the current message is complete and that subsequent writes will be to the next message. If more than 32 bytes are written, the 33rd byte will be the first byte of the next message. The purpose of this bit is to unambiguously align the message boundaries. Another use would be to abandon the current write and move the write pointer to the beginning of the next message. (Previous message data will remain in the unwritten portion of the message being abandoned, which will have to be ignored by the receiving software).

If the message FIFO pointers are already at a message boundary then writing this bit to a '1' will have no affect.

On reads this bit is always returned as a '0'.

**TX\_FI\_BUSY**

This bit indicates that the internal hardware is transferring the data from the Transmit FIFO registers (TDAT) into the internal RAM. This bit need not be read by software if the time interval between successive 32 bit transfers is greater than 3 SYSCLK cycles.

### TX\_MSG\_LVL[3:0]

This indicates the current number of messages in the TXFIFO.

TX_MSG_LVL[3:0]	Number of Messages
0000	0
:	:
1000	8

Values greater than 1000 will not occur. The number of free messages available in the FIFO is given by 8 – TX\_MSG\_LVL. The TX\_MSG\_LVL\_VALID bit must be polled before reading these bits.

### IUSER[2:0]

These bits are a reflection of the USER[2:0] bits output in the header of the in-band link on the Transmit Protection Serial Link. IUSER[2] is sourced from the IUSER2 input to the SBSLITE. IUSER[1:0] is sourced from the TXPUSER[1:0] bits of register 008H.

### IPAGE[1:0]

These bits are a reflection of the PAGE[1:0] bits output in the header of the in-band link on the Transmit Protection Serial Link. PAGE[1] reflects the current memory page used by the IMSU. PAGE[0] reflects the current memory page used by the OMSU.

### TX\_LINK[1:0]

These bits reflect the last written value of the TX\_LINK[1:0] field of the PILC Transmit Control Register. The upper byte of this register therefore reflects all of the configurable bits of the message Header1 byte.

### TX\_MSG\_LVL\_VALID

This bit indicates that the value of TX\_MSG\_LVL is valid. When read with a logic 0 this register should be re-read until TX\_MSG\_LVL\_VALID is a logic 1. This bit will be clear for only approximately 0.12% of the time. This bit must always be polled before reading the TX\_MSG\_LVL bits.

**Register 0A6H: PILC Receive FIFO Data High**

Bit	Type	Function	Default
Bit 15	R	RDAT[31:16]	0
Bit 14	R	RDAT[31:16]	0
Bit 13	R	RDAT[31:16]	0
Bit 12	R	RDAT[31:16]	0
Bit 11	R	RDAT[31:16]	0
Bit 10	R	RDAT[31:16]	0
Bit 9	R	RDAT[31:16]	0
Bit 8	R	RDAT[31:16]	0
Bit 7	R	RDAT[31:16]	0
Bit 6	R	RDAT[31:16]	0
Bit 5	R	RDAT[31:16]	0
Bit 4	R	RDAT[31:16]	0
Bit 3	R	RDAT[31:16]	0
Bit 2	R	RDAT[31:16]	0
Bit 1	R	RDAT[31:16]	0
Bit 0	R	RDAT[31:16]	0

When reading data out of the receive FIFO, this register must be read before register 0A7H.

**RDAT[31:16]**

RDAT[31:16] and RDAT[15:0] form the 32 bit wide data word read from the FIFO. The FIFO is organized as 32 bits wide and 64 words deep, giving a total of eight 32 byte messages. This register must be read before register 097H.

**Register 0A7H: PILC Receive FIFO Data Low**

Bit	Type	Function	Default
Bit 15	R	RDAT[15:0]	0
Bit 14	R	RDAT[15:0]	0
Bit 13	R	RDAT[15:0]	0
Bit 12	R	RDAT[15:0]	0
Bit 11	R	RDAT[15:0]	0
Bit 10	R	RDAT[15:0]	0
Bit 9	R	RDAT[15:0]	0
Bit 8	R	RDAT[15:0]	0
Bit 7	R	RDAT[15:0]	0
Bit 6	R	RDAT[15:0]	0
Bit 5	R	RDAT[15:0]	0
Bit 4	R	RDAT[15:0]	0
Bit 3	R	RDAT[15:0]	0
Bit 2	R	RDAT[15:0]	0
Bit 1	R	RDAT[15:0]	0
Bit 0	R	RDAT[15:0]	0

Reading this register initiates a read access to the next location in the receive FIFO.

**RDAT[15:0]**

RDAT[31:16] and RDAT[15:0] form the 32 bit wide data word read from the FIFO. The FIFO is organized as 32 bits wide and 64 words deep, giving a total of eight 32 byte messages.

**Register 0A9H: PILC Receive FIFO Control Register**

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R	Unused	0
Bit 8	R	Unused	0
Bit 7	R	Unused	0
Bit 6	R	Unused	0
Bit 5	R	Unused	0
Bit 4	R	Unused	0
Bit 3	R	Unused	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	RX_CRC_SWIZ_EN	0
Bit 0	R/W	RX_BYPASS	0

**RX\_BYPASS**

When this bit is set to a logic 1. The PILC's message receive functions are bypassed and no messages are extracted from the Receive Working Serial Link. The receive message FIFO RAM is disabled and thus message data reads will return undefined data.

**RX\_CRC\_SWIZ\_EN**

When this bit is set to a logic 1, the calculated CRC-16 is bit reversed before being compared with CRC-16 bytes of the received message. This facility can be used for diagnostic testing of CRC-16 generation and checking functionality

**Reserved**

This bit should be set to a logic 1 for proper operation of the PILC.



**Register 0AAH: PILC Receive Auxiliary Register**

Bit	Type	Function	Default
Bit 15	R	RX_STTS_VALID	X
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R	Unused	0
Bit 8	R	Unused	0
Bit 7	R	RX_AUX[7:0]	0
Bit 6	R	RX_AUX[7:0]	0
Bit 5	R	RX_AUX[7:0]	0
Bit 4	R	RX_AUX[7:0]	0
Bit 3	R	RX_AUX[7:0]	0
Bit 2	R	RX_AUX[7:0]	0
Bit 1	R	RX_AUX[7:0]	0
Bit 0	R	RX_AUX[7:0]	0

**RX\_AUX[7:0]**

These bits constitute the output from an Auxiliary channel between CPUs at each end of the link. Their use is at the Software developers' discretion. A read from this register will return the AUX header byte of the last message received (without a CRC-16 error).

**RX\_STTS\_VALID**

This bit indicates that the value of RX\_AUX is valid. When read with a '0' this register should be re-read until RX\_STTS\_VALID is a '1'. This bit will be cleared for less than 0.15% of the time.

**Register 0ABH: PILC Receive Status and FIFO Synch Register**

Bit	Type	Function	Default
Bit 15	R	RX_STTS_VALID	X
Bit 14	R	RX_LINK[1:0]	0
Bit 13	R	RX_LINK[1:0]	0
Bit 12	R	OPAGE[1:0]	0
Bit 11	R	OPAGE[1:0]	0
Bit 10	R	OUSER[2:0]	0
Bit 9	R	OUSER[2:0]	0
Bit 8	R	OUSER[2:0]	0
Bit 7	R	CRC_ERR	0
Bit 6	R	HDR_CRC_ERR	0
Bit 5	R	RX_MSG_LVL[3:0]	0
Bit 4	R	RX_MSG_LVL[3:0]	0
Bit 3	R	RX_MSG_LVL[3:0]	0
Bit 2	R	RX_MSG_LVL[3:0]	0
Bit 1	R	RX_FI_BUSY	0
Bit 0	R	RX_SYNC_DONE	X
Bit 0	W	RX_XFER_SYNC	0

When this register is read, it returns the status for the Receive Message Channel. When a logic 1 is written into bit 0 of this register, it is used to synchronize the Receive FIFO to the start of a message boundary or perform a message skip.

## RX\_XFER\_SYNC

Writing a logic 1 to this bit initiates a read sequence from the start of the next *unread* message. The hardware aligns the message read buffer address to the start of the next *unread* message and prefetches the first Dword from the *unread* message buffer so that it is ready to be read from the WILC Receive FIFO Data registers.

An *unread* message in this context means that the s/w has not read any of the message payload data by reading the WILC Receive FIFO Data registers.

After the RX XFER SYNC process has been completed successive reads from the Receive FIFO return the last Dword read from the Receive FIFO and prefetch the next Dword (when available).

This bit must be written to a logic 1 at the start of a message read sequence.

When multiple complete messages are being read (software knows that there is more than one message in the FIFO using the RX\_MSG\_LVL bits) this bit does not need to be written between individual message reads. It must be written for the 1<sup>st</sup> message.

When software uses a variable length message protocol it may want to abandon reading a message buffer before reading the entire message buffer of 8 DWords (16 Words). In this case this bit must be written with a '1' to move the message pointer to the start of the next message buffer before starting the read of that buffer.

After writing this bit with a logic 1 software should not start reading the FIFO until the RX\_FI\_BUSY bit has cleared. In the worst case this will take 4 SYSCLK cycles.

At this point the 1<sup>st</sup> DWORD of the message is available for reading and the CRC\_ERR bit is valid. Software may abandon a CRC errored message without reading the message buffer by writing this bit with a logic 1 again.

Whenever the RP8D block is not in frame or character alignment, the PILC will be receiving random data and the PILC receive message FIFO will be filled with this random data. Once the RP8D is in character alignment and in frame alignment (OCAV and OFAV in register 0C8H are low), this bit should be written to 16 times before attempting to use the PILC. This will flush out the receive message FIFO.

On reads this bit is always returns the RX\_SYNC\_DONE status.

## RX\_SYNC\_DONE

This bit indicates the status of an RX\_XFER\_SYNC operation. When this bit is a logic 1 it indicates that an RX\_XFER\_SYNC has been done. S/W should check this bit at the start of a message read sequence or when attempting to perform a message skip sequence.

## RX\_FI\_BUSY

This bit indicates that the internal hardware is transferring data from the Receive FIFO RAM into the Receive FIFO registers. The bit is set following a write to this register with the RX\_XFER\_SYNC bit set or following a read from the PILC Receive FIFO Data Low register.

Following an RX\_XFER\_SYNC write this bit need not be read by software if

the time interval to the successive Receive FIFO DATA register read is greater than approximately 4 SYSCLK cycles.

This bit need not be read by software if the time interval between successive Receive FIFO DATA register reads greater than approximately 3 SYSCLK cycles.

This means between a read access from the PILC Received FIFO Data Low register and a read from the PILC Received FIFO Data High register. Note that there is no time restriction between a read accesses from the PILC Received FIFO Data High register and a read from the PILC Received FIFO Data Low register

## RX\_MSG\_LVL[3:0]

This indicates the current number of messages in the Receive FIFO.

RX_MSG_LVL[3:0]	Number of Messages
0000	0
:	:
1000	8

Values greater than 1000 will not occur.

## HDR\_CRC\_ERR

If this bit is set to a logic 1, the last message slot received was received with an errored CRC-16 field. This bits is updated every message slot. This bit is provided as status only.

## CRC\_ERR

If this bit it set to '1', the message at the head of the Receive FIFO has an errored CRC-16 field.

The usual sequence would be to read this register before reading the message buffer to check if the message buffer that will be read from next has been received with a CRC error. If a Receive FIFO Synchronization has been started the value of this bit is invalid until the RX\_XFER\_SYNC operation has completed. This bit is valid when RX\_FI\_BUSY is a logic 0 following a Receive FIFO Synchronization. The software must only check the status of this bit before reading the first word of a message from the receive FIFO.

#### OUSER[2:0]

These bits are a reflection of the USER[2:0] bits received in the message header of the latest received message (without a CRC-16 error) on the Protection Serial Link. OUSER[2] is output from the SBSLITE on OUSER2 when the Protection Serial Link is selected.

#### OPAGE[1:0]

These bits are a reflection of the PAGE[1:0] bits received in the message header of the latest received message (without a CRC-16 error) on the Protection Serial Link. When the Protection Serial Link is selected, OPAGE[1] controls the active page of the IMSU and OPAGE[0] controls the active page of the OMSU.

#### RX\_LINK[1:0]

These bits are a reflection of the LINK[1:0] bits received in the message header of the latest received message (without a CRC-16 error) on the Protection Serial Link.

#### RX\_STTS\_VALID

This bit indicates that the values of RX\_MSG\_LVL , RX\_LINK, OPAGE, and OUSER are valid. When read with a logic 0 this register should be re-read until RX\_STTS\_VALID is a logic 1. This bit will be cleared for only approximately 0.15% of time.

**Register 0ADH: PILC Interrupt Enable and Control Register.**

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R/W	RX_TIMEOUT_VAL[1:0]	0
Bit 11	R/W	RX_TIMEOUT_VAL[1:0]	0
Bit 10	R/W	RX_THRESHOLD_VAL[2:0]	1
Bit 9	R/W	RX_THRESHOLD_VAL[2:0]	0
Bit 8	R/W	RX_THRESHOLD_VAL[2:0]	1
Bit 7	R	Unused	0
Bit 6	R/W	RX_TIMEOUTE	0
Bit 5	R/W	RX_THRSHLDE	0
Bit 4	R/W	RX_OVFLWE	0
Bit 3	R/W	RX_LINK_CHGE	0
Bit 2	R/W	OPAGE_CHGE[1:0]	0
Bit 1	R/W	OPAGE_CHGE[1:0]	0
Bit 0	R/W	OUUSER0_CHGE	0

**OUUSER0\_CHGE**

Writing a logic 1 to the RX\_OUUSER0\_CHGE bit enables the generation of an interrupt on a change of state from a logic 0 to a logic 1 of received message header bit OUSER[0].

**OPAGE\_CHGE[1:0]**

Writing a logic 1 to the OPAGE\_CHGE[n] bit enables the generation of an interrupt on a change of state of the received PAGE bits. The OPAGE bits that changed value are indicated by a logic 1 in the corresponding OPAGE\_CHGI[n].

**RX\_LINK\_CHGE**

Writing a logic 1 to the RX\_LINK\_CHGE bit enables the generation of an interrupt on a change of state of the received LINK bits. When either of the received LINK bits has changed value the RX\_LINK\_CHGI bit will be set to a logic 1.

**RX\_OVFLWE**

Writing a logic 1 to the RX\_OVFLWE bit enables the generation of an interrupt when RX\_OVFLWI is a logic 1.

### RX\_THRSHLDE

Writing a logic 1 to the RX\_THRSHLDE bit enables the generation of an interrupt when RX\_THRSHLDI is a logic 1.

### RX\_TIMEOUTE

Writing a logic 1 to the RX\_TIMEOUTE bit enables the generation of an interrupt when RX\_TIMEOUTI is a logic 1.

### RX\_THRESHOLD\_VAL[2:0]

Variable Threshold dictates the minimum number of messages required to be in the RXFIFO before an interrupt is generated. '000' = 1 message '111' = 8 messages.

RX_THRESHOLD_VAL[2:0]	Messages
000	1
001	2
010	3
011	4
100	5
101	6
110	7
111	8

### RX\_TIMEOUT\_VAL[1:0]

These bits specify a variable delay, relative to a read from the receive message FIFO, in steps of 125 us, before an interrupt is generated, if the Receive FIFO level is greater than 0. The objective is to stop stale messages collecting in the RXFIFO.

RX_TIMEOUT_VAL[1:0]	Nominal Delay In Frames	Minimum Delay from Message Reception	Maximum Delay from Message Reception	Minimum Delay from FIFO read	Maximum Delay from FIFO read
00	1	152µs	222µs	125µs	250µs
01	2	277µs	347µs	250µs	375µs
10	3	402µs	472µs	375µs	500µs
11	4	527µs	597µs	500µs	625µs

**Register 0AFH: PILC Interrupt Reason Register**

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R	Unused	0
Bit 11	R	Unused	0
Bit 10	R	Unused	0
Bit 9	R	Unused	0
Bit 8	R	Unused	0
Bit 7	R	Unused	0
Bit 6	R	RX_TIMEOUTI	0
Bit 5	R	RX_THRSHLDI	0
Bit 4	R	RX_OVFLWI	0
Bit 3	R	RX_LINK_CHGI	0
Bit 2	R	OPAGE_CHGI[1:0]	0
Bit 1	R	OPAGE_CHGI[1:0]	0
Bit 0	R	OUSER0_CHGI	0

This register contains the status of events that may be enabled to generate interrupts..

All bits in this register are cleared on read.

**OUSER0\_CHGI**

A logic 1 in this bit indicates that the last received value of the OUSER[0] header bit has changed from a '0' to a '1' from the previously received values. This bit is cleared on a read.

**OPAGE\_CHGI[1:0]**

A logic 1 in these bits indicates that the last received value of the corresponding OPAGE[1:0] header bits has changed from the previously received values. These bits are cleared on read.

**RX\_LINK\_CHGI**

A logic 1 in this bit indicates that the last received value of the LINK[1:0] header bits has changed from the previously received values. This bit is cleared on a read.



RX\_OVFLWI

A logic 1 in this bit indicates that a Receive FIFO Overflow has occurred. This bit is cleared on a read.

RX\_THRSHLDI

A logic 1 in this bit indicates that the Receive FIFO Threshold has been reached. This bit is cleared on a read.

RX\_TIMEOUTI

A logic 1 in this bit indicates a Receive FIFO Timeout. This bit is cleared on read.

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**Register 0B0H: TW8E Control and Status**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	FIFOERRE	0
Bit 3	R/W	TPINS	0
Bit 2	R/W	Reserved	0
Bit 1	W	CENTER	0
Bit 0	R/W	DLCV	0

This register provides control and reports the status of the TW8E.

**DLCV**

The diagnose line code violation bit (DLCV) controls the insertion of line code violation in the working transmit serial data stream. When this bit is set high, the encoded data is continuously inverted to generate line code violations. The inverted data will represent both valid and invalid 8B/10B characters as not all 8B/10B characters have positive running disparity and negative running disparity characters simply the inverse of each other. Note that SBI and TelecomBus control characters are not affected by the DLCV bit but are passed unaltered.

**CENTER**

The FIFO centering control bit (CENTER) controls the separation of the FIFO read and write pointers. CENTER is a write only bit. When a logic high is written to CENTER, and the current FIFO depth is not in the range of 3, 4 or 5 characters, the FIFO depth is forced to be four 8B/10B characters deep, with a momentary data corruption. Writing to the CENTER bit when the FIFO depth is in the 3, 4 or 5 character range produces no effect. CENTER always returns a logic low when read.

This bit must be set once CSU lock has been achieved.

#### TPINS

The Test Pattern Insertion (TPINS) controls the insertion of test pattern in the working transmit serial data stream for jitter testing purpose. When this bit is set high, the test pattern stored in the registers (TP[9:0]) is used to replace all the overhead and payload bytes of the transmit data stream. When TPINS is set low, no test pattern is inserted.

#### FIFOERRE

The FIFO overrun/underrun error interrupt enable bit (FIFOERRE) enables FIFO overrun/underrun interrupts. An interrupt is generated on a FIFO error event if the FIFOERRE is set to logic 1. No interrupt is generated if FIFOERRE if is set to logic 0.

#### Reserved

These bits must be set low for correct operation of the SBSLITE.

**Register 0B1H: TW8E Interrupt Status**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	FIFOERRI	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register reports interrupt status due the detection of FIFO error.

**FIFOERRI**

The FIFO overrun/underrun error interrupt indication bit (FIFOERRI) reports a FIFO overrun/underrun error event. FIFO overrun/underrun errors occur when FIFO logic detects FIFO read and write pointers in close proximity to each other. FIFOERRI is set to logic 1 on a FIFO overrun/underrun error. FIFOERRI is set to logic 0 when this register is read.

**Note:** the default value would only be seen immediately after a digital reset performed while the CSU is running and locked. If the CSU is disabled, or is in the process of locking, FIFO errors will be generated continually and a “1” value will appear in FIFOERRI bit almost immediately.

**Register 0B2H: TW8E Time-slot Configuration #1**

Bit	Type	Function	Default
Bit 15	R/W	TMODE8[1]	0
Bit 14	R/W	TMODE8[0]	0
Bit 13	R/W	TMODE7[1]	0
Bit 12	R/W	TMODE7[0]	0
Bit 11	R/W	TMODE6[1]	0
Bit 10	R/W	TMODE6[0]	0
Bit 9	R/W	TMODE5[1]	0
Bit 8	R/W	TMODE5[0]	0
Bit 7	R/W	TMODE4[1]	0
Bit 6	R/W	TMODE4[0]	0
Bit 5	R/W	TMODE3[1]	0
Bit 4	R/W	TMODE3[0]	0
Bit 3	R/W	TMODE2[1]	0
Bit 2	R/W	TMODE2[0]	0
Bit 1	R/W	TMODE1[1]	0
Bit 0	R/W	TMODE1[0]	0

This register configures the path termination mode of time-slots 1 to 8 of the TW8E.

**TMODE1[1:0]-TMODE8[1:0]**

The time-slot path termination mode select register bits (TMODE1[1:0]-TMODE8[1:0]) configures the mode settings for time-slots 1 to 8 of the TW8E. Time-slots are numbered in order of transmission on the working transmit serial data stream. Time-slot #1 is the first byte transmitted and time-slot #12 is the last byte transmitted. The setting stored in TMODEx[1:0] (x can be 1-8) determines which set of TelecomBus control signals are to be encoded in 8B/10B characters.

TMODEx[1]	TMODEx[0]	Functional Description
0	0	MST level. This mode must be used when in TelecomBus mode with valid H1/H2 pointers where it is not important to mark the location of the J1 byte.
0	1	HPT level. This mode must be used when in TelecomBus mode where valid V1/V2 tributary pointers must be preserved and the location of the J1 byte is indicated on the IC1FP input.
1	0	LPT level. This mode must be used for SBI336 mode and in TelecomBus mode with a valid V5 signal but without valid V1/V2 pointers.
1	1	Reserved

**Register 0B3H: TW8E Time-slot Configuration #2**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	TMODE12[1]	0
Bit 6	R/W	TMODE12[0]	0
Bit 5	R/W	TMODE11[1]	0
Bit 4	R/W	TMODE11[0]	0
Bit 3	R/W	TMODE10[1]	0
Bit 2	R/W	TMODE10[0]	0
Bit 1	R/W	TMODE9[1]	0
Bit 0	R/W	TMODE9[0]	0

This register configures the path termination mode of time-slots 9 to 12 of the TW8E.

**TMODE9[1:0]-TMODE12[1:0]**

The time-slot path termination mode select register bits (TMODE9[1:0]-TMODE12[1:0]) configures the mode settings for time-slots 9 to 12 of the TW8E. Time-slots are numbered in order of transmission on the working transmit serial data stream. Time-slot #1 is the first byte transmitted and time-slot #12 is the last byte transmitted. The setting stored in TMODEx[1:0] (x can be 9-12) determines which set of TelecomBus control signals are to be encoded in 8B/10B characters.

TMODEx[1]	TMODEx[0]	Functional Description
0	0	MST level. This mode must be used when in TelecomBus mode with valid H1/H2 pointers where it is not important to mark the location of the J1 byte.
0	1	HPT level. This mode must be used when in TelecomBus mode where valid V1/V2 tributary pointers must be preserved and the location of the J1 byte is indicated on the IC1FP input.
1	0	LPT level. This mode must be used for SBI336 mode and in TelecomBus mode with a valid V5 signal but without valid V1/V2 pointers.
1	1	Reserved

**Register 0B4H: TW8E Test Pattern**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	TP[9]	1
Bit 8	R/W	TP[8]	0
Bit 7	R/W	TP[7]	1
Bit 6	R/W	TP[6]	0
Bit 5	R/W	TP[5]	1
Bit 4	R/W	TP[4]	0
Bit 3	R/W	TP[3]	1
Bit 2	R/W	TP[2]	0
Bit 1	R/W	TP[1]	1
Bit 0	R/W	TP[0]	0

This register contains the test pattern to be inserted into the working transmit serial data stream.

**TP[9:0]**

The Test Pattern registers (TP[9:0]) contains the test pattern that is used to insert into the working transmit serial data stream for jitter test purpose. When the TPINS bit is set high, the test pattern stored in TP[9:0] is used to replace all the overhead and payload bytes of the transmit data stream.

**Register 0B5H: TW8E Analog Control**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	TXLV_ENB	0
Bit 7	R/W	PISO_ENB	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	1
Bit 1	R/W	Reserved	1
Bit 0	R/W	ARSTB	1

This registers controls the analog blocks.

**ARSTB**

Setting this bit low will reset the TWPS and TWLV blocks.

**PISO\_ENB**

Setting this bit high will disable the TWPS circuitry.

**TXLV\_ENB**

Setting this bit high will disable the TWLV circuitry.

**Reserved**

The Reserved bits should not be modified.



**Register 0B8H: TP8E Control and Status**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	FIFOERRE	0
Bit 3	R/W	TPINS	0
Bit 2	R/W	Reserved	0
Bit 1	W	CENTER	0
Bit 0	R/W	DLCV	0

This register provides control and reports the status of the TP8E.

**DLCV**

The diagnose line code violation bit (DLCV) controls the insertion of line code violation in the protection transmit serial data stream. When this bit is set high, the encoded data is continuously inverted to generate line code violations. The inverted data will represent both valid and invalid 8B/10B characters as not all 8B/10B characters have positive running disparity and negative running disparity characters simply the inverse of each other. Note that SBI and TelecomBus control characters are not affected by the DLCV bit but are passed unaltered.

**CENTER**

The FIFO centering control bit (CENTER) controls the separation of the FIFO read and write pointers. CENTER is a write only bit. When a logic high is written to CENTER, and the current FIFO depth is not in the range of 3, 4 or 5 characters, the FIFO depth is forced to be four 8B/10B characters deep, with a momentary data corruption. Writing to the CENTER bit when the FIFO depth is in the 3, 4 or 5 character range produces no effect. CENTER always returns a logic low when read.

This bit must be set once CSU lock has been achieved.

#### TPINS

The Test Pattern Insertion (TPINS) controls the insertion of test pattern in the protection transmit serial data stream for jitter testing purpose. When this bit is set high, the test pattern stored in the registers (TP[9:0]) is used to replace all the overhead and payload bytes of the transmit data stream. When TPINS is set low, no test pattern is inserted.

#### FIFOERRE

The FIFO overrun/underrun error interrupt enable bit (FIFOERRE) enables FIFO overrun/underrun interrupts. An interrupt is generated on a FIFO error event if the FIFOERRE is set to logic 1. No interrupt is generated if FIFOERRE if is set to logic 0.

#### Reserved

These bits must be set low for correct operation of the SBSLITE.

**Register 0B9H: TP8E Interrupt Status**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	FIFOERRI	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register reports interrupt status due the detection of FIFO error.

**FIFOERRI**

The FIFO overrun/underrun error interrupt indication bit (FIFOERRI) reports a FIFO overrun/underrun error event. FIFO overrun/underrun errors occur when FIFO logic detects FIFO read and write pointers in close proximity to each other. FIFOERRI is set to logic 1 on a FIFO overrun/underrun error. FIFOERRI is set to logic 0 when this register is read.

**Note:** the default value would only be seen immediately after a digital reset performed while the CSU is running and locked. If the CSU is disabled, or is in the process of locking, FIFO errors will be generated continually and a “1” value will appear in FIFOERRI bit almost immediately.

**Register 0BAH: TP8E Time-slot Configuration #1**

Bit	Type	Function	Default
Bit 15	R/W	TMODE8[1]	0
Bit 14	R/W	TMODE8[0]	0
Bit 13	R/W	TMODE7[1]	0
Bit 12	R/W	TMODE7[0]	0
Bit 11	R/W	TMODE6[1]	0
Bit 10	R/W	TMODE6[0]	0
Bit 9	R/W	TMODE5[1]	0
Bit 8	R/W	TMODE5[0]	0
Bit 7	R/W	TMODE4[1]	0
Bit 6	R/W	TMODE4[0]	0
Bit 5	R/W	TMODE3[1]	0
Bit 4	R/W	TMODE3[0]	0
Bit 3	R/W	TMODE2[1]	0
Bit 2	R/W	TMODE2[0]	0
Bit 1	R/W	TMODE1[1]	0
Bit 0	R/W	TMODE1[0]	0

This register configures the path termination mode of time-slots 1 to 8 of the TP8E.

**TMODE1[1:0]-TMODE8[1:0]**

The time-slot path termination mode select register bits (TMODE1[1:0]-TMODE8[1:0]) configures the mode settings for time-slots 1 to 8 of the TP8E. Time-slots are numbered in order of transmission on the protection transmit serial data stream. Time-slot #1 is the first byte transmitted and time-slot #12 is the last byte transmitted. The setting stored in TMODEx[1:0] (x can be 1-8) determines which set of TelecomBus control signals are to be encoded in 8B/10B characters.

TMODEx[1]	TMODEx[0]	Functional Description
0	0	MST level. This mode must be used when in TelecomBus mode with valid H1/H2 pointers where it is not important to mark the location of the J1 byte.
0	1	HPT level. This mode must be used when in TelecomBus mode where valid V1/V2 tributary pointers must be preserved and the location of the J1 byte is indicated on the IC1FP input.
1	0	LPT level. This mode must be used for SBI336 mode and in TelecomBus mode with a valid V5 signal but without valid V1/V2 pointers.
1	1	Reserved

**Register 0BBH: TP8E Time-slot Configuration #2**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	TMODE12[1]	0
Bit 6	R/W	TMODE12[0]	0
Bit 5	R/W	TMODE11[1]	0
Bit 4	R/W	TMODE11[0]	0
Bit 3	R/W	TMODE10[1]	0
Bit 2	R/W	TMODE10[0]	0
Bit 1	R/W	TMODE9[1]	0
Bit 0	R/W	TMODE9[0]	0

This register configures the path termination mode of time-slots 9 to 12 of the TP8E.

**TMODE9[1:0]-TMODE12[1:0]**

The time-slot path termination mode select register bits (TMODE9[1:0]-TMODE12[1:0]) configures the mode settings for time-slots 9 to 12 of the TW8E. Time-slots are numbered in order of transmission on the working protection serial data stream. Time-slot #1 is the first byte transmitted and time-slot #12 is the last byte transmitted. The setting stored in TMODEx[1:0] (x can be 9-12) determines which set of TelecomBus control signals are to be encoded in 8B/10B characters.

TMODEx[1]	TMODEx[0]	Functional Description
0	0	MST level. This mode must be used when in TelecomBus mode with valid H1/H2 pointers where it is not important to mark the location of the J1 byte.
0	1	HPT level. This mode must be used when in TelecomBus mode where valid V1/V2 tributary pointers must be preserved and the location of the J1 byte is indicated on the IC1FP input.
1	0	LPT level. This mode must be used for SBI336 mode and in TelecomBus mode with a valid V5 signal but without valid V1/V2 pointers.
1	1	Reserved

**Register 0BCH: TP8E Test Pattern**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	TP[9]	1
Bit 8	R/W	TP[8]	0
Bit 7	R/W	TP[7]	1
Bit 6	R/W	TP[6]	0
Bit 5	R/W	TP[5]	1
Bit 4	R/W	TP[4]	0
Bit 3	R/W	TP[3]	1
Bit 2	R/W	TP[2]	0
Bit 1	R/W	TP[1]	1
Bit 0	R/W	TP[0]	0

This register contains the test pattern to be inserted into the protection transmit serial data stream.

**TP[9:0]**

The Test Pattern registers (TP[9:0]) contains the test pattern that is used to insert into the protection transmit serial data stream for jitter test purpose. When the TPINS bit is set high, the test pattern stored in TP[9:0] is used to replace all the overhead and payload bytes of the transmit data stream.

**Register 0BDH: TP8E Analog Control**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	TXLV_ENB	0
Bit 7	R/W	PISO_ENB	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	1
Bit 1	R/W	Reserved	1
Bit 0	R/W	ARSTB	1

This register controls the analog blocks.

**ARSTB**

Setting this bit low will reset the TPPS and TPLV blocks.

**PISO\_ENB**

Setting this bit high will disable the TPPS circuitry.

**TXLV\_ENB**

Setting this bit high will disable the TPLV circuitry.

**Reserved**

The Reserved bits should not be modified.

**Register 0C0H: RW8D Control and Status**

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	RX_INV	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	FUOE	0
Bit 6	R/W	LCVE	0
Bit 5	R/W	OFAE	0
Bit 4	R/W	OCAE	0
Bit 3	R	OFAV	X
Bit 2	R	OCAV	X
Bit 1	R/W	FOFA	0
Bit 0	R/W	FOCA	0

This register provides control and reports the status of the RW8D.

**FOCA**

The force out-of-character-alignment bit (FOCA) controls the operation of the character alignment block. A transition from logic zero to logic one in this bit forces the character alignment block to the out-of-character-alignment state where it will search for the transport frame alignment character (K28.5). This bit must be manually set to logic zero before it can be used again.

**FOFA**

The force out-of-frame-alignment bit (FOFA) controls the operation of the frame alignment block. A transition from logic zero to logic one in this bit forces the frame alignment block to the out-of-frame-alignment state where it will search for the transport frame alignment character (K28.5). This bit must be manually set to logic zero before it can be used again.

**OCAV**

The out-of-character-alignment status bit (OCAV) reports the state of the character alignment block. OCAV is set high when the character alignment block is in the out-of-character-alignment state. OCAV is set low when the character alignment block is in the in-character-alignment state.



#### OFAV

The out-of-frame-alignment status bit (OFAV) reports the state of the frame alignment block. OFAV is set high when the frame alignment block is in the out-of-frame-alignment state. OFAV is set low when the frame alignment block is in the in-frame-alignment state.

#### OCAE

The out-of-character-alignment interrupt enable bit (OCAE) controls the change of character alignment state interrupts. Interrupts may be generated when the character alignment block changes state to the out-of-character-alignment state or to the in-character-alignment state. When OCAE is set high, an interrupt is generated when a change of state occurs. Interrupts due to changes of character alignment state are masked when OCAE is set low.

#### OFAE

The out-of-frame-alignment interrupt enable bit (OFAE) controls the change of frame alignment state interrupts. Interrupts may be generated when the frame alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. When OFAE is set high, an interrupt is generated when a change of state occurs. Interrupts due to changes of frame alignment state are masked when OFAE is set low.

#### LCVE

The line code violation interrupt enable bit (LCVE) controls the line code violation event interrupts. Interrupts may be generated when a line code violation is detected. When LCVE is set high, an interrupt is generated when an LCV is detected. Interrupts due to LCVs are masked when LCVE is set low.

#### FUOE

The FIFO underrun/overflow status interrupt enable (FUOE) controls the underrun/overflow event interrupts. Interrupts may be generated when the underrun/overflow event is detected. When FUOE is set high, an interrupt is generated when a FIFO underrun or overflow condition is detected. Interrupts due to FIFO underrun or overflow conditions are masked when FUOE is set low.

#### RX\_INV

The receive incoming data invert bit (RX\_INV) controls the active polarity of the parallel incoming data stream. When RX\_INV is set high, the data is complemented before further processing by the SBSLITE. When RX\_INV is set low, the data is not complemented.

Reserved

These bits must be set low for correct operation of the SBSLITE.

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**Register 0C1H: RW8D Interrupt Status**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	FUOI	X
Bit 6	R	LCVI	X
Bit 5	R	OFAI	X
Bit 4	R	OCAI	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register reports interrupt status due to change of character alignment, change of frame alignment, detection of line code violations, and FIFO overrun or underrun events in the RW8D.

**OCAI**

The out-of-character-alignment interrupt status bit (OCAI) reports and acknowledges change of character alignment state interrupts. Interrupts are generated when the character alignment block changes state to the out-of-character-alignment state or to the in-character-alignment state. OCAI is set high when change of state occurs. When the interrupt is masked by the OCAE bit the OCAI remains valid and may be polled to detect change of frame alignment events.

**OFAI**

The out-of-frame-alignment interrupt status bit (OFAI) reports and acknowledges change of frame alignment state interrupts. Interrupts are generated when the frame alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. OFAI is set high when change of state. When the interrupt is masked by the OFAE bit the OFAI remains valid and may be polled to detect change of frame alignment events.

## LCVI

The line code violation event interrupt status bit (LCVI) reports and acknowledges line code violation interrupts. Interrupts are generated when the character alignment block detects a line code violation in the incoming data stream. LCVI is set high when a line code violation event is detected. When the interrupt is masked by the LCVE bit the LCVI remains valid and may be polled to detect change of frame alignment events.

## FUOI

The FIFO underrun/overflow event interrupt status bit (FUOI) reports and acknowledges the FIFO underrun/overflow interrupts. Interrupts are generated when the character alignment block detects a that the read and write pointers are within one byte of each other. FUOI is set high when this event is detected. When the interrupt is masked by the FUE bit the FUOI remains valid and may be polled to detect underrun/overflow events.

This bit may be set when the Receive Working link is disconnected.

**Register 0C2H: RW8D LCV Count**

Bit	Type	Function	Default
Bit 15	R	LCV[15]	X
Bit 14	R	LCV[14]	X
Bit 13	R	LCV[13]	X
Bit 12	R	LCV[12]	X
Bit 11	R	LCV[11]	X
Bit 10	R	LCV[10]	X
Bit 9	R	LCV[9]	X
Bit 8	R	LCV[8]	X
Bit 7	R	LCV[7]	X
Bit 6	R	LCV[6]	X
Bit 5	R	LCV[5]	X
Bit 4	R	LCV[4]	X
Bit 3	R	LCV[3]	X
Bit 2	R	LCV[2]	X
Bit 1	R	LCV[1]	X
Bit 0	R	LCV[0]	X

This register reports the number of line code violations in the previous accumulation period in the RW8D.

**LCV[15:0]**

The LCV[15:0] bits reports the number of line code violations that have been detected since the last time the LCV registers were polled. The LCV register is polled by writing this register or by writing to the SBSLITE Master Clock Monitor, Accumulation Trigger register. The write access transfers the internally accumulated error count to the LCV register within 6 SYSCLK cycles and simultaneously resets the internal counter to begin a new cycle of error accumulation.

**Register 0C3H: RW8D Analog Control**

Bit	Type	Function	Default
Bit 15	R/W	Reserved	1
Bit 14	R/W	Reserved	1
Bit 13	R/W	DRU_ENB	0
Bit 12	R/W	RX_ENB	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	ARSTB	1
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0		Unused	X

This register controls the WDRU and RWLV analog blocks. Please refer to their respective documents for a description of the functionality of these bits.

**Note:** THIS REGISTER MUST BE SET TO CC34h FOR PROPER OPERATION OF THE RW8D BLOCKS. FOR DISABLING THIS RECEIVER, THIS REGISTER SHOULD BE SET TO F834H

**DRU\_ENB**

Setting this bit high will disable the WDRU.

**RX\_ENB**

Setting this bit high will disable the RWLV.

**ARSTB**

Setting this bit low will reset the WDRU and RWLV blocks.

**Reserved**

The Reserved bits should be set as described above.

**Register 0C8H: RP8D Control and Status**

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	RX_INV	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	FUOE	0
Bit 6	R/W	LCVE	0
Bit 5	R/W	OFAE	0
Bit 4	R/W	OCAE	0
Bit 3	R	OFAV	X
Bit 2	R	OCAV	X
Bit 1	R/W	FOFA	0
Bit 0	R/W	FOCA	0

This register provides control and reports the status of the RP8D.

**FOCA**

The force out-of-character-alignment bit (FOCA) controls the operation of the character alignment block. A transition from logic zero to logic one in this bit forces the character alignment block to the out-of-character-alignment state where it will search for the transport frame alignment character (K28.5). This bit must be manually set to logic zero before it can be used again.

**FOFA**

The force out-of-frame-alignment bit (FOFA) controls the operation of the frame alignment block. A transition from logic zero to logic one in this bit forces the frame alignment block to the out-of-frame-alignment state where it will search for the transport frame alignment character (K28.5). This bit must be manually set to logic zero before it can be used again.

**OCAV**

The out-of-character-alignment status bit (OCAV) reports the state of the character alignment block. OCAV is set high when the character alignment block is in the out-of-character-alignment state. OCAV is set low when the character alignment block is in the in-character-alignment state.

#### OFAV

The out-of-frame-alignment status bit (OFAV) reports the state of the frame alignment block. OFAV is set high when the frame alignment block is in the out-of-frame-alignment state. OFAV is set low when the frame alignment block is in the in-frame-alignment state.

#### OCAE

The out-of-character-alignment interrupt enable bit (OCAE) controls the change of character alignment state interrupts. Interrupts may be generated when the character alignment block changes state to the out-of-character-alignment state or to the in-character-alignment state. When OCAE is set high, an interrupt is generated when a change of state occurs. Interrupts due to changes of character alignment state are masked when OCAE is set low.

#### OFAE

The out-of-frame-alignment interrupt enable bit (OFAE) controls the change of frame alignment state interrupts. Interrupts may be generated when the frame alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. When OFAE is set high, an interrupt is generated when a change of state occurs. Interrupts due to changes of frame alignment state are masked when OFAE is set low.

#### LCVE

The line code violation interrupt enable bit (LCVE) controls the line code violation event interrupts. Interrupts may be generated when a line code violation is detected. When LCVE is set high, an interrupt is generated when an LCV is detected. Interrupts due to LCVs are masked when LCVE is set low.

#### FUOE

The FIFO underrun/overflow status interrupt enable (FUOE) controls the underrun/overflow event interrupts. Interrupts may be generated when the underrun/overflow event is detected. When FUOE is set high, an interrupt is generated when a FIFO underrun or overflow condition is detected. Interrupts due to FIFO underrun or overflow conditions are masked when FUOE is set low.

#### RX\_INV

The receive incoming data invert bit (RX\_INV) controls the active polarity of the parallel incoming data stream. When RX\_INV is set high, the data is complemented before further processing by the SBSLITE. When RX\_INV is set low, the data is not complemented.



Reserved

These bits must be set low for correct operation of the SBSLITE.

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**Register 0C9H: RP8D Interrupt Status**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	FUOI	X
Bit 6	R	LCVI	X
Bit 5	R	OFAI	X
Bit 4	R	OCAI	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register reports interrupt status due to change of character alignment, change of frame alignment, detection of line code violations, and FIFO overrun or underrun events in the RP8D.

**OCAI**

The out-of-character-alignment interrupt status bit (OCAI) reports and acknowledges change of character alignment state interrupts. Interrupts are generated when the character alignment block changes state to the out-of-character-alignment state or to the in-character-alignment state. OCAI is set high when change of state occurs. When the interrupt is masked by the OCAE bit the OCAI remains valid and may be polled to detect change of frame alignment events.

**OFAI**

The out-of-frame-alignment interrupt status bit (OFAI) reports and acknowledges change of frame alignment state interrupts. Interrupts are generated when the frame alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. OFAI is set high when change of state. When the interrupt is masked by the OFAE bit the OFAI remains valid and may be polled to detect change of frame alignment events.

## LCVI

The line code violation event interrupt status bit (LCVI) reports and acknowledges line code violation interrupts. Interrupts are generated when the character alignment block detects a line code violation in the incoming data stream. LCVI is set high when a line code violation event is detected. When the interrupt is masked by the LCVE bit the LCVI remains valid and may be polled to detect change of frame alignment events.

## FUOI

The FIFO underrun/overflow event interrupt status bit (FUOI) reports and acknowledges the FIFO underrun/overflow interrupts. Interrupts are generated when the character alignment block detects a that the read and write pointers are within one byte of each other. FUOI is set high when this event is detected. When the interrupt is masked by the FUE bit the FUOI remains valid and may be polled to detect underrun/overflow events.

This bit may be set when the Receive Protection link is disconnected.

**Register 0CAH: RP8D LCV Count**

Bit	Type	Function	Default
Bit 15	R	LCV[15]	X
Bit 14	R	LCV[14]	X
Bit 13	R	LCV[13]	X
Bit 12	R	LCV[12]	X
Bit 11	R	LCV[11]	X
Bit 10	R	LCV[10]	X
Bit 9	R	LCV[9]	X
Bit 8	R	LCV[8]	X
Bit 7	R	LCV[7]	X
Bit 6	R	LCV[6]	X
Bit 5	R	LCV[5]	X
Bit 4	R	LCV[4]	X
Bit 3	R	LCV[3]	X
Bit 2	R	LCV[2]	X
Bit 1	R	LCV[1]	X
Bit 0	R	LCV[0]	X

This register reports the number of line code violations in the previous accumulation period in the RP8D.

**LCV[15:0]**

The LCV[15:0] bits reports the number of line code violations that have been detected since the last time the LCV registers were polled. The LCV register is polled by writing this register or by writing to the SBSLITE Master Clock Monitor, Accumulation Trigger register. The write access transfers the internally accumulated error count to the LCV register within 6 SYSCLK cycles and simultaneously resets the internal counter to begin a new cycle of error accumulation.

**Register 0CBH: RP8D Analog Control**

Bit	Type	Function	Default
Bit 15	R/W	Reserved	1
Bit 14	R/W	Reserved	1
Bit 13	R/W	DRU_ENB	0
Bit 12	R/W	RX_ENB	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	ARSTB	1
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0		Unused	X

This register controls the PDRU and RPLV analog blocks. Please refer to their respective documents for a description of the functionality of these bits.

**Note:** THIS REGISTER MUST BE SET TO CC34h FOR PROPER OPERATION OF THE RP8D BLOCK. FOR DISABLING THIS RECEIVER, THIS REGISTER SHOULD BE SET TO F834H

**DRU\_ENB**

Setting this bit high will disable the PDRU.

**RX\_ENB**

Setting this bit high will disable the RPLV.

**ARSTB**

Setting this bit low will reset the PDRU and RPLV blocks.

**Reserved**

The Reserved bits should be set as described above.

**Register 0D0H: CSTR Control**

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	1
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	CSU_ENB	0
Bit 3	R/W	CSU_RSTB	1
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	Reserved	1

**Reserved**

The Reserved bits must be set to their default values for proper operation.

**CSU\_RSTB**

The CSU\_RSTB signal is a software reset signal that forces the CSU1250 into a reset. In order to properly reset the CSU, CSU\_RSTB should be held low for at least 1 ms.

**CSU\_ENB**

The active low CSU enable control signal (CSU\_ENB) bit can be used to force the CSU1250 into low power configuration if it is set to logic 1. For normal operation, it is set to logic 0.

**Register 0D1H: CSTR Configuration and Status**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	LOCKV	X
Bit 0	R/W	LOCKE	0

**LOCKV**

The CSU lock status bit (LOCKV) indicates whether the clock synthesis unit has successfully locked with the reference clock. LOCKV is set low when the CSU has not successfully locked with the reference SYSCLK. LOCKV is set high when the CSU has locked with the reference SYSCLK.

**LOCKE**

The CSU lock interrupt enable bit (LOCKE) controls the assertion of CSU lock state interrupts by the CSTR. When LOCKE is high, an interrupt is generated when the CSU lock state changes. Interrupts due to CSU lock state are masked when LOCKE is set low.

**Register 0D2H: CSTR Interrupt Status**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	LOCKI	0

**LOCKI**

The CSU lock interrupt status bit (LOCKI) responds to changes in the CSU lock state. Interrupts are to be generated as the CSU achieves lock with the reference clock, or loses its lock to the reference clock. As a result, the LOCKI register bit is set high when any of these changes occurs. LOCKI register bit will be cleared when it is read. When LOCKE is set high, LOCKI is used to produce the interrupt output that is reflected in the SBSLITE Master Interrupt Source register. Whether or not the interrupt is masked by the LOCKE bit, the LOCKI bit itself remains valid and may be polled to detect change of lock status events.



**Register 0E0H: REFDLL Configuration**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3		Unused	X
Bit 2	R/W	ERRORE	X
Bit 1	R/W	Reserved	0
Bit 0	R/W	LOCK	0

The REFDLL Configuration Register controls the basic operation of the DLL connected to the SREFCLK input.

**LOCK**

The LOCK register is used to force the DLL to ignore phase offsets indicated by the phase detector after phase lock has been achieved. When LOCK is set to logic zero, the DLL will track phase offsets measured by the phase detector between the SREFCLK and the DLL's reference clock. When LOCK is set to logic one, the DLL will not change the tap after the phase detector indicates of zero phase offset between the SREFCLK and the reference clock for the first time.

**ERRORE**

The ERROR interrupt enable (ERRORE) bit enables the error indication interrupt. When ERRORE is set high, an interrupt is generated upon assertion event of the ERR output and ERROR register. When ERRORE is set low, changes in the ERROR and ERR status do not generate an interrupt.

**Reserved**

These bits must be set to set low for correct operation of the SBSLITE.

**Register 0E2H: REFDLL Reset**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

The REFDLL Reset Register is used to reset the REFDLL.

Writing any value to this register performs a software reset of the REFDLL. A software reset requires a maximum of 24\*256 SREFCLK cycles for the REFDLL to regain lock.

Reserved

The Reserved bits are read only and should be ignored by the user.

**Register 0E3H: REFDLL Control Status**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	ERRORI	X
Bit 4	R	Reserved	X
Bit 3		Unused	X
Bit 2	R	ERROR	X
Bit 1	R	Reserved	0
Bit 0	R	RUN	0

The REFDLL Control Status Register provides information on the operation of the DLL connected to the SREFCLK input.

**Note:** Because the clear-on-read ERRORI bit is located in this register, polling the register to check the status of the RUN bit may inadvertently clear a pending ERRORI interrupt. Care should be taken to handle this possibility in software, perhaps by examining the ERRORI bit and responding appropriately during read accesses. Clearing the ERRORI bit will not change the status of the ERROR bit, so it is also possible to simply poll the ERROR bit and ignore ERRORI.

**RUN**

The DLL lock status register bit (RUN) indicates the DLL found a delay line tap in which the phase difference between the rising edge of the reference clock and the rising edge of SREFLCK is zero. After system reset, RUN is logic zero until the phase detector indicates an initial lock condition. When the phase detector indicates lock, RUN is set to logic 1.

The RUN register bit is cleared only by a system reset (RSTB), a software reset (in the SBSLITE Master Reset Register), or a REFDLL software reset (writing to register 0E2H).

## ERROR

The delay line error register bit (ERROR) indicates the DLL has run out of dynamic range. When the DLL attempts to move beyond the end of the delay line, ERROR is set high. When ERROR is high, the DLL cannot generate a output clock phase that causes the rising edge of the reference clock to be aligned to the rising edge of SREFCLK. ERROR is set low, when the DLL captures lock again.

## ERRORI

The delay line error event register bit (ERRORI) indicates the ERROR register bit has gone high. When the ERROR register changes from a logic zero to a logic one, the ERRORI register bit is set to logic one. If the ERRERE interrupt enable is high, the INT output is also asserted when ERRORI asserts. The ERRORI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

## Reserved

The Reserved bits are read only and should be ignored by the user.

**Register 0E8H: SYSDLL Configuration**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3		Unused	X
Bit 2	R/W	ERRORE	X
Bit 1	R/W	Reserved	0
Bit 0	R/W	LOCK	0

The SYSDLL Configuration Register controls the basic operation of the DLL connected to the SYSCLK input.

**LOCK**

The LOCK register is used to force the DLL to ignore phase offsets indicated by the phase detector after phase lock has been achieved. When LOCK is set to logic zero, the DLL will track phase offsets measured by the phase detector between the SYSCLK input and the DLL's reference clock. When LOCK is set to logic one, the DLL will not change the tap after the phase detector indicates of zero phase offset between SYSCLK and the reference clock for the first time.

**ERRORE**

The ERROR interrupt enable (ERRORE) bit enables the error indication interrupt. When ERRORE is set high, an interrupt is generated upon assertion event of the ERR output and ERROR register. When ERRORE is set low, changes in the ERROR and ERR status do not generate an interrupt.

**Reserved**

These bits must be set to set low for correct operation of the SBSLITE.

**Register 0EAH: SYSDLL Reset**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

The SYSDLL Reset Register is used to reset the SYSDLL.

Writing any value to this register performs a software reset of the SYSDLL. A software reset requires a maximum of 24\*256 SYSCLK cycles for the SYSDLL to regain lock.

**Reserved**

The Reserved bits are read only and should be ignored by the user.

**Register 0EBH: SYSDLL Control Status**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	ERRORI	X
Bit 4	R	Reserved	X
Bit 3		Unused	X
Bit 2	R	ERROR	X
Bit 1	R	Reserved	0
Bit 0	R	RUN	0

The SYSDLL Control Status Register provides information on the operation of the DLL connected to the SYSCLK input.

**Note:** Because the clear-on-read ERRORI bit is located in this register, polling the register to check the status of the RUN bit may inadvertently clear a pending ERRORI interrupt. Care should be taken to handle this possibility in software, perhaps by examining the ERRORI bit and responding appropriately during read accesses. Clearing the ERRORI bit will not change the status of the ERROR bit, so it is also possible to simply poll the ERROR bit and ignore ERRORI.

**RUN**

The DLL lock status register bit (RUN) indicates the DLL found a delay line tap in which the phase difference between the rising edge of the reference clock and the rising edge of SYSCLK is zero. After system reset, RUN is logic zero until the phase detector indicates an initial lock condition. When the phase detector indicates lock, RUN is set to logic 1.

The RUN register bit is cleared only by a system reset (RSTB), an SBS software reset (in the SBS Master Reset Register), or a SYSDLL software reset (writing to register 0EAH).

## ERROR

The delay line error register bit (ERROR) indicates the DLL has run out of dynamic range. When the DLL attempts to move beyond the end of the delay line, ERROR is set high. When ERROR is high, the DLL cannot generate a output clock phase that causes the rising edge of the reference clock to be aligned to the rising edge of SYSCLK. ERROR is set low, when the DLL captures lock again.

## ERRORI

The delay line error event register bit (ERRORI) indicates the ERROR register bit has gone high. When the ERROR register changes from a logic zero to a logic one, the ERRORI register bit is set to logic one. If the ERRERE interrupt enable is high, the INT output is also asserted when ERRORI asserts. The ERRORI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

## Reserved

The Reserved bits are read only and should be ignored by the user.



## 12 Test Features Description

Simultaneously asserting (low) the CSB, RDB, and WRB inputs causes all digital output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the SBSLITE. Test mode registers (as opposed to normal mode registers) are selected when TRS (A[8]) is high.

In addition, the SBSLITE also supports a standard IEEE 1149.1 five-signal JTAG boundary scan test port for use in board testing. All digital device inputs may be read and all digital device outputs may be forced via the JTAG test port.

### 12.1 JTAG Test Port

The SBSLITE JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

**Table 24 Instruction Register (Length - 3 bits)**

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

**Table 25 Identification Register**

Length	32 bits
Version Number	1H
Part Number	8611H
Manufacturer's Identification Code	0CDH
Device Identification	186110CDH

**Table 26 Boundary Scan Register**

Pin/ Enable	Register Bit	Cell Type	I.D. Bit
Logic 1	291	IN_CELL	L
Logic 1	290	IN_CELL	L
Logic 1	289	IN_CELL	L
Logic 1	288	IN_CELL	H
Logic 1	287	IN_CELL	H
Logic 1	286	IN_CELL	L
Logic 1	285	IN_CELL	L
Logic 1	284	IN_CELL	L
Logic 1	283	IN_CELL	L
Logic 1	282	IN_CELL	H
Logic 1	281	IN_CELL	H
Logic 1	280	IN_CELL	L
Logic 1	279	IN_CELL	L
Logic 1	278	IN_CELL	L
Logic 1	277	IN_CELL	L
Logic 1	276	IN_CELL	H
Logic 1	275	IN_CELL	L
ALE	274	IN_CELL	L
RDB	273	IN_CELL	L
WRB	272	IN_CELL	H
CSB	271	IN_CELL	L
RWSEL	270	IN_CELL	L
RSTB	269	IN_CELL	L
RC1FP	268	IN_CELL	L
NC	267	OUT_CELL	H
NC	266	OUT_CELL	H
Logic 1	265	IN_CELL	L
NC	264	OUT_CELL	L
NC	263	IO_CELL	H
NC	262	OUT_CELL	H
NC	261	OUT_CELL	L
NC	260	OUT_CELL	H
NC	259	OUT_CELL	-
NC	258	OUT_CELL	-
NC	257	OUT_CELL	-
NC	256	OUT_CELL	-
NC	255	OUT_CELL	-
NC	254	OUT_CELL	-

Pin/ Enable	Register Bit	Cell Type	I.D. Bit
NC	253	OUT_CELL	-
NC	252	OUT_CELL	-
NC	251	OUT_CELL	-
OEB_D[15]	250	OUT_CELL	-
D[15]	249	IO_CELL	-
OEB_D[14]	248	OUT_CELL	-
D[14]	247	IO_CELL	-
NC	246	OUT_CELL	-
NC	245	OUT_CELL	-
NC	244	OUT_CELL	-
NC	243	OUT_CELL	-
NC	242	OUT_CELL	-
NC	241	OUT_CELL	-
NC	240	OUT_CELL	-
NC	239	OUT_CELL	-
NC	238	OUT_CELL	-
NC	237	OUT_CELL	-
NC	236	OUT_CELL	-
NC	235	OUT_CELL	-
NC	234	OUT_CELL	-
NC	233	OUT_CELL	-
NC	232	OUT_CELL	-
NC	231	OUT_CELL	-
USER_IN	230	IN_CELL	-
OEB_D[13]	229	OUT_CELL	-
D[13]	228	IO_CELL	-
OEB_D[12]	227	OUT_CELL	-
D[12]	226	IO_CELL	-
OEB_D[11]	225	OUT_CELL	-
D[11]	224	IO_CELL	-
OEB_D[10]	223	OUT_CELL	-
D[10]	222	IO_CELL	-
OEB_D[9]	221	OUT_CELL	-
D[9]	220	IO_CELL	-
Logic 1	219	IN_CELL	-
Logic 1	218	IN_CELL	-
Logic 1	217	IN_CELL	-
Logic 1	216	IN_CELL	-
Logic 1	215	IN_CELL	-
Logic 1	214	IN_CELL	-

Pin/ Enable	Register Bit	Cell Type	I.D. Bit
Logic 1	213	IN_CELL	-
Logic 1	212	IN_CELL	-
Logic 1	211	IN_CELL	-
Logic 1	210	IN_CELL	-
Logic 1	209	IN_CELL	-
OEB_D[8]	208	OUT_CELL	-
D[8]	207	IO_CELL	-
OEB_D[7]	206	OUT_CELL	-
D[7]	205	IO_CELL	-
Logic 1	204	IN_CELL	-
Logic 1	203	IN_CELL	-
Logic 1	202	IN_CELL	-
Logic 1	201	IN_CELL	-
Logic 1	200	IN_CELL	-
Logic 1	199	IN_CELL	-
Logic 1	198	IN_CELL	-
OEB_D[6]	197	OUT_CELL	-
D[6]	196	IO_CELL	-
OEB_D[5]	195	OUT_CELL	-
D[5]	194	IO_CELL	-
OEB_D[4]	193	OUT_CELL	-
D[4]	192	IO_CELL	-
Logic 1	191	IN_CELL	-
Logic 1	190	IN_CELL	-
Logic 1	189	IN_CELL	-
Logic 1	188	IN_CELL	-
Logic 1	187	IN_CELL	-
OEB_D[3]	186	OUT_CELL	-
D[3]	185	IO_CELL	-
OEB_D[2]	184	OUT_CELL	-
D[2]	183	IO_CELL	-
OEB_D[1]	182	OUT_CELL	-
D[1]	181	IO_CELL	-
OEB_D[0]	180	OUT_CELL	-
D[0]	179	IO_CELL	-
A[8]	178	IN_CELL	-
A[7]	177	IN_CELL	-
A[6]	176	IN_CELL	-
A[5]	175	IN_CELL	-
A[4]	174	IN_CELL	-

Pin/ Enable	Register Bit	Cell Type	I.D. Bit
A[3]	173	IN_CELL	-
A[2]	172	IN_CELL	-
A[1]	171	IN_CELL	-
Logic 1	170	IN_CELL	-
Logic 1	169	IN_CELL	-
NC	168	OUT_CELL	-
NC	167	IO_CELL	-
A[0]	166	IN_CELL	-
OEB_USER_OUT	165	OUT_CELL	-
USER_OUT	164	OUT_CELL	-
OEB_JUST_REQ	163	OUT_CELL	-
JUST_REQ	162	IO_CELL	-
NC	161	OUT_CELL	-
NC	160	OUT_CELL	-
NC	159	OUT_CELL	-
NC	158	OUT_CELL	-
NC	157	OUT_CELL	-
NC	156	OUT_CELL	-
NC	155	OUT_CELL	-
NC	154	OUT_CELL	-
NC	153	OUT_CELL	-
NC	152	OUT_CELL	-
NC	151	OUT_CELL	-
NC	150	OUT_CELL	-
NC	149	OUT_CELL	-
NC	148	OUT_CELL	-
NC	147	OUT_CELL	-
NC	146	OUT_CELL	-
NC	145	OUT_CELL	-
NC	144	OUT_CELL	-
NC	143	OUT_CELL	-
NC	142	OUT_CELL	-
NC	141	OUT_CELL	-
NC	140	OUT_CELL	-
NC	139	OUT_CELL	-
NC	138	OUT_CELL	-
NC	137	OUT_CELL	-
NC	136	OUT_CELL	-
NC	135	OUT_CELL	-
NC	134	OUT_CELL	-

Pin/ Enable	Register Bit	Cell Type	I.D. Bit
NC	133	OUT_CELL	-
NC	132	OUT_CELL	-
Logic 1	131	IN_CELL	-
OEB_INTB	130	OUT_CELL	-
INTB	129	OUT_CELL	-
NC	128	OUT_CELL	-
NC	127	OUT_CELL	-
NC	126	OUT_CELL	-
NC	125	OUT_CELL	-
NC	124	OUT_CELL	-
NC	123	OUT_CELL	-
NC	122	OUT_CELL	-
NC	121	OUT_CELL	-
NC	120	OUT_CELL	-
NC	119	OUT_CELL	-
NC	118	OUT_CELL	-
NC	117	OUT_CELL	-
NC	116	OUT_CELL	-
NC	115	OUT_CELL	-
NC	114	OUT_CELL	-
NC	113	OUT_CELL	-
NC	112	OUT_CELL	-
NC	111	OUT_CELL	-
NC	110	OUT_CELL	-
NC	109	OUT_CELL	-
NC	108	OUT_CELL	-
NC	107	OUT_CELL	-
NC	106	OUT_CELL	-
NC	105	OUT_CELL	-
IT AIS	104	IN_CELL	-
IPL	103	IN_CELL	-
IC1FP	102	IN_CELL	-
IV5	101	IN_CELL	-
ITPL	100	IN_CELL	-
IDP	99	IN_CELL	-
IDATA[7]	98	IN_CELL	-
IDATA[6]	97	IN_CELL	-
IDATA[5]	96	IN_CELL	-
IDATA[4]	95	IN_CELL	-
IDATA[3]	94	IN_CELL	-

Pin/ Enable	Register Bit	Cell Type	I.D. Bit
IDATA[2]	93	IN_CELL	-
IDATA[1]	92	IN_CELL	-
IDATA[0]	91	IN_CELL	-
NC	90	OUT_CELL	-
NC	89	OUT_CELL	-
SREFCLK	88	IN_CELL	-
SYSCLK	87	IN_CELL	-
NC	86	OUT_CELL	-
NC	85	IO_CELL	-
NC	84	OUT_CELL	-
NC	83	OUT_CELL	-
Logic 1	82	IN_CELL	-
OCMP	81	IN_CELL	-
ICMP	80	IN_CELL	-
NC	79	OUT_CELL	-
NC	78	OUT_CELL	-
NC	77	OUT_CELL	-
NC	76	OUT_CELL	-
Logic 1	75	IN_CELL	-
Logic 1	74	IN_CELL	-
Logic 1	73	IN_CELL	-
Logic 1	72	IN_CELL	-
Logic 1	71	IN_CELL	-
Logic 1	70	IN_CELL	-
Logic 1	69	IN_CELL	-
Logic 1	68	IN_CELL	-
Logic 1	67	IN_CELL	-
Logic 1	66	IN_CELL	-
Logic 1	65	IN_CELL	-
Logic 1	64	IN_CELL	-
Logic 1	63	IN_CELL	-
Logic 1	62	IN_CELL	-
OEB_OC1FP	61	OUT_CELL	-
OC1FP	60	OUT_CELL	-
OEB_OPL	59	OUT_CELL	-
OPL	58	OUT_CELL	-
OEB_OV5	57	OUT_CELL	-
OV5	56	OUT_CELL	-
OEB_OTPL	55	OUT_CELL	-
OTPL	54	OUT_CELL	-

Pin/ Enable	Register Bit	Cell Type	I.D. Bit
OEB_OTAIS	53	OUT_CELL	-
OT AIS	52	OUT_CELL	-
OEB_ODATA[7]	51	OUT_CELL	-
ODATA[7]	50	OUT_CELL	-
OEB_ODATA[6]	49	OUT_CELL	-
ODATA[6]	48	OUT_CELL	-
OEB_ODATA[5]	47	OUT_CELL	-
ODATA[5]	46	OUT_CELL	-
OEB_ODATA[4]	45	OUT_CELL	-
ODATA[4]	44	OUT_CELL	-
OEB_ODATA[3]	43	OUT_CELL	-
ODATA[3]	42	OUT_CELL	-
Logic 1	41	IN_CELL	-
NC	40	OUT_CELL	-
NC	39	OUT_CELL	-
NC	38	OUT_CELL	-
NC	37	OUT_CELL	-
NC	36	OUT_CELL	-
NC	35	OUT_CELL	-
Reserved	34	IN_CELL	-
NC	33	OUT_CELL	-
NC	32	OUT_CELL	-
NC	31	OUT_CELL	-
NC	30	OUT_CELL	-
NC	29	OUT_CELL	-
NC	28	OUT_CELL	-
OEB_ODATA[2]	27	OUT_CELL	-
ODATA[2]	26	OUT_CELL	-
OEB_ODATA[1]	25	OUT_CELL	-
ODATA[1]	24	OUT_CELL	-
OEB_ODATA[0]	23	OUT_CELL	-
ODATA[0]	22	OUT_CELL	-
OEB_ODP	21	OUT_CELL	-
ODP	20	OUT_CELL	-
NC	19	OUT_CELL	-
NC	18	OUT_CELL	-
NC	17	OUT_CELL	-
NC	16	OUT_CELL	-
NC	15	OUT_CELL	-
NC	14	OUT_CELL	-



Pin/ Enable	Register Bit	Cell Type	I.D. Bit
NC	13	OUT_CELL	-
NC	12	OUT_CELL	-
NC	11	OUT_CELL	-
NC	10	OUT_CELL	-
NC	9	OUT_CELL	-
NC	8	OUT_CELL	-
NC	7	OUT_CELL	-
NC	6	OUT_CELL	-
NC	5	OUT_CELL	-
NC	4	OUT_CELL	-
OEB_TC1FP	3	OUT_CELL	-
TC1FP	2	OUT_CELL	-
NC	1	OUT_CELL	-
NC	0	OUT_CELL	-

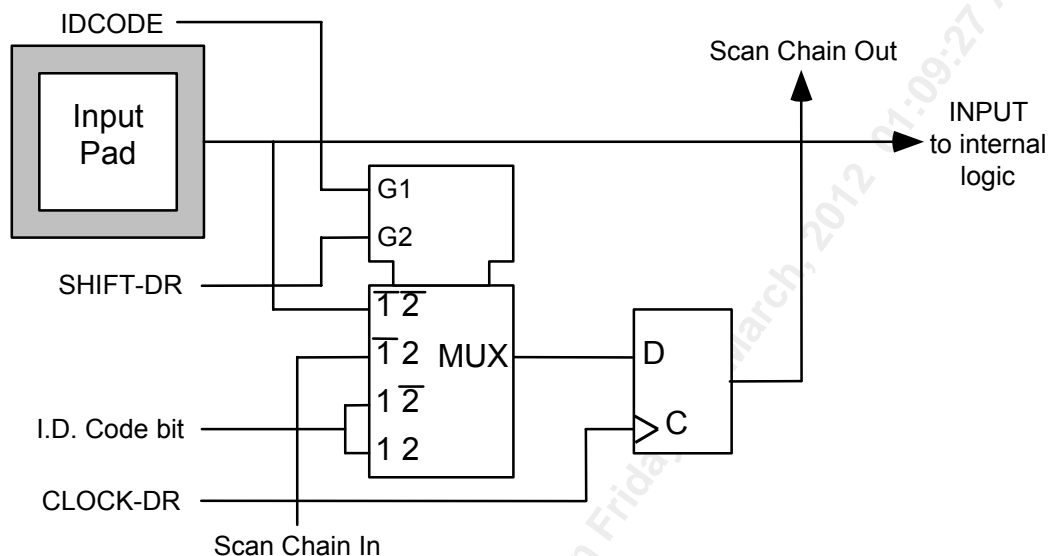
**Notes:**

1. When set high, INTB will be set to high impedance.
2. Enable cell OEB\_*pinname*, tristates pin *pinname* when set high.
3. The first bit of the boundary scan chain is Logic 1 (register bit 291).
4. Cells titled 'Logic 1' are Input Observation cells whose input pad has a pull-up and is unbonded.
5. Cells titled NC are Output or Bi-directional cells whose pad is unconnected to the device package.
6. The Output cell in register bit 264 is the active low output enable for the Bi-directional cell in register bit 263.
7. The Output cell in register bit 168 is the active low output enable for the Bi-directional cell in register bit 167.
8. The Output cell in register bit 86 is the active low output enable for the Bi-directional cell in register bit 85.

### 12.1.1 Boundary Scan Cells

In the following diagrams, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the center of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the Boundary Scan Register table located above.

**Figure 12 Input Observation Cell (IN\_CELL)**



**Figure 13 Output Cell (OUT\_CELL)**

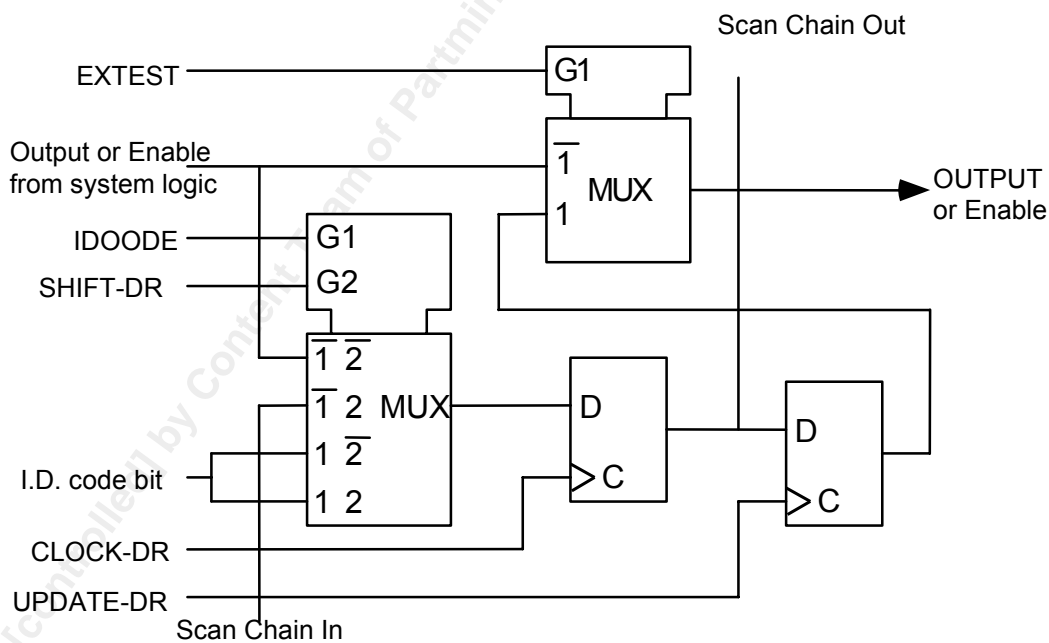


Figure 14 Bi-directional Cell (IO\_CELL)

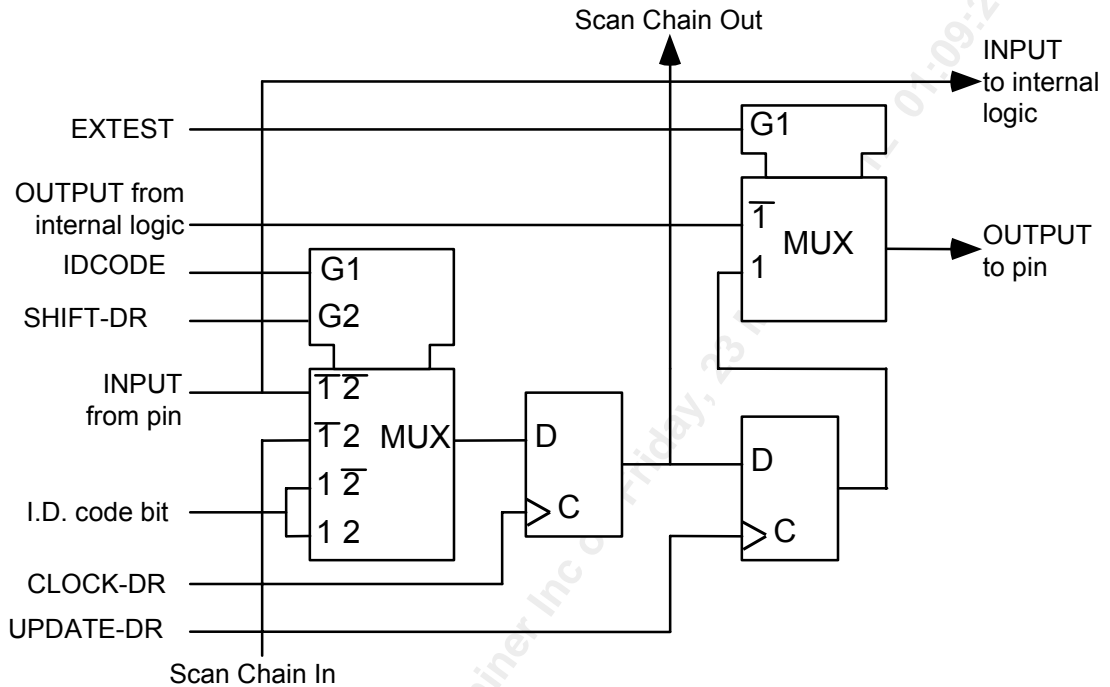
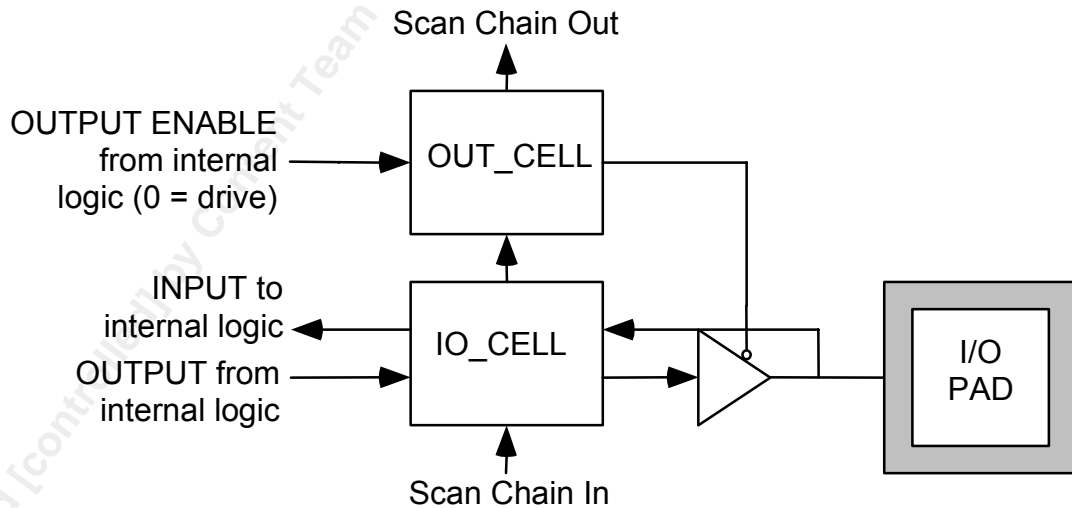


Figure 15 Layout of Output Enable and Bi-directional Cells



## 13 Operation

### 13.1 LVDS Optimizations

The LVDS interface implemented on the SBS, SBSLITE and NSE follows the IEEE 1596.3-1996 specification with some minor exceptions. The changes are implemented to customize and optimize the LVDS interface for the system and are described in detail below. Even with these differences the LVDS interface should be compatible with the physical layer of other LVDS interfaces. The differences from the IEEE specification include:

Faster rise/fall times (200 – 400) ps versus the specified (300 - 500) ps. Faster edge rates are commonly used with higher speed LVDS interfaces in the industry to ease interfacing. The IEEE 1596.3-1996 edge rates are optimized for data rates below 400 Mbps.

1. Hysteresis is not implemented in the receive LVDS interface. Hysteresis is used in many implementations to negate the effect of noise that may exist on unused LVDS links. Hysteresis was not implemented in the SBS, SBSLITE and NSE devices to minimize circuit complexity, power, and cost. Instead, the RX interfaces and the DRUs for unused links can be disabled (powered down) through register control in order to prevent sensitivity to noise on these links.
2. The LVDS transmitter contains an on-chip 100-ohm termination. Most implementations use a single 100-ohm termination on the receiver. By implementing a double termination (on both the LVDS receiver and transmitter) better signal integrity and matching is ensured.
3. Although not a difference with the Layer 1 IEEE 1596.3-1996 specification, the Layer 2 8B/10B encoding is discussed here for completeness. 8B/10B encoding guarantees transition density as compared to scrambled encoding, which provides only a certain probability of transition density. This guaranteed transition density allows a simpler and more power-effective data recovery unit, provides a more robust serial interface (greater trace or back-plane distance achievable). It also negates the need for complete SONET framing since the A1A2 and J0 bytes can be encoded into special escape characters of the LVDS data stream.
4. The device uses 20% resistors; not 10% as specified by the LVDS specification. They are 20% resistors since that was the highest tolerance resistor available for on-chip applications. However, because they are integrated on-chip, this LVDS interface can achieve much better signal integrity than one with off-chip terminations.

## 13.2 LVDS Hot Swapping

The LVDS electrical interface differs from a standard CMOS interface; there is no inherent problem in leaving the LVDS inputs floating. Note that the LVDS receiver consists of a differential amplifier with a wide common-mode range. The power dissipation is independent of the data transitions (that is, if the input is connected). There is an internal 100  $\Omega$  termination across the positive and negative input. Floating inputs will settle to an arbitrary voltage (between VDD and VSS) determined by leakage paths. Regardless of this arbitrary voltage, the input structure of the receiver will operate in its proper range and the receiver output will be logic 1 or 0 depending on internal offsets. Noise events (power supply noise, crosstalk) may induce the receiver to toggle randomly, generating "ambiguous" data. This ambiguous data will not result in any problems but is not a desirable condition since it simply wastes power.

Unused links should be disabled in software. This will ensure that the power consumption for those links will be reduced to nearly 0 mW. There is no requirement for how quickly the link should be disabled. Disabling the link simply results in lower power dissipation since the circuitry will be shut down. This action is not mandatory, but is good practice.

During a hot-swapping situation, there will be no electrical damage on the LVDS inputs provided that maximum ratings are not exceeded (see absolute maximum ratings section 15). There are no problems with hot-swapping. The "hot-swap" channel can be left enabled and the device will sync up once the far end transmitter is connected. There are no effects on other channels. Hot swapping of cards is still allowed by reprogramming of the links in software. The framing algorithm used in the receive framer blocks will keep the receiver in an out-of-frame state in the case of a link being hot swapped while still enabled. The device will pass on the random data received on this link, or the user may choose to pass on an AIS indication via register configuration. Despite passing on random data, control signals will be suppressed such that there will be no false J0 indications on the outgoing SBI or TelecomBus.

## 13.3 Selecting Between the Receive Working and Protection Links

The data from only one of the two receive links is propagated to the Outgoing Bus on the SBS. The selection of which link, the working or protect, the SBSLITE listens to is controlled by the RWSEL input or the RWSEL\_VAL bit in register 001H. If the RWSEL\_SRC bit in register 001H is set to a logic 0, the RWSEL\_VAL bit is used to select the active link. If RWSEL\_SRC is a logic 1, the RWSEL input is used to select the active link.

RWSEL is sampled at the C1 position of every frame, as marked by the RC1FP input, and when a change is detected the switching between the links is synchronized to the first byte of the following frame. This allows for a controlled switch between the working and protection links.

Note that both the working and protection PRBS monitors and in-band link controllers are active regardless of which link is selected by RWSEL. This provides a method to monitor the inactive link without disrupting the data on the active link.

## 13.4 Interrupt Service Routing

The SBSLITE will assert the INTB output to a logic 0 when a condition that is configured to produce an interrupt occurs. To find which condition caused this interrupt to occur, the procedure outlined below should be followed:

Read the SBSLITE Master Interrupt Source Register (010H) to find the functional block which caused the interrupt.

Find the register address of the corresponding block that caused the interrupt and read its Interrupt Status registers. The interrupt bits in the functional block and the interrupt source identification bits from step 1 are cleared once these register(s) have been read and the interrupt(s) identified.

Service the interrupt(s).

If the INTB pin is still logic 0, then there are still interrupts to be serviced and steps 1 to 3 need to be repeated. Otherwise, all interrupts have been serviced. Wait for the next assertion of INTB.

Note that all interrupts in the SBSLITE may be disabled by setting the INTE bit of the SBSLITE Master Interrupt Enable Register (016H) to a logic 0. Interrupts may also be disabled on a block by block basis by setting the appropriate block enable bits in this register to a logic 0.

## 13.5 Accessing Indirect Registers

Indirect registers are used to conserve address space in the SBSLITE.

### 13.5.1 Accessing Indirect Registers in the ICASM, OCASM, ISTT and OSTT

When writing to an indirect register in the ICASM, OCASM, ISTT or OSTT, the following procedure should be followed:

- Read the BUSY bit in the Indirect Access Control Register. If it is a logic 0, continue to step 2. If it is a logic 1, continue polling the BUSY bit.
- Write the desired configuration for the tributary into the Indirect Access Data Register.
- Write the desired tributary number into the Indirect Access Address Register.
- Write to the Indirect Access Control Register with RWB set to logic 0.
- Read the BUSY bit. Once it is a logic 0, the indirect write has been completed.
- When reading an indirect register from the ICASM, OCASM, ISTT or OSTT, the following procedure should be followed:
  - Read the BUSY bit in the Indirect Access Control Register. If it is a logic 0, continue to step 2. If it is a logic 1, continue polling the BUSY bit.
  - Write the desired tributary number into the Indirect Access Address Register.

- Write to the Indirect Access Control Register with RWB set to logic 1.
- Read the BUSY bit. If it is a logic 0, continue to step 5. If it is a logic 1, continue polling the BUSY bit.
- Read the Indirect Access Data Register to find the state of the register bits for the selected tributary.

### 13.5.2 Accessing Indirect Registers in the WPP and PPP

When writing to an indirect register in the WPP or PPP, the following procedure should be followed:

- Read the BUSY bit in the Indirect Access Register. If it is a logic 0, continue to step 2. If it is a logic 1, continue polling the BUSY bit.
- Write the desired configuration into the Indirect Data Register.
- Write the desired path number and indirect address number into the Indirect Address Register with RDWRB set to logic 0.
- Read the BUSY bit. Once it is a logic 0, the indirect write has been completed.
- When reading an indirect register from the WPP or PPP, the following procedure should be followed:
- Read the BUSY bit in the Indirect Access Register. If it is a logic 0, continue to step 2. If it is a logic 1, continue polling the BUSY bit.
- Write the desired path number and indirect address number into the Indirect Address Register with RDWRB set to logic 1.
- Read the BUSY bit. If it is a logic 0, continue to step 4. If it is a logic 1, continue polling the BUSY bit.
- Read the Indirect Data Register to find the state of the register bits for the selected path and indirect address.

### 13.5.3 Software Design Notes:

Software should not attempt to write to indirect addresses other than those specifically mentioned in the register description. Other indirect addresses should be considered reserved.

Software should implement a timeout so that a BUSY bit which is stuck at 1 will not cause an infinite loop in the software. BUSY bits will not be stuck at 1 in normal operation, but may become stuck at 1 if an invalid access is attempted, or an access is attempted while the device is not being clocked.

## 13.6 Using the Performance Monitoring Features

The performance monitor counters within the different blocks are provided for performance monitoring purposes. All performance monitor counters have been sized to not saturate if polled at regular intervals. The counters will saturate and not roll over if they reach their maximum value.

Writing to the SBSLITE Master Signal Monitor #1, Accumulation Trigger Register (014H) causes a device update of all the counters. If this register is written to, the TIP bit in the SBSLITE Receive Synchronization Delay Register (007H) can be polled to determine when all the counter values have been transferred and are ready to be read. Alternately, software can wait the number of SYSCLK cycles shown in

**Table 27 Maximum Performance Monitor Counter Transfer Time**

Trigger Register Address	Block Name	SYSCLK cycles to complete transfer (MAX)
014H	All Blocks (WPP, PPP, RW8D and RP8D)	17
07CH	WPP	17
08CH	PPP	17
0C2H	RW8D	6
0CAH	RP8D	6

### 13.7 Configuring the Transmit Encoders (TW8E and TP8E)

The transmit encoder blocks (TW8E and TP8E) may be configured in one of three possible termination modes. The selection between the three modes is performed at the STS/AU level. The three modes are:

**Low Order Path Termination Mode (LPT).** This mode must be used when connecting the SBS to an SBI or SBI336 bus. This mode may also be used when connecting the SBS to a TelecomBus where the V5 and TPL signals must be preserved across the Serial TelecomBus. The ERDI[1:0] and REI bits of the V5 byte (bits 0, 4 and 5) will be preserved but the remaining bits will be set to zero by the receive decoder at the far end of the serial link. The V1 and V2 pointers will also be set to all zeros.

**High Order Path Termination Mode (HPT).** This mode may be used when connecting the SBS to a TelecomBus where the V1 and V2 pointers must be preserved across the Serial TelecomBus. Note that in this mode, the V5 signal will be zeroed out by the receive decoder at the far end of the serial link, but the data within the V5 byte will be preserved. In this mode the J1 byte will be overwritten with a control character on the serial link.

**Multiplex Section Termination Mode (MST).** This mode may be used when connecting the SBS to a TelecomBus where H1 and H2 pointers must be preserved across the Serial TelecomBus and the J1 byte cannot be overwritten. Note that in this mode, a receiving device must use the H1/H2 pointers to locate the J1 byte position.

The selection of the termination mode is contained in registers 0B2H and 0B3H for the TW8E, and in registers 0BAH and 0BBH for the TP8E.



## 13.8 Interpreting the Status of the Receive Decoders (RW8D and RP8D)

The receive decoded blocks (RW8D and RP8D) produce interrupts based on four receiver conditions or events: OCA (Out of Character Alignment), OFA (Out of Frame Alignment), FUI (FIFO Underrun/Overrun) and LCV (Line Code Violation). Understanding the relationship between these conditions can help to diagnose device status. These conditions have the following interrelationships:

OCA implies OFA until character alignment is re-achieved. OCA will most likely cause some LCVs but not necessarily a continual stream. Since character boundaries are not known, framing and disparity are meaningless.

OFA, by itself, does not cause any of the other conditions.

FUI may produce zero, one or many OCVs, depending on how the FIFO underrun/overrun occurs.

Persistent LCVs (five or more in any sequence of 15 characters) cause OCA.

## 13.9 Using the Memory Switch Units (IMSU and OMSU)

The Memory Switch Unit (MSU) blocks in the SBS (IMSU and OMSU) can be used to rearrange the position of the bytes (or columns) within the SBI336 or TelecomBus frame. Each block buffers an entire frame (9720 bytes) or row (1080 columns) and rearranges them before outputting them.

### 13.9.1 Selection Between the Two Connection Memory Pages

The selection of which input byte (or column) is to be output at each output byte (or column) location is controlled by the settings in the connect memory pages. There are two connection memory pages, one of which is used to control the switching function while the other may be modified with new connections through the microprocessor interface.

The two pages can be swapped by changing the CMP value. There are three possible sources for the CMP value. They are the ICMP/OCMP input pins, the ICMP\_VAL/OCMP\_VAL bits in the SBSLITE Master Configuration Register (001H), and the PAGE[1:0] bits from the ILC block on the active receive link. The selection of the source of CMP is controlled by the setting of the ICMP\_SRC[1:0]/OCMP\_SRC[1:0] bits in the SBSLITE Master Configuration Register (001H).

### 13.9.2 Procedure for Writing to the Connection Memory Page

When writing to a location in the connection memory page in the IMSU or OMSU, the following procedure should be followed:

- Write the desired configuration into the Indirect Time Switch Data Register.

- Write to the desired address into the Indirect Time Switch Address Register with RWB set to logic 0.
- Wait for a minimum of 4 SYSCLK cycles before repeating for the next address.
- When reading from a location in the connection memory page in the IMSU or OMSU, the following procedure should be followed:
- Write the desired address location into the Indirect Time Switch Address Register with RWB set to logic 1.
- Wait a minimum of 8 SYSCLK cycles.
- Read the value from the Indirect Time Switch Data Register and check the VALID bit. If the VALID bit is a logic 0, the data in the register is not valid and this register should be read again. If the VALID bit is a logic 1, the value in the IN\_BYTE[13:0] bits is valid.

### 13.9.3 MSU Ram Address Map

Each ram location in the connection memory page corresponds to a byte (or column) in the SBI336 or TelecomBus being output from the MSU. The data contained in the ram location points to the byte (or column) from the input SBI336 or TelecomBus which is to be switched to the output. In byte mode, ram address 0 corresponds to the first byte in the frame, and ram address 9719 corresponds to the last byte in the frame. In column mode, ram address 0 corresponds to the first column in the frame and ram address 1079 corresponds to the last column in the frame.

### 13.9.4 Example Column Mode Addresses for TU-11 Tributaries (AU-3)

The following table shows the ram addresses for each column for AU-3 traffic containing TU-11 tributaries.

Column	Transport Overhead	VC-3 Path Overhead	TU-11 #1	TU-11 #2 - #336	Fixed Stuff	TU-11 #1	TU-11 #2 - #336	Fixed Stuff	TU-11 #1	TU-11 #2 - #336
Column	0 – 35	36 – 47	48	49 – 383	384 – 395	396	397 – 731	732 – 743	744	745 - 1079

### 13.9.5 Example Column Mode Addresses for TU-11 Tributaries (SDH AU-4 or SBI336)

The following table shows the ram addresses for each column for AU-4 traffic containing TU-11 tributaries. Note that for SBI336 traffic, columns 0 – 71 are all considered unused.

Column	Transport Overhead	VC-4 Path Overhead	Fixed Stuff	TU-11 #1	TU-11 #2 - #336	TU-11 #1	TU-11 #2 - #336	TU-11 #1	TU-11 #2 - #336
Column	0 – 35	36 – 39	40 – 71	72	73 – 407	408	409 – 743	744	745 - 1079

### 13.9.6 Example Byte Mode Addresses for TU-11 Tributaries (SDH AU-4 or SBI336)

The following table shows the ram addresses for each byte for AU-4 traffic containing TU-11 tributaries. Note that for SBI336 traffic, all bytes in the Transport Overhead, Path Overhead and Fixed Stuff columns are considered unused.

	Transport Overhead	VC-4 Path Overhead	Fixed Stuff	TU-11 #1	TU-11 #2 - #336	TU-11 #1	TU-11 #2 - #336	TU-11 #1	TU-11 #2 - #336
1	0 – 35	36 – 39	40 – 71	72	73 – 407	408	409 – 743	744	745 - 1079
2	1080 – 1115	1116 – 1119	1120 – 1151	1152	1153 – 1487	1488	1489 – 1823	1824	1825 – 2159
3	2160 – 2195	2196 – 2199	...						
4	3240 – 3275	3276 – 3279	...						
5	4320 – 4355	4356 – 4359	...						
6	5400 – 5435	5436 – 5439	...						
7	6480 – 6515	6516 – 6519	...						
8	7560 – 7595	7596 – 7599	...						
9	8640 – 8675	8676 – 8679	8680 – 8711	8712	8713 – 9047	9048	9049 – 9383	9384	9385 – 9719

### 13.10 Using the PRBS Generator and Monitors (WPP and PPP)

A pseudo-random (using the  $X^{23} + X^{18} + 1$  polynomial) or incrementing pattern can be inserted/extracted in the SONET/SDH payload. With PRBS data and incrementing data patterns, the payload envelope is filled with pseudo-random/incrementing bytes with the exception of POH and fixed stuff columns. In the case of the incrementing counts, the count starts at 0 and increments to FFh before the count starts over at 0 once again. The incrementing count is free to float within the payload envelope and therefore the 0 count is not associated with any fixed location within a payload envelope. This PRBS generator and monitor is compatible with the PRBS generators and monitors in other CHESS™ Set devices. It may not be compatible with external test equipment.

#### 13.10.1 Mixed Payload (STS-12c/STM-4/AU4-4c, STS-3c/STM-1, and STS-1/STM-0)

The WPP and PPP are designed to process the payload of an STS-12/STM-4 frame in a time-multiplexed manner. Each time division (12 STS-1/STM-0 paths) can be programmed to a granularity of an STS-1/STM-0. It is possible to process one STS-12c/STM-4c, twelve STS-1/STM-0 or four STS-3c/STM-1 or a mix of STS-1/STM-0 and STS-3c/STM-1 as long as the aggregate data rate is not more than one STS-12/STM-4 equivalent. The mixed payload configuration can support the three STS-1/STM-0 and STS-3c/STM-1 combinations shown below:

- Three STS-1/STM-0 with three STS-3c/STM-1
- Six STS-1/STM-0 with two STS-3c/STM-1

- Nine STS-1/STM-0 with one STS-3c/STM-1

The STS-1/STM-0 path that each one of the payload occupies, cannot be chosen randomly. They must be placed on STS-3c/STM-1 boundaries (group of three STS-1/STM-0).

### 13.10.2 Synchronization

Before being able to monitor the correctness of the PRBS payload, the monitor must synchronize to the incoming PRBS. The process of synchronization involves synchronizing the monitoring LFSR to the transmitting LFSR. Once the two are synchronized the monitoring LFSR is able to generate the next expected PRBS bytes. When receiving sequential PRBS bytes (STS-12c/VC-4-4c), the LFSR state is determined after receiving 3 PRBS bytes (24 bits of the sequence). The last 23 of 24 bits (excluding MSB of first received byte) would give the complete LFSR state. The 8 newly generated LFSR bits after a shift by 8 (last 8 XOR products) will produce the next expected PRBS byte.

The implemented algorithm requires four PRBS bytes of the same payload to ascertain the LFSR state. From this recovered LFSR state the next expected PRBS byte is calculated.

Out of Synchronization and Synchronized states are defined for the monitor. While in progress of synchronizing to the incoming PRBS stream, the monitor is out of synchronization and remains in this state until the LFSR state is recovered and the state has been verified by receiving 4 consecutive PRBS bytes without error. The monitor will then change to the Synchronized State and remains in that state until forced to resynchronize via the RESYNC register bit or upon receiving 3 consecutive bytes with errors. When forced to resynchronize, the monitor changes to the Out of Synchronization State and tries to regain synchronization. It is important to note however that the monitor can falsely synchronize to an all zero pattern. If inverted PRBS is selected, the monitor can falsely synchronize to an all 1 pattern. It is therefore recommended that users poll the monitor's LFSR value after synchronization has been declared, to confirm that the value is neither all 1s or all 0s.

Upon detecting 3 consecutive PRBS byte errors, the monitor will enter the Out of Synchronization State and automatically try to resynchronize to the incoming PRBS stream. Once synchronized to the incoming stream, it will take 4 consecutive non-erred PRBS bytes to change back into the Synchronized State. The auto synchronization is useful when the input frame alignment of the monitored stream changes. The realignment will affect the PRBS sequence causing all input PRBS bytes to mismatch and forcing the need for a resynchronization of the monitor. The auto resynchronization does this, detecting a burst of errors and automatically re-synchronizing.

### 13.10.3 Error Detection and Accumulation

By comparing the received PRBS byte with the calculated PRBS byte, the monitor is able to detect byte errors in the payload. A byte error is detected on a comparison mismatch of the two bytes. Only a single byte error is counted regardless of the number of erroneous bits in the byte. All byte errors are accumulated in a 16 bit byte error counter. The error counter will saturate at its maximum value of FFFFh, i.e. it will not wrap around to 0000h if further PRBS byte errors are encountered. The counter is readable via the WPP Monitor Error Count Register or the PPP Monitor Error Count Register. The error counter is cleared when transferred into the registers and the accumulation restarts at zero. When reading error counts for concatenated payloads of STS-3c /STM-1c or STS-12c/STM-3c sizes, it is necessary to read the error count in all slices (all associated STS-1/STM-0's). For each independent STS-1/STM-0 monitored by a PRGM, the error count register for each individual STS-1/STM-0 must be read.

Byte errors are accumulated only when the monitor is in synchronized state. To enter the synchronize state, the monitor must have synchronized to the incoming PRBS stream and received 4 consecutive bytes without errors. Once synchronized, the monitor falls out of synchronization when forced to by programming the RESYNC register bit high, or once it detects 3 consecutive PRBS byte errors. When out of synchronization, detected errors are not accumulated.

## 13.11 Using the In-Band Link Controller (WILC and PILC)

The In-Band Link Controllers provides a mechanism for communication between devices over the serial interface. The ILC inserts and retrieves messages from the transport overhead of the SBI336 or TelecomBus frame. The messages are 36 bytes each and 4 messages are transmitter each frame. These messages are inserted into the Data Communication Channel (DCC) bytes, in rows 3,6,7 and 8. Each message contains 2 header bytes, 32 bytes containing the free format information, and 2 bytes for a CRC-16. There is an independent in-band link controller for working and the protection links (WILC for the working link and PILC for the protection link).

If no information bytes are available to transmit, the ILC will continue to send messages but will insert all zeros into the information bytes and will set the VALID bit in the header to zero. The header and CRC bytes will be transmitted normally. When the receive link recognizes that the VALID bit is a zero, it will not write the all zero message into the receive FIFO.

### 13.11.1 Transmitting Messages

When writing to the transmit FIFO in the WILC or PILC, the following procedure should be followed:

- Write a logic 1 to the TX\_XFER\_SYNC bit of the Transmit Status and FIFO Synch Register (095H or 0A5H). This will ensure the subsequent writes to the FIFO start at the beginning of a message.
- Write to the Transmit Data High Register (090H or 0A0H).
- Write to the Transmit Data Low Register (091H or 0A1H). Writing to this register will initiate a transfer of the Transmit Data High Register and Transmit Data Low Register into the transmit FIFO.

- Read the TX\_FI\_BUSY bit in the Transmit Status and FIFO Synch Register (095H or 0A5H) or wait a minimum of 3 SYSCLK cycles. If TX\_FI\_BUSY is a logic 0, continue to step 5. If it is a logic 1, continue polling the TX\_FI\_BUSY bit.
- Loop back to Step 2 until the entire message has been written in to the FIFO.

When transmitting multiple 32 byte messages, the TX\_XFER\_SYNC bit does not have to be written to between each message.

When transmitting a message shorter than 32 bytes, the TX\_XFER\_SYNC bit should be set after writing the last byte of the message into the FIFO. This will allow the short message to be transmitted and move the FIFO to the next 32 byte partition.

### 13.11.2 Retrieving Messages

When reading messages from the receive FIFO in the WILC or PILC, the following procedure should be followed:

- Write a logic 1 to the RX\_XFER\_SYNC bit of the Receive Status and FIFO Synch Register (09BH or 0ABH). This will initiate a read from the receive FIFO.
- Read the RX\_FI\_BUSY bit in the Receive Status and FIFO Synch Register (09BH or 0ABH) or wait a minimum of 4 SYSCLK cycles. If RX\_FI\_BUSY is a logic 0, continue to step 3. If it is a logic 1, continue polling the RX\_FI\_BUSY bit.
- Read the Receive Status and FIFO Synch Register (09BH or 0ABH) and check the state of the CRC\_ERR. If this bit is a logic 1, the current message in the FIFO had a CRC error and the data is not reliable and the user may want to skip to the next message. This may be done by writing logic 1 to the RX\_XFER\_SYNC bit (09BH or 0ABH), then returning to step 1.
- Read the Receive FIFO Data High Register (096H or 0A6H).
- Read the Receive FIFO Data Low Register (097H or 0A7H).
- Read the RX\_FI\_BUSY bit in the Receive Status and FIFO Synch Register (09BH or 0ABH) or wait a minimum of 4 SYSCLK cycles. If RX\_FI\_BUSY is a logic 0, continue to step 7. If it is a logic 1, continue polling the RX\_FI\_BUSY bit.
- Loop back to Step 4 until the entire message has been read out of the FIFO.

When reading more than one message from the receive FIFO, the RX\_XFER\_SYNC does not have to be set between each message.

Before reading the any messages, the software may want to check how many messages are contained in the receive FIFO. This can be done by reading the RX\_MSG\_LVL[3:0] bits in the Receive Status and FIFO Synch Register (09BH or 0ABH). When reading these bits, the RX\_STTS\_VALID bit must also be checked. If RX\_STTS\_VALID is a logic 1, the RX\_MSG\_LVL[3:0] bits are valid. If RX\_STTS\_VALID is a logic 0, the RX\_MSG\_LVL[3:0] bits are not valid and this register should be read again until RX\_STTS\_VALID is a logic 1.

### 13.11.3 Transmit Message Header Bytes

**LINK[1:0]:** These bits reflect the state of the TX\_LINK[1:0] bits in the Transmit Control Register (093H or 0A3H).

**PAGE[1:0]:** These bits reflect the state of the CMP value used by each of the MSU blocks. PAGE[1] reflects the current memory page used by the IMSU. PAGE[0] reflects the current memory page used by the OMSU.

**USER[2:0]:** The USER[2] bit reflects the state of the IUSER2 input to the SBSLITE. The USER[1:0] bits transmitted by the WILC reflects the state of the TXWUSER[1:0] bits in register 008H. The USER[1:0] bits transmitted by the PILC reflects the state of the TXPUSER[1:0] bits in register 008H.

**AUX[7:0]:** These bits reflect the state of the TX\_AUX[7:0] bits in the Transmit Control Register (093H or 0A3H).

### 13.11.4 Receive Message Header Bytes

**LINK[1:0]:** The LINK[1:0] bits from the latest received message are reflected in the RX\_LINK[1:0] bits of the Receive Status and FIFO Synch Register (09DH or 0ADH). These bits are only update if the receive message contains a correct CRC value. If the CRC is in error, these bits will keep their previous value. A change in state of either of these bits can be configured to cause an interrupt by setting the RX\_LINK\_CHGE bit in the Interrupt Enable and Control Register (09DH or 0ADH).

**PAGE[1:0]:** The PAGE[1:0] bits from the latest received message are reflected in the OPAGE[1:0] bits of the Receive Status and FIFO Synch Register (09DH or 0ADH). The PAGE[1:0] bits on the active link (as selected by RWSEL) may be used to control the connection memory pages of the MSU blocks. PAGE[1] will control the CMP value for the IMSU when the ICMP\_SRC[1:0] bits in register 001H are set to "10". PAGE[0] will control the CMP value for the OMSU when the OCOMP\_SRC[1:0] bits in register 001H are set to "10". These bits are only update if the receive message contains a correct CRC value. If the CRC is in error, these bits will keep their previous value. A change in state in either of these bits can be configured to cause an interrupt by setting the OPAGE\_CHGE[1:0] bits in the Interrupt Enable and Control Register (09DH or 0ADH).

**USER[2:0]:** The USER[2:0] bits from the latest received message are reflected in the OUSER[2:0] bits of the Receive Status and FIFO Synch Register (09DH or 0ADH). The USER[2] from the active link (as selected by RWSEL) will also be output on the OUSER2 output of the SBSLITE. These bits are only update if the receive message contains a correct CRC value. If the CRC is in error, these bits will keep their previous value.

**AUX[7:0]:** The AUX[7:0] bits from the latest received message are reflected in the RX\_AUX[7:0] bits of the Receive Auxiliary Register (09AH or 0AAH). These bits are only update if the receive message contains a correct CRC value. If the CRC is in error, these bits will keep their previous value.

### 13.11.5 Disabling the ILC

The functions of the WILC and PILC blocks may be disabled. When disabled, no messages are inserted or retrieved. All data passes through the ILC unmodified.

The TX\_BYPASS bit in the Transmit Control Register (093H or 0A3H) will disable the transmit half of the ILC. The RX\_BYPASS bit in the Receive FIFO Control Register (099H or 0A9H) will disable the receive half of the ILC.

### 13.12 Using J1 and V1 insertion registers

Registers 061H and 062H allow for the insertion of J1 and V1 indicators on the OC1FP signal. By using these registers, it is possible to insert J1 and V1 indicators at STS/AU granularity. The OLOCK0 bit in register 060H controls the position of the J1 indicators, which may either follow C1 (Z0) or H3. On the multiframe, V1 indicators always follow the J1 indicator.

These registers should not be used in SBI mode. In TelecomBus mode, the registers act as an OR function with existing J1 indicators, and should not be used with STS/AUs where J1 is floating. When J1 is fixed to 0 or 522, the incoming J1 from the serial link will still propagate through the device, and setting the appropriate J1 indicator will have no additional effect; however, V1 insertion may be used in this case to mark the multiframe.

### 13.13 “C1” Synchronization

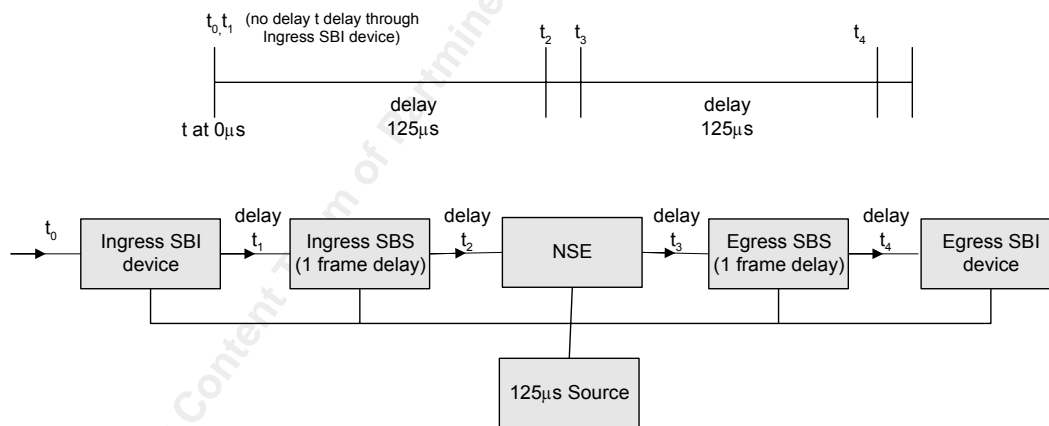
Any NSE/SBSLITE fabric can be viewed as a collection of five “columns” of devices: column 0 consists of the ingress flow from the load devices (e.g., some SBI device); column 1 consists of the ingress flow through the SBSLITE devices; column 2 consists of the NSE-20G device; column 3 consists of the egress flow through the SBSLITE devices; and column 4 consists of the egress flow through the load devices (e.g. some SBI device). Note that the devices in columns 0 and 4 are SBI bus devices while columns 1 and 3 are SBS or SBSLITE devices. The dual column references refer to their two separate simplex flows. Path-aligned STS-12/STM-4 frames are pipelined through this structure in a regular fashion, under control of a single clock source and frame pulse. There are latencies between these columns, and these latencies may vary from path to path. The following design is used to accommodate these latencies.



A timing pulse for SBI frames (2kHz, 500  $\mu$ s) is generated and fed to each device in the fabric. Each chip has a *FrameDelay* register (RC1DLY) which contains the count of 77.76 MHz clock ticks that device should delay from the reference timing pulse before expecting the C1 characters of the ingress STS-12/STM-4 frames to have arrived. The base timing pulse is called  $t$ . The delays from  $t$  based on the settings of the RC1DLY registers in the successive columns of the devices are called  $t_0, \dots, t_4$ . The first signal,  $t_1$  (equal to  $t_0$ ), determines the start of an STS-12/STM-4 frame; this signal is used to instruct the ingress load devices (column 0) to start emitting an STS-12/STM-4 frame (with its special “C1” control character) at that time.  $t_1$  is determined by the customer, based on device and wiring delays to be approximately the earliest time that all “C1” characters will have arrived in the ingress FIFOs of the  $t_1$  column of devices.  $t_1$  is selected to provide assurance that all “C1” characters have arrived at the  $i^{\text{th}}$  column. The  $i^{\text{th}}$  column of devices use the  $t_i$  signal to synchronize emission of the STS-12/STM-4 frames. The ingress FIFOs permit a variable latency in C1 arrival of up to 24 clock cycles.

Note: the SBSLITE device, being a memory switch adds a latency of one complete frame plus a few clock ticks to the data in DS0 switching mode. In column switching mode, the latency is one row plus a few clock ticks.

**Figure 16 “C1” Synchronization Control**



### 13.14 Synchronized Control Setting Changes

The NSE-20G and SBSLITE support dual switch control settings. These dual settings permit one bank of settings to be operational while the other bank is updated as a result of some new connection requests. The CMP input selects the current operational switch control settings. CMP is sampled by the SBSLITE and the NSE-20G on the base timing pulse  $t$ . The internal blocks sample the registered CMP value as they receive the next C1 character—at least a delay of RC1DLY. The new CMP value is applied on the first A1 character of the following STS-12/STM-4 frame or multi-frame. This switchover is hitless; the control change does not disrupt the user data flow in any way. This feature is required for the addition of arbitrary new connections, as existing connections may need to be rerouted (see the discussion of the connection routing algorithm in this document).

The DS0-granularity switch settings RAM is organized into two control settings banks, these are switched by the above mechanisms on C1 boundaries. The NSE also has to coordinate the switching of the connected SBSLITE devices (if using the In-Band link facility), so a broader understanding of the issues is required.

To illustrate the system, the following describes actual examples:

### 13.14.1 SBS/NSE Systems with DS0 and CAS Switching

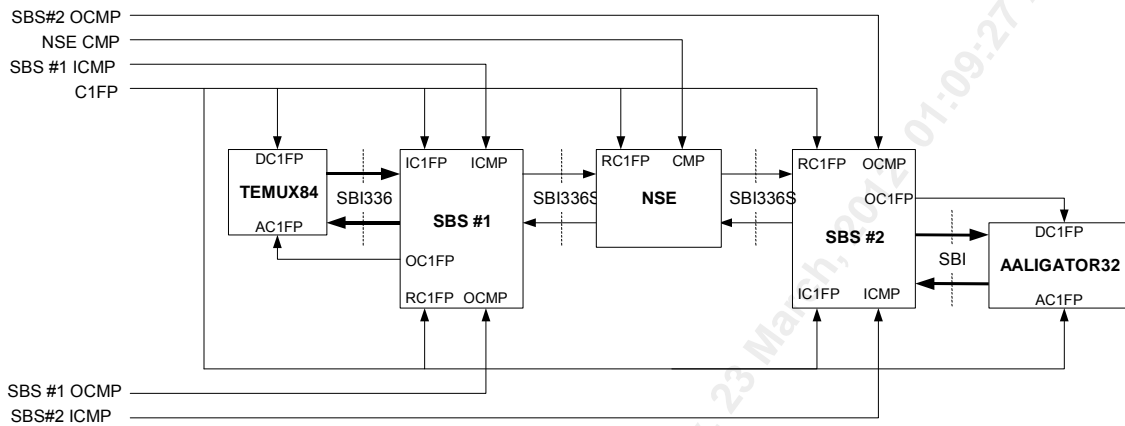
When building a DS0 and Channel Associated Signaling switching system with the SBS, SBSLITE and NSE devices the overall timing is based on the CAS signaling multi-frame on the SBI bus. In this configuration the delay through the SBSLITE devices is a single 125uS SBI frame plus a few 77.76MHz clocks and the delay through the NSE is a few 77.76MHz clocks. A single C1FP frame synchronization signal is distributed around the system. Internal to the SBSLITE and NSE devices are programmable offsets used to account for propagation delays through the system. The key constraint is that all SBI frames are aligned going into the NSE device.

Compatible devices are TEMUX84, FREEDM336, FREEDM336-84, IMA84, and other future SBI336 devices.

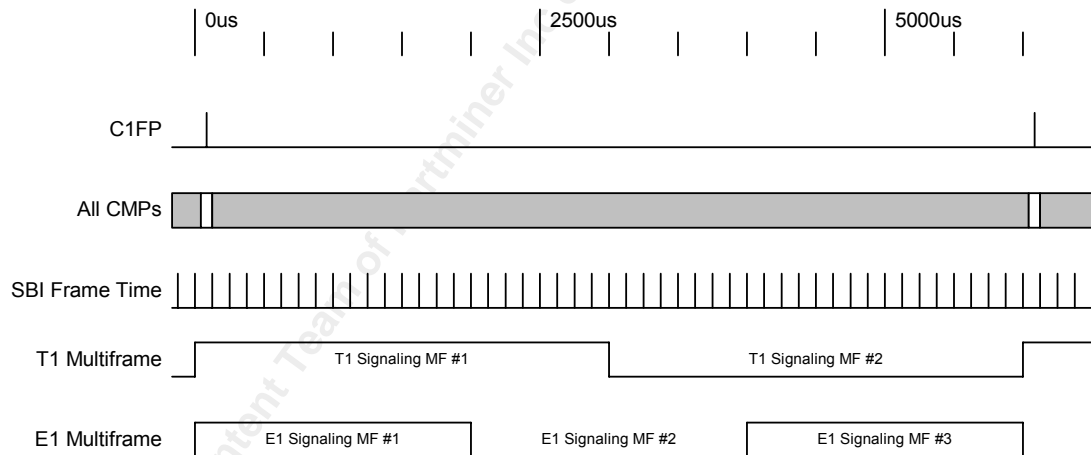
The SBSLITE and NSE devices have two configuration pages controlling the switching of each DS0 with CAS. The SBSLITE has independent configuration pages for each direction of data flow through the device. The NSE has one set of configuration pages. System configuration changes are made by writing to the offline configuration page in all affected devices and then swapping from the old configuration page to the new configuration page. The ICMP and OCMP signals control the current configuration page of the SBSLITE and the CMP signal controls the current configuration page of the NSE. Swapping of configuration pages must be aligned to frame switching through the system to avoid any possible data corruption. The ICMP, OCMP and CMP signals are sampled with the SBSLITE IC1FP and RC1FP signals and the NSE RC1FP signals respectively. The CMP signals can be connected together at the expense of having to ensure all device configuration pages are current.

The following diagram shows how the devices are connected together. The following timing diagrams show the external signals and the internal device frame alignment signal generated from the programmed delays. Although the CMP signals are sampled externally with the C1FP signals they are also delayed internally to coincide with the internally delayed frame signals. These are also shown in the timing diagram. All internal signals are identified by the .INT suffix.

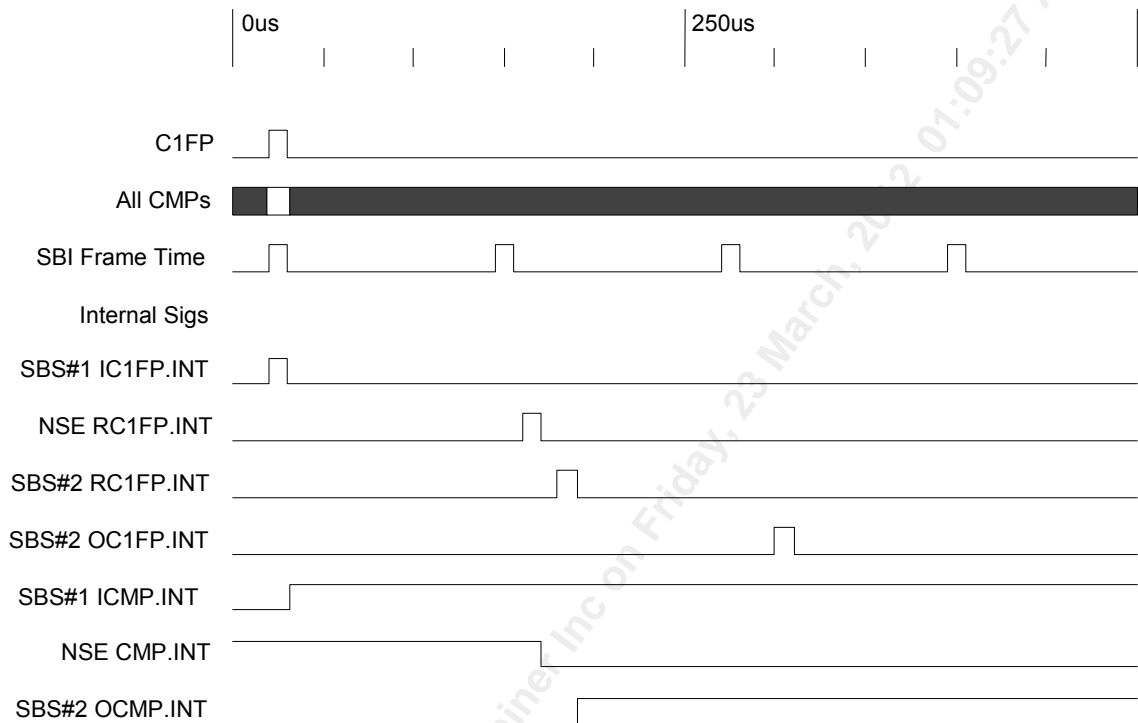
**Figure 17 Temux84/SBS/NSE/SBS/AALIGATOR32 System DS0 Switching with CAS**



**Figure 18 CAS Multi-frame Timing**



**Figure 19 Switch Timing DSOs with CAS**

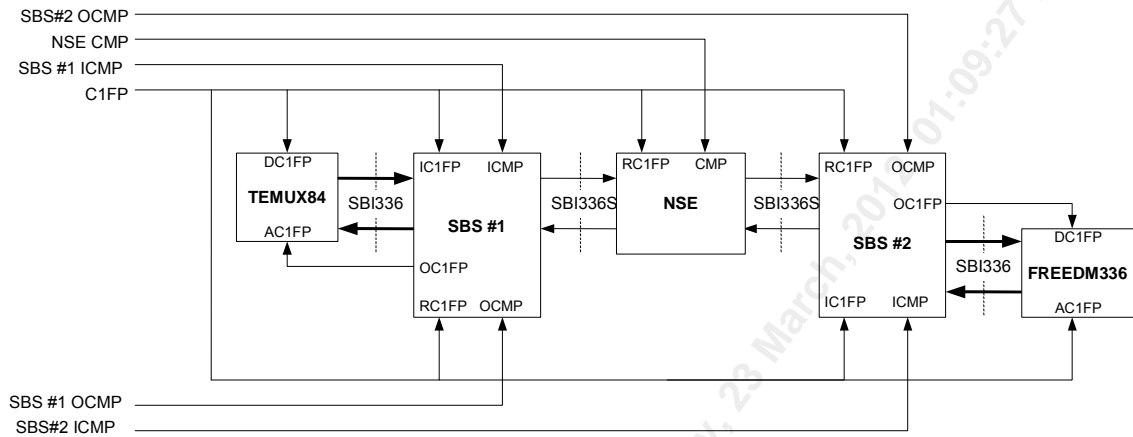


### 13.14.2 SBS/NSE Systems Switching DS0s Without CAS

This is very similar to the DS0 switching system configuration with CAS described in the previous section. The only difference is that in this system the global C1FP can be reduced to every SBI multi-frame rather than the longer 48 frame SBI bus signaling multi-frame. The advantage is that there is less latency when making switch configuration changes via the CMP signals.

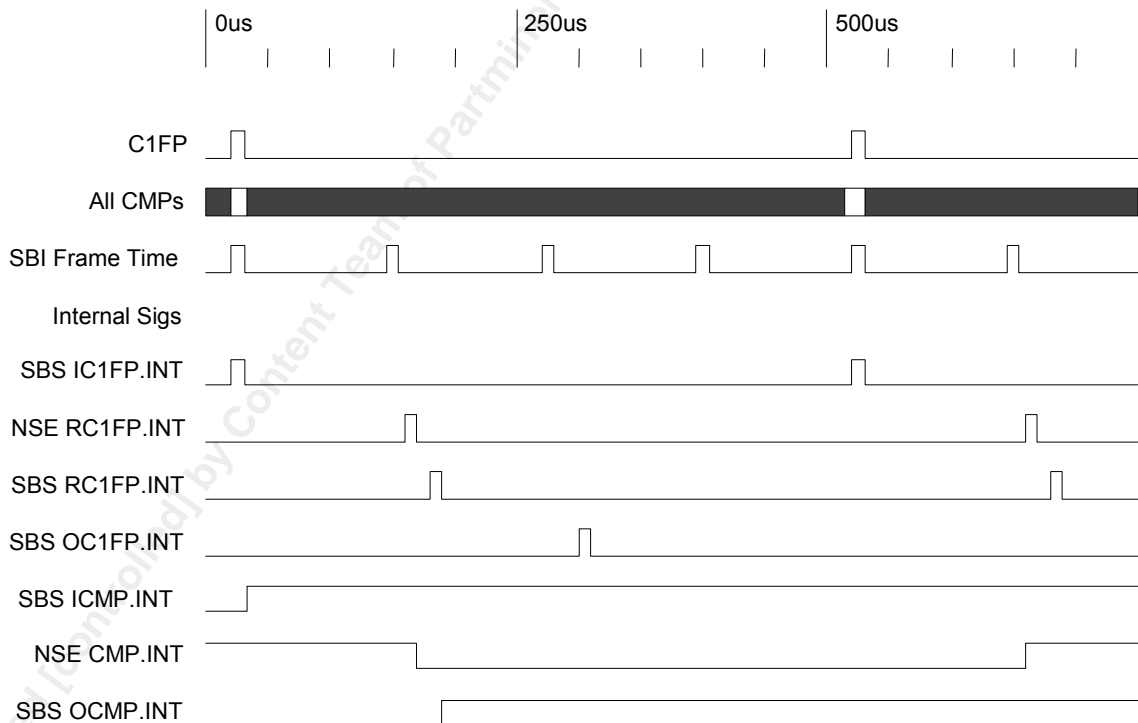
The following diagram shows the system with the FREEDM336 which does not require Channel Associated Signaling. Notice that the data latency through the system is the same as the case when switching DS0s with CAS.

**Figure 20 Temux84/SBS/NSE/SBS/FREEDM336 System DS0 Switching no CAS**



The following timing diagram shows the system timing when in this configuration.

**Figure 21 Switch Timing - DSOs Without CAS**



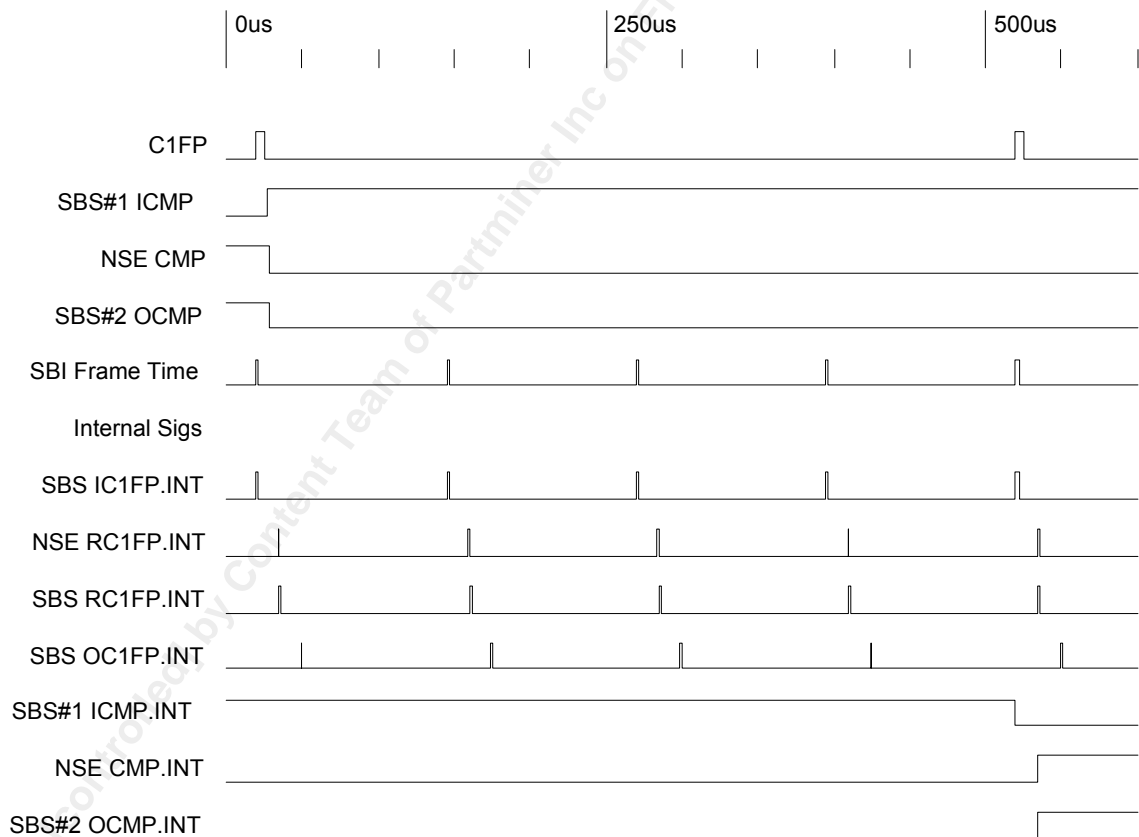
### 13.14.3 SBS/NSE Non-DS0 Level Switching With SBI336 Devices

The SBSLITE and NSE supports another mode of operation that has lower latency and lower power when not switching at the DS0 level. In this mode both of these devices become a column switch rather than a DS0 switch. This also saves SW configuration since only one row of the switch configuration rams has to be configured rather than all nine rows.

When switching DS0 through the system the SBSLITE must store an entire frame of DS0s before routing them to the destination to allow for the last DS0 of a frame to be switched to the first DS0 of the output. When doing column switching only one row of the SBI structure needs to be stored before switching can take place.

The same diagram from the previous section can be used here. The following timing diagram shows the system timing for this mode of operation.

**Figure 22 Non DS0 Switch Timing**



### 13.15 Device Latency

The following table is a list of the approximate latency of the SBSLITE in various operating modes. No blocks are bypassed (see register 004H)

Mode	Latency (SYSCLK cycles)
TX : DS0 switching mode, TX FIFO centered	9752
TX : Column switching mode, TX FIFO centered	1112
RX : DS0 switching mode, RC1DLY centre of range	9748
RX : Column switching mode, RC1DLY centre of range	1108

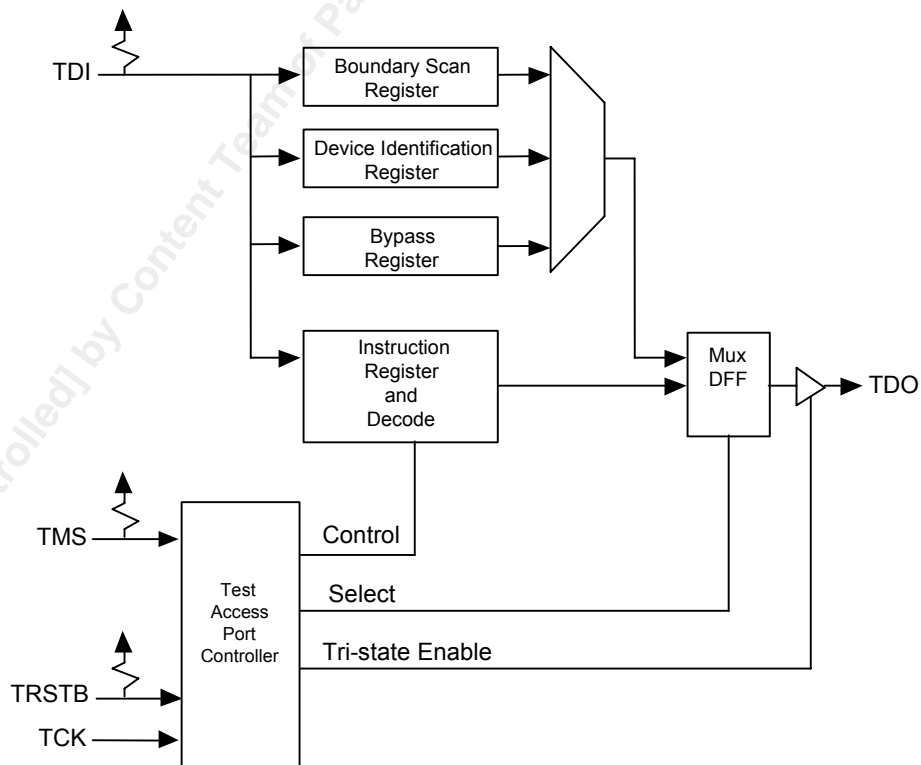
### 13.16 Switch Setting Algorithm.

Please see the Open Path Algorithm (OPA), Chip Set Driver (CSD) and the related CHES-Narrowband application notes for more information on the switch setting algorithms and software support.

### 13.17 JTAG Support

The SBSLITE supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins; TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

**Figure 23 Boundary Scan Architecture**



The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

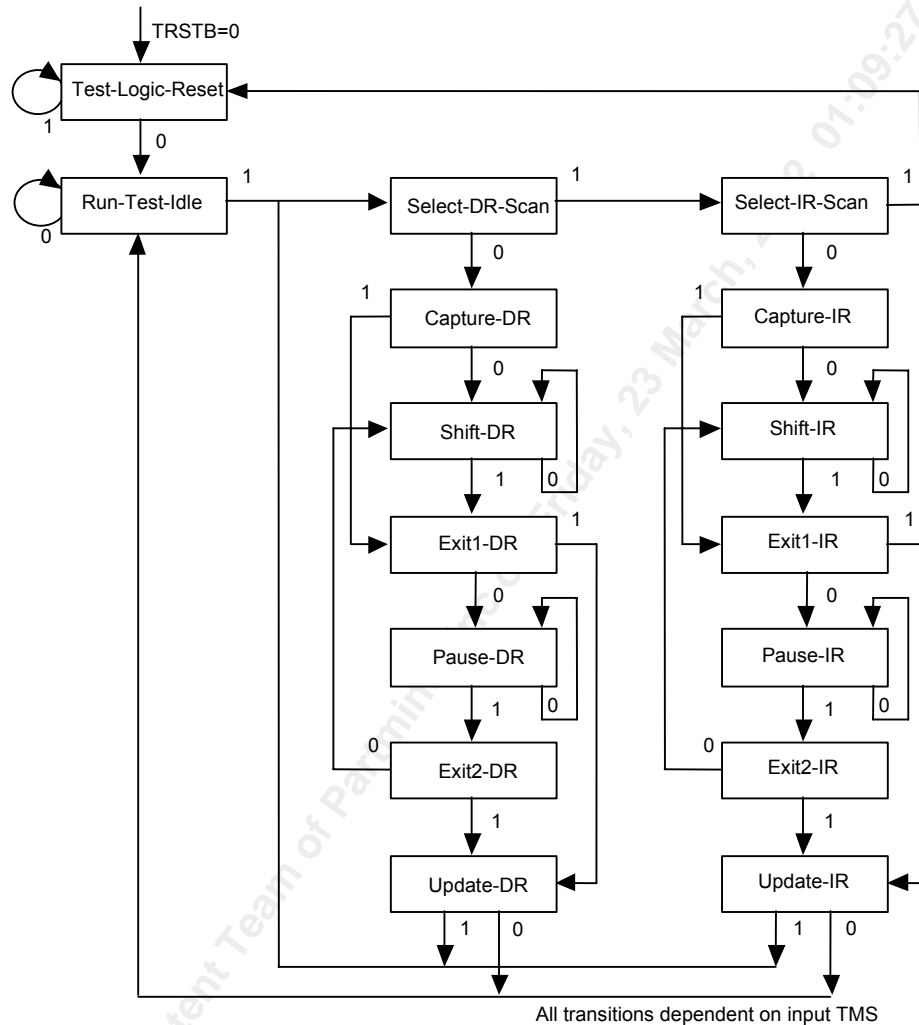
The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register placed in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

### 13.17.1 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.



Figure 24 TAP Controller Finite State Machine



### 13.17.2 States

#### Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

#### Run-Test-Idle

The run test/idle state is used to execute tests.

### **Capture-DR**

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

### **Shift-DR**

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

### **Update-DR**

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

### **Capture-IR**

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

### **Shift-IR**

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

### **Update-IR**

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

### **Boundary Scan Instructions**

The following is a description of the standard instructions. Each instruction selects a serial test data register path between input, TDI and output, TDO.

#### **13.17.3 Instructions**

##### **BYPASS**

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

## EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is placed between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

## SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

## IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

## STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

## 14 Functional Timing

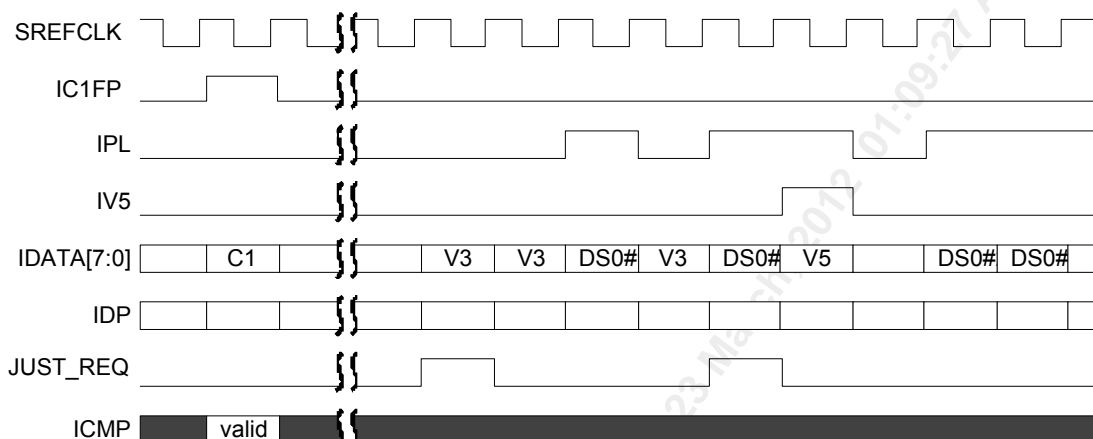
### 14.1 Incoming SBI336 Bus Functional Timing

Figure 25 shows the functional timing for the incoming 77.76MHz SBI336 bus configured for connection to a physical layer device. When configured for the SBI336 bus timing is provided by a 77.76MHz SREFCLK which is also connected to SYSCLK. When connecting to a physical layer device the justification request signal, JUST\_REQ, is used by the physical layer device to control link timing from a slave link layer device and is an input to the SBSLITE.

Figure 25 shows a number of capabilities of the SBI bus. IC1FP is a 2KHz pulse that indicates the SBI336 frame alignment from which all control signals and data are synchronized. The payload signal indicates valid tributary data as well as positive and negative tributary timing adjustments. In Figure 25 the first occurrence of IPL high shows a negative timing adjustment where valid data is carried in the V3 location. The last cycle with IPL low indicates a positive timing adjustment in the tributary octet after V3 where there is no valid data. The IV5 signal indicates that the current data octet is the V5 octet used for tributary framing alignment. The JUST\_REQ signal is only valid during the V3 octets and the tributary octets following the V3 octets. The first occurrence of JUST\_REQ high during the V3 octet indicates to the slave link layer device that it should speed next frame by performing a negative timing adjustment. The second occurrence of JUST\_REQ high during the tributary octet after the V3 octet indicates to the slave link layer device that it should slow down by performing a positive timing adjustment during the next frame. The last V3 in the diagram is meant to be the last V3 for all the tributaries.

The ICMP signal selects the active connection memory page in the memory switch. It is sampled at the C1 byte position in every multi-frame. ICMP is ignored at all other positions within the SBI frame. The connection memory page is switched on the next SBI bus multi-frame boundary after ICMP is sampled. The SBI multi-frame can be either 4 or 48 frames, depending on the value of MF\_48 in the SBSLITE Master Configuration Register.

**Figure 25 Incoming SBI336 Functional Timing**



When configured as connecting to a link layer device the JUST\_REQ signal is an output synchronized to OC1FP rather than IC1FP as shown in Figure 25. With the exception of the JUST\_REQ signal, the functional timing of the incoming SBI336 bus is the same when connecting to a Link Layer device as connecting to a physical layer device.

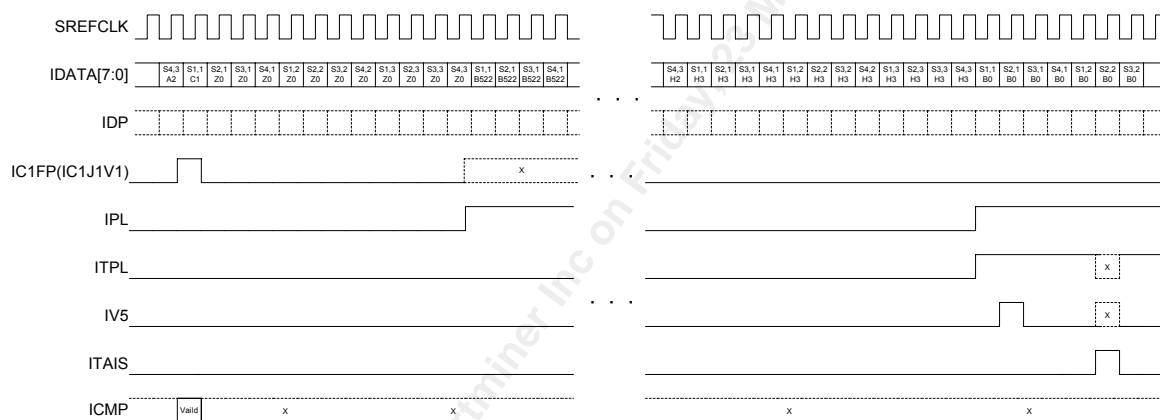
## 14.2 Incoming 77MHz TelecomBus Functional Timing

Figure 26 shows the timing of the Incoming TelecomBus stream when configured for 77.76MHz mode. Timing is provided by SREFCLK. SONET/SDH data is carried in the IDATA[7:0]. The bytes are arranged in order of transmission in an STS-12/STM-4 stream. Each transport/section overhead byte is labeled by Sx,y and type. Payload bytes are labeled by Sx,y and Bn, where 'n' is the active offset of the byte. Within Sx,y, the STS-3/STM-1 number is given by 'x' and the column number within the STS-3/STM-1 is given by 'y'. The IPL signal is set high to mark payload bytes and is set low at all other bytes. Similarly, ITPL is set high to mark tributary payload bytes and is set low at all other bytes. The composite transport frame and payload frame signal IC1J1V1 is equivalent to the IC1FP in SBI mode and is set high with IPL set low to mark the C1 byte of a transport frame. IC1J1V1/IC1FP is set high with IPL set high to mark the J1 bytes and V1 multi-frame of all the streams within IDATA[7:0]. For locked STS/AUs, the SBSLITE requires that all J1s follow immediately after the C1(Z0) or the H3 overhead bytes. The SBSLITE also requires that all H4 multi-frames be aligned forcing all V1 bytes to follow the J1 bytes. Multi-frame alignment is based on the first V1 indication by IC1J1V1 after the twelve J1 bytes. Tributary path frame boundaries are marked by a logic high on the IV5 signal. Tributaries in AIS alarm are indicated by the ITAIS signal.

The ICMP signal selects the active connection memory page in the memory switch. It is only valid at the C1 byte position and is ignored at all other positions within the transport frame. The connection memory page is switched on the next TelecomBus frame boundary after ICMP is sampled at the C1 byte.

In Figure 26 below, STS-3/STM-1 numbers 1, 2, and 4 are configured for STS-3/AU3 operation. STS-3/STM-1 number 3 is configured for STS-3c/AU4 operation. All streams are shown to have an active offset of 522 by the high level on IPL and IC1J1V1/IC1FP at byte S<sub>x,y</sub>/B522. No pointer justifications are shown. All streams are configured to carry virtual tributaries/tributary units. The payload frame boundary of one such tributary is located at byte S<sub>2,1</sub>/B0, as marked by a high level on IV5. At byte S<sub>2,2</sub>/B0, the tributary carried in stream S<sub>2,2</sub> (2 (STM-1 #2, AU3 #2)) is shown to be in tributary path AIS by the high level on ITAIS signal. The arrangement shown in Figure 26 is for illustrative purposes only; other configurations, alarm conditions, active offsets and justification events, etc. are possible.

**Figure 26 Incoming 77MHz TelecomBus Functional Timing**

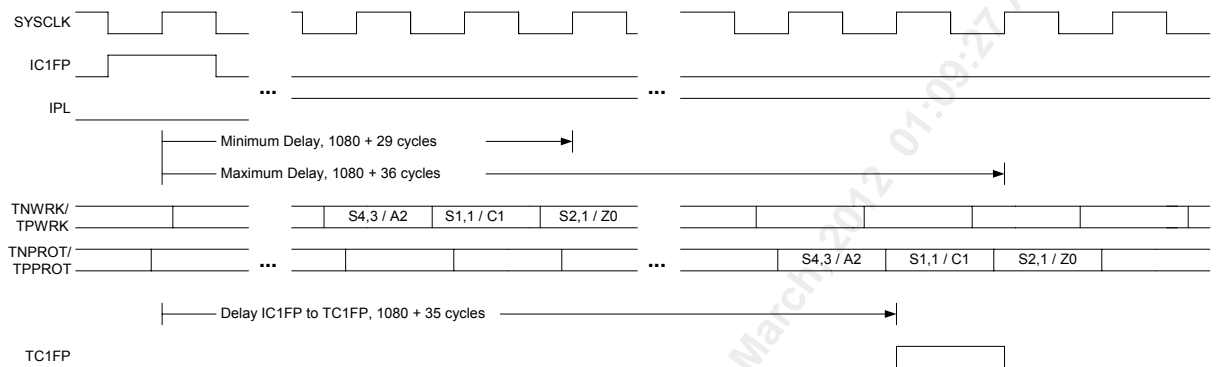


### 14.3 Transmit Serial LVDS Functional Timing

The delay through the SBSLITE is dependent on the operating mode. The timing from the Incoming Telecom or SBI bus to the LVDS link differs between TelecomBus mode and SBI mode. The timing when in SBI mode is also dependent on whether the SBSLITE is switching at the DS0 level and above or is switching only at the tributary level. When switching only tributaries in SBI mode we have the same delay through the SBSLITE as when switching tributaries in TelecomBus mode.

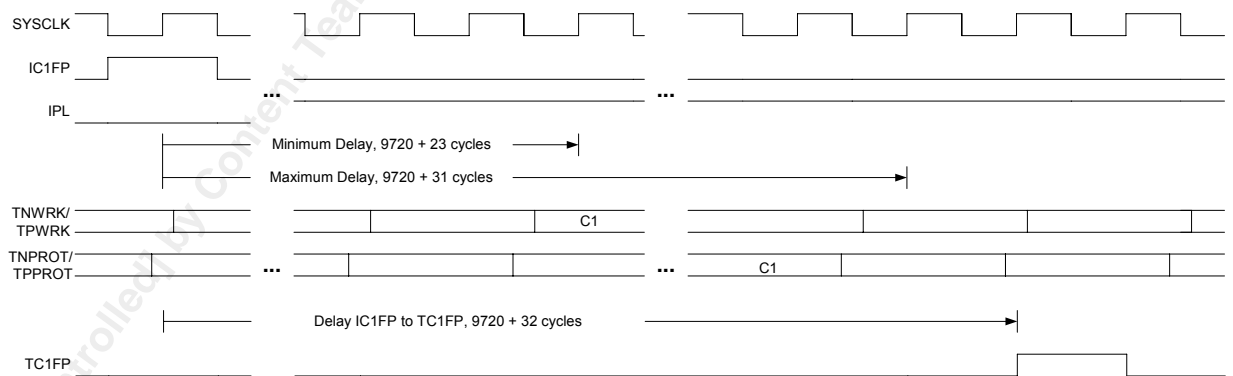
When switching tributaries in SBI mode or when in TelecomBus mode the SBSLITE is acting as a column switch. TelecomBus Due to the presence of FIFOs in the data path, the delay to the various links can differ by up to 7 SYSCLK cycles. The minimum delay (1109 SYSCLK cycles) is shown in Figure 27 to be incurred by the transmit working serial data link (TPWRK/TNWRK). This is equivalent to one row (1080 clock cycles) in a 77.76MHz TelecomBus structure or SBI336 bus structure plus 29 clock cycles through the data path. The maximum delay (1116 SYSCLK cycles) is shown to be incurred by the transmit protection serial data link (TPPROT/TNPROT). The TC1FP output is provided as a reference to indicate the approximate time the C1 characters are being output on the serial link. The relative phases in Figure 27 are shown for illustrative purposes only. Links may have different delays relative the each other than what is shown.

**Figure 27 Incoming TelecomBus to LVDS Functional Timing**



When switching DS0s in SBI mode the delay through the SBSLITE increases. Due to the presence of FIFOs in the data path, the delay to the various links can differ by up to 7 SYSCLK cycles. The minimum delay (9749 SYSCLK cycles) is shown in Figure 28 to be incurred by the transmit working serial data link (TPWRK/TNWRK). This is equivalent to one complete SBI336 frame (9720 clock cycles) plus 29 clock cycles through the data path. The maximum delay (9756 SYSCLK cycles) is shown to be incurred by the transmit protection serial data link (TPPROT/TNPROT). The TC1FP output is provided as a reference to indicate the approximate time the C1 characters are being output on the serial link. The relative phases in Figure 28 are shown for illustrative purposes only. Links may have different delays relative the each other than what is shown.

**Figure 28 Incoming SBI Bus to LVDS Timing with DS0 Switching**



Although Figure 27 and Figure 28 show IC1FP relative to SYSCLK, IC1FP is sampled by SREFCLK.

## 14.4 Receive Serial LVDS Functional Timing

Figure 29 below shows the relative timing of the receive LVDS links. TelecomBus Links carry SONET/SDH or SBI336 frame octets that are encoded in 8B/10B characters. Frame boundaries, tributary justification events and tributary alarm conditions are encoded in special control characters. The upstream devices sourcing the links share a common clock and have a common transport frame alignment that is synchronized by the Receive Serial Interface Frame Pulse signal (RC1FP). Due to phase noise of clock multiplication circuits and backplane routing discrepancies, the links will not be phase aligned to each other (within a tolerance level of 24 byte times) but are frequency locked. The delay from RC1FP being sampled high to the first and last C1 character is shown in Figure 29. In this example, the first C1 is delivered by the working link (RNWRK/ RPWRK). The delay to the last C1 represents the time when both links have delivered their C1 character. The minimum value for the internal programmable delay (RC1FPDLY[13:0]) is the delay to the last C1 character plus 15. The maximum value is the delay to the first C1 character plus 31. Consequently, the external system must ensure that the relative delays between all the receive LVDS links be less than 16 bytes. The relative phases of the links in Figure 29 are shown for illustrative purposes only.

**Figure 29 Receive LVDS Link Timing**

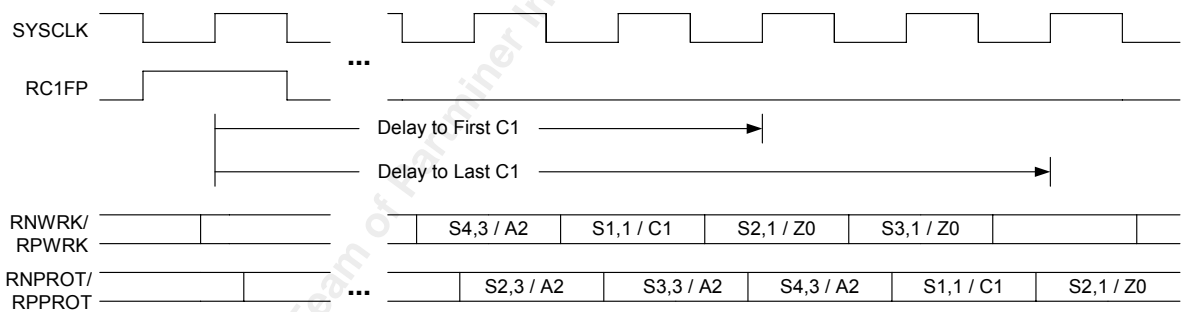
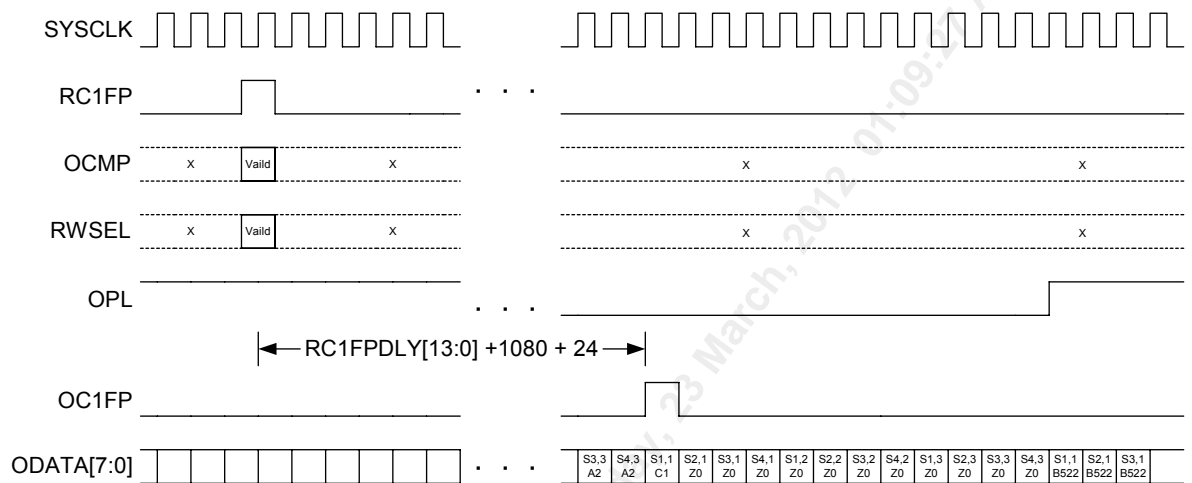


Figure 30 shows the timing relationships around the RC1FP signal. The Outgoing Memory Page selection signal (OCMP) and the Receive Working Serial Data Select signal (RWSEL) are only valid at the SYSCLK cycle at the C1 location as indicated by RC1FP. They are ignored at all other locations within the transport frame. In column switching mode, the delay from RC1FP to the C1 byte on the outgoing Telecom or SBI336 bus stream is the sum of the value programmed into the RC1FPDLY[13:0] register, the OMSU switching latency of 1080 SYSCLK cycles and the processing delay of 24 SYSCLK cycles. In DS0 switching mode, the delay from RC1FP to the C1 byte on the outgoing SBI336 bus stream is the sum of the value programmed into the RC1FPDLY[13:0] register, the OMSU switching latency of 9720 SYSCLK cycles and the processing delay of 24 SYSCLK cycles.



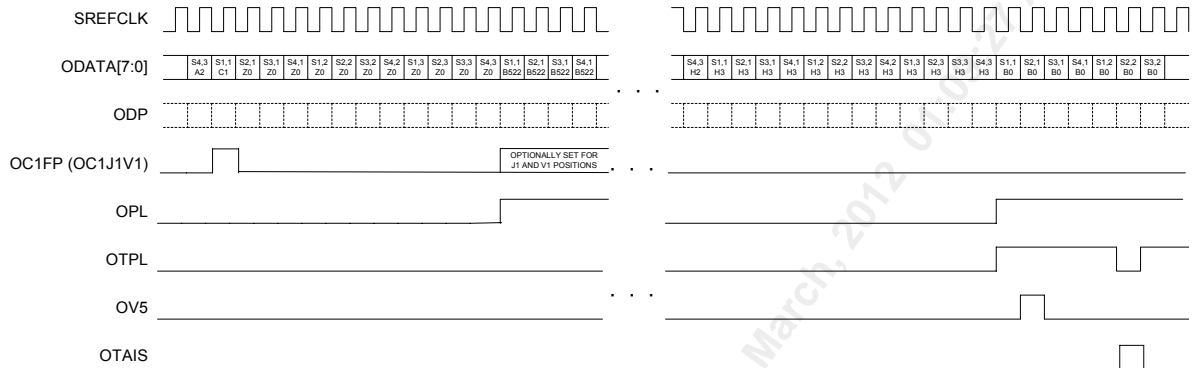
**Figure 30 Outgoing Synchronization Timing**



## 14.5 Outgoing 77.76MHz TelecomBus Functional Timing

Figure 31 shows the timing of the Outgoing TelecomBus stream. Timing is provided by SREFCLK. SONET/SDH data is carried on the ODATA[7:0] signals. The bytes are arranged in order of transmission in an STS-12/STM-4 stream. Each transport/section overhead byte is labeled by S<sub>x,y</sub> and type. Payload bytes are labeled by S<sub>x,y</sub> and B<sub>n</sub>, where 'n' is the active offset of the byte. Within S<sub>x,y</sub>, the STS-3/STM-1 number is given by 'x' and the column number within the STS-3/STM-1 is given by 'y'. The OPL signal is set high to mark payload bytes and is set low at all other bytes. Similarly, OTPL is set high to mark tributary payload bytes and is set low at all other bytes. The composite transport frame and payload frame signal, OC1FP (OC1J1V1), is set high with OPL set low to mark the C1 byte of a transport frame. OC1J1V1 is optionally set high with OPL also set high to mark the J1 byte and the byte following J1 of all the streams within ODATA[7:0]. Tributary path frame boundaries are marked by a logic high on the OV5 signal. Tributaries in AIS alarm are indicated by the OTAIS signal.

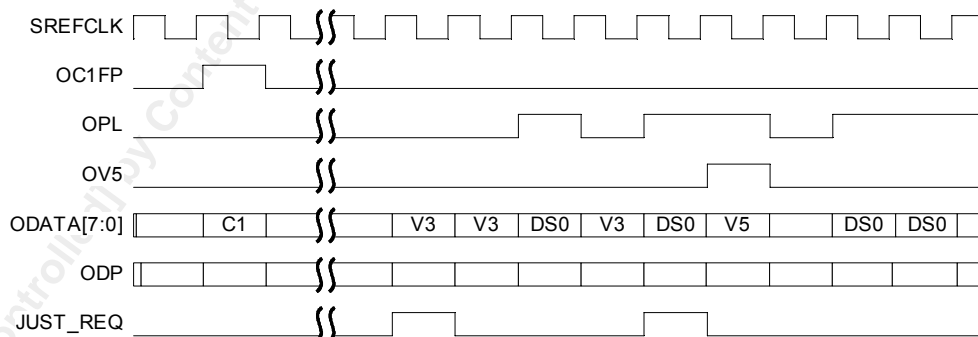
**Figure 31** Outgoing 77.76MHz TelecomBus Functional Timing



### 14.6 Outgoing SBI336 Functional Timing

Figure 32 shows the functional timing for the outgoing 77.76MHz SBI336 bus configured for connection to a link layer device. When configured for the SBI336 bus, timing is provided by a 77.76MHz SREFCLK which is also connected to SYSCLK. When connecting to a link layer device the justification request signal, JUST\_REQ, is output from the SBSLITE and is used to control the link timing. If the SBSLITE is connected to a physical layer device the JUST\_REQ signal is an input synchronized to IC1FP rather than OC1FP. With the exception of the JUST\_REQ signal, the functional timing of the outgoing SBI336 bus is the same when connecting to a physical layer device as connecting to a link layer device.

**Figure 32** Outgoing SBI336 Functional Timing



## 15 Absolute Maximum Ratings

Maximum ratings are the worst-case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions. Note: if a voltage is applied to an input pin when the device is powered down, the current needs to be limited below 20mA and the maximum voltage rating does not apply.

**Table 28 Absolute Maximum Ratings**

<b>Storage Temperature</b>	-40°C to +125°C
<b>Supply Voltage (DVDDO, AVDH, CSU_AVDH)</b>	-0.3V to +4.6V
<b>Supply Voltage (DVDDI, AVDL, CSU_AVDL)</b>	-0.3V to +2.5V
<b>Input Pad Tolerance</b>	-2V < VDDO < +2V for 10ns, 100mA max
<b>Output Pad Overshoot Limits</b>	-2V < VDDO < +2V for 10ns, 20mA max
<b>Voltage on Any Digital Pin</b>	-0.5V to DVDDO+0.5V
<b>Voltage on LVDS Pin</b>	-0.5V to AVDH+0.5V
<b>Static Discharge Voltage</b>	±1000 V
<b>Latch-Up Current</b>	±100 mA except RESK, TPWRK, TNWRK, TPPROT, TNPROT, RPWRK, RNWRK, RPPROT and RNPROT
<b>Latch-Up Current on TPWRK, TNWRK, TPPROT, TNPROT, RPWRK, RNWRK, RPPROT and RNPROT</b>	±90 mA
<b>Latch-Up Current on RESK pin</b>	±50 mA
<b>DC Input Current</b>	±20 mA
<b>Lead Temperature</b>	+230°C
<b>Absolute Maximum Junction Temperature</b>	+150°C

## 16 Power Information

### 16.1 Power Requirements

Conditions	Parameter	Typ <sup>1,3</sup>	High <sup>4</sup>	Max <sup>2</sup>	Units
<b>PM8611 (SBSLITE)</b> 77.76MHz Incoming Outgoing interface with Serial LVDS Tx/Rx interface	IDDOP (VDDI)	0.253	—	0.282	A
	IDDOP (VDDO)	0.055	—	0.090	A
	IDDOP (AVDL)	0.110	—	0.153	A
	IDDOP (AVDH)	0.034	—	0.040	A
	Total Power	0.9471	1.1214	—	W

**Notes:**

1. Typical IDD values are calculated as the mean value of current under the following conditions: typically processed silicon, nominal supply voltage, T<sub>J</sub>=60 °C, outputs loaded with 30 pF (if not otherwise specified), and a normal amount of traffic or signal activity. These values are suitable for evaluating typical device performance in a system
2. Max IDD values are currents guaranteed by the production test program and/or characterization over process for operating currents at the maximum operating voltage and operating temperature that yields the highest current (including outputs loaded to 30 pF, unless otherwise specified)
3. Typical power values are calculated using the formula:

$$\text{Power} = \sum_i (\text{VDDNomi} \times \text{IDDTypi})$$

Where i denotes all the various power supplies on the device, VDDNomi is the nominal voltage for supply i, and IDDTypi is the typical current for supply i (as defined in note 1 above). These values are suitable for evaluating typical device performance in a system

4. High power values are a “normal high power” estimate and are calculated using the formula:

$$\text{Power} = \sum_i (\text{VDDMaxi} \times \text{IDDHighi})$$

Where i denotes all the various power supplies on the device, VDDMaxi is the maximum operating voltage for supply i, and IDDHighi is the current for supply i. IDDHigh values are calculated as the mean value plus two sigmas (2σ) of measured current under the following conditions: T<sub>J</sub>=105° C, outputs loaded with 30 pF (if not otherwise specified). These values are suitable for evaluating board and device thermal characteristics

### 16.2 Power Sequencing

Due to ESD protection structures in the SBSLITE pads it is necessary to exercise caution when powering the IC up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions, incorrect power sequencing may damage these ESD protection devices or trigger latch up.

The recommended power supply sequencing is as follows:

1. The 1.8 V supplies can be brought up at the same time or after the 3.3 V supplies as long as the 1.8V supplies never exceed the 3.3V supplies by more than 0.3V.
2. Analog supplies must not exceed digital supplies of the same nominal voltage by more than 0.3V.

3. Data applied to I/O pins must not exceed VDDO by more than 0.3V unless the data is current-limited to 20 mA \*.
4. There are no power-up ramp rate restrictions.
5. The SBSLITE must be powered down according to the same restrictions above.

\* These rules are intended to allow for hot-swap of LVDS signals, as the differential links are appropriately current-limited.

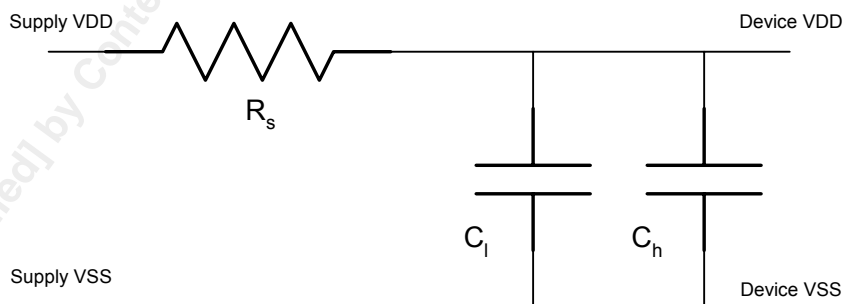
### 16.3 Analog Power Filtering Recommendations

To achieve best performance of the LVDS links, an analog filter network should be installed between the power balls and the supply.

**Table 29 Analog Power Filters**

	$R_s$	$C_l$	$C_h$	Notes
CSU_AVDH (1 ball)	3.3-ohm	100nF	10nF	One Filter network per VDD ball.
CSU_AVDL (3 balls)	0.47-ohm	4.7uF	10nF	One Filter network per VDD ball.
AVDH[1] (1 ball)	3.3-ohm	1.0uF	10nF	One Filter network per VDD ball.
AVDH[2] AVDH[0] (2 balls)	0-ohm	100nF	10nF	One Filter network per VDD ball.
AVDL (1 ball)	0-ohm	100nF	10nF	One Filter network per VDD ball.

**Figure 33 Analog Power Filter Circuit**



## 17 D. C. Characteristics

$T_A = -40^{\circ}\text{C}$  to  $T_J = +125^{\circ}\text{C}$ ,  $V_{DDO} = 3.3\text{V} \pm 5\%$ ,  $V_{DDI} = 1.8\text{V} \pm 5\%$   
(Typical Conditions:  $T_C = 25^{\circ}\text{C}$ ,  $V_{DDO} = 3.3\text{V}$ ,  $V_{DDI} = 1.8\text{V}$ )

**Table 30 D.C Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VDVDDO	Power Supply	3.14	3.3	3.47	Volts	
VDVDDI	Power Supply	1.71	1.8	1.89	Volts	
VAVDH	Power Supply	3.14	3.3	3.47	Volts	
VCSU_AVDH	Power Supply	3.14	3.3	3.47	Volts	
VAVDH	Power Supply	1.71	1.8	1.89	Volts	
VCSU_AVDH	Power Supply	1.71	1.8	1.89	Volts	
VIL	Input Low Voltage	0		0.8	Volts	Guaranteed Input Low voltage.
VIL_TCK	Input Low Voltage	0		0.75	Volts	Guaranteed Input Low voltage – TCK only.
VIH	Input High Voltage	2.0		$V_{DDO} + 0.5$	Volts	Guaranteed Input High voltage.
VOL	Output or Bi-directional Low Voltage		0.1	0.4	Volts	Guaranteed output Low voltage at $V_{DVDDO} = 3.14\text{V}$ and $I_{OL} =$ maximum rated for pad.
VOH	Output or Bi-directional High Voltage	2.4	2.7		Volts	Guaranteed output High voltage at $V_{DVDDO} = 3.14\text{V}$ and $I_{OH} =$ maximum rated for pad.
VT+	Reset Input High Voltage	2.2		$V_{DDO} + 0.5$	Volts	Applies to RSTB and TRSTB only.
VT-	Reset Input Low Voltage	-0.5		0.8	Volts	Applies to RSTB and TRSTB only.
VTH	Reset Input Hysteresis Voltage		0.5		Volts	Applies to RSTB and TRSTB only.
IILPU	Input Low Current	-200	-50	-4	$\mu\text{A}$	$V_{IL} = \text{GND}$ . Notes 1 and 3.
IHPU	Input High Current	-10	0	+10	$\mu\text{A}$	$V_{IH} = V_{DVDDO}$ . Notes 1 and 3.
IIL	Input Low Current	-10	0	+10	$\mu\text{A}$	$V_{IL} = \text{GND}$ . Notes 2 and 3.
IH	Input High Current	-10	0	+10	$\mu\text{A}$	$V_{IH} = V_{DVDDO}$ . Notes 2 and 3.
VICM	LVDS Input Common-Mode Range	0		2.4	V	

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VIDM	LVDS Input Differential Sensitivity			100	mV	
RIN	LVDS Differential Input Impedance	85	100	115	$\Omega$	
VLOH	LVDS Output voltage high		1375	1475	mV	R <sub>LOAD</sub> =100 $\Omega$ $\pm$ 1%
VLOL	LVDS Output voltage low	925	1025		mV	R <sub>LOAD</sub> =100 $\Omega$ $\pm$ 1%
VODM	LVDS Output Differential Voltage	300	350	400	mV	R <sub>LOAD</sub> =100 $\Omega$ $\pm$ 1%
VOCM	LVDS Output Common-Mode Voltage	1125	1200	1275	mV	R <sub>LOAD</sub> =100 $\Omega$ $\pm$ 1%
RO	LVDS Output Impedance, Differential	85	110	115	$\Omega$	
\DeltaVODM	Change in  VODM  between "0" and "1"			25	mV	R <sub>LOAD</sub> =100 $\Omega$ $\pm$ 1%
\DeltaVOCM	Change in V <sub>OCM</sub> between "0" and "1"			25	mV	R <sub>LOAD</sub> =100 $\Omega$ $\pm$ 1%
I <sub>SP</sub> , I <sub>SN</sub>	LVDS Short-Circuit Output Current			10	mA	Drivers shorted to ground
I <sub>SPN</sub>	LVDS Short-Circuit Output Current			10	mA	Drivers shorted together
C <sub>IN</sub>	Input Capacitance		5		pF	t <sub>A</sub> =25°C, f = 1 MHz
C <sub>OUT</sub>	Output Capacitance		5		pF	t <sub>A</sub> =25°C, f = 1 MHz
C <sub>IO</sub>	Bi-directional Capacitance		5		pF	t <sub>A</sub> =25°C, f = 1 MHz

**Notes on D.C. Characteristics:**

1. Input pin or bi-directional pin with internal pull-up resistor.
2. Input pin or bi-directional pin without internal pull-up resistor
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).

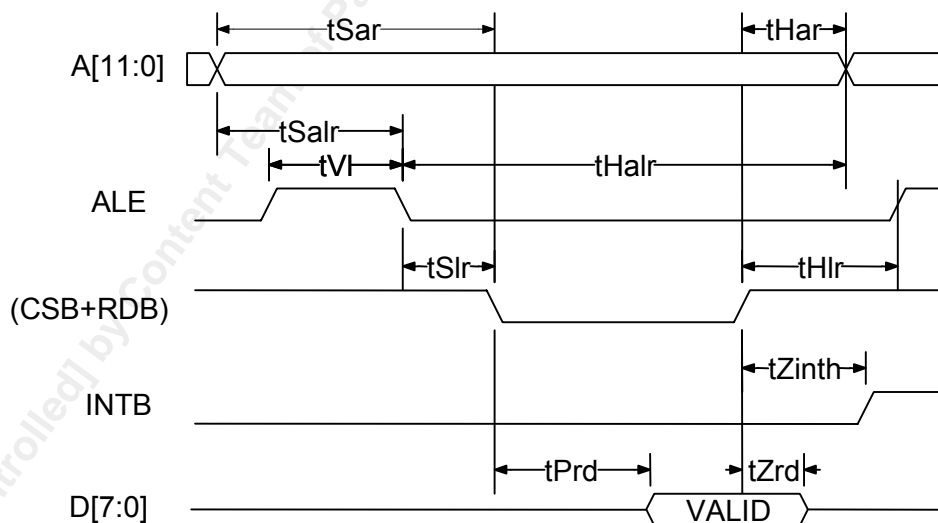
## 18 Microprocessor Interface Timing Characteristics

( $T_A = -40^{\circ}\text{C}$  to  $T_J = +125^{\circ}\text{C}$ ,  $V_{DDO} = 3.3\text{V} \pm 5\%$ ,  $V_{DDI} = 1.8\text{V} \pm 5\%$ )

**Table 31 Microprocessor Interface Read Access (Figure 34)**

Symbol	Parameter	Min	Max	Units
tSAR	Address to Valid Read Set-up Time	5		ns
tHAR	Address to Valid Read Hold Time	5		ns
tSALR	Address to Latch Set-up Time	5		ns
tHALR	Address to Latch Hold Time	5		ns
tVL	Valid Latch Pulse Width	2		ns
tSLR	Latch to Read Set-up	0		ns
tHLR	Latch to Read Hold	5		ns
tPRD	Valid Read to Valid Data Propagation Delay		15	ns
tZRD	Valid Read Negated to Output Tri-state		15	ns
tZINTH	Valid Read Negated to INTB High		20	ns

**Figure 34 Microprocessor Interface Read Timing**



**Notes on Microprocessor Interface Read Timing:**

- Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
- Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[15:0]).



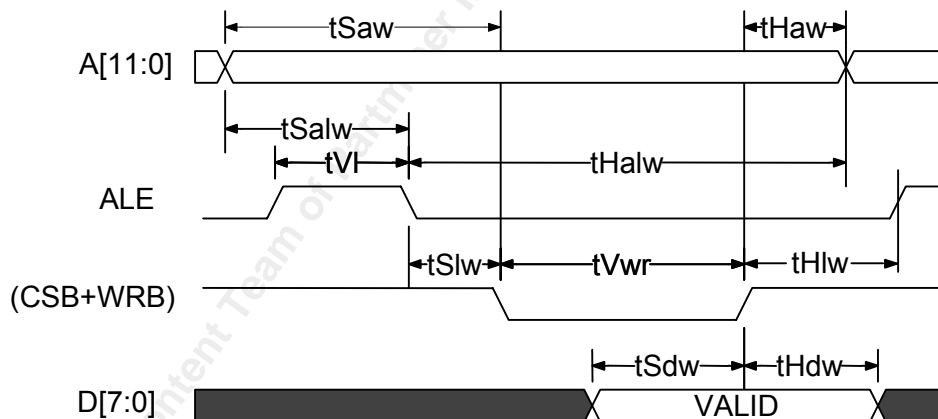
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. In non-multiplexed address/data bus architectures, ALE should be held high so parameters  $t_{SALR}$ ,  $t_{HALR}$ ,  $t_{VL}$ ,  $t_{SLR}$ , and  $t_{HLR}$  are not applicable.
5. Parameter  $t_{HAR}$  is not applicable if address latching is used.
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

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**Table 32 Microprocessor Interface Write Access (Figure 35)**

Symbol	Parameter	Min	Max	Units
tSAW	Address to Valid Write Set-up Time	5		ns
tSDW	Data to Valid Write Set-up Time	10		ns
tSALW	Address to Latch Set-up Time	5		ns
tHALW	Address to Latch Hold Time	5		ns
tVL	Valid Latch Pulse Width	2		ns
tSLW	Latch to Write Set-up	0		ns
tHLW	Latch to Write Hold	5		ns
tHDW	Data to Valid Write Hold Time	5		ns
tHAW	Address to Valid Write Hold Time	5		ns
tVWR	Valid Write Pulse Width	15		ns

**Figure 35 Microprocessor Interface Write Timing**



**Notes on Microprocessor Interface Write Timing:**

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.
2. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tSALW, tHALW, tVL, tSLW, and tHLW are not applicable.
3. Parameter tHAW is not applicable if address latching is used.
4. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
5. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

## 19 A.C. Timing Characteristics

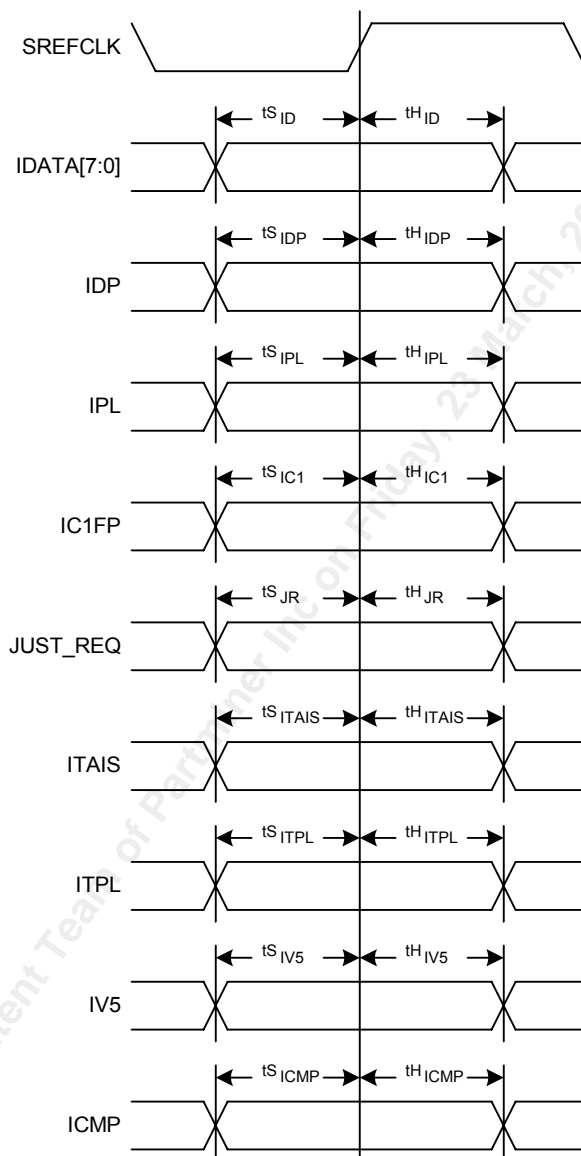
( $T_A = -40^{\circ}\text{C}$  to  $T_J = +125^{\circ}\text{C}$ ,  $V_{DDO} = 3.3\text{V} \pm 5\%$ ,  $V_{DDI} = 1.8\text{V} \pm 5\%$ )

### 19.1 SBSLITE Incoming Bus Timing

Table 33 SBSLITE Incoming Timing (Figure 36)

Symbol	Description	Min	Max	Units
	SREFCLK Frequency (nominally 77.76MHz )	-50	+50	ppm
	SREFCLK Duty Cycle	40	60	%
tSID	IDATA[7:0] Set-up Time	3		ns
tHID	IDATA[7:0] Hold Time	0		ns
tSIDP	IDP Set-up Time	3		ns
tHIDP	IDP Hold Time	0		ns
tS PL	IPL Set-Up Time	3		ns
tH PL	IPL Hold Time	0		ns
tS C1	IC1FP Set-Up Time	3		ns
tH C1	IC1FP Hold Time	0		ns
tSJR	JUST_REQ Set-Up Time	3		ns
tHJR	JUST_REQ Hold Time	0		ns
tS TAIS	ITAIS Set-Up Time	3		ns
tH TAIS	ITAIS Hold Time	0		ns
tS TPL	ITPL Set-Up Time	3		ns
tH TPL	ITPL Hold Time	0		ns
tS V5	IV5 Set-Up Time	3		ns
tH V5	IV5 Hold Time	0		ns
tS CMP	ICMP Set-Up Time	3		ns
tH CMP	ICMP Hold Time	0		ns

Figure 36 SBSLITE Incoming Timing



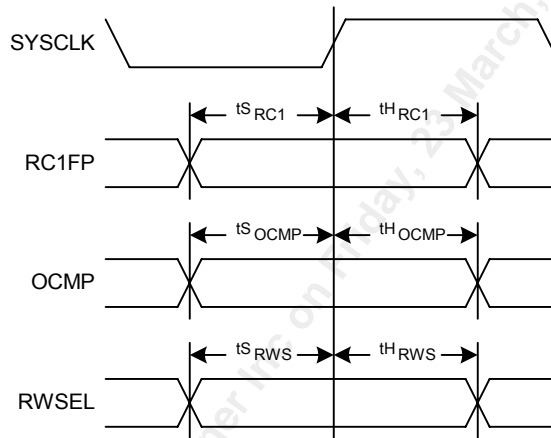
## 19.2 SBSLITE Receive Bus Timing

Table 34 SBSLITE Receive Timing (Figure 37)

Symbol	Description	Min	Max	Units
	SYCLK Frequency (nominally 77.76 MHz )	-50	+50	ppm
	SYCLK Duty Cycle	40	60	%
tSRC1	RC1FP Set-Up Time	3		ns
tHRC1	RC1FP Hold Time	0		ns

Symbol	Description	Min	Max	Units
tSOCMP	OCMP Set-Up Time	3		ns
tHOCMP	OCMP Hold Time	0		ns
tSRWS	RWSEL Set-Up Time	3		ns
tHRWS	RWSEL Hold Time	0		ns

**Figure 37 SBSLITE Receive Timing**



**Notes on Input Timing:**

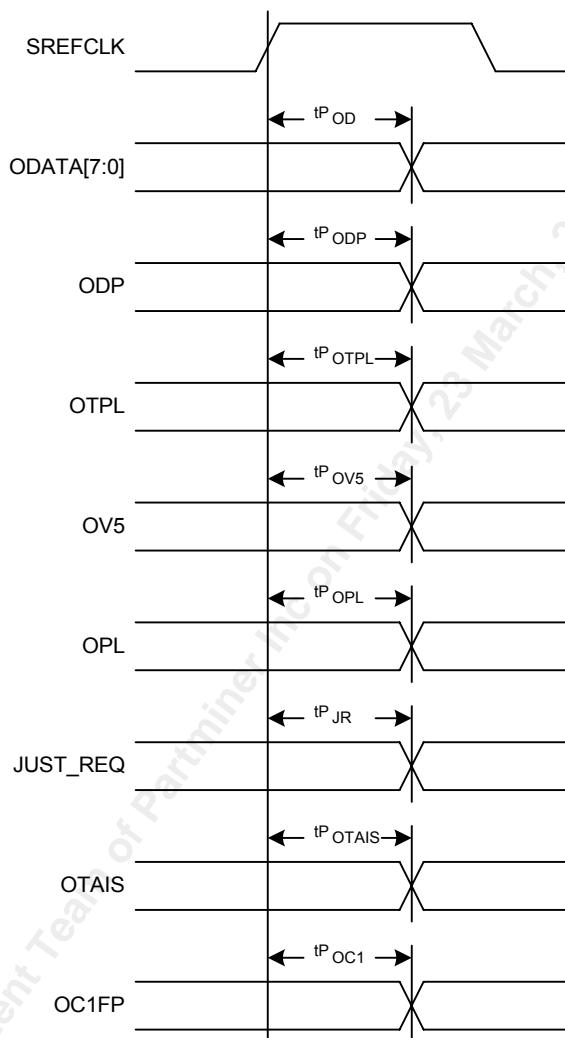
1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

### 19.3 SBSLITE Outgoing Bus Timing

**Table 35 SBSLITE Outgoing Timing (Figure 38)**

Symbol	Description	Min	Max	Units
tPOD	SREFCLK High to ODATA[7:0] Valid	1	7	ns
tPODP	SREFCLK High to ODP Valid	1	7	ns
tPOTPL	SREFCLK High to OTPL Valid	1	7	ns
tPOV5	SREFCLK High to OV5 Valid	1	7	ns
tPOPL	SREFCLK High to OPL Valid	1	7	ns
tPJR	SREFCLK High to JUST_REQ Valid	1	7	ns
tPOTAIS	SREFCLK High to OTAIS Valid	1	7	ns
tPOC1	SREFCLK High to OC1FP Valid	1	7	ns

Figure 38 SBSLITE Outgoing Timing

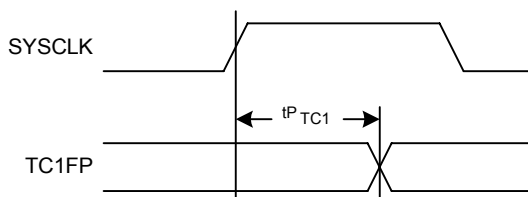


## 19.4 SBSLITE Transmit Bus Timing

Table 36 SBSLITE Transmit Timing (Figure 39)

Symbol	Description	Min	Max	Units
t <sup>P</sup> TC1	SYSCLK High to TC1FP Valid	1	7	ns

**Figure 39 SBSLITE Transmit Timing**



**Notes on Output Timing:**

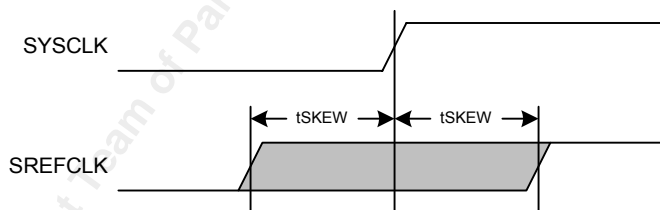
1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Output propagation delays are measured with a 50 pF load on the outputs operating at 77.76MHz except where indicated.

## 19.5 SYSCLK / REFCLK Skew Requirement

**Table 37 SYSCLK / REFCLK Skew Requirement (Figure 40)**

Symbol	Description	Min	Max	Units
tSKEW	SREFCLK to SYSCLK Skew	-1	1	ns

**Figure 40 SYSCLK / REFCLK Skew Requirement**



## 19.6 Serial Interface

**Table 38 Serial Interface Timing**

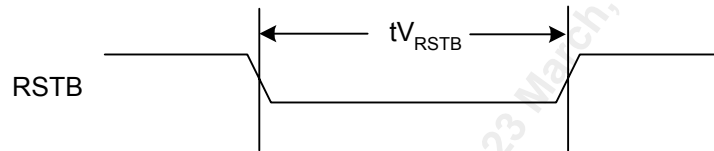
Symbol	Description	Min	Typical	Max	Units
fRLVDS	RPWRK, RNWRK, RPPROT, RNPROT Bit Rate	10f <sub>SYSCLK</sub>	10f <sub>SYSCLK</sub>	10f <sub>SYSCLK</sub>	Mbps
tFALL	VODM fall time, 80%-20%, (RLOAD=100Ω ±1%)	200	300	400	ps
tRISE	VODM rise time, 20%-80%, (RLOAD=100Ω ±1%)	200	300	400	ps
tSKEW	Differential Skew			50	ps

## 19.7 RSTB Timing

Table 39 RSTB Timing (Figure 41)

Symbol	Description	Min	Max	Units
tVRSTB	RSTB Pulse Width	100		ns

Figure 41 RSTB Timing



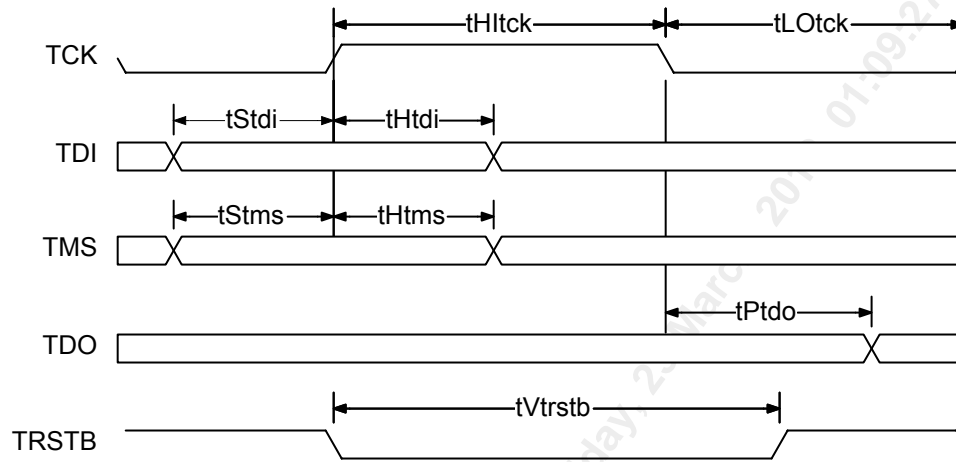
## 19.8 JTAG Port Interface

Table 40 JTAG Port Interface (Figure 42)

Symbol	Description	Min	Max	Units
FTCK	TCK Frequency		4	MHz
THITCK	TCK HI Pulse Width	100		ns
THITCK	TCK LO Pulse Width	100		ns
TSTMS	TMS Set-up time to TCK	25		ns
THTMS	TMS Hold time to TCK	25		ns
TSTDI	TDI Set-up time to TCK	25		ns
HTDI	TDI Hold time to TCK	25		ns
TPTDO	TCK Low to TDO Valid	2	35	ns
TVTRSTB	TRSTB Pulse Width	100		ns



Figure 42 JTAG Port Interface Timing



## 20 Ordering Information

Table 41 Ordering Information

Part No.	Description
PM8611-PI	160-Pin Plastic Ball Grid Array (PBGA) 15mm x 15mm: 1.0mm BP
PM8611-PGI	160-Pin PBGA, 15x15 mm, 1.00 mm BP (RoHS-compliant)

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## 21 Thermal Information

The SBSLITE is designed to operate over a wide temperature range and is suited for outside plant equipment<sup>1</sup>.

**Table 42 Outside Plant Thermal Information**

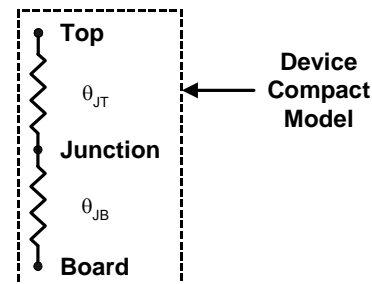
Maximum long-term operating junction temperature ( $T_J$ ) to ensure adequate long-term life	105 °C
Maximum junction temperature ( $T_J$ ) for short-term excursions with guaranteed continued functional performance <sup>2</sup> . This condition will typically be reached when local ambient reaches 85 °C.	125 °C
Minimum ambient temperature ( $T_A$ )	-40 °C

**Table 43 Thermal Resistance vs. Air Flow<sup>3</sup>**

Airflow	Natural Convection	1 m/s	2 m/s
$\theta_{JA}$ (°C/W)	29.3	23.2	20.7

**Table 44 Device Compact Model<sup>4</sup>**

Junction-to-Top Thermal Resistance, $\theta_{JT}$	5.15 °C/W
Junction-to-Board Thermal Resistance, $\theta_{JB}$	16 °C/W



Power depends upon the operating mode. To obtain power information, refer 'High' power values in section 16 Power Requirements.

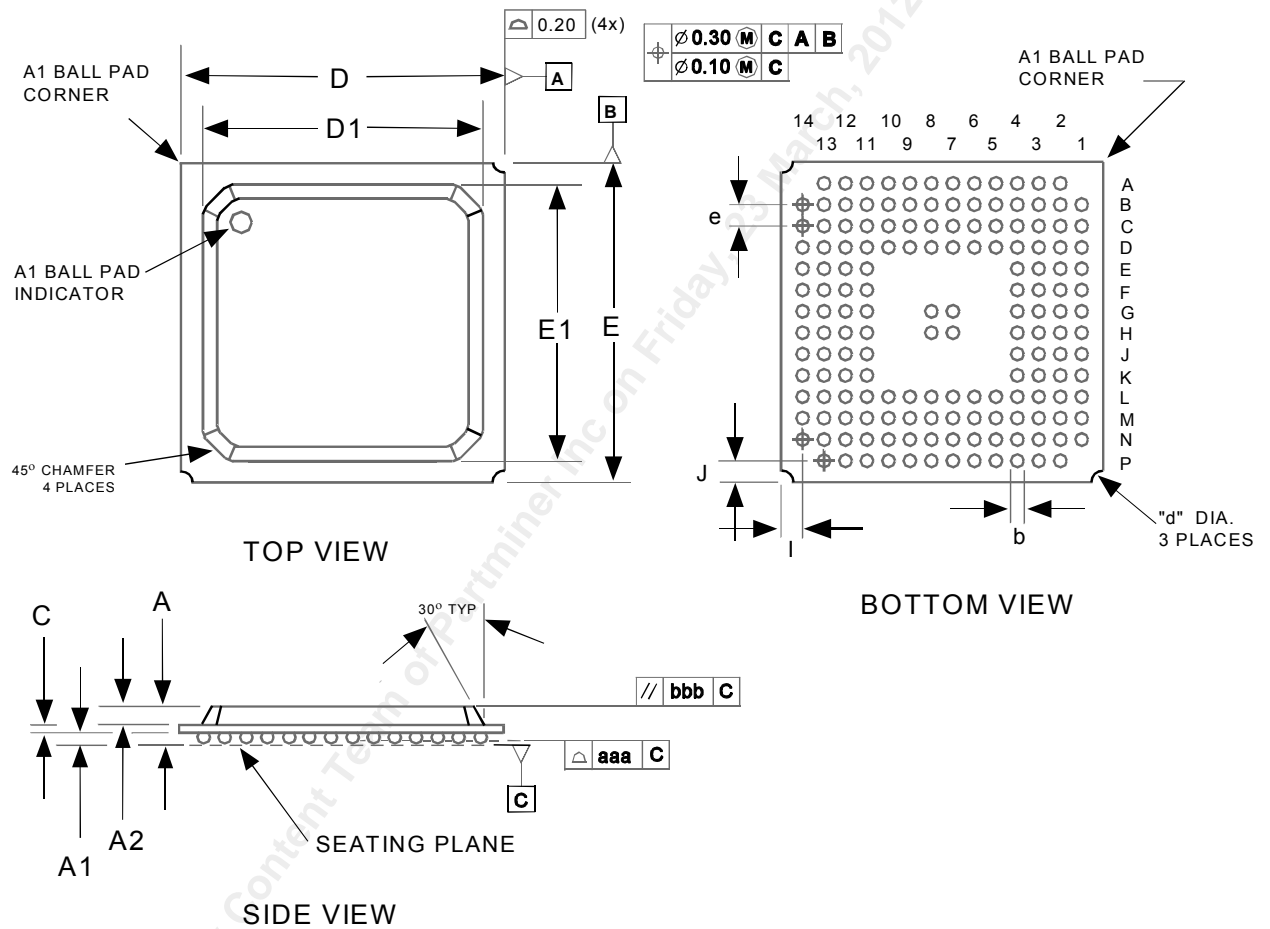
### Notes

1. The minimum ambient temperature requirement for Outside Plant Equipment meets the minimum ambient temperature requirement for Industrial Equipment
2. Short-term is used as defined in Telcordia Technologies Generic Requirements GR-63-Core Core.
3.  $\theta_{JA}$ , the total junction to ambient thermal resistance, is measured according to JEDEC Standard JESD51 (2S2P).
4.  $\theta_{JB}$ , the junction-to-board thermal resistance, is obtained by simulating conditions described in JEDEC Standard JESD 51-8 and  $\theta_{JT}$ , the junction-to-top thermal resistance, is obtained by simulating conditions described in SEMI Standard G30-88.

## 22 Mechanical Information

The SBSLITE comes in a 15 x 15 x 1.81 mm 160 PBGA (4 layer) package.

**Figure 43 160 Pin PBGA 15x15mm Body**



PACKAGE TYPE : 160 PLASTIC BALL GRID ARRAY - PBGA																
BODY SIZE : 15 x 15 x 1.61 MM (2 layer)																
Dim	A (2 layer)	A (4 layer)	A1	A2	C (2 layer)	C (4 layer)	D	D1	E	E1	I	J	e	b	aaa	bbb
Min.	1.40	1.60	0.30	0.80	0.30	0.50	-	12.50	-	12.50	-	-	-	0.40	-	-
Nom.	1.61	1.81	0.40	0.85	0.36	0.56	15.00	13.00	15.00	13.00	1.00	1.00	1.00	0.50	-	-
Max.	1.80	2.02	0.50	0.90	0.40	0.62	-	13.70	-	13.70	-	-	-	0.60	0.15	0.35

## Notes

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