

# SC70-6 and SOT23-6/8 to DIP-8 Evaluation Board User's Guide

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NOTES:



### **Preface**

### **NOTICE TO CUSTOMERS**

All documentation becomes dated, and this manual is no exception. Microchip tools and documentation are constantly evolving to meet customer needs, so some actual dialogs and/or tool descriptions may differ from those in this document. Please refer to our web site (www.microchip.com) to obtain the latest documentation available.

Documents are identified with a "DS" number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is "DSXXXXXA", where "XXXXXX" is the document number and "A" is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB<sup>®</sup> IDE on-line help. Select the Help menu, and then Topics to open a list of available on-line help files.

### INTRODUCTION

This chapter contains general information that will be useful to know before using the SC70-6 and SOT-23-6/8 to DIP-8 Evaluation Board. Items discussed in this chapter include:

- Document Layout
- · Conventions Used in this Guide
- · The Microchip Web Site
- The Microchip Web Site
- Customer Support
- Document Revision History

### DOCUMENT LAYOUT

This document describes how to use the SC70-6 and SOT-23-6/8 to DIP-8 Evaluation Board as a development tool to emulate and debug firmware on a target board. The manual layout is as follows:

- Chapter 1. "Product Overview" Important information about the SC70-6 and SOT-23-6/8 to DIP-8 Evaluation Board.
- Chapter 2. "Installation and Operation" Includes instructions on how to get started with this evaluation board.
- Appendix A. "Schematic and Layouts" Shows the schematic and layout diagrams for the SC70-6 and SOT-23-6/8 to DIP-8 Evaluation Board.
- Appendix B. "Bill of Materials (BOM)" Lists the parts used to build the SC70-6 and SOT-23-6/8 to DIP-8 Evaluation Board.

### **CONVENTIONS USED IN THIS GUIDE**

This manual uses the following documentation conventions:

### **DOCUMENTATION CONVENTIONS**

| Description                                      | Represents  | Examples                                     |  |
|--|---|--|--|
| Arial font:                                      |   |  |  |
| Italic characters Referenced books               |   | MPLAB <sup>®</sup> IDE User's Guide          |  |
|  | Emphasized text   | is the only compiler                         |  |
| Initial caps                                     | A window  | the Output window                            |  |
|  | A dialog  | the Settings dialog                          |  |
|  | A menu selection  | select Enable Programmer                     |  |
| Quotes   | A field name in a window or dialog  | "Save project before build"                  |  |
| Underlined, italic text with right angle bracket | A menu path   | File>Save                                    |  |
| Bold characters                                  | A dialog button   | Click <b>OK</b>                              |  |
|  | A tab   | Click the <b>Power</b> tab                   |  |
| N'Rnnnn  | A number in verilog format, where N is the total number of digits, R is the radix and n is a digit. |  |  |
| Text in angle brackets < >                       | A key on the keyboard Press <enter>, <f1></f1></enter>  |  |  |
| Courier New font:                                | •   |  |  |
| Plain Courier New                                | Sample source code  | #define START                                |  |
|  | Filenames   | autoexec.bat                                 |  |
|  | File paths  |  |  |
|  | Keywords  | _asm, _endasm, static                        |  |
|  | Command-line options  | -Opa+, -Opa-                                 |  |
|  | Bit values  | 0, 1   |  |
|  | Constants   | 0xFF, 'A'                                    |  |
| Italic Courier New                               | A variable argument   | file.o, where file can be any valid filename |  |
| Square brackets []                               | Optional arguments  | <pre>mcc18 [options] file [options]</pre>    |  |
| Curly brackets and pipe character: {   }         | Choice of mutually exclusive arguments; an OR selection   | errorlevel {0 1}                             |  |
| Ellipses   | Replaces repeated text  | <pre>var_name [, var_name]</pre>             |  |
|  | Represents code supplied by user  | <pre>void main (void) { }</pre>              |  |

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- General Technical Support Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip consultant program member listing
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- Field Application Engineer (FAE)
- · Technical Support
- · Development Systems Information Line

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Technical support is available through the web site at: http://support.microchip.com In addition, there is a Development Systems Information Line which lists the latest versions of Microchip's development systems software products. This line also provides information on how customers can receive currently available upgrade kits.

The Development Systems Information Line numbers are:

1-800-755-2345 - United States and most of Canada

1-480-792-7302 - Other International Locations

### DOCUMENT REVISION HISTORY

### Revision A (October 2009)

· Initial Release of this Document.

| SC70-6 and SOT-23-6/8 to DIP-8 Evaluation Board User's Guide |  |
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|  |  |
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NOTES:

## **Chapter 1. Product Overview**

### 1.1 INTRODUCTION

This chapter provides an overview of the SC70-6 and SOT-23-6/8 to DIP-8 Evaluation Board and covers the following topics:

- What is the SC70-6 and SOT-23-6/8 to DIP-8 Evaluation Board?
- What the SC70-6 and SOT-23-6/8 to DIP-8 Evaluation Board kit includes

### 1.2 WHAT IS THE SC70-6 AND SOT-23-6/8 TO DIP-8 EVALUATION BOARD?

The SC70-6 and SOT-23-6/8 to DIP-8 Evaluation Board allows the system designer to quickly evaluate the operation of Microchip Technology's devices in any of the following packages:

- SC70-6
- SC70-5
- SC70-3
- SOT-23-8
- SOT-23-6
- SOT-23-5
- SOT-23-3
- DIP-8

The board has a 6-pin header (PICkit Serial, ICSP, etc.) that can be easily jumpered to the device's desired pins to communicate with the device (using PICkit Serial) or in the case of PIC microcontrollers or EEPROM, programmed (using ICSP).

Figure 1-1 shows the top view of the PCB. The board allows the devices to easily be jumpered into a desired circuit. Also, the SC70 and SOT-23 packages could be converted to a DIP footprint. Each pad has a passive component footprint that is connected to the VDD plane (RxU) and a second passive component footprint that is connected to the VSS plane (RxD).

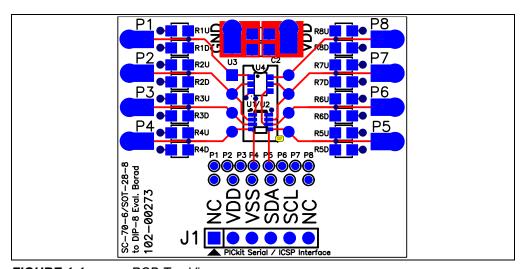


FIGURE 1-1: PCB Top View.

### SC70-6 and SOT-23-6/8 to DIP-8 Evaluation Board User's Guide

Devices from the following Microchip product families can be installed into this PCB:

- A/D Converters (ADCs)
- · Battery Management
- CAN
- Comparators
- D/A Converters (DACs)
- DC-to-DC Converters
- Digital Potentiometers (Digi-Pots)
- EEPROM Serial Memory
- · Fan Controllers
- IrDA
- LIN
- · Linear Regulators
- Operational Amplifiers (Op Amps)
- · Piezoelectric Horn Driver
- Power MOSFET Drivers
- Programmable Gain Amplifiers (PGAs)
- · Selectable Gain Amplifiers
- · Smoke Detection Front End
- Switching Regulators
- Temperature Sensors
- · Voltage References
- · Voltage Supervisors and Detectors
- PICmicro<sup>®</sup> Microcontrollers

# 1.3 WHAT THE SC70-6 AND SOT-23-6/8 TO DIP-8 EVALUATION BOARD KIT INCLUDES

This SC70-6 and SOT-23-6/8 to DIP-8 Evaluation Board kit includes:

- SC70-6 and SOT-23-6/8 to DIP-8 Evaluation Board, 102-00273
- Important Information Sheet



## Chapter 2. Installation and Operation

### 2.1 INTRODUCTION

The SC70-6 and SOT-23-6/8 to DIP-8 Evaluation Board allows the system designer to quickly evaluate the operation of devices. This board is generic so that any device, of the appropriate footprint, may be installed. Refer to the device data sheet, however, for suitability of device evaluation (noise, lead length, signal integrity, etc).

As well as the device, other desired passive components (resistors and capacitors) and connection posts may be installed. This allows the board to evaluate a minimum configuration for the device. Also, this allows the device to be easily jumpered into an existing system.

The board also has a 6-pin interface (PICkit Serial, ICSP, BFMP, etc.) whose signals can easily be jumpered to any of the device's pins.

### 2.2 FEATURES

The SC70-6 and SOT-23-6/8 to DIP-8 Evaluation Board has the following features:

- · Connection terminals may be either through-hole or surface-mount
- Three package type footprints supported:
  - SC70-6
  - SC70-5
  - SC70-3
  - SOT-23-8
  - SOT-23-6
  - SOT-23-5
  - SOT-23-3
  - DIP-8 (300 millimeter spacing)
- Footprints for optional passive components (SMT 805 footprint) for:
  - Power supply filtering (C<sub>1</sub> and C<sub>2</sub> footprints)
  - Device bypass capacitor (RxD footprint for device pin connected to V<sub>DD</sub>)
  - Output filtering (RxD footprint)
  - Output pull-up resistor (RxU footprint)
  - Output pull-down resistor (RxD footprint)
  - Output loading resistor (RxD footprint)
- Silk-screen area to write specifics of implemented circuit (on back of PCB), such as MCP4018 10  $k\Omega$
- · Can be used for SC70 or SOT-23 to DIP-8 converter
- PICkit Serial Analyzer / PICkit 2 Programming (ICSP) Header

### 2.3 GETTING STARTED

The SC70-6 and SOT-23-6/8 to DIP-8 Evaluation Board is a blank PCB that allows the user to configure the circuit to the exact requirements. The passive components use the surface-mount 805 package layout.

This evaluation board supports the following Microchip product device families:

- A/D Converters (ADCs)
- · Battery Management
- CAN
- Comparators
- D/A Converters (DACs)
- DC-to-DC Converters
- Digital Potentiometers (Digi-Pots)
- EEPROM Serial Memory
- · Fan Controllers
- IrDA
- LIN
- · Linear Regulators
- Operational Amplifiers (Op Amps)
- · Piezoelectric Horn Driver
- Power MOSFET Drivers
- · Programmable Gain Amplifiers (PGAs)
- · Selectable Gain Amplifiers
- · Smoke Detection Front End
- · Switching Regulators
- Temperature Sensors
- Voltage References
- · Voltage Supervisors and Detectors
- PICmicro<sup>®</sup> Microcontrollers

Figure 2-1 shows the evaluation board circuit. The pins on the 8-pin SOT-23-8 and DIP devices are tied together (pin number to pin number). The pins of the6-pin SC70 and SOT-23 devices are tied as if the DIP was a 6-pin DIP. This circuit allows each pin to individually have any of the following: a pull-up resistor, a pull-down resistor (or a loading/filtering capacitor). Power supply filtering capacitors are connected between the VDD and VSS pads (C1 and C2).

The circuit has a 6-pin header that can be used for PICkit Serial communication as well as PIC ICSP. The signals of this header would need to be jumpered to the appropriate device signal.

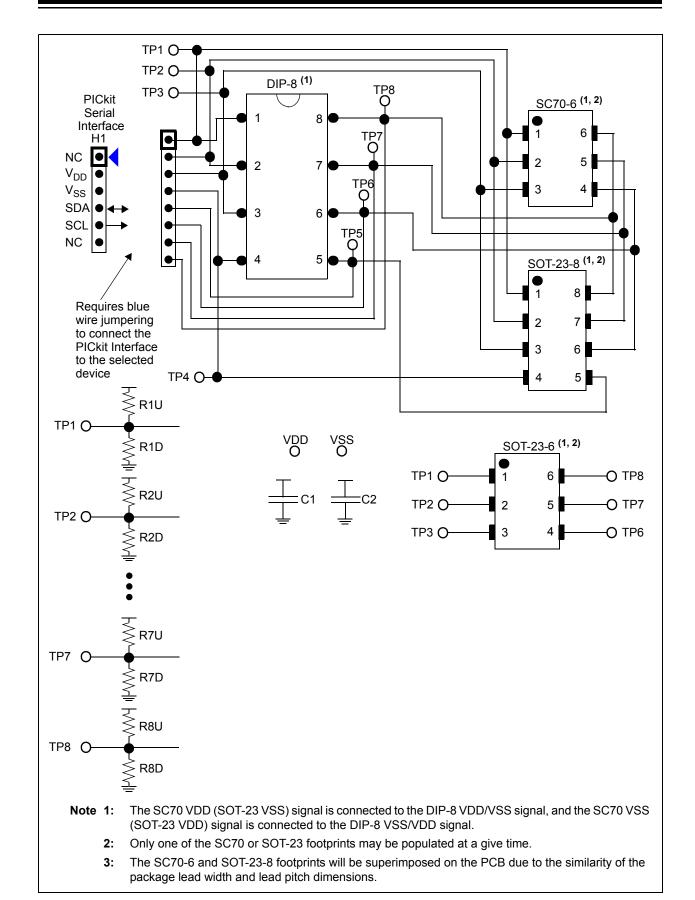


FIGURE 2-1: SC70-6 and SOT-23-6/8 to DIP-8 Evaluation Board Circuit.

### 2.3.1 The Hardware

Figure 2-2 shows the component layout of the SC70-6 and SOT-23-6/8 to DIP-8 Evaluation Board. This is a small four-layer board (1.43" x 1.255" (36.322 mm x 31.877 mm)). There are ten connection points/pads that can use either through-hole or surface-mount connector posts.

The pad labeled VDD is connected to the PCB power plane, while the pad labeled VSS is connected to the PCB ground plane. All the passive components that are connected to VDD or VSS are connected to either the power plane or ground plane.

The eight remaining PCB pads correspond to the device pins (i.e.; pad 1 connects to pin 1).

Each pad has two passive components associated with them: a pull-up resistor and a pull-down resistor. The pull-up resistor is always RXU and the pull-down resistor is RXD. The "X" is a numeric value that corresponds to a particular pad (1 to 8). As an example, Pad 5's pull-up resistor is R5U. Capacitor C1 and C2 are the power supply filtering capacitors. For whichever pin is the device's VDD, the RxD component footprint can be used for the device's bypass capacitor. Table 2-1 describes the components.

A 6-pin header interface is available to support the PICkit Serial or the PICmicro In-Circuit Serial Programming (ICSP) interface. For additional information, refer to Section 2.4.5 "PICkit Serial or In-Circuit Serial Programming (ICSP) Interface (Header J1)".

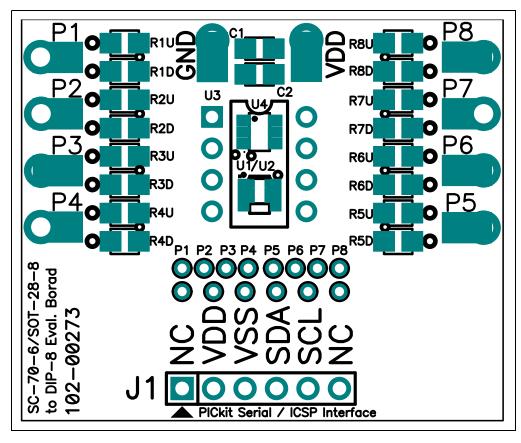


FIGURE 2-2: SC70-6 and SOT-23-6/8 to DIP-8 Evaluation Board Layout.

TABLE 2-1: OPTIONAL PASSIVE COMPONENTS (2)

| Component                              | Comment                        |
|--|--------------------------------|
| C1, C2                                 | Power supply bypass capacitors |
| R1U, R2U, R3U, R4U, R5U, R6U, R7U, R8U | Pull-up resistor               |
| R1D, R2D, R3D, R4D, R5D, R6D, R7D, R8D | Pull-down resistor (1)         |

- **Note 1:** Whichever pin is the device's VDD pin, that corresponding RXD footprint can be used for the device's bypass capacitor. So if Pin 8 is the device's VDD pin, then install the bypass capacitor in the R8D footprint.
  - 2: All passive components use the surface mount 805 footprint

### 2.4 SC70-6 AND SOT-23-6/8 TO DIP-8 EVALUATION BOARD DESCRIPTION

The SC70-6 and SOT-23-6/8 to DIP-8 Evaluation Board PCB is designed to be flexible in the type of device evaluation that can be implemented.

The following sections describe each element of this evaluation board in further detail. Refer to Figure 2-3.

### 2.4.1 Power and Ground

The SC70-6 and SOT-23-6/8 to DIP-8 Evaluation Board has a VDD Pad and a VSS pad. These pads can have connection posts installed that allows easy connection to the power ( $V_{DD}$ ) and ground ( $V_{SS}$ ) planes. The layout allows either through-hole or surface-mount connectors.

The power and ground planes are connected to the appropriate passive components on the PCB (such as power plane to RXU and ground plane to RXD components).

### 2.4.2 PCB PADs

For each package pin (pins 1 to 8), there is a PCB pad (pads 1 to 8). The device will have some power pins ( $V_{DD}$ ) and some ground pins ( $V_{SS}$ ). To ease connections on the PCB, vias to the power and ground plane have been installed close to each PCB pad. This allows any pad to be connected to the power or ground plane (see Figure 2-3). So when power is connected to the VDD and VSS pads, the power is connected to the appropriate device pin.

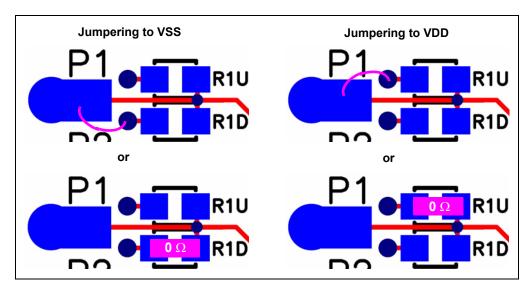


FIGURE 2-3: Connecting the PCB pad to either VDD or VSS.

### 2.4.3 Passive Components (RXU, RXD, C1, and C2)

The footprints for these components are present to allow maximum flexibility in the use of this PCB to evaluate a wide range of devices. The purpose of these components may vary depending on the device under evaluation and how it is to be used in the desired circuit. Refer to the device data sheet for the recommended components that should be used when evaluating that device.

- Component RXU allows a pull-up resistor to be installed for the device pin
- Component RXD allows a pull-down resistor or a a capacitive load/filter to be installed for the device pin
- Component C1 and C2 allows power supply filtering capacitors to be installed

### 2.4.4 Device Footprints

This section describes the characteristics of the component footprints so that you are better able to determine if the desired component(s) will be compatible with the board.

#### 2.4.4.1 SC70-6 AND SOT-23-8

The 6-pin SC70 footprint has been superimposed on the 8-pin SOT-23 footprint. Figure 2-4 shows how the SC70-6 and the SOT-23-8 footprint have been superimposed. This was done since the pin pitch and width are identical for these two packages. Only the body width is different (the SC70 is narrower).

The 6-pin SC70 and 8-pin SOT-23 footprint is laid out for packages that have a typical pitch of 0.65 mm (BSC), a maximum lead width of 0.30 mm.

The 6-pin SC70 footprint has a molded package width of 1.25 mm (BSC), while the 8-pin SOT-23 footprint has a maximum molded package width of 1.75 mm.

Packages that meet these characteristics should be able to be used with this board.

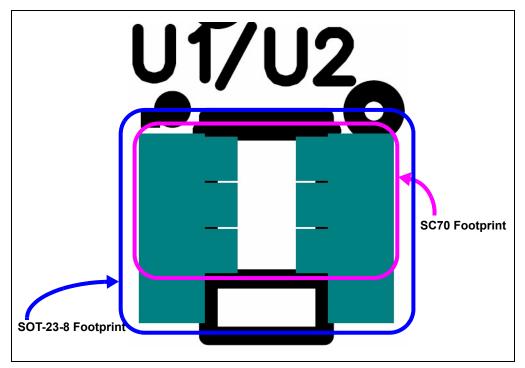


FIGURE 2-4: Superimposing of SC70-6 and SOT-23-8 Footprints.

### **Installation and Operation**

### 2.4.4.2 SOT-23-6

The 6-pin SOT-23 footprint is laid out for packages that have a typical pitch of 0.65 mm (BSC), a maximum lead width of 0.45 mm, and a maximum molded package width of 1.75 mm. Six lead SOT-23 packages that meet these characteristics should be able to be used with this board.

### 2.4.4.3 DIP-8

The 8-pin DIP footprint is laid out for packages that have a typical pitch of 100 mil (BSC), a maximum lead width of 22 mil, and a molded package width of 300 mil. 8-lead SOT-23 packages that meet these characteristics should be able to be used with this board.

### 2.4.4.4 PASSIVE COMPONENTS

All passive components (RXU, RXD, and CX) use a surface mount 805 footprint. Any component that has a compatible footprint could be used with this board.

### 2.4.4.5 HEADER (1X6)

The header has a typical pitch of 100 mil (BSC). This header is designed to be compatible with the PICkit Serial Analyzer and PICkit 2 Programmer.

# 2.4.5 PICkit Serial or In-Circuit Serial Programming (ICSP) Interface (Header J1)

Figure 2-5 shows the interface connection of Header J1. The VDD and VSS signals are connected to the appropriate power or ground plane. The other four signals are open and can be easily jumpered to any of the eight P1 through P8 connection points.

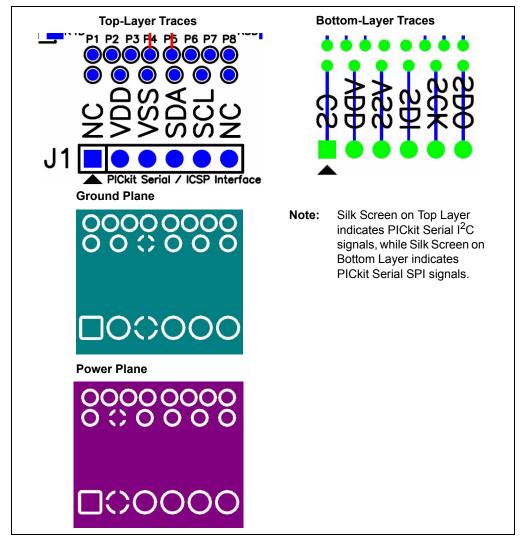


FIGURE 2-5: PICkit Serial / ICSP Interface Connections.

### 2.4.5.1 PICKIT SERIAL INTERFACE

Table 2-2 shows the pin number assignment for the different signals for each of the supported interface protocols (SPI,  $I^2C$ , etc.)

TABLE 2-2: PICKIT SERIAL HEADER SIGNALS

| Pin    |     | PICkit           | Comments |           |           |          |
|--------|-----|------------------|----------|-----------|-----------|----------|
| Number | SPI | I <sup>2</sup> C | USART    | Microwire | LIN       | Comments |
| 1      | CS  | _                | TX       | CS        | TX        |          |
| 2      | VDD | VDD              | VDD      | VDD       | _         |          |
| 3      | VSS | VSS              | VSS      | VSS       | VSS       |          |
| 4      | SDI | SDA              | _        | SDI       | CS/WAKE   |          |
| 5      | SCK | SCL              | _        | SCK       | FAULT/TXE |          |
| 6      | SDO | _                | RX       | SDO       | RX        |          |

### 2.4.5.2 ICSP INTERFACE

The ICSP interface allows a PICmicro MCU device to be programmed with programmers that support this interface, such as the PICkit 2 programmer (part number PG164120). Table 2-3 shows the pin number assignment for the ICSP signals.

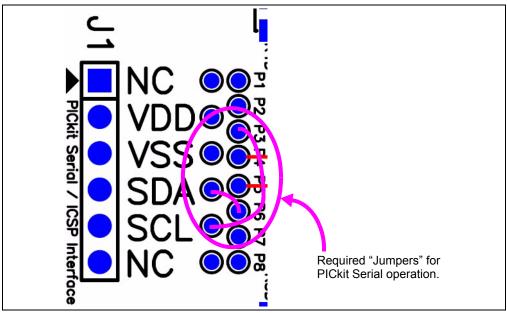
TABLE 2-3: ICSP HEADER SIGNALS

|               | 100. 112.12 21.010.11.120 |                     |  |
|---------------|---------------------------|---------------------|--|
| Pin<br>Number | ICSP Signal               | Comments            |  |
| 1             | VPP                       | High Voltage Signal |  |
| 2             | VDD                       |                     |  |
| 3             | VSS                       |                     |  |
| 4             | DT                        | ICSP™ Data          |  |
| 5             | CLK                       | ICSP™ Clock         |  |
| 6             | _                         |                     |  |

## 2.4.6 Evaluating the MCP4018 Device (A Digital Potentiometer with I<sup>2</sup>C interface)

The MCP4018 is a Digital Potentiometer that is in a 6-lead SC70 package with an I<sup>2</sup>C serial interface. This allows the device to be communicated to (Read and Write) by the PICkit Serial Analyzer. For this to occur, the PICkit Serial Analyzer signals must be connected to the correct MCP4018 signals. These connections are shown in Figure 2-6.

Other Digital Potentiometers that are supported by this evaluation board are shown in Table 2-4.

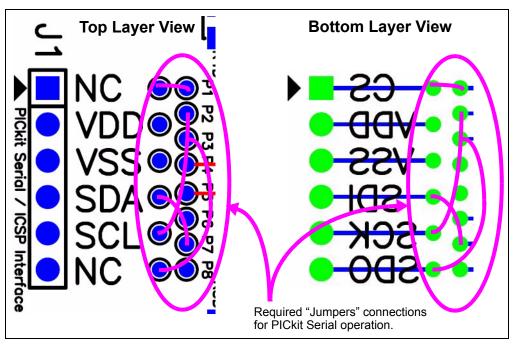


**FIGURE 2-6:** PICkit Serial / ICSP Header and Example Connections (for MCP4018 - I<sup>2</sup>C interface).

# 2.4.7 Evaluating the MCP41X2 Device (A Digital Potentiometer with SPI interface)

The MCP41X2 is a Digital Potentiometer that is in a 8-lead DIP package with an SPI serial interface. This allows the device to be communicated to (Read and Write) by the PICkit Serial Analyzer. For this to occur, the PICkit Serial Analyzer signals must be connected to the correct MCP41X2 signals. These connections are shown in Figure 2-7.

Other Digital Potentiometers that are supported by this evaluation board are shown in Table 2-4.



**FIGURE 2-7:** PICkit Serial / ICSP Header and Example Connections (for MCP41X2 - SPI Interface).

### 2.4.8 The PCB as a SC70, SOT-23 to DIP Socket Converter

There may be occasions when it is desirable to convert the footprint of the device to that of a DIP package. This allows the device to be installed into an existing DIP socket. Two 1x4 row pins need to be installed into the PCB's DIP footprint (on the bottom) when the device is installed into the appropriate package footprint.

This allows the PCB to convert the SC70 and SOT-23 footprints to a 300-mil DIP-8 footprint.

TABLE 2-4: SUPPORTED DIGITAL POTENTIOMETERS

| IADLL 2-4. | 3011 OKTED DIGITAL I OTENTIONIE TEKS |        |     |                                  |  |
|------------|--------------------------------------|--------|-----|----------------------------------|--|
| Device     | SC70                                 | SOT-23 | DIP | Comment                          |  |
| MCP4012    | _                                    | Yes    | _   | SOT-23-6, uses Up/Down interface |  |
| MCP4013    | _                                    | Yes    | _   | SOT-23-6, uses Up/Down interface |  |
| MCP4014    | _                                    | Yes    |     | SOT-23-5, uses Up/Down interface |  |
| MCP4017    | Yes                                  | _      | 1   |                                  |  |
| MCP40D17   | Yes                                  | _      | l   |                                  |  |
| MCP4018    | Yes                                  | _      | l   |                                  |  |
| MCP40D18   | Yes                                  | _      | 1   |                                  |  |
| MCP4019    | Yes                                  | _      | l   |                                  |  |
| MCP40D19   | Yes                                  | _      | l   |                                  |  |
| MCP4022    |                                      | Yes    | 1   | SOT-23-6, uses Up/Down interface |  |
| MCP4023    |                                      | Yes    | l   | SOT-23-6, uses Up/Down interface |  |
| MCP4024    |                                      | Yes    | l   | SOT-23-5, uses Up/Down interface |  |
| MCP4131    |                                      | _      | Yes | Has multiplexed SDI/SDO          |  |
| MCP4132    |                                      | _      | Yes |                                  |  |
| MCP4141    | _                                    |        | Yes | Has multiplexed SDI/SDO          |  |
| MCP4142    |                                      | _      | Yes |                                  |  |
| MCP4151    | _                                    |        | Yes | Has multiplexed SDI/SDO          |  |
| MCP4152    | _                                    |        | Yes |                                  |  |
| MCP4161    | _                                    | _      | Yes | Has multiplexed SDI/SDO          |  |
| MCP4162    | _                                    | _      | Yes |                                  |  |
| MCP41010   | _                                    | _      | Yes |                                  |  |
| MCP41050   | _                                    | _      | Yes |                                  |  |
| MCP41100   |                                      | _      | Yes |                                  |  |



## Appendix A. Schematic and Layouts

### A.1 INTRODUCTION

This appendix contains the schematics and layouts for the SC70-6 and SOT-23-6/8 to DIP-8 Evaluation Board. Diagrams included in this appendix:

- · Board Schematic
- · Board Top Trace, Silk and Pads
- · Board Bottom Trace & Pads
- · Board Layer 2 Ground Plane
- · Board Layer 3 Power Plane
- · Board Bottom Silk, Trace and Pads

### A.2 SCHEMATICS AND PCB LAYOUT

Board - Schematic shows the schematic of the SC70-6 and SOT-23-6/8 to DIP-8 Evaluation Board. The layer order is shown in Figure A-1.

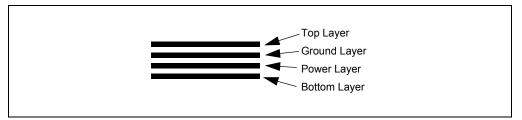
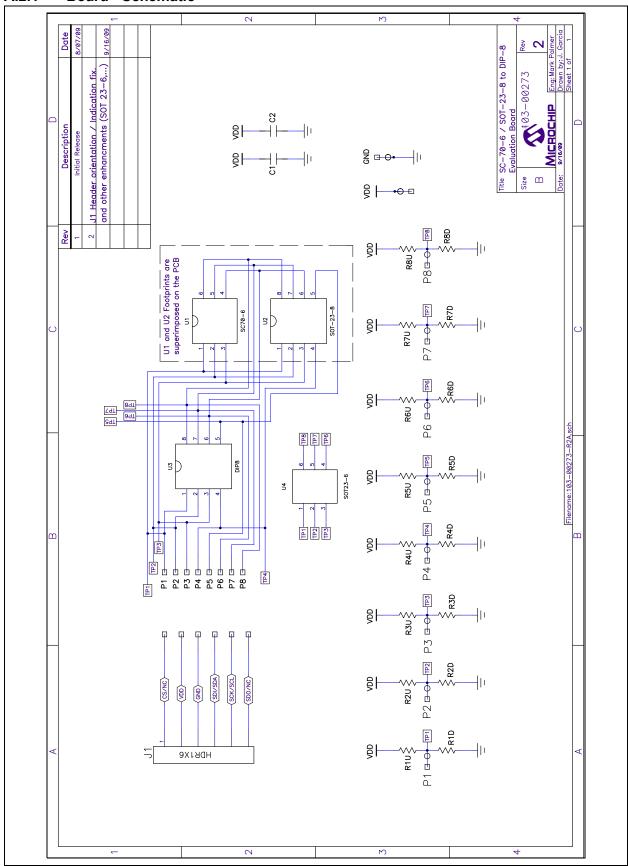
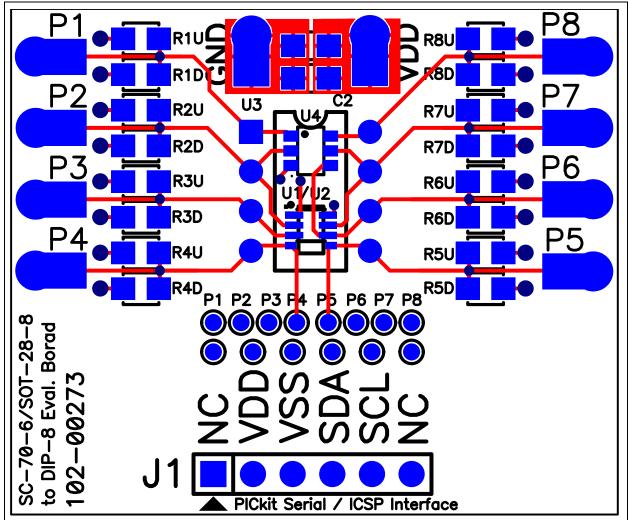


FIGURE A-1: Layer Order.

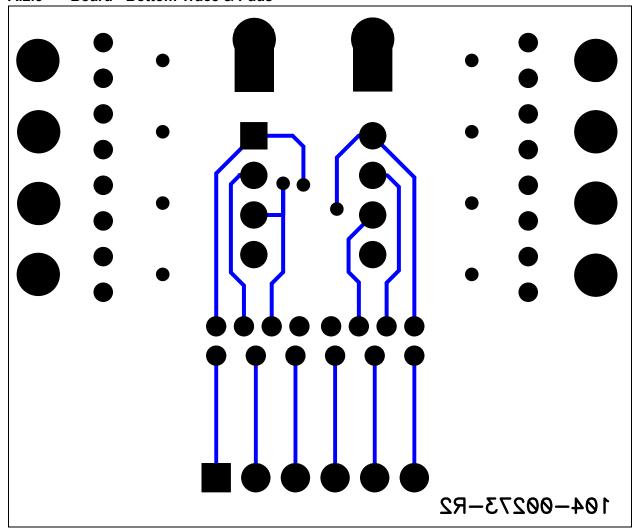
### A.2.1 Board - Schematic



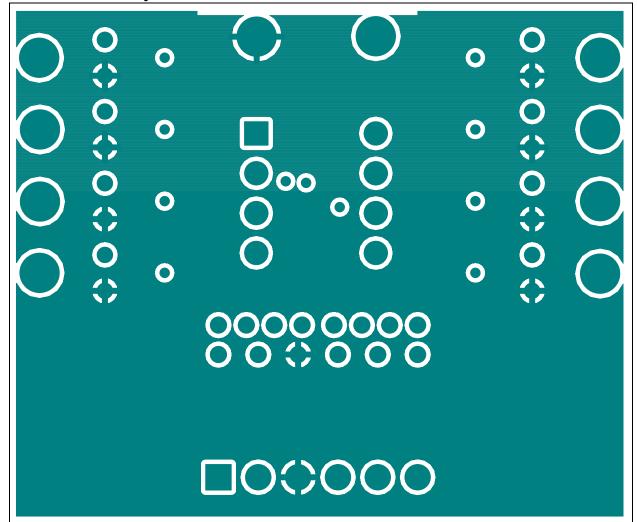
A.2.2 Board - Top Trace, Silk and Pads



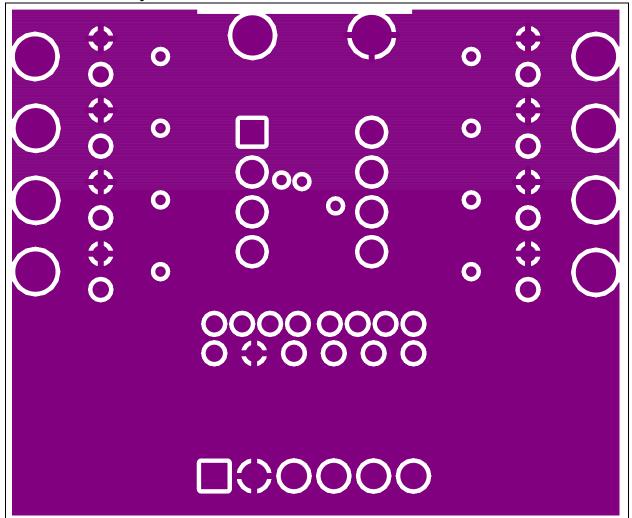
### A.2.3 Board - Bottom Trace & Pads



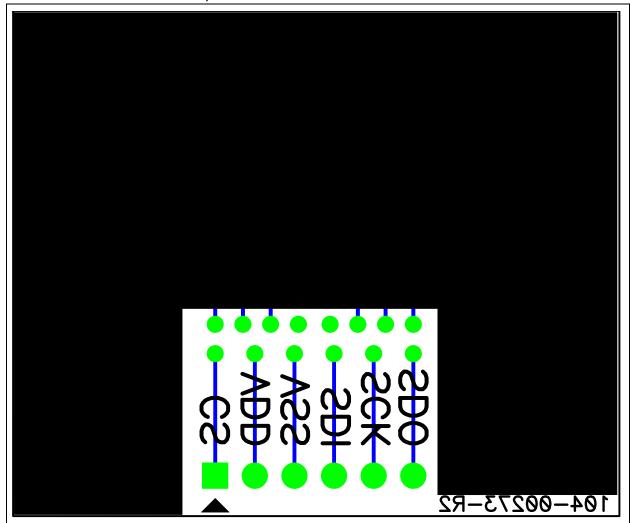
### A.2.4 Board - Layer 2 Ground Plane



### A.2.5 Board - Layer 3 Power Plane



### A.2.6 Board - Bottom Silk, Trace and Pads



| SC70-6 and SOT-23-6/8 to DIP-8 Evaluation Board User's Guide |
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## Appendix B. Bill of Materials (BOM)

TABLE B-1: BILL OF MATERIALS

| Qty | Reference   | Description  | Manufacturer                         | Part Number    |
|-----|---|--|--------------------------------------|----------------|
| 1   | PCB   | RoHS Compliant Bare PCB, SC70-6 and-<br>SOT-23-6/8 to DIP-8 Evaluation Board                                 | Microchip<br>Technology Inc.         | 104-00273      |
| 0   | C1, C2  | Device Power Supply inItering Capacitor<br>Surface-mount (805 package)<br>(Optional - Application-dependent) | _                                    | User-specified |
| 0   | J1  | PICkit Serial or BFMP Header (6-pin, 100 mil spacing)  | _                                    | _              |
| 0   | P1, P2, P3, P4,<br>P5, P6, P7, P8,<br>V <sub>DD</sub> , V <sub>SS</sub> | Through-hole connector(s) for P1, P2, P3, P4, P5, P6, P7, P8, V <sub>DD</sub> , V <sub>SS</sub>              | Keystone<br>Electronics <sup>®</sup> | 5012           |
| 0   | P1, P2, P3, P4,<br>P5, P6, P7, P8,<br>V <sub>DD</sub> , V <sub>SS</sub> | Surface-mount connector(s) for P1, P2, P3, P4, P5, P6, P7, P8, V <sub>DD</sub> , V <sub>SS</sub>             | Keystone<br>Electronics <sup>®</sup> | 5016           |
| 0   | R1U, R2U, R3U,<br>R4U, R5U, R6U,<br>R7U, R8U                            | Pin Pull-up resistor<br>Surface-mount (805 package)<br>(Optional - Application-dependent)                    | _                                    | User-specified |
| 0   | R3A, R3B, R3C,<br>R3D, R3E, R3F,<br>R3G, R3H                            | Pin Pull-down resistor <sup>(1)</sup> Surface-mount (805 package) (Optional - Application-dependent)         | _                                    | User-specified |
| 0   | U1  | SC70-6 Device (supports SC70-5 and SC70-3 devices)   | _                                    | User-specified |
| 0   | U2  | SOT23-8 Device   | _                                    | User-specified |
| 0   | U3  | DIP-8 Device   | _                                    | User-specified |
| 0   | U4  | SOT23-6 Device (Supports SOT23-5 and SOT23-3 devices)  | _                                    | User-specified |

**Note 1:** These footprints could be used for pin signal filtering by using a capacitor.

<sup>2:</sup> The components listed in this Bill of Materials are representative of the PCB assembly. The released BOM used in manufacturing uses all RoHS-compliant components

| SC70-6 and SOT-23-6/8 to DIP-8 Evaluation | on Board User's Guide |
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## Appendix C. Board Revision 1 Errata

### C.1 ISSUE

The Revision 1 of this PCB has an issue when the PICkit Serial / ICSP Interface Header (J1) pin 1 is incorrectly assigned to the PICkit Serials pin 6. This means that the orientation marker on the PCB are incorrect for the PICkit Serial Analyzer.

### C.2 SOLUTION

Orientate the PICkit Serial Analyzer pin 1 to the PCB pin 6. Revision 2 of the Schematic and PCB addresses this issue.

### C.3 HOW TO DETERMINE PCB REVISION

Look at the bottom layer of the board (see Figure C.4.5), in the bottom right corner. You will see some text, 104-00273-R1. The R1 indicates that the PCB is Revision 1.

### C.4 SCHEMATICS AND PCB LAYOUT OF REVISION 1

Board - Schematic - Revision 1 shows the schematic of the SC70-6 and SOT-23-6/8 to DIP-8 Evaluation Board.

Board - Revision 1 - Top Layer and Silk shows the layout for the top layer of the SC70-6 and SOT-23-6/8 to DIP-8 Evaluation Board. The layer order is shown in Figure C-1.

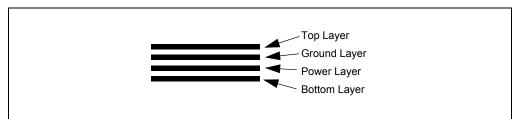
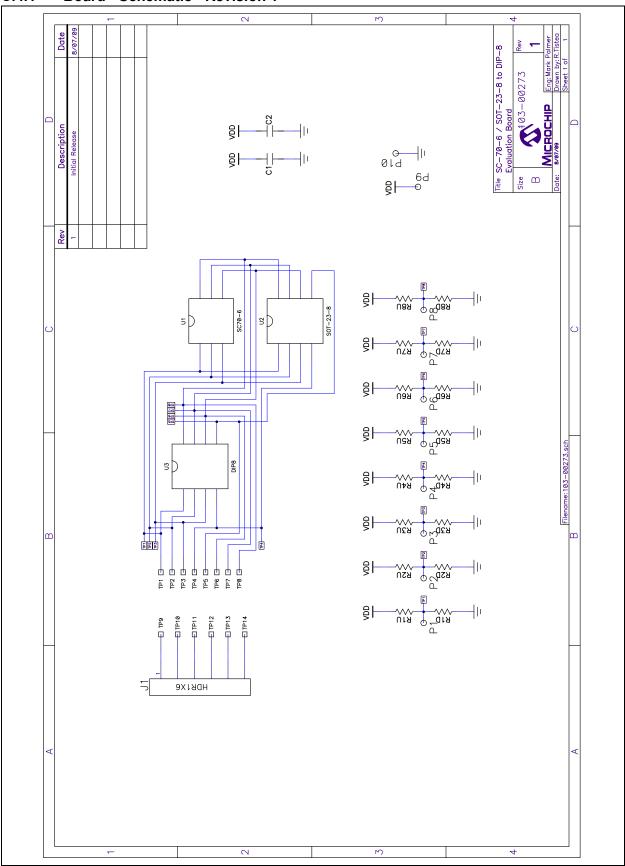
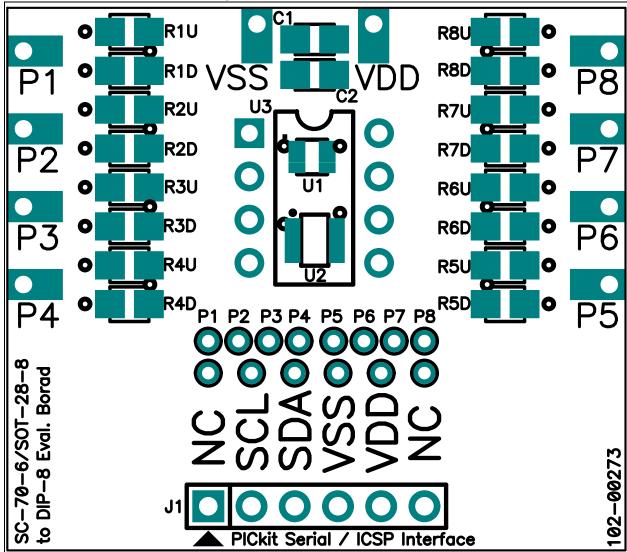


FIGURE C-1: Layer Order.

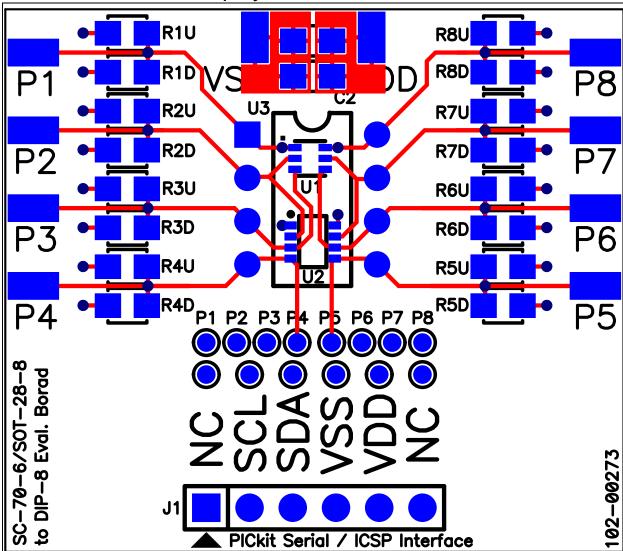
### C.4.1 Board - Schematic - Revision 1



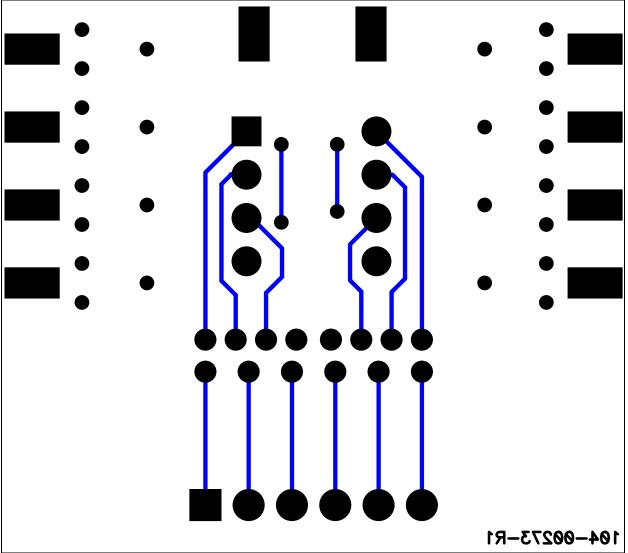
### C.4.2 Board - Revision 1 - Layout Components and Silk



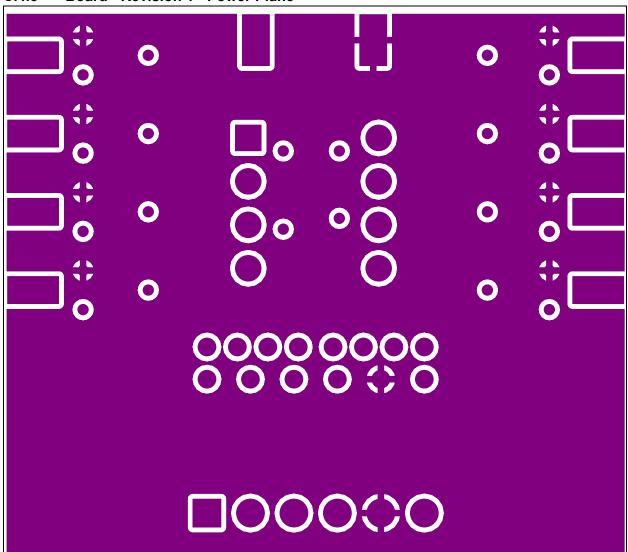
### C.4.3 Board - Revision 1 - Top Layer and Silk



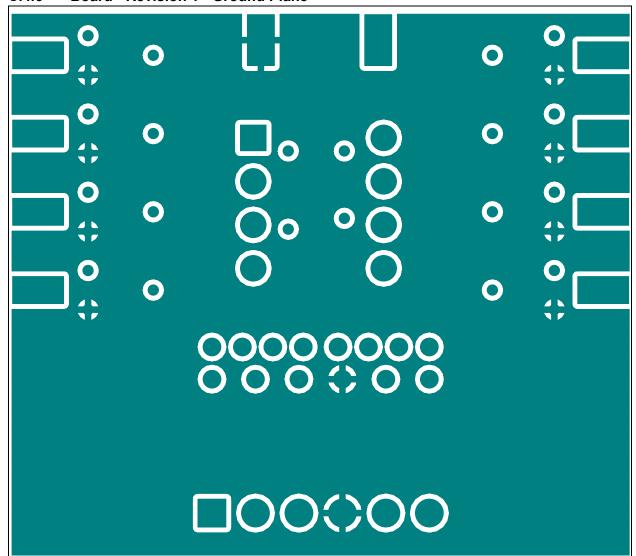












### C.4.7 Board - Revision 1 - Bottom



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| D | vai | u  | NE | VIS | IUH |   |    | ιαια |

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