MICROCHIP

SSC7150

Motion Coprocessor

Product Features

- High Performance 32-bit Embedded Controller
- Low power 7.65mA (typ) in active mode
- System in deep sleep consumes 70µA (typ)
- 3.3-Volt I/O
- Package
  - 6mm x 6mm, 28-pin QFN

Sensor Firmware

- Sensor fusion firmware features include:
  - Self-contained 9-axis sensor fusion
  - Sensor data pass-through
  - Fast in-use background calibration of all sensors and calibration monitor
  - Magnetic immunity: Enhanced magnetic distortion detection and suppression
  - Gyroscope drift cancellation
- Easy to implement complete turnkey sensor fusion solution
- Sensor power management
- Sensors Supported
  - Bosch BMC150 Geomagnetic Sensor/Accelerometer
  - Bosch BMG160 Gyroscope

Hardware Features

The hardware features in the SSC7150 motion coprocessor include the following:

- Two I^2C Controllers
  - Supports I^2C bus speeds to 400kHz
  - Host Interface Supports Slave Operation
  - Sensor Interface Supports Master Operation
- Low Power Modes

Target Markets

- Remote Controls, Gaming
- Fitness Monitoring
- Internet of Things Applications

Description

The SSC7150 motion coprocessor is a low-power, flexible, turnkey solution. SSC7150 makes implementing sensor fusion easy for motion-based embedded applications. Microchip created this solution, enabling faster time to market without the need for sensor-fusion expertise. The SSC7150 is extremely efficient. Low average current while running complex sensor-fusion algorithms results in lower power consumption for multiple applications.

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Table of Contents

1.0 PIN CONFIGURATION

1.1 Description

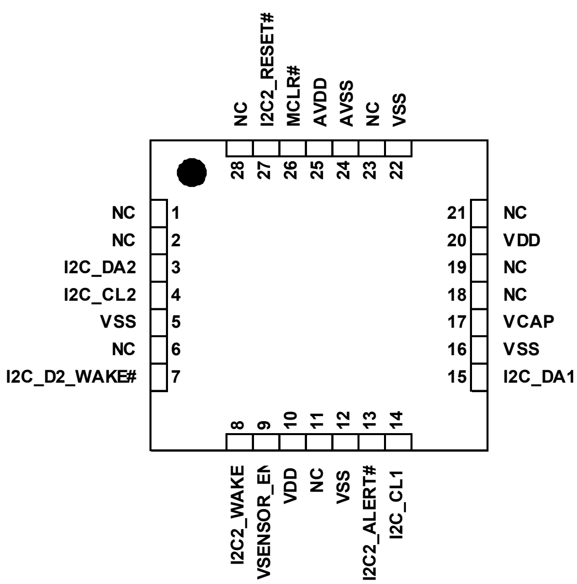
The Pin Configuration chapter includes a Pin Diagram, Pin List, Pin Description and Package Details.

1.2 Terminology and Symbols for Pins/Buffers

Term	Definition
#	The '#' sign at the end of a signal name indicates an active-low signal.

1.3 Pin Diagram

FIGURE 1-1: 28 PIN QFN PIN DIAGRAM



Note:	The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

1.4 Pin List

The Pin List is shown in Table 1-1.

TABLE 1-1: SSC7150 28 QFN PIN CONFIGURATION

28 QFN Number	Pin Name
1	NC
2	NC
3	I2C_DA2
4	I2C_CL2
5	VSS
6	NC
7	I2C_D2_WAKE#
8	I2C2_WAKE
9	VSENSOR_EN
10	VDD
11	NC
12	VSS
13	I2C2_ALERT#
14	I2C_CL1
15	I2C_DA1
16	VSS
17	VCAP
18	NC
19	NC
20	VDD
21	NC
22	VSS
23	NC
24	AVSS
25	AVDD
26	MCLR#
27	I2C2_RESET#
28	NC

1.4.1 FIVE VOLT TOLERANT PINS

Table 1-2 lists the 5 Volt tolerant pins in the SSC7150. All other pins in the device are 3.3V only.

TABLE 1-2: 5V-TOLERANT PINS

Pin Number	Pin Name
13	I2C2_ALERT#
14	I2C_CL1
15	I2C_DA1
26	MCLR#

1.5 Pin Description

1.5.1 OVERVIEW

The following tables describe the signal functions in the SSC7150 pin configuration. See Section 1.6, "Notes for Tables in this Chapter," on page 7 for notes that are referenced in the Pin Description tables.

1.5.2 HOST INTERFACE

The SSC7150 can be used with an I^2C host interface. The pins required for each interface are shown in Table 1-3 and Table 1-4. See the associated Notes for board connection information for the unused interface.

TABLE 1-3: I^2C HOST INTERFACE

I2C Interface Signals			
Pin Ref. Number	**Signal Name**	**Description**	**Notes**
4	I2C_CL2	I2C Controller Clock to Host Interface	
3	I2C_DA2	I2C Controller Data to Host Interface	
13	I2C2_ALERT#	Alert Interrupt signal from motion coprocessor to Host. Used to tell Host data from motion coprocessor is ready to be sent out. Active low output.	
7	I2C_D2_WAKE#	Used to wake the motion coprocessor from a low power state due to host I2C communication. Active low input. Connect to I2C_DA2.	
8	I2C2_WAKE	Used to wake motion coprocessor from a Sleep state. This signal must be driven high at least 11ms prior to sending any I2C traffic to the motion coprocessor. Active high input.	
27	I2C2_RESET#	Reset input. Used to reset the host I2C interface.	

1.5.3 I^2C SENSOR INTERFACE

TABLE 1-4: I^2C SENSOR INTERFACE

I2C Sensor Interface			
Pin Ref. Number	**Signal Name**	**Description**	**Notes**
14	I2C_CL1	I2C Controller Clock to Sensor Interface	
15	I2C_DA1	I2C Controller Data to Sensor Interface	

1.5.4 MISCELLANEOUS FUNCTIONS

TABLE 1-5: MISCELLANEOUS FUNCTIONS

Miscellaneous Functions			
Pin Ref. Number	**Signal Name**	**Description**	**Notes**
26	MCLR#	Master Clear (Reset) Input	Note 1
9	VSENSOR_EN	Sensor voltage switch control output.	
1, 2, 6, 11, 18, 19, 21, 23, 28	NC	Pins labelled NC should be left unconnected on the board	

1.5.5 POWER INTERFACE

TABLE 1-6: POWER INTERFACE

Power Interface			
Pin Ref. Number	**Signal Name**	**Description**	**Notes**
17	VCAP	Internal Voltage Regulator Capacitor	Note 2
10, 20	VDD	VDD supply	
5, 12, 16, 22	VSS	VDD associated ground	
25	AVDD	AVDD supply	
24	AVSS	AVDD associated ground	

1.6 Notes for Tables in this Chapter

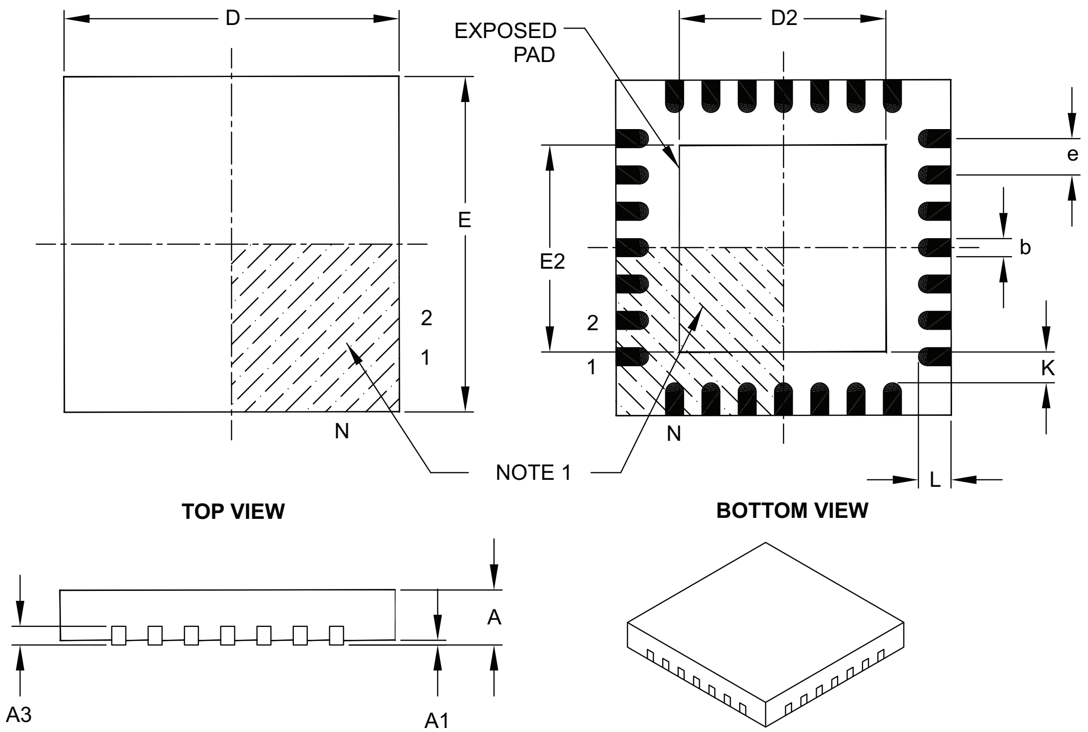
Note 1	A pull-up to VDD is required on the MCLR# pin. Use a 10K ohm pull-up resistor.
Note 2	A low-ESR (1 Ohm) capacitor is required on the VCAP pin, which is used to stabilize the internal voltage regulator output. The VCAP pin must not be connected to VDD, and must have a CEFC capacitor, with at least a 6V rating, connected to ground. The type can be ceramic or tantalum.

1.7 Package Details

This section provides the technical details of the packages.

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



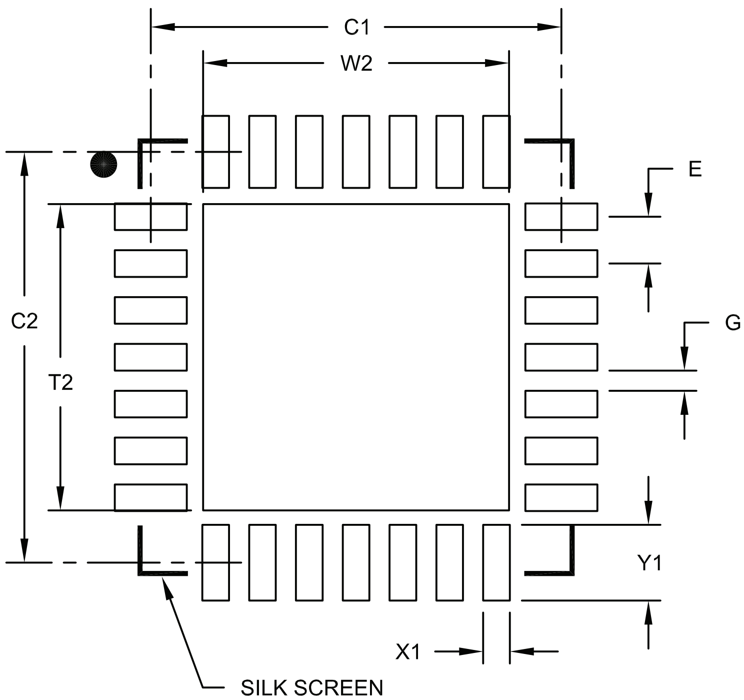
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Width	E	6.00 BSC		
Exposed Pad Width	E2	3.65	3.70	4.20
Overall Length	D	6.00 BSC		
Exposed Pad Length	D2	3.65	3.70	4.20
Contact Width	b	0.23	0.30	0.35
Contact Length	L	0.50	0.55	0.70
Contact-to-Exposed Pad	K	0.20	–	–

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-105B

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			4.25
Optional Center Pad Length	T2			4.25
Contact Pad Spacing	C1		5.70	
Contact Pad Spacing	C2		5.70	
Contact Pad Width (X28)	X1			0.37
Contact Pad Length (X28)	Y1			1.00
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

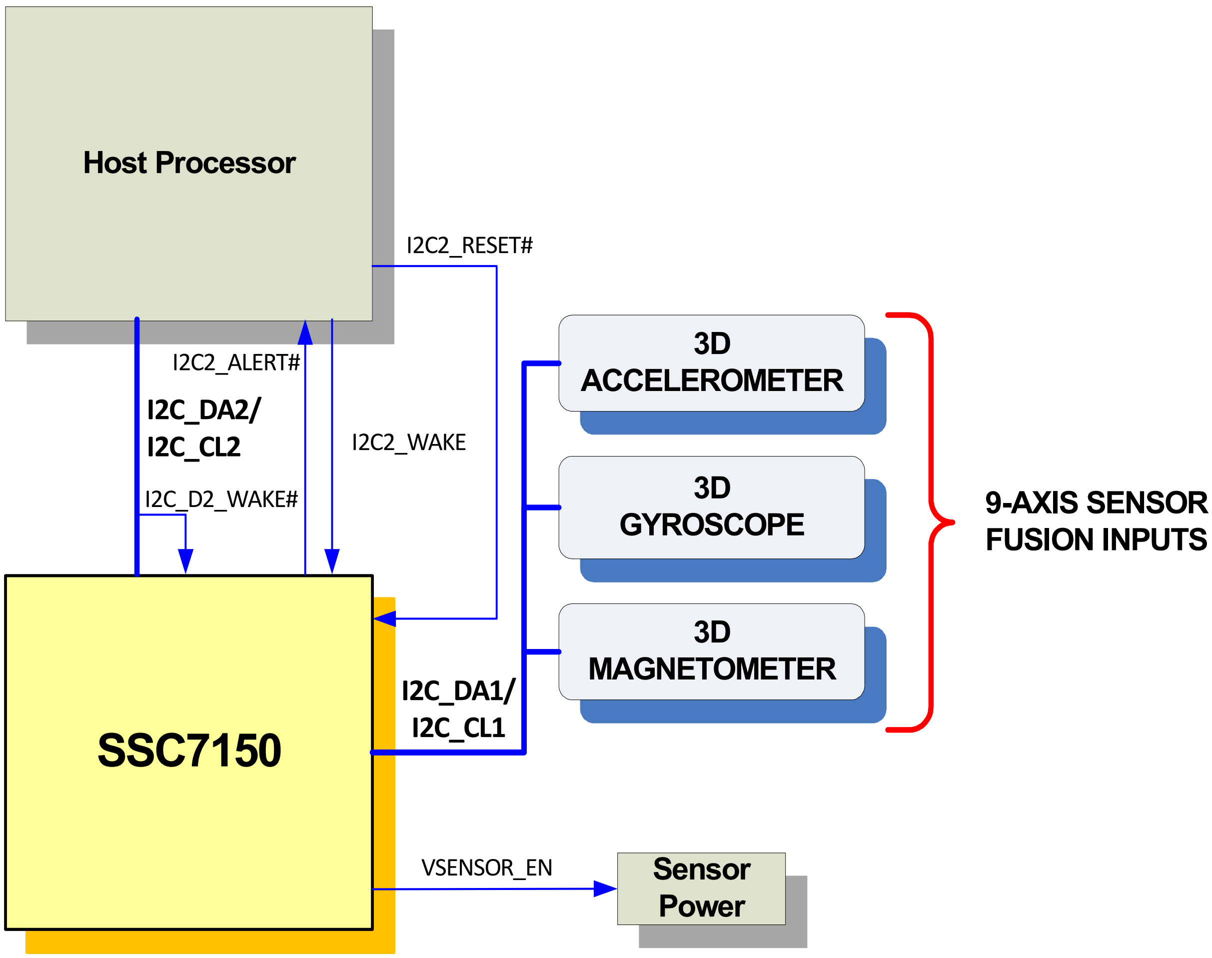
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A

2.0 SYSTEM BLOCK DIAGRAM

The SSC7150 system block diagram is shown in Figure 2-1.

FIGURE 2-1: SSC7150 SYSTEM BLOCK DIAGRAM



3.0 GUIDELINES FOR GETTING STARTED

3.1 Basic Connection Requirements

Getting started with the SSC7150 requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see **Section 3.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins, even if the ADC module is not used (see **Section 3.2 "Decoupling Capacitors"**). Note that there is no ADC support in this device. See Note below.
- VCAP pin (see **Section 3.3 "Capacitor on Internal Voltage Regulator (Vcap)"**)
- MCLR# pin (see **Section 3.4 "Master Clear (MCLR#) Pin"**)

Note:	The AVDD and AVSS pins must be connected, regardless of ADC use and the ADC voltage reference source.

Refer to the following schematic for connection information:

SSC7150 Sensor Hub Module, Assy. 6753, Schematic Revision 1.4.

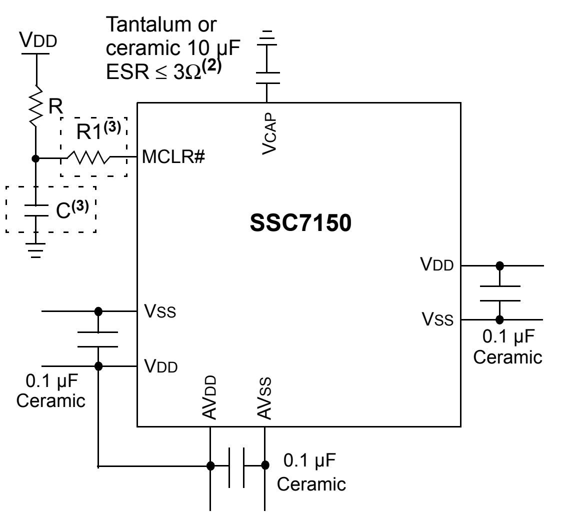
3.2 Decoupling Capacitors

The use of decoupling capacitors on power supply pins, such as VDD, VSS, AVDD and AVSS is required. See Figure 3-1.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A value of 0.1 µF (100 nF), 10-20V is recommended. The capacitor should be a low Equivalent Series Resistance (low-ESR) capacitor and have resonance frequency in the range of 20 MHz and higher. It is further recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended that the capacitors be placed on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high frequency noise:** If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing PCB track inductance.

FIGURE 3-1: RECOMMENDED MINIMUM CONNECTION



Note 1: Aluminum or electrolytic capacitors should not be used. ESR ≤ 3W from -40°C to 125°C @ SYSCLK frequency (i.e., MIPS)

2: Recommended components. See Figure 3-2.

3.2.1 BULK CAPACITORS

The use of a bulk capacitor is recommended to improve power supply stability. Typical values range from 4.7 µF to 47 µF. This capacitor should be located as close to the device as possible.

3.3 Capacitor on Internal Voltage Regulator (VCAP)

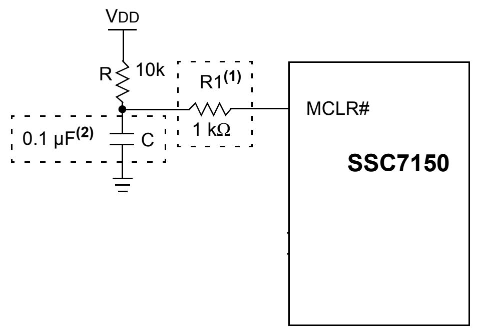
3.3.1 INTERNAL REGULATOR MODE

A low-ESR (1 Ohm) capacitor is required on the VCAP pin, which is used to stabilize the internal voltage regulator output. The VCAP pin must not be connected to VDD, and must have a CEFC capacitor, with at least a 6V rating, connected to ground. The type can be ceramic or tantalum. Refer to **Section 4.0 “Electrical Characteristics”** for additional information on CEFC specifications.

3.4 Master Clear (MCLR#) Pin

The MCLR# pin is the Device Reset pin. Pulling the MCLR# pin low generates a device Reset. Figure 3-2 illustrates a typical MCLR# circuit.

FIGURE 3-2: MCLR# PIN CONNECTIONS



Recommended Components:

Note 1: 470Ω ≤ R1 ≤ 1Ω will limit any current flowing into MCLR# from the external capacitor C, in the event of MCLR# pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

2: The capacitor can be sized to prevent unintentional Resets from brief glitches or to extend the device Reset period during POR.

4.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the SSC7150 electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the SSC7150 devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings

(See Note 1)

Ambient temperature under bias ....-40°C to +85°C

Storage temperature .... -65°C to +150°C

Voltage on V_{DD} with respect to V_{SS} .... -0.3V to +4.0V

Voltage on any pin that is not 5V tolerant, with respect to V_{SS} **(Note 3)**...................................... - 0.3V to (V_{DD} + 0.3V)

Voltage on any 5V tolerant pin with respect to V_{SS} when $V_{DD} \geq 2.3V$ **(Note 3)**...................................... - 0.3V to +5.5V

Voltage on any 5V tolerant pin with respect to V_{SS} when $V_{DD} < 2.3V$ **(Note 3)**...................................... - 0.3V to +3.6V

Maximum current out of V_{SS} pin(s) ....300 mA

Maximum current into V_{DD} pin(s) **(Note 2)**... 300 mA

Maximum output current sunk by any I/O pin..15 mA

Maximum output current sourced by any I/O pin...15 mA

Maximum current sunk by all ports..200 mA

Maximum current sourced by all ports **(Note 2)** ....200 mA

Note 1: Stresses above those listed under **"Absolute Maximum Ratings"** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 4-1).

3: See the **"Pin List"** section for the 5V tolerant pins.

4.1 DC Characteristics

TABLE 4-1: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Typical	Max.	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	T_J	-40	—	+125	°C
Operating Ambient Temperature Range	T_A	-40	—	+85	°C
Power Dissipation: Internal Chip Power Dissipation: $P_{INT} = V_{DD} \times (I_{DD} - \Sigma I_{OH})$ I/O Pin Power Dissipation: $I/O = \Sigma (\{V_{DD} - V_{OH}\} \times I_{OH}) + \Sigma (V_{OL} \times I_{OL})$	P_D	$P_{INT} + P_{I/O}$			W
Maximum Allowed Power Dissipation	P_{DMAX}	$(T_J - T_A)/\theta_{JA}$			W

TABLE 4-2: THERMAL PACKAGING CHARACTERISTICS

Characteristics	Symbol	Typical	Max.	Unit	Notes
Package Thermal Resistance, 28-pin QFN	θ_{JA}	35	—	°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-JA (θ_{JA}) numbers are achieved by package simulations.

TABLE 4-3: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			**Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ T_A ≤ +85°C				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Operating Voltage							
DC10	V_{DD}	Supply Voltage **(Note 2)**	2.3	—	3.6	V	—
DC12	V_{DR}	RAM Data Retention Voltage **(Note 1)**	1.75	—	—	V	—
DC16	V_{POR}	**V_{DD} Start Voltage** to Ensure Internal Power-on Reset Signal	1.75	—	2.1	V	—
DC17	S_{VDD}	**V_{DD} Rise Rate** to Ensure Internal Power-on Reset Signal	0.00005	—	0.115	V/µs	—

Note 1: This is the limit to which V_{DD} can be lowered without losing RAM data.

2: Overall functional device operation at $V_{BORMIN} < V_{DD} < V_{DDMIN}$ is tested, but not characterized. Refer to parameter BO10 in Table 4-7 for BOR values.

TABLE 4-4: DC CHARACTERISTICS: OPERATING/POWER-DOWN CURRENT

DC CHARACTERISTICS				**Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ T_A ≤ +85°C	
Parameter No.	**Symbol**	**Typical (3)**	**Max.**	**Units**	**Conditions**
Operating/Power-Down Current **(Note 1, 2)**					
DC20	I_{PEAK}	19.5	20.0	mA	—
DC30	I_{ACTIVE}	7.65	7.90	mA	—
DC40	I_{IDLE}	1.77	1.95	mA	—
DC50	I_{PD}	70	150	μA	—

Note 1: A device's supply current is mainly a function of the operating voltage and frequency, as well as temperature.

2: The current measurements are as follows:

- Peak current (I_{PEAK}):
  This is the peak active current value when a sensor is actively providing environmental changes.
- Active current (I_{ACTIVE}):
  This is the average operating current value when a sensor is actively providing environmental changes.
- Idle current (I_{IDLE}):
  This is the average idle current value when no sensor is actively providing environmental changes (and the device is not in power-down mode).
- Power-Down current (I_{PD}):
  This is the current value when the device is in power-down mode. This is the state entered when the Host issues the SET_POWER (Sleep) Command.
  Wakeup from power-down mode requires the I2C2_WAKE pin.

3: Data in "Typical" column is at 3.3V, 25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 4-5: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature-40°C ≤ TA ≤ +85°C				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical (1)**	**Max.**	**Units**	**Conditions**
	VIL	Input Low Voltage					
DI10		I/O Pins	VSS	—	0.2 VDD	V	
DI18		I2C_DAx, I2C_CLx	VSS	—	0.3 VDD	V	I^2C disabled **(Note 4)**
DI19		I2C_DAx, I2C_CLx	VSS	—	0.8	V	I^2C enabled **(Note 4)**
	VIH	Input High Voltage					
DI20		I/O Pins not 5V-tolerant (5)	0.65 VDD	—	VDD	V	**(Note 4,6)**
		I/O Pins 5V-tolerant (5)	0.65 VDD	—	5.5	V	
DI28		I2C_DAx, I2C_CLx	0.65 VDD	—	5.5	V	I^2C disabled **(Note 4,6)**
DI29		I2C_DAx, I2C_CLx	2.1	—	5.5	V	I^2C enabled, 2.3V ≤ VPIN ≤ 5.5 **(Note 4,6)**
	IIL	Input Leakage Current **(Note 3)**					
DI50		I/O Ports	—	—	±1	µA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
DI55		MCLR#(2)	—	—	±1	µA	VSS ≤ VPIN ≤ VDD

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The leakage current on the MCLR# pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: This parameter is characterized, but not tested in manufacturing.

5: See the **"Pin List"** section for the 5V-tolerant pins.

6: The VIH specifications are only in relation to externally applied inputs, and not with respect to the user-selectable internal pull-ups. External open drain input signals utilizing the internal pull-ups of the device are provided to be recognized only as a logic "high" internally to the device. For External "input" logic inputs that require a pull-up source, to ensure the minimum VIH of those components, it is recommended to use an external pull-up resistor rather than the internal pull-ups of the device.

TABLE 4-6: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			**Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C				
Param.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
DO10	Vol	Output Low Voltage I/O Pins	—	—	0.4	V	IOL ≤ 10 mA, VDD = 3.3V
DO20	VOH	Output High Voltage I/O Pins	1.5 (1)	—	—	V	IOH ≥ -14 mA, VDD = 3.3V
			2.0 (1)	—	—		IOH ≥ -12 mA, VDD = 3.3V
			2.4	—	—		IOH ≥ -10 mA, VDD = 3.3V
			3.0 (1)	—	—		IOH ≥ -7 mA, VDD = 3.3V

Note 1: Parameters are characterized, but not tested.

TABLE 4-7: ELECTRICAL CHARACTERISTICS: BROWN-OUT RESET (BOR)

DC CHARACTERISTICS			**Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C				
Param. No.	**Symbol**	**Characteristics**	**Min.(1)**	**Typical**	**Max.**	**Units**	**Conditions**
BO10	Vbor	BOR Event on VDD transition high-to-low(2)	2.0	—	2.3	V	—

Note 1: Parameters are for design guidance only and are not tested in manufacturing.
2: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized.

TABLE 4-8: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

DC CHARACTERISTICS			**Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Comments**
D321	Cefc	External Filter Capacitor Value	8	10	—	µF	Capacitor must be low series resistance (1 ohm). Typical voltage on the VCAP pin is 1.8V.

4.2 AC Characteristics and Timing Parameters

The information contained in this section defines SSC7150 AC characteristics and timing parameters.

FIGURE 4-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

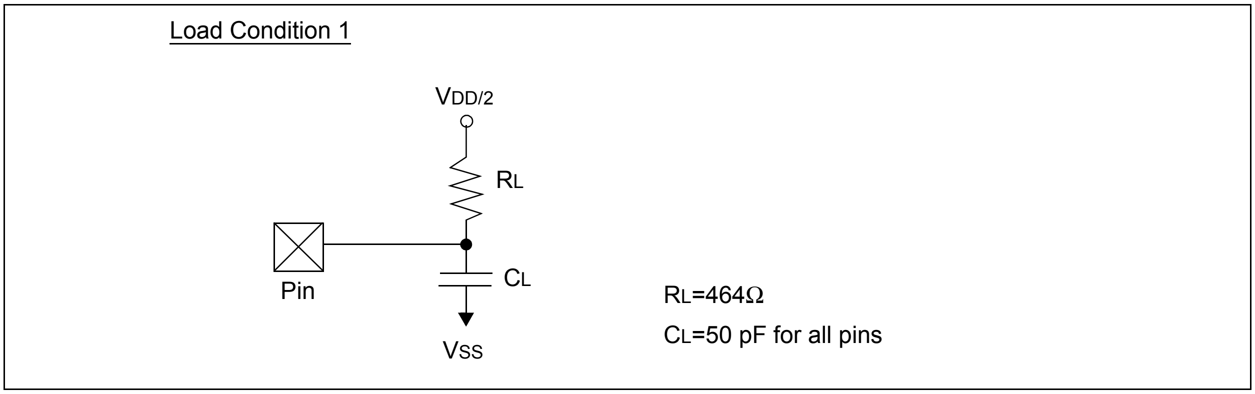
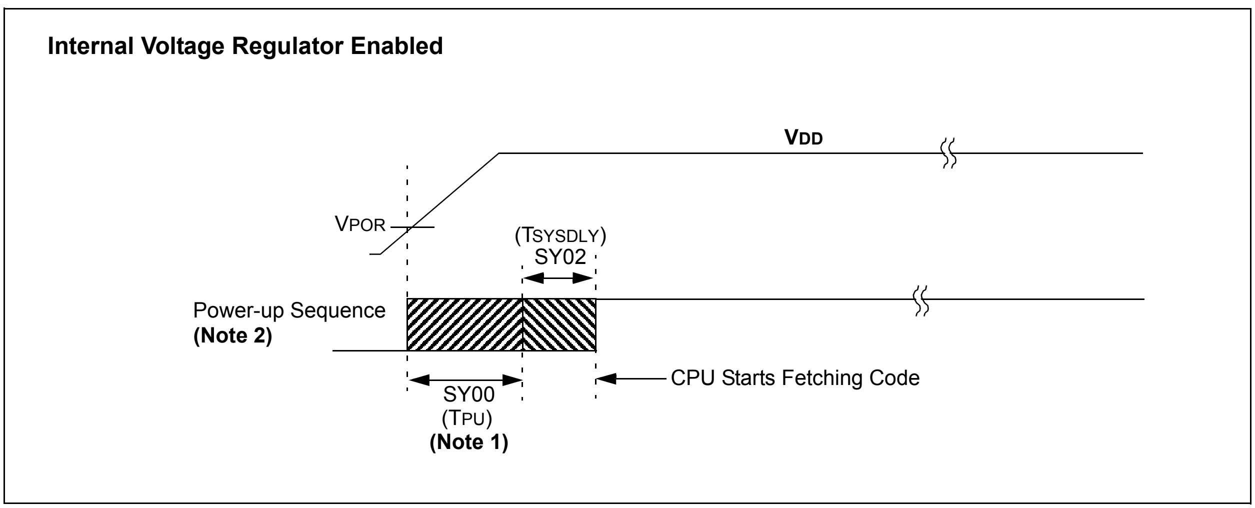


TABLE 4-9: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +85°C				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical (1)**	**Max.**	**Units**	**Conditions**
DO56	C_{IO}	All I/O pins	—	—	50	pF	
DO58	C_B	I2C_DAx, I2C_CLx	—	—	400	pF	In I^2C™ mode

Note 1: Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 4-2: POWER-ON RESET TIMING CHARACTERISTICS



Note 1: The power-up period will be extended if the power-up sequence completes before the device exits from BOR (V_{DD} < V_{DDMIN}).

2: Includes interval voltage regulator stabilization delay.

FIGURE 4-3: EXTERNAL RESET TIMING CHARACTERISTICS

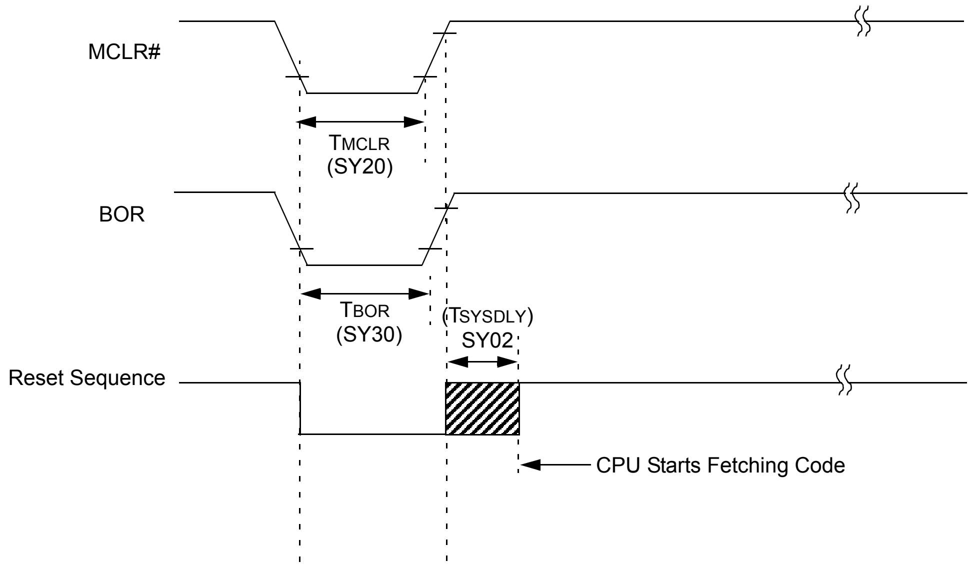


TABLE 4-10: RESET TIMING

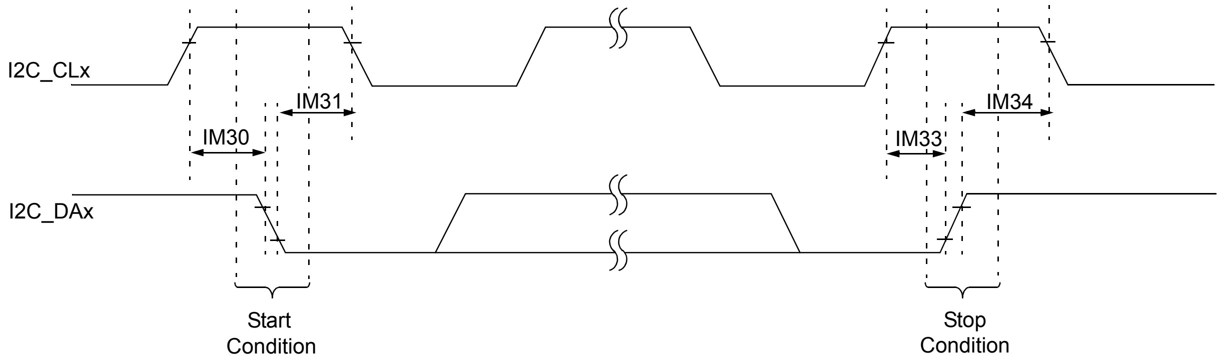
AC CHARACTERISTICS			**Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C				
Param. No.	**Symbol**	**Characteristics (1)**	**Min.**	**Typical (2)**	**Max.**	**Units**	**Conditions**
SY00	TPU	Power-up Period Internal Voltage Regulator Enabled	—	400	600	µs	—
SY02	Tsysdly	System Delay Period: Time Required to Reload Device Configuration Fuses plus SYSCLK(3) Delay before First instruction is Fetched.	—	1 µs + 8 SYSCLK cycles	—	—	—
SY20	Tmclr	MCLR# Pulse Width (low)	2	—	—	µs	—
SY30	TBOR	BOR Pulse Width (low)	—	1	—	µs	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in “Typ” column is at 3.3V, 25°C unless otherwise stated. Characterized by design but not tested.

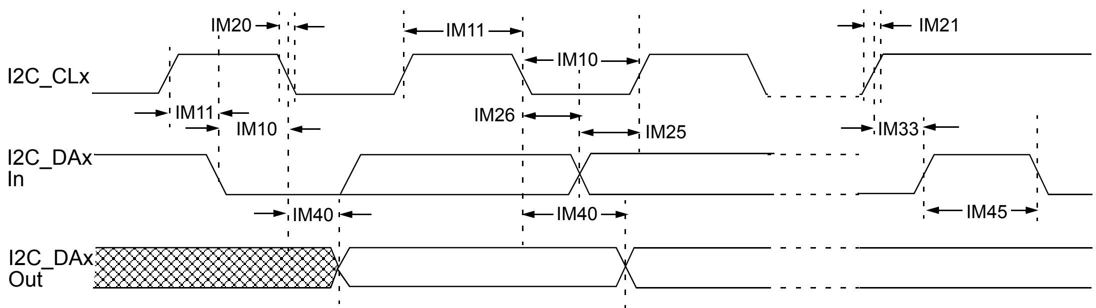
3: SYSCLK is 48MHz

FIGURE 4-4: I^2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)



Note: Refer to Figure 4-1 for load conditions.

FIGURE 4-5: I^2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)



Note: Refer to Figure 4-1 for load conditions.

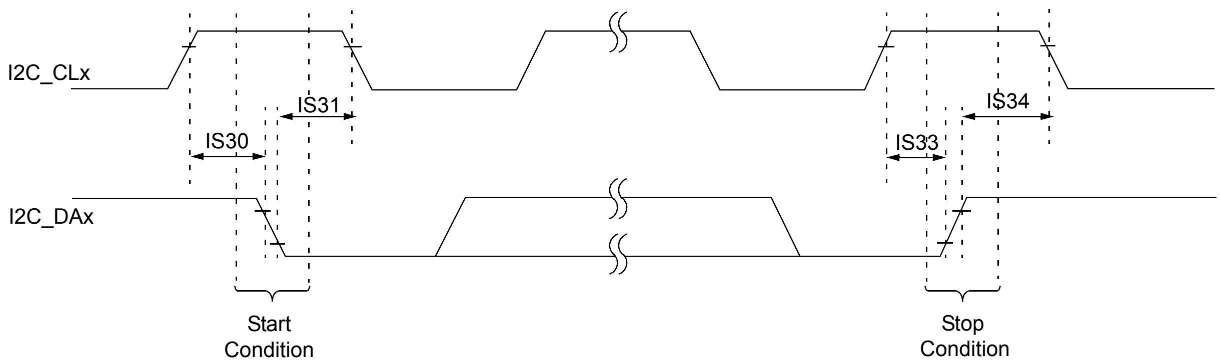
TABLE 4-11: I²C BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHARACTERISTICS				**Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C			
Param. No.	**Symbol**	**Characteristics**		**Min.(1)**	**Max.**	**Units**	**Conditions**
IM10	TLO:SCL	Clock Low Time	100 kHz mode	TPB * (BRG + 2)	—	µs	—
			400 kHz mode	TPB * (BRG + 2)	—	µs	
IM11	THI:SCL	Clock High Time	100 kHz mode	TPB * (BRG + 2)	—	µs	—
			400 kHz mode	TPB * (BRG + 2)	—	µs	
IM20	TF:SCL	I2C_DAx and I2C_CLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
IM21	TR:SCL	I2C_DAx and I2C_CLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	—
			400 kHz mode	100	—	ns	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	µs	—
			400 kHz mode	0	0.9	µs	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	TPB * (BRG + 2)	—	µs	Only relevant for Repeated Start condition
			400 kHz mode	TPB * (BRG + 2)	—	µs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	TPB * (BRG + 2)	—	µs	After this period, the first clock pulse is generated
			400 kHz mode	TPB * (BRG + 2)	—	µs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	TPB * (BRG + 2)	—	µs	—
			400 kHz mode	TPB * (BRG + 2)	—	µs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	TPB * (BRG + 2)	—	ns	—
			400 kHz mode	TPB * (BRG + 2)	—	ns	
IM40	TAA:SCL	Output Valid from Clock	100 kHz mode	—	3500	ns	—
			400 kHz mode	—	1000	ns	
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	µs	The amount of time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
IM50	CB	Bus Capacitive Loading		—	400	pF	—
IM51	TPGD	Pulse Gobbler Delay		52	312	ns	See **Note 2**

Note 1: BRG is the value of the I²C™ Baud Rate Generator.

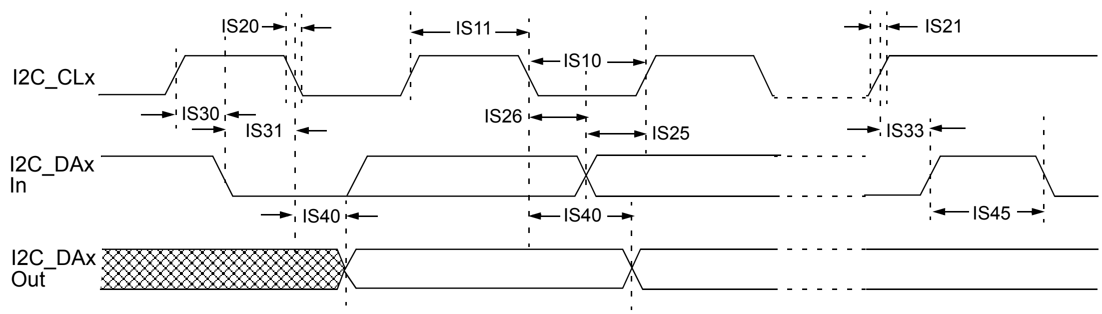
2: The typical value for this parameter is 104 ns.

FIGURE 4-6: I^2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)



Note: Refer to Figure 4-1 for load conditions.

FIGURE 4-7: I^2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)



Note: Refer to Figure 4-1 for load conditions.

TABLE 4-12: I²Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +85°C			
Param. No.	**Symbol**	**Characteristics**		**Min.**	**Max.**	**Units**	**Conditions**
IS10	$T_{LO:SCL}$	Clock Low Time	100 kHz mode	4.7	—	µs	—
			400 kHz mode	1.3	—	µs	—
IS11	$T_{HI:SCL}$	Clock High Time	100 kHz mode	4.0	—	µs	—
			400 kHz mode	0.6	—	µs	—
IS20	$T_{F:SCL}$	I2C_DAx and I2C_CLx Fall Time	100 kHz mode	—	300	ns	C_B is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 C_B	300	ns	
IS21	$T_{R:SCL}$	I2C_DAx and I2C_CLx Rise Time	100 kHz mode	—	1000	ns	C_B is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 C_B	300	ns	
IS25	$T_{SU:DAT}$	Data Input Setup Time	100 kHz mode	250	—	ns	—
			400 kHz mode	100	—	ns	
IS26	$T_{HD:DAT}$	Data Input Hold Time	100 kHz mode	0	—	ns	—
			400 kHz mode	0	0.9	µs	
IS30	$T_{SU:STA}$	Start Condition Setup Time	100 kHz mode	4700	—	ns	Only relevant for Repeated Start condition
			400 kHz mode	600	—	ns	
IS31	$T_{HD:STA}$	Start Condition Hold Time	100 kHz mode	4000	—	ns	After this period, the first clock pulse is generated
			400 kHz mode	600	—	ns	
IS33	$T_{SU:STO}$	Stop Condition Setup Time	100 kHz mode	4000	—	ns	—
			400 kHz mode	600	—	ns	
IS34	$T_{HD:STO}$	Stop Condition Hold Time	100 kHz mode	4000	—	ns	—
			400 kHz mode	600	—	ns	
IS40	$T_{AA:SCL}$	Output Valid from Clock	100 kHz mode	0	3500	ns	—
			400 kHz mode	0	1000	ns	
IS45	$T_{BF:SDA}$	Bus Free Time	100 kHz mode	4.7	—	µs	The amount of time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
IS50	C_B	Bus Capacitive Loading		—	400	pF	—

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00001885A (01-30-15)	Document Release	

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Device:	SSC7150 (1)		
Package:	ML	=	28 pin QFN (2)
Sensor Fusion Firmware:	AB0	=	Bosch 9-axis Sensor Fusion
Tape and Reel Option:	Blank	=	Tray packaging
	TR	=	Tape and Reel (3)

Example:

SSC7150-ML-AB0 = 28-QFN, Bosch 9-axis sensor fusion.

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