

FEATURES

- 700MHz min. shift frequency
- Extended 100E VEE range of -4.2V to -5.5V
- 8 bits wide
- Bi-directional
- Four selectable modes for full functionality
- Asynchronous Master Reset
- Fully compatible with industry standard 10KH, 100K ECL levels
- Internal 75KΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E141
- Pin-compatible with E241
- Available in 28-pin PLCC package

DESCRIPTION

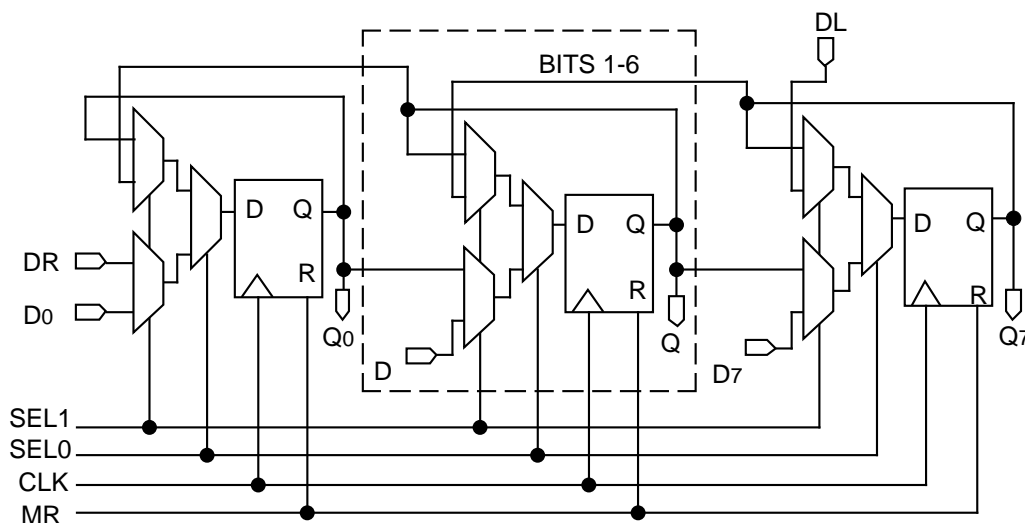
The SY10/100E141 are 8-bit, full-function shift registers designed for use in new, high-performance ECL systems. The E141 performs serial/parallel in and serial/parallel out, shifting in either direction. The eight inputs D₀-D₇ accept parallel input data, while DL/DR accept serial input data for left/right shifting.

The two select pins, SEL₀ and SEL₁ permit four modes of operation: Load, Hold, Shift Left and Shift Right, as shown in the Truth Table. Input data is clocked into the register on the rising clock edge after meeting the minimum set-up time. A logic HIGH on the Master Reset (MR) pin asynchronously resets all the registers to zero.

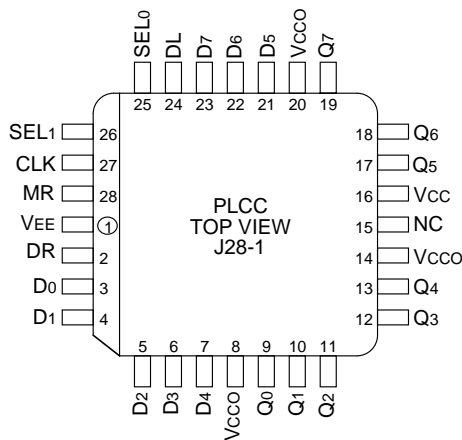
PIN NAMES

Pin	Function
D ₀ -D ₇	Parallel Data Inputs
DL, DR	Serial Data Inputs
SEL ₀ , SEL ₁	Mode Select Inputs
CLK	Clock
Q ₀ -Q ₇	Data Outputs
MR	Master Reset
V _{CC0}	Vcc to Output

BLOCK DIAGRAM



PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10E141JC	J28-1	Commercial	SY10E141JC	Sn-Pb
SY10E141JCTR ⁽²⁾	J28-1	Commercial	SY10E141JC	Sn-Pb
SY100E141JC	J28-1	Commercial	SY100E141JC	Sn-Pb
SY100E141JCTR ⁽²⁾	J28-1	Commercial	SY100E141JC	Sn-Pb
SY10E141JY ⁽³⁾	J28-1	Industrial	SY10E141JY with Pb-Free bar-line indicator	Matte-Sn
SY10E141JYTR ^(2, 3)	J28-1	Industrial	SY10E141JY with Pb-Free bar-line indicator	Matte-Sn
SY100E141JY ⁽³⁾	J28-1	Industrial	SY100E141JY with Pb-Free bar-line indicator	Matte-Sn
SY100E141JYTR ^(2, 3)	J28-1	Industrial	SY100E141JY with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

TRUTH TABLE

Function	DL	DR	SEL ₀	SEL ₁	MR	CLK	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇
Load	X	X	L	L	L	Z	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇
Shift Right	X	L	L	H	L	Z	L	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆
	X	H	L	H	L	Z	H	L	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅
Shift Left	L	X	H	L	L	Z	L	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	L
	H	X	H	L	L	Z	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	L	H
Hold	X	X	H	H	L	Z	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	L	H
	X	X	H	H	L	Z	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	L	H
Reset	X	X	X	X	H	X	L	L	L	L	L	L	L	L

DC ELECTRICAL CHARACTERISTICSV_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I _{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA	—
I _{EE}	Power Supply Current	—	—	—	—	—	—	—	—	—	mA	—
	10E	—	131	157	—	131	157	—	131	157		
	100E	—	131	157	—	131	157	—	151	181		

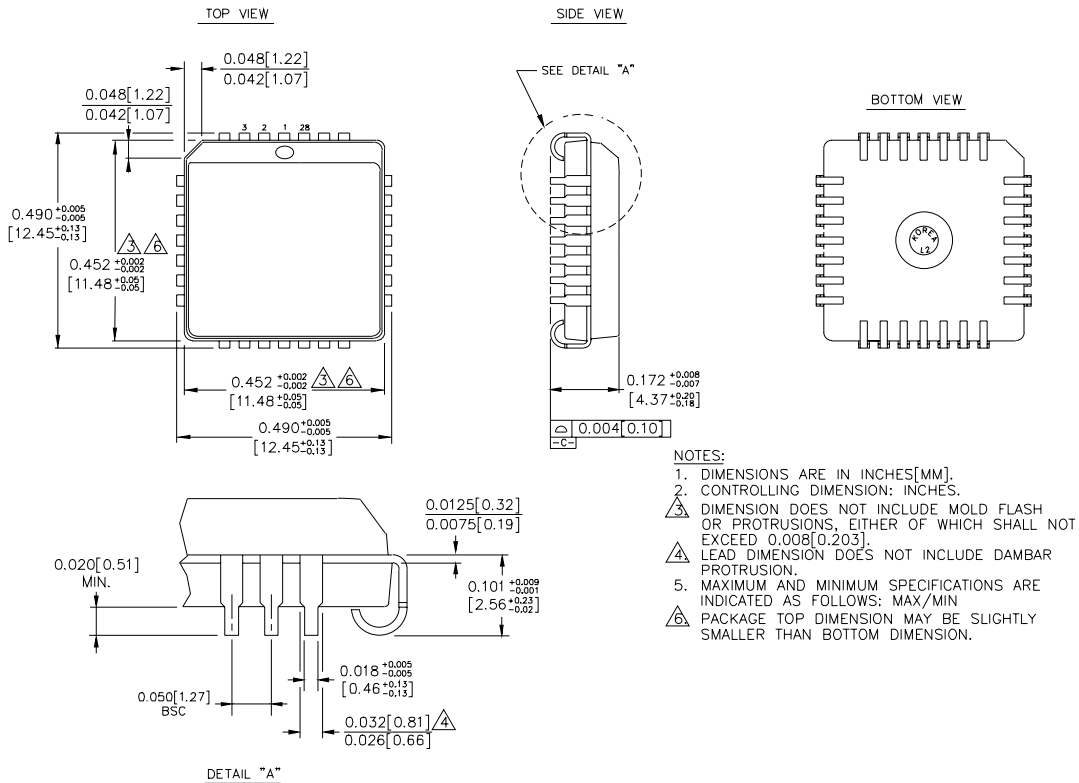
AC ELECTRICAL CHARACTERISTICSV_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f _{SHIFT}	Max. Shift Frequency	700	900	—	700	900	—	700	900	—	MHz	—
t _{PD}	Propagation Delay to Output CLK MR	625	750	975	625	750	975	625	750	975	ps	—
		600	725	975	600	725	975	600	725	975		
t _s	Set-up Time	—	—	—	—	—	—	—	—	—	ps	—
	D	175	25	—	175	25	—	175	25	—		
	SEL ₀	350	200	—	350	200	—	350	200	—		
t _H	Hold Time	—	—	—	—	—	—	—	—	—	ps	—
	D	200	-25	—	200	-25	—	200	-25	—		
	SEL ₀	100	-200	—	100	-200	—	100	-200	—		
t _{RR}	Reset Recovery Time	900	700	—	900	700	—	900	700	—	ps	—
		—	—	—	—	—	—	—	—	—		
t _{PW}	Minimum Pulse Width CLK, MR	400	—	—	400	—	—	400	—	—	ps	—
t _{skew}	Within-Device Skew	—	60	—	—	60	—	—	60	—	ps	1
t _r	Rise/Fall Time	300	525	800	300	525	800	300	525	800	ps	—
t _f	20% to 80%	—	—	—	—	—	—	—	—	—		

Note:

1. Within-device skew is defined as identical transitions on similar paths through a device.

28-PIN PLCC (J28-1)



Rev. 03

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