SY100S834L

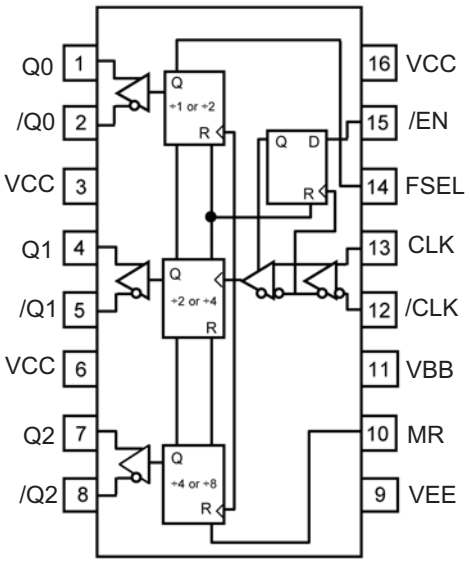
3.3V ÷2, ÷4, ÷8 Clock Generation Chip

Features

- 3.3V Power Supply
- 50 ps Output to Output Skew
- Synchronous Enable/Disable
- Master Reset for Synchronization
- Internal 75 kΩ Input Pull Down Resistors
- Available in 16-Pin SOIC Package

Package Type

SY100S834L
16-Lead Narrow SOIC (Z16-2)



General Description

The SY100S834L is a low skew ÷2, ÷4, ÷8 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other; therefore, the common output edges are all precisely aligned. The devices can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. In addition, by using the VBB output, a sinusoidal source can be AC-coupled into the device. If a single-ended input is to be used, the VBB output should be connected to the input and bypassed to ground via a 0.01 µF capacitor. The VBB output is designed to act as the switching reference for the input of the SY100S834L under single-ended input conditions. As a result, this pin can only source/sink up to 0.5 mA of current.

The Function Select (FSEL) input is used to determine what clock generation chip function is. When FSEL input is LOW, SY100S834L functions as a divide by 2, by 4 and by 8 clock generation chip. However, if FSEL input is HIGH, it functions as a divide by 1, by 2 and by 4 clock generation chip. This latter feature will increase the clock frequency by two folds.

The common enable (/EN) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the low state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock; therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon start-up, the internal flip-flops will attain a random state; the master reset (MR) input allows for the synchronization of the internal dividers, as well as for multiple SY100S834Ls in a system.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

PECL Power Supply Voltage (V_{CC}) (Note 1) ..... +8V
NECL Power Supply Voltage (V_{EE}) (Note 2) ..... –8V
PECL Mode Input Voltage (V_{IN}) (Note 3) ..... +6V
NECL Mode Input Voltage (V_{IN}) (Note 4) ..... –6V
Continuous Output Current (I_{OUT}) ..... 50 mA
Surge Output Current (I_{OUT}) ..... 100 mA

† Notice: Stresses above those listed under "Absolute Maximum ratings" may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: V_{EE} = 0V.
2: V_{CC} = 0V.
3: V_{EE} = 0V, $V_{IN} \le V_{CC}$.
4: V_{CC} = 0V, $V_{IN} \ge V_{EE}$.

DC ELECTRICAL CHARACTERISTICS (Note 1)

Electrical Characteristics: V_{CC} = 3.0V to 3.8V; V_{EE} = 0V or V_{EE} = –3.8V to –3.0V; V_{CC} = 0V; T_A = –40˚C to +85˚C, unless otherwise stated.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Current	I_{EE}	—	—	49	mA	T_A = –40°C to +25°C
		—	—	54		T_A = +85°C
Output High Voltage (Note 2)	V_{OH}	V_{CC} – 1.085	V_{CC} – 1.005	V_{CC} – 0.88	V	T_A = –40°C
		V_{CC} – 1.025	V_{CC} – 0.955	V_{CC} – 0.88		T_A = 0°C to +85°C
Output Low Voltage (Note 2)	V_{OL}	V_{CC} – 1.830	V_{CC} – 1.695	V_{CC} – 1.555	V	T_A = –40°C
		V_{CC} – 1.810	V_{CC} – 1.705	V_{CC} – 1.620		T_A = 0°C to +85°C
Input High Voltage (Single Ended)	V_{IH}	V_{CC} – 1.165	—	V_{CC} – 0.880	V	—
Input Low Voltage (Single Ended)	V_{IL}	V_{CC} – 1.810	—	V_{CC} – 1.475	V	—
Output Reference Voltage	V_{BB}	V_{CC} – 1.38	—	V_{CC} – 1.26	V	—
Common Mode Range (Note 3)	V_{IHCMR}	V_{CC} – 1.3	—	V_{CC} – 0.4	V	T_A = –40°C
		V_{CC} – 1.4	—	V_{CC} – 0.4		T_A = 0°C to +85°C
Input High Current	I_{IH}	—	—	150	µA	—
Input Low Current	I_{IL}	0.5	—	—	µA	V_{IN} = V_{IL} (Min)

Note 1: Devices are designed to meet the DC specifications shown in the above table after thermal equilibration has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained
2: Outputs are terminated through a 50Ω resistor to V_{CC} – 2.0V.
3: The CMR range is referenced to the most positive side of the differential input voltage. Normal operation is obtained if the high level falls within the specified range and the peak-to-peak voltage lies between 250 mV and 1V.

AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = 3.0V to 3.8V; V_{EE} = 0V or V_{CC} = 4.2V to 5.5V; V_{EE} = 0V or V_{EE} = –3.8V to –3.0V; V_{CC} = 0V or V_{EE} = –5.5V to –4.2V; V_{CC} = 0V; T_A = –40°C to +85°C, unless otherwise stated.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Maximum Toggle Frequency	f_{MAX}	800	—	—	MHz	—
Propagation Delay CLK to Q	t_{PD}	960	1100	1200	ps	—
Propagation Delay MR to Q	t_{PD}	650	800	1010	ps	—
Within-Device Skew (Note 1)	t_{SKEW}	—	—	50	ps	—
Set-Up Time (/EN-to-CLK)	t_s	400	—	—	ps	—
Hold Time (CLK-to-/EN)	t_h	200	—	—	ps	—
Input Swing (Note 2)	V_{PP}	250	—	1000	mV	—
Output Rise/Fall Time Q (20% to 80%)	t_r/t_f	275	400	525	ps	—

Note 1: Skew is measured between outputs under identical.

2: Input swing for which AC parameters are ensured.

TEMPERATURE SPECIFICATIONS

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	–40	—	+85	°C	—
Storage Temperature	T_S	–65	—	+150	°C	—
Lead Temperature	T_{LEAD}	—	—	+260	°C	Soldering, 20 sec.
Package Thermal Resistance (SOIC)						
Junction-to-Ambient	θ_{JA}	—	—	—	°C/W	—
		—	—	—		—
Junction-to-Case	θ_{JC}	—	—	—	°C/W	—

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1, 2	Q0, /Q0	Differential 2 or 1 outputs
3, 6, 16	VCC	Positive power supply
4, 5	Q1, /Q1	Differential 4 or 2 outputs
7, 8	Q2, /Q2	Differential 8 or 4 outputs
9	VEE	Negative power supply
10	MR	Master reset
11	VBB	Reference output
12, 13	CLK, /CLK	Differential clock inputs
14	FSEL	Function select, single-ended ECL logic.
15	/EN	Synchronous enable, single-ended ECL logic.

2.1 Truth Table

TABLE 2-2: TRUTH TABLE

CLK	/EN	MR	Function
Z	L	L	Divide
ZZ	H	L	Hold Q0 - Q2
X	X	H	Reset Q0 - Q2

Note: Z = Low-to-high transition.

Note: ZZ = High-to-low transition.

TABLE 2-3: FUNCTION SELECT TRUTH TABLE

FSEL	Q0 Outputs	Q1 Outputs	Q2 Outputs
L	Divide by 2	Divide by 4	Divide by 8
H	Divide by 1	Divide by 2	Divide by 4

3.0 TIMING DIAGRAM

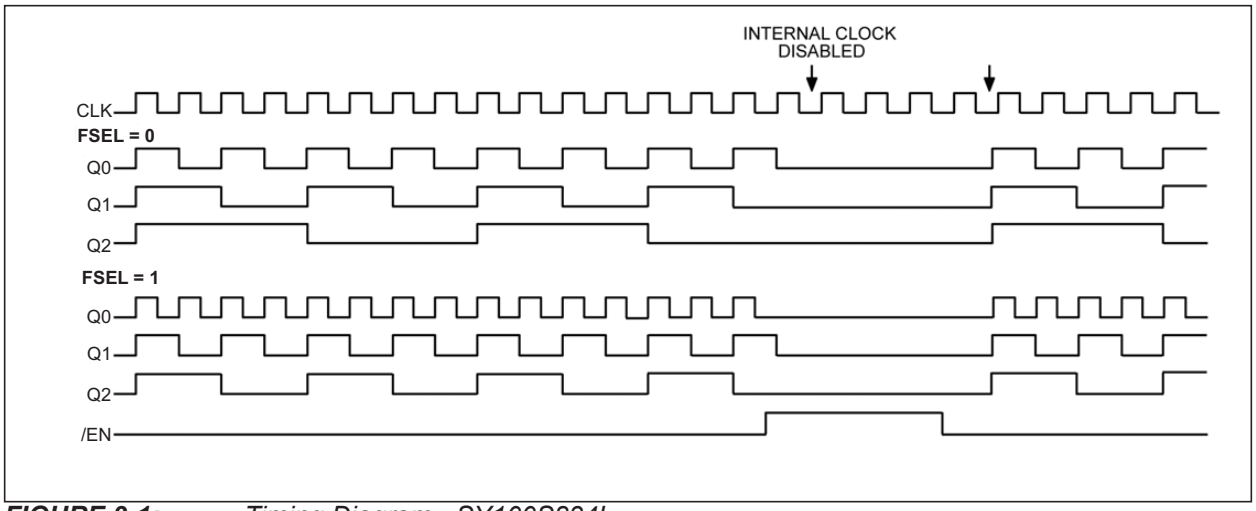


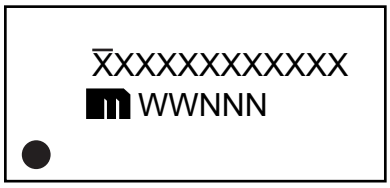
FIGURE 3-1: *Timing Diagram - SY100S834L.*

The /EN signal will freeze the internal clocks to the flip-flops on the first falling edge of CLK after its assertion. The internal dividers will maintain their state during the internal clock freeze and will return to clocking once the internal clocks are unfrozen. The outputs will transition to their next states in the same manner, time and relationship as they would have had the /EN signal not been asserted.

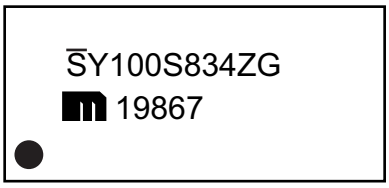
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

16-Lead SOIC*



Example

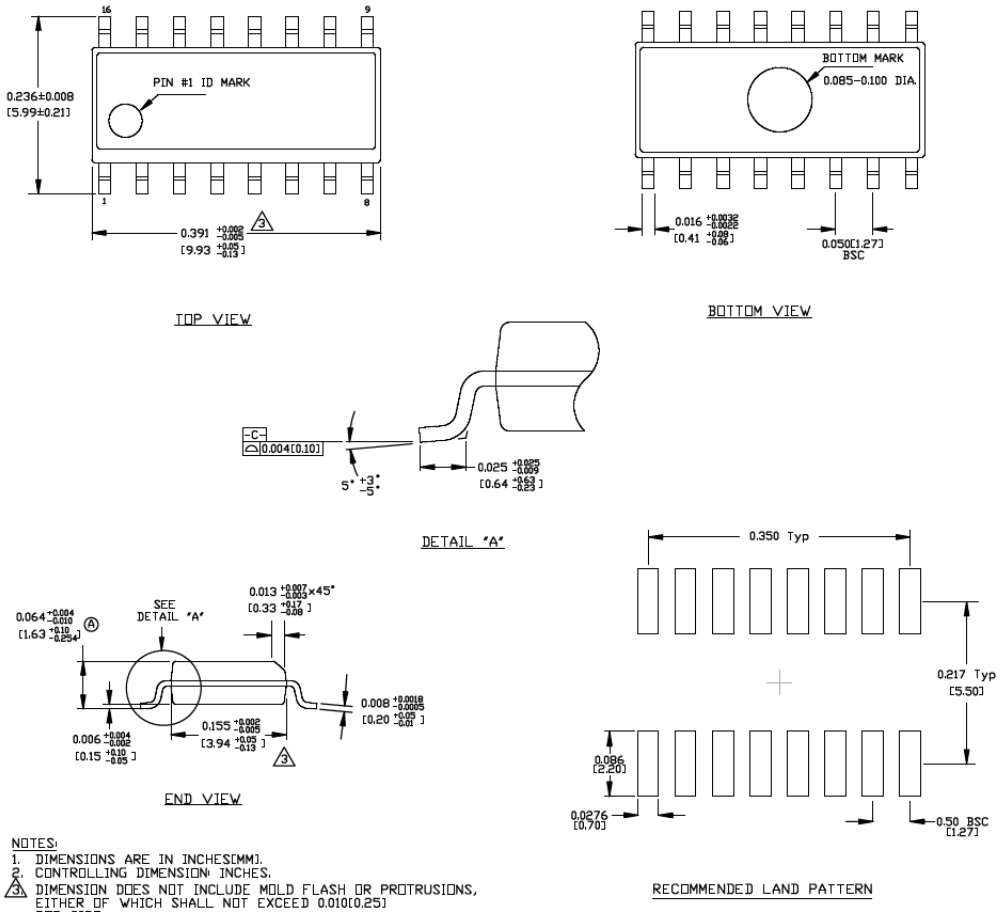


Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

TITLE

16 LEAD SOICN PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	SOICN-16LD-PL-1	**UNIT**	INCH [MM]
Lead Frame	Copper	**Lead Finish**	Matte Tin



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.010[0.25] PER SIDE.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

APPENDIX A: REVISION HISTORY

Revision A (May 2020)

- Converted Micrel document SY100S834L to Microchip data sheet DS20006353A.
- Minor text changes throughout.
- Removed all reference to the EOL SY100S834 version.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	-XX	X	X	-XX
Device	Voltage Option	Package	Temperature Range	Special Processing

Device:	SY100S834L: 3.3V ÷2, ÷4, ÷8 Clock Generation Chip		
Voltage Option:	L =	3.3V	
Package:	Z	=	16-Lead SOIC
Temperature Range:	G	=	–40˚C to +85˚C (NiPdAu Pb-Free)
Special Processing:	<blank>=		48/Tube
	TR	=	1,000/Reel

Examples:

a) SY100S834LZG: 3.3V, ÷2, ÷4, ÷8 Clock Generation Chip, 3.3V, –40˚C to +85˚C, 16-Lead SOIC, 48/Tube

b) SY100S834LZG-TR: 3.3V, ÷2, ÷4, ÷8 Clock Generation Chip, 3.3V, –40˚C to +85˚C, 16-Lead SOIC, 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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