

3.3V/5V ECL Differential AND/NAND

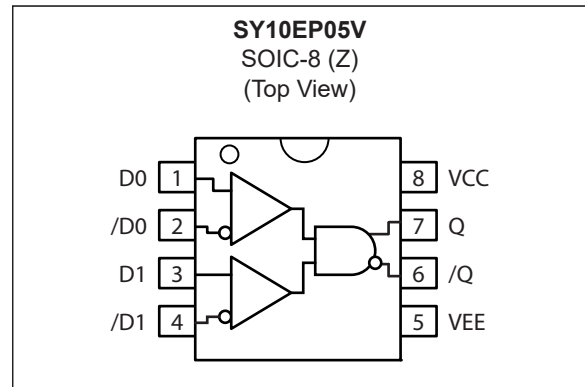
Features

- 3.3V or 5V Power Supply Options
- 180 ps Typical Propagation Delay
- Maximum Frequency: 3 GHz Typical
- Internal Input Resistors: Pull-Down on D, Pull-Down and Pull-Up on /D
- Q Output will Default Low with Inputs Open or at V_{EE}
- Transistor Count: 126
- Available in 8-Lead SOIC Package

General Description

The SY10EP05V is a 2-input differential AND/NAND gate. The device is functionally equivalent to the EL05 device. With AC performance much faster than the EL05 device, the EP05V is ideal for applications requiring the fastest AC performance available.

Package Type



SY10EP05V

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

| | |
|---|--------|
| PECL Power Supply Voltage (V_{CC}) (Note 1) | +6.0V |
| NECL Power Supply Voltage (V_{EE}) (Note 2) | -6.0V |
| PECL Mode Input Voltage (V_{IN}) (Note 3) | +6.0V |
| NECL Mode Input Voltage (V_{IN}) (Note 4) | -6.0V |
| Continuous Output Current (I_{OUT}) | 50 mA |
| Surge Output Current (I_{OUT}) | 100 mA |

† **Notice:** Stresses above those listed under “Absolute Maximum ratings” may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: $V_{EE} = 0V$.

2: $V_{CC} = 0V$.

3: $V_{EE} = 0V$, $V_{IN} \leq V_{CC}$.

4: $V_{CC} = 0V$, $V_{IN} \geq V_{EE}$.

DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{CC} = 3.0V$ to $5.5V$; $V_{EE} = 0V$ or $V_{EE} = -5.5V$ to $-3.0V$; $V_{CC} = 0V$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated, (Note 1)

| Parameter | Symbol | Min. | Typ. | Max. | Units | Condition |
|--------------------------------------|-------------|------------------|------------------|------------------|---------|------------------------|
| Power Supply Current | I_{EE} | — | 22 | 29 | mA | — |
| Output High Voltage (Note 2) | V_{OH} | $V_{CC} - 1.135$ | $V_{CC} - 1.060$ | $V_{CC} - 0.885$ | V | $T_A = -40^\circ C$ |
| | | $V_{CC} - 1.070$ | $V_{CC} - 0.945$ | $V_{CC} - 0.820$ | | $T_A = +25^\circ C$ |
| | | $V_{CC} - 1.010$ | $V_{CC} - 0.885$ | $V_{CC} - 0.760$ | | $T_A = +85^\circ C$ |
| Output Low Voltage (Note 2) | V_{OL} | $V_{CC} - 1.950$ | $V_{CC} - 1.810$ | $V_{CC} - 1.685$ | V | $T_A = -40^\circ C$ |
| | | $V_{CC} - 1.950$ | $V_{CC} - 1.745$ | $V_{CC} - 1.620$ | | $T_A = +25^\circ C$ |
| | | $V_{CC} - 1.950$ | $V_{CC} - 1.685$ | $V_{CC} - 1.560$ | | $T_A = +85^\circ C$ |
| Input High Voltage (Single-Ended) | V_{IH} | $V_{CC} - 1.210$ | — | $V_{CC} - 0.885$ | V | $T_A = -40^\circ C$ |
| | | $V_{CC} - 1.145$ | — | $V_{CC} - 0.820$ | | $T_A = +25^\circ C$ |
| | | $V_{CC} - 1.085$ | — | $V_{CC} - 0.760$ | | $T_A = +85^\circ C$ |
| Input Low Voltage (Single-Ended) | V_{IL} | $V_{CC} - 1.935$ | — | $V_{CC} - 1.610$ | V | $T_A = -40^\circ C$ |
| | | $V_{CC} - 1.870$ | — | $V_{CC} - 1.545$ | | $T_A = +25^\circ C$ |
| | | $V_{CC} - 1.810$ | — | $V_{CC} - 1.485$ | | $T_A = +85^\circ C$ |
| Common Mode Range (Note 3) | V_{IHCMR} | $V_{EE} + 2.0$ | — | V_{CC} | V | — |
| Input High Current | I_{IH} | — | — | 150 | μA | — |
| Input Low Current D | I_{IL} | 0.5 | — | — | μA | $V_{IN} = V_{IL(MIN)}$ |
| Input Low Current /D | | -150 | — | — | | |

Note 1: Devices are designed to meet the DC specifications shown in the table above after thermal equilibration has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

2: Outputs are terminated through a 50Ω resistor to $V_{CC} - 2.0V$.

3: The CMR range is referenced to the most positive side of the differential input voltage. Normal operation is obtained if the high level falls within the specified range and the peak-to-peak voltage lies between 150 mV and 1.2V.

AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{CC} = 3.0V$ to $5.5V$; $V_{EE} = 0V$ or $V_{EE} = -5.5V$ to $-3.0V$; $V_{CC} = 0V$; $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise stated. All loading with a 50Ω resistor to $V_{CC} - 2.0V$.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Conditions |
|--|--------------------------|------|------|------|-------|----------------------|
| Maximum Toggle Frequency (Note 1) | f_{MAX} | — | 3.0 | — | GHz | — |
| Propagation Delay D-to-Q (Differential) | t_{PLH} , t_{PHL} | 160 | 180 | 260 | ps | — |
| Input Voltage Swing (Differential Configuration, Note 2) | V_{PP} | 150 | 800 | 1200 | mV | — |
| Output Rise/Fall Time Q (20% to 80%) | t_r/t_f | 70 | — | 170 | ps | $T_A = -40^{\circ}C$ |
| | | 80 | 130 | 180 | | $T_A = +25^{\circ}C$ |
| | | 100 | — | 200 | | $T_A = +85^{\circ}C$ |

Note 1: Measured with 750 mV input signal, 50% duty cycle. f_{MAX} guaranteed for functionality only. V_{OL} and V_{OH} are guaranteed at DC only.

2: Input swing for which AC parameters are ensured.

TEMPERATURE SPECIFICATIONS

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|------------------------------------|---------------|------|------|------|---------------|--------------------|
| Temperature Ranges | | | | | | |
| Lead Temperature | T_{LEAD} | — | — | +260 | $^{\circ}C$ | Soldering, 20 sec. |
| Operating Temperature Range | T_A | -40 | — | +85 | $^{\circ}C$ | — |
| Storage Temperature Range | T_S | -65 | — | +150 | $^{\circ}C$ | — |
| Package Thermal Resistances | | | | | | |
| Thermal Resistance, SOIC-8Ld | θ_{JA} | — | 160 | — | $^{\circ}C/W$ | Still-Air |
| | | — | 109 | — | $^{\circ}C/W$ | 500 lfpm |
| | θ_{JC} | — | 39 | — | $^{\circ}C/W$ | — |

TRUTH TABLE

| D0 | D1 | /D0 | /D1 | Q | /Q |
|----|----|-----|-----|---|----|
| L | L | H | H | L | H |
| L | H | H | L | L | H |
| H | L | L | H | L | H |
| H | H | L | L | H | L |

SY10EP05V

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 2-1](#).

TABLE 2-1: PIN FUNCTION TABLE

| Pin Name | Pin Number | Description |
|--------------------|--------------|--------------------------|
| D0, /D0 D1, /D1 | 1, 2 3, 4 | ECL Data Inputs. |
| VEE | 5 | Negative Supply Voltage. |
| /Q, Q | 6, 7 | ECL Data Outputs. |
| VCC | 8 | Positive Supply Voltage. |

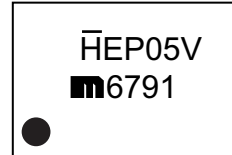
3.0 PACKAGING INFORMATION

3.1 Package Marking Information

8-Lead SOIC*



Example



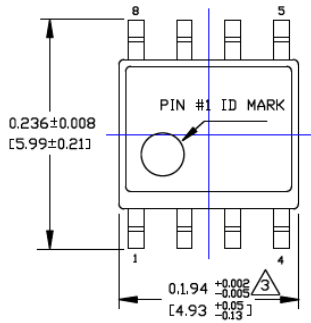
| | | |
|----------------|--|--|
| Legend: | XX...X | Product code or customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC [®] designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |
| | •, ▲, ▼ | Pin one index is identified by a dot, delta up, or delta down (triangle mark). |
| Note: | In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo. | |
| | Underbar (¯) and/or Overbar (¯) symbol may not be to scale. | |

SY10EP05V

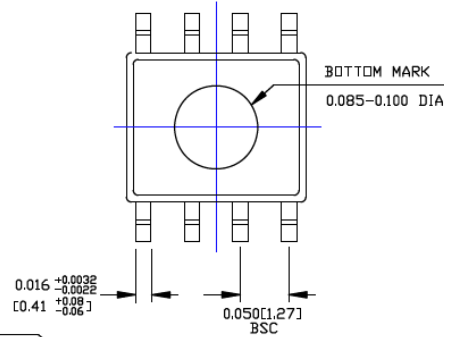
TITLE

8 LEAD SOICN PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

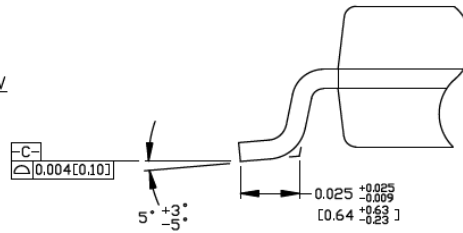
| DRAWING # | SOICN-8LD-PL-1 | UNIT | INCH [MM] |
|-----------|----------------|------|-----------|
|-----------|----------------|------|-----------|



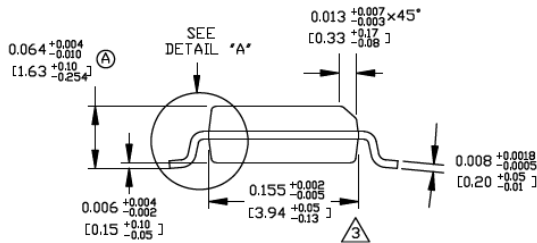
TOP VIEW



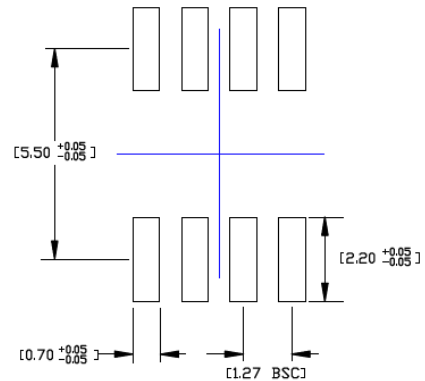
BOTTOM VIEW



DETAIL "A"



END VIEW



RECOMMENDED LAND PATTERN

NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.010[0.25] PER SIDE.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

APPENDIX A: REVISION HISTORY

Revision A (January 2020)

- Converted Micrel document SY10EP05V to Microchip data sheet DS20006252A.
- Minor text changes throughout.
- Removal of all reference to the MSOP package option for the device.

SY10EP05V

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

| <u>Part No.</u> | <u>X</u> | <u>X</u> | <u>X</u> | <u>-XX</u> |
|---------------------------|----------------|---------------------------|---------------------------------|------------|
| Device | Supply Voltage | Package | Temp. Range | Packing |
| Device: | SY10EP05: | ECL Differential AND/NAND | | |
| Supply Voltage: | V | = | 3.3V/5V | |
| Package: | Z | = | 8-Lead SOIC | |
| Temperature Range: | G | = | -40°C to +85°C (NiPdAu Pb-Free) | |
| Packing: | <blank> | = | 95/Tube | |
| | TR | = | 1,000/Reel | |

Examples:

a) SY10EP05VZG:
SY10EP05, 3.3V/5V, 8-Lead SOIC,
-40°C to +85°C Temperature Range, 95/Tube

b) SY10EP05VZG-TR:
SY10EP05, 3.3V/5V, 8-Lead SOIC,
-40°C to +85°C Temperature Range, 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

SY10EP05V

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ISBN: 978-1-5224-5517-2

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