FEATURES

- **Two independent differential 2:1 multiplexers**
- **Guaranteed AC performance over temperature and voltage:**
  - **DC-to >5Gbps data rate throughput**
  - **<310ps IN-to-Out t_{pd}**
  - **<110ps t_r / t_f**
- **Unique, patent-pending input isolation design minimizes crosstalk**
- **Ultra-low jitter design:**
  - **<1ps$_{RMS}$ random jitter**
  - **<10ps$_{PP}$ deterministic jitter**
  - **<10ps$_{PP}$ total jitter (clock)**
  - **<0.7ps$_{RMS}$ crosstalk-induced jitter**
- **Unique, patent-pending 50ý input termination and VT pin accepts DC-coupled and AC-coupled inputs (CML, LVDS, PECL)**
- **800mV LVPECL output swing**
- **Power supply 2.5V ±5% or 3.3V ±10%**
- **–40°C to +85°C temperature range**
- **Available in 32-pin (5mm ∞ 5mm) MLF® package**

APPLICATIONS

- **Data communication systems**
- **SONET applications**
- **Fibre Channel applications**
- **GigE applications**

Precision Edge®

DESCRIPTION

The SY58026U features two ultra-fast, low jitter 2:1 differential muxes with a guaranteed maximum data throughput of 5Gbps.

The SY58026U differential inputs include a unique internal termination design that allows access to the termination network through a VT pin. The device easily interfaces to different logic standards, both AC- and DC-coupled, without external resistor-bias and termination networks. The result is a clean, stub-free, low jitter interface solution. The differential 800mV LVPECL outputs have extremely fast rise/fall times guaranteed to be less than 110ps.

The SY58026U operates from a 2.5V or 3.3V supply, and is guaranteed over the full industrial temperature range (–40°C to +85°C). The SY58026U is part of Micrel's Precision Edge® product family.

All support documentation can be found on Micrel's web site at www.micrel.com.

FUNCTIONAL BLOCK DIAGRAM
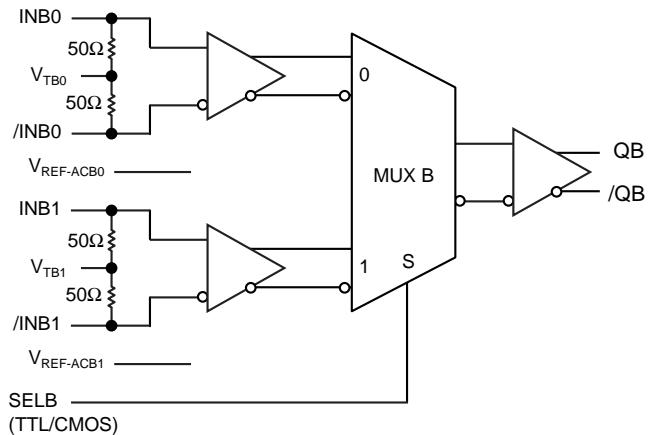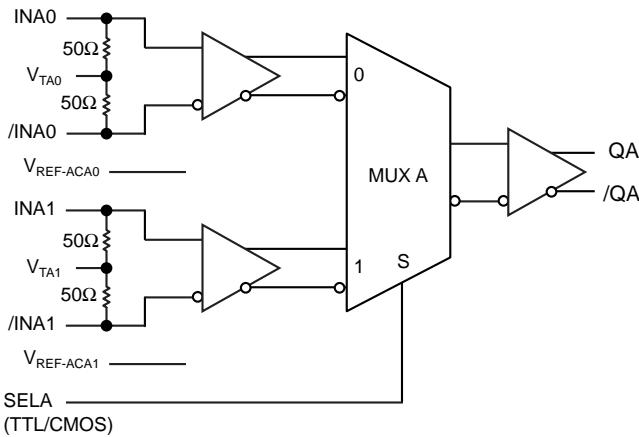
United States Patent No. RE44,134

PACKAGE/ORDERING INFORMATION
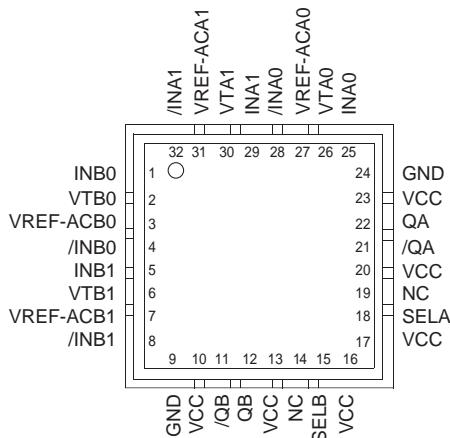
32-Pin MLF® (MLF-32)

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY58026UMI	MLF-32	Industrial	SY58026U	Sn-Pb
SY58026UMITR[2]	MLF-32	Industrial	SY58026U	Sn-Pb
SY58026UMG	MLF-32	Industrial	SY58026U with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY58026UMGTR[2]	MLF-32	Industrial	SY58026U with Pb-Free bar-line indicator	Pb-Free NiPdAu

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC electricals only.
2. Tape and Reel.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
25, 28, 29, 32, 1, 4, 5, 8	INA0, /INA0, INA1, /INA1, INB0, /INB0, INB1, /INB1	Differential Inputs: These input pairs are the differential signal inputs to the device. Inputs accept AC- or DC-coupled differential signals as small as 100mV. Each pin of a pair internally terminates to a VT pin through 50ý. Note that these inputs will default to an indeterminate state if left open. Unused differential input pairs can be terminated by connecting one input to V_{CC} and the complementary input to GND through a 1ký resistor. The VT pin is to be left open in this configuration. Please refer to the "Input Interface Applications" section for more details.
26, 30, 2, 6	VTA0 , VTA1, VTB0, VTB1	Input Termination Center-Tap: Each side of the differential input pair, terminates to a VT pin. Each VT pin provides a center-tap to a termination network for maximum interface flexibility. See "Input Interface Applications" section for more details.
18, 15	SELA, SELB	Bank A, Bank B Input Channel Select (TTL/CMOS): These TTL/CMOS-compatible inputs select the inputs to the multiplexers. These inputs are internally connected to a 25ký pull-up resistor and will default to a logic HIGH state if left open. Input switching threshold is V_{CC}/2.
27, 31, 3, 7	VREF-ACA0, VREF-ACA1, VREF-ACB0, VREF-ACB1	Reference Output Voltage: These outputs bias to V_{CC} –1.2V. Connect to VT pin when AC-coupling the data inputs. Bypass with 0.01µF low ESR capacitor to V_{CC}. Maximum current source or sink is 0.5mA. See "Input Interface Applications" section.
10, 13, 16, 17, 20, 23	VCC	Positive Power Supply: Bypass with 0.1µF™ƒ0.01µF low ESR capacitors.
22, 21, 12, 11	QA, /QA, QB, /QB	Differential 100k LVPECL Outputs: MUX A and MUX B selected LVPECL outputs. See "Output Interface Applications" section for termination. Refer to the "Truth Table" for logic operation.
9, 24	GND, Exposed pad	Ground: Ground pins and exposed pad must be connected to the same ground plane.
14, 19	NC	Not connected.

Absolute Maximum Ratings[1]

Power Supply Voltage (V_{CC}) .... −0.5V to +4.0V
Input Voltage (V_{IN}) .... −0.5V to V_{CC}
LVPECL Output Current (I_{OUT})
    Continuous 50mA
    Surge 100mA
Termination Current[3]
    Source or sink current on V_T .... ±100mA
Input Current
    Source or sink current on IN, /IN ....±50mA
Current (V_{REF-AC})
    Source or sink current on V_{REF-AC}[3] ....±1.5mA
Lead Temperature (soldering, 20 sec.) .... 260°C
Storage Temperature Range (T_S) ....−65°C to +150°C

Operating Ratings[2]

Power Supply Voltage (V_{CC}) ....+2.375V to +2.625V
.... +3.0V to +3.6V
Ambient Temperature Range (T_A) ....−40°C to +85°C
Package Thermal Resistance[4]
    MLF® (θ_{JA})
        Still-Air .... 35°C/W
    MLF® (ψ_{JB})
        Junction-to-board .... 20°C/W

DC ELECTRICAL CHARACTERISTICS[5]

T_A= −40°C to +85°C; unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply	V_{CC} = 2.5V V_{CC} = 3.3V	2.375 3.0	2.5 3.3	2.625 3.6	V V
I_{CC}	Power Supply Current	No load, max. V_{CC}.		100	130	mA
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		80	100	120	ý
R_{IN}	Input Resistance (IN-to-V_T, /IN-to-V_T)		40	50	60	ý
V_{IH}	Input High Voltage (IN, /IN)	Note 6	V_{CC} −1.6		V_{CC}	V
V_{IL}	Input Low Voltage (IN, /IN)		0		V_{IH} −0.1	V
V_{IN}	Input Voltage Swing (IN, /IN)	See Figure 1a.	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage Swing |IN − /IN|	See Figure 1b.	0.2			V
V_{T_IN}	In-to-V_T (IN, /IN)				1.28	V
V_{REF-AC}	Output Reference Voltage		V_{CC}−1.3	V_{CC}−1.2	V_{CC}−1.1	V

Notes:

1. Permanent device damage may occur if "Absolute Maximum Ratings" are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to the limited drive capability, use for input of the same package only.
4. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential (GND) on the PCB. Ψ_{JB} uses 4-layer θ_{JA} in still air unless otherwise stated.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. V_{IH} (min) not lower than 1.2V.

LVPECL OUTPUT DC ELECTRICAL CHARACTERISTICS[6]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A = –40°C to +85°C; R_L = 50ý to V_{CC} –2V, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output High Voltage Q, /Q		V_{CC}–1.145		V_{CC}–0.895	V
V_{OL}	Output Low Voltage Q, /Q		V_{CC}–1.945		V_{CC}–1.695	V
V_{OUT}	Output Voltage Swing Q, /Q	See Figure 1a.	550	800		mV
$V_{DIFF-OUT}$	Differential Output Voltage Swing Q, /Q	See Figure 1b.	1100	1600		mV

LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS[6]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A= –40°C to 85°C unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current		–175		75	µA
I_{IL}	Input LOW Current	V_{IL} = 0V	–300			µA

Note:

6. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS[7]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A= −40°C to +85°C; R_L = 50ý to V_{CC}−2V, unless otherwise stated.

Symbol	Parameter		Condition		Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency		V_{OUT} ž 400mV	NRZ Data	5			Gbps
				Clock		6		GHz
t_{pd}	Propagation Delay	IN-to-Q	V_{IN} ž 300mV		160	230	310	ps
		SEL-to-Q			100	220	400	ps
t_{SKEW}	Input-to-Input Skew (Within-bank)		**Note 8**			7	15	ps
	Bank-to-Bank Skew		**Note 9**			8	20	ps
	Part-to-Part Skew		**Note 10**				100	ps
t_{JITTER}	Data	Random Jitter (RJ)	**Note 11**				1	ps$_{RMS}$
		Deterministic Jitter (DJ)	**Note 12**				10	ps$_{PP}$
	Clock	Cycle-to-Cycle Jitter (RJ)	**Note 13**				1	ps$_{RMS}$
		Total Jitter (TJ)	**Note 14**				10	ps$_{PP}$
	Crosstalk-induced Jitter Channel-to-Channel (Within-bank)		**Note 15,** Within-bank.				0.7	ps$_{RMS}$
t_r, t_f	Output Rise/Fall Time 20% to 80%		At full swing.		35	70	110	ps

Notes:

7. High-speed AC parameters are guaranteed by design and characterization. V_{IN} swing ž 100mV unless otherwise noted.

8. Input-to-input skew is the difference in time between two inputs to the output within a bank.

9. Bank-to-bank skew is the difference in time from input to the output between bank.

10. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.

11. Random jitter is measured with a K28.7 comma detect character pattern, measured at 5Gbps and 2.5Gbps/3.2Gbps.

12. Deterministic jitter is measured at 2.5Gbps/3.2Gbps, with both K28.5 and 2^{23}–1 PRBS pattern

13. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, T_n–T_{n-1} where T is the time between rising edges of the output signal.

14. Total jitter definition: with an ideal clock input of frequency - f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

15. Crosstalk is measured at the output while applying two similar frequencies that are asynchronous with respect to each other at the inputs.

TRUTH TABLES

INA0	/INA0	INA1	/INA1	SELA	QA	/QA
0	1	X	X	0	0	1
1	0	X	X	0	1	0
X	X	0	1	1	0	1
X	X	1	0	1	1	0

INB0	/INB0	INB1	/INB1	SELB	QB	/QB
0	1	X	X	0	0	1
1	0	X	X	0	1	0
X	X	0	1	1	0	1
X	X	1	0	1	1	0

SINGLE-ENDED AND DIFFERENTIAL SWINGS
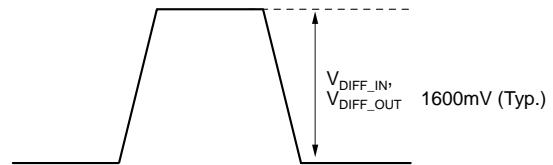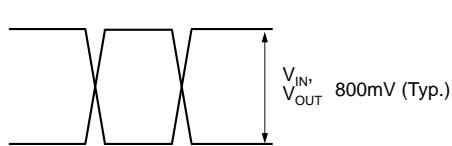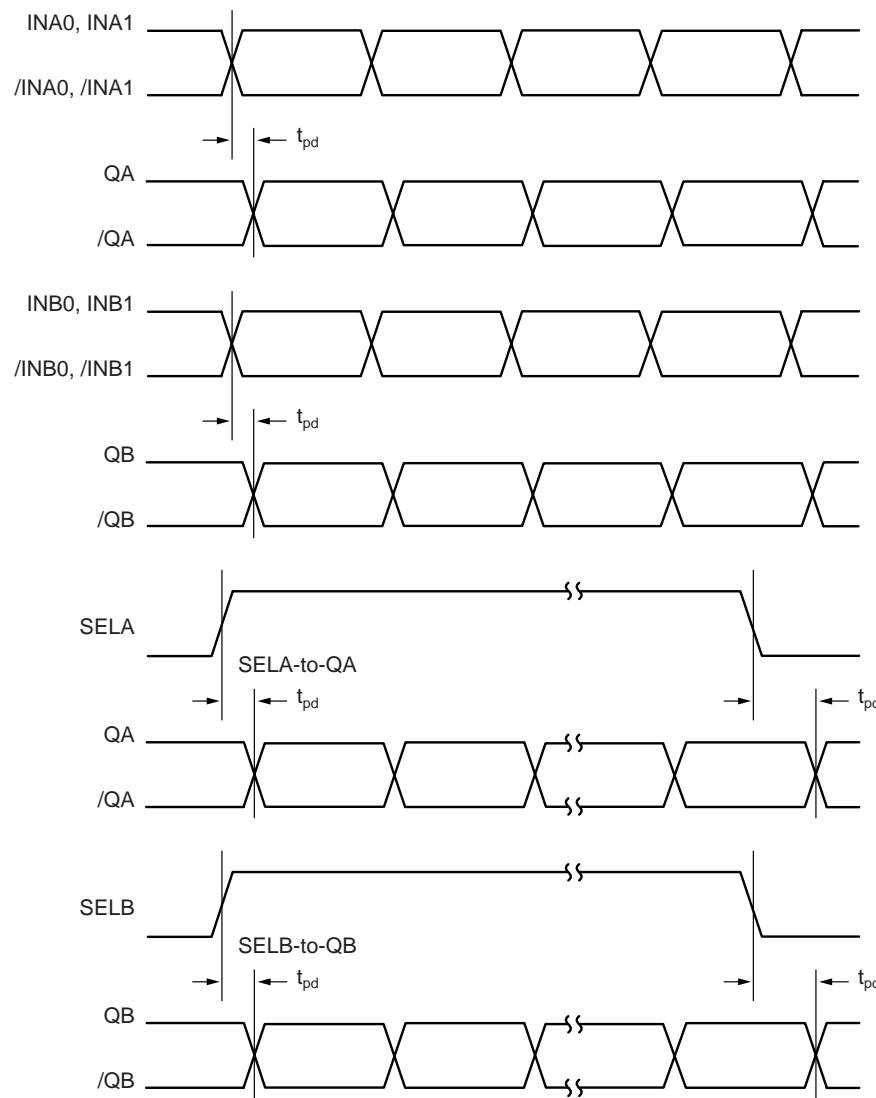
V_{IN}, V_{OUT} 800mV (Typ.)

Figure 1a. Single-Ended Voltage Swing

V_{DIFF_IN}, V_{DIFF_OUT} 1600mV (Typ.)

Figure 1b. Differential Voltage Swing

TIMING DIAGRAM

INA0, INA1

/INA0, /INA1

t_{pd}

QA

/QA

INB0, INB1

/INB0, /INB1

t_{pd}

QB

/QB

SELA

SELA-to-QA

t_{pd}

t_{pd}

QA

/QA

SELB

SELB-to-QB

t_{pd}

t_{pd}

QB

/QB

TYPICAL OPERATING CHARACTERISTICS

V_{CC} = 3.3V, T_A = 25°C, R_L = 50ý to V_{CC} − 2V, DC coupled, unless otherwise stated.

200MHz Output
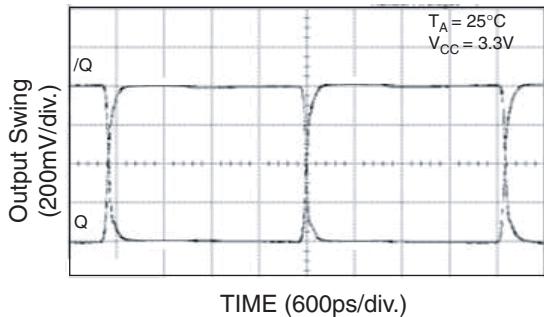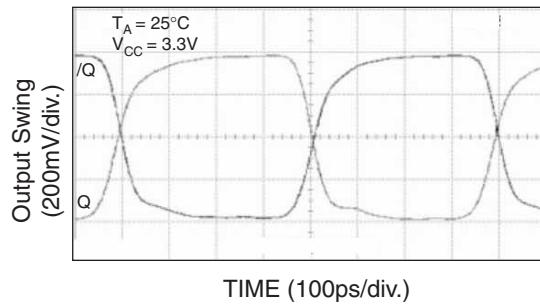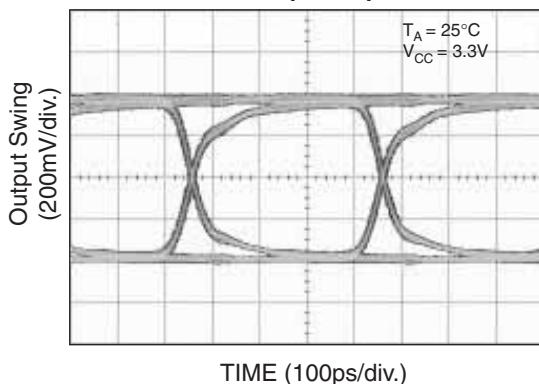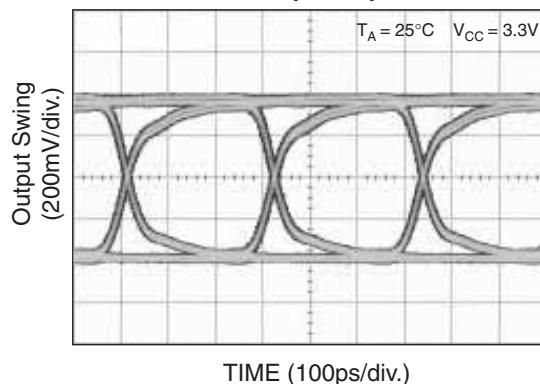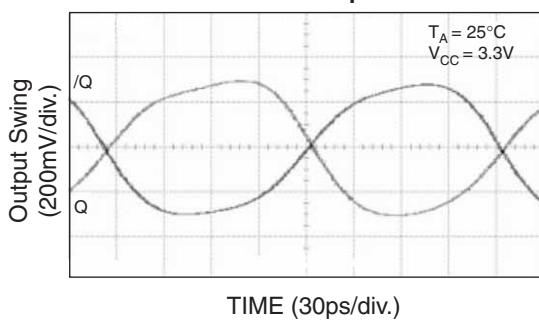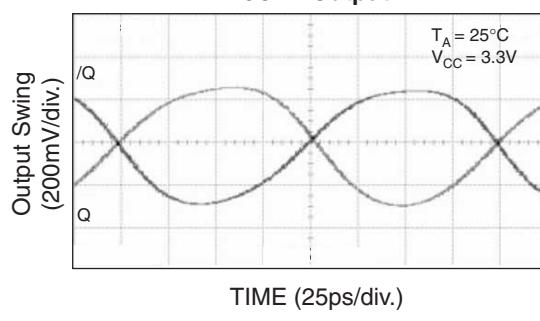
T_A = 25°C
V_{CC} = 3.3V

/Q

Q

Output Swing
(200mV/div.)

TIME (600ps/div.)

1.25GHz Output

T_A = 25°C
V_{CC} = 3.3V

/Q

Q

Output Swing
(200mV/div.)

TIME (100ps/div.)

2.5Gbps Output

T_A = 25°C
V_{CC} = 3.3V

Output Swing
(200mV/div.)

TIME (100ps/div.)

3.2Gbps Output

T_A = 25°C V_{CC} = 3.3V

Output Swing
(200mV/div.)

TIME (100ps/div.)

4GHz Output

T_A = 25°C
V_{CC} = 3.3V

/Q

Q

Output Swing
(200mV/div.)

TIME (30ps/div.)

5GHz Output

T_A = 25°C
V_{CC} = 3.3V

/Q

Q

Output Swing
(200mV/div.)

TIME (25ps/div.)

5Gbps Output

/Q

Q

T_A = 25°C
V_{CC} = 3.3V

Output Swing
(200mV/div.)

TIME (50ps/div.)

TYPICAL OPERATING CHARACTERISTICS

V_{CC} = 3.3V, T_A = 25°C, R_L = 50ý to V_{CC} − 2V, DC coupled, unless otherwise stated.

**Propagation Delay
vs. Temperature**

**Frequency
vs. Output Swing**
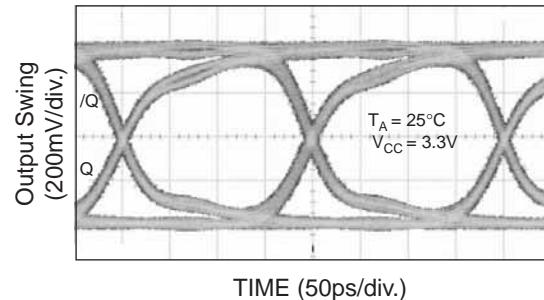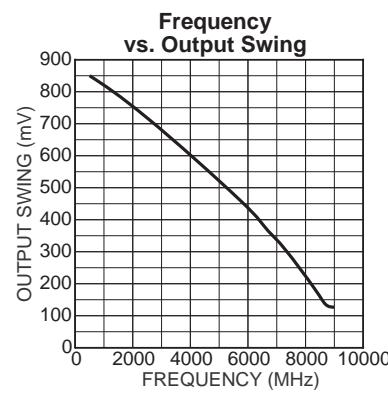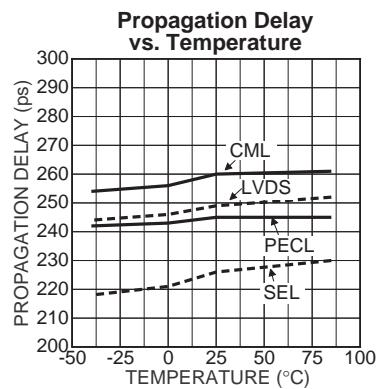
INPUT AND OUTPUT STAGE INTERNAL TERMINATION
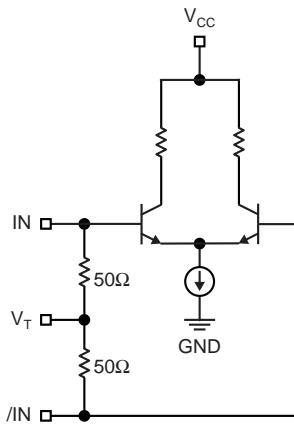
Figure 2a. Simplified Differential Input Stage
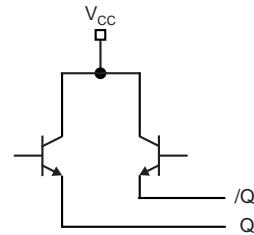
Figure 2b. Simplified LVPECL Output Stage

INPUT INTERFACE APPLICATIONS

For V_{CC} = 3.3V, R_b = 50Ω.
For V_{CC} = 2.5V, R_b = 19Ω.
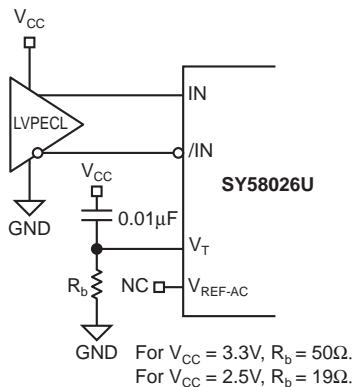
**Figure 3a. DC-Coupled
PECL Interface**

For V_{CC} = 3.3V, R_p = 100Ω.
For V_{CC} = 2.5V, R_p = 50Ω.
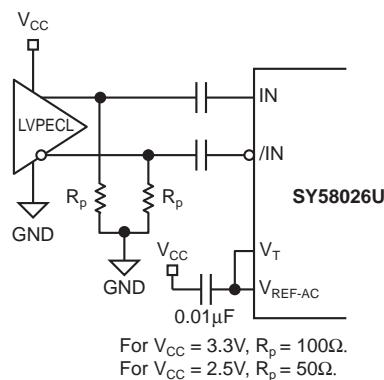
**Figure 3b. AC-Coupled
PECL Interface**
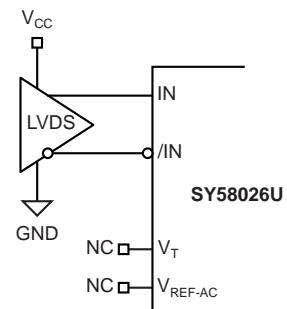
**Figure 3c. LVDS
Interface**
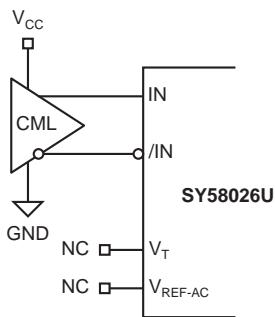
Option: May connecct V_T to V_{CC}.

**Figure 3d. DC-Coupled
CML Interface**
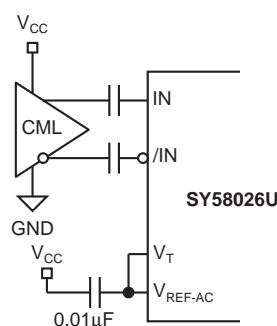
**Figure 3e. AC-Coupled
CML Interface**

OUTPUT INTERFACE APPLICATIONS
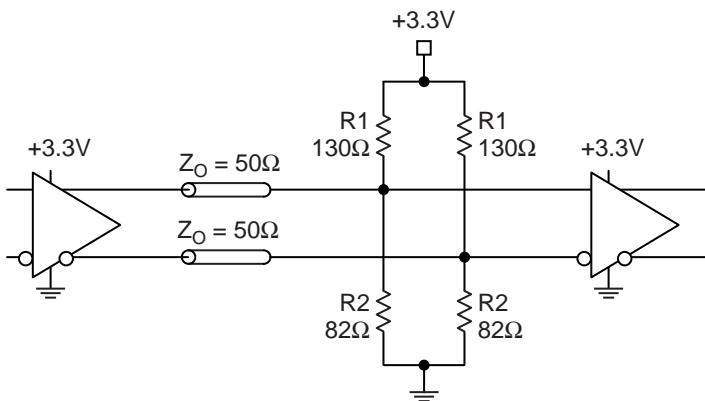
Figure 4a. Parallel Thevenin-Equivalent Termination
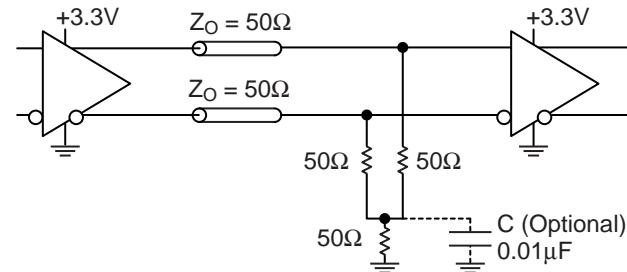

Figure 4b. Parallel Termination (3-Resistor)
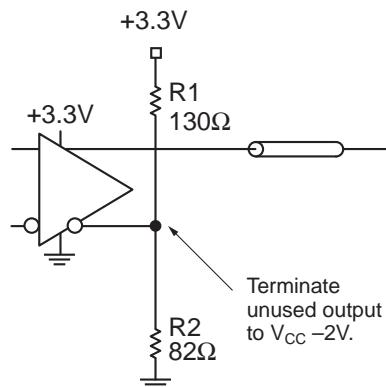
Figure 4c. Terminating Unused Outputs

RELATED MICREL PRODUCTS AND SUPPORT DOCUMENTATION

| Part Number	Function	Data Sheet Link
SY58016L	3.3V 10Gbps Differential CML Line Driver/Receiver with Internal Termination	http://www.micrel.com/product-info/products/sy58016l.shtml
SY58017U	10.7Gbps Differential CML 2:1 MUX with Internal Termination	http://www.micrel.com/product-info/products/sy58017u.shtml
SY58018U	5Gbps LVPECL 2:1 MUX with Internal Termination	http://www.micrel.com/product-info/products/sy58018u.shtml
SY58019U	10.7Gbps 400mV LVPECL 2:1 MUX with Internal Termination	http://www.micrel.com/product-info/products/sy58019u.shtml
SY58025U	10.7Gbps Dual 2:1 CML MUX with Internal Termination	http://www.micrel.com/product-info/products/sy58025u.shtml
SY58027U	10.7Gbps Dual 2:1 400mV LVPECL MUX with Internal Termination	http://www.micrel.com/product-info/products/sy58027u.shtml
SY58051U	10.7Gbps AnyGate® with Internal Input and Output Termination	http://www.micrel.com/product-info/products/sy58051u.shtml
SY58052U	10Gbps Clock/Data Retimer with 50ý Input Termination	http://www.micrel.com/product-info/products/sy58052u.shtml
	MLF™ Application Note	www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

32-PIN *Micro*LeadFrame® (MLF-32)

5.0 BSC

32

PIN #1 ID
0.20 DIA TYP.

1
2

5.0 BSC

TOP VIEW

0.25±0.05 32X

0.50 BSC

PIN #1 ID
R0.20

0.20 MIN.

32

1
2

3.10±0.10

0.40±0.05 4X

3.10±0.10
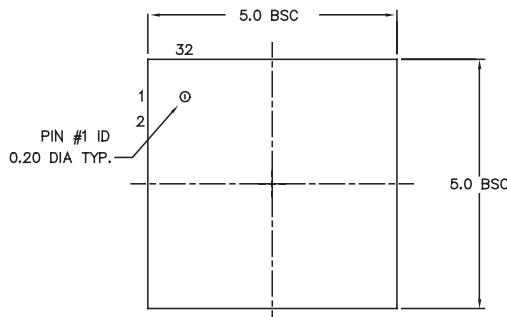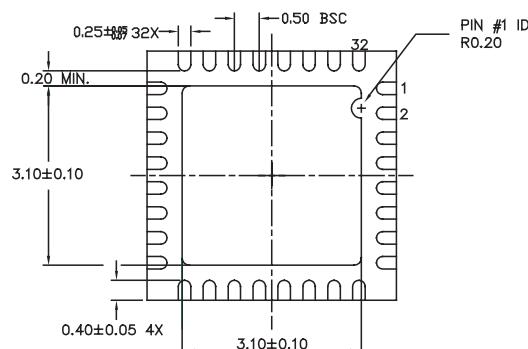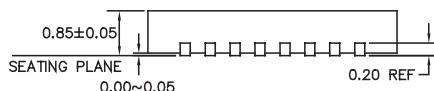
BOTTOM VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.

0.85±0.05

SEATING PLANE

0.00~0.05

0.20 REF

SIDE VIEW

Package

EP- Exposed Pad

Die

CompSide Island

Heat Dissipation

Heat Dissipation

V_{EE}

Heavy Copper Plane

V_{EE}

Heavy Copper Plane
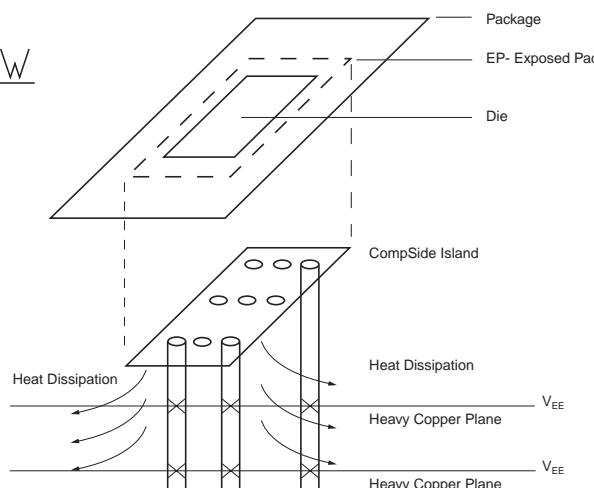
PCB Thermal Consideration for 32-Pin MLF® Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:
1. Package meets Level 2 Moisture Sensitivity Classification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB http://www.micrel.com

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Encoders, Decoders, Multiplexers & Demultiplexers *category:*

Click to view products by Microchip *manufacturer:*

Other Similar products are found below :

MC74HC163ADTG 74HC253N NLV74VHC1G01DFT1G TC74AC138P(F) NLV14051BDR2G NLV74HC238ADTR2G COMX-CAR-210 5962-8607001EA NTE74LS247 5962-8756601EA 8CA3052APGGI8 TC74VHC138F(EL,K,F PI3B3251LE PI3B3251QE NTE4028B NTE4514B NTE4515B NTE4543B NTE4547B NTE74LS249 NLV74HC4851AMNTWG MC74LVX257DG M74HCT4851ADWR2G AP4373AW5-7-01 MC74LVX257DTR2G 74VHC4066AFT(BJ) 74VHCT138AFT(BJ) 74HC158D.652 74HC4052D(BJ) 74VHC138MTC COMX-CAR-P1 JM38510/65852BEA JM38510/30702BEA 74VHC138MTCX 74HC138D(BJ) NL7SZ19DFT2G 74AHCT138T16-13 74LCX138FT(AJ) 74LCX157FT(AJ) NL7SZ18MUR2G PCA9540BD,118 QS3VH16233PAG8 SNJ54HC251J SN54LS139AJ SN74CBTLV3257PWG4 SN74ALS156DR SN74AHCT139PWR 74HC251D.652 74HC257D.652 74HCT153D.652