SY58031U

Ultra-Precision 1:8 CML Fanout Buffer with Internal I/O Termination

General Description

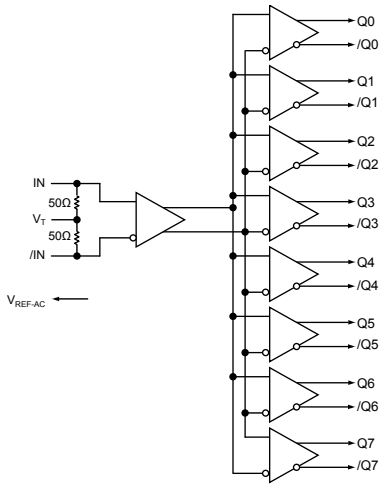
The SY58031U is a 2.5V/3.3V precision, high-speed, fully differential CML 1:8 fanout buffer. The SY58031U is optimized to provide eight identical output copies with less than 20ps of skew and only 75fs$_{RMS}$ phase jitter. It can process clock signals as fast as 6GHz.

The differential input includes Micrel's unique, 3-pin input termination architecture that allows the SY58031U to directly interface to CML, LVPECL, and LVDS differential signals (AC- or DC-coupled) without any level-shifting or termination resistor networks in the signal path. The result is a clean, stub-free, low-jitter interface solution. The CML outputs feature 400mV typical swing into 50Ω loads and provide an extremely fast rise/fall time guaranteed to be less than 60ps.

The SY58031U operates from a 2.5V ±5% supply or 3.3V ±10% supply and is guaranteed over the full industrial temperature range (–40°C to +85°C). For applications that require high-speed 1:8 LVPECL fanout buffers, consider the SY58032U and SY58033U. The SY58031U is part of Micrel's high-speed, Precision Edge® product line.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

Block Diagram



Precision Edge®

Features

- Precision 1:8, 400mV CML fanout buffer
- Guaranteed AC performance over temperature and voltage:
  - Clock frequency range: DC to >6GHz
  - <60ps t_r/t_f time
  - <270ps t_{pd}
  - <20ps output-to-output skew
- Low-jitter performance:
  - 75fs$_{RMS}$ phase jitter (typ.)
- 50Ω source-terminated CML outputs
- 400mV CML output swing into 50Ω load
- Fully differential I/O
- Accepts an input signal as low as 100mV
- Unique, patent-pending input termination and VT pin accepts DC-coupled and AC-couple differential inputs (LVPECL, LVDS, and CML)
- Power supply 2.5V ±5% or 3.3V ±10%
- Industrial temperature range: –40°C to +85°C
- Available in 32-pin, 5mm × 5mm QFN package

Applications

- All SONET and GigE clock distribution
- All Fibre Channel clock and data distribution
- Network routing engine timing distribution
- High-end, low-skew multiprocessor synchronous clock distribution

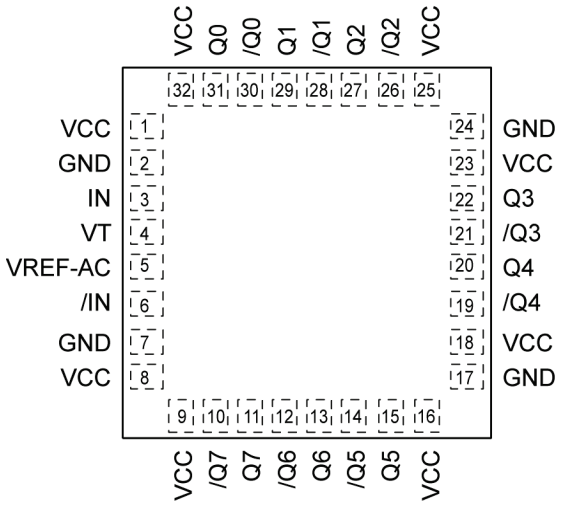
Ordering Information

Part Number[1]	Package Type	Operating Range	Package Marking	Lead Finish
SY58031UMG	QFN-32	Industrial	SY58031U with Pb-free bar-line indicator	Pb-Free NiPdAu
SY58031UMGTR[2]	QFN-32	Industrial	SY58031U with Pb-free bar-line indicator	Pb-Free NiPdAu

Note:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC electricals only.
2. Tape and Reel.

Pin Configuration



32-Pin QFN

Pin Description

Pin Number	Pin Name	Pin Function
3, 6	IN, /IN	Differential signal input: Each pin of this pair internally terminates with 50Ω to the VT pin. Note that this input will default to an indeterminate state if left open. See Input Interface Applications section.
4	VT	Input termination center-tap: Each input terminates to this pin. The VT pin provides a center-tap for each input (IN, /IN) to the termination network for maximum interface flexibility. See Input Interface Applications section.
2, 7, 17, 24	GND, Exposed Pad	Ground. Exposed pad must be connected to a ground plane that is the same potential as the ground pin.
1, 8, 9, 16 18, 23, 25, 32	VCC	Positive power supply: Bypass with 0.1µF/0.01µF low ESR capacitors as close to the pins as possible
31, 30, 29, 28, 27, 26, 22, 21 20, 19, 15, 14 13, 12, 11, 10	Q0, /Q0, Q1, /Q1 Q2, /Q2. Q3, /Q3 Q4, /Q4, Q5, /Q5 Q6, /Q6, Q7, /Q7	CML differential output pairs: Differential buffered output copy of the input signal. The CML output swing is typically 400mV into 50Ω. Unused output pairs may be left floating with no impact on jitter. See CML Output Termination section
5	VREF-AC	Bias Reference Voltage: Equal to V_{CC}–1.2V (typical), and used for AC-coupled applications. See Input Interface Applications section. When using V_{REF-AC}, bypass with 0.01µF capacitor to V_{CC}. Maximum sink/source current is 0.5mA.

Absolute Maximum Ratings[3]

Power Supply Voltage (VCC)..... –0.5V to +4.0V
Input Voltage (VIN)..... –0.5V to VCC
Current (VT)
  Source or sink current on VT pin..... ±100mA
Input Current (VT)
  Source or sink current on IN, /IN..... ±50mA
Current (VREF)
  Source or sink current on VREF-AC[5] ..... ±1.5mA
Lead Temperature (soldering, 20s)..... 260°C
Storage Temperature (Ts)..... –65°C to +150°C

Operating Ratings[4]

Power Supply Voltage (V_{CC}) ..... +2.375V to +3.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Junction Thermal Resistance[6]
  QFN (θ_{JA}), Still-Air..... 35°C/W
  QFN (ψ_{JB}), Junction-to-Board..... 20°C/W

DC Electrical Characteristics[7]

T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage	2.5V nominal 3.3V nominal	2.375 3.0	2.5 3.3	2.625 3.6	V
I_{CC}	Power supply current	VCC = max., no lead. Includes current through 50Ω pull-ups.		265	330	mA
V_{IH}	Input HIGH voltage	IN1, /IN1, Note 8	V_{CC}-1.6		V_{CC}	V
V_{IL}	Input LOW voltage	IN1, /IN1	0		V_{IH}-0.1	V
V_{IN}	Input voltage swing	IN1, /IN1, see Figure 1.	0.1		1.7	V
V_{DIFF_IN}	Differential input voltage swing [IN0, /IN0], [IN1, /IN1]	IN1, /IN1, see Figure 2.	0.2			V
R_{IN}	In-to-V_T resistance		40	50	60	Ω
$V_{T\ IN}$	Max. In-to-V_T (IN, /IN)				1.28	V
V_{REF-AC}			V_{CC}-1.3	V_{CC}-1.2	V_{CC}-1.1	V

CML DC Electrical Characteristics[7]

V_{CC} = 2.5V ±5% or 3.3V ±10%; R_L = 100Ω across Q and /Q; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output HIGH voltage		V_{CC}-0.02		V_{CC}	V
V_{OUT}	Output LOW voltage	See Figure 1.	325	400		mV
V_{DIFF_OUT}	Differential voltage swing	See Figure 2.	650	800		mV
R_{OUT}	Output source impedance		40	50	60	Ω

Notes:

3. Exceeding the absolute maximum ratings may damage the device.
4. The datasheet ratings are not guaranteed if the device is operated beyond the operating ratings.
5. Due to the limited drive capability, use for input of the same package only.
6. Thermal performance assumes exposed pad is soldered (or equivalent) to the device's most negative potential (GND) on the PCB. ψ_{JB} uses 4-layer θ_{JA} in still-air number unless otherwise stated.
7. The device is not guaranteed to function outside its operating ratings.
8. V_{IH} (min.) not lower than 1.2V.

AC Electrical Characteristics[9]

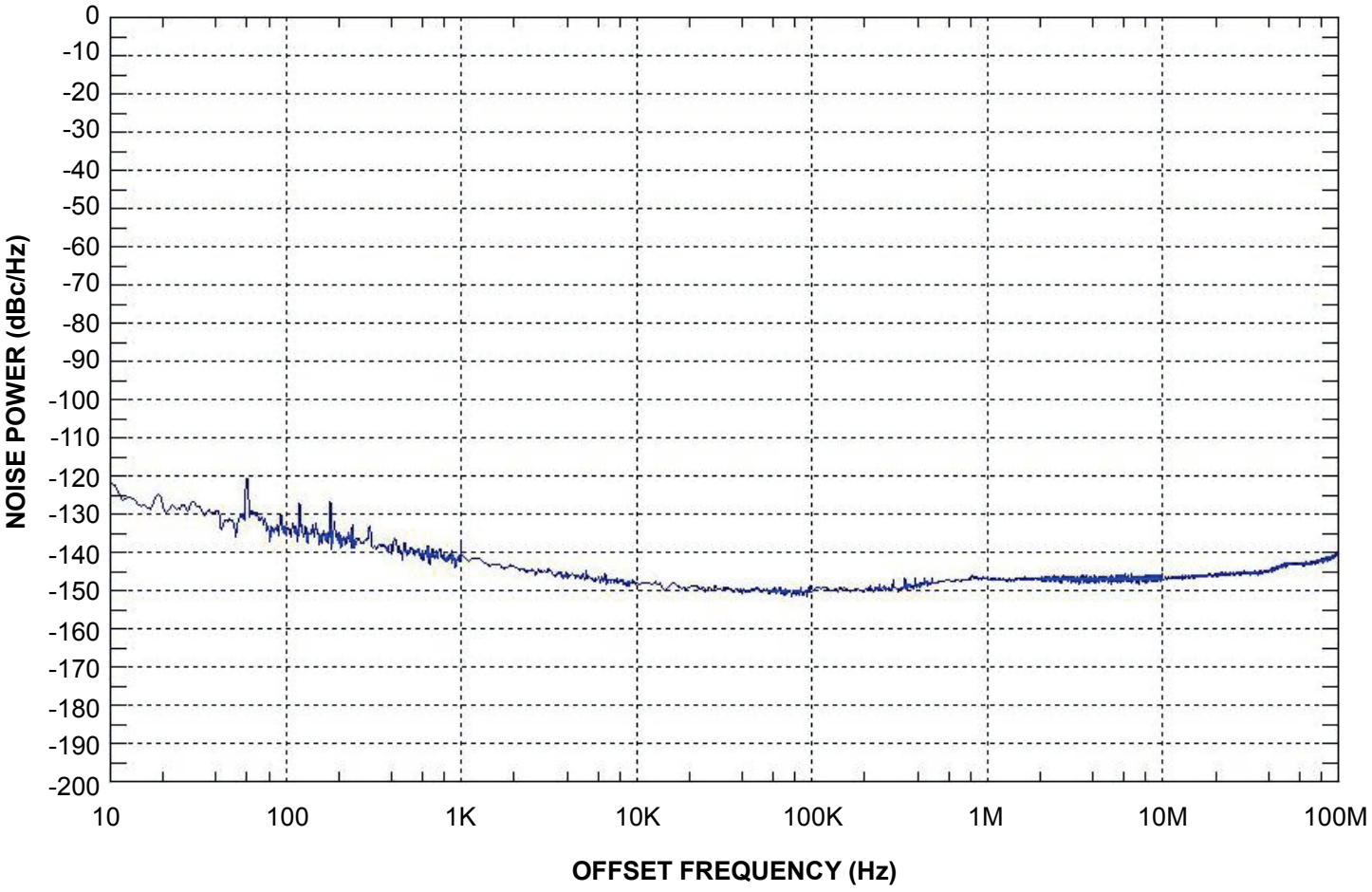
VCC = 2.5V ±5% or 3.3V ±10%; RL = 100Ω across each output pair or equivalent; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{MAX}	Maximum operating frequency	V_{OUT} ≥200mV clock	6			GHz
t_{pd}	Propagation delay (IN-to-Q)		120	230	270	ps
$t_{pd\ tempco}$	Differential propagation delay temperature coefficient			35		fs/°C
t_{SKEW}	Output-to-output (within device)	Note 10		7	20	ps
	Part-to-part	Note 11			100	ps
t_{JITTER}	RMS phase jitter	Output: 622MHz Integration range 12kHz – 20MHz		75		ps
t_r/t_f	Output rise/fall time	20% to 80% at full output swing.	20	45	60	ps

Notes:

9. High frequency AC electricals are guaranteed by design and characterization. All outputs loaded, V_{IN} ≥100mV.
10. Output-to-output skew is measured between outputs under identical transitions.
11. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature with no skew of the edges at the respective inputs. Part-to-part skew includes variation in t_{pd}.

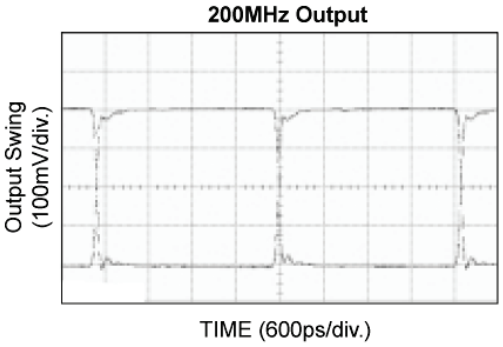
Phase Noise Plot

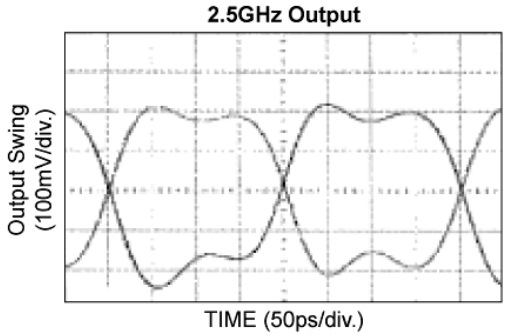


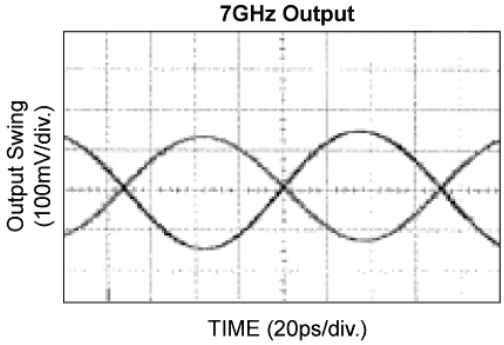
Phase Noise Plot: 622MHz @ 3.3V

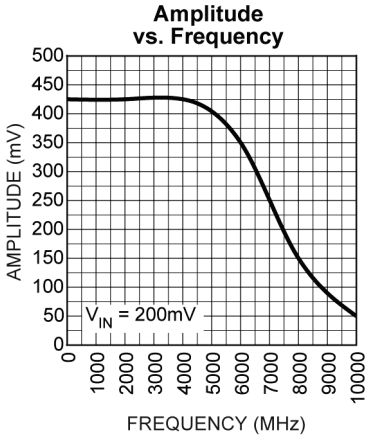
hbwhelp@micrel.com or (408) 955-1690

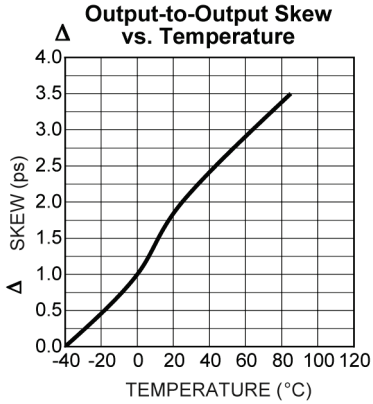
Typical Operating Characteristics

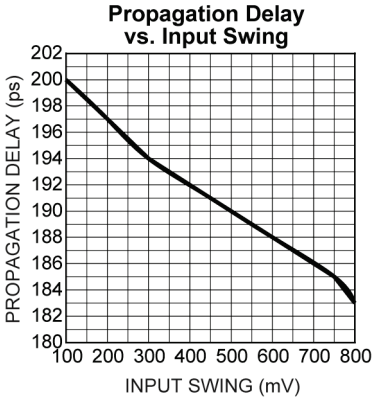


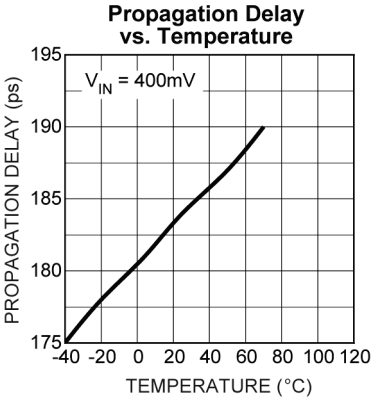












Single-Ended and Differential Swings

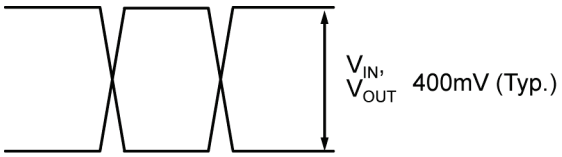


Figure 1. Single-Ended Voltage Swing

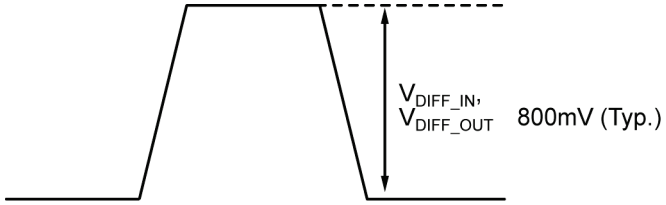
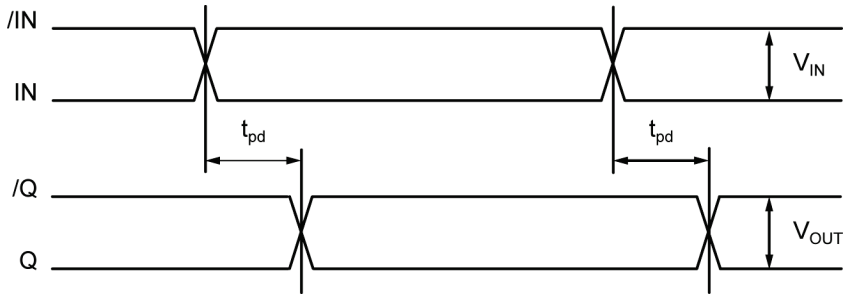


Figure 2. Differential Voltage Swing

Timing Diagram



Input Buffer

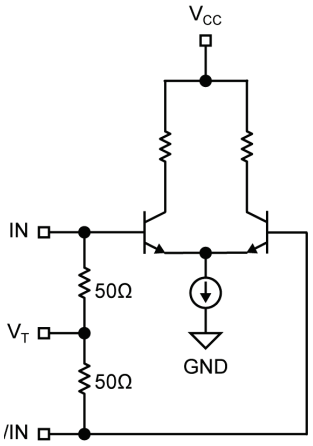


Figure 3. Simplified Differential Input Buffer

Input Interface Applications

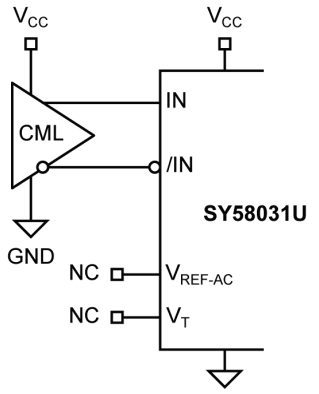


Figure 4. DC-Coupled CML Input Interface
Optional: May connect V_T to V_{CC}

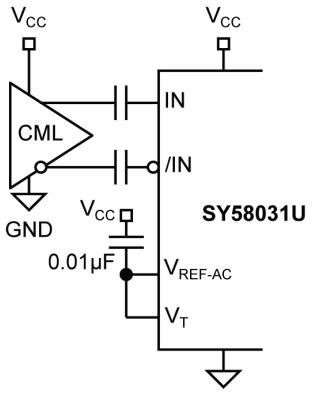


Figure 5. AC-Coupled CML Input Interface

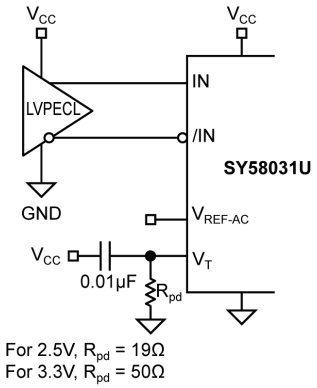


Figure 6. LVPECL Input Interface

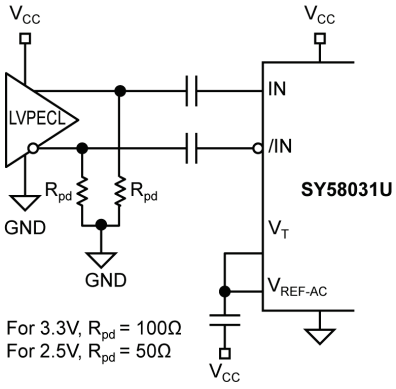


Figure 7. AC-Coupled LVPECL Input Interface

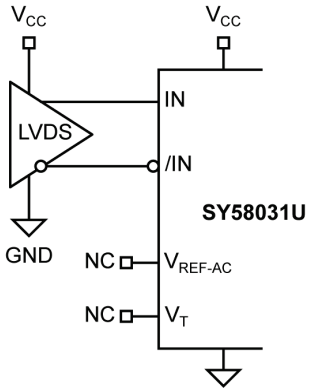


Figure 8. LVDS Input Interface

CML Output Termination

Figure 9 and Figure 10 illustrate how to terminate a CML output using both the AC- and DC-coupled configuration. All outputs of the SY58031U are 50Ω with a 16mA current source.

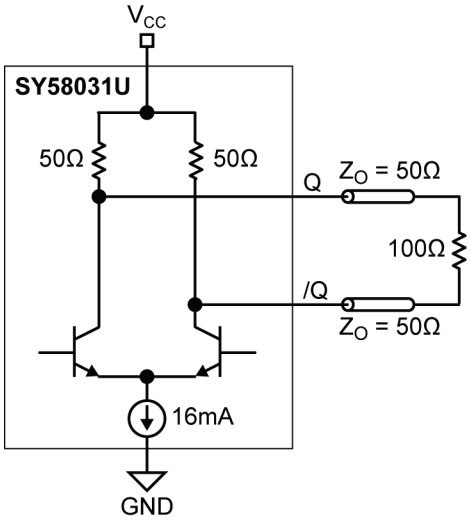


Figure 9. CML DC-Coupled Termination

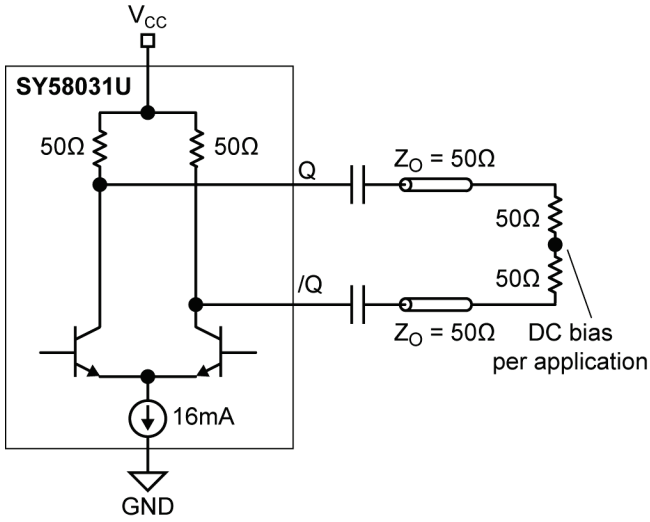
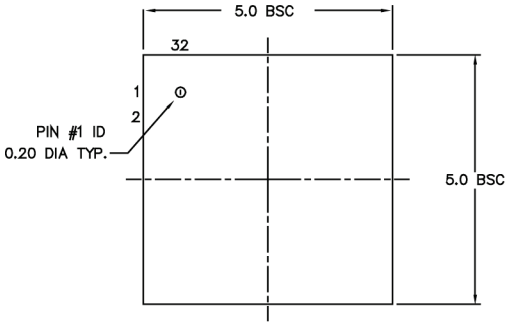


Figure 10. CML AC-Coupled Termination

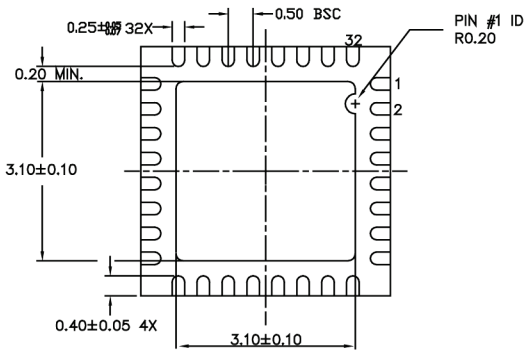
Related Micrel Products and Support Documentation

Part Number	Function	Website Link
SY58031U	Ultra-Precision 1:8 CML Fanout Buffer with Internal I/O Termination	http://www.micrel.com/_PDF/HBW/sy58031u.pdf
SY58032U	Ultra-Precision 1:8 LVPECL Fanout Buffer with Internal Termination	http://www.micrel.com/_PDF/HBW/sy58032u.pdf
SY58033U	Ultra-Precision 1:8 400mV Fanout Buffer with Internal Termination	http://www.micrel.com/_PDF/HBW/sy58033u.pdf
	HBW Solutions	http://www.micrel.com/index.php/en/products/clock-timing.html

Package Information[12, 13]

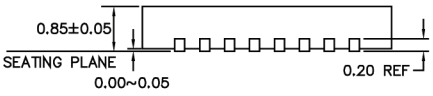


TOP VIEW

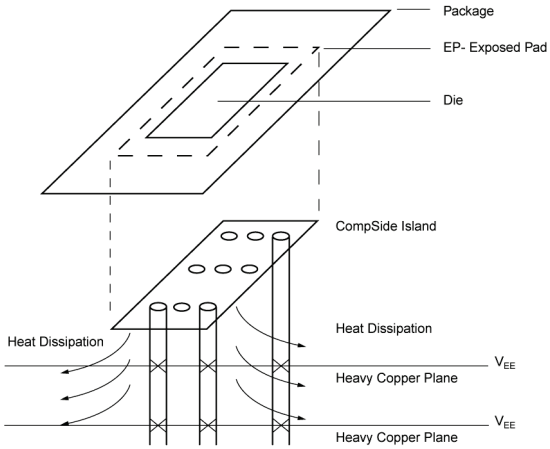


BOTTOM VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



SIDE VIEW



32-Pin QFN and PCB Thermal Consideration for Package
(Always solder, or equivalent, the exposed pad to the PCB)

Note:

12. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.
13. Package meets Level 2 qualification. All parts are dry-packaged before shipment. Exposed pads must be soldered to a ground for proper thermal management.

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