SY89202U

Precision 1:8 LVPECL Fanout Buffer with Three ÷1/÷2/÷4 Clock Divider Output Banks

General Description

The SY89202U is a precision, high-speed, integrated clock divider LVPECL fanout buffer capable of handling clocks up to 1.5GHz. Optimized for communications applications, the three independently controlled output banks are phase matched and can be configured for pass-through (÷1), ÷2 or ÷4 divide ratios.

The differential input includes Micrel's unique, 3-pin input termination architecture that allows the user to interface to any AC- or DC-coupled signal as small as 100mV ($200mV_{pp}$) without any level shifting or termination resistor networks in the signal path. The low skew, low jitter outputs are 800mV, 100k compatible LVPECL, with extremely fast rise/fall times guaranteed to be less than 220ps.

The EN (enable) input guarantees that the ÷1, ÷2 and ÷4 outputs will start from the same state without any runt pulse after an asynchronous MR (master reset) is asserted. This is accomplished by enabling the outputs after a four-clock delay to allow the counters to synchronize.

The SY89202U is part of Micrel's Precision Edge® product family.

Datasheets and support documentation can be found on Micrel's web site at www.micrel.com.

Precision Edge®

Features

Three low-skew LVPECL output banks with programmable ÷1, ÷2 and ÷4 divider options

- Three independently programmable output banks
- Guaranteed AC performance over temp and voltage:
  – >1.5GHz clock frequency (f_{MAX})
  – <930ps In-to-Out t_{pd}
  – <220ps t_r/t_f
- Ultra-low jitter design:
  – <$1ps_{RMS}$ random jitter (RJ)
  – <$10ps_{PP}$ total jitter (clock)
- Internal input termination
- Patent-pending input termination and VT pin accepts AC- and DC-coupled inputs (CML, PECL, LVDS)
- 800mV LVPECL output swing
- CMOS/TTL-compatible output enable (EN) and divider select control
- Power supply 2.5V ±5% or 3.3V ±10%
- –40°C to +85°C industrial temperature range
- Available in 32-pin QFN package

Applications

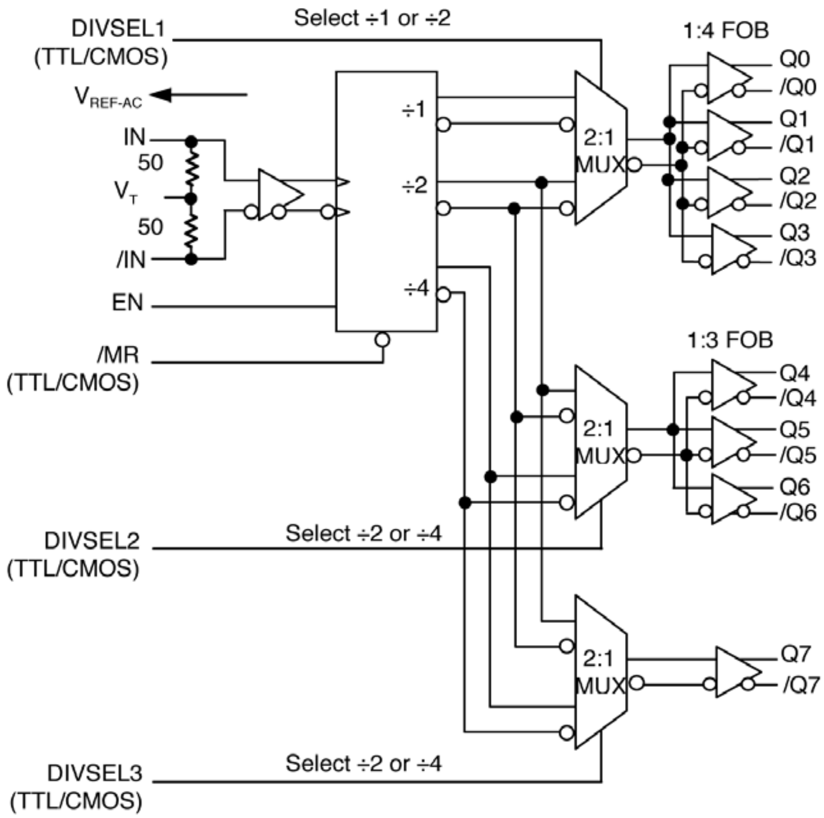
- All SONET/SDH channel select applications
- All Fibre Channel multi-channel select applications
- All Gigabit Ethernet multi-channel select applications

Markets

- LAN/WAN
- Enterprise servers
- ATE
- Test and measurement

United States Patent No. RE44,134

Functional Block Diagram



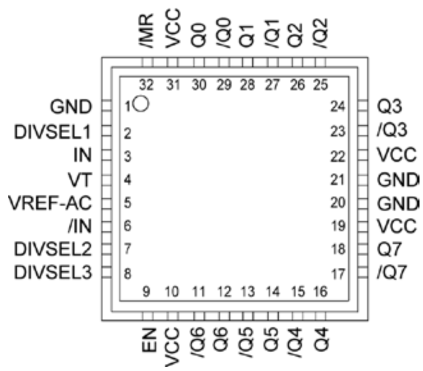
Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89202UMG	QFN-32	Industrial	SY89202U with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY89202UMGTR[(2)]	QFN-32	Industrial	SY89202U with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25_C, DC Electricals Only.
2. Tape and Reel.

Pin Configuration



32-Pin QFN

Pin Description

Pin Number	Pin Name	Pin Function
2, 7, 8	DIVSEL1 DIVSEL2 DIVSEL3	Single-Ended Inputs: These TTL/CMOS inputs select the divide ratio for each of the three banks of outputs. Note that each of these inputs is internally connected to a 25k Ω pull-up resistor and will default to logic HIGH state if left open. The input-switching threshold is $V_{CC}/2$.
3, 6	IN, /IN	Differential Input: This input pair is the differential signal input to the device. This input accepts AC- or DC-coupled signals as small as 100mV. The input pair internally terminates to a VT pin through 50Ω. Note that these inputs will default to an indeterminate state if left open. Please refer to the “Input Interface Applications” section for more details.
4	VT	Input Termination Center-Tap: Each side of the differential input pair terminates to the VT pin. The VT pin provides a center-tap to a termination network for maximum interface flexibility. See “Input Interface Applications” section for more details.
5	VREF-AC	Reference Voltage: This output biases to V_{CC} –1.2V. It is used for AC-coupling inputs IN and /IN. For AC-coupled applications, connect V_{REF-AC} directly to the VT pin. Bypass with 0.01µF low ESR capacitor to V_{CC}.
9	EN	Single-Ended Input: This TTL/CMOS input disables and enables the Q0 – Q7 outputs. This input is internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state if left open. The input-switching threshold is $V_{CC}/2$. For the input enable and disable functional description, refer to “Timing Diagram” section.
10, 19, 22, 31	VCC	Positive power supply. Bypass with 0.1µF‖0.01µF low ESR capacitors as close to VCC pins as possible.
16, 15, 14, 13, 12, 11	Q4, /Q4, Q5, /Q5, Q6, /Q6	Bank 2 LVPECL differential output pairs controlled by DIVSEL2: LOW, Q4 – Q6 = ÷2, HIGH, Q4 – Q6 = ÷4. Unused output pairs may be left open. Each output is designed to drive 800mV into 50Ω terminated at V_{CC}–2V.
30, 29, 28, 27, 26, 25, 24, 23	Q0, /Q0, Q1, /Q1, Q2, /Q2, Q3, /Q3	Bank 1 LVPECL differential output pairs controlled by DIVSEL1: LOW, Q0 – Q3 = ÷1, HIGH, Q0 – Q3 = ÷2. Unused output pairs may be left open. Each output is designed to drive 800mV into 50Ω terminated at V_{CC}–2V.
18, 17	Q7, /Q7	Bank 3 LVPECL differential output pair controlled by DIVSEL3: LOW, Q7 = ÷2, HIGH, Q7 = ÷4. Unused output pairs may be left open. Each output is designed to drive 800mV into 50 Ω terminated at V_{CC}–2V.
32	/MR	Single-Ended Input: This TTL/CMOS-compatible master reset function asynchronously sets Q0 – Q7 outputs LOW and /Q0 – /Q7 outputs HIGH, and holds them in that state as long as the /MR input remains LOW. This input is internally connected to a 25k Ω pull-up resistor and will default to a logic HIGH state if left open. The input-switching threshold is $V_{CC}/2$.
1, 20, 21	GND, Exposed Pad	Ground: Ground pin and exposed pad must be connected to the same ground plane.

Truth Table

/MR[1]	EN[2, 3]	DIVSEL1	DIVSEL2	DIVSEL3	Q0 – Q3	Q4 – Q6	Q7
0	X	X	X	X	0	0	0
1	0	X	X	X	0	0	0
1	1	0	0	0	÷1	÷2	÷2
1	1	1	1	1	÷2	÷4	÷4

Notes:

1. /MR asynchronously forces Q0 – Q7 LOW (/Q0 - /Q7 HIGH).
2. EN forces Q0 – Q7 LOW between 2 and 6 input clock cycles after the falling edge of EN. Refer to “Timing Diagram” section.
3. EN synchronously enables the outputs between 2 and 6 input clock cycles after the rising edge of EN. Refer to “Timing Diagram” section.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) .... –0.5V to +4.0V
Input Voltage (V_{IN}) .... –0.5V to V_{CC}
Termination Current
Source or sink current on V_T .... ±100mA
Output Current
Source or sink current on IN, /IN .... ±50mA
V_{REF-AC} Current
Source or sink current on V_{REF-AC} .... ±1.5mA
Lead Temperature (soldering, 20 sec.) .... +260ºC
Storage Temperature (T_s) .... –65ºC to 150ºC

Operating Ratings[2]

Supply Voltage (V_{CC}) .... +2.375V to +2.625V
.... +3.0V to +3.6V
Ambient Temperature (T_A) .... –40ºC to +85ºC
Package Thermal Resistance[3]
QFN (θ_{JA})
Still-Air 35ºC/W
QFN (ψ_{JB})
Junction-to-Board 20ºC/W

DC Electrical Characteristics[4]

T_A =–40°C to +85°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply		2.375 3.0		2.625 3.6	V V
I_{CC}	Power Supply Current	No load, max. V_{CC}		125	180	mA
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
R_{IN}	Input Resistance (IN-to-V_T)		45	50	55	Ω
V_{IH}	Input High Voltage (IN, /IN)		1.2		V_{CC}	V
V_{IL}	Input Low Voltage (IN, /IN)		0		V_{IH}–0.1	V
V_{IN}	Input Voltage Swing (IN, /IN)	See Figure 1a.	0.1		V_{CC}	V
V_{DIFF_IN}	Differential Input Voltage Swing |IN-/IN|	See Figure 1b.	0.2			V
V_{REF-AC}	Output Reference Voltage (V_{REF-AC})		V_{CC}–1.3	V_{CC}–1.2	V_{CC}–1.1	V
IN-to-V_T	Voltage from Input to V_T				1.8	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package Thermal Resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. θ_{JA} and ψ_{JB} values are determined for a 4-layer board in still air, unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

LVPECL Outputs DC Electrical Characteristics(5)

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A = –40ºC to + 85ºC; R_L = 50Ω to V_{CC}–2V, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage Q, /Q		V_{CC}-1.145		V_{CC}–0.895	V
V_{OL}	Output LOW Voltage Q, /Q		V_{CC}-1.945		V_{CC} –1.695	V
V_{OUT}	Output Voltage Swing Q, /Q	See Figure 1a.	550	800		mV
$V_{DIFF-OUT}$	Differential Output Voltage Swing |Q – /Q|	See Figure 1b.	1100	1600		mV

LVTTL/CMOS DC Electrical Characteristics(5)

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A = –40ºC to + 85ºC, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IH}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current		–125		30	µA
I_{IL}	Input LOW Current		–300			µA

Note:

5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics(6)

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A = –40ºC to + 85ºC, R_L = 50Ω to V_{CC}–2V, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Output Toggle Frequency	Output swing ≥ 400mV	1.5			GHz
	Maximum Input Frequency		3.0			GHz
t_{PD}	Differential Propagation Delay	IN-to-Q	530	700	930	ps
	/MR – Q Propagation Delay				900	ps
t_{PD} Tempco	Differential Propagation Delay Temperature Coefficient			115		fs/°C
t_{SKEW}	Within-bank Skew	Within same fanout bank, Note 7		10	25	ps
	Bank-to-Bank Skew	Same divide setting, Note 8		15	35	ps
	Bank-to-Bank Skew	Different divide setting, Note 8		25	50	ps
	Part-to-Part Skew	Note 9			200	ps
t_{JITTER}	Deterministic Jitter (DJ)	Note 10			10	ps_{PP}
	Random Jitter (RJ)	Note 11			1	ps_{RMS}
	Total Jitter	Note 12			10	ps_{PP}
	Cycle-to-Cycle Jitter	Note 13			1	ps_{RMS}
t_r, t_f	Output Rise/Fall Time	20% to 80%, At full output swing.	70	130	220	ps

Notes:

6. Measured with 100mV input swing. See "Timing Diagrams" section for definition of parameters. High-frequency AC-parameters are guaranteed by design and characterization.
7. Within-bank skew is the difference in propagation delays among the outputs within the same bank.
8. Bank-to-bank skew is the difference in propagation delays between outputs from different banks. Bank-to-bank skew is also the phase offset between each bank, after MR is applied.
9. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
10. Deterministic jitter is measured with a K28.7 101010 pattern, measured at $<f_{MAX}$.
11. Random jitter is measured with a K28.7 101010 pattern, measured at $<f_{MAX}$.
12. Total jitter definition: with an ideal clock input of frequency $<f_{MAX}$, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.
13. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, $T_n – T_{n-1}$ where T is the time between rising edges of the output signal.

Single-Ended and Differential Swings

Figure 1a. Single-Ended Voltage Swing

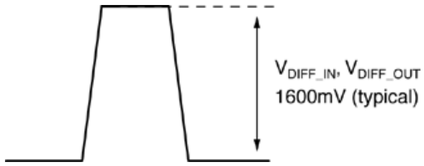
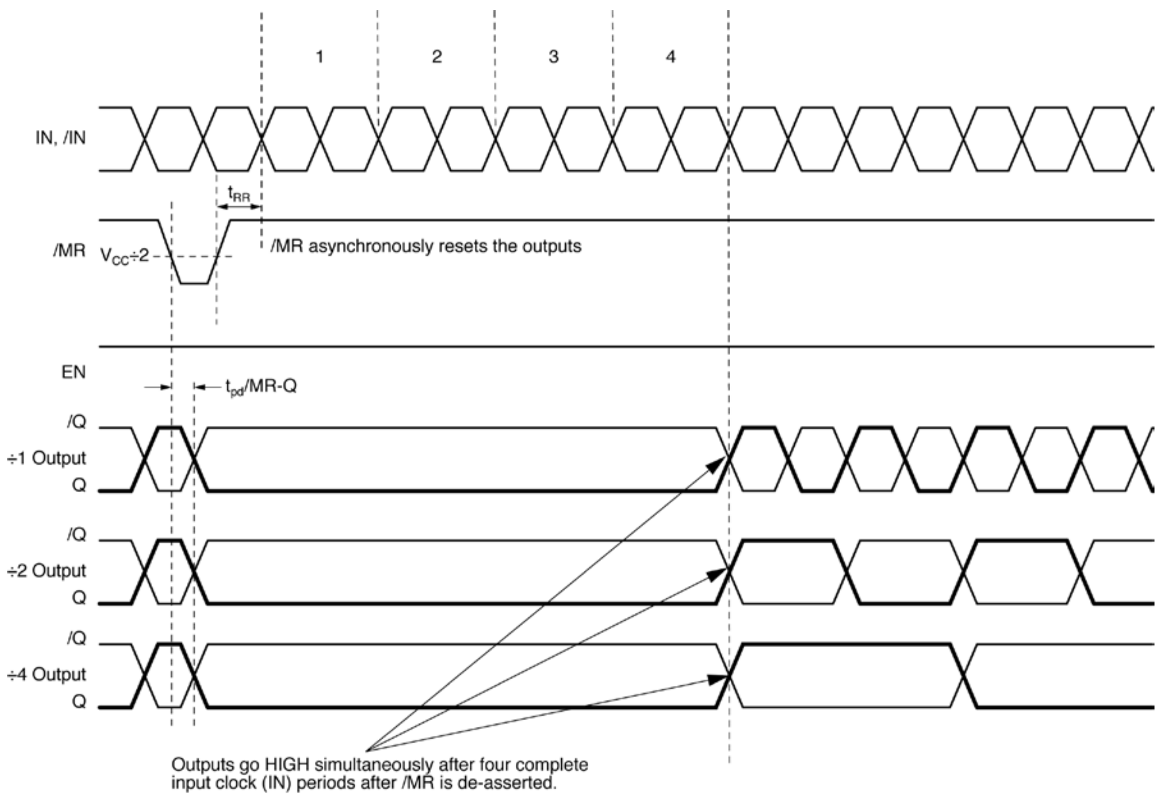
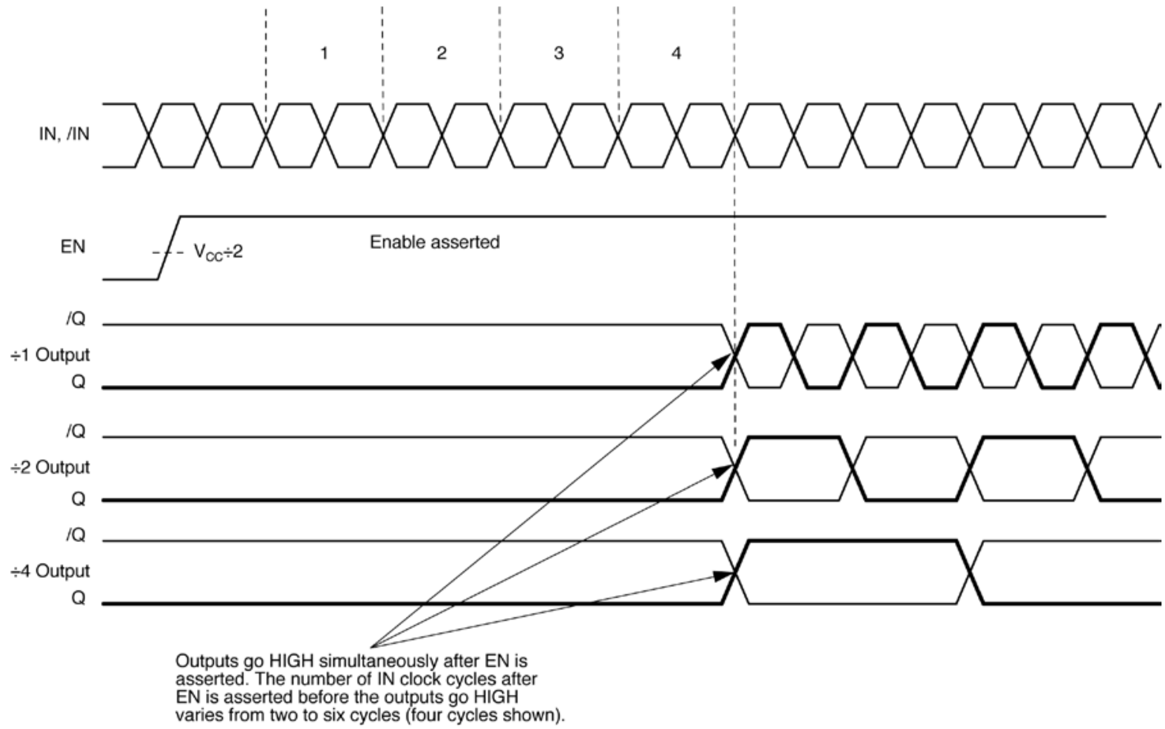


Figure 1b. Differential Voltage Swing

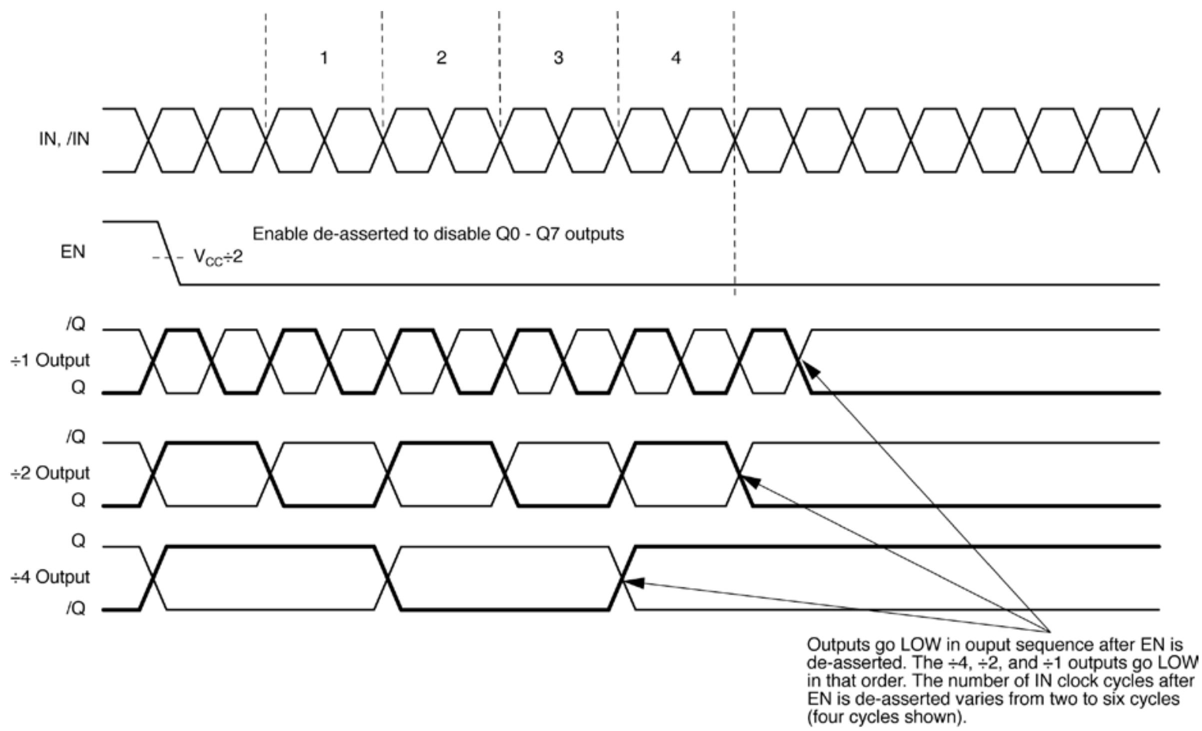
Timing Diagrams



Timing Diagram Showing Reset with Output Enabled



Timing Diagram Showing Enable Timing

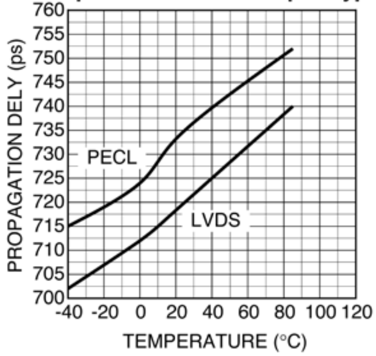


Timing Diagram Showing Disable Timing

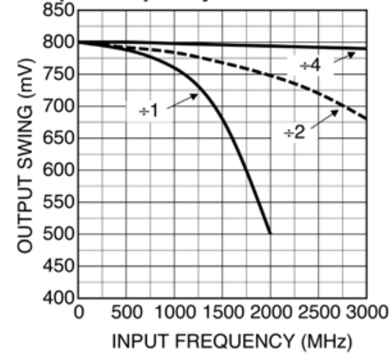
hbwhelp@micrel.com or (408) 955-1690

Typical Operating Characteristics

Propagation Delay vs. Temperature for Each Input Type

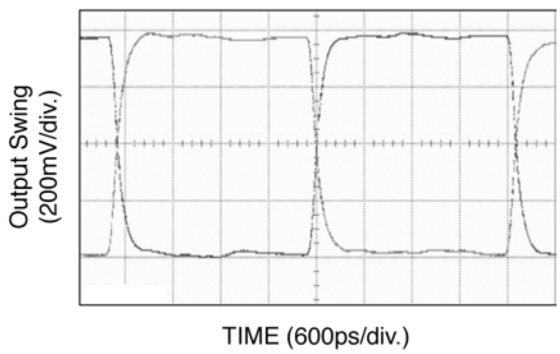


Output Swing vs. Input Frequency for Each Divider

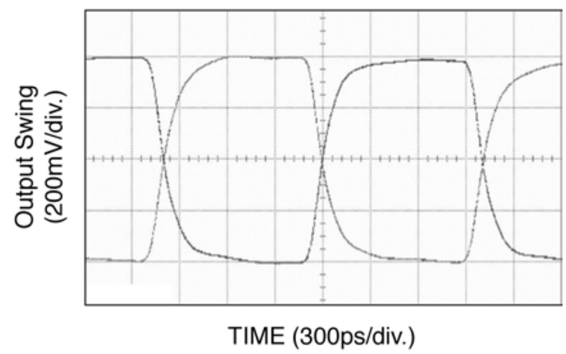


Functional Characteristics

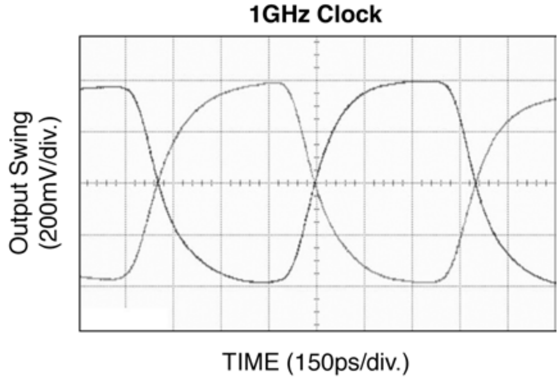
200MHz Clock



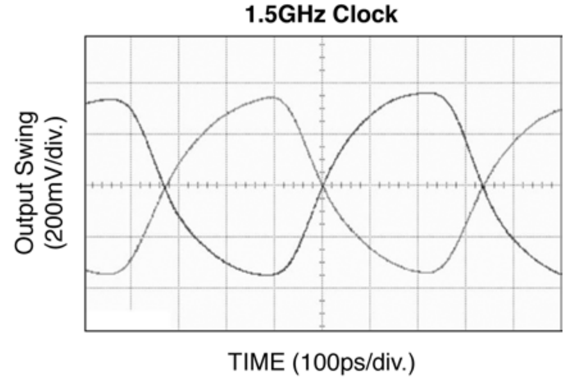
500MHz Clock



1GHz Clock



1.5GHz Clock



Input and Output Stages

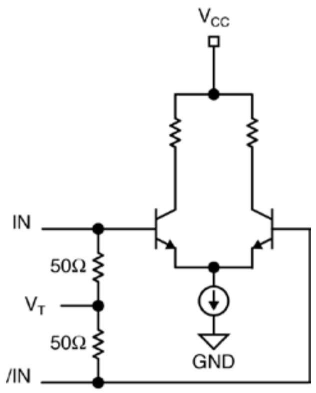


Figure 2a. Simplified Differential Input Stage

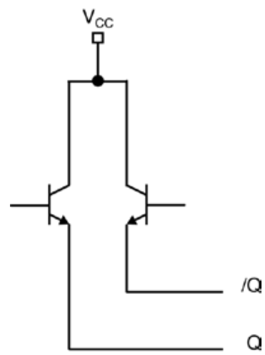


Figure 2b. Simplified LVPECL Output Stage

Input Interface Applications

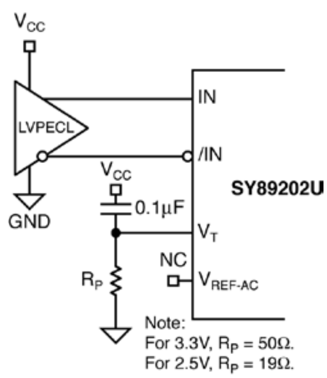


Figure 3a. LVPECL Interface (DC-Coupled)

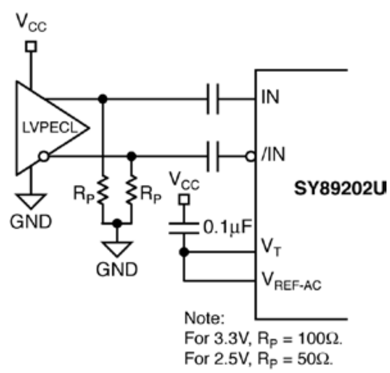


Figure 3b. LVPECL Interface (AC-Coupled)

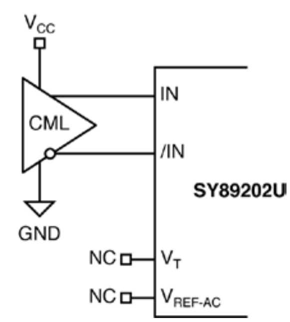


Figure 3c. CML Interface (DC-Coupled)

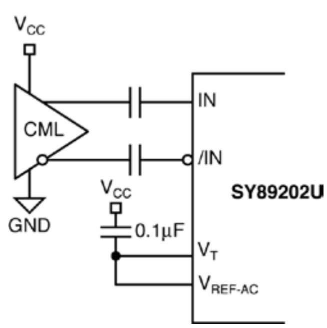


Figure 3d. CML Interface (AC-Coupled)

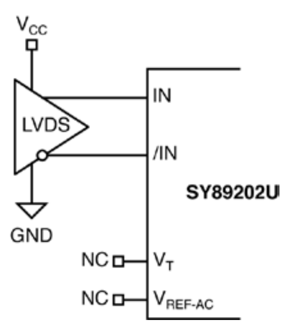


Figure 3e. LVDS Interface (DC-Coupled)

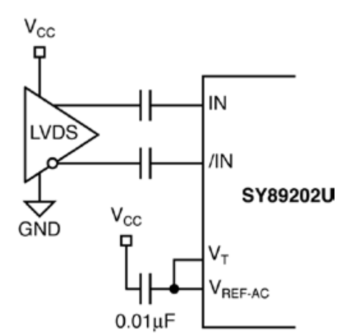


Figure 3f. LVDS Interface (AC-Coupled)

LVPECL Output Interface Applications

LVPECL has high input impedance, and very low output impedance (open emitter), and small signal swing which results in low EMI. LVPECL is ideal for driving 50Ω- and 100Ω-controllled impedance transmission lines. There are several techniques for terminating the LVPECL output: Parallel Termination-Thevenin Equivalent, Parallel Termination (3-resistor), and AC-Coupled Termination. Unused output pairs may be left floating. However, single-ended outputs must be terminated, or balanced.

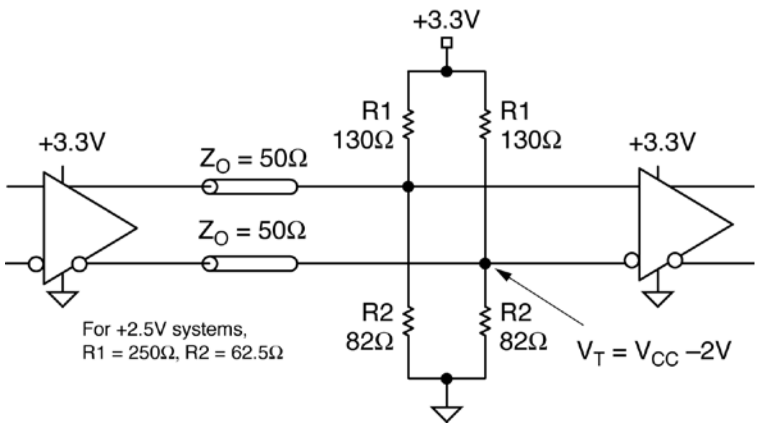


Figure 4. Parallel Termination-Thevenin Equivalent

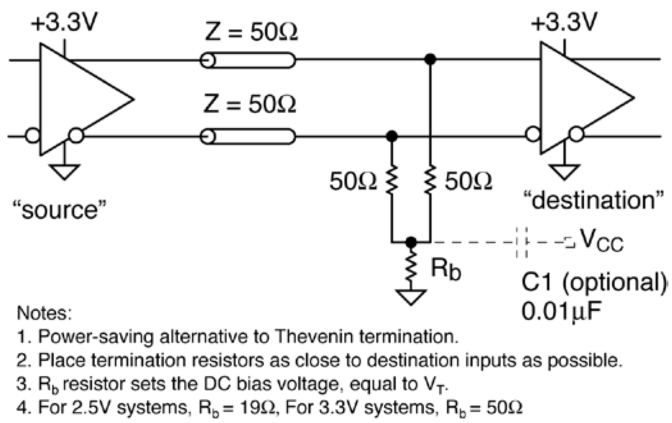
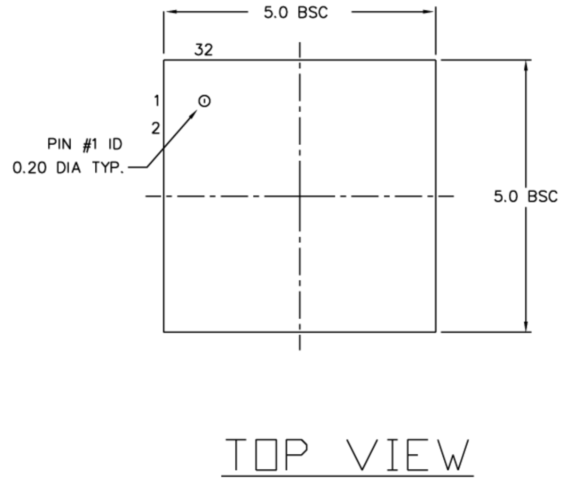


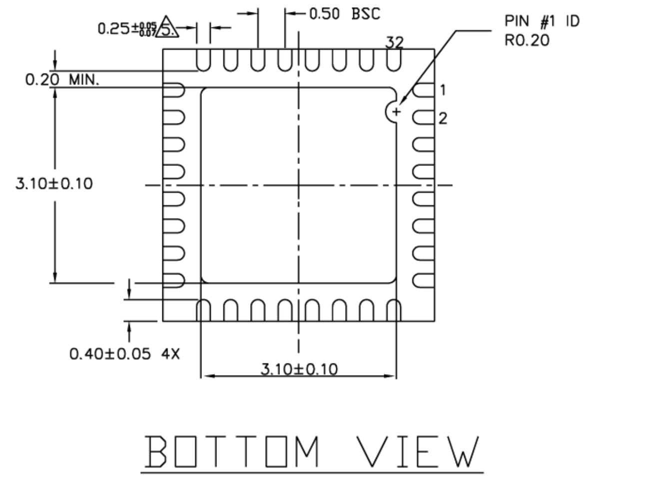
Figure 5. Parallel Termination (3-Resistor)

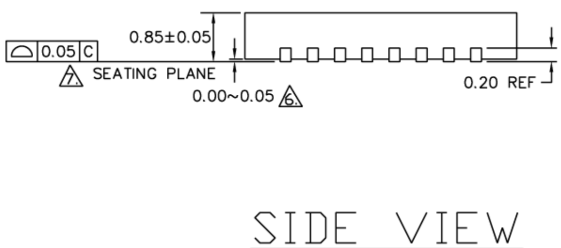
Related Product and Support Documentation

Part Number	Function	Datasheet Link
SY89200U	Ultra-Precision 1:8 LVDS Fanout with Three ÷1/÷2/÷4 Clock Divider Output Banks	http://www.micrel.com/_PDF/HBW/sy89200u.pdf#page=1
HBW Solutions	New Products and Applications	http://www.micrel.com/page.do?page=/product-info/as/HBWsolutions.shtml

Package Information







NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
5. DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
6. APPLIED ONLY FOR TERMINALS.
7. APPLIED FOR EXPOSED PAD AND TERMINALS.

32-Pin QFN

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