SY89221U

Precision 1:15 LVPECL Fanout Buffer with 2:1 MUX and Four ÷1/÷2/÷4 Clock Divider Output Banks

General Description

The SY89221U is a 2.5/3.3V precision, high-speed, integrated clock divider and LVPECL fanout buffer capable of handling clocks up to 1.5GHz. Optimized for communications applications, the four independently controlled output banks are phase-matched and can be configured for pass through ÷1, ÷2 or ÷4 divider ratios.

The differential input includes Micrel's unique, 3-pin input termination architecture that allows the user to interface to any differential signal (AC- or DC-coupled) as small as 100mV ($200mV_{PP}$) without any level shifting or termination resistor networks in the signal path. The low-skew, low-jitter outputs are LVPECL compatible with extremely fast rise/fall times that are guaranteed to be less than 220ps.

The /MR (master reset) input asynchronously resets the outputs. A four-clock delay after de-asserting /MR allows the counters to synchronize and start the outputs from the same state without any runt pulse.

The SY89221U is part of Micrel's Precision Edge® product family. All support documentation can be found at Micrel's web site at: www.micrel.com.

Features

- Four low-skew LVPECL output banks with independently programmable ÷1, ÷2 and ÷4 divider options
- Four output banks, 15 total outputs
- Guaranteed AC performance over temperature and voltage:
  - Accepts a clock frequency up to 1.5GHz
  - <1600ps IN-to-OUT propagation delay
  - <270ps rise/fall time
  - <35 ps within-bank skew
- Fail Safe Input
  - Prevents outputs from oscillating
- Ultra-low jitter design:
  - $<1ps_{RMS}$ random jitter
  - $<10ps_{PP}$ total jitter (clock)
- Patent-pending input termination and VT pin accepts DC- and AC-coupled inputs (CML, PECL, LVDS)
- CMOS/TTL-compatible output enable (EN) and divider select control
- 2.5V ±5% or 3.3V ±10% power supply
- –40°C to +85°C temperature range
- Available in 64-pin TQFP

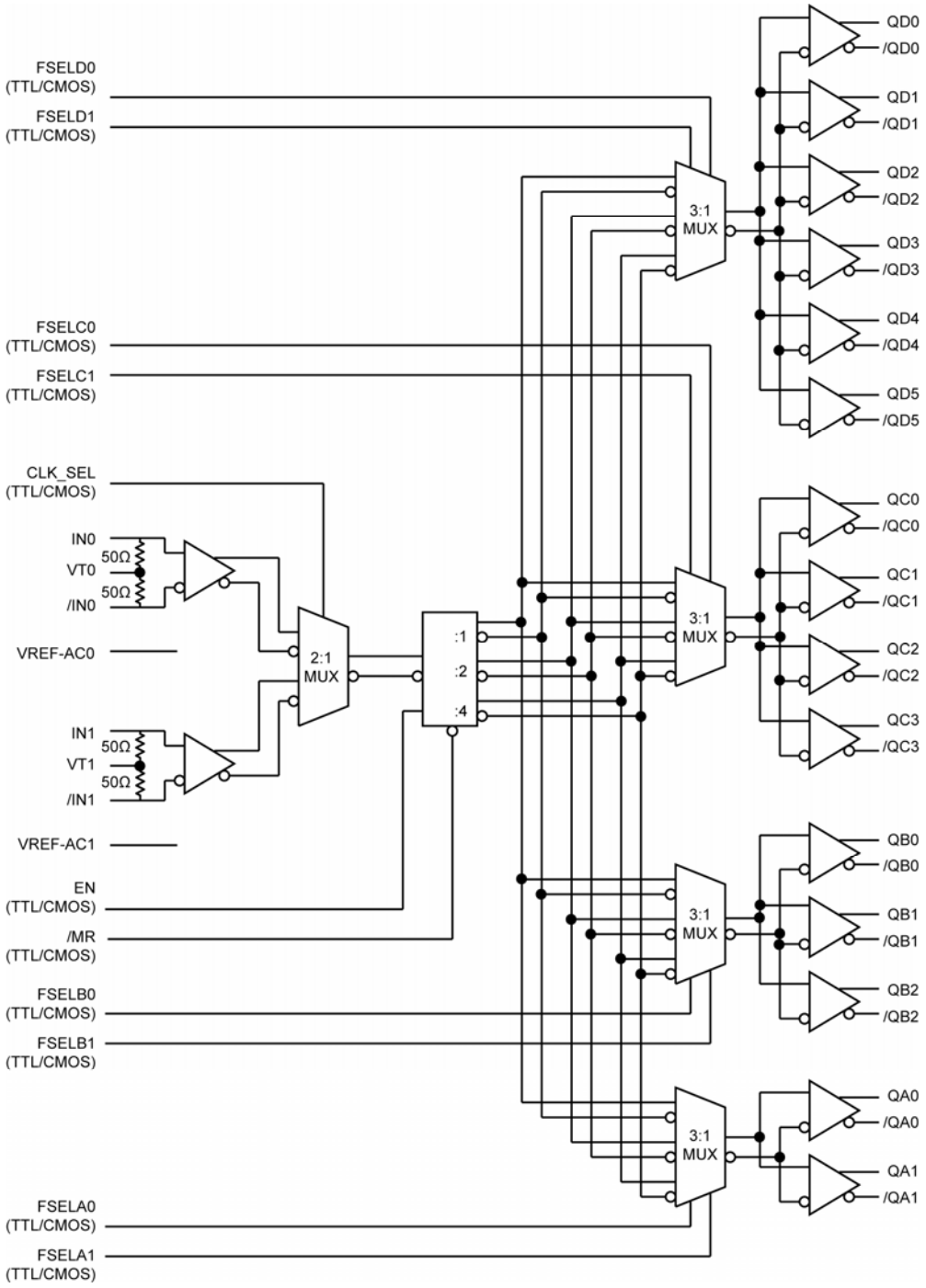
Applications

- All SONET/SDH applications
- All Fibre Channel applications
- All Gigabit Ethernet applications

Markets

- LAN/WAN routers/switches
- Enterprise servers
- Storage
- ATE
- Test and measurement

Functional Block Diagram



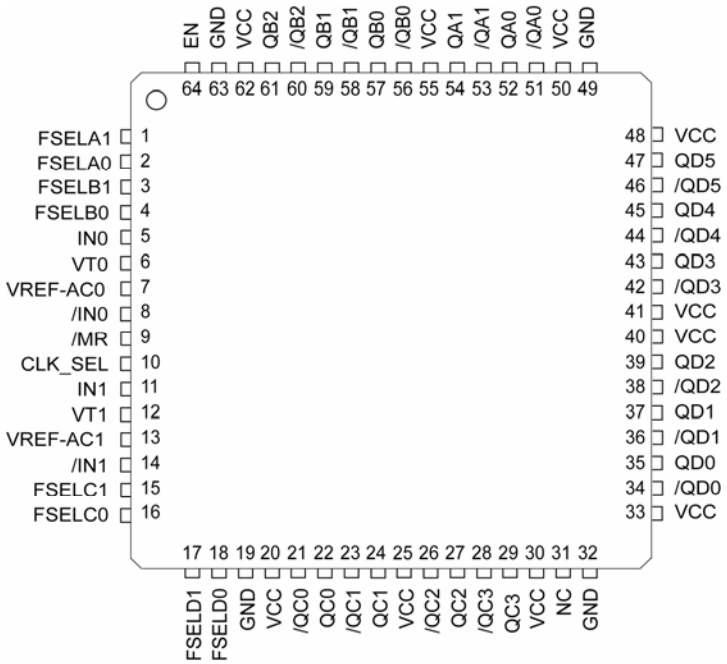
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89221UHY	T64-1	Industrial	SY89221UHY with Pb-Free bar-line indicator	Pb-Free Matte-Sn
SY89221UHYTR[2]	T64-1	Industrial	SY89221UHY with Pb-Free bar-line indicator	Pb-Free Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.

Pin Configuration



64-Pin EPAD-TQFP (T64-1)

Pin Description

Pin Number	Pin Name	Pin Function
1, 2 3, 4 15, 16 17, 18	FSELA1, FSELA0 FSELB1, FSELB0 FSELC1, FSELC0 FSELD1, FSELD0	Single-Ended Inputs: These TTL/CMOS inputs select the divide ratio for each of the four banks of outputs. Note that each of these inputs is internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open. The input-switching threshold is $V_{CC}/2$.
5, 8, 11, 14	IN0, /IN0 IN1, /IN1	Differential Inputs: These input pairs are the differential signal inputs to the device. They accept AC- or DC-coupled signals as small as 100mV. The input pairs internally terminate to a VT pin through 50Ω. Note that these inputs will default to an indeterminate state if left open. Please refer to the “Input Interface Applications” section for more details.
6, 12	VT0, VT1	Input Termination Center-Tap: Each side of a differential input pair terminates to a VT pin. The VT pin provides a center-tap to a termination network for maximum interface flexibility. See “ Input Interface Applications” section for more details.
7, 13	VREF-AC0, VREF-AC1	Reference Voltage: These outputs bias to V_{CC}–1.2V. They are used for AC-coupling inputs IN and /IN. Connect VREF-AC directly to the corresponding VT pin. Bypass with 0.01µF low ESR capacitor to VCC. Due to limited drive capability, the VREF-AC pin is only intended to drive its respective VT pin. Maximum sink/source current is ±1.5mA. Please refer to the “Input Interface Applications” section for more details.
9	/MR	Single-Ended Input: This TTL/CMOS-compatible master reset function asynchronously sets the true outputs LOW, complimentary outputs HIGH, and holds them in that state as long as /MR remains LOW. This input is internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state if left open. The input-switching threshold is $V_{CC}/2$.
10	CLK_SEL	Single-Ended Input: This TTL/CMOS-compatible input selects the inputs to the multiplexer. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state if left open. The input-switching threshold is $V_{CC}/2$.
20, 25, 30, 33, 40 41, 48, 50, 55, 62	VCC	Positive Power Supply. Bypass with 0.1µF||0.01µF low ESR capacitor as close to V_{CC} pin as possible.
21, 22 23, 24 26, 27 28, 29	/QC0, QC0 /QC1, QC1 /QC2, QC2 /QC3, QC3	Bank C LVPECL differential output pairs controlled by FSELC0 and FSELC1. Refer to “Function Table” for details. Unused output pairs may be left open. Each output is designed to drive 800mV into 50Ω terminated to V_{CC} – 2V.
31	NC	No connect.
34, 35, 36, 37 38, 39, 42, 43 44, 45, 46, 47	/QD0, QD0 /QD1, QD1 /QD2, QD2 /QD3, QD3 /QD4, QD4 /QD5, QD5	Bank D LVPECL differential output pairs controlled by FSELD0 and FSELD1. Refer to “Function Table” for details. Unused output pairs may be left open. Each output is designed to drive 800mV into 50Ω terminated to V_{CC} – 2V.
51, 52 53, 54	/QA0, QA0 /QA1, QA1	Bank A LVPECL differential output pairs controlled by FSELA0 and FSELA1. Refer to “Function Table” for details. Unused output pairs may be left open. Each output is designed to drive 800mV into 50Ω terminated to V_{CC} – 2V.
56, 57 58, 59 60, 61	/QB0, QB0 /QB1, QB1 /QB2, QB2	Bank B LVPECL differential output pairs controlled by FSELB0 and FSELB1. Refer to “Function Table” for details. Unused output pairs may be left open. Each output is designed to drive 800mV into 50Ω terminated to V_{CC} – 2V.

Pin Description (continued)

Pin Number	Pin Name	Pin Function
64	EN	Single-Ended Input: This TTL/CMOS input disables and enables the outputs. It is internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state if left open. When disabled, true outputs go LOW and complementary outputs switches to HIGH. The input switching threshold is $V_{CC}/2$. For the input enable and disable functional description, refer to Figures 2d and 2e.
19, 32, 49, 63	GND, Exposed Pad	Ground and exposed pad must be connected to the same GND plane on the board.

Function Table

/MR[1]	EN[2, 3]	CLK_SEL	FSELx0[4]	FSELx1[4]	Q
1	1	0	0	0	IN0÷1
1	1	1	0	0	IN1÷1
1	1	0	1	0	IN0÷2
1	1	1	1	0	IN1÷2
1	1	0	X	1	IN0÷4
1	1	1	X	1	IN1÷4
1	0	X	X	X	0
0	X	X	X	X	0

Notes:

1. /MR asynchronously forces Q LOW (/Q HIGH).
2. EN forces Q LOW between 2 and 6 input clock cycles after the falling edge of EN. Refer to “Timing Diagram” section.
3. EN synchronously enables the outputs between two and six input clock cycles after the rising edge of EN. Refer to “Timing Diagram” section.
4. FSEL valid for each of the banks A, B, C, and D. Banks can be programmed independent of each other.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
Termination Current
  Source or sink current on V_T ..... ±100mA
LVPECL Output Current (I_{OUT})
  Continuous 50mA
  Surge 100mA
Input Current
  Source or sink current on IN, /IN ..... ±50mA
V_{REF-AC} Current[3]
  Source or sink current on V_{REF-AC} ..... ±2mA
Lead Temperature (soldering, 20sec.) ..... 260°C
Storage Temperature (T_s) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{IN}) ..... +2.375V to +2.625V or
..... +3.0V to 3.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance[4]
  TQFP
    Still-air (θ_{JA}) ..... 35°C/W
    Junction-to-board (ψ_{JB}) ..... 20°C/W

DC Electrical Characteristics[5]

V_{CC} = +2.5V ±5% or 3.3V ±10%, T_A = –40°C to +85°C unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Positive Supply Voltage Range		2.375 3.0		2.625 3.6	V
I_{CC}	Power Supply Current			140	190	mA
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
R_{IN}	Input Resistance (IN-to-V_T, /IN-to-V_T)		45	50	55	Ω
V_{IH}	Input HIGH Voltage (IN, /IN)		1.2		V_{CC}	V
V_{IL}	Input LOW Voltage (IN, /IN)		0		V_{IH}–0.1	V
V_{IN}	Input Voltage Swing (IN, /IN)	See Figure 1a; Note 6	0.1		2.5	V
V_{DIFF_IN}	Differential Input Voltage Swing |IN – /IN|	See Figure 1b	0.2			V
V_{IN_FSI}	Input Voltage Threshold that Triggers FSI			30	100	mV
V_{REF-AC}	Reference Voltage		V_{CC}–1.3	V_{CC}–1.2	V_{CC}–1.1	V
V_{T_IN}	Voltage from Input to V_T				1.28	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to the limited drive capability use for input of the same package only.
4. ψ_{JB} and θ_{JA} values are determined for a 4-layer board in still-air number, unless otherwise stated.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. V_{IN}(max) is specified when V_T is floating.

LVTTL/CMOS DC Electrical Characteristics[7]

V_{CC} = +2.5V ±5% or 3.3V ±10%, T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current		–125		30	µA
I_{IL}	Input LOW Current		-300			µA

LVPECL Outputs DC Electrical Characteristics[7]

V_{CC} = +2.5V ±5% or 3.3V ±10%, T_A = –40°C to +85°C, R_L = 50Ω to V_{CC}–2V, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output Voltage HIGH (Q, /Q)		V_{CC} -1.145		V_{CC} - 0.895	V
V_{OL}	Output Voltage LOW (Q, /Q)		V_{CC} -1.945		V_{CC} -1.695	V
V_{OUT}	Output Voltage Swing (Q, /Q)	See Figure 1a	550	800		mV
V_{DIFF_OUT}	Differential Output Voltage Swing |Q – /Q|	See Figure 1b	1100	1600		mV

Note:

7. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics[8]

V_{CC} = +2.5V ±5% or 3.3V ±10%, T_A = –40°C to +85°C, R_L = 50Ω to V_{CC}–2V, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	V_{OUT} ≥ 400mV	1.5	2.0		GHz
t_{PD}	Differential Propagation Delay	IN-to-Q	800	1250	1600	ps
		CLK_SEL-to-Q	700	1000	1400	ps
		/MR(H-L)-to-Q	700	1000	1400	ps
t_{RR}	Reset Recovery Time	/MR (L-H)-to-IN	300			ps
t_{PD} Tempco	Differential Propagation Delay Temperature Coefficient			225		fs/°C
t_{SKEW}	Within-Bank Skew	Within same fanout bank[9, 10]		10	35	ps
	Bank-to-Bank Skew	Same divide setting[11]		15	40	ps
	Bank-to-Bank Skew	Different divide setting[11]		25	60	ps
	Part-to-Part Skew	Note 12			400	ps
t_{JITTER}	Random Jitter (RJ)	Note 13			1	ps_{RMS}
	Total Jitter (TJ)	Note 14			10	ps_{PP}
	Cycle-to-Cycle Jitter	Note 15			1	ps_{RMS}
t_r, t_f	Output Rise/Fall Time (20% to 80%)	At full output swing	120	180	270	ps
	Duty Cycle	Divide-by-2 or Divide-by-4	47		53	%
		Divide-by-1, input > 1GHz	45		55	
		Divide-by-1, input < 1GHz	47		53	

Notes:

8. Measured with 100mV input swing. See “Timing Diagrams” section for definition of parameters. High-frequency AC-parameters are guaranteed by design and characterization.
9. Within-bank skew is the difference in propagation delays among the outputs within the same bank.
10. Skews within banks depend on the number of outputs. Within-bank skew decreases if the bank has lesser outputs.
11. Bank-to-bank skew is the difference in propagation delays between outputs from different banks. Bank-to-bank skew is also the phase offset between each bank, after MR is applied.
12. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
13. Random jitter is measured with a K28.7 comma detect character pattern.
14. Total jitter definition: with an ideal clock input frequency ≤ f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.
15. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, T_n–T_{n-1} where T is the time between rising edges of the output signal.

Functional Description

Clock Select (CLK_SEL)

CLK_SEL is an asynchronous TTL/CMOS compatible input that selects one of the two input signals. Internal 25kΩ pull-up resistor defaults the input to logic HIGH if left open. Delay between the clock selection and multiplexer selecting the correct input signal depends on the divider settings. The delay varies due to the asynchronous nature of the input. Input switching threshold is $V_{CC}/2$. Refer to Figure 2a.

Fail-Safe Input (FSI)

The input includes a special failsafe circuit to sense the amplitude of the input signal and to latch the outputs when there is no input signal present, or when the amplitude of the input signal drops sufficiently below $100mV_{PK}$ ($200mV_{PP}$), typically $30mV_{PK}$. Maximum frequency of the SY89221U is limited by the FSI function. Refer to Figure 2b.

Input Clock Failure Case

If the input clock fails to a floating, static, or extremely low signal swing, the FSI function will eliminate a metastable condition and guarantee a stable output signal. No ringing and no undetermined state will occur at the output under these conditions.

Please note that the FSI function will not prevent duty cycle distortion in case of a slowly deteriorating (but still toggling) input signal. Due to the FSI function, the propagation delay will depend on rise and fall time of the input signal and on its amplitude. Refer to “Typical Operating Characteristics” for detailed information.

Master Reset (/MR)

/MR is a TTL/CMOS compatible input that resets the output signals. Internal 25kΩ pull-up resistor defaults the input to logic HIGH if left open. A LOW input to /MR asynchronously sets the true outputs LOW and complimentary outputs HIGH. The outputs will remain in this state until /MR is forced HIGH. Input switching threshold is $V_{CC}/2$. Refer to Figure 2c.

Enable Outputs (EN)

EN is a synchronous TTL/CMOS compatible input that enables/disables the outputs based on the input to this pin. Internal 25kΩ pull-up resistor defaults the input to logic HIGH if left open. A logic LOW input causes the true outputs to go LOW and complementary outputs to go HIGH. It takes 2 to 6 input clock cycles before the outputs are enabled/disabled because the signals are going through a series of flip-flops. Input switching threshold is $V_{CC}/2$. Refer to Figure 2d and 2e.

Single-Ended and Differential Swings

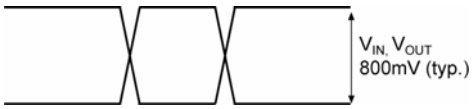


Figure 1a. Single-Ended Voltage Swing

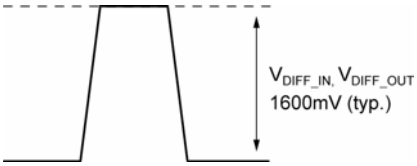


Figure 1b. Differential Voltage Swing

Timing Diagrams

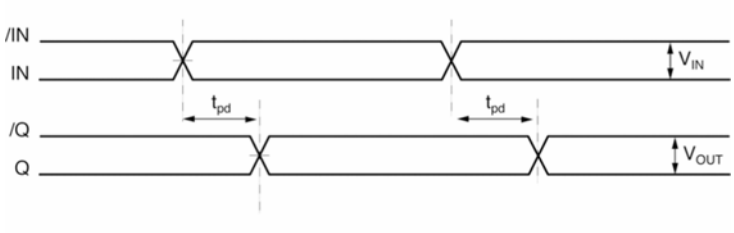


Figure 2a. Propagation Delay

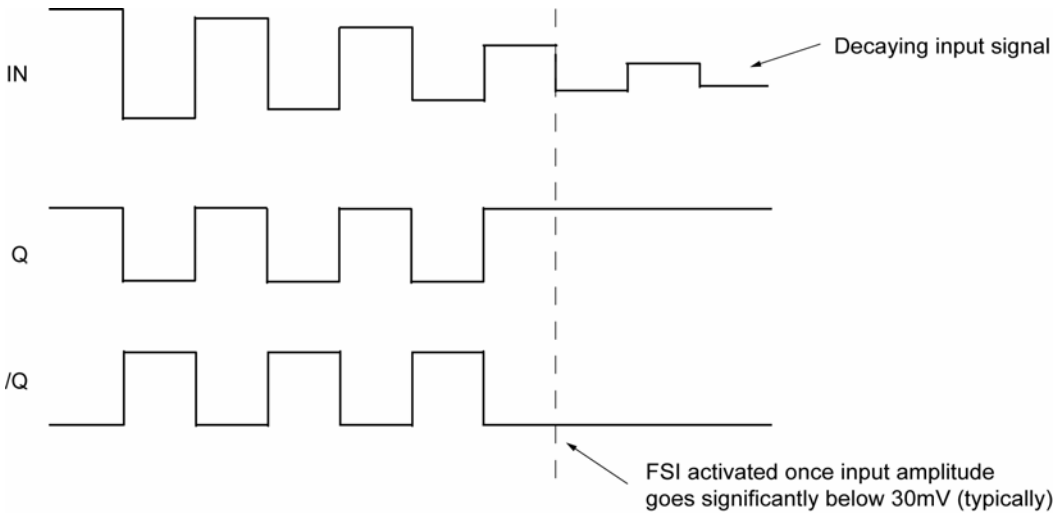


Figure 2b. Fail Safe Feature

Timing Diagrams

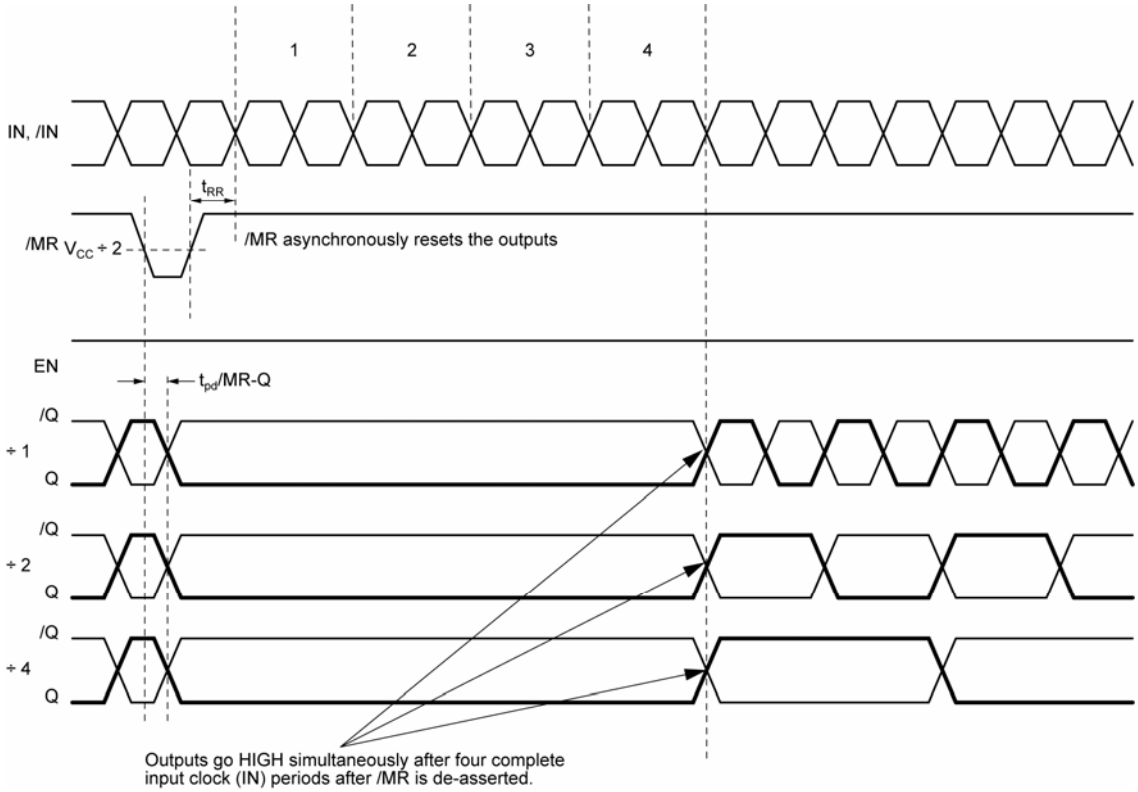


Figure 2c. Reset with Output Enabled

Timing Diagrams

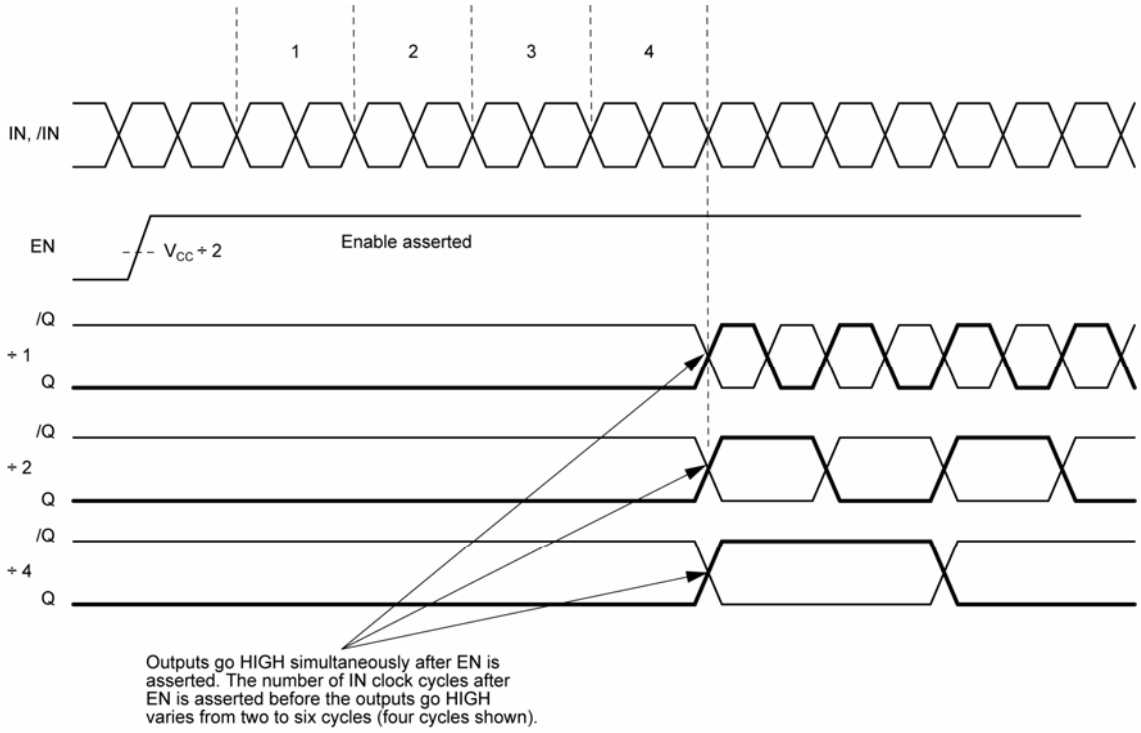


Figure 2d. Enable Timing

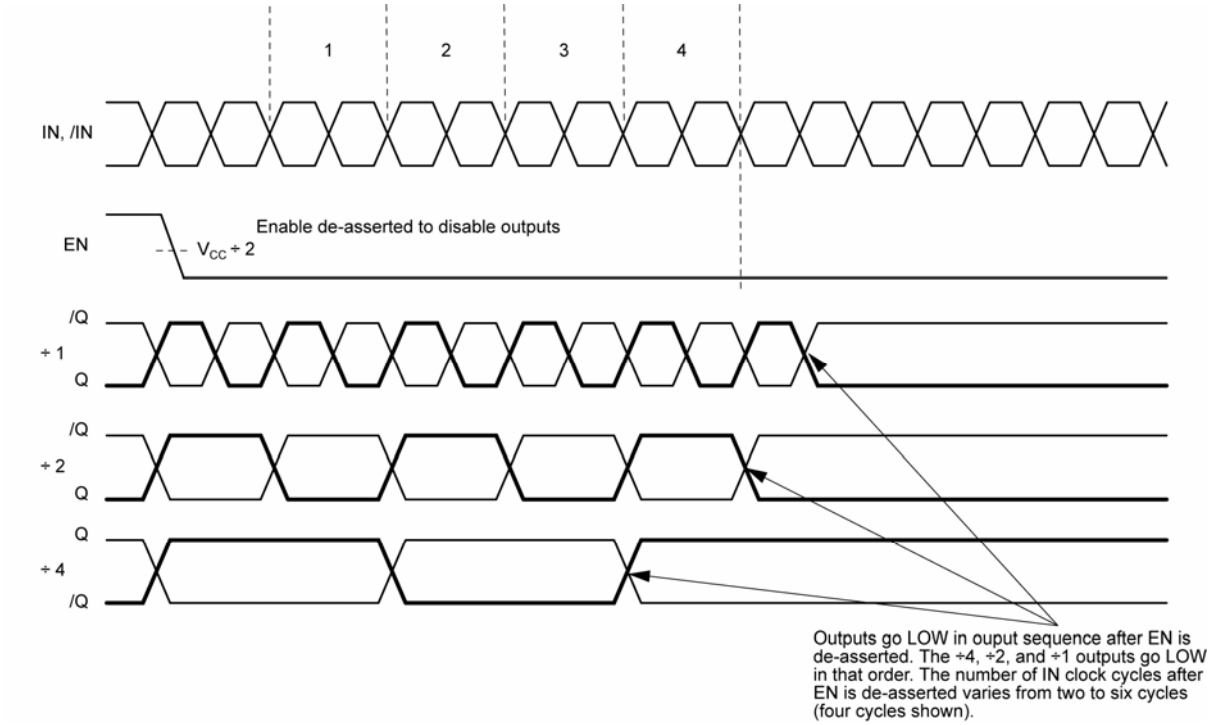
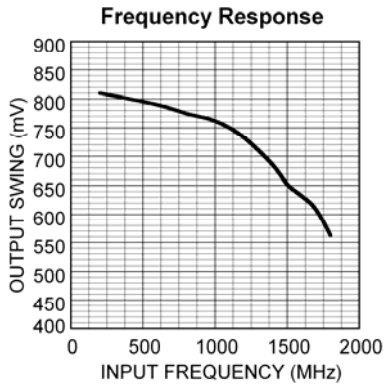
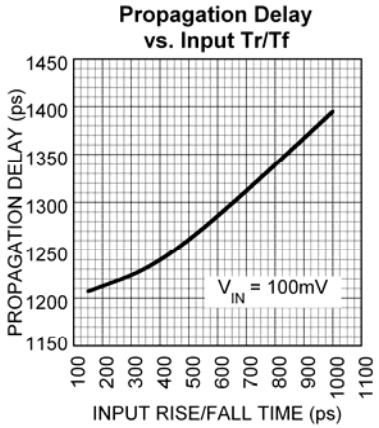


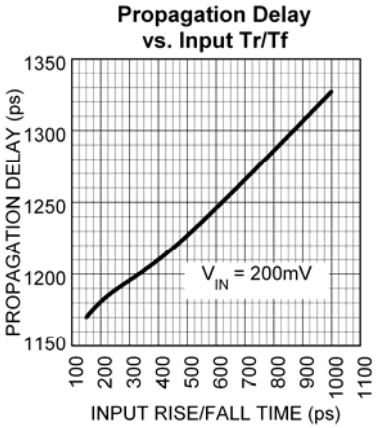
Figure 2e. Disable Timing

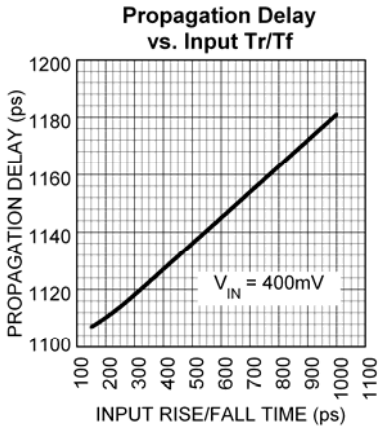
Typical Operating Characteristics

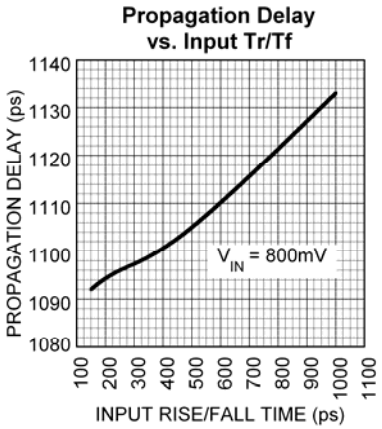
V_{CC} = 3.3V, GND = 0V, V_{IN} = 100mV, R_L = 50Ω to V_{CC}-2V, T_A = 25°C, unless otherwise stated.







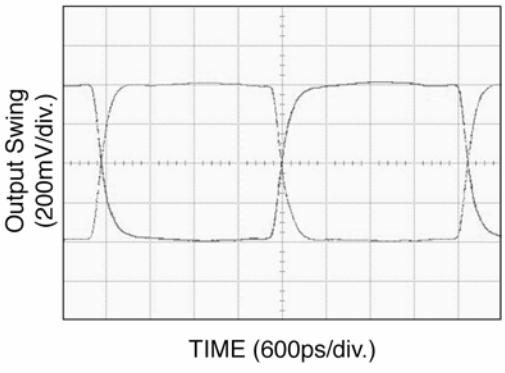




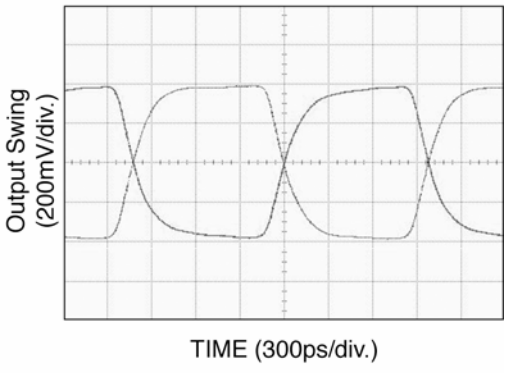
Functional Characteristics

V_{CC} = 3.3V, GND = 0V, V_{IN} = 100mV, R_L = 50Ω to V_{CC}-2V, T_A = 25°C, unless otherwise stated.

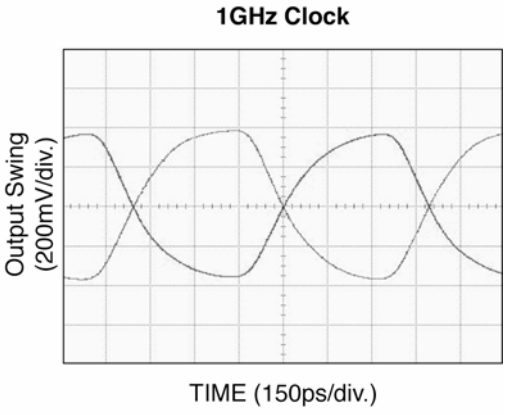
200MHz Clock



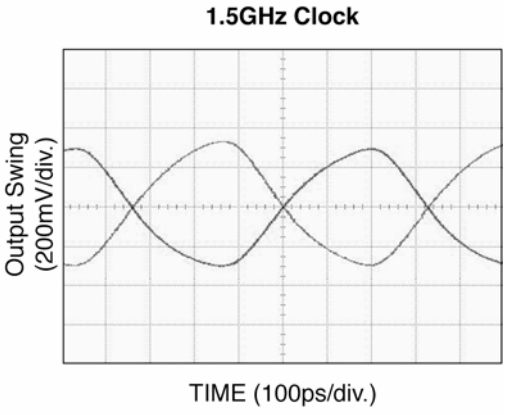
500MHz Clock



1GHz Clock



1.5GHz Clock



Input and Output Stages

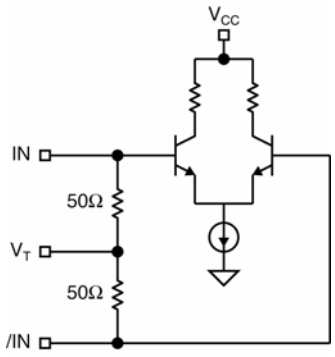


Figure 3a. Simplified Differential Input Stage

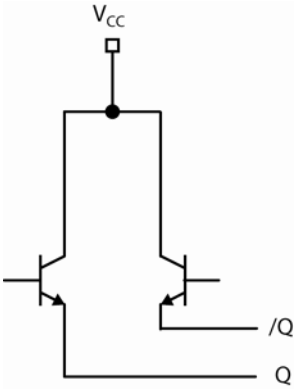


Figure 3b. Simplified Differential Output Stage

Input Interface Applications

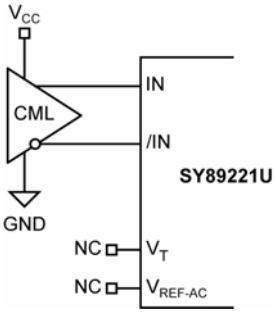


Figure 4a. CML Interface (DC-Coupled)
May connect V_T to V_{CC}

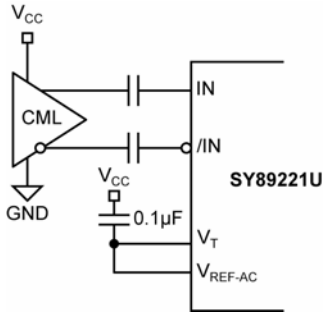


Figure 4b. CML Interface (AC-Coupled)

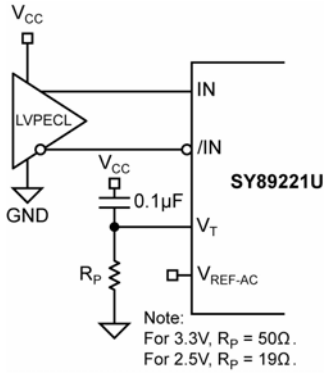


Figure 4c. LVPECL Interface (DC-Coupled)

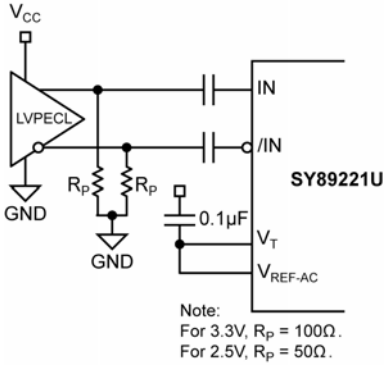


Figure 4d. LVPECL Interface (AC-Coupled)

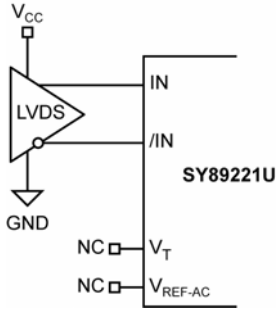


Figure 4e. LVDS Interface

LVPECL Output Interface Applications

LVPECL has high input impedance, and very low output impedance (open emitter), and small signal swing which results in low EMI. LVPECL is ideal for driving 50Ω- and 100Ω-controlled impedance transmission lines. There are several techniques for terminating the LVPECL output: Parallel Termination-Thevenin Equivalent, Parallel Termination (3-resistor), and AC-coupled Termination. Unused output pairs may be left floating. However, single-ended outputs must be terminated, or balanced.

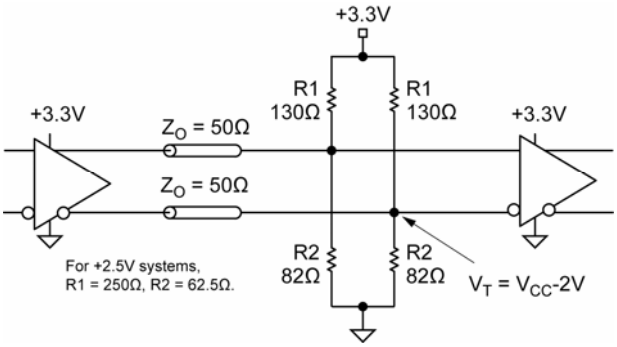


Figure 5a. Parallel Termination-Thevenin Equivalent

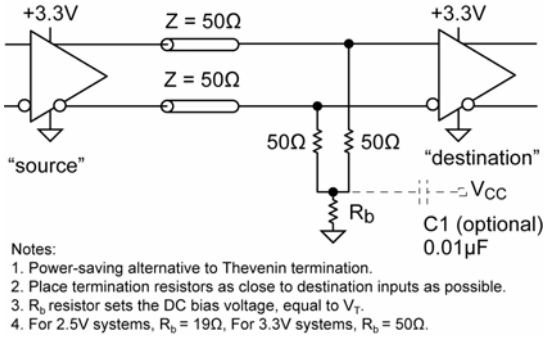
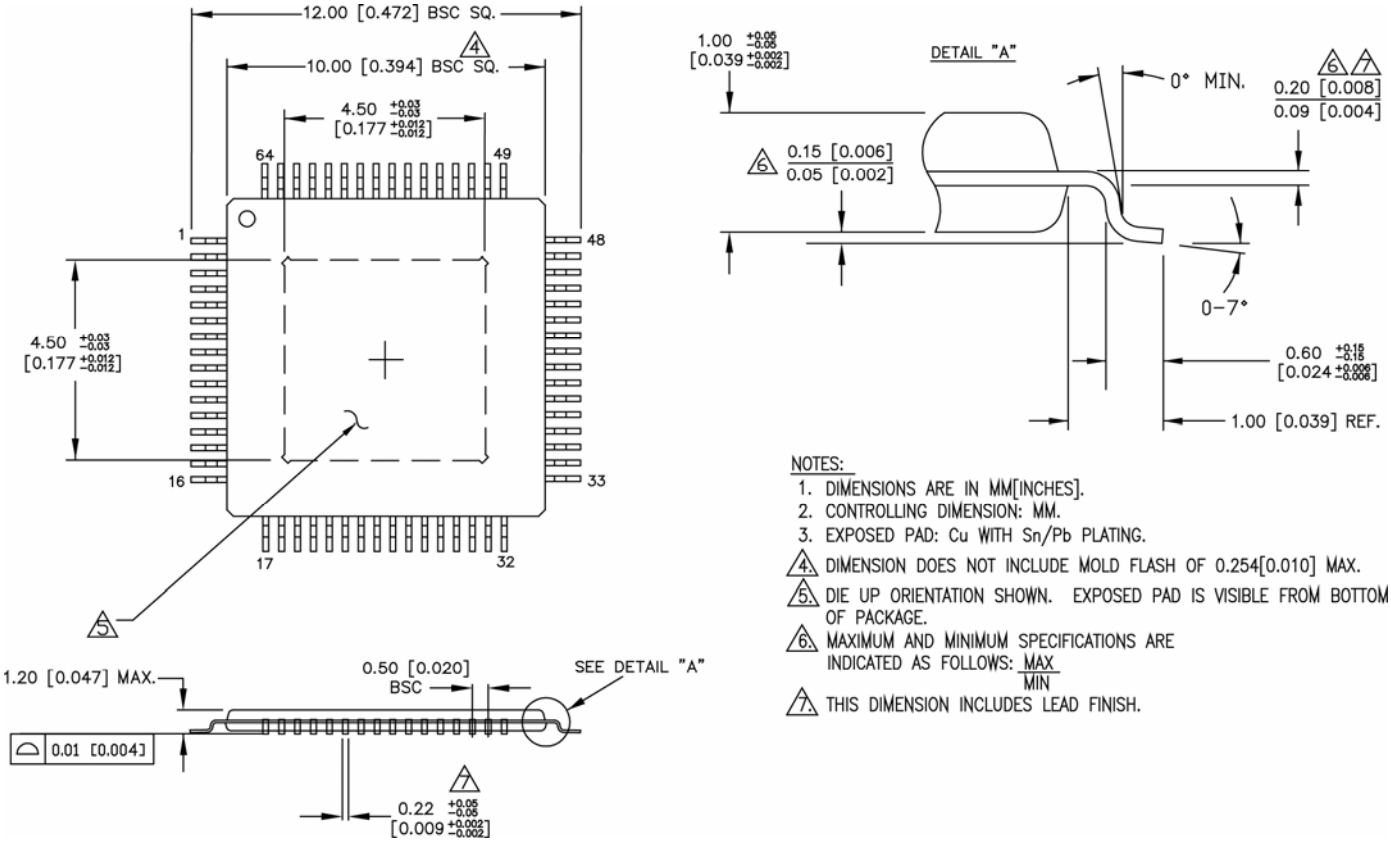


Figure 5b. Parallel Termination (3-Resistor)

Related Product and Support Documentation

Part Number	Function	Data Sheet Link
SY89218U	Precision 1:15 LVDS Fanout Buffer with 2:1 MUX and Four ÷1/÷2/÷4 Clock Divider Output Banks	http://www.micrel.com/_PDF/HBW/sy89218u.pdf
SY89200U	Ultra-Precision 1:8 LVDS Fanout with Three ÷1/÷2/÷4 Clock Divider Output Banks	http://www.micrel.com/_PDF/HBW/sy89200u.pdf
SY89202U	Ultra-Precision 1:8 LVPECL Fanout with Three ÷1/÷2/÷4 Clock Divider Output Banks	http://www.micrel.com/_PDF/HBW/sy89202u.pdf
HBW Solutions	New Products and Applications	http://www.micrel.com/page.do?page=/product-info/as/HBWsolutions.shtml

Package Information



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