3.3V/5V 1.5Gbps DIFFERENTIAL CML/PECL/LVPECL-to-LVDS TRANSLATOR

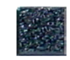
Precision Edge®
SY89325V

FEATURES

- Guaranteed AC performance over temp and voltage:
  - DC-to >1.5Gbps data rate throughput
  - >750MHz clock f_{MAX}
  - <50ps within-device skew
- Ultra-low jitter design:
  - <1ps_{RMS} random jitter
  - <10ps_{PP} deterministic jitter
  - <1ps_{RMS} cycle-to-cycle jitter
  - <10ps_{PP} total jitter (clock)
- Accepts CML, PECL, LVPECL inputs
- 350mV LVDS output swing
- Power supply 3.3V ±10% or 5.0V ±10%
- –40°C to +85°C temperature range
- Available in ultra-small (2mm × 2mm) 8-pin MLF® package

APPLICATIONS

- High-speed logic
- Data communications systems
- Wireless communications systems
- Telecom systems



Precision Edge®

DESCRIPTION

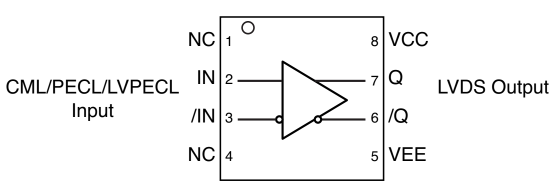
The SY89325V is a fully differential, CML/PECL/LVPECL-to-LVDS translator. It achieves LVDS signaling up to 1.5Gbps and clock rates of 750MHz, depending of the distance and the characteristics of the media and noise coupling sources. LVDS is intended to drive 50Ω impedance transmission line media such as PCB traces, backplanes, or cables.

SY89325V inputs can be terminated with a single resistor between the true and complement pins of the input.

The SY89325V is a member of Micrel's Precision Edge® family of high-speed logic devices. This family features ultra-small packaging, high signal integrity, and operation at many different supply voltages. For applications that require dual translators, consider the SY55855V.

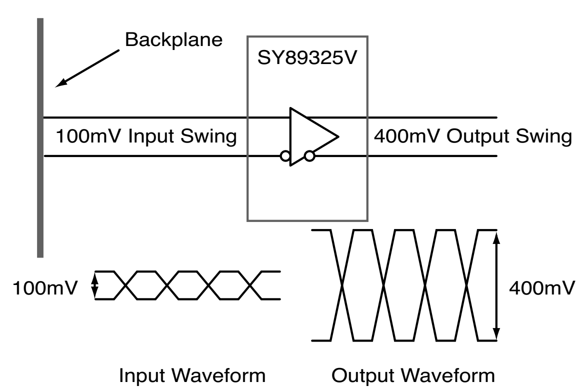
All support documentation can be found on Micrel's web site at www.micrel.com.

FUNCTIONAL BLOCK DIAGRAM



8-Pin MLF® (2mm × 2mm)

TYPICAL APPLICATIONS CIRCUIT



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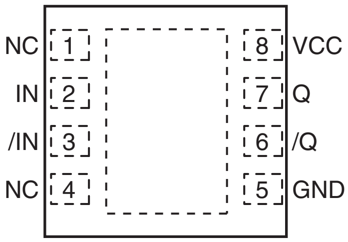
*Micro*LeadFrame and MLF are registered trademarks of Amkor Technology, Inc.

PACKAGE/ORDERING INFORMATION



8-Pin MLF® (MLF-8)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89325VMITR	MLF-8	Industrial	325	Sn-Pb
SY89325VMGTR(1)	MLF-8	Industrial	325 with Pb-Free bar-line indicator	Pb-Free NiPdAu

Note:

1. Pb-Free package is recommended for new designs.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
2, 3	IN, /IN	Differential Inputs: These input pairs are the differential signal inputs to the device. These inputs accept AC- or DC-coupled signals as small as 100mV. External termination is required.
8	VCC	Positive power supply. Bypass with 0.1µF||0.01µF low ESR capacitors.
7, 6	Q, /Q	Differential LVDS Output: This output is the output of the device. Terminate with 100Ω across the pair. See "Output Interface Applications" section.
5	GND, Exposed	Ground. Ground pin and exposed pad must be connected to the same ground plane.
1, 4	NC	No connect.

Absolute Maximum Ratings(1)

Supply Voltage (V_{CC}) .... –0.5V to + 6.0V
Input Voltage (V_{IN}) .... –0.5V to V_{CC} +0.5V
Input Current
Source or sink current on IN, /IN .... ±50mA
CML Output Voltage (V_{OUT}) .... V_{CC}–1.0V to V_{CC}+0.5V
Lead Temperature (soldering, 20 sec.) .... +260°C
Storage Temperature (T_S) .... –65°C to +150°C

Operating Ratings(2)

Supply Voltage (V_{CC}) .... +3.0V to +3.6V
.... +4.5V to +5.0V
Ambient Temperature (T_A) .... –40°C to +85°C
Package Thermal Resistance(3)
MLF® (θ_{JA})
Still-Air .... 93°C/W
MLF® (Ψ_{JB})
Junction-to-board .... 60°C/W

DC ELECTRICAL CHARACTERISTICS(4)

T_A = –40°C to +85°C; unless stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply		3.0	3.3	3.6	V
			4.5	5.0	5.7	V
I_{CC}	Power Supply Current	$V_{CC} \le 3.6V$			50	mA
		$3.6V \le V_{CC} \le 5.7V$			80	mA

INPUT DC ELECTRICAL CHARACTERISTICS(4)

V_{CC} = 3.3V ±10% or 5.0V ±10%; T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage (IN, /IN)		1.6		V_{CC}	V
V_{IL}	Input LOW Voltage (IN, /IN)		1.5		V_{CC} –0.1	V
V_{IN}	Input Voltage Swing (IN, /IN)	See Figure 1a.	100			mV
V_{DIFF_IN}	Differential Input Voltage Swing |IN - /IN|	See Figure 1b.	200			mV

LVDS OUTPUT DC ELECTRICAL CHARACTERISTICS(4)

V_{CC} = 3.3V ±10% or 5.0V ±10%; T_A = –40°C to +85°C; R_L = 100Ω across output pair, or equivalent, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	I_{OH} = –4.0mA			1.474	V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0mA	0.925			V
V_{OCM}	Output Common Mode Voltage		1.125		1.375	V
ΔV_{OCM}	Change in Common Mode Voltage		–50		+50	mV
V_{OUT}	Output Voltage Swing		250	350		mV
$V_{DIFF-OUT}$	Differential Output Voltage Swing		500	700		mV

Notes:

1. Permanent device damage may occur if ratings in the “Absolute Maximum Ratings” section are exceeded. This is a stress rating only and functional operation is not implied for conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device’s most negative potential on the PCB. Ψ_{JB} uses 4-layer θ_{JA} in still-air unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS(5)

V_{CC} = 3.3V ±10% or 5.0V ±10%; T_A = –40°C to +85°C; output loaded with 100Ω across the output pair, or equivalent unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	V_{OUT} ≥ 200mV NRZ Data	1.5			Gbps
		Clock		750		MHz
t_{pd}	Propagation Delay IN-to-Q	V_{IN} ≥ 100mV	300		700	ps
t_{JITTER}	Random Jitter (RJ)	**Note 6**			1	ps_{RMS}
	Deterministic Jitter (DJ)	**Note 7**			10	ps_{PP}
	Cycle-to-Cycle Jitter	**Note 8**			1	ps_{RMS}
	Total Jitter (TJ)	**Note 9**			10	ps_{PP}
t_r, t_f	Rise / Fall Time (20% to 80%) Q, /Q	At full output swing.	100		300	ps

Notes:

5. Measured with 100mV input swing. See "Timing Diagrams" section for definition of parameters. High-frequency AC-parameters are guaranteed by design and characterization.
6. Random jitter is measured with a K28.7 comma detect character pattern, measured at 1.5Gbps.
7. Deterministic jitter is measured at f_{MAX}, with both K28.5 and 2^{23} –1 PRBS pattern
8. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, $T_n – T_{n–1}$ where T is the time between rising edges of the output signal.
9. Total jitter definition: with an ideal clock input of frequency ≤ f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

SINGLE-ENDED AND DIFFERENTIAL SWINGS

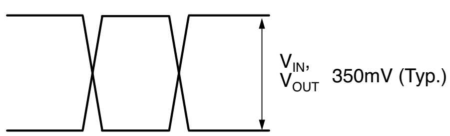


Figure 1a. Single-Ended Voltage Swing

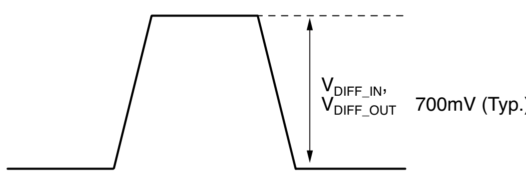


Figure 1b. Differential Voltage Swing

TIMING DIAGRAM

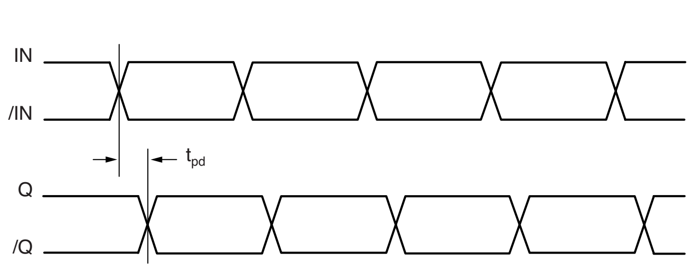
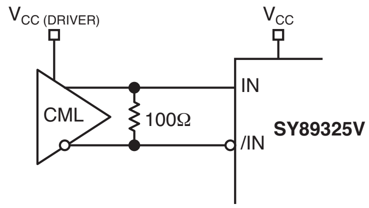


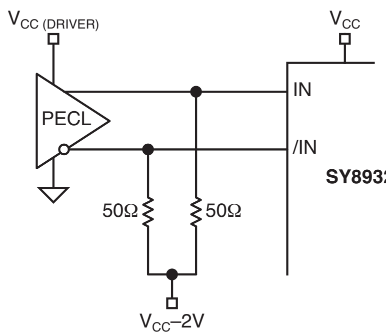
Figure 2. Timing Diagram

INPUT INTERFACE APPLICATIONS



Note: V_{CC} of SY89325V must be ≥ $V_{CC\ (DRIVER)}$

Figure 3. CML-DC Coupled



Note: V_{CC} of SY89325V must be ≥ $V_{CC\ (DRIVER)}$

Figure 4. PECL-DC Coupled

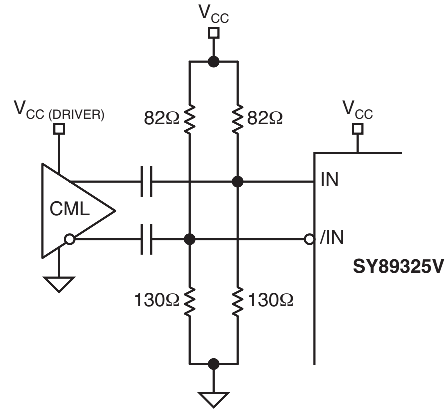


Figure 5. CML-AC Coupled

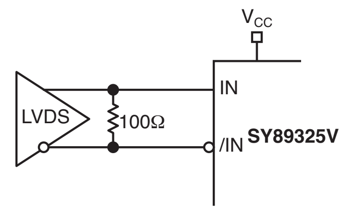


Figure 6. LVDS

OUTPUT INTERFACE APPLICATIONS

LVDS specifies a small swing of 350mV typical, on a nominal 1.25V common mode above ground. The common mode voltage has tight limits to permit large variations in ground between an LVDS driver and receiver. Also, change in common mode voltage, as a function of data input, is kept to a minimum, to keep EMI low.

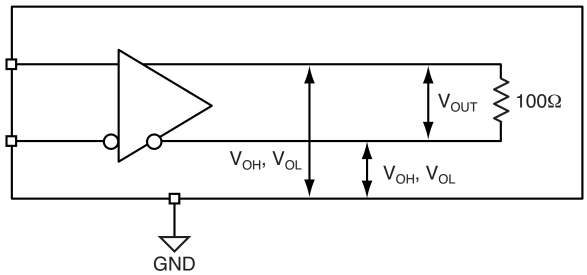


Figure 8a. LVDS Differential Measurement

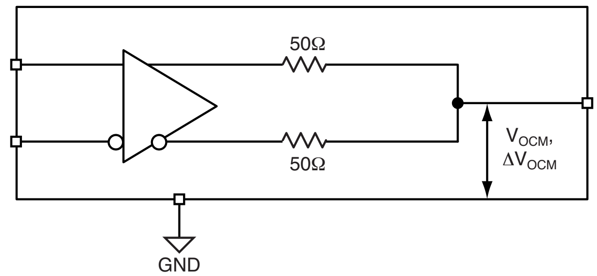
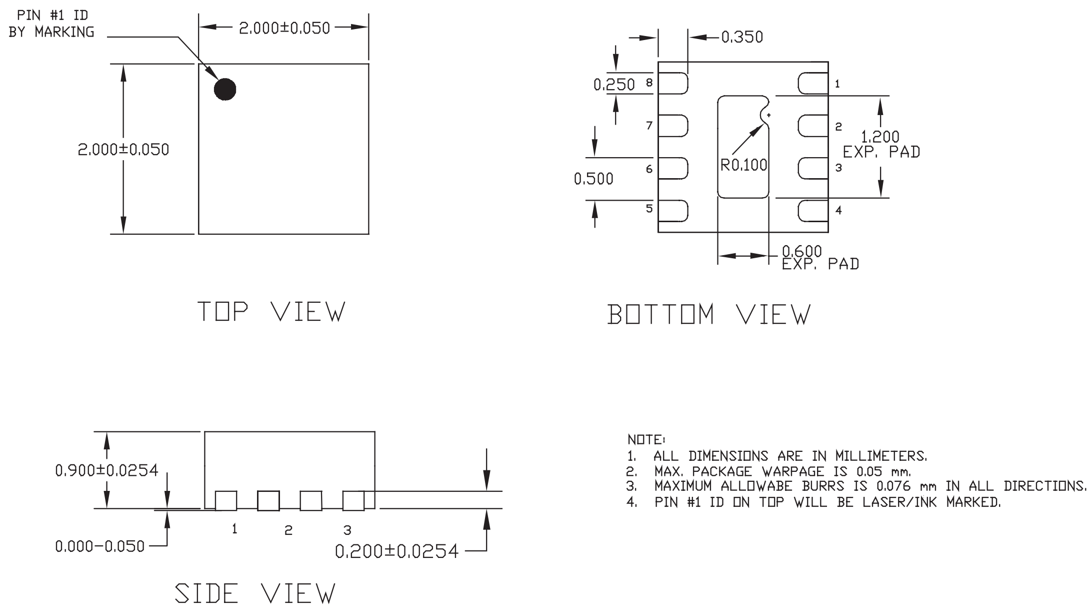


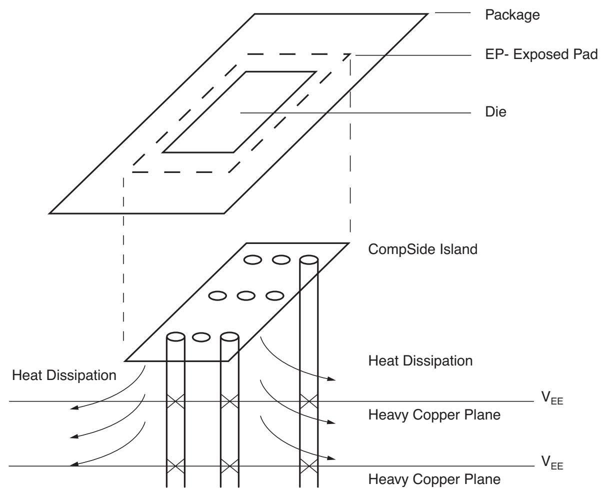
Figure 8b. LVDS Common Mode Measurement

RELATED PRODUCT AND SUPPORT DOCUMENTATION

Part Number	Function	Data Sheet Link
SY55855V	Dual CML/PECL/LVPECL-to-LVDS Translator	www.micrel.com/product-info/products/sy55855v.shtml
	MLF® Application Note	www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

8 LEAD MicroLeadFrame® (MLF-8)





PCB Thermal Consideration for 8-Pin MLF® Package

Package Notes:

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

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