3.3V, 500MHz, 1:9 DIFFERENTIAL HSTL (1.5V) FANOUT BUFFER/ TRANSLATOR

Precision Edge® SY89808L

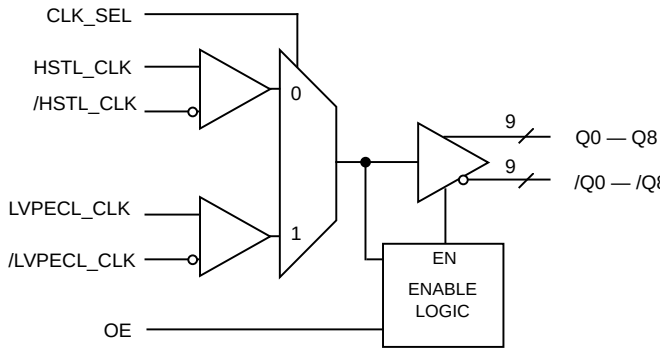
FEATURES

- 9 differential HSTL (1.5V compatible) output pairs
- 500MHz maximum clock frequency
- Triple-buffered enable function
- 3.3V core supply, 1.8V output supply for reduced power
- LVPECL and HSTL inputs
- HSTL outputs drive 50Ω to ground with no offset voltage
- Low pin-to-pin skew (25ps max.)
- Guaranteed over industrial –40°C to +85°C temperature range
- Available in 32-pin TQFP package

APPLICATIONS

- Workstations
- Parallel processor-based systems
- High-performance computing
- Communications

LOGIC SYMBOL



Precision Edge®

DESCRIPTION

The SY89808L is a High-Performance Bus Clock Driver with 9 differential HSTL (High-Speed Transceiver Logic) 1.5V compatible output pairs. The part is designed for use in low-voltage (3.3V/1.8V) applications which require a large number of outputs to drive precisely aligned, ultra-low skew signals to their destination. The input is multiplexed from either HSTL or LVPECL (Low-Voltage Positive-Emitter-Coupled Logic) by the CLK_SEL pin.

The Output Enable (OE) is synchronous and triple-buffered so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any potential of generating a runt clock pulse when the device is enabled/disabled, as can occur with an asynchronous control. The triple-buffering feature provides a three-clock delay from the time the OE input is asserted/de-asserted to when the clock appears at the outputs.

The SY89808L features an ultra-low pin-to-pin skew of less than 25ps. The SY89808L is available in a 32-TQFP space saving package, enabling a lower overall cost solution.

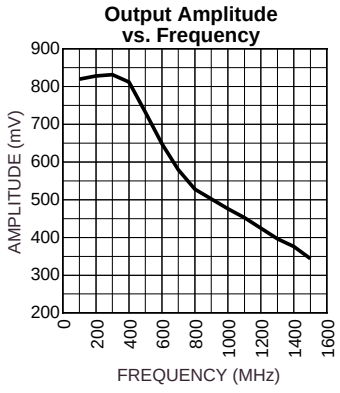
TRUTH TABLE

OE(1)	CLK_SEL	$Q_0 - Q_8$	$/Q_0 - /Q_8$
0	0	LOW	HIGH
0	1	LOW	HIGH
1	0	HSTL_CLK	/HSTL_CLK
1	1	LVPECL_CLK	/LVPECL_CLK

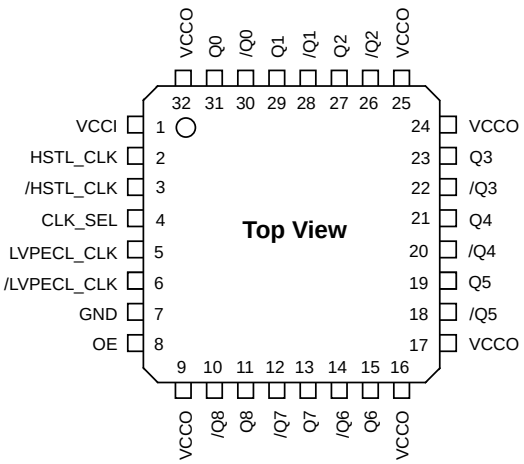
Notes:

1. The OE (output enable) signal is synchronized with the low level of the HSTL_CLK and LVPECL_CLK signal.

TYPICAL PERFORMANCE



PACKAGE/ORDERING INFORMATION



32-Pin TQFP (T32-1)

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89808LTI	T32-1	Industrial	SY89808LTI	Sn-Pb
SY89808LTITR[2]	T32-1	Industrial	SY89808LTI	Sn-Pb
SY89808LTG[3]	T32-1	Industrial	SY89808LTG with Pb-Free bar line indicator	NiPdAu Pb-Free
SY89808LTGTR[2, 3]	T32-1	Industrial	SY89808LTG with Pb-Free bar line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

PIN DESCRIPTION

Pin Number	Pin Name	Type	Pin Function
2, 3	HSTL_CLK, /HSTL_CLK	HSTL Input	Differential clock input selected by CLK_SEL. Can be left floating if not selected. Floating input, if selected produces an indeterminate output. HSTL input signal requires external termination 50Ω to GND.
5, 6	LVPECL_CLK, /LVPECL_CLK	LVPECL Input	Differential clock input selected by CLK_SEL. Can be left floating. Floating input, if selected produces a LOW at the output (internal 75Ω pull-downs). Requires external termination. 75kΩ pull-up.
4	CLK_SEL	LVTTL Input	Selects HSTL_CLK input when LOW and LVPECL_CLK output when HIGH. 11kΩ pull-up.
8	OE	LVTTL Input	Enable input synchronized internally to prevent glitching of the Q0-Q8 and /Q0-/Q8 outputs. Must be a minimum of three clock periods wide if synchronous with the CLK inputs and must meet the t_S and t_H requirements (refer to AC Electrical Characteristics). If asynchronous, must be a minimum of four clock periods wide. 11kΩ pull-up.
31, 29, 27, 23, 21, 19, 15, 13, 11	Q0–Q8	HSTL Output	Differential clock outputs from HSTL_CLK when CLK_SEL = LOW and LVPECL outputs when CLK_SEL = HIGH. HSTL outputs must be terminated with 50Ω to GND. Q0–Q8 outputs are static LOW when OE = LOW. Unused output pairs may be left floating.
30, 28, 26, 22, 20, 18, 14, 12, 10	/Q0–/Q8	HSTL Output	Differential clock outputs from HSTL_CLK when CLK_SEL = LOW and LVPECL outputs when CLK_SEL = HIGH. HSTL outputs must be terminated with 50Ω to GND. /Q0–/Q8 outputs are static HIGH when OE = LOW. Unused output pairs may be left floating.
1	VCCI	VCC Core Power	Core V_{CC} connected to 3.3V supply. Bypass with 0.1µF in parallel with 0.01µF low ESR capacitors as close to V_{CCI} pin as possible.
9, 16, 17, 24, 25, 32	VCCO	VCC Output Power	Output Buffer V_{CC} connected to 1.8V supply. Bypass with 0.1µF in parallel with 0.01µF low ESR capacitors as close to V_{CCO} pins as possible. All V_{CCO} pins should be connected together on the PCB.
7	GND	Ground	Ground.

Absolute Maximum Ratings[1]

Supply Voltage (V_{IN}) ..... –0.5V to V_{CCI}
V_{CC} Pin Potential to Ground Pin
(V_{CCI}, V_{CCO}) ..... –0.5V to +4.0V
DC Output Current, Output HIGH (I_{OUT}) ..... –50mA
Lead Temperature (soldering, 20 sec.) ..... 260°C
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage
(V_{CCI}) ..... +3.15V to +3.45V
(V_{CCO}) ..... +1.6V to +2.0V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance
TQFP (θ_{JA})
–Still-Air ..... 50°C/W
–500lfpm ..... 42°C/W
TQFP (θ_{JC}) ..... 20°C/W

DC ELECTRICAL CHARACTERISTICS

Power Supply T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CCI}	V_{CC} Core		3.15	3.3	3.45	V
V_{CCO}	V_{CC} Output		1.6	1.8	2.0	V
I_{CCI}	I_{CC} Core	Max V_{CC}, No Load	—	80	110	mA

HSTL V_{CCI} = 3.3V ± 5%; V_{CCO} = 1.8V ± 10%; R_L = 50Ω to GND; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage		1.0	—	1.2	V
V_{OL}	Output LOW Voltage		0.2	—	0.4	V
V_{IH}	Input HIGH Voltage		V_X +0.1	—	1.6	V
V_{IL}	Input LOW Voltage		–0.3	—	V_X –0.1	V
V_X	Input Crossover Voltage		0.68	—	0.9	V
I_{IH}	Input HIGH Current		+20	—	–350	µA
I_{IL}	Input LOW Current		—	—	–500	µA

LVPECL V_{CCI} = 3.3V ± 5%; V_{CCO} = 1.8V ± 10%; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Max	Units
V_{IH}	Input HIGH Voltage		V_{CCI} – 1.165	V_{CCI} – 0.880	V
V_{IL}	Input LOW Voltage		V_{CCI} – 1.810	V_{CCI} – 1.475	V
I_{IH}	Input HIGH Current		—	+150	µA
I_{IL}	Input LOW Current		0.5	—	µA

LVCMOS/LVTTL V_{CCI} = 3.3V ± 5%; V_{CCO} = 1.8V ± 10%; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0	—	—	V
V_{IL}	Input LOW Voltage		—	—	0.8	V
I_{IH}	Input HIGH Current		+20	—	–250	µA
I_{IL}	Input LOW Current		—	—	–600	µA

Notes:

1. Permanent device damage may occur if "Absolute Maximum Ratings" are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratlng conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

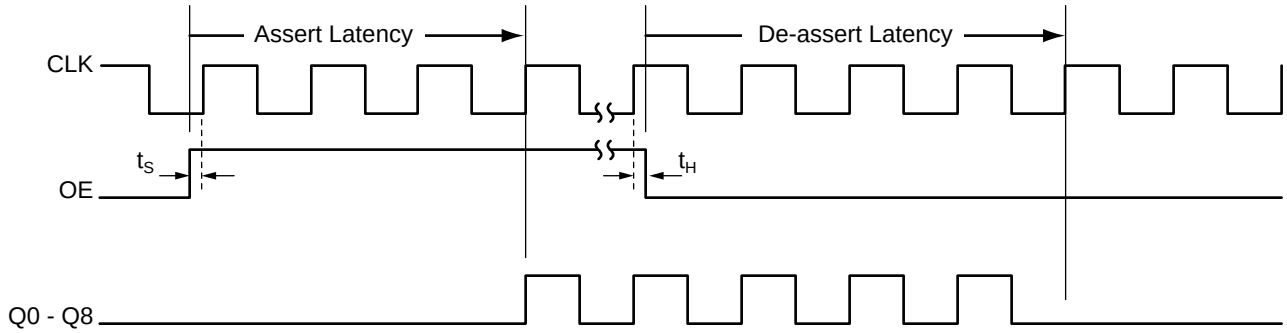
AC ELECTRICAL CHARACTERISTICS

V_{CCI} = 3.3V ± 5%; V_{CCO} = 1.8V ± 10%; All outputs are loaded with 50Ω to GND; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	$V_{OUT} \geq 450mV$	500	—	—	MHz
t_{pd}	Propagation Delay CLK-to-Q	**Note 3**	0.800	1.000	1.200	ns
	SEL-to-Q	**Note 3**	0.800	1.200	1.700	ns
t_{SKEW}	Within-Device Skew	**Note 4**	—	—	25	ps
t_{SKPP}	Part-to-Part Skew	**Note 5**	—	—	400	ps
V_{pp}	Minimum Input Swing LVPECL_CLK	**Note 6**	150	—	—	mV
V_{CMR}	Common Mode Range LVPECL_CLK	**Note 7**	–1.5	—	–0.4	V
t_S	OE Set-Up Time	**Note 8**	1.0	—	—	ns
t_H	OE Hold Time		0.5	—	—	ns
t_r, t_f	Output Rise/Fall Time (20% – 80%)		250	450	650	ps
t_{JITTER}	Cycle-to-Cycle Jitter	**Note 9**			1	ps_{RMS}
	Total Jitter	**Note 10**			10	ps_{PP}

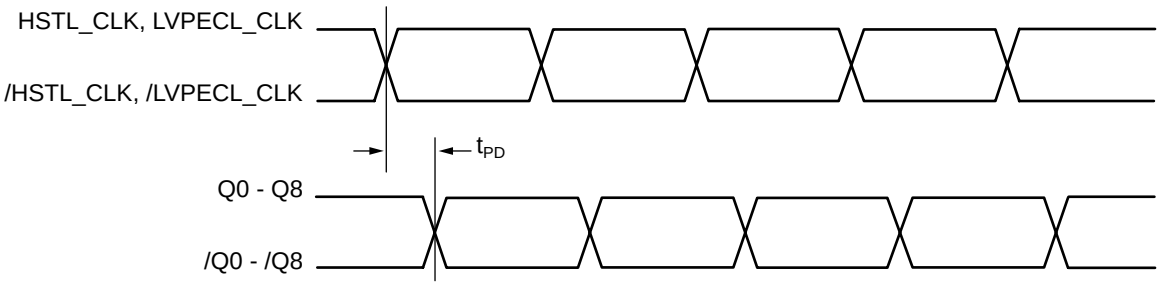
3. Differential propagation delay is defined as the delay from the crossing point of the differential input signals to the crossing point of the differential output signals.
4. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device operating at the same voltage and temperature.
5. The part-to-part skew is defined as the absolute worst case difference between any two delay paths on any two devices operating at the same voltage and temperature.
6. The V_{PP} (min.) is defined as the minimum input differential voltage which will cause no increase in the propagation delay.
7. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The numbers in the table are referenced to V_{CCI}. The V_{IL} level must be such that the peak-to-peak voltage is less than 1.0V and greater than or equal to V_{PP} (min.). The lower end of the CMR range varies 1:1 with V_{CCI}. The V_{CMR} (min) will be fixed at 3.3V – $|V_{CMR}$ (min)|.
8. OE set-up time is defined with respect to the rising edge of the clock. OE HIGH to LOW transition ensures outputs remain disabled during the next clock cycle. OE LOW to HIGH transition enables normal operation of the next input clock.
9. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, T_n–$T_{n–1}$ where T is the time between rising edges of the output signal.
10. Total jitter definition: with an ideal clock source of ≤ f_{max}, no more than one output edge in 10^{12} output edges will deviate by more than the specified amount.

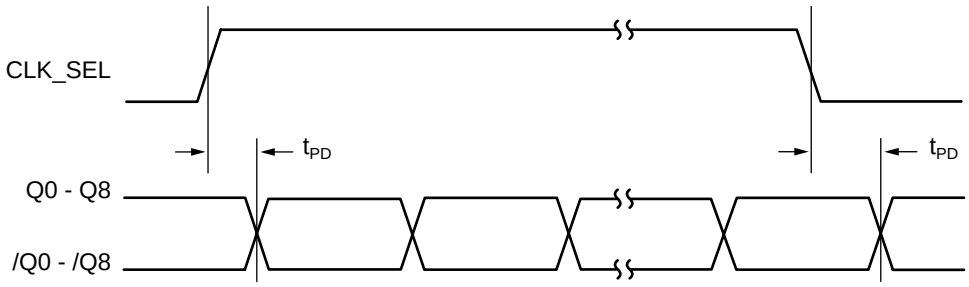
TIMING DIAGRAMS



Notes:

1. The OE input signal must be a minimum of 3 clock periods with width.
2. The internal enable is asserted and de-asserted on the falling edge of clock.
3. The internal enable occurs 2.5 clock cycles (plus the set-up time of OE with the rising edge of clock) after the rising edge of the external OE.
4. If OE does not meet the t_S of t_H specifications as in asynchronous applications, OE must be a minimum of 4 clock periods in width.

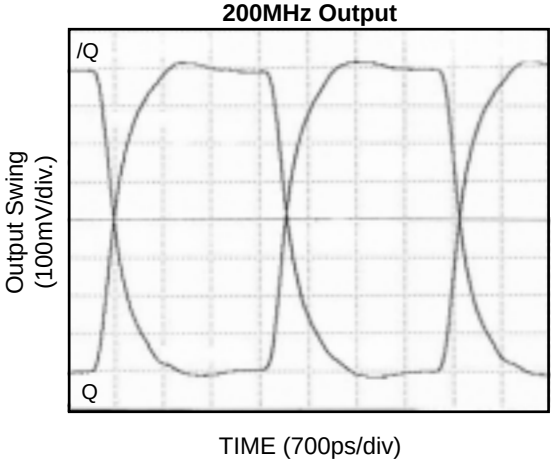




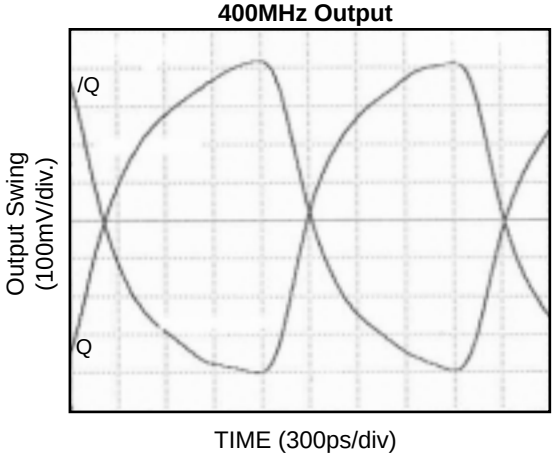
TYPICAL OPERATING CHARACTERISTICS

V_{CCI} = 3.0V, V_{CCO} = 1.8V, T_A = 25°C, unless otherwise stated.

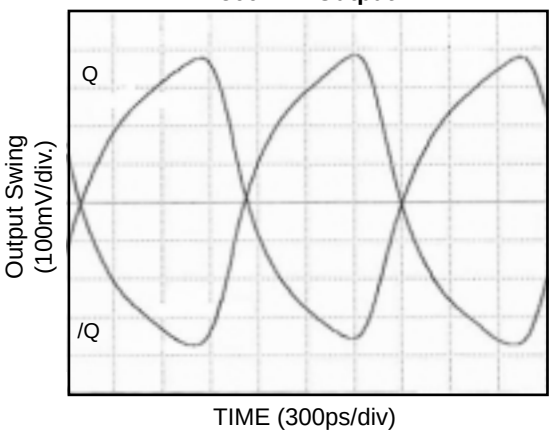
200MHz Output



400MHz Output



500MHz Output



LVPECL/HSTL INPUTS

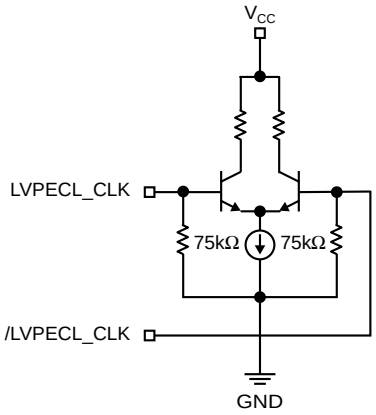


Figure 1. Simplified LVPECL Input Stage

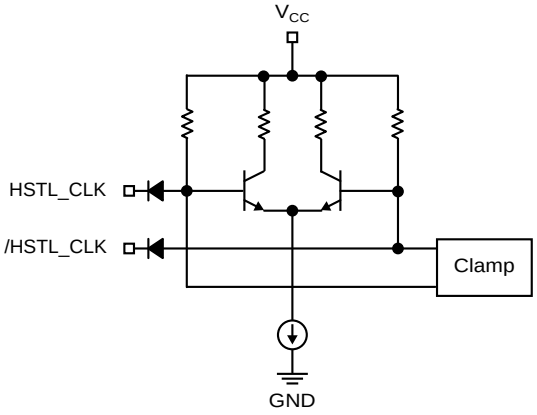


Figure 2. Simplified HSTL Input Stage

HSTL OUTPUTS

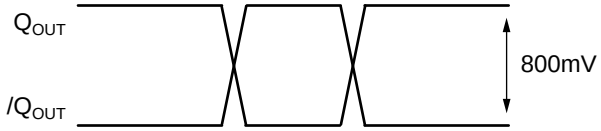


Figure 3. Output Driver Signal Levels (Single-Ended)

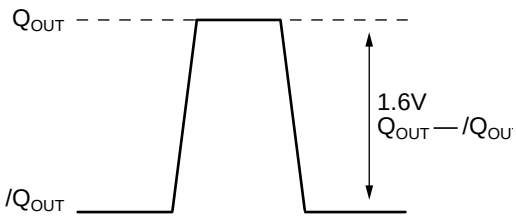
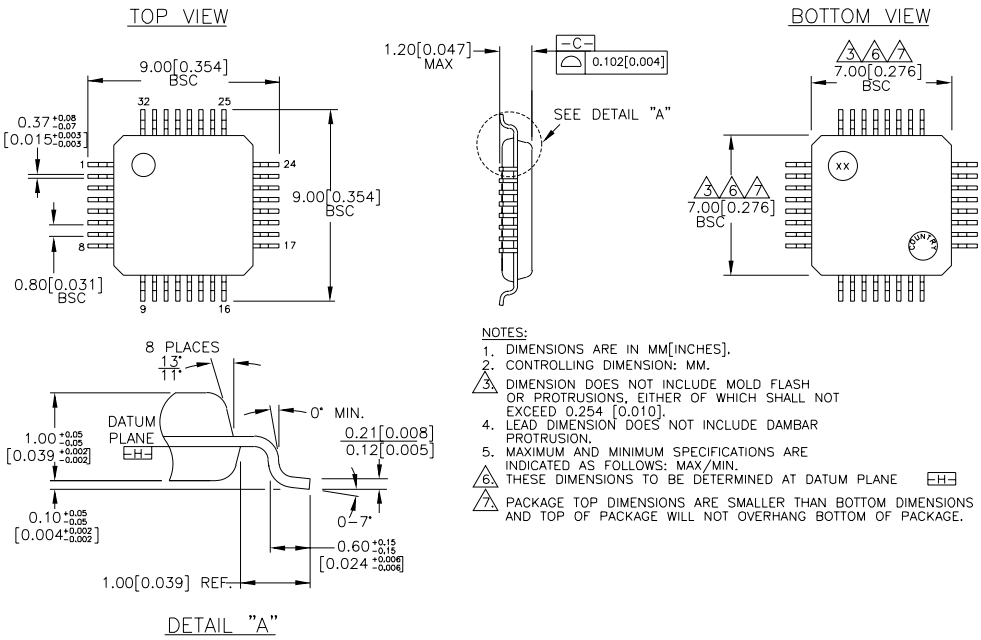


Figure 4. Output Driver Signal Levels (Differential)

RELATED PRODUCT AND SUPPORT DOCUMENTATION

Part Number	Function	Data Sheet Link
SY89809L	3.3V 1:9 High-Performance, Low-Voltage Bus Clock Driver	www.micrel.com/product-info/products/sy89809l.shtml
SY89823L	3.3V, 500MHz 1:22 Differential HSTL (1.5V) Fanout Buffer/Translator	www.micrel.com/product-info/products/sy89823l.html
	Exposed Pad Application Note	www.amkor.com/products/notes_papers/epad.pdf
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml
MIC3775	750mA μCap Low-Voltage Low-Dropout Regulator	www.micrel.com/product-info/products/mic3775.shtml

32 LEAD TQFP (T32-1)



Package Notes:

Package meets Level 2 qualification.

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