MICREL ®

SY89809L

3.3V 1:9 High-Performance, Low-Voltage Bus Clock Driver

Precision Edge®

General Description

The SY89809L is a High-Performance Bus Clock Driver with 9 differential HSTL (High-Speed Transceiver Logic) output pairs. The part is designed for use in low-voltage (3.3V/1.8V) applications, which require a large number of outputs to drive precisely aligned, ultra-low skew signals to their destination. The input is multiplexed from either HSTL or LVPECL (Low-Voltage Positive-Emitter-Coupled Logic) by the CLK_SEL pin. The Output Enable (OE) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control.

The SY89809L features low pin-to-pin skew (50ps max.) and low part-to-part skew (200ps max.)—performance previously unachievable in a standard product having such a high number of outputs. The SY89809L is available in a single space saving package, enabling a lower overall cost solution.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Features

- 3.3V core supply, 1.8V output supply for reduced power
- LVPECL and HSTL inputs
- 9 differential HSTL (low-voltage swing) output pairs
- HSTL outputs drive 50Ω-to-ground with no offset voltage
- 500MHz maximum clock frequency
- Low part-to-part skew (200ps max.)
- Low pin-to-pin skew (50ps max.)
- Available in 32-pin TQFP

Applications

- High-performance PCs
- Workstations
- Parallel processor-based systems
- Other high-performance computing
- Communications
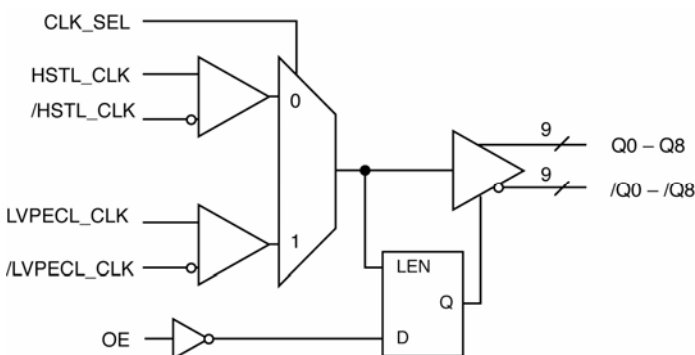
Level	Direction	Signal
HSTL	Input	HSTL_CLK, /HSTL_CLK
HSTL	Output	Q0 – Q8, /Q0 – /Q8
LVPECL	Input	LVPECL_CLK, /LVPECL_CLK
LVCMOS/LVTTL	Input	CLK_SEL, OE

Table 1. Signal Groups

Logic Symbol

OE[1]	CLK_SEL	Q0 – Q8	/Q0 – /Q8
0	0	LOW	HIGH
0	1	LOW	HIGH
1	0	HSTL_CLK	/HSTL_CLK
1	1	LVPECL_CLK	/LVPECL_CLK

Table 2. Truth Table

Note:

1. The OE (output enable) signal is synchronized with the low level of the HSTL_CLK and LVPECL_CLK signal.

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89809LTC	T32-1	Commercial	SY89809LTC	Sn-Pb
SY89809LTCTR[2]	T32-1	Commercial	SY89809LTC	Sn-Pb
SY89809LTH[3]	T32-1	Commercial	SY89809LTH with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY89809LTHTR[2, 3]	T32-1	Commercial	SY89809LTH with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25°C$, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

Pin Configuration
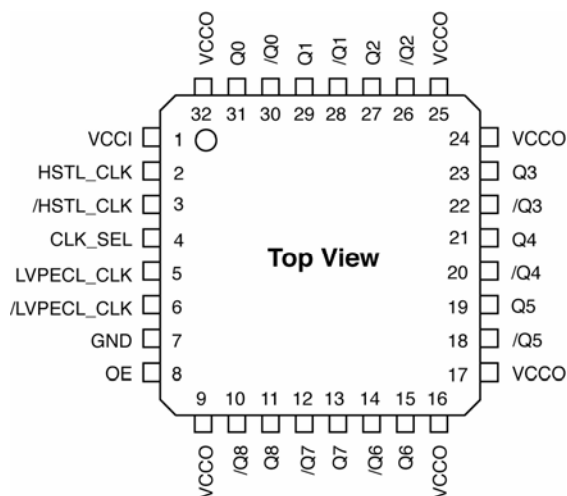
32-Pin TQFP (T32-1)

Pin Description

Pin Number	Pin Name	Type	Pin Function
2, 3	HSTL_CLK, /HSTL_CLK	HSTL Input	Differential input: This HSTL input can be selected by CLK_SEL. If it is not used, it can be left floating. This produces a LOW at the output. If driven by an HSTL driver, an external 50Ω to ground termination is required at the input.
5, 6	LVPECL_CLK, /LVPECL_CLK	LVPECL Input	Differential input: This LVPECL input can be selected by CLK_SEL. If it is not used, it can be left floating. This produces a LOW at the output (internal 75kΩ pull-downs).
4	CLK_SEL	LVTTL Input	Selected HSTL_CLK input when LOW and LVPECL_CLK output when HIGH. 11kΩ pull-up.
8	OE	LVTTL Input	Single-ended input: This LVTTL input disables and enables the Q0-Q8 output pairs. It is internally synchronized to prevent glitching of the Q0-Q8 output pairs. It is internally connected to a 11kΩ pull-up resistor and will default to a logic HIGH state if left open.
31, 29, 27, 23, 21, 19, 15, 13, 11	Q0 – Q8	HSTL Output	Differential clock outputs from HSTL_CLK when CLK_SEL = LOW and LVPECL outputs when CLK_SEL = HIGH. HSTL outputs must be terminated with 50Ω to GND. Q0-Q8 outputs are static LOW when OE = LOW. Unused output pairs may be left floating.
30, 28, 26, 22, 20, 18, 14, 12, 10	/Q0 – /Q8	HSTL Output	Differential clock outputs from HSTL_CLK when CLK_SEL = LOW and LVPECL outputs when CLK_SEL = HIGH. HSTL outputs must be terminated with 50Ω to GND. /Q0-/Q8 outputs are static HIGH when OE = LOW. Unused output pairs may be left floating.
1	VCCI	VCC Core Power	Core V_{CC} connected to 3.3V supply. Bypass with 0.1µF in parallel with 0.01µF low ESR capacitors as close to V_{CCI} pin as possible.
9, 16, 17, 24, 25, 32	VCCO	VCC Output Power	Output Buffer VCC connected to 1.8V supply. Bypass with 0.1µF in parallel with 0.01µF low ESR capacitors as close to V_{CCO} pins as possible. All V_{CCO} pins should be connected together on the PCB.
7	GND	Ground	Ground.

Absolute Maximum Ratings[1]

Supply Voltage (V_{IN}).. –0.5V to V_{CCI}
V_{CC} Pin Potential to Ground Pin
  (V_{CCI}, V_{CCO}) .... –0.5V to +4.0V
DC Output Current, Output HIGH (I_{OUT})....................–50mA
Lead Temperature (soldering, 20sec.)......................260°C
Storage Temperature (T_s) ....–65°C to +150°C

Operating Ratings[2]

Supply Voltage
  (V_{CCI}).. +3.0V to +3.6V
  (V_{CCO}).. +1.6V to +2.0V
Ambient Temperature (T_A) ....0°C to +85°C
Package Thermal Resistance
  TQFP (θ_{JA})
    –Still-Air...50°C/W
    –500lfpm ....42°C/W
  TQFP (θ_{JC}) ....20°C/W

DC Electrical Characteristics

T_A = 0°C to +85°C, unless noted.

Power Supply

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CCI}	V_{CC} Core		3.0	3.3	3.6	V
V_{CCO}	V_{CC} Output		1.6	1.8	2.0	V
I_{CCI}	I_{CC} Core			115	140	mA

HSTL

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage[3]		1.0		1.2	V
V_{OL}	Output LOW Voltage[3]		0.2		0.4	V
V_{IH}	Input HIGH Voltage		V_X +0.1		1.6	V
V_{IL}	Input LOW Voltage		–0.3		V_X –0.1	V
V_X	Input Crossover Voltage		0.68		0.9	V
I_{IH}	Input HIGH Current		+20		–350	µA
I_{IL}	Input LOW Current				–500	µA

LVPECL

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		V_{CCI} –1.165		V_{CCI} –0.880	V
V_{IL}	Input LOW Voltage		V_{CCI} –1.810		V_{CCI} –1.475	V
I_{IH}	Input HIGH Current				+150	µA
I_{IL}	Input LOW Current		0.5			µA

LVCMOS/LVTTL

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current		+20		–250	µA
I_{IL}	Input LOW Current				–600	µA

Notes:

1. Exceeding the absolute maximum rating may damage the device.

2. The device is not guaranteed to function outside its operating rating.

3. Outputs loaded with 50Ω to ground.

AC Electrical Characteristics[4]

T_A = 0°C to +85°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
t_{PD}	Propagation Delay[5]		825	1050	1275	ps
f_{MAX}	Maximum Operating Frequency[6]		500			MHz
t_{SKEW}	Within-Device Skew[7]				50	ps
t_{SKPP}	Part-to-Part Skew[8]				200	ps
t_{JITTER}	Phase Noise(RMS)	12kHz-20MHz @ 500MHz See Figure 3		0.241	1	ps
V_{PP}	Minimum Input Swing[9] LVPECL_CLK		600			mV
V_{CMR}	Common Mode Range[10] LVPECL_CLK		−1.5		−0.4	V
t_S	OE Set-Up Time[11]		1.0			ns
t_H	OE Hold Time		0.5			ns
t_r, t_f	Output Rise/Fall Time (20% to 80%)		300		650	ps

Notes:

4. Outputs loaded with 50Ω to ground. Airflow ≥ 300lfpm.

5. Differential propagation delay is defined as the delay from the crossing point of the differential input signals to the crossing point of the differential output signals.

6. Output swing greater than 450mV.

7. The within-device skew is defined as the worst-case difference between any two similar delay paths within a single device operating at the same voltage and temperature.

8. The part-to-part skew is defined as the absolute worst-case difference between any two delay paths on any two devices operating at the same voltage and temperature.

9. The V_{PP}(min) is defined as the minimum input differential voltage which will cause no increase in the propagation delay.

10. V_{CMR} is defined as the range within which the VIH level may vary with the device still meeting the propagation delay specification. The numbers in the table are referenced to V_{CCI}. The VIL level must be such that the peak-to-peak voltage is less than 1.0V and greater than or equal to V_{PP}(min).

11. OE set-up time is defined with respect to the rising edge of the clock. OE HIGH-to-LOW transition ensures outputs remain disabled during the next clock cycle.
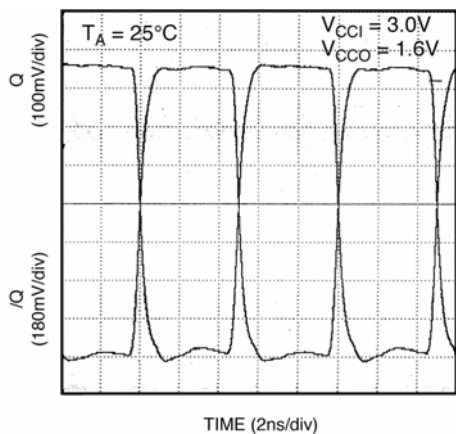
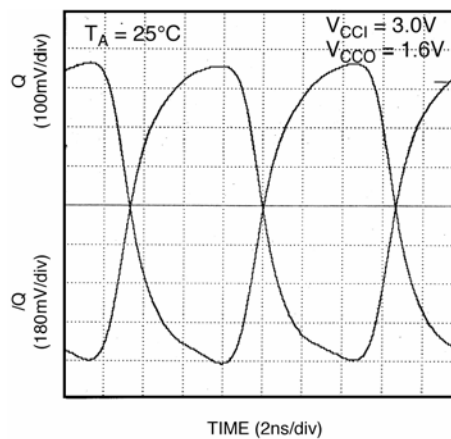# Output Waveforms

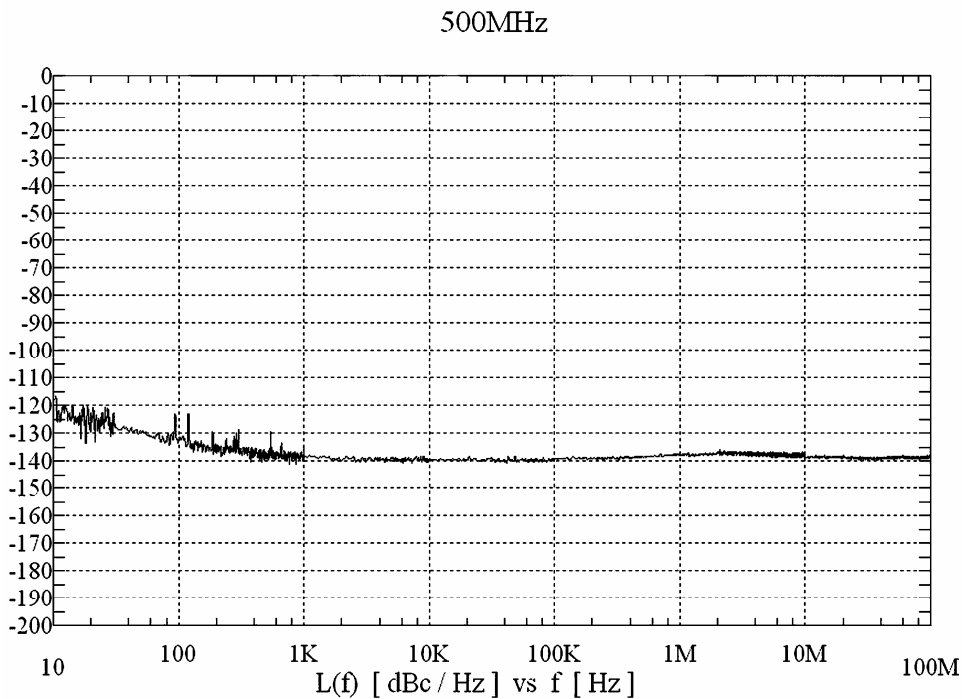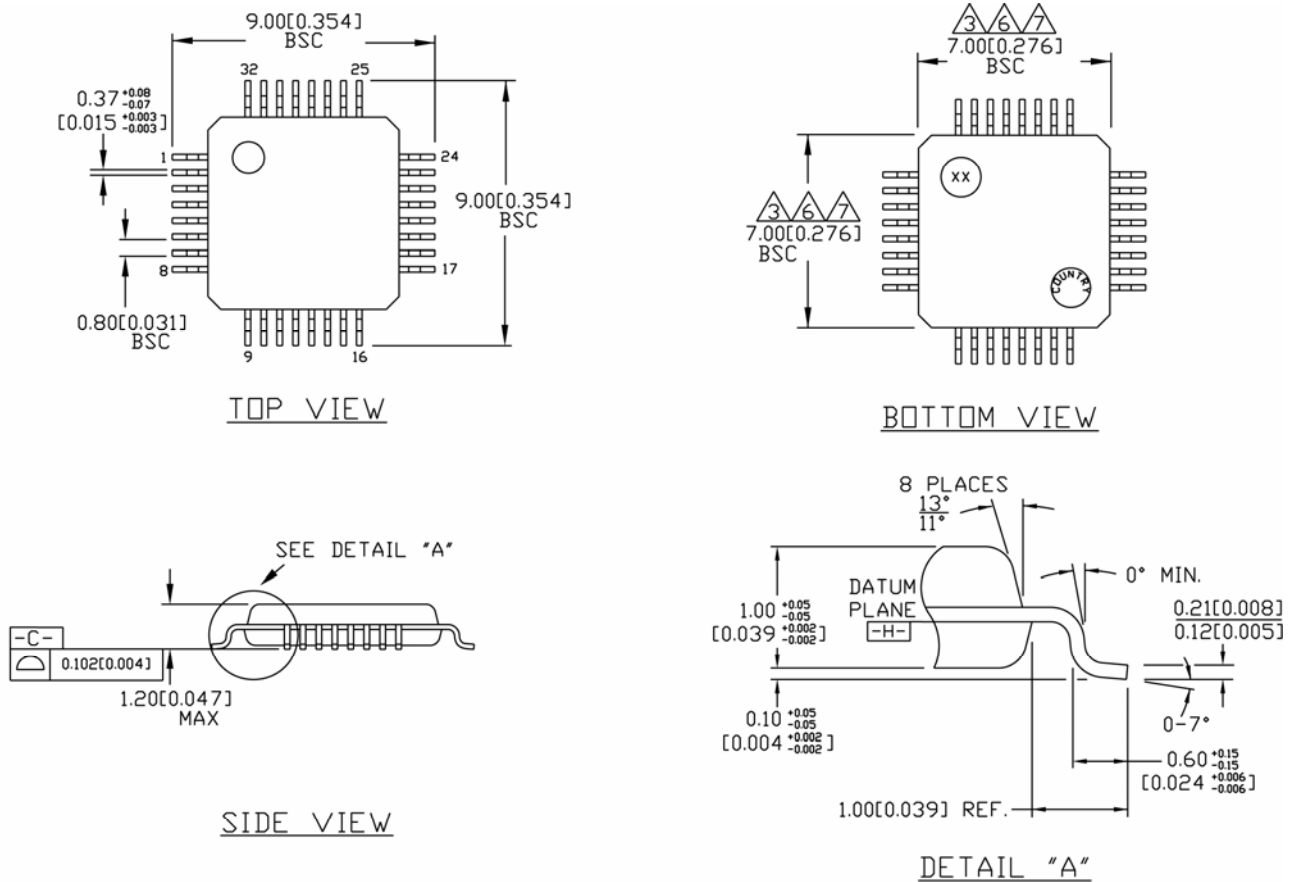**Figure 1. 100MHz Output Waveform**

Figure 2. 300MHz Output Waveform

Figure 4. Phase Noise Plot

Package Information

TOP VIEW

BOTTOM VIEW

SIDE VIEW

DETAIL "A"

NOTES:
1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.254 [0.010].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN.
6. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE [-H-]
7. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.

32-Pin TQFP (T32-1)

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