TC14433/A

3-1/2 Digit Analog-to-Digital Converter with BCD Outputs

Features

- Accuracy: ±0.05% of Reading ±1 Count
- Two Voltage Ranges: 1.999V and 199.9 mV
- Up to 25 Conversions Per Second
- Z_{IN} > 1000M Ohms
- Single Positive Voltage Reference
- Auto-Polarity and Auto-Zero
- Overrange and Underrange Signals Available
- Operates in Auto-Ranging Circuits
- Uses On-Chip System Clock or External Clock
- Wide Supply Range: ±4.5V to ±8V

Applications

- Portable Instruments
- Digital Voltmeters
- Digital Panel Meters
- Digital Scales
- Digital Thermometers
- Remote A/D Sensing Systems

Description

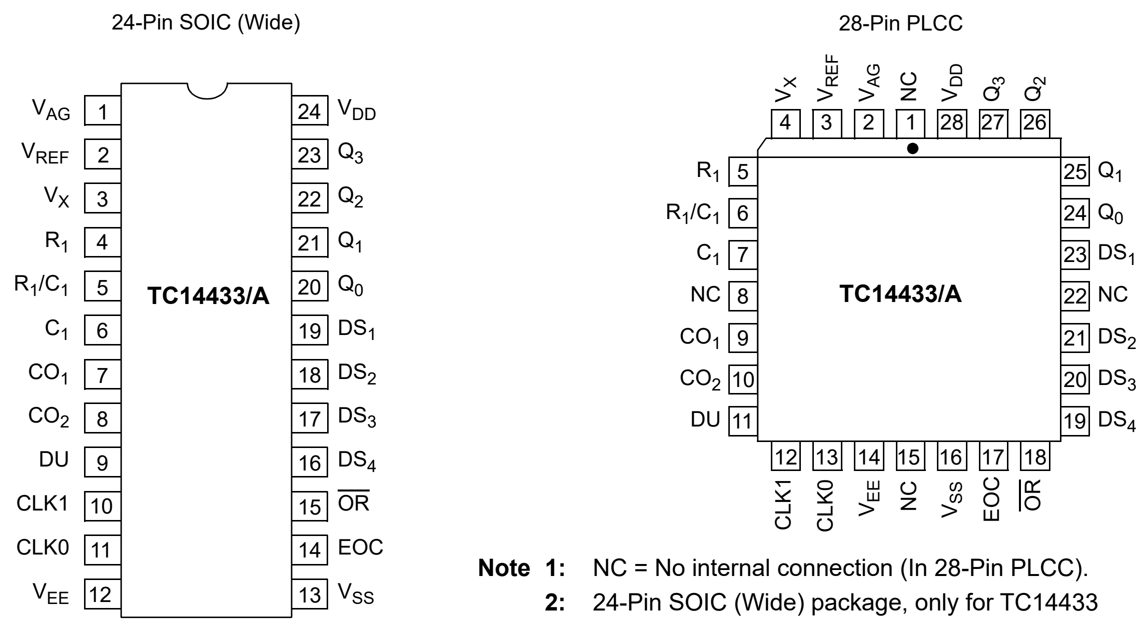
The TC14433 is a low-power, high-performance, monolithic CMOS 3-1/2 digit A/D converter. The TC14433 combines both analog and digital circuits on a single IC, thus minimizing the number of external components.

This dual-slope A/D converter provides automatic polarity and zero correction with the addition of two external resistors and two capacitors. The full scale voltage range of this ratiometric IC extends from 199.9 mV to 1.999V. The TC14433 can operate over a wide range of power supply voltages, including batteries and standard 5-V supplies.

The TC14433A features improved performance over the industry standard TC14433. Rollover, which is the measurement of identical positive and negative signals, is specified to have the same reading within one count for the TC14433A. Power consumption of the TC14433A is typically 4 mW, approximately one-half that of the industry standard TC14433.

The TC14433/A is available in 24-Pin SOIC (TC14433 device only) and 28-Pin PLCC packages.

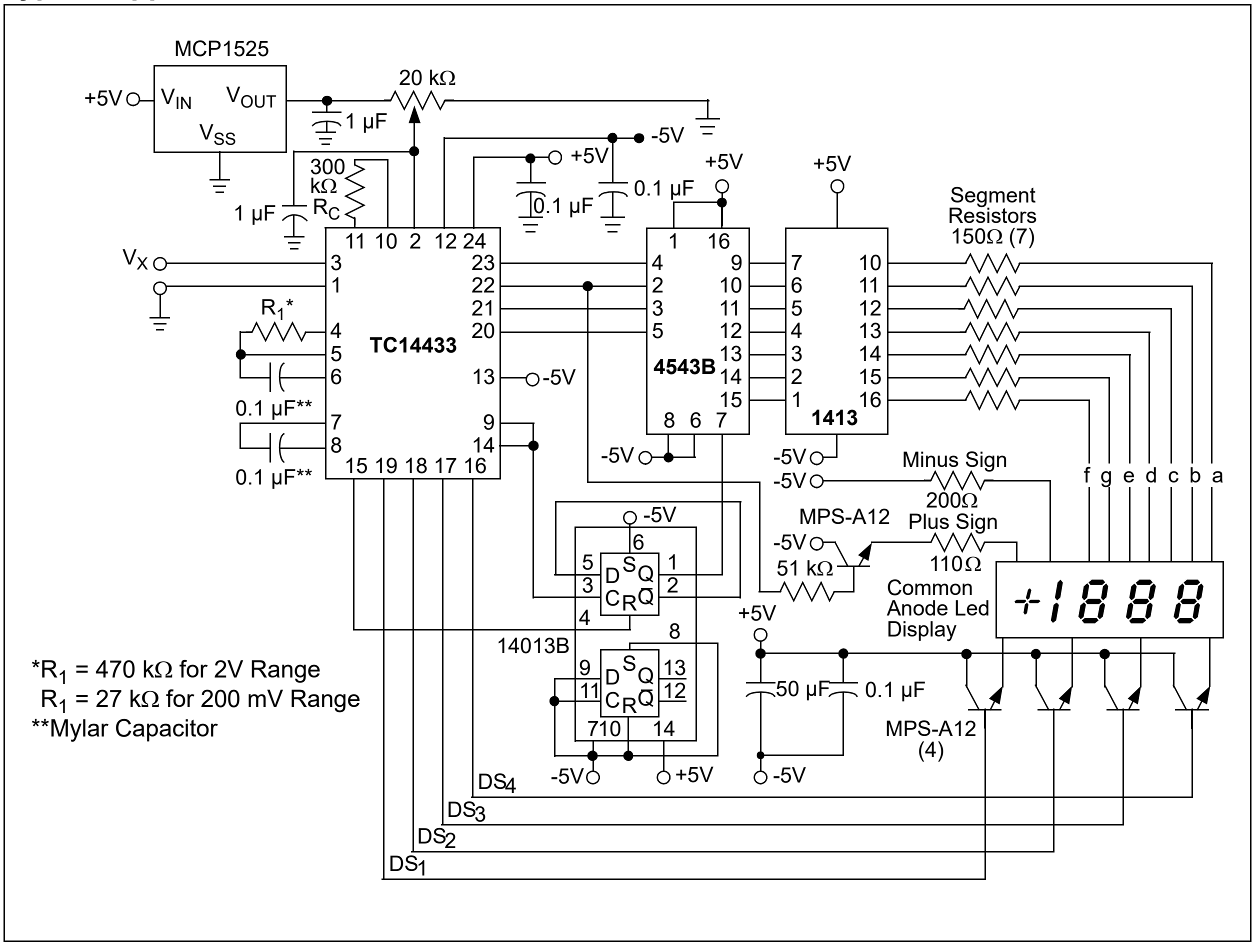
Package Type



Note 1: NC = No internal connection (In 28-Pin PLCC).

2: 24-Pin SOIC (Wide) package, only for TC14433 device.

Typical Application



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage ($V_{DD} – V_{EE}$) .... -0.5V to +18V
Voltage on Any Pin:
Reference to V_{EE} .... -0.5V to (V_{DD} + 0.5)
DC Current, Any Pin: .... ±10 mA
Power Dissipation ($T_A \leq 70°C$):
Plastic PLCC 1.0W
SOIC .... 940 mW
Operating Temperature Range .... -40°C to +85°C
Storage Temperature Range .... -65°C to +160°C

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TC14433/A ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise specified, V_{DD} = +5V, V_{EE} = -5V, C_1 = 0.1 µF, (Mylar), C_0 = 0.1 µF, R_C = 300 kΩ, R_1 = 470 kΩ @ V_{REF} = 2V, R_1 = 27 kΩ @ V_{REF} = 200 mV, T_A = +25°C.

Parameter	Symbol	Temp. = +25°C			Temp. = -40°C to +85°C (except +25°C)				Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Units	
Analog Input									
Rollover Error (Positive) and Negative Full Scale Symmetry	SYE	-1	—	+1	—	—	—	Counts	200 mV Full Scale V_{IN} -V_{IN} = +V_{IN}
Linearity Output Reading (**Note 1**)	NL	-0.05	+0.05	+0.05	—	—	—	%rdg	V_{REF} = 2V
		-1	—	+1	—	—	—	counts	V_{REF} = 200 mV
Stability Output Reading (**Note 2**)	SOR	— —	— —	2 3	— —	— —	— —	LSD LSD	V_X = 1.99V, V_{REF} = 2V V_X = 199 mV, V_{REF} = 200 mV
Zero Output Reading	ZOR	—	0	0	—	—	—	LSD	V_X = 0V, V_{REF} = 2V
Bias Current: Analog Input Reference Input Analog Ground	I_{IN}	— — —	±20 ±20 ±20	±100 ±100 ±100	— — —	— — —	— — —	pA pA pA	
Common Mode Rejection	CMRR	—	65	—	—	—	—	dB	V_X = 1.4V, V_{REF} = 2V, F_{OC} = 32 kHz
Output Voltage (Pins 14 to 23) (**Note 3**)	V_{OL}	— —	0 -5	0.05 -4.95	— —	— —	0.05	V	V_{SS} = 0V, “0” Level V_{SS} = 5V, “0” Level
Digital									
Output Voltage (Pins 14 to 23) (**Note 3**)	V_{OH}	4.95 4.95	5 5	— —	4.95 4.95	— —	— —	V V	V_{SS} = 0V, “1” Level V_{SS} = 05, “1” Level
Output Current (Pins 14 to 23)	I_{OH}	-0.2 -0.5	-0.36 -0.9	— —	-0.14 -0.35	— —	— —	mA mA	V_{SS} = 0V, V_{OH} = 4.6V Source V_{SS} = -5V, V_{OH} = 5V Source

Note 1: Accuracy – The accuracy of the meter at full scale is the accuracy of the setting of the reference voltage. Zero is recalculated during each conversion cycle. The meaningful specification is linearity. In other words, the deviation from correct reading for all inputs other than positive full scale and zero is defined as the linearity specification.

2: The LSD stability for 200 mV scale is defined as the range that the LSD will occupy 95% of the time.

3: Pin numbers refer to 24-pin SOIC.

TC14433/A ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise specified, V_{DD} = +5V, V_{EE} = -5V, C_1 = 0.1 µF, (Mylar), C_0 = 0.1 µF, R_C = 300 kΩ, R_1 = 470 kΩ @ V_{REF} = 2V, R_1 = 27 kΩ @ V_{REF} = 200 mV, T_A = +25°C.

Parameter	Symbol	Temp. = +25°C			Temp. = -40°C to +85°C (except +25°C)				Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Units	
Output Current (Pins 14 to 23)	I_{OL}	0.51 1.3	0.88 2.25	— —	0.36 0.9	— —	— —	mA mA	V_{SS} = 0V, V_{OL} = 0.4V Sink V_{SS} = -5V, V_{OL} = -4.5V Sink
Clock Frequency		—	66	—	—	—	—	kHz	R_C = 300 kΩ
Input Current -DU	I_{DU}	—	±0.00 001	±0.3	—	—	±1	µA	
Power									
Quiescent Current: TC14433A	I_Q		— 0.4 1.4	— 2 4	— — —	— — —	— 3.7 7.4	— mA mA	V_{DD} to V_{EE}, I_{SS} = 0 V_{DD} = 5, V_{EE} = -5 V_{DD} = 8, V_{EE} = -8
Quiescent Current: TC14433		— — —	— 0.9 1.8	— 2 4	— — —	— — —	— 3.7 7.4	— mA mA	V_{DD} to V_{EE}, I_{SS} = 0 V_{DD} = 5, V_{EE} = -5 V_{DD} = 8, V_{EE} = -8
Supply Rejection	PSRR	—	0.5	—	—	—	—	mV/V	V_{DD} to V_{EE}, I_{SS} = 0, V_{REF} = 2V, V_{DD} = 5, V_{EE} = -5

Note 1: Accuracy – The accuracy of the meter at full scale is the accuracy of the setting of the reference voltage. Zero is recalculated during each conversion cycle. The meaningful specification is linearity. In other words, the deviation from correct reading for all inputs other than positive full scale and zero is defined as the linearity specification.

2: The LSD stability for 200 mV scale is defined as the range that the LSD will occupy 95% of the time.

3: Pin numbers refer to 24-pin SOIC.

TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +5V and V_{EE} = -5V.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+85	°C	Note
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 24LD CERDIP	θ_{JA}	—	N/A	—	°C/W	
Thermal Resistance, 24LD SOIC Wide	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 28LD PLCC	θ_{JA}	—	61.2	—	°C/W	

Note: The internal junction temperature (T_J) must not exceed the absolute maximum specification of +150°C.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise specified, V_{DD} = +5V, V_{EE} = -5V, C_1 = 0.1 µF, (Mylar), C_0 = 0.1 µF, R_C = 300 kΩ, R_1 = 470 kΩ @ V_{REF} = 2V, R_1 = 27 kΩ @ V_{REF} = 200 mV, T_A = +25°C.

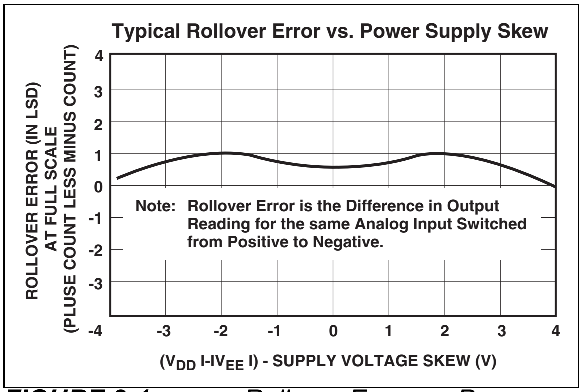


FIGURE 2-1: *Rollover Error vs. Power Supply Skew.*

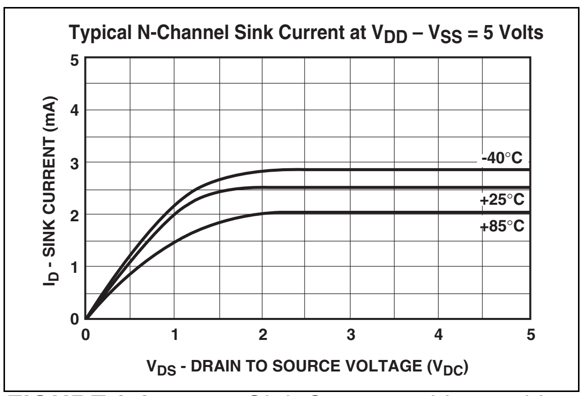
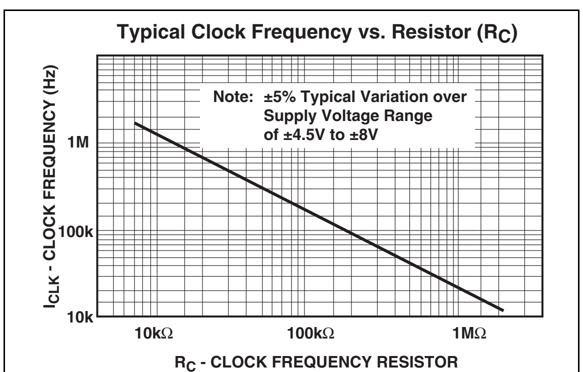


FIGURE 2-2: *Sink Current at V_{DD} = 5V.*



$$\text{CONVERSION RATE} = \frac{\text{CLOCK FREQUENCY}}{16,400} \pm 1.5\%$$

$$\text{MULTIPLEX RATE} = \frac{\text{CLOCK FREQUENCY}}{80}$$

FIGURE 2-3: *Clock Frequency vs. Resistor (R_C).*

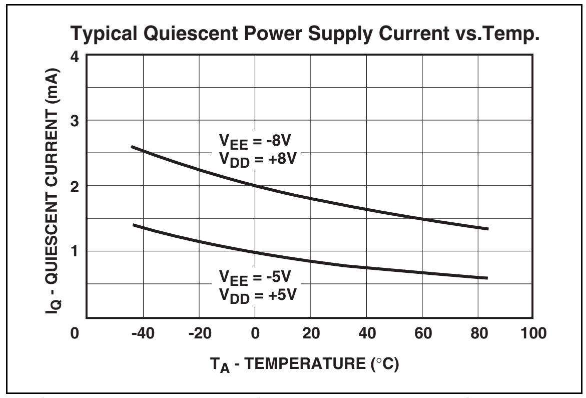


FIGURE 2-4: *Quiescent Power Supply Current vs. Ambient Temperature.*

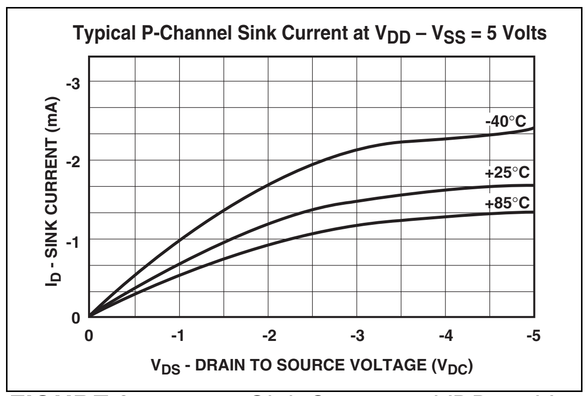
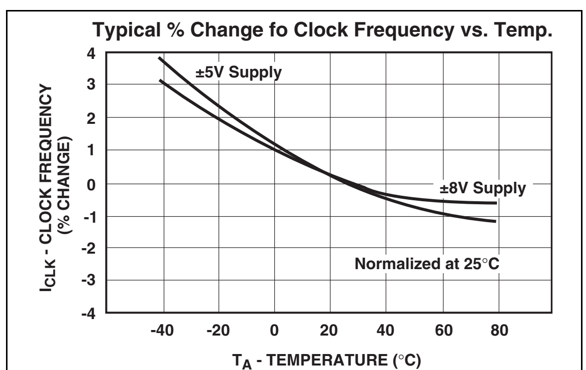


FIGURE 2-5: *Sink Current at VDD = 5V.*



$$\text{CONVERSION RATE} = \frac{\text{CLOCK FREQUENCY}}{16,400} \pm 1.5\%$$

$$\text{MULTIPLEX RATE} = \frac{\text{CLOCK FREQUENCY}}{80}$$

FIGURE 2-6: *% Change to Clock Frequency vs. Ambient Temperature.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin No. 24-Pin SOIC	Pin No. 28-Pin PLCC	Symbol	Description
1	2	V_{AG}	This is the analog ground. It has a high input impedance. The pin determines the reference level for the unknown input voltage (V_X) and the reference voltage (V_{REF}).
2	3	V_{REF}	Reference voltage – Full scale output is equal to the voltage applied to V_{REF}. Therefore, full scale voltage of 1.999V requires 2V reference and 199.9-mV full scale requires a 200-mV reference. V_{REF} functions as system reset also. When switched to V_{EE}, the system is reset to the beginning of the conversion cycle.
3	4	V_X	The unknown input voltage (V_X) is measured as a ratio of the reference voltage (V_{REF}) in a ratiometric A/D conversion.
4	5	R_1	This pin is for external components used for the integration function in the dual slope conversion. Typical values are 0.1 µF (Mylar) capacitor for C_1.
5	6	R_1/C_1	R_1 = 470 kΩ (resistor) for 2V full scale.
6	7	C_1	R_1 = 27 kΩ (resistor) for 200-mV full scale. Clock frequency of 66 kHz gives 250-ms conversion time.
7	9	CO_1	These pins are used for connecting the offset correction capacitor. The recommended value is 0.1 µF.
8	10	CO_2	These pins are used for connecting the offset correction capacitor. The recommended value is 0.1 µF.
9	11	DU	Display update input pin. When DU is connected to the EOC output, every conversion is displayed. New data will be strobed into the output latches during the conversion cycle if a positive edge is received on DU, prior to the ramp down cycle. When this pin is driven from an external source, the voltage should be referenced to V_{SS}.
10	12	CLK_1	Clock input pins. The TC14433 has its own oscillator system clock. Connecting a single resistor between CLK_1 and CLK_0 sets the clock frequency.
11	13	CLK_0	A crystal or OC circuit may be inserted in lieu of a resistor for improved CLK_1. The clock input can be driven from an external clock source, which needs to only have standard CMOS output drive. This pin is referenced to V_{EE} for external clock inputs. A 300-kΩ resistor yields a clock frequency of about 66 kHz. See **Section 2.0 “Typical Performance Curves”**. (Also see Figure 5-3 for alternate circuits.)
12	14	V_{EE}	Negative power current. Connection pin for the most negative supply. Please note the current for the output drive circuit is returned through V_{SS}. Typical supply current is 0.8 mA.
13	16	V_{SS}	Negative power supply for output circuitry. This pin sets the low voltage level for the output pins (BCD, Digit Selects, EOC, and OR). When connected to analog ground, the output voltage is from analog ground to V_{DD}. If connected to V_{EE}, the output swing is from V_{EE} to V_{DD}. The recommended operating range for V_{SS} is between the V_{DD} -3 volts and V_{EE}.
14	17	EOC	End of conversion output generates a pulse at the end of each conversion cycle. This generated pulse width is equal to one half the period of the system clock.
15	18	OR	Overrange pin. Normally this pin is set high. When V_X exceeds V_{REF}, the OR is low.

TABLE 3-1: PIN FUNCTION TABLE (CONTINUED)

Pin No. 24-Pin SOIC	Pin No. 28-Pin PLCC	Symbol	Description
16	19	DS_4	Digit select pin. The digit select output goes high when the respective digit is selected. The MSD (1/2-digit) turns on immediately after an EOC pulse.
17	20	DS_3	The remaining digits turn on in sequence from MSD to LSD.
18	21	DS_2	To ensure that the BCD data has settled, an inter-digit blanking time of two clock periods is included.
19	23	DS_1	Clock frequency divided by 80 equals multiplex rate. For example, a system clock of 60 kHz gives a multiplex rate of 0.8 kHz.
20	24	Q_0	See Figure 5-4 for digit select timing diagram.
21	25	Q_1	BCD data output pin. Multiplexed BCD outputs contain three full digits of information during digit select DS_2, DS_3, and DS_4.
22	26	Q_2	During DS_1, the 1/2 digit, overrange, underrange, and polarity information are available.
23	27	Q_3	Refer to the Truth Table 5-1.
24	28	V_{DD}	Positive power supply. This is the most positive power supply pin.
—	1	NC	Not used.
—	8	NC	Not used.
—	15	NC	Not used.
—	22	NC	Not used.

4.0 DETAILED DESCRIPTION

The TC14433 CMOS IC becomes a modified dual-slope A/D with a minimum of external components. This IC has the customary CMOS digital logic circuitry, as well as CMOS analog circuitry. It provides the user with digital functions (such as counters, latches, and multiplexers) and analog functions (such as operational amplifiers and comparators) on a single chip. Refer to the functional block diagram in Figure 4-3.

Features of the TC14433/A include auto-zero, high input impedances, and auto-polarity. Low power consumption and a wide range of power supply voltages are also advantages of this CMOS device. The system's auto-zero function compensates for the offset voltage of the internal amplifiers and comparators. In this "ratiometric system," the output reading is the ratio of the unknown voltage to the reference voltage, where a ratio of 1:1 is equal to the maximum count of 1999. It takes approximately 16,000 clock periods to complete one conversion cycle. Each conversion cycle may be divided into six segments. Figure 4-1 shows the conversion cycle in six segments for both positive and negative inputs.

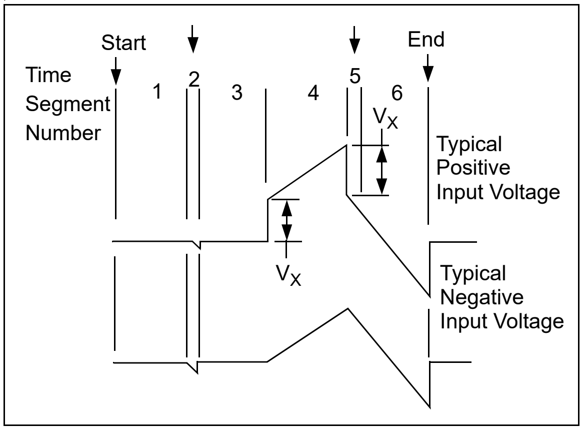


FIGURE 4-1: *Integrator Waveforms at Pin 6.*

Segment 1 – The offset capacitor (C_O), which compensates for the input offset voltages of the buffer and integrator amplifiers, is charged during this period. However, the integrator capacitor is shorted. This segment requires 4,000 clock periods.

Segment 2 – During this segment, the integrator output decreases to the comparator threshold voltage. At this time, a number of counts equivalent to the input offset voltage of the comparator is stored in the offset latches for later use in the auto-zero process. The time for this segment is variable and less than 800 clock periods.

Segment 3 – This segment of the conversion cycle is the same as Segment 1.

Segment 4 – Segment 4 is an up-going ramp cycle with unknown input voltage (V_X as the input to the integrator). Figure 4-2 shows the equivalent configuration of the analog section of the TC14433. The actual configuration of the analog section is dependent upon the polarity of the input voltage during the previous conversion cycle.

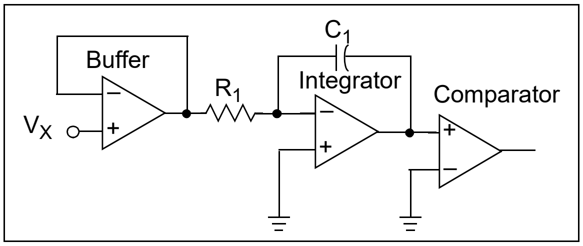


FIGURE 4-2: *Equivalent Circuit Diagrams of the Analog Section During Segment 4 of the Timing Cycle.*

Segment 5 – This segment is a down-going ramp period with the reference voltage as the input to the integrator. Segment 5 of the conversion cycle has a time equal to the number of counts stored in the offset storage latches during Segment 2. As a result, the system zeros automatically.

Segment 6 – This is an extension of Segment 5. The time period for this portion is 4,000 clock periods. The results of the A/D conversion cycle are determined in this portion of the conversion cycle.

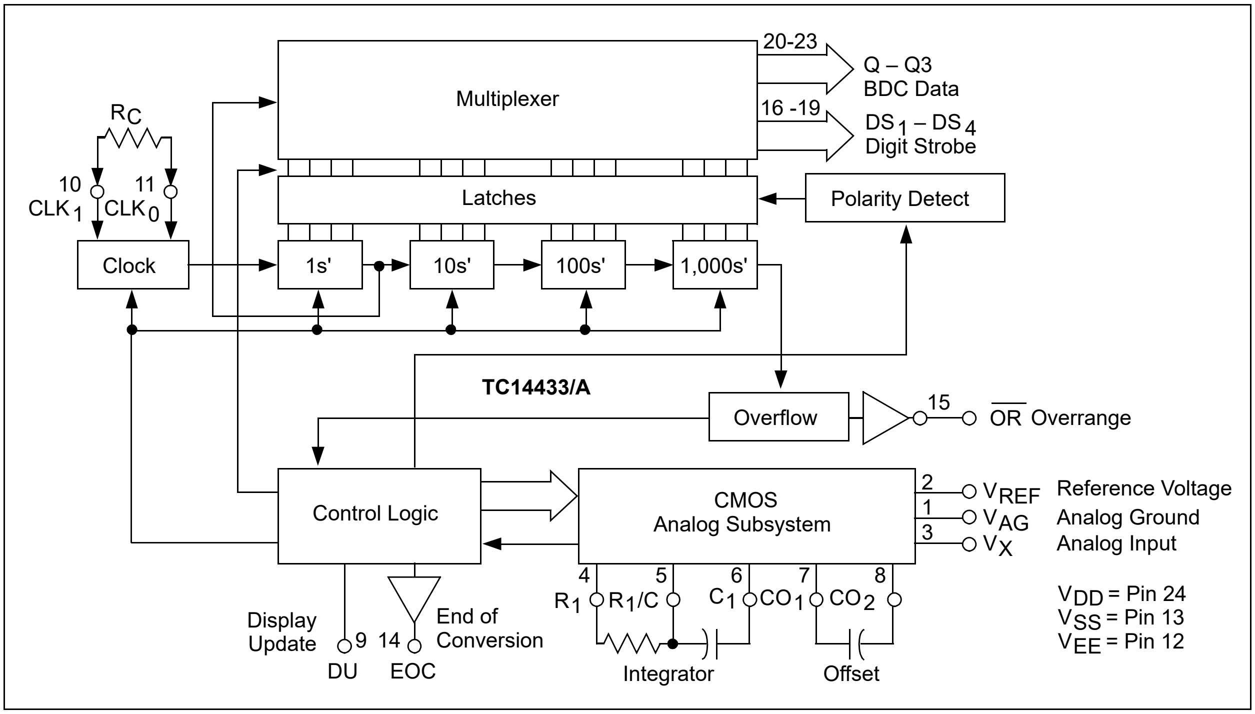


FIGURE 4-3: *Functional Block Diagram.*

5.0 TYPICAL APPLICATIONS

The typical application circuit is an example of a 3-1/2 digit voltmeter using the TC14433 with common-anode displays. This system requires a 2.5-V reference. Full scale may be adjusted to 1.999V or 199.9 mV. Input overrange is indicated by flashing a display. This display uses LEDs with common anode digit lines. Power supply for this system is shown as a dual ±5V supply; however, the TC14433 will operate over a wide voltage range.

The circuit in Figure 5-1 shows a 3-1/2 digit LCD voltmeter. The 14024B provides the low frequency square wave signal drive to the LCD backplane. Dual power supplies are shown here; however, one supply may be used when V_{SS} is connected to V_{EE}. In this case, V_{AG} must be at least 2.8V above V_{EE}.

When only segments b and c of the decoder are connected to the 1/2 digit of the display, 4, 0, 7, and 3 appear as 1.

The overrange indication (Q_3 = 0 and Q_0 = 1) occurs when the count is greater than 1999; (for example, 1.999V for a reference of 2V) The underrange indication, useful for auto-ranging circuits, occurs when the count is less than 180; (for example, 0.180V for a reference of 2V).

Note:	If the most significant digit is connected to a display other than a “1” only, such as a full digit display, segments other than b and c must be disconnected. The BCD to 7-segment decoder must blank on BCD inputs 1010 to 1111 (see Table 5-1).

TABLE 5-1: TRUTH TABLE

Coded Condition of MSD	Q_3	Q_2	Q_1	Q_0	BDC to 7-Segment Decoding	
+0	1	1	1	0	Blank	
-0	1	0	1	0	Blank	
+0 UR	1	1	1	1	Blank	
-0 UR	1	0	1	1	Blank	
+1	0	1	0	0	4 – 1	Hook up only segments b and c to MSD
-1	0	0	0	0	0 – 1	
+1 OR	0	1	1	1	7 – 1	
-1 OR	0	0	1	1	3 – 1	

Note 1: Q_3 – 1/2 digit, low for “1”, high for “0”.
Q_2 – Polarity: “1” = positive, “0” = negative.
Q_0 – Out of range condition exists if Q_0 = 1. When used in conjunction with Q_3, the type of out of range condition is indicated; that is, Q_3 = 0 → OR or Q_3 = 1 → UR.

Figure 5-2 is an example of a 3-1/2 digit LED voltmeter with a minimum of external components (only 11 additional components). In this circuit, the 14511B provides the segment drive and the 75492 or 1413 provides the sink for digit current. Display is blanked during the overrange condition.

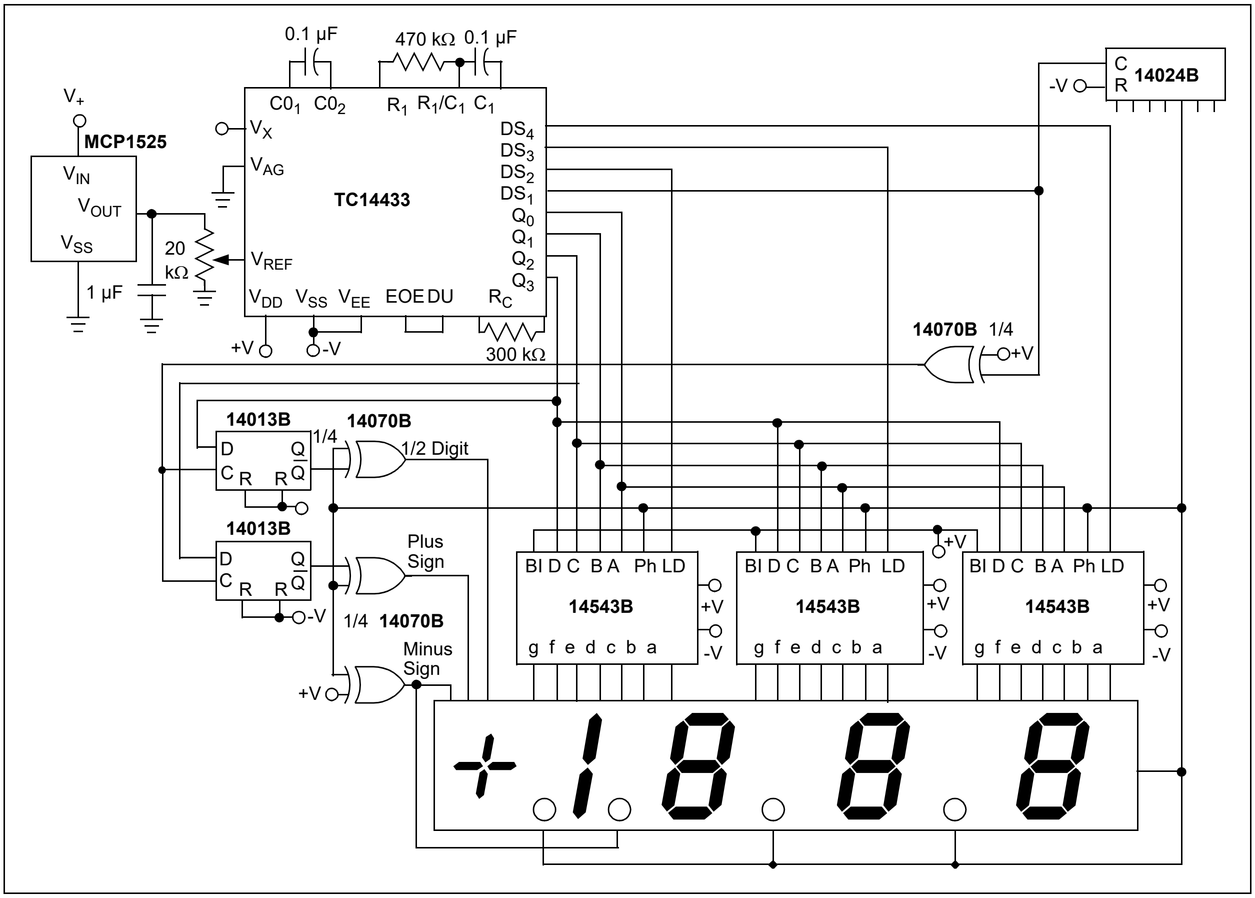
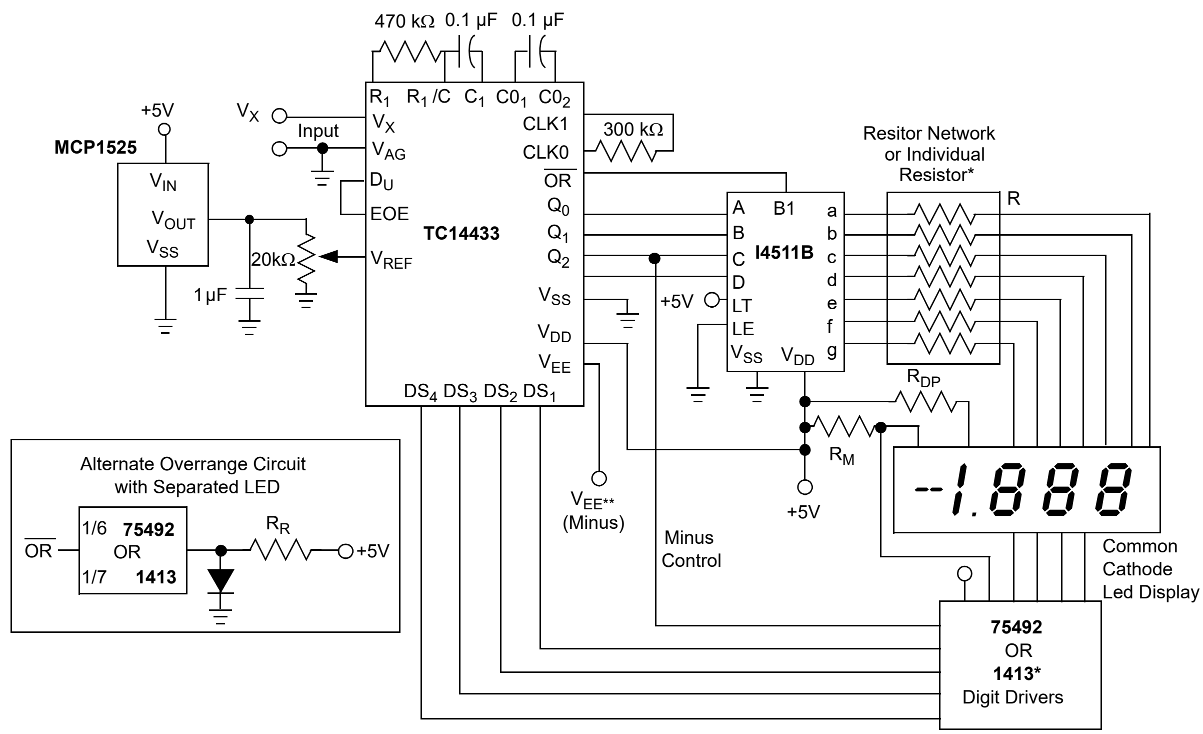


FIGURE 5-1: *3-1/2 Digit Voltmeter with LCD Display.*



Note 1: For V_{REF} = 2000V; V: 1.999V full scale.

2: For V_{REF} = 200 mV; V: 199.9-mV full scale (change 470 kΩ to R = 27 kΩ and decimal point position).

3: Peak digit current for an eight displayed is seven times the segment current:
*To increase the segment current capability, add two 75491 ICs between the 14511B and the resistor network. The use of the 1413 as digit driver increases digit current capability over the 75492.
**V can range between -2.8V and -11V.

FIGURE 5-2: *3-1/2 Digit LED Voltmeter with Low Component Count Using Common Cathode Display.*

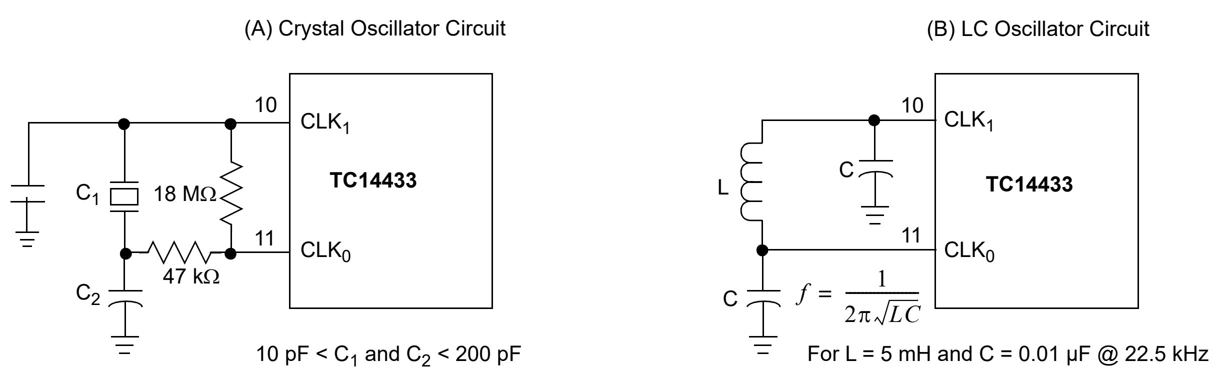


FIGURE 5-3: *Alternate Oscillator Circuits.*

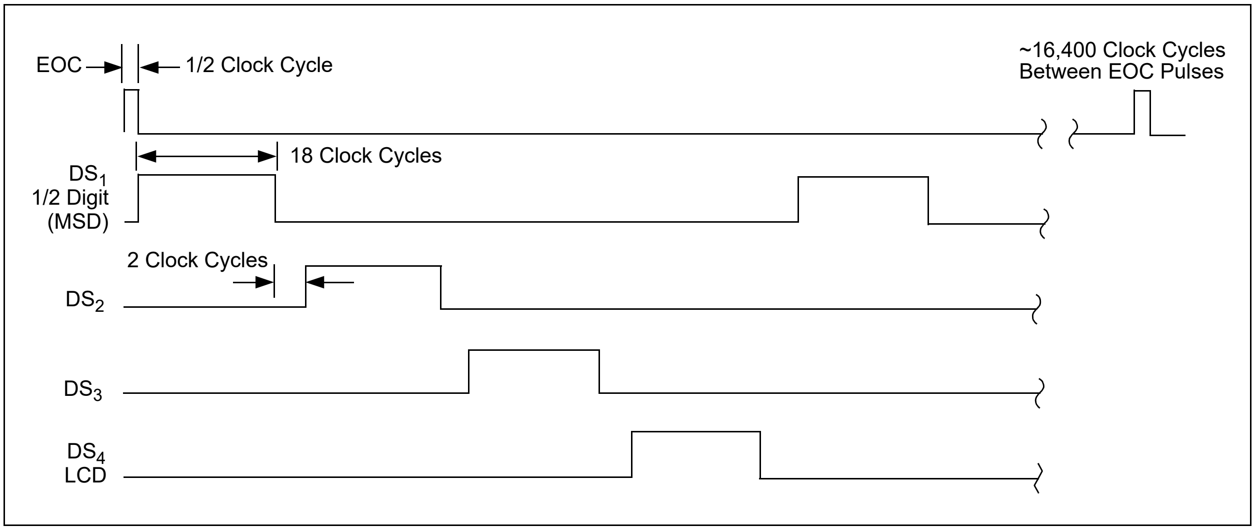
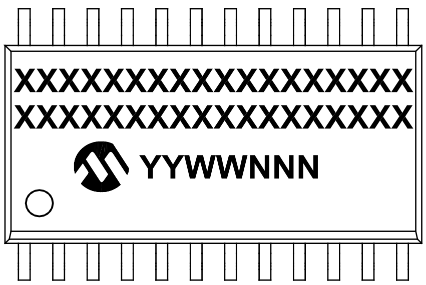


FIGURE 5-4: *Digit Select Timing Diagram.*

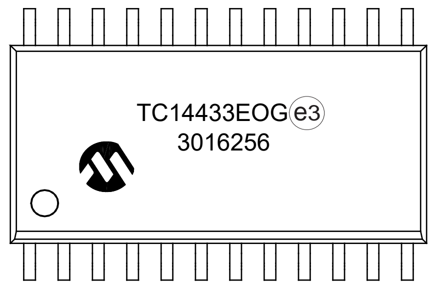
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

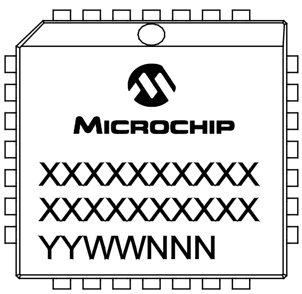
24-Lead SOIC (7.50 mm)



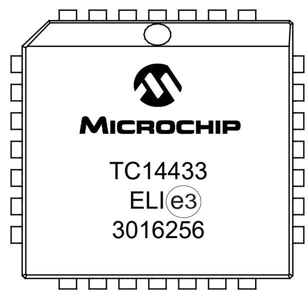
Example



28-Lead PLCC



Example

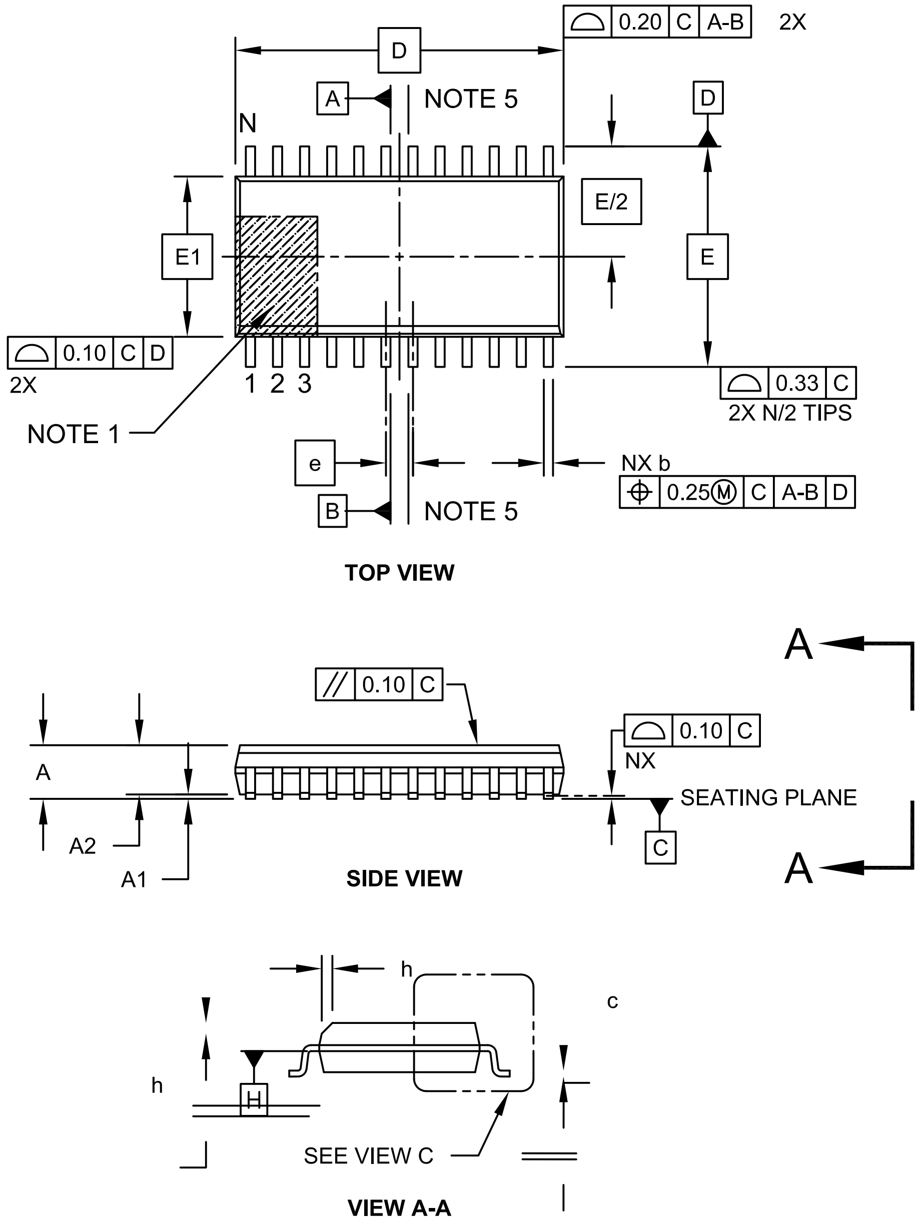


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

24-Lead Plastic Small Outline (OG) - Wide, 7.50 mm Body [SOIC]

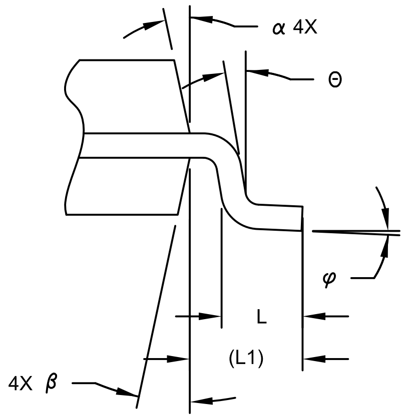
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



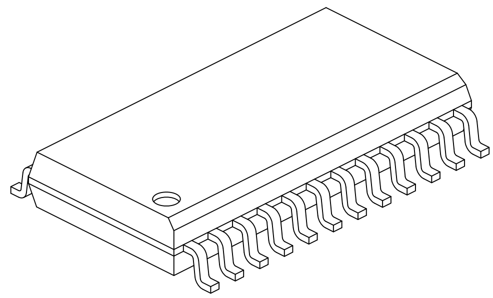
Microchip Technology Drawing C04-025C Sheet 1 of 2

24-Lead Plastic Small Outline (OG) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	24		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E	10.30 BSC		
Molded Package Width	E1	7.50 BSC		
Overall Length	D	15.40 BSC		
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1	1.40 REF		
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.20	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

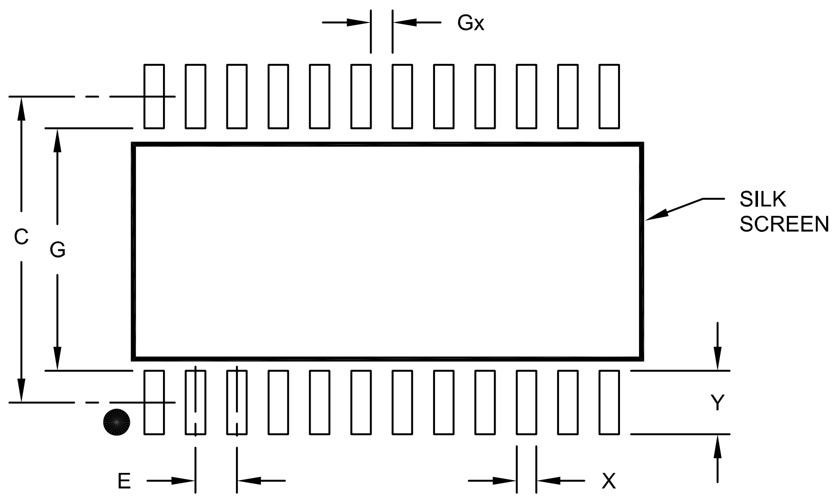
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-025C Sheet 2 of 2

24-Lead Plastic Small Outline (OG) – Wide, 7.50 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		9.40	
Contact Pad Width (X24)	X			0.60
Contact Pad Length (X24)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

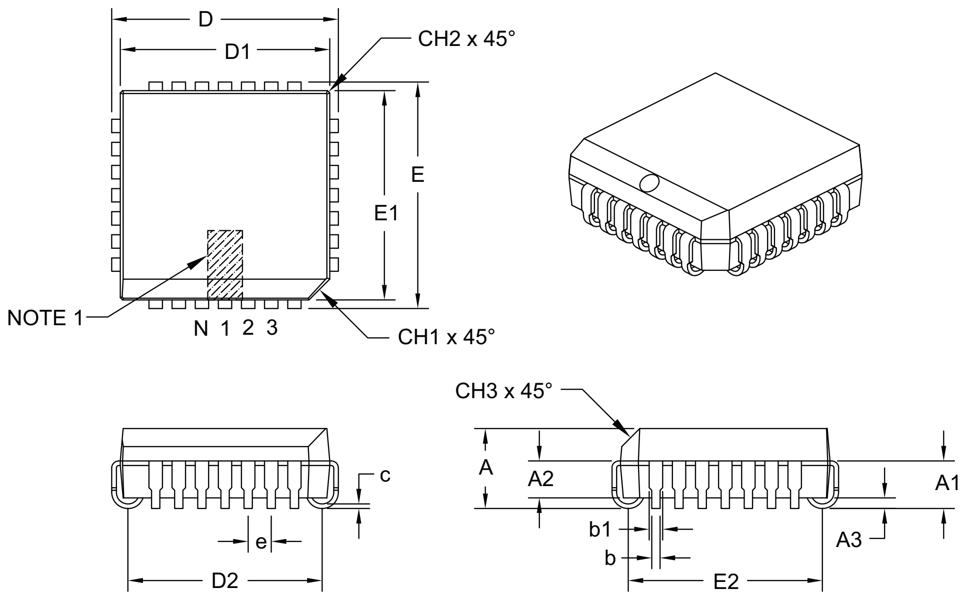
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2025A

28-Lead Plastic Leaded Chip Carrier (LI) – Square [PLCC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



		Units	INCHES		
		Dimension Limits	MIN	NOM	MAX
Number of Pins	N			28	
Pitch	e			.050	
Overall Height	A		.165	.172	.180
Contact Height	A1		.090	.105	.120
Molded Package to Contact	A2		.062	–	.083
Standoff §	A3		.020	–	–
Corner Chamfer	CH1		.042	–	.048
Chamfers	CH2		–	–	.020
Side Chamfer	CH3		.042	–	.056
Overall Width	E		.485	.490	.495
Overall Length	D		.485	.490	.495
Molded Package Width	E1		.450	.453	.456
Molded Package Length	D1		.450	.453	.456
Footprint Width	E2		.382	.410	.438
Footprint Length	D2		.382	.410	.438
Lead Thickness	c		.0075	–	.0125
Upper Lead Width	b1		.026	–	.032
Lower Lead Width	b		.013	–	.021

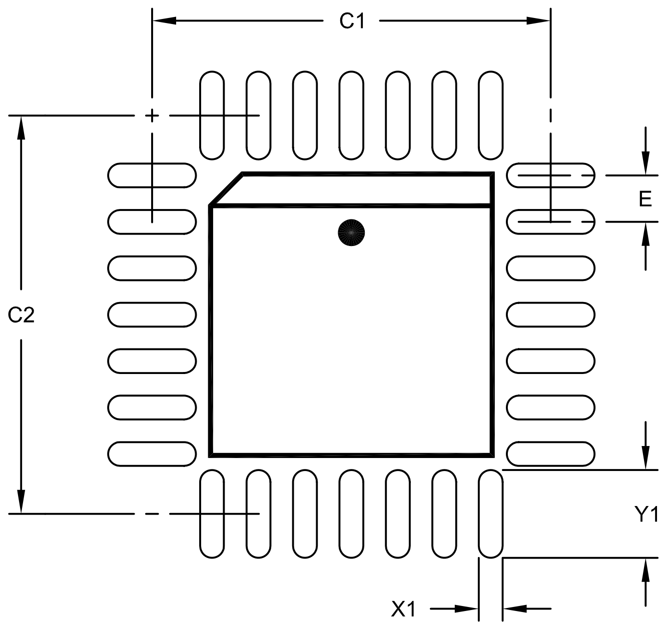
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

Microchip Technology Drawing C04-026B

28-Lead Plastic Leaded Chip Carrier (LI) - Square [PLCC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	.050 BSC		
Contact Pad Spacing	C1		.429	
Contact Pad Spacing	C2		.429	
Contact Pad Width (X28)	X1			.026
Contact Pad Length (X28)	Y1			.094

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2026A

NOTES:

APPENDIX A: REVISION HISTORY

Revision F (April 2018)

The following is the list of modifications:

1. Removed all 24-pin PDIP references as all PDIP packages have reached the end of life.
2. Updated existing device examples in the Product Identification System section.
3. Made minor text changes throughout.

Revision E (August 2016)

The following is the list of modifications:

1. Updated the Temperature Range in the Product Identification System page.

Revision D (July 2008)

The following is the list of modifications:

1. Changed Operating Temperature in Absolute Maximum Ratings to -40°C to +85°C.
2. Added Packaging Marking information.
3. Added Package Outline Drawings.
4. Added **Appendix A: "Revision History"**
5. Added "**Product Identification System".**

Revision C (January 2006)

- Undocumented changes.

Revision B (May 2002)

- Undocumented changes.

Revision A (March 2001)

- Original release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	[X][1]
Device	Temperature Range	Package	Tape and Reel Option

Device:	TC14433:	3 1/2 Digit, A/D Converter
	TC14433A:	3 1/2 Digit, A/D Converter
Tape and Reel Option:	Blank	= Standard packaging (tube or tray)
	713	= Tape and Reel[1]
Temperature Range:	E	= -40°C to +85°C
	C	= -40°C to +70°C
Package:	LI	= Plastic Leaded Chip Carrier, Square, 28-lead
	OG	= Plastic Small Outline, Wide 7.50 mm, 24-lead

Examples:

a) TC14433EOG: 24LD SOIC package

b) TC14433COG: 24LD SOIC package

c) TC14433AELI: 28LD PLCC package

d) TC14433ELI713: Tape and Reel, 28LD PLCC package

e) TC14433AEOG: 24LD SOIC package

Note 1: Tape and Reel identifier appears only in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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