VSC8564-11 Datasheet
Quad-Port 10/100/1000BASE-T PHY with Synchronous Ethernet, Intellisec™, and QSGMII/SGMII MAC

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 4.2

Revision 4.2 was published in May 2019. The following is a summary of the changes in this document.

- The VeriPHY information was updated in the Flexibility section. For more information, see Flexibility, page 3.
- VeriPHY™ Cable Diagnostics section was updated. For more information, see VeriPHY Cable Diagnostics, page 74.
- The VeriPHY Control 1/2/3 sections were removed.
- The references to the VeriPHY were removed from the Extended Registers Page 1 Space table. For more information, see Table 69, page 98.

1.2 Revision 4.1

Revision 4.1 was published in August 2017. The following was a summary of the changes in this document.

- All references to LVDS were clarified to reflect LVDS compatibility.
- All references to serial parallel interface were corrected to serial peripheral interface.
- Operating modes were updated to correctly reflect available functionality. For more information, see Operating Modes, page 5.
- A note was added about the use of recovered clock outputs and fast link failure indication in EEE mode. For more information, see Media Recovered Clock Outputs, page 59 and Fast Link Failure Indication, page 66.
- The equipment loop description was updated to correctly reflect available functionality. For more information, see Equipment Loop, page 73.
- EEE Control register descriptions were updated to indicate sticky bits. For more information, see Table 79, page 105.
- Media/MAC SerDes transmit CRC error counter register descriptions were updated. For more information, see Table 92, page 112.
- Design considerations were updated. For more information, see Design Considerations, page 162.
- Temperature specifications were added to the part ordering information. For more information, see Table 172, page 166.

1.3 Revision 4.0

Revision 4.0 was published in November 2015. It was the first publication of this document

2 Product Overview

VSC8564-11 is a low-power, quad-port Gigabit Ethernet transceiver with four SerDes interfaces for quad-port dual media capability. It also includes an integrated quad-port two-wire serial multiplexer (MUX) to control SFPs or PoE modules. It has a low electromagnetic interference (EMI) line driver, and integrated line side termination resistors that conserve both power and printed circuit board (PCB) space.

The VSC8564-11 device includes Intellisec™, Microsemi's implementation of IEEE 802.1AE 128/256-bit MACsec protocols to meet the security requirements for protecting data traversing Ethernet LANs. It does input classification, frame encryption/decryption, performance, and latency monitoring.

The VSC8564-11 also supports a ring resiliency feature that allows a 1000BASE-T connected PHY port to switch between master and slave timing without having to interrupt the 1000BASE-T link.

Using Microsemi's EcoEthernet v2.0 PHY technology, the VSC8564-11 supports energy efficiency features such as Energy Efficient Ethernet (EEE), ActiPHY link down power savings, and PerfectReach that can adjust power based on the cable length. It also supports fully optimized power consumption in all link speeds.

Microsemi's mixed signal and digital signal processing (DSP) architecture is a key operational feature of the VSC8564-11, assuring robust performance even under less-than-favorable environmental conditions. It supports both half-duplex and full-duplex 10BASE-T, 100BASE-TX, and 1000BASE-T communication speeds over Category 5 (Cat5) unshielded twisted pair (UTP) cable at distances greater than 100 m, displaying excellent tolerance to NEXT, FEXT, echo, and other types of ambient environmental and system electronic noise. The device also supports four dual media ports that can support up to four 100BASE-FX, 1000BASE-X fiber, and/or triple-speed copper SFPs.

The following illustrations show a high-level, general view of typical VSC8564-11 applications.

Figure 1 • **Dual Media Application Diagram**

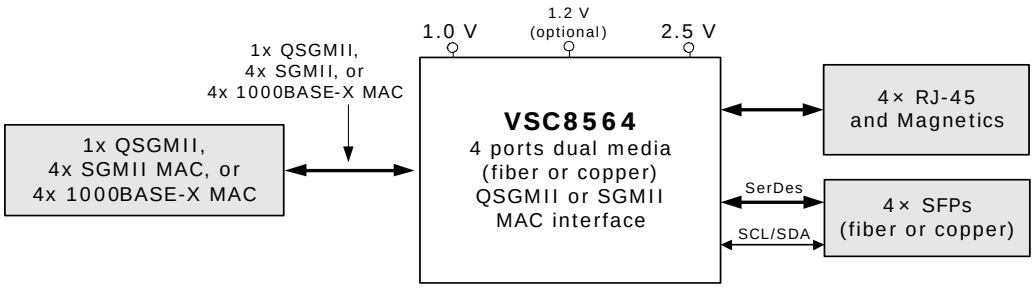


Figure 2 • **Copper Transceiver Application Diagram**

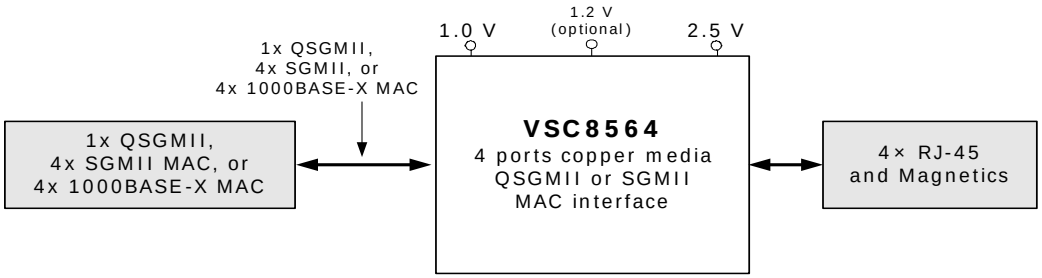
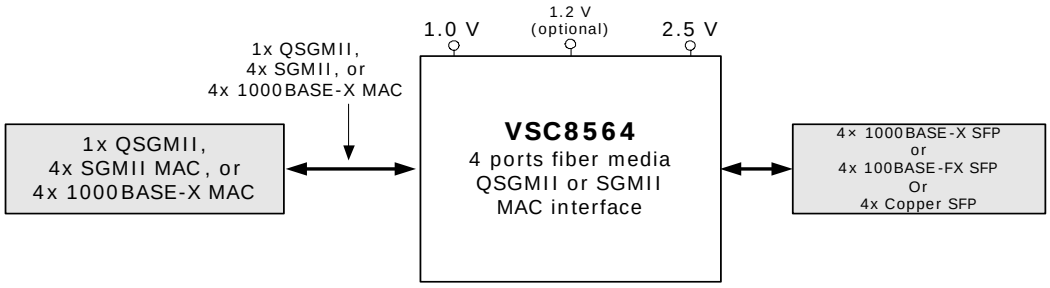


Figure 3 • **Fiber Media Transceiver Application Diagram**



2.1 Key Features

This section lists the main features and benefits of the VSC8564-11 device.

2.1.1 Low Power

- Low power consumption of approximately 425 mW per port in 1000BASE-T mode, 200 mW per port in 100BASE-TX mode, 225 mW per port in 10BASE-T mode, and less than 115 mW per port in 100BASE-FX and 1000BASE-X modes (MACsec adds 250 mW per port to the power consumption)
- ActiPHY™ link down power savings
- PerfectReach™ smart cable reach algorithm
- IEEE 802.3az-2010 Energy Efficient Ethernet idle power savings, even for legacy non-EEE systems

2.1.2 Advanced Carrier Ethernet Support

- Recovered clock outputs with programmable clock squelch control and fast link failure indication (typical <1 ms; worst-case <3 ms) for G.8261 Synchronous Ethernet applications
- Ring resiliency for maintaining linkup integrity when switching between 1000BASE-T master and slave timing
- Supports IEEE 802.3bf timing and synchronization standard
- Integrated quad two-wire serial mux to control SFP and PoE modules
- Support for 802.3ah unidirectional transport for 100BASE-FX and 1000BASE-X fiber media

2.1.3 Wide Range of Support

- Compliant with IEEE 802.3 (10BASE-T, 10BASE-Te, 100BASE-TX, 1000BASE-T, 100BASE-FX, and 1000BASE-X) specifications
- Support for >16 kB jumbo frames in all speeds with programmable synchronization FIFOs
- Supports Cisco QSGMII v1.3, Cisco SGMII v1.9, 1000BASE-X MACs, and IEEE 1149.1 JTAG boundary scan
- Available in a low-cost, 256-pin BGA package with a 17 mm × 17 mm body size

2.1.4 Flexibility

- VeriPHY® cable diagnostics suite provides extensive network cable operating conditions and status
- Patented, low EMI line driver with integrated line side termination resistors
- Four programmable direct-drive LEDs per port with adjustable brightness levels using register controls; bi-color LED support using two LED pins
- Serial LED interface option
- Extensive test features including near end, far end, copper media connector, SerDes MAC/media loopback, and Ethernet packet generator with CRC error counter to decrease time-to-market

Note: All MAC interfaces must be the same — all QSGMII or SGMII.

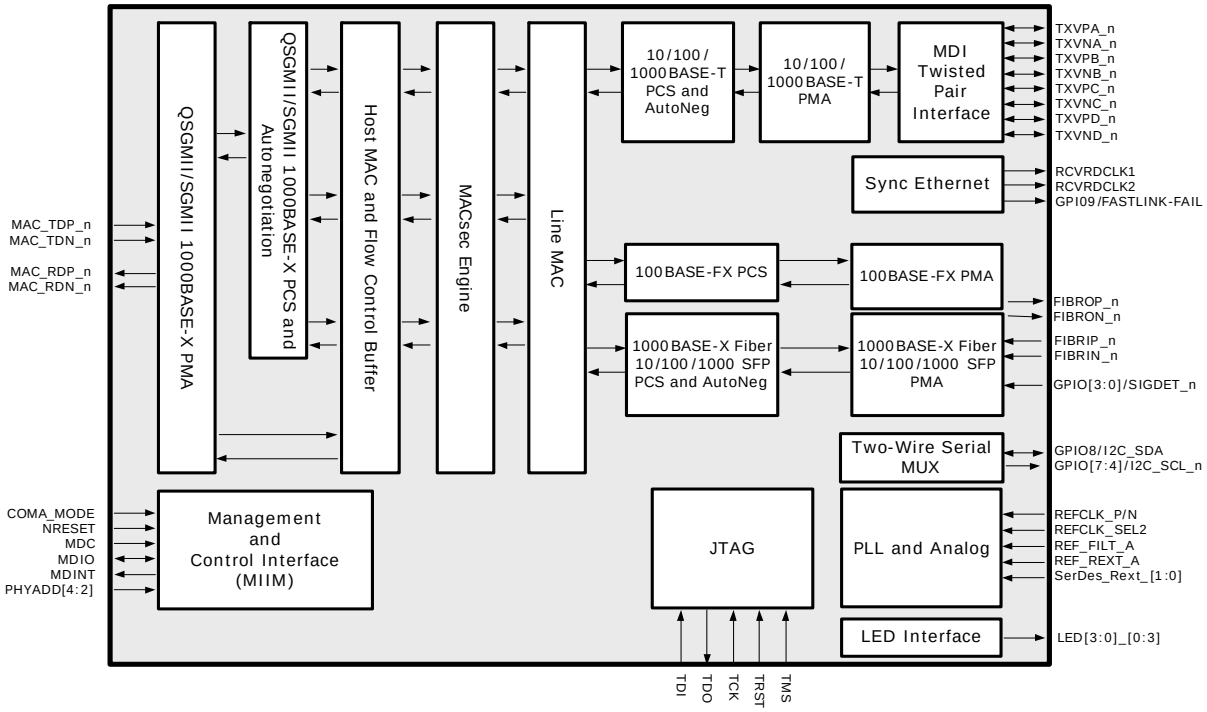
2.1.5 MACsec Encryption

- Fully IEEE 802.1AE-2006 compliant supporting GCM-AES-128, and fully IEEE 802.1AEbn-2011 compliant supporting GCM-AES-256
- Supports full-duplex operation at all speeds
- VLAN and MPLS header bypassing
- 16 secure associations (SA) per port

2.2 Block Diagram

The following illustration shows the primary functional blocks of the VSC8564-11 device.

Figure 4 • **Block Diagram**



Note: All MAC interfaces must be the same—all QSGMII, SGMII, or 1000BASE-X.

3 Functional Descriptions

This section describes the functional aspects of the VSC8564-11 device, including available configurations, operational features, and testing functionality. It also defines the device setup parameters that configure the device for a particular application.

3.1 Operating Modes

The following table lists the operating modes of the VSC8564-11 device.

Table 1 • **Operating Modes**

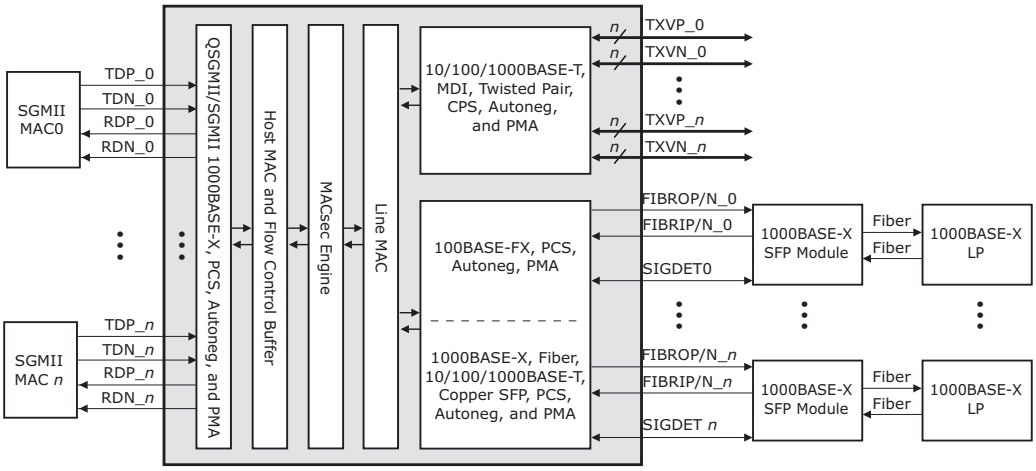
Operating Mode	Supported Media	Notes
QSGMII/SGMII MAC-to-1000BASE-X Link Partner	1000BASE-X	See Figure 5, page 5.
QSGMII/SGMII MAC-to-100BASE-FX Link Partner	100BASE-FX	See Figure 7, page 6.
QSGMII/SGMII MAC-to-AMS and 1000BASE-X SerDes	1000BASE-X, 10/100/1000BASE-T	See Figure 8, page 7.
QSGMII/SGMII MAC-to-AMS and 100BASE-FX SerDes	100BASE-FX, 10/100/1000BASE-T	See Figure 9, page 8.
QSGMII/SGMII MAC-to-AMS and Protocol Transfer Mode	SFP/Fiber protocol transfer mode (10/100/1000BASE-T Cu SFP), 10/100/1000BASE-T	See Figure 10, page 8.
QSGMII/SGMII MAC-to-Cat5 Link Partner	10/100/1000BASE-T	See Figure 11, page 9.
QSGMII/SGMII MAC-to-Protocol Transfer Mode	SFP/Fiber protocol transfer mode (10/100/1000BASE-T Cu SFP)	See Figure 12, page 9.
1000BASE-X MAC to Cat5 Link Partner	1000BASE-T only	See Figure 13, page 10.

Note: All MAC interfaces must be the same — all QSGMII or SGMII.

3.1.1 QSGMII/SGMII MAC to 1000BASE-X Link Partner

The following illustrations show the register settings used to configure a QSGMII/SGMII MAC to 1000BASE-X link partner.

Figure 5 • **SGMII MAC to 1000BASE-X Link Partner**

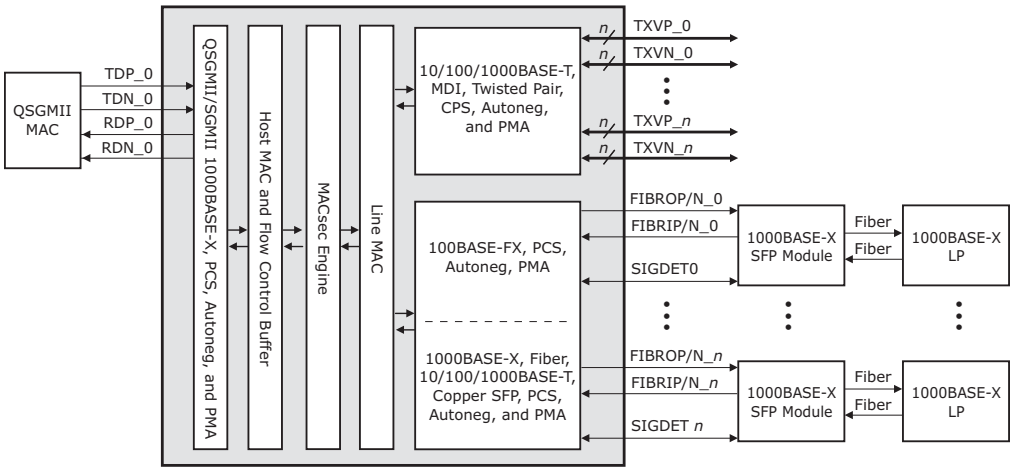


3.1.1.1 MAC Interface SGMII

- Set register 19G bits 15:14 = 00

- Set Register 23 (main register) bit 12 = 0
- Set Register 18G = 0x80F0.

Figure 6 • **QSGMII MAC to 1000BASE-X Link Partner**



3.1.1.2 MAC Interface QSGMII

- Set register 19G bits 15:14 = 01
- Set Register 23 (main register) bit 12 = 0
- Set Register 18G = 0x80E0. For more information, see Table 109, page 121.

3.1.1.3 Media Interface 1000BASE-X SFP Fiber (1000BASE-X Link Partner)

- Set register 23 bits 10:8 = 010
- Set register 0 bit 12 = 1 (enable autonegotiation)
- Set Register 18G = 0x8FC1. For more information, see Table 109, page 121.

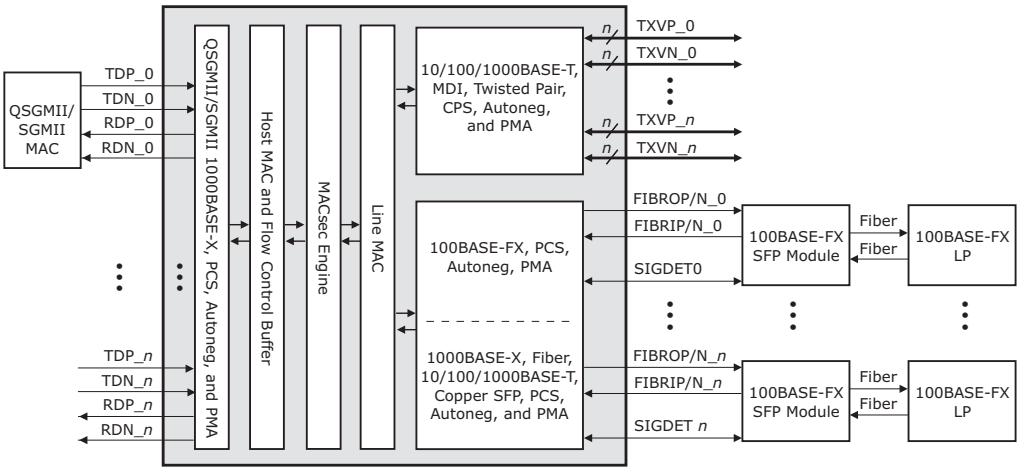
The F in 0x8FC1 identifies the port. To exclude a port from the configuration, set its bit to 0. For example, the configuration of port 0 and port 1 to 1000BASE-X is 0011 or 3, making the bit setting 0x83C1.

Note: Whenever there is a mode change in register 23, a software reset (register 0 bit 15) is required to make the mode change effective. This register will read the currently active mode and not what was just written.

3.1.2 QSGMII/SGMII MAC to 100BASE-FX Link Partner

The following illustration shows the register settings used to configure a QSGMII/SGMII MAC to 100BASE-FX link partner.

Figure 7 • **QSGMII/SGMII MAC to 100BASE-FX Link Partner**



3.1.2.1 Media Interface 100BASE-FX SFP Fiber (100BASE-FX Link Partner)

- Set register 23 bits 10:8 = 011
- Set register 0 bit 12 = 0 (autonegotiation not present in 100BASE-FX PHY)
- Set Register 18G = 0x8FD1. For more information, see Table 109, page 121.

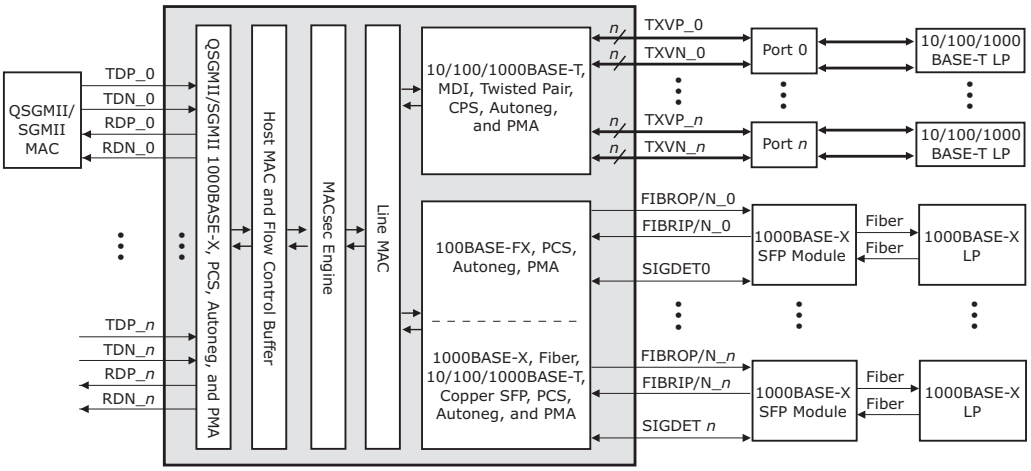
For QSGMII, only port 0 is used.

Note: Whenever there is a mode change, a software reset (register 0 bit 15) is required to make the mode change effective. This register is cleared when read.

3.1.3 QSGMII/SGMII MAC to AMS and 1000BASE-X Media SerDes

The following illustration shows the register settings used to configure a QSGMII/SGMII MAC to AMS and 1000BASE-X media SerDes.

Figure 8 • **QSGMII/SGMII MAC to AMS and 1000BASE-X Media SerDes**



3.1.3.1 Media Interface 1000BASE-X SFP Fiber (1000BASE-X Link Partner)

- Set register 23 bits 10:8 = 010
- Set register 0 bit 12 = 1 (enable autonegotiation)

3.1.3.2 AMS Preference Setup

- Set register 23 bit 10 = 1 (enable AMS)
- Set register 23 bit 11 to the port preferences

The media selected by AMS can be read from register 20E1 bits 7:6. For more information, see Table 25, page 54.

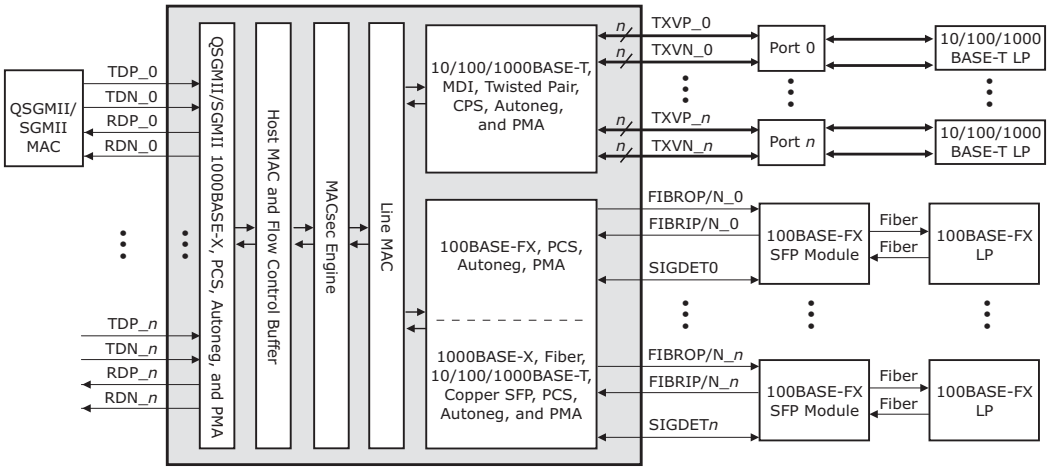
For QSGMII, only port 0 is used.

Note: Whenever there is a mode change, a software reset (register 0 bit 15) is required to make the mode change effective. This register is cleared when read.

3.1.4 QSGMII/SGMII MAC to AMS and 100BASE-FX Media SerDes

The following illustration shows the register settings used to configure a QSGMII/SGMII MAC to AMS and 100BASE-FX media SerDes.

Figure 9 • **QSGMII/SGMII MAC to AMS and 100BASE-FX Media SerDes**



3.1.4.1 Media Interface 100BASE-FX SFP Fiber (100BASE-FX Link Partner)

- Set register 23 bits 10:8 = 011
- Set register 0 bit 12 = 1 (enable autonegotiation)

3.1.4.2 AMS Preference Setup

- Set register 23 bit 10 = 1 (enable AMS)
- Set register 23 bit 11 to the port preferences

The media selected by AMS can be read from register 20E1 bits 7:6. For more information, see Table 25, page 54.

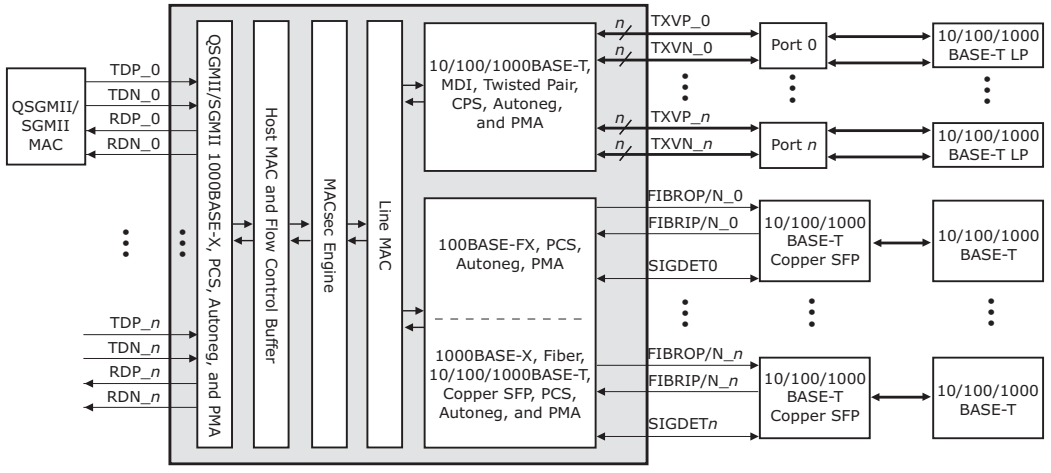
For QSGMII, only port 0 is used.

Note: Whenever there is a mode change, a software reset (register 0 bit 15) is required to make the mode change effective. This register is cleared when read.

3.1.5 QSGMII/SGMII MAC-to-AMS and Protocol Transfer Mode

The following illustration shows the register settings used to configure a QSGMII/SGMII MAC-to-AMS and Protocol Transfer mode.

Figure 10 • **QSGMII/SGMII MAC-to-AMS and Protocol Transfer Mode**



3.1.5.1 Media Interface 10/100/1000BASE-T Cu-SFP

- Set register 23 bits 10:8 = 001
- Set register 23 bit 12 = 0
- Set register 0 bit 12 = 1 (enable autonegotiation)

3.1.5.2 AMS Preference Setup

- Set register 23 bit 10 = 1 (enable AMS)
- Set register 23 bit 11 to the port preferences

The media selected by AMS can be read from register 20E1 bits 7:6. For more information, see Table 25, page 54.

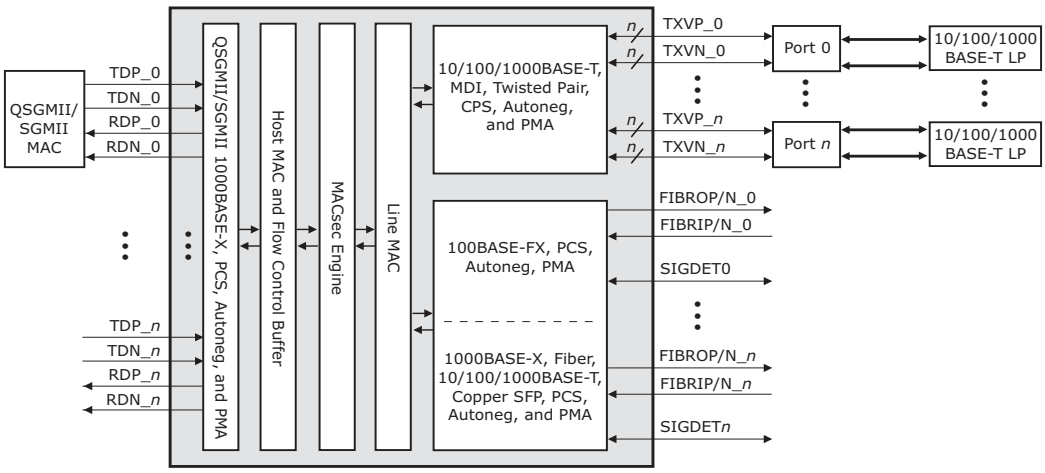
For QSGMII, only port 0 is used.

Note: Whenever there is a mode change, a software reset (register 0 bit 15) is required to make the mode change effective. This register is cleared when read.

3.1.6 QSGMII/SGMII MAC to Cat5 Link Partner

The following illustration shows the register settings used to configure a QSGMII/SGMII MAC to Cat5 link partner.

Figure 11 • **QSGMII/SGMII MAC to Cat5 Link Partner**



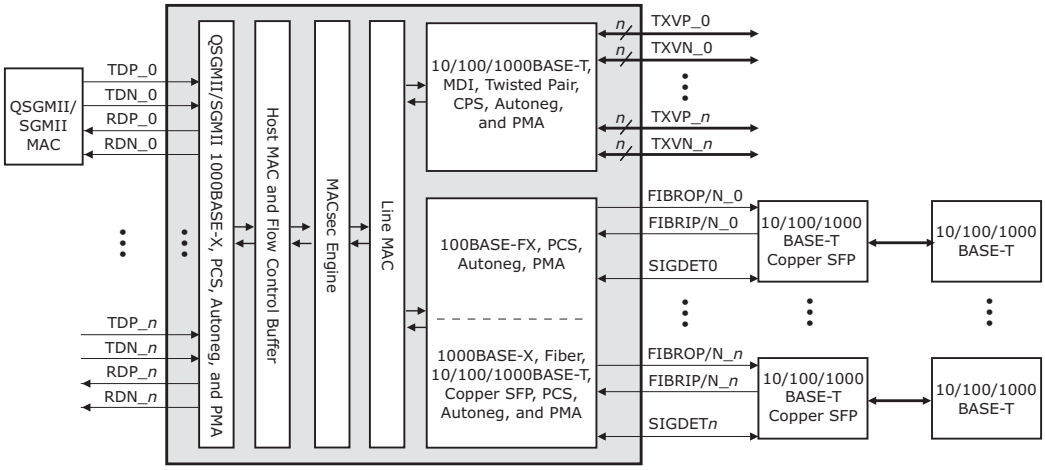
For QSGMII, only port 0 is used.

Note: Whenever there is a mode change, a software reset (register 0 bit 15) is required to make the mode change effective. This register is cleared when read.

3.1.7 QSGMII/SGMII MAC-to-Protocol Transfer Mode

The following illustration shows the register settings used to configure a QSGMII/SGMII MAC to Protocol Transfer Mode.

Figure 12 • **QSGMII/SGMII MAC to Protocol Transfer Mode**



3.1.7.1 Media Interface 10/100/1000BASE-T Cu SFP

- Set register 23 bits 10:8 = 001
- Set register 23 bit 11 = 0
- Set register 0 bit 12 = 1 (enable autonegotiation)

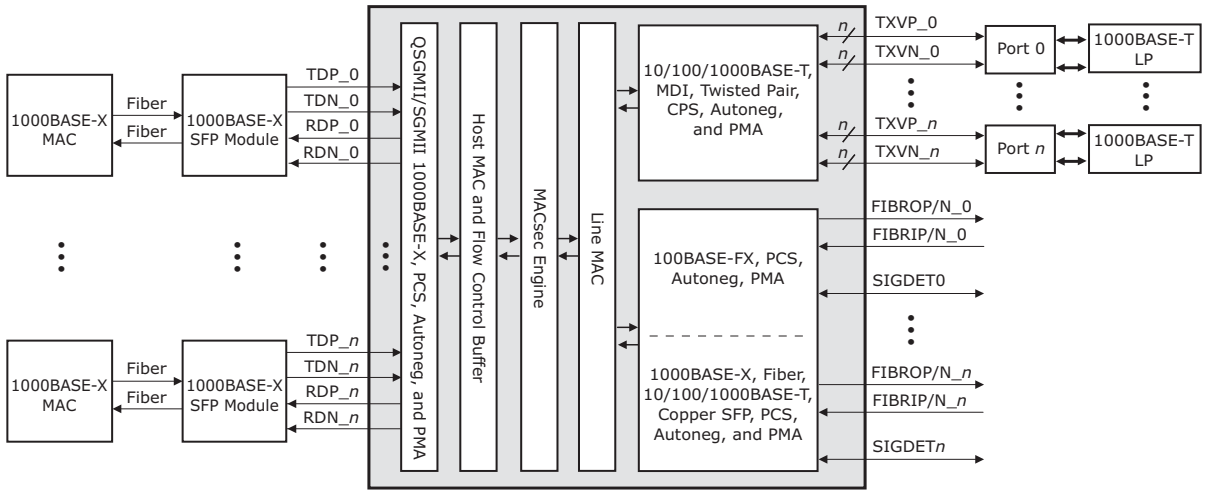
For QSGMII, only port 0 is used.

Note: Whenever there is a mode change, a software reset (register 0 bit 15) is required to make the mode change effective. This register is cleared when read.

3.1.8 1000BASE-X MAC to Cat5 Link Partner

The following illustration shows the register settings used to configure a 1000BASE-X MAC to Cat5 link partner.

Figure 13 • **1000BASE-X MAC to Cat5 Link Partner**



In this mode, the device provides data throughput of 1000 Mbps only.

3.1.8.1 MAC Interface

- Set Register 18G = 0x80F0 to configure the 1000BASE-X MAC SerDes. For more information, see Table 109, page 121.
- Set register 19G bits 15:14 = 00
- Set Register 23 (main register) bit 12 = 1

3.1.8.2 Clause 37 MAC Autonegotiation

- Set Register 16E3 bit 7 = 1

Note: Whenever there is a mode change, a software reset (register 0 bit 15) is required to make the mode change effective. This register is cleared when read.

3.2 SerDes MAC Interface

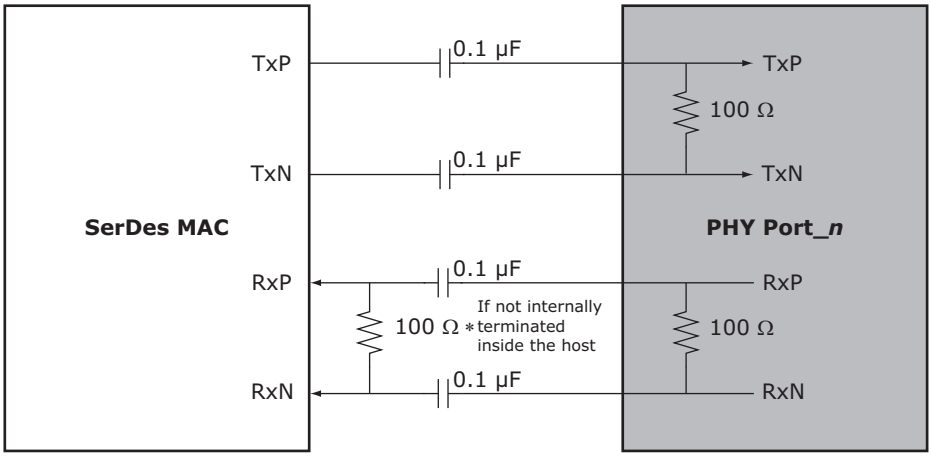
The VSC8564-11 SerDes MAC interface performs data serialization and deserialization functions using an integrated SerDes block. The interface operates in 1000BASE-X compliant mode, QSGMII mode, or SGMII mode. Register 19G is a global register and needs to be set once to configure the device to the desired mode. The other register bits are configured on a per-port basis and the operation either needs to be repeated for each port, or a broadcast write needs to be used by setting register 22, bit 0 to configure all the ports simultaneously. The SerDes and enhanced SerDes blocks have the termination resistor integrated into the device.

3.2.1 1000BASE-X MAC

When connected to a SerDes MAC compliant to 1000BASE-X, the VSC8564-11 device provides data throughput at a rate of 1000 Mbps only; 10 Mbps and 100 Mbps rates are not supported. To configure the device for SerDes MAC mode, set register 19G, bits 15:14 = 0, and register 23, bit 12 = 1. The device also supports 1000BASE-X Clause 37 MAC-side autonegotiation and is enabled through register 16E3,

bit 7. To configure the rest of the device for 1000 Mbps operation, select 1000BASE-T only by disabling the 10BASE-T/100BASE-TX advertisements in register 4.

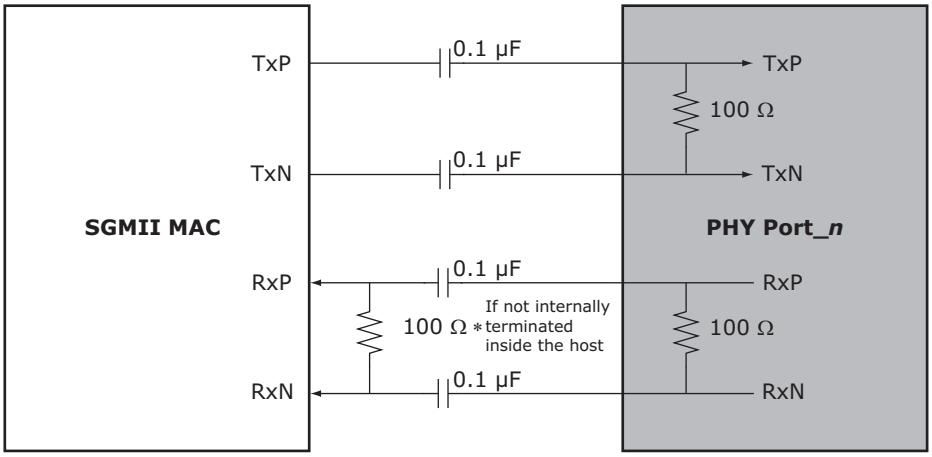
Figure 14 • **SerDes MAC Interface**



3.2.2 SGMII MAC

When configured to detect and switch between 10BASE-T, 100BASE-T, and 1000BASE-T data rates, the VSC8564-11 device can be connected to an SGMII-compatible MAC. To configure the device for SGMII MAC mode, set register 19G, bits 15:14 = 00 and register 23, bit 12 = 0. In addition, set register 18G as desired. This device also supports SGMII MAC-side autonegotiation and is enabled through register 16E3, bit 7.

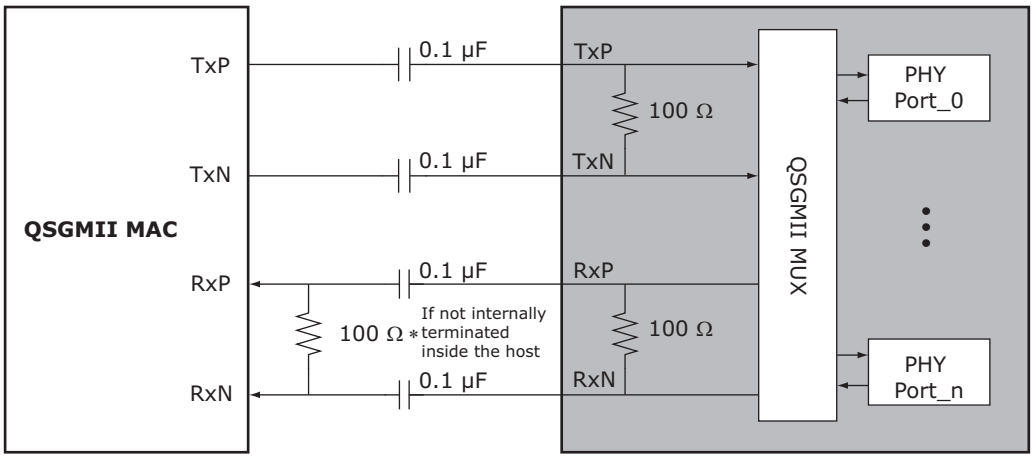
Figure 15 • **SGMII MAC Interface**



3.2.3 QSGMII MAC

The VSC8564-11 device supports a QSGMII MAC to convey four ports of network data and port speed between 10BASE-T, 100BASE-T, and 1000BASE-T data rates and operates in both half-duplex and full-duplex at all port speeds. The MAC interface protocol for each port within QSGMII can be either 1000BASE-X or SGMII, if the QSGMII MAC that the VSC8564-11 is connecting to supports this functionality. To configure the device for QSGMII MAC mode, set register 19G, bits 15:14 = 01. In addition, set register 18G as desired. The device also supports SGMII MAC-side autonegotiation on each individual port and is enabled through register 16E3, bit 7, of that port.

Figure 16 • **QSGMII MAC Interface**



3.3 SerDes Media Interface

The VSC8564-11 device SerDes media interface performs data serialization and deserialization functions using an integrated SerDes block in the SerDes media interface. The interface operates at 1.25 Gbps speed, providing full-duplex and half-duplex for 10/100/1000 Mbps bandwidth that can connect directly to 100BASE-FX/1000BASE-X-compliant optical devices as well as to 10/100/1000BASE-T copper SFP devices. The interface also provides support for unidirectional transport as defined in IEEE 802.3-2008, Clause 66. The SerDes interface has the following operating modes:

- QSGMII/SGMII to 1000BASE-X
- QSGMII/SGMII to 100BASE-FX
- QSGMII/SGMII to SGMII/1000BASE-X protocol transfer

The SerDes media block has the termination resistor integrated into the device. A software reset through register 0, bit 15 is required when changing operating modes between 100BASE-FX and 1000BASE-X.

3.3.1 QSGMII/SGMII to 1000BASE-X

The 1000BASE-X SerDes media in QSGMII/SGMII mode supports IEEE 802.3 Clause 36 and Clause 37, which describe 1000BASE-X fiber autonegotiation. In this mode, control and status of the SerDes media is displayed in the VSC8564-11 device registers 0 through 15 in a manner similar to what is described in IEEE 802.3 Clause 28. In this mode, connected copper SFPs can only operate at 1000BASE-T speed. A link in this mode is established using autonegotiation (enabled or disabled) between the PHY and the link partner. To configure the PHY in this mode, set register 23, bits 10:8 = 010. To configure 1000BASE-X autonegotiation for this mode, set register 0, bit 12. Setting this mode and configurations can be performed individually on each of the four ports. Ethernet packet generator (EPG), cyclical redundancy check (CRC) counters, and loopback modes are supported in 1000BASE-X mode.

3.3.2 QSGMII/SGMII to 100BASE-FX

The VSC8564-11 supports 100BASE-FX communication speed for connecting to fiber modules such as GBICs and SFPs. This capability is facilitated by using the connections on the SerDes pins when connected to a MAC through QSGMII/SGMII. Ethernet packet generator (EPG), cyclical redundancy check (CRC) counters, and loopback modes are supported in the 100BASE-FX mode. Setting this mode and configurations can be performed individually on each of the four ports. To configure the PHY in this mode, set register 23, bits 10:8 = 011.

3.3.3 QSGMII to SGMII Protocol Conversion

QSGMII to SGMII (protocol transfer) mode is a feature that links a fiber module or triple speed 10/100/1000-T copper SFP to the QSGMII MAC through the VSC8564-11 device. SGMII can be converted to QSGMII with protocol conversion using this mode.

To configure the PHY in this mode, set register 23, bits 10:8 = 001. To establish the link, assert the relevant signal detect pins.

All relevant LED modes are supported except for collision, duplex, and autonegotiation fault. The triple-speed copper SFP's link status and data type plugged into the port can be indicated by the PHY's LEDs. Setting this particular mode and configuration can be performed individually on each of the four ports within a QSGMII grouping.

3.3.4 Unidirectional Transport for Fiber Media

The VSC8564-11 device supports IEEE 802.3ah for unidirectional transport across its 1000BASE-X and 100BASE-FX fiber media. This feature enables transmission across fiber media, regardless of whether the PHY has determined that a valid link has been established (register 1, bit 2). The only valid operating modes for unidirectional fiber mode are 100BASE-FX or 1000BASE-X fiber media.

To enable this feature, set register 0, bit 5 to 1. For status of the unidirectional ability, read register 1, bit 7.

Note: Automatic media sensing does not work with this feature. In addition, because unidirectional fiber media must have autonegotiation disabled, SGMII autonegotiation must also be disabled (register 16E3, bit 7 = 0).

3.4 PHY Addressing and Port Mapping

This section contains information about PHY addressing and port mapping.

3.4.1 PHY Addressing

The VSC8564-11 includes four external PHY address pins, PHYADD[4:1], to allow control of multiple PHY devices on a system board sharing a common management bus. These pins, with the physical address of the PHY, form the PHY address port map. The equation [{PHYADD[4:1], 1'b0} + physical address of the port (0 to 3)], and the setting of PHY address reversal bit in register 20E1, bit 9, determine the PHY address.

3.4.2 SerDes Port Mapping

The VSC8564-11 includes seven 1.25 GHz SerDes macros and one 5 GHz enhanced SerDes macro. Three of the seven SerDes macros are configured as SGMII MAC interfaces and the remaining four are configured as 1000BASE-X/100BASE-FX SerDes media interfaces. The enhanced SerDes macro can be configured as either a QSGMII MAC interface or the fourth SGMII MAC interface. The following table shows the different operating modes based on the settings of register 19G, bits 15:14.

Table 2 • **MAC Interface Mode Mapping**

19G[15:14]	Operating Mode
00	SGMII
01	QSGMII
10	Reserved
11	Reserved

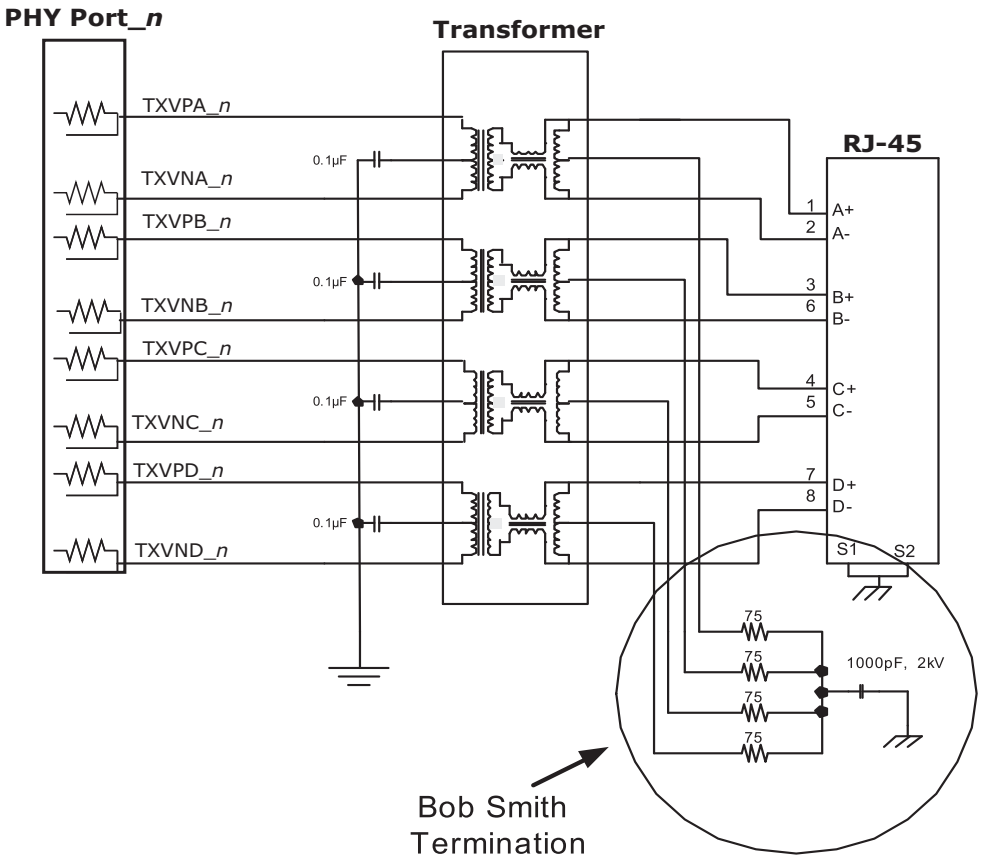
3.5 Cat5 Twisted Pair Media Interface

The VSC8564-11 twisted pair interface is compliant with IEEE 802.3-2008 and the IEEE 802.3az-2010 standard for energy efficient Ethernet.

3.5.1 Voltage Mode Line Driver

Unlike many other gigabit PHYs, the VSC8564-11 uses a patented voltage mode line driver that allows it to fully integrate the series termination resistors, which are required to connect the PHY's Cat5 interface to an external 1:1 transformer. Also, the interface does not require the user to place an external voltage on the center tap of the magnetic. The following illustration shows the connections.

Figure 17 • **Cat5 Media Interface**



3.5.2 Cat5 Autonegotiation and Parallel Detection

The VSC8564-11 supports twisted pair autonegotiation, as defined by IEEE 802.3-2008 Clause 28 and IEEE 802.3az-2010. The autonegotiation process evaluates the advertised capabilities of the local PHY and its link partner to determine the best possible operating mode. In particular, autonegotiation can determine speed, duplex configuration, and master or slave operating modes for 1000BASE-TX. Autonegotiation also enables a connected MAC to communicate with its link partner MAC through the VSC8564-11 using optional next pages, which set attributes that may not otherwise be defined by the IEEE standard.

If the Category 5 (Cat5) link partner does not support autonegotiation, the VSC8564-11 automatically uses parallel detection to select the appropriate link speed.

Autonegotiation is disabled by clearing register 0, bit 12. When autonegotiation is disabled, the state of register bits 0.6, 0.13, and 0.8 determine the device operating speed and duplex mode.

Note: While 10BASE-T and 100BASE-TX do not require autonegotiation, Clause 40 has defined 1000BASE-T to require autonegotiation.

3.5.3 Automatic Crossover and Polarity Detection

For trouble-free configuration and management of Ethernet links, the VSC8564-11 includes a robust automatic crossover detection feature for all three speeds on the twisted pair interface (10BASE-T, 100BASE-T, and 1000BASE T). Known as HP Auto-MDIX, the function is fully compliant with Clause 40 of IEEE 802.3-2008.

Additionally, the device detects and corrects polarity errors on all MDI pairs — a useful capability that exceeds the requirements of the standard.

Both HP Auto-MDIX detection and polarity correction are enabled in the device by default. Default settings can be changed using device register bits 18.5:4. Status bits for each of these functions are located in register 28.

Note: The VSC8564-11 can be configured to perform HP Auto-MDIX, even when autonegotiation is disabled and the link is forced into 10/100 speeds. To enable this feature, set register 18.7 to 0. To use the feature, also set register 0.12 to 0.

The HP Auto-MDIX algorithm successfully detects, corrects, and operates with any of the MDI wiring pair combinations listed in the following table, which shows that twisted pair A (of four twisted paris A, B, C, and D) is connected to the RJ45 connector 1,2 in normal MDI mode.

Table 3 • **Supported MDI Pair Combinations**

RJ45 Connections				
1, 2	**3, 6**	**4, 5**	**7, 8**	**Mode**
A	B	C	D	Normal MDI
B	A	D	C	Normal MDI-X
A	B	D	C	Normal MDI with pair swap on C and D pair
B	A	C	D	Normal MDI-X with pair swap on C and D pair

3.5.4 Manual MDI/MDIX Setting

As an alternative to HP Auto-MDIX detection, the PHY can be forced to be MDI or MDI-X using register 19E1, bits 3:2. Setting these bits to 10 forces MDI and setting 11 forces MDI-X. Leaving the bits 00 enables the HP Auto-MDIX setting to be based on register 18, bits 7 and 5.

3.5.5 Link Speed Downshift

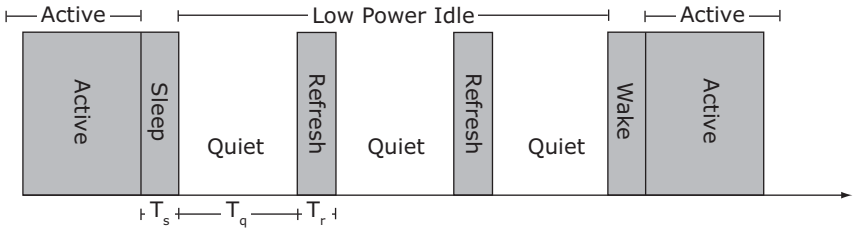
For operation in cabling environments that are incompatible with 1000BASE-T, the VSC8564-11 provides an automatic link speed downshift option. When enabled, the device automatically changes its 1000BASE-T autonegotiation advertisement to the next slower speed after a set number of failed attempts at 1000BASE-T. No reset is required to get out of this state when a subsequent link partner with 1000BASE-T support is connected. This feature is useful in setting up in networks using older cable installations that include only pairs A and B, and not pairs C and D.

To configure and monitor link speed downshifting, set register 20E1, bits 4:1. For more information, see Table 73, page 100.

3.5.6 Energy Efficient Ethernet

The VSC8564-11 supports the IEEE 802.3az-2010 Energy Efficient Ethernet standard. This standard provides a method for reducing power consumption on an Ethernet link during times of low utilization. It uses low power idles (LPI) to achieve this objective.

Figure 18 • **Low Power Idle Operation**



Using LPI, the usage model for the link is to transmit data as fast as possible and then return to a low power idle state. Energy is saved on the link by cycling between active and low power idle states. During LPI, power is reduced by turning off unused circuits and using this method, energy use scales with bandwidth utilization.

The VSC8564-11 uses LPI to optimize power dissipation in 100BASE-TX and 1000BASE-T modes of operation. In addition, the IEEE 802.3az-2010 standard defines a 10BASE-Te mode that reduces transmit signal amplitude from 5 V peak-to-peak to approximately 3.3 V peak-to-peak. This mode reduces power consumption in 10 Mbps link speed and fully interoperates with legacy 10BASE-T compliant PHYs over 100 m Cat5 cable or better.

To configure the VSC8564-11 in 10BASE-Te mode, set register 17E2.15 to 1 for each port. Additional energy efficient Ethernet features are controlled through Clause 45 registers. For more information, see Clause 45 Registers to Support Energy Efficient Ethernet and 802.3bf, page 126.

3.5.7 Ring Resiliency

Ring resiliency changes the timing reference between the master and slave PHYs without altering the master/slave configuration in 1000BASE-T mode. The master PHY transmitter sends data based on the local clock and initiates timing recovery in the receiver. The slave PHY instructs node to switch the local timing reference to the recovered clock from other PHYs in the box, freezes timing recovery, and locks clock frequency for the transmitter. The master PHY makes a smooth transition to transmission from local clock to recovered clock after timing lock is achieved.

Ring resiliency can be used in synchronous Ethernet systems, because the local clocks in each node are synchronized to a grandmaster clock.

Note: For ring resiliency to successfully exchange master/slave timing over 1000BASE-T, the link partner must also support ring resiliency.

3.6 MACsec Block Operation

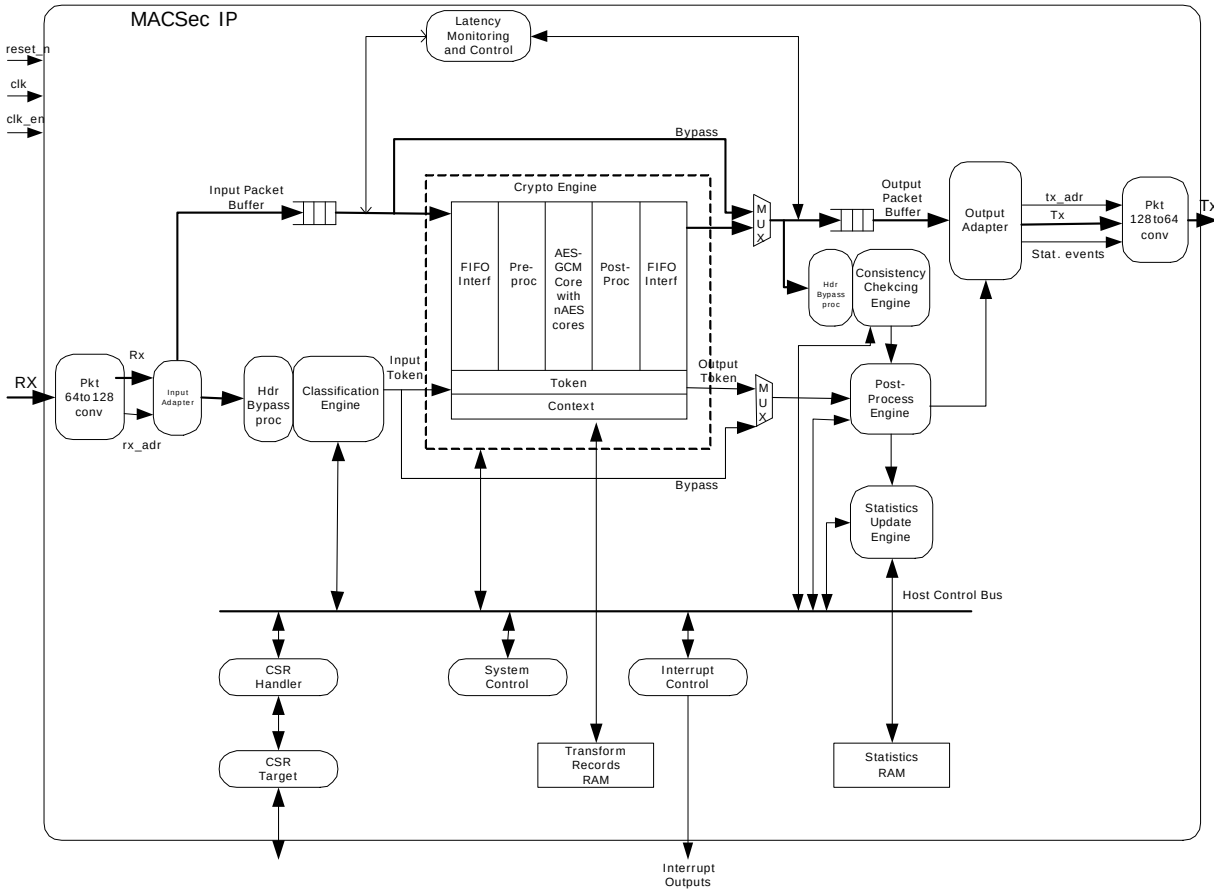
The VSC8564-11 device includes a high-performance streaming MACsec frame processing engine that provides hardware acceleration for the complete MACsec frame transform along with frame classification and statistics counter updates. The following list includes some of the major features of the MACsec engine.

- Fully IEEE 802.1AE-2006, IEEE 802.1AEbn, and IEEE 802.1AEbw-2013 compliant.
- 16 secure associations (SA) per direction and 16 ingress consistency check rules.
- MACsec cipher suite GCM-AES-128 support.
- MACsec cipher suite GCM-AES-256 support.
- MACsec cipher suite GCM-AES-XPN-128/256 support.
- VLAN and Q-in-Q tag detection.
- MACsec tag detection and sub-classification (Untagged, Tagged, BadTag, KaY).
- Programmable “control” packet classification.
- 8-entry programmable non-match flow operation selection (drop, bypass), depending on MACsec tag sub-classification and control packet classification.
- Programmable confidentiality offset (0 B – 127 B).
- SecTAG insertion and removal.
- Integrity Check Value (ICV) checking/removal and calculation/insertion.
- Packet number generation and checking.
- IEEE 802.1AE MACsec statistics counter support.
- Ingress path consistency checking (ICC)–64/16 entry programmable matching table with separate drop/transfer decisions.
- MTU checking and oversize dropping dependent on VLAN User priority for VLAN frames and at global level for non-VLAN frames.
- Advanced MACsec transformations–VLAN tag bypass and EoMPLS header bypass.
- Hardware offload for the nextPN and lowestPN update from the host(KaY).
- Support for AES-ECB, AES-CTR, and AES-GCM/GMAC transformation for FIPS certification of the crypto core.

3.6.1 MACsec Architecture

The MACsec block operates as a frame processing pipeline whose main function is the implementation of the MACsec transform on Ethernet frames. The following illustration shows the MACsec data flow in one direction.

Figure 19 • **MACsec Architecture**



The following sections describe the blocks in the MACsec data flow.

3.6.1.1 PKT64to128 Block

The Packet 64to128 block is the Rx interface of the MACsec IP with the other blocks. It converts the 64-bit packet interface to the 128-bit packet interface with which the MACsec IP works. It also presents the port information associated with the current frame. In the egress configuration, the PKT64to128 block has a FIFO to temporarily handle back-pressure from the MACsec IP due to frame expansion. Based on packet expansion within the MACsec IP, the PKT64to128 block provides flow control feedback to the flow control buffer, which manages all data build up that occurs as a result of MACsec frame expansion.

3.6.1.2 Input Adapter Block

The Input Adapter manages the Input Packet interface to ensure interface protocol compliance.

3.6.1.3 Input Classification Engine Block

The Input Classification engine inspects the received frame data and performs the following functions:

- **Control Frame Classification.** A total of 29 programmable rules to classify the frame as a control frame.
- **VLAN Tag Detection.** Programmable functionality to detect VLAN tags and extract information before further classification.
- **MACsec Tag Detection.** Programmable functionality to detect MACsec tags and check whether they are valid (also detects special KaY packet tags).
- **Default Frame Handling.** Classify packets into eight classes based on the outputs of the control frame classification and MACsec tag detection modules, with control registers to define what to do with a packet (drop or bypass) for each class.

- **Flow Lookup Frame Classification and Frame Handling.** Classify frames based on frame header field contents and outputs of the control frame classification, VLAN tag detection, and MACsec tag detection modules. Flow control registers define what to do with a frame (drop, bypass, or MACsec process) when matching entries. A programmable per-rule priority level resolves any overlap between these rules.
- **Flow Lookup/Default Classification Multiplexer.** Give priority to the decision from the flow lookup frame classification. The default frame handling is used for a frame only if none of the flow lookup entries match.

3.6.1.4 Latency Monitoring and Control

The Latency Monitoring and Control module monitors the latency that the first word of each frame incurs going through the pipeline, and optionally stalls the output side until this latency matches a programmable value. This ensures each frame incurs the same latency through the pipeline, irrespective of any processing time differences.

3.6.1.5 MACsec Crypto Engine

The MACsec Crypto engine performs the standard MACsec encapsulation/decapsulation processing. This engine is able to perform a MACsec transform on a frame using GCM-AES-128 according to the IEEE 802.1AE-2006 MACsec specification and its amendment, IEEE 802.1AEbn-2011, which adds the GCM-AES-256 cipher suite. The crypto engine also transforms a frame using GCM-AES-XPN-128/256 according to IEEE 802.1aebw-2013. This includes modifications to the Ethernet frame header, insertion/removal of the MACsec header (SecTAG), encryption/decryption, authentication, and authentication result insertion/verification. It does not perform MACsec header parsing, but relies on external logic to provide a processing token that tells it how to process the incoming frame.

In addition to the MACsec specifications 0-byte, 30-byte, and 50-byte confidentiality offset, the MACsec crypto engine supports byte-grained confidentiality offsets from 1 to 127 bytes. The MACsec crypto engine supports one or two VLAN tag bypass operation wherein VLAN tags that bypass MACsec processing are fully excluded from the encryption and authentication, such that the receiver side must be able to remove the bypassed VLAN tags without breaking the MACsec packet. It also supports MPLS header bypass wherein the MPLS link header is excluded from encryption and authentication and the client Ethernet frame is subjected to MACsec transformations.

3.6.1.6 Consistency Checking Engine Block

The Consistency Checking engine checks the contents of a frame at the output of the MACsec Crypto engine (after any MACsec decryption) against a set of 16/64 programmable rules (depending on the configuration) for consistency. A programmable per-rule priority level resolves any overlap between these rules. This engine is not present in the egress configuration.

3.6.1.7 Output Post-Processing Engine Block

The Output Post-Processing engine checks the classification and MACsec Crypto engine processing results against a fixed set of MACsec compliance rules, resulting in a drop decision if the rules are violated. Additionally, it performs programmable MTU checking on the MACsec Crypto engine output frame, with individual global and per-VLAN-user-priority MTU settings.

It combines these internal decisions with decisions made by the Classification and Consistency Checking engines into a final pass/drop decision to the output adapter.

Furthermore, based on all the information from the MACsec Crypto engine and the consistency checking engine available to it, the Output Post-Processing engine decides which statistics counters to increment.

3.6.1.8 Statistics Update Engine Block

The Statistics Update engine updates the statistics counter in the statistics RAM, as instructed by the Output Post-process engine. This allows the updating to be scheduled with external statistics access and to occur in parallel with the post-processing of the next frame. This engine also can be configured to skip certain statistics counters.

3.6.1.9 Output Adapter Block

The Output Adapter block manages the output packet interface and ensures interface protocol compliance by isolating the MACsec IP from this interface.

3.6.1.10 PKT128to64 Block

The Packet 128to64 block is the interface of the MACsec IP with the other blocks. It converts the 128-bit packet interface of MACsec IP to the 64-bit packet interface used to communicate with other blocks. It also prepares the security fail debug code to be put into FCS field for packets failing security check.

3.6.2 MACsec Target Applications

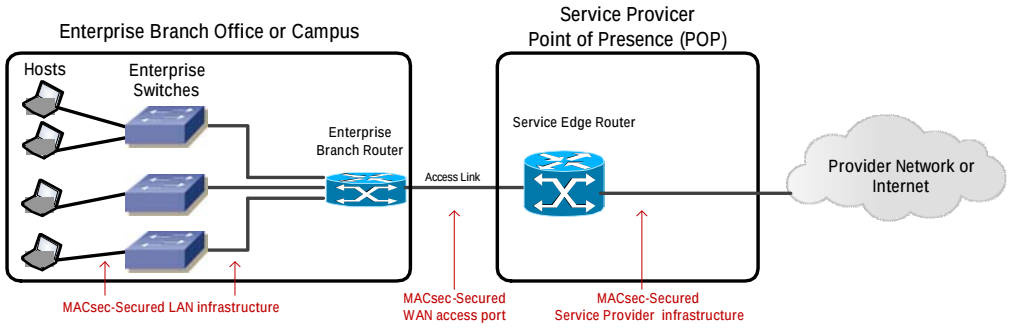
The MACsec engine targets the following applications.

- Secure enterprise infrastructure and WAN ports
- Secure end-to-end Carrier Ethernet connections
- Secure Carrier Ethernet Mobile Backhaul

3.6.2.1 MACsec Secured Enterprise Infrastructure and WAN Port

The following illustration shows an enterprise branch office or campus where a Local Area Network (LAN) connected to a Wide Area Network (WAN) operated by a service provider is protected using MACsec.

Figure 20 • **Secure Enterprise Infrastructure and WAN**



Each host has a dedicated physical link to an Enterprise Ethernet switch, and the switches are connected to an enterprise branch router that also provides WAN access. In smaller configurations, hosts can also connect directly to the branch router. All internal branch office Ethernet ports are secured using MACsec.

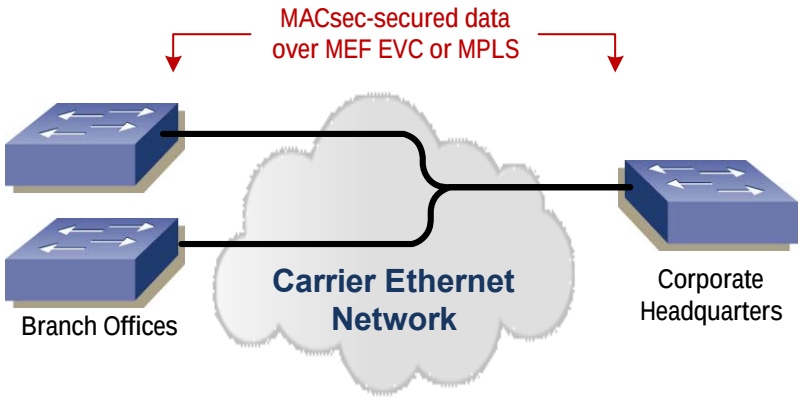
The branch router connects across an access link to a service provider's service edge router, and this access link is secured using MACsec. MACsec may also be used to secure the service provider's network.

The 802.1X security protocols can be used for authentication and to automate the distribution and management of MACsec encryption keys. The VSC8564-11 device supports 128-bit and 256-bit encryption.

3.6.2.2 MACsec Secured Carrier Ethernet Connection

The following illustration shows a Carrier Ethernet network providing end-to-end MACsec secured WAN connectivity for an enterprise.

Figure 21 • **Secure Carrier Ethernet Connection**



With traditional MACsec, VLAN tags or MPLS labels are fully encrypted and hidden from the Carrier Ethernet network thereby limiting the enterprise to only the simplest point-to-point private line connectivity services.

The VSC8564-11 device supports leaving the VLAN tags or MPLS labels unencrypted for use by the Carrier Ethernet network while fully securing the enterprise's Ethernet data inside these encapsulations. This approach uses standard, non-proprietary encapsulation formats with 128-bit and 256-bit encryption.

By enabling these features, the enterprise is able to take advantage of the latest Layer-2 (L2) VPN services available from a Carrier Ethernet network. These L2 VPN services can be point-to-point or multipoint, and can use standardized Metro Ethernet Forum (MEF) Carrier Ethernet and Internet Engineering Task Force (IETF) MPLS service offerings including multiple Virtual Private Lines per WAN port.

3.6.3 Formats, Transforms, and Classification

This section shows the frame formats before and after MACsec transformation with an overview of the classifiable fields that can be used for SA classification for different MACsec applications. Classification fields are selectable per SA. In depicting which fields may be used for pre-decrypt classification, it is assumed that the confidentiality offset field is not used (all fields after SecTAG are encrypted).

3.6.3.1 Standard MACsec Formats

The following table summarizes the MACsec frame combinations in the standard MACsec mode.

Table 4 • **Standard MACsec Frame Combinations**

Unencrypted Format	Pre-Encryption (Tx) Classification Fields	Pre-Decryption (Rx) Classification Fields
Untagged Ethernet	DA, SA, Etype	DA, SA, SecTAG
Single-tagged Ethernet	DA, SA, TPID, VID, Etype	DA, SA, SecTAG
Dual-tagged Ethernet	DA, SA, TPID1, VID1, TPID2, VID2, Etype	DA, SA, SecTAG

The following illustrations show each frame format before and after standard MACsec transformation.

Figure 22 • **Untagged Ethernet**

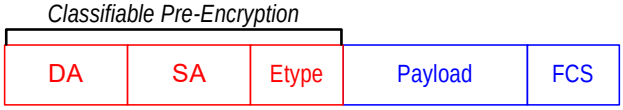


Figure 23 • **Standard MACsec Transform of Untagged Ethernet**

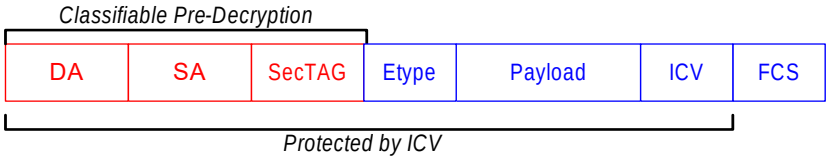


Figure 24 • **Single-Tagged Ethernet**

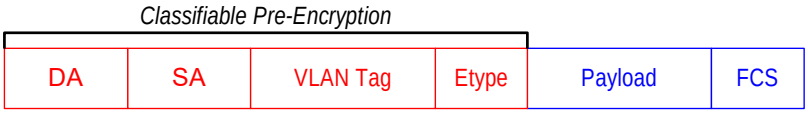


Figure 25 • **Standard MACsec Transform of Single-Tagged Ethernet**

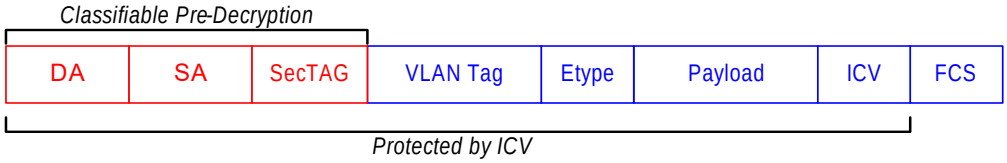


Figure 26 • **Dual-Tagged Ethernet**

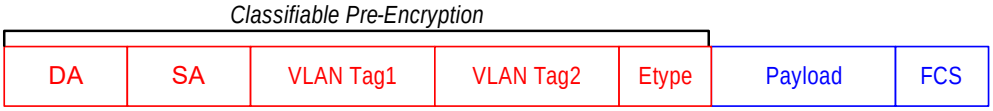
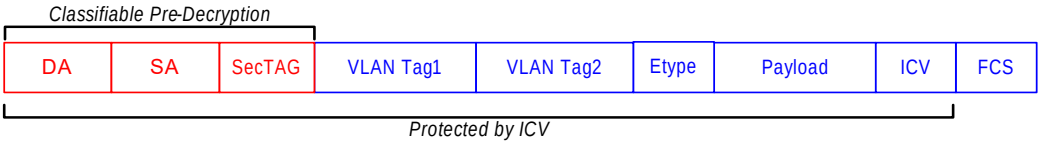


Figure 27 • **Standard MACsec Transform of Dual-Tagged Ethernet**



3.6.3.2 Advanced MACsec Formats

The following table summarizes the MACsec frame combinations in the advanced MACsec mode.

Table 5 • **Advanced MACsec Frame Combinations**

Unencrypted Format	Encrypted Format	Pre-Encryption (Tx) Classification Fields	Pre-Decryption (Rx) Classification Fields
Single-tagged Ethernet	MACsec plus single tag bypass	DA, SA, TPID, VID, Etype	DA, SA, TPID, VID, SecTAG
Dual-tagged Ethernet	MACsec plus single tag bypass	DA, SA, TPID1, VID1, TPID2, VID2, Etype	DA, SA, TPID1, VID1, SecTAG
Dual-tagged Ethernet	MACsec plus dual tag bypass	DA, SA, TPID1, VID1, TPID2, VID2, Etype	DA, SA, TPID1, VID1, TPID2, VID2, SecTAG
EoMPLS with one Label	MACsec plus EoMPLS header bypass	C-DA, C-SA, MPLS Etype, 32-bit Label	C-DA, C-SA, MPLS Etype, 32-bit label, SecTAG
EoMPLS with two Labels	MACsec plus EoMPLS header bypass	C-DA, C-SA, MPLS Etype, 32-bit Label1, 32-bit Label2	C-DA, C-SA, MPLS Etype, 32-bit label1, 32-bit label2, SecTAG

The following illustrations show each frame format before and after advanced MACsec transformation.

Figure 28 • **Single-Tagged Ethernet**

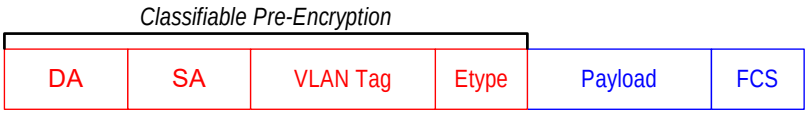


Figure 29 • **MACsec Transform to Single Tag Bypass**

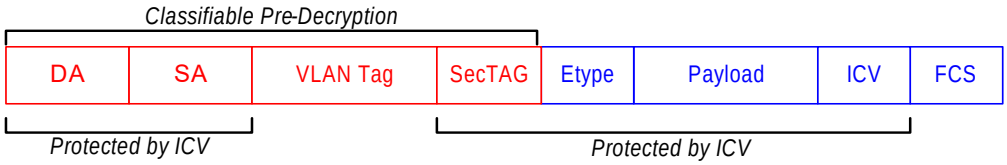


Figure 30 • **Dual-Tagged Ethernet**

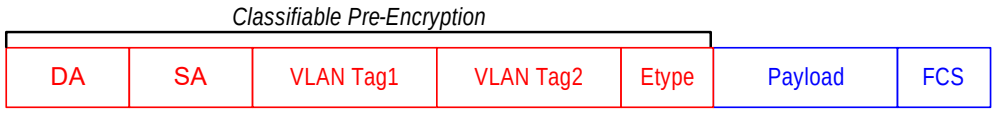


Figure 31 • **MACsec Transform to Single and Dual Tag Bypass**

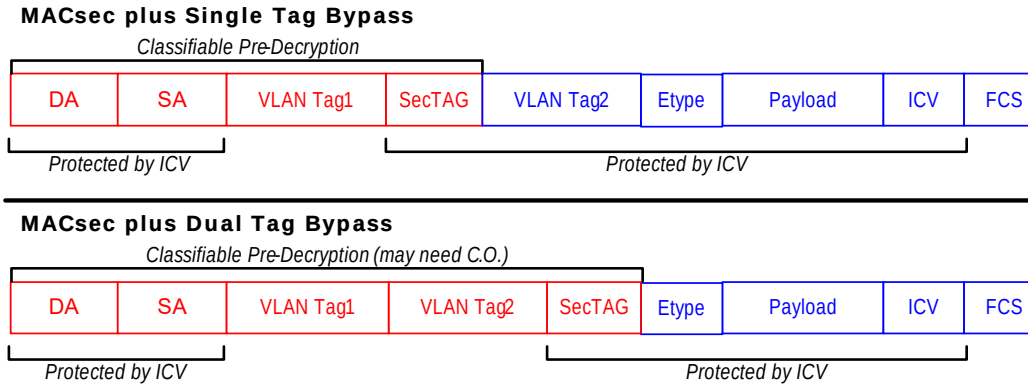


Figure 32 • **EoMPLS with One Label**

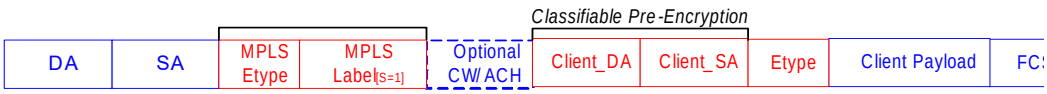


Figure 33 • **Standard and Advanced MACsec Transform**

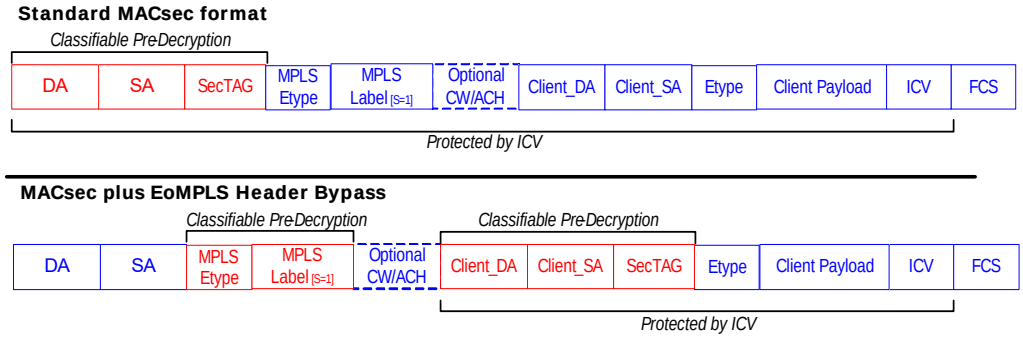


Figure 34 • **EoMPLS with Two Labels**

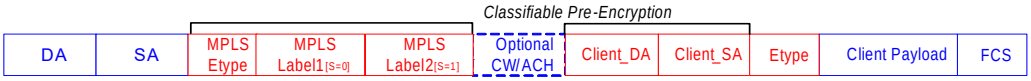
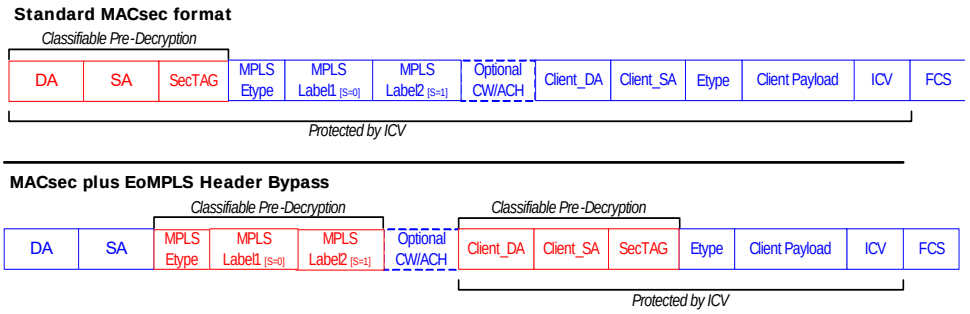


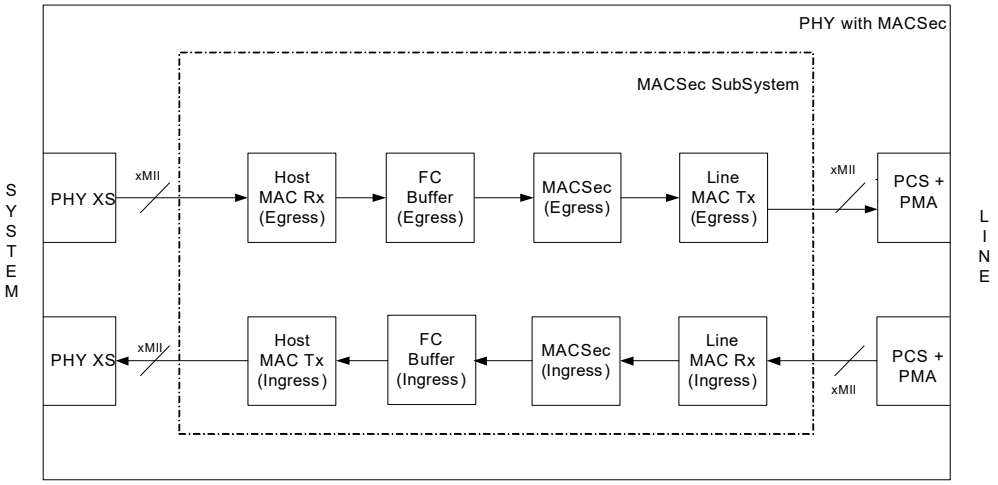
Figure 35 • **Standard and Advanced MACsec Transform**



3.6.4 MACsec Integration in PHY

The MACsec block is designed to be integrated with a host MAC and a line MAC to form a plug-in MACsec solution between an existing Ethernet MAC (system-side) and an existing Ethernet PHY (line-side). MACsec adds bandwidth in egress. This increase in bandwidth is handled adding IEEE 802.3 pause flow control toward the system. The FC buffer block provides packet buffering and controls the IEEE 802.3 pause flow control generation to handle MACsec frame expansion. The following illustration shows the integration of MACsec in the PHY.

Figure 36 • **MACsec in PHY**



3.6.5 MACsec Pipeline Operation

MACsec ingress and egress pipeline operations are identical except for a few situations mentioned in the following sections. The MACsec block always operates in cut-through mode. The length of the frame is calculated on the fly and does not need to be known before the start of processing. This means that MACsec egress processing encrypts (protects) all bytes of the frame fed into the MACsec core. If the frame contains Ethernet padding, this padding is encrypted/protected by MACsec and the ICV is appended after it. For ingress processing, the MACsec block accepts frames with Ethernet padding and it strips Ethernet padding from short MACsec frames.

Ethernet frames are submitted to the MACsec egress/ingress block with their Ethernet header (destination address, source address, Ethertype) but without the leading preamble and start-of-frame bytes and trailing 4-byte CRC (FCS). It is the responsibility of the host/line MAC to strip and check the CRC of each incoming frame.

In the case of large frames, the first output data word of a frame may leave the MACsec pipeline before the last input data word of a frame enters, and errors such as ICV check verification or MTU checking may only be detected after the last byte of frame data has been processed. As a consequence, dropping a frame is accomplished by setting the frame abort signal and not by preventing the frame from appearing on the output. In other words, the system/line MAC transmits a frame with bad CRC. The engine can be programmed to drop frames completely (internal drop), but only if the decision to drop has been made by the flow lookup stage. The pipeline outputs the (processed) frames in the same order they are input, unless the frame is dropped internally. The MACsec block can also be bypassed completely to improve latency.

The SL field in MACsec indicates the end of the MACsec frame, which is needed to locate the ICV in case Ethernet padding follows the ICV. For such frames, the MACsec block uses the information from the SecTAG of the frame to calculate the actual MACsec frame length and uses this length during ingress processing. All data that follows the ICV is removed from the data stream by the MACsec block. This action is the de-padding action, using the MACsec protocol header. The ICV is assumed to be at the location as indicated by the SecTAG, otherwise the frame does not pass the MACsec integrity check.

If the SL field in the MACsec frame indicates a longer frame than the packet actually received by the MACsec block (if the frame does not pass MACsec PDU check), the MACsec block flags this situation as an integrity check failure or packet length error, depending on the difference in length.

Note: The de-padding action is applicable only for MACsec frames that are going to be decrypted/validated by the MACsec flow and will not change the regular MACsec processing latency. No de-padding action is performed on bypass/drop frames.

After ingress MACsec processing, it is possible for the frame to become smaller than 64 bytes. Such frames are then padded by the host MAC (if enabled) and the packet processing switch/system receives 64 byte frames after Ethernet padding.

In the egress direction the MACsec core calculates and updates the SL field in the MACsec header, and authenticates and encrypts (optionally) the frame if a frame's size (including the MACsec header and ICV) is less than 64-bytes.

Note: This short length field indicates frame data from after the first byte of the MACsec header to byte immediately before ICV.

For this feature to work, host MAC receiver should be configured to allow undersized frames and line MAC transmitter should be configured to pad frames.

Host and line MACs do not accept less than 64 byte frames (without Ethernet padding) from system/line interfaces. Also they do not remove the Ethernet padding from the frames.

Each frame at input is accompanied by the following signals:

- **Port Number.** Two-bit signal that indicates the source port (common, reserved, controlled, or uncontrolled) of the packet as defined in the IEEE 802.1AE standard.
- **Bad CRC/Packet Error.** Bits that indicate that the packet has a bad CRC/packet error.

Frames with a bad CRC or other packet errors are forwarded to the output with the same errors, unless their classification leads to a decision to drop them. Because error signals appear at the end of a frame and processing must start before the end of a frame is received, classification and processing is performed, but statistics are not updated.

The source port for MAC data/control frames is configurable. Typically, egress MAC data frames are put on the controlled port and MAC control frames are put on the uncontrolled port. All ingress frames are put on the common port. This configuration is controlled using MAC_DATA_FRAMES_SRC_PORT and MAC_CTRL_FRAMES_SRC_PORT in the MACSEC_CTL_CFG register. Control packet classification determines the frames that are assumed to have come from controlled/uncontrolled ports in egress and the frames that should go to controlled/uncontrolled ports in ingress.

LPI and fault signals that appear on the Ethernet interface can be detected by the MAC and converted into internal status frames (single-byte frames containing the state of the signals). The MACsec block can recognize these status frames on the input and propagate them to its output.

Status frames travel through the pipeline along with normal Ethernet frames, so they appear at the output after the preceding Ethernet frame and before any frames that appear after the status change. However, status frames do not take part in any operations of the pipeline. They are invisible to static classification, flow lookup, MACsec processing, and consistency checking.

The following illustrations show the egress and ingress MACsec data flows.

Figure 37 • **MACsec Egress Data Flow**

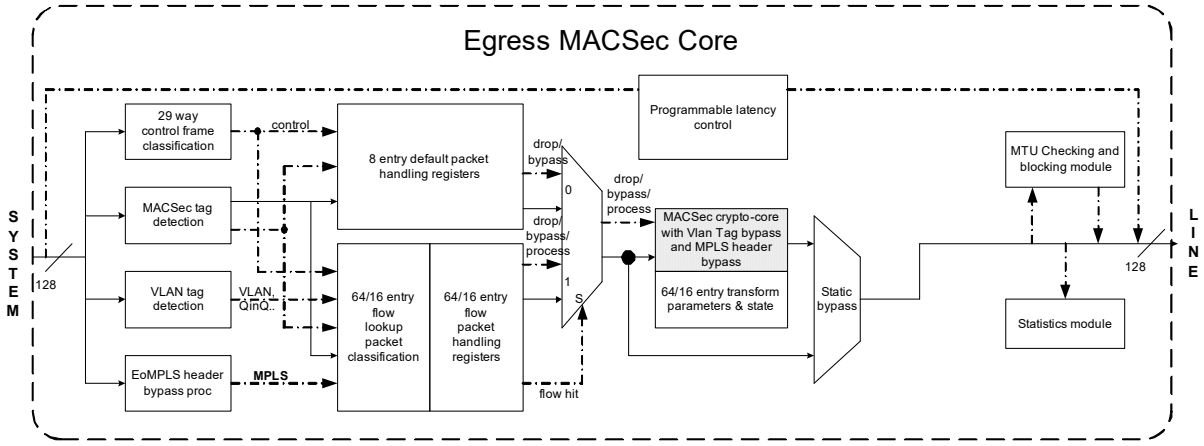
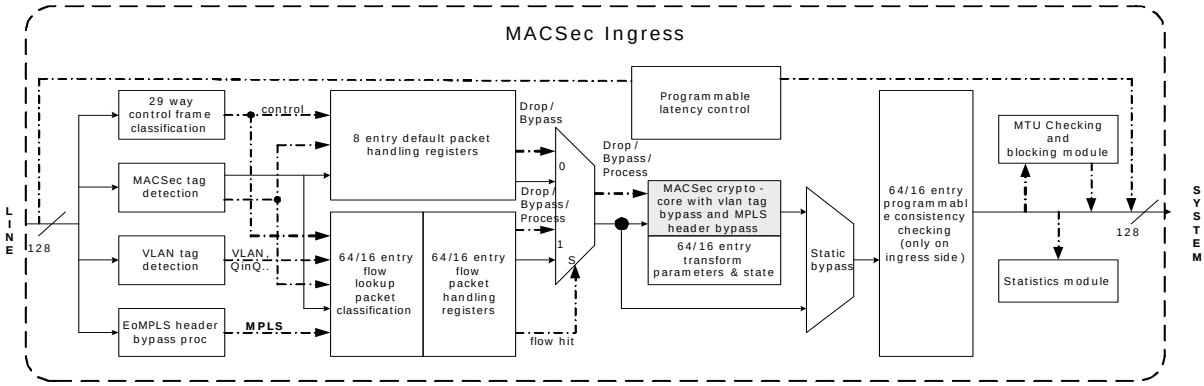


Figure 38 • **MACsec Ingress Data Flow**



The following sections describe the pipeline stages. Of these pipeline stages, the MACsec transform stage is the only one that can modify the frame data or drop a frame completely (no frame will appear at the output of the pipeline in that case). Other stages can only perform the following actions for frame data:

- Inspect the frame data, such as performing a classification based on fields in a header.
- Drop the frame (which is already streaming out) by setting the frame abort signal along with the last word of data.

Static Classification

This is the first stage of packet classification. Control packet classification, MACsec tag parsing, and VLAN tag parsing are carried out in parallel.

Flow Lookup

Each table of 16 SA flows can match on a number of criteria. An action and a MACsec context is associated with each flow. If the packet does not match any of these 16 flows, one of eight default actions is selected, depending on the results of MACsec tag parsing and control packet classification.

MACsec Transform

This stage carries out the actual MACsec encryption and authentication. It uses the MACsec context associated with the flow that was matched in the previous stage. A MACsec context is a data structure

containing all information (such as key and sequence numbers) needed to carry out a MACsec transform. This stage can also bypass or drop certain packets.

The MACsec transform stage can be bypassed by setting MACSEC_BYPASS_ENA = 1 in the MACSEC_ENA_CFG register. Setting the MACSEC_BYPASS_ENA = 0 and MACSEC_ENA = 1 results in traffic passing through the MACsec transform block. Setting the MACSEC_BYPASS_ENA and MACSEC_ENA bits to 0 results in all traffic being dropped at the input interface of MACsec.

Ingress Consistency Checking

This stage is not present in the egress-only version of the MACsec block. It extracts information from the decrypted packet and checks it against a table of 64/16 rules. Rules can either reject or pass certain packets. Separate default actions can be configured for control and non-control packets (in case no match is found in the table).

Output Postprocessor

This stage checks the results of the MACsec transform operation. It also checks that the length of a packet does not exceed the MTU (incrementing a counter if the MTU is exceeded, and optionally tagging the packet for deletion). Each of the eight VLAN user priorities and non-VLAN packets can have a different MTU. This stage implements the MACsec-compliant post-processing decision tree and updates all MACsec statistics.

3.6.5.1 Static Classification

Control packet classification, MACsec header parsing, and VLAN tag parsing are the three static classification operations performed in parallel to produce the following results:

- **Control.** Single bit that is set if the packet is classified as a control packet.
- **MACsec Tag Status.** One of four values: untagged, tagged, bad tag and KaY, where tagged means the packet has a valid non-KaY MACsec SecTAG.
- **VLAN Related Status Signals.** VLAN valid, VLAN ID, Inner VLAN ID, VLAN User Priority, Inner VLAN User Priority, QTAG valid, STAG valid, and Q-in-Q valid.
- **Parsed Ethertype.** First non-VLAN Ethertype found in the frame.

The following sections describe the static classification operations.

3.6.5.1.1 Control Packet Classification

Control packet classification is used to identify frames from uncontrolled ports and exclude them from MACsec processing. Frames such as the MAC control frames and MKA/EAPOL frames are forwarded without MACsec processing because they use uncontrolled ports for transmission. MKA/EAPOL frames are used for Key exchange and have Ethertype 0x888E.

The control packet classification logic classifies a packet as a control packet based on its destination address and/or its Ethertype. It yields a single-bit output (control) classifying the packet either as a control packet or not.

The control packet classification logic can match a packet based on 29 individually enabled criterion. If the packet matches one or more of the enabled criterion, the packet is classified as a control packet and the control output is set to 1. If no enabled criterion is matched, the packet is not classified as a control packet. The CTL_PACKET_CLASS_PARAMS and CTL_PACKET_CLASS_PARAMS2 registers configure control packet classification. The match criterion are as follows:

- The fixed Ethernet destination address 01_00_0C_CC_CC_CC. The corresponding register CP_MAC_DA_48* has this address as a reset value, but this value can be changed if needed.
- The fixed Ethernet destination address range 01_80_C2_00_00_0? (the first 44 bits must match; the trailing 4 bits are don't care). The corresponding register CP_MAC_DA_44* has this address range as a reset value, but this value can be changed if needed. It is always a range with 44 matching bits and 4 don't care bits.
- One free to program Ethernet destination address range specified by the CP_MAC_DA_START and CP_MAC_DA_END registers. Ethernet addresses are treated as unsigned 48-bit integers, as shown in the following examples.

```
If CP_MAC_DA_START = 00_80_C2_00_00_00 and CP_MAC_DA_END = 00_80_C2_00_00_0F,
the matched range is identical to the range normally matched by MAC_DA_44.
```

If CP_MAC_DA_START = 00_00_00_00_00_00 and CP_MAC_DA_END = FF_FF_FF_FF_FF_FF, all destination addresses are matched (every packet is classified as a control packet).
If CP_MAC_DA_START = CP_MAC_DA_END,
then only a single address will be matched.

- Eight individual Ethernet destination addresses: CP_MAC_DA_MATCH_0 through CP_MAC_DA_MATCH_7.
- Sixteen individual Ethertypes: CP_MAC_ET_MATCH_0 through CP_MAC_ET_MATCH_7 where each Ethertype compare value field shares a register with two destination address compare value bytes and CP_MAC_ET_MATCH_10 through MAC_ET_MATCH_17 registers.
- Two combinations of destination address and Ethertype: CP_MAC_DA_ET_MATCH_8 and CP_MAC_DA_ET_MATCH_9. A packet matches only if both the destination address and the Ethertype match.
- Even though the registers for destination addresses and Ethertypes 8 and 9 have the same format as those for destination addresses and Ethertypes 0 to 7 and 10 to 17, they have different semantics. Destination address 8 can only be enabled in combination with Ethertype 8, and only packets with both a matching destination address and a matching Ethertype will match this criterion. The same applies to destination address and Ethertype 9. On the other hand, destination addresses 0 to 7 can be enabled independent of Ethertypes 0 to 7. When both destination address 0 and Ethertype 0 are enabled, packets that have either a matching destination address or a matching Ethertype (or both) will be classified as control packets.
- After reset, control packet matching criteria are disabled. The registers for a matching criterion must be programmed to enable it.
- Either the first Ethertype after the DA/SA fields or the parsed Ethertype, determined by the VLAN parsing algorithm, is the Ethertype value (number 0 to 17, including the combined numbers 8, 9) from the packet that can be used to compare. This selection is done using the CP_MATCH_MODE register.
- Rules are enabled using the CP_MATCH_ENABLE register.

3.6.5.1.2 MACsec Tag Parsing

The MACsec tag parsing logic inspects MACsec tags. MACsec tags must follow the source address, without any intervening VLAN tags. (They may follow VLAN tags only in VLAN tag bypass mode.) MACsec tag parsing classifies each packet into one of four categories:

- **Untagged.** No MACsec tag (Ethertype differs from 0x88E5).
- **Bad Tag.** Invalid MACsec tag, as determined by the tag detection logic.
- **KaY Tag.** These packets are generated and/or handled by software and no MACsec processing is performed on them by the hardware except for straight bypass.
- **Tagged.** Valid MACsec tag that is not KaY.

The following table shows the IEEE 802.1AE checks that determine the status of the MACsec tag parsing.

Table 6 • **MACsec Tag Parsing Checks**

MACsec Tag (SecTAG) Check	Result
Ethertype is not MACsec type	Untagged
V bit = 1	Bad tag
C bit = 0 and E bit = 1	KaY
C bit =1 and E bit = 0	Bad tag
SC bit = 1 and ES bit = 1	Bad tag
SC bit = 1 and SCB bit = 1	Bad tag
SL ? 48	Bad tag
PN = 0	Bad tag
All other	Tagged

MACsec tag parsing checks are controlled by configuring the SAM_NM_PARSING register.

3.6.5.1.3 VLAN Tag Parsing

The VLAN tag parsing logic recognizes VLAN tags that immediately follow the source address. Both 802.1Q and 802.1s tags can be recognized. Packets with two VLAN tags can also be recognized.

The VLAN tag parsing logic generates the following signals that can be used by flow lookup and other processing stages.

- **VLAN Valid.** Single bit that is set when a VLAN tag (of any type) is successfully parsed.
- **Stag Valid.** Single bit that is set if the first valid VLAN tag is an 802.1S tag.
- **Qtag Valid.** Single bit that is set if the first valid VLAN tag is an 802.1Q tag.
- **Q-in-Q Found.** Single bit that is set if two valid VLAN tags were found.
- **VLAN User Priority.** Three-bit field derived from the first VLAN tag. For non-VLAN tag packets the default user priority is returned. User priority processing can be disabled to also return the default user priority.
- **VLAN ID.** Twelve-bit field taken from the first VLAN tag. Undefined for non- VLAN packets.
- **Inner VLAN User Priority.** Three-bit field derived from the second (inner) VLAN tag. This value is always passed through the re-mapping table (the SAM_CP_TAG2 register) and the result value is used in classification. Undefined for non-VLAN packets or VLAN packets without a second VLAN tag.
- **Inner VLAN ID.** Twelve-bit field that is taken from the second (inner) VLAN tag. Undefined for non-VLAN packets or VLAN packets without a second VLAN tag.
- **Ethertype.** Ethertype extracted from the packet after zero, one, or two VLAN tags.

VLAN parsing is controlled by configuring the SAM_CP_TAG, SAM_PP_TAGS, SAM_PP_TAGS2, and SAM_CP_TAG2 registers.

The parsed VLAN fields (including UP) are used in SA flow classification lookup. The MACsec block also maintains VLAN statistics on a per user priority basis. This includes dropped and oversize packets on a user priority basis.

3.6.5.2 Flow Lookup/SA Flow Classification

The flow lookup logic associates each packet with one of the two following flows:

- A table of SA matching flows, each of which can match a packet based on a set of match criterion. If a packet matches multiple (enabled) SA flows, the SA flow with the highest user-defined priority value is selected. The flow specifies which action must be performed (drop the packet, pass it unchanged, or perform a MACsec transform). Each SA flow for which a MACsec operation is specified corresponds to exactly one MACsec context (and hence to a single MACsec SA, either ingress or egress). In other words, all packets that are to be processed using a single MACsec SA have to be matched by a single SA flow.
- A table of eight non-matching flows. If no enabled SA flow matches a packet, a non-matching flow is selected based on the MACsec tag parsing result and the control bit (from the control packet classification). For these non-matching flows the only possible actions are bypass and drop (MACsec operations cannot be selected here).

The output of the flow lookup is as follows:

- **SA Hit.** Single bit signal that is set if the packet matched an enabled SA flow.
- **SA Index.** Index of the SA flow being matched. If no SA flow was matched, this field is composed from the control packet classification and MACsec tag parsing results, which identifies the non-matching flow used.

3.6.5.2.1 SA Match Criteria

Each SA flow has a set of registers that specify the match criteria using one of two following categories:

- The four MACsec tag match bits (untagged, tagged, bad_tag, and kay_tag in the SAM_MISC_MATCH registers). If the corresponding bit is set in the SAM_MISC_MATCH register, packets from that category (as classified by the MACsec classification logic) can be matched if the other criteria are also satisfied. If the corresponding bit is clear, packets from that category can not be matched.

- The mask-able match criteria. Each of these criteria can be masked by a mask bit in the SAM_MASK registers. If the corresponding mask bit is clear, the matching criterion is not tested and packets may be matched regardless of actual value in the packet. If the corresponding mask bit is set, the matching criterion is tested; if the packet has a different value from that specified in the flow, the packet will not be matched.

The following table shows the match criteria and maskable bits.

Table 7 • **Match Criteria and Maskable Bits**

Egress/Ingress SA Match Classifiers	Data Bits	Mask Bits
MAC SA and MAC DA (mask bit per byte)	96	12
MAC Ethertype (parsed Ethertype)	16	1
VLAN class / parsing result (vlan_valid, qtag_valid, stag_valid, qinq_found)	4	4
VLAN UP (parsed User Priority)	3	1
VLAN ID	12	1
Inner VLAN UP (inner User Priority when Q-in-Q is detected)	3	1
Inner VLAN ID (inner VLAN ID when Q-in-Q is detected)	12	1
Source port (controlled/uncontrolled/common/reserved)	2	1
Control packet	1	1
MACsec tag classifier output (untagged/tagged/bad tag/KaY)	0	4
MACsec SCI (compared only for MACsec tagged frames, available only in ingress)	64	1
MACsec TCI.AN (compared only for MACsec tagged frames, available only in ingress, individually masked)	8	8
Field_2B_16B (used in MPLS header bypass mode)	64	64
SA match priority	4	0
Entry enable	1	0

If all four MACsec tag match bits are set and none of the mask bits are set, the flow matches all possible packets. If none of the MACsec tag match bits are set, the flow does not match any packets.

If an exact match of the MAC source address is desired, all six mac_sa_mask bits must be set. If an exact match of the MAC destination address is desired, all six ma_da_mask bits must be set.

The SCI and TCI.AN fields are used in only in the ingress SA flow classification. The TCI.AN field match can be masked per bit. If an exact match of the TCI.AN field is desired, all eight tci_an_mask bits must be set. If a match on the SCI field is desired, make sure that the SCI field is expected in the packet and match on the SC bit in the TCI field (SC bit must be set). For packets without an SCI field, the TCI field in combination with the MAC source address determines the match criterion (as defined in the 802.1AE standard).

The VLAN ID output can be undefined for non-VLAN packets. When matching packets on VLAN ID, also match on vlan_valid = 1.

A packet is matched on the parsed Ethertype from the VLAN classification logic. This differs from the Ethertype used by the control packet classification logic.

Each flow can be enabled or disabled individually. Only enabled flows are selected when they match a frame. When multiple enabled flows match a frame, the one with the highest match_priority field (a number from 0 to 15) will be selected; among equal priority flows the one with the lowest index will be selected.

The match_priority field is always 4-bit wide (16 priority levels) regardless of the number of SAs supported in the given configuration. The SA_MATCH_PARAMS registers control the SA match criteria.

3.6.5.2.2 Enabling and Disabling Flows

SA_MATCH_CTL_PARAMS registers control the enabling and disabling of matching table entries in the main SA matching module. It is also possible to set, clear, and toggle enable bits with a single write action.

Note: To write the match registers of an SA flow or the MACsec context, the flow must be disabled first to ensure that all flow parameters are loaded into the engine when the flow is enabled again.

If the block supports more than 32 SAs, setting, clearing and toggling of enable bits for SA entries beyond 32 requires two write operations. The upper flags are stored with the first write operation to SAM_TOGGLE2, SAM_SET2, or SAM_CLEAR2 respectively. The action for all SA entries is applied and the upper flags are cleared to zero with the second write operation to SAM_TOGGLE1, SAM_SET1, or SAM_CLEAR1 respectively.

Each SA flow can be enabled or disabled individually. If an SA flow is disabled, it will not match any packets.

When a previously enabled SA flow is disabled (by writing to the SAM_ENTRY_CLEAR1/2 or SAM_ENTRY_TOGGLE1/2 registers), the hardware loads the unsafe field in SAM_IN_FLIGHT register with the number of packets currently processed in the pipeline and the software must wait for the unsafe field to reach zero before it writes to the MACsec context or any of the registers belonging to that SA flow. This is necessary to make sure that all packets that might make use of the disabled flow or the associated MACsec context have left the engine.

3.6.5.2.3 Flow Actions

Each SA flow has a SAM_FLOW_CTRL_IGR/EGR register that specifies the action that must be taken when a frame is matched by that SA flow. The action is determined by one of the following four flow types.

- **Bypass** The frame is passed unchanged.
- **Drop.** The frame is dropped. The drop_action field specifies the action.
  - The packet can be forwarded with a corrupt CRC indication.
  - The packet can be forwarded with a bad packet (packet error) indication.

Note: In both cases, the frame abort signal is set towards the MAC and the drop behavior is the same.

- The packet can be dropped internally. The dropped packet does not appear on the output of the MACsec because the drop_internal decision is taken before the end of the packet is seen. This operation can drop packets received with CRC and/or packet errors.

3.6.5.2.4 MACsec Ingress and Egress Processing

MACsec ingress and egress processing includes performing the MACsec transform (adding/removing SecTag, encryption/decryption, and generating/verifying ICV), post-processing steps, and updating statistics counters. A properly configured MACsec block implements all per-packet steps of a compliant MACsec implementation.

The flow action also specifies the destination port of the packet (as defined in the 802.1AE standard) in a two-bit field that appears at the output of the data pipeline to PKT128to64 and will be used for statistics.

The following table shows the egress SA flow action related to a matching entry, as defined in the SAM_FLOW_CTRL_EGR register.

Table 8 • **Egress SA Flow Actions**

SA Flow Action	Description	Data Bits
Flow type	Bypass/Drop/Egress process	2

Table 8 • **Egress SA Flow Actions *(continued)***

SA Flow Action	Description	Data Bits
Dest_port	Destination port 00b: Common port 01b: Reserved port 10b: Controlled Port 11b: Uncontrolled port	2
Drop_action	Defines the way drop operation is performed	2
protect_frame	1b: Enable frame protection 0b: Bypass frame through crypto-core	1
sa_in_use	MACsec SA is in use for the looked up SA	1
include_sci	Enables use of implicit/explicit SCI	1
use_es	Enable ES bit	1
use_scb	Enable SCB bit	1
Tag_bypass_size	The number of allowed tags to bypass MACsec (0/1/2)	2
Confidentiality offset	The number of bytes that must be authenticated but not encrypted after SecTAG	7
Confidentiality protect	Enables confidentiality protection	1

The following table shows the ingress SA flow action related to a matching entry, as defined in the SAM_FLOW_CTRL_IGR register.

Table 9 • **Ingress SA Flow Actions**

SA Match Action	Description	Data Bits
Flow Type	Bypass/Drop/Ingress process	2
Dest_port	Destination port 00b: Common port 01b: Reserved port 10b: Controlled Port 11b: Uncontrolled port	2
Drop_action	Defines the way drop operation is performed	2
Drop_non_reserved	Perform drop_action if packet is not from the reserved port	1
Replay_protect	Enable/Disable frame replay protection	1
sa_in_use	MACsec SA is in use for the looked up SA	1
validate_frames	Frame validation level for MACsec ingress processing (disable/check/strict)	2
Confidentiality offset	The number of bytes that must be authenticated but not decrypted after SecTAG	7

MACsec contexts, which store the sequence number, keys, SCI, and other information, are used for further transformation of frames for MACsec egress/ingress flow type processes.

3.6.5.2.5 Non-Matching Flows

The SAM_NM_FLOW_NCP/SAM_NM_FLOW_CP registers define how packets that did not match any of the SA match entries are handled. This is subdivided into eight packet type categories, split by whether or not the packet was classified as a control packet and the output of the MACsec tag classification logic (untagged/tagged/bad tag/KaY).

The actions specified for each flow are a subset of those specified for SA flows (only pass and drop are possible). Each of these flows can specify that a packet must be dropped or bypassed. It also specifies the destination port. The way a packet must be dropped can also be specified.

3.6.5.3 VLAN Tag and EoMPLS Header Bypass Modes

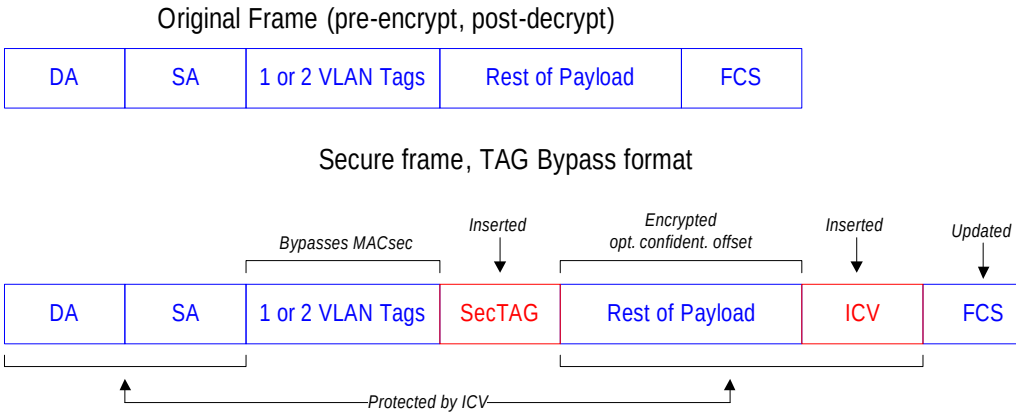
VLAN tag bypass and EoMPLS header bypass are advanced MACsec processing modes with the following classification extensions to the standard configuration.

- Handling of VLAN Tag bypass format (tag bypass).
- Handling of EoMPLS header bypass format (header bypass).
- Processing of packets with SecTAG appearing after one or two VLAN tags, where VLAN tags are not included in the cryptographic operations (Microsemi tag bypass format).
- Processing of packets with SecTAG (and C-SA & C-DA) appearing after an Ethernet Header (SA, DA, ET) with from 2 to 16 bytes of data, where the header and data is not included in the cryptographic operations (Microsemi header bypass format).
- Control packet detection for packets in these proprietary formats.
- Programmable match fields used in SA lookup for packets in these proprietary formats.

3.6.5.3.1 Tag Bypass Frame Format

Tag bypass is an extension to the standard MACsec frame that allows one or two VLAN tags in front of the SecTAG. These VLAN tags are fully excluded from MACsec protection and bypassed instead. The following illustration shows the format of the frame.

Figure 39 • **VLAN Tag Bypass Format**



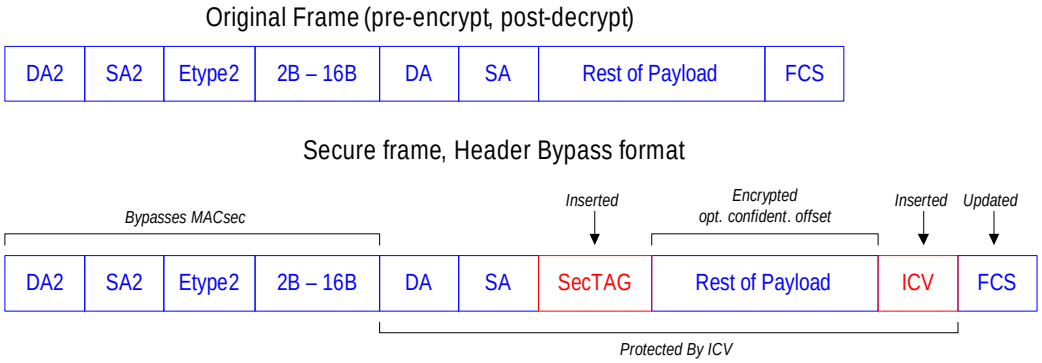
The following logic is used to process the tag bypass format.

- For egress processing, the number of bypassed VLAN tags for encryption is looked-up in the MACsec flow action (SAM_FLOW_CTRL_EGR::TAG_BYPASS_SIZE). If this value is zero, the standard MACsec protection is applied.
- For ingress processing, the number of bypassed VLAN tags is determined by the VLAN parser and position of the SecTAG. The VLAN parser does not look beyond the SecTAG.
- KaY packets (to be bypassed) are detected on both egress and ingress configurations (the VLAN parser defines SecTAG position).
- VLAN tags that bypass MACsec processing are fully excluded from the encryption and authentication, such that the receiver side must be able to remove the bypassed VLAN tags without breaking the MACsec packet.

3.6.5.3.2 EoMPLS Header Bypass Frame Format

EoMPLS Header bypass is an extension to the frame handling of the standard MACsec frame format that allows an additional proprietary header in front of the MAC frame. The following illustration shows the format of the frame.

Figure 40 • **EoMPLS Header Bypass Format**



The following restrictions are applied to the EoMPLS header bypass format.

- The mode is statically controlled by programming the size of the bypassed header. Size of zero indicates absence of the bypassed header.
- No other secure format is possible on the port when header bypass is enabled.
- 2B–16B field is always one size on a port, configurable to be 2, 4, 6...16 Bytes. A static configuration register specifies size of the field. For EoMPLS this is generally configured as multiple of 4B.

The following logic is used to process the EoMPLS header bypass format.

- **Control Packet Detection.** Based on Etype2 matching a configured (static) value.
  - If Etype2 matches, detect and process control packets using MAC_DA, MAC_SA, and parsed Etype (after MAC_SA) to detect EAPOL/MKA transported in MPLS tunnels.
  - Other Etype2 values, detect and process control packets using MAC_DA2, MAC_SA2, and Etype2 to detect any other MAC control frames.
- **SecTAG Position.** Determined by size of 2B–16B field and located right after it.
- **Egress SA Match.** Uses Etype2, up to first 64 bits of the 2B–16B field, MAC_DA, and MAC_SA. The 2B–16B match field in the SA is bit-maskable.
- **Ingress SA Match.** Uses Etype2, up to first 64 bits of the 2B–16B field, MAC_DA, MAC_SA, and SecTAG fields. The 2B–16B match field in the SA is bit-maskable.

3.6.5.4 MACsec Transform

The MACsec transform carries out the actual frame transformation. For egress MACsec operations it inserts the SecTAG, optionally encrypts the payload data, and appends the ICV. For ingress MACsec operations, it removes the SecTAG, optionally decrypts the payload data, and removes and validates the ICV. The MACsec transform stage can detect error conditions (such as sequence number and authentication errors) that cause the frame to be dropped by applying a flow define drop_action.

The MACsec transform does not detect errors in the SecTag that the MACsec classification logic can catch. Only packets that are classified as tagged (valid non-KaY tag) may be submitted to ingress MACsec processing.

The MACsec transform stage uses the MACsec crypto engine for the actual MACsec transform, which operates in the following two major modes.

- In MACsec mode, the crypto engine is active and MACsec transforms can be performed.
- In static bypass mode, the crypto engine is effectively bypassed, which leads to a lower system latency. In this mode, no MACsec transforms are possible. The classification, consistency checking, and MTU check logic are still functional and the MACsec block may still filter (pass or drop) frames.

The MISC_CONTROL register enables static bypass, controls the latency equalization function, allows MACsec-compliant handling of MACsec frames for which no MACsec SA is available, and controls the maximum size of transform record.

If a MACsec SecY receives a MACsec frame on the common port for which it has no SA and the frame payload is unchanged (authenticate-only operation, C = 0, E = 0), it can still forward the frame to the controlled port without checking the authentication simply by stripping the SecTAG and ICV. This will occur if all the following conditions are met.

- The frame is classified as tagged.
- The frame is not matched by any installed MACsec SAs. The frame may either match no SA flow at all or a non-MACsec SA flow.
- The flow type of SAM_NM_FLOW_CP/SAM_NM_FLOW_NCP (whichever is applicable to that packet) for tagged frames is set to bypass.
- The TCI field has C = 0, E = 0.
- The nm_macsec_en bit is set.
- The validate_frames setting is either disabled or check, but not strict.

3.6.5.4.1 MACsec Context and Transform Record

The MACsec block contains an array of MACsec transform records that correspond to the number of supported SAs. Each transform record is 20 × 32-bit words (80 bytes) in size in the ingress direction and 24 × 32-bit words (96 bytes) in size in the egress direction, and corresponds to the SA flow with the same index. The MACsec transform operation is fully specified by a combination of the contents of the SAM_FLOW_CTRL_IGR/EGR register and the contents of the transform record. It corresponds to the operation of a single MACsec SA.

Transform record refers to the data structure as stored in the array. MACsec context refers to the information contained in a transform record. Transform record data are stored in the XFORM_RECORD_REGS registers. The following tables show the format for each transform record.

Table 10 • **Transform Record Format (Non-XPN)**

	128 Bit AES Keys		256 Bit AES key	
128 Bit block	**Egress**	**Ingress**	**Egress**	**Ingress**
0	CTRL Word	CTRL Word	CTRL Word	CTRL Word
	Context ID	Context ID	Context ID	Context ID
	Key0	Key0	Key0	Key0
	Key1	Key1	Key1	Key1
1	Key2	Key2	Key2	Key2
	Key3	Key3	Key3	Key3
	HashKey0	HashKey0	Key4	Key4
	HashKey1	HashKey1	Key5	Key5
2	HashKey2	HashKey2	Key6	Key6
	HashKey3	HashKey3	Key7	Key7
	Seq	Seq	HashKey0	HashKey0
	IV0	Mask1[1]	HashKey1	HashKey1
3	IV1	IV0	HashKey2	HashKey2
	(Zero)	IV1	HashKey3	HashKey3
	(Zero)	(Zero)	Seq	Seq
	(Zero)	(Zero)	IV0	Mask1
4			IV1	IV0
			(Zero)	IV1
			(Zero)	(Zero)
			(Zero)	(Zero)

1. For MACsec, MASK is an unsigned integer controlling a valid range of packet numbers.

Table 11 • **Transform Record Format (XPN)**

	128 Bit AES Keys		256 Bit AES key	
128 Bit block	**Egress**	**Ingress**	**Egress**	**Ingress**
0	CTRL Word	CTRL Word	CTRL Word	CTRL Word
	Context ID	Context ID	Context ID	Context ID
	Key0	Key0	Key0	Key0
	Key1	Key1	Key1	Key1
1	Key2	Key2	Key2	Key2
	Key3	Key3	Key3	Key3
	HashKey0	HashKey0	Key4	Key4
	HashKey1	HashKey1	Key5	Key5
2	HashKey2	HashKey2	Key6	Key6
	HashKey3	HashKey3	Key7	Key7
	Seq Low	Seq Low	HashKey0	HashKey0
	Sec High	Sec High	HashKey1	HashKey1
3	DUMMY	Sec Mask	HashKey2	HashKey2
	IS0 (Salt)	IV0 (Salt)	HashKey3	HashKey3
	IS1 (Salt)	IV1 (Salt)	Seq Low	Seq Low
	IS2 (Salt)	IV2 (Salt)	Sec High	Sec High
4	IV0 (SCI)		DUMMY	Sec Mask
	IV1 (SCI)		IS0 (Salt)	IV0 (Salt)
			IS1 (Salt)	IV1 (Salt)
			IS2 (Salt)	IV2 (Salt)
5			IV0 (SCI)	
			IV1 (SCI)	

All fields of the transform record must be populated by the host software before the corresponding SA flow can be enabled. The ctx_size bit in the CONTEXT_CTRL register controls the size of the context that must be fetched. For bypass and drop flows, the transform record is not used. The hardware only updates the sequence number field; it does not modify the other fields during MACsec egress and ingress processing.

The context control word is the first 32-bit word in each transform record. It specifies the type of operation. Only those settings that are relevant for MACsec operations need to be defined. The following table shows the fields in context control word.

Table 12 • **Context Control Word Fields**

Bits	Name	Description
3:0	ToP	Type of packet 0110b: Egress 1111b: Ingress All other values are invalid
4	Reserved	Write with zero and ignore on read
5	IV0	First word of IV present in context (SCI for MACsec) Must be set to 1b

Table 12 • **Context Control Word Fields *(continued)***

Bits	Name	Description
6	IV1	Second word of IV present in context (SCI for MACsec) Must be set to 1b
7	IV2	Third word of IV present in context (use sequence number instead) Must be set to 0b
12:8	Reserved	Write with zero and ignore on read
13	Updated Seq	Update sequence number Must be set to 1b for MACsec
14	IV Format	If set, use sequence number as part of IV Must be set to 1b for MACsec
15	Encrypt Auth	If set, encrypt ICV Must be set to 1b for MACsec
16	Key	Load crypto key from context Must be set to 1b for MACsec
19:17	Crypto Algorithm	Algorithm for data encryption 101b: AES CTR 128 111b: AES CTR 256
20	Reserved	Write with zero and ignore on read
22:21	Digest Type	Type of digest key Only single digest key is supported, setting 10b
25:23	Auth Algorithm	Algorithm for authentication Only AES-GHASH is supported, setting 100b
27:26	AN	The two-bit Association Number inserted in the SecTag for egress operations Must be kept 00b for ingress
29:28	Seq type	Type of sequence number: only supported setting is 01b Use 32-bit sequence number, on ingress use the mask as a replay window size
30	Seq mask	Sequence mask is present in context 0b: Egress 1b: Ingress
31	Context ID	Context ID present: must be set to 1b

The following list shows the other fields of the transform record.

- **Context ID.** Unique identifier for each context. It is sufficient to give all transform records a different context ID, possibly by assigning them a number from 0 to maximum index.
- **Key 0 … Key 7.** AES encryption key for the MACsec SA. Each word of the key is a 32-bit integer representing four bytes of the key in little-endian order. The number of words depends on AES key length.
- **H_Key 0, H_Key 1, H_Key 2, and H_Key 3.** 128-bit key for the authentication operation. It is represented in the same byte order as Key 0...Key 7. It is derived from Key 0...Key 7 as follows: H_key = E (Key, 128'h0). This means performing a 128/256 bit AES-ECB block encryption operation with Key 0...Key 7 as the key and a block of 128 zero bits as the plaintext input. The cipher-text result of the AES block encryption is the 128-bit H_Key.
- **Sequence Number.** For egress MACsec this is one less than the sequence number (PN) that is to be inserted into the MACsec frame. For a new SA this must be initialized to 0. After each egress packet, this field is incremented by 1. If it rolls over from 0xFFFFFFFF to 0, a sequence number error occurs and the context is not updated, which means that the same error will occur again for

any subsequent egress packets with that context - the external system will forward these packets to the line with CRC/packet error. For ingress MACsec the sequence number must be initialized to 1.

- **Mask (replay window size).** Window size for ingress sequence number checking. By default it is 0 (strict ordering enforced). It can be set to any integer value up to 2^{32}–1, in which case any nonzero sequence number is accepted.
- **SCI 0 and SCI 1.** SCI that belongs to the specific MACsec SA. An SCI that depends on the source MAC address and the ES and SCB bits is defined, even in modes that do not explicitly transmit or receive the SCI with each packet. This is a 64-bit block, represented by two 32-bit integers in little-endian order. It is the same byte order in which SAM_SCI_MATCH_HI/SAM_SCI_MATCH_LO represent an SCI.

When the sequence number of an egress SA is about to roll over, it must be replaced by a new SA with different keys. It is not allowed to reset the sequence number of an egress SA to a lower value because doing so generally leads to sequence number checking failures at the receiving end of the connection.

For inbound frames, the PN is compared against the sequence number (PN) from the context, resulting in one of the following three cases:

- If the received number is above or equal to the number in the context:

```
{received_PN? next_PN}
```

In this case the context sequence number (PN) is updated (if the update_seq bit is set to 1b). The updated value is the received number plus one.

- If the received number is below the number from the context, but within the replayWindow:

```
{received_PN < next_PN and received_PN ? (next_PN - replayWindow)
```

In this case no context update is required.

- If the received number is below the number from the context, and outside the replayWindow:

```
{received_PN < (next_PN - replayWindow)
```

In this case the sequence number check fails and error bit e10 is set in the result token. No context update is done.

3.6.5.4.2 MACsec Crypto Engine Interrupt Control/Status Register

The INTR_CTRL_STATUS register provides control and status for interrupts within the MACsec crypto engine only. The interrupt output pin controlled here is one of the inputs on the top-level Advanced Interrupt Controller (controlled using the AIC registers).

The following main interrupts are given by the Crypto engine.

- Bit 4 Outbound Sequence Number Threshold

This interrupt is triggered if a sequence number exceeds the programmed sequence number threshold (specified in SEQ_NUM_THRESH) due to an outbound sequence number increment.

- Bit 5 Outbound Sequence Number Roll-over

This interrupt is triggered if a sequence number rolls over (increment from maximum to zero) due to an outbound sequence number increment.

3.6.5.5 Ingress Consistency Checking

Consistency checking is used to verify that MACsec ingress packets satisfy certain properties after decryption. Packets are passed or dropped based on a set of rules. The number of rules is a fixed hardware parameter. As opposed to the static classification and flow lookup stages, consistency checking logic inspects the packet data after the MACsec transform.

Consistency checking logic contains a complete VLAN tag parser performing the same operations as the VLAN tag parser located in the input packet classification logic. The configuration of the parser is controlled by a separate set of registers (IG_CP_TAG, IG_PP_TAGS, IG_PP_TAGS2, and IG_CP_TAG2) similar to the input packet VLAN tag parser. It extracts the payload Ethertype from the second or third Ethertype location in the packet if that packet contains one and two VLAN tags respectively. The VLAN tag parser also extracts (and post-processes) the following fields:

- User Priority field from the first VLAN tag it encounters, to be used by the MTU checking logic and statistics counters update logic.

- VLAN ID and VLAN Up from the second VLAN tag in case of Q-in-Q.

Each consistency check rule can match on a set of mask-able match criteria. If the corresponding mask bit is cleared, the match criterion is not checked and packets can satisfy the rule regardless of the value in the packet. If the corresponding mask bit is set, a packet only satisfies the rule if the value in the packet matches the value in the rule. The following list shows the mask-able match criteria.

- **sai_hit (1b or 0b).** The packet was matched by one of the SA flows during flow lookup.
- **sai_nr (range 0 to SAmax-1).** The packet was matched by the specific SA flow (or is not matched by any SA flow and has a specific combination of control packet and MACsec tag classification). To match packets that were matched by a specific SA flow, also match on sai_hit = 1
- **vlan_valid (1b or 0b).** The packet contains a valid VLAN tag.
- **vlan_id (12 bits value).** The packet has the specified VLAN ID. A match on this criterion is only meaningful if also matched on vlan_valid = 1.
- **vlan_id_inner (12 bits value).** The packet has the specified VLAN ID at second VLAN tag. A match on this criterion is only meaningful if also matched on vlan_valid = 1 and Q-in-Q is detected.
- **vlan_up_inner (3 bits value).** The packet has the specified VLAN Up at second VLAN tag. A match on this criterion is only meaningful if also matched on vlan_valid = 1 and Q-in-Q is detected.
- **etype_valid (1b or 0b).** The Ethertype is greater than cp_etype_max_len.
- **payload_e_type (16 bits value).** The packet has a specific Ethertype if a VLAN packet is detected, this value is the Ethertype following the VLAN tag.
- **ctrl_packet (1b or 0b).** The packet is a control packet.

If all mask bits are cleared, the rule will match every possible packet.

Each of the consistency check rules can be enabled or disabled individually. If a rule is disabled, it will not be selected for match checking. If more than one enabled rule is matched, the one with the highest priority (3 bit number from 0 to 7) is picked. The lowest numbered rule is picked from equal priority rules.

The rule that is eventually selected specifies either a pass or a drop action.

If no rules match, the default action is taken (pass or drop). It is possible to define different default actions for control and non-control packets. After reset, the default action for both of them is drop.

ICC rule configuration is controlled by the IG_CC_PARAMS and IG_CC_PARAMS2 registers.

3.6.5.6 Output Post-Processor

The final stage of the pipeline is the output post-processor. It implements the post-processing decision tree that includes MACsec-compliant post-processing, as well as processing and MTU checking for non-MACsec frames. It can drop the frame due to error conditions detected by the MACsec transform stage (such as sequence number rollover and authentication failure), it checks for the correct combinations of port numbers, it checks the frame length against the MTU, and it updates all statistics counters. For ingress packets, the post-processor uses results of the consistency checking module's VLAN tag detection logic instead of the VLAN parser in front of the MACsec crypto-engine.

The post-process statistics updating is done in accordance with Fig. 10-4 and 10-5 for secure frame generation and secure frame verification management control and frame counters.

3.6.5.6.1 MTU Checking

Registers provide MTU limit values for VLAN tagged frames (per User Priority as provided by the consistency checking module) and one global MTU limit value for non-VLAN frames (detected by the consistency checking module). The limits programmed are also used for statistics counters that rely on an MTU value.

Ingress Frame MTU Checking

- The frame length is the size of the input frame (including header and excluding Ethernet preamble, start-of-frame byte, and CRC).
- The VLAN User Priority is extracted from the VLAN tag as parsed (and post-processed) by the VLAN tag parser implemented in the consistency checking logic.

Egress Frame MTU Checking

- The frame length is the size of the output frame (including header and excluding Ethernet preamble, start-of-frame byte, and CRC).

- The VLAN user priority is the one provided by the VLAN parsing logic in the static classification logic.

MTU checking is configured using the VLAN_MTU_CHECK and NON_VLAN_MTU_CHECK registers.

3.6.5.6.2 Statistics

The following two types of statistics counters are used.

- Per-frame counters are 40 bits wide. They overflow after about 10^{12} frames. A MACsec block processing 10 Gbps traffic can process in the order of 10^{7} frames per second so that the 40-bit counters only saturate after 10^{5} seconds (one day).
- Per-octet counters are 80 bits wide. They overflow after about 10^{24} octets. Even for a system that processes in excess of 10^{9} bytes per second, this means that they will never overflow during the expected lifetime of the system.

The statistics counters can be configured to be auto-cleared on read. Also they can be configured to saturate at maximum value instead of rolling over.

There are three classes of statistics counters, as follows:

- **Global Statistics.** The MACsec block maintains global statistics counters to implement MACsec. Some global statistics are maintained per-SA, so they must be obtained by accumulating (summing) the per-SA statistics of the relevant SAs.
- **Per-SA Statistics.** The MACsec block maintains all per-SA statistics for ingress and egress MACsec operations. Software maintains statistics for all four SAs that might belong to an SC. It keeps the per-SA statistics, even for SAs that it has deleted from the SA flow table. When an SA flow is deleted, its final SA statistics must be collected and added into the per-SA and per-SC statistics.
- **Per-SC Statistics.** The MACsec block does not maintain any per-SC statistics. However, the per-SC statistics are the sum of per-SA statistics of the SAs belonging to that SC. Whenever the software reads per-SA statistics from the hardware, it must not only add them to the per-SA statistics administration, but to the per-SC statistics administration as well.

The following tables show the per SA (per SC), global (SecY), and per user priority egress statistics generated. Eight sets of user priority counters are implemented. If a frame is detected as VLAN it also increments user priority counters in addition to per-SA/global (SecY) counters.

Table 13 • **Egress SA Counters**

Egress SA STAT Counters	Size
sa.OutOctetsEncrypted/sa.OutOctetsProtected	80
sa.OutPktsEncrypted/sa.OutPktsProtected/sa.OutPktsHitDropReserved	40
sa.OutPktsTooLong (MTU check)	40
sa.ifOutBroadcast	40
sa.ifOutMulticast	40
sa.ifOutUnicast	40

Table 14 • **Egress Global Counters**

Egress Global Counters	Size
global.TransformErrorPkts	80
global.OutPktsCtrl	80
global.OutPktsUnknownSA	40
global.OutOverSizePkts (MTU check)	40
global.ifOutBroadcast	40
global.ifOutMulticast	40
global.ifOutUnicast	40

Table 14 • **Egress Global Counters *(continued)***

Egress Global Counters	Size
global.ifOutOctets	40

Table 15 • **Egress Per-User Global Counters**

Egress Global Counters	Size
Vlan.OutOctetsUP	80
Vlan.OutPktsUP	40
Vlan.OutDroppedPktsUP	40
Vlan.OutOverSizePktsUP	40

The following tables show the per SA (per SC), global (SecY), and per user priority ingress statistics generated. Eight sets of user priority counters are implemented. If a frame is detected as VLAN, it also increments user priority counters in addition toper-SA/global (SecY) counters.

Table 16 • **Ingress SA Counters**

Ingress SA STAT Counters	Size
sa.InOctetsDecrypted/sa.InOctetsValidated	80
sa.InPktsUnchecked/sa.InPktsHitDropReserved	40
sa.InPktsDelayed	40
sa.InPktsLate	40
sa.InPktsOk	40
sa.InPktsInvalid	40
sa.InPktsNotValid	40
sa.InPktsAuthFail[1]	40
sa.InPktsNotUsingSA	40
sa.InPktsUnusedSA	40
sa.InPktsSAMiss[1]	40
sa.InPktsUntaggedHit	40
sa.ifInBroadcast	40
sa.ifInMulticast	40
sa.ifInUnicast	40

1. Implemented indirectly. sa.InPktsAuthFail is reported in software by adding sa.InPktsInvalid and sa.InPktsNotValid. sa.InPktsSAMiss is reported in software by adding sa.InPktsNotUsingSA and sa.InPktsUnusedSA.

Table 17 • **Ingress Global Counters**

Ingress Global Counters	Size
global.TransformErrorPkts	80
global.InPktsCtrl	80
global.InPktsNoTag	40
global.InPktsUntagged	40

Table 17 • **Ingress Global Counters *(continued)***

Ingress Global Counters	Size
global.InPktsTagged	40
global.InPktsBadTag	40
global.InPktsUntaggedMiss	40
global.InPktsNoSCI	40
global.InPktsUnknownSCI	40
global.InPktsSCIMiss*	
global.InConsistCheckControlledNotPass	40
global.InConsistCheckUncontrolledNotPass	40
global.InConsistCheckControlledPass	40
global.InConsistCheckUncontrolledPass	40
global.InOverSizePkts	40
global.ifInBroadcast	40
global.ifInMulticast	40
global.ifInUnicast	40
global.ifInOctets	40

Table 18 • **Ingress Per-User Global Counters**

Egress Global Counters	Size
Vlan.OutOctetsUP	80
Vlan.OutPktsUP	40
Vlan.OutDroppedPktsUP	40
Vlan.OutOverSizePktsUP	40

3.6.5.7 Correlation with 802.1AE MACsec Statistics

The following table shows how the MACsec block statistics are derived from the MACsec standard.

Table 19 • **802.1AE Correlation**

MACsec name (802.1AE)	Direction	Type	Microsemi MACsec register
Frame verification statistics (MACsec specification 10.7.9)			
InPktsUntagged	Ingress	Global	global.InPktsUntagged
InPktsNoTag	Ingress	Global	global.InPktsNoTag
InPktsBadTag	Ingress	Global	global.InPktsBadTag
InPktsUnknownSCI	Ingress	Global	global.InPktsUnknownSCI
InPktsNoSCI	Ingress	Global	global.InPktsNoSCI
InPktsOverrun	Ingress	Global	Not implemented, condition does not occur, report as zero.
InPktsUnchecked	Ingress	Per-SC	sa.InPktsUnchecked
InPktsDelayed	Ingress	Per-SC	sa.InPktsDelayed
InPktsLate	Ingress	Per-SC	sa.InPktsLate

Table 19 • **802.1AE Correlation *(continued)***

MACsec name (802.1AE)	Direction	Type	Microsemi MACsec register
InPktsOK	Ingress	Per-SC, per-SA	sa.InPktsOK
InPktsInvalid	Ingress	Per-SC, per-SA	sa.InPktsInvalid
InPktsNotValid	Ingress	Per-SC, per-SA	sa.InPktsNotValid
InPktsNotUsingSA	Ingress	Per-SC, per-SA	sa.InPktsNotUsingSA
InPktsUnusedSA	Ingress	Per-SC, per-SA	sa.InPktsUnusedSA
Frame validation statistics (MACsec specification 10.7.10)			
InOctetsValidated	Ingress	Global	Accumulate over each ingress SA with authentication only: sa.InOctetsDecrypted/Validated
InOctetsDecrypted	Ingress	Global	Accumulate over each ingress SA with encryption: sa.InOctetsDecrypted/Validated
Frame generation statistics (MACsec specification 10.7.18)			
OutPktsUntagged	Egress	Global	global.OutPktsUntagged
OutPktsTooLong	Egress	Global	Accumulate over each egress SA: sa.OutPktsTooLong
OutPktsProtected	Egress	Per-SC, per-SA	sa.OutPktsEcnrypted/Protected if the SA is authenticate only.
OutPktsEncrypted	Egress	Per-SC, per-SA	sa.OutPktsEncrypted/Protected if the SA uses encryption
Frame protection statistics (MACsec spec 10.7.19)			
OutOctetsProtected	Egress	Global	Accumulate over each egress SA with authentication only: sa.OutOctetsEncrypted/Protected
OutOctetsEncrypted	Egress	Global	Accumulate over each egress SA with encryption: sa.OutOctetsEncrypted/Protected

3.6.5.8 Interrupts

The MACsec block can raise five interrupts from ingress and four from the egress block. The available interrupts are as follows:

3.6.5.8.1 MACsec Crypto-Core Interrupt

Indicates several errors detected by the MACsec crypto engine block. The software must read the INTR_CTRL_STATUS register of the MACsec crypto core to see which condition caused the interrupt. The software must then write the same bits to INT_CTRL_STATUS to clear the interrupt condition, as applicable.

- Input error (bit 0) may occur if the MACsec crypto core attempts to process certain malformed short MACsec packets where the packet is shorter than indicated by the SL field.
- Output error and fatal error (bits 1 and 14) indicate a hardware error.
- Processing error (bit 2) may indicate a hardware error, but more likely the flow type in SAM_FLOW_CTRL is inconsistent with the context control word in the transform record (MACsec ingress versus MACsec egress).
- Context error (bit 3) indicates an error in the transform record, probably the context control word, especially the settings for encryption and authentication algorithms.

- Sequence number threshold (bit 4) indicates that an egress flow has exceeded its sequence number threshold. The MACsec SA must be re-keyed to prevent a sequence number rollover. Exceeding the sequence number threshold will not affect packet processing; it is meant to be used as a warning for imminent sequence number rollover.
- Sequence number rollover (bit [5]) indicates that an egress flow has encountered a sequence number rollover. The software must look in the transform record table to see which active egress SA has a sequence number value of 0xFFFFFFFF in case of 32-bit Packet number or 0xFFFFFFFF_FFFFFFFF in case of 64-bit packet number. This egress SA flow must immediately be disabled and it must be re-keyed.

Use the following steps to make effective use of the sequence number threshold interrupt.

1. Set the SEQ_NUM_THRESHOLD register to an appropriate value. A suitable value might be 0xF0000000 for a 32-bit packet number.
2. Make sure the sequence number threshold interrupt is enabled.

Use the following steps if the sequence number threshold interrupt occurs.

1. Temporarily disable the sequence number threshold interrupt, then clear that interrupt bit.
2. Check all transform records of active egress SAs for a sequence number that is either over the threshold or close to it (any egress SA with a sequence number above 0xE0000000).
3. Start a re-keying procedure for all those SAs.
4. After re-keying has been completed (and new SAs are installed on both sides of the connection), re-enable the sequence number threshold interrupt.

3.6.5.8.2 Classification Drop Interrupt

Raised when a packet is dropped by the flow lookup logic where either the SA flow or the non-matching flow specifies a drop action.

3.6.5.8.3 Consistency Check Drop Interrupt (ingress only)

Raised when a packet is dropped by the ingress consistency checking logic.

3.6.5.8.4 Post-Processing Drop Interrupt

Raised when a packet is dropped by the post-processing stage for any other reason than MTU check failure. Ingress packets with an ICV check failure or sequence number check failure raise this interrupt.

3.6.5.8.5 MTU Check Drop Interrupt

Raised when a packet is dropped due to MTU check failure.

Note: Frequent packet dropping may indicate an attack attempt, a configuration error, or a software malfunction.

3.6.5.9 Updating the MACsec SA for Ingress

For synchronization purposes, the MACsec standard requires the lowestPN and the nextPN in an active SA to be updated to a greater value provided by the KaY (unless it is not already reached). This is achieved in the MACsec core by updating the sequence number in an active context to a greater value if the sequence number in the context did not reach this value. The lowest acceptable PN is implicitly updated assuming that the replay window size is not changed. The host must program next_pn_lower (and next_pn_upper for XPN flow) to the desired sequence number, must specify the flow for which the update should occur in next_pn_context_id register and should enable the update in enable_update register. MACsec core will clear this enable_update register once the transform record field is updated. If the sequence number is already equal or above the configured value, then no internal update is performed.

3.6.6 Debug Fault Code in FCS

Incrementing a counter for a packet may be a security failure in some cases. The SA_SECFAIL_MASK/GLOBAL_SECFAIL_MASK register can be used to configure which counter increments are regarded as security fail events. Debug functionality enables packets failing security check to be transmitted with corrupted FCS, which consists of a debug fault code to debug the security failing packet. The FCS of a frame failing security check is corrupted on the output. The corrupted FCS

field contains a fault code for debugging using a frame analyzer. The fault code uses 31 bits, with the last FCS bit reserved to make sure the FCS check fails.

The following table shows the FCS fault code for the 32 bits.

Table 20 • **FCS Fault Codes**

Bit	Description
31	Reserved to make sure that FCS check fails
30	SA hit
29:24	SA pointer If the SA-hit bit[30] is 0, then bits[29:27] are reserved, bit[26] indicates if the frame is classified as control frame, and bits[25:24] indicate the MACsec tag classification of the frame: 00b = untagged, 01b = tagged, 10b = bad tag, 11b = KaY tag
23:10	Global stat event vector
9:0	SA stat event vector

The following tables show the format of the ingress global and SA stat event vectors.

Table 21 • **Ingress Global Stat Event Vector Format**

Event Bit Position	Ingress Global Counter
0	global.TransformErrorPkts
1	global.InPktsCtrl
2	global.InPktsNoTag
3	global.InPktsUntagged
4	global.InPktsTagged
5	global.InPktsBadTag
6	global.InPktsUntaggedMiss
7	global.InPktsNoSCI
8	global.InPktsUnknownSCI
9	global.InConsistCheckControlledNotPass
10	global.InConsistCheckUncontrolledNotPass
11	global.InConsistCheckControlledPass
12	global.InConsistCheckUncontrolledPass
13	global.InOverSizePkts
14	global.ifInUcastPkts
15	global.ifInMulticastPkts
16	global.ifInBroadcastPkts
17	global.ifInOctets

Table 22 • **Ingress SA Stat Event Vector Format**

Event Bit Position	Ingress SA Stat Counter
0	sa.InOctetsDecrypted/InOctetsValidated
1	sa.InPktsUnchecked/InPktsHitDropReserved

Table 22 • **Ingress SA Stat Event Vector Format *(continued)***

Event Bit Position	Ingress SA Stat Counter
2	sa.InPktsDelayed
3	sa.InPktsLate
4	sa.InPktsOk
5	sa.InPktsInvalid
6	sa.InPktsNotValid
7	sa.InPktsNotUsingSA
8	sa.InPktsUnusedSA
9	sa.InPktsUntaggedHit
10	sa.ifInUcastPkts
11	sa.ifInMulticastPkts
12	sa.ifInBroadcastPkts

The following tables show the format of the egress global and SA stat event vectors.

Table 23 • **Egress Global Stat Event Vector Format**

Event Bit Position	Egress Global Counter
0	global.TransformErrorPkts
1	global.OutPktsCtrl
2	global.OutPktsUnknownSA
3	global.OutPktsUntagged
4	global.OutOverSizePkts (MTU check)
5	global.ifOutUcastPkts
6	global.ifOutMulticastPkts
7	global.ifOutBroadcastPkts
8	global.ifOutOctets
13:9	Reserved: zeroes

Table 24 • **Egress SA Stat Event Vector Format**

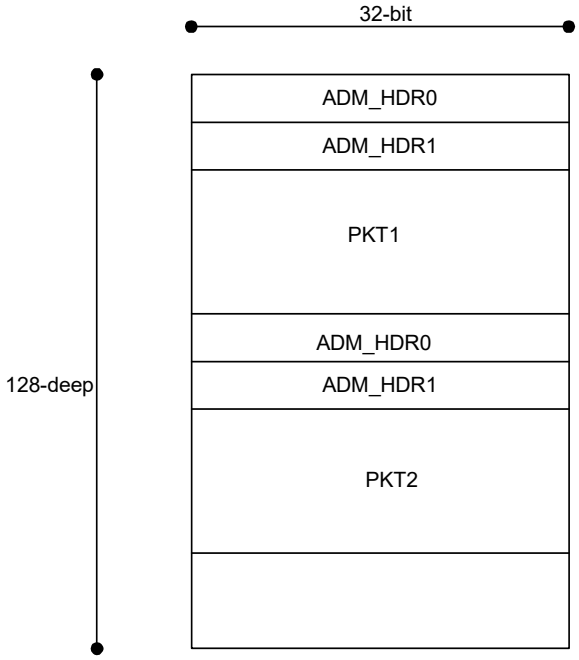
Event Bit Position	Egress SA Stat Counter
0	sa.OutOctetsEncrypted/OutOctetsProtected
1	sa.OutPktsEncrypted/OutPktsProtected/OutPktsHitDropReserved
2	sa.OutPktsTooLong (MTU check)
3	sa.ifOutUcastPkts
4	sa.ifOutMulticastPkts
5	sa.ifOutBroadcastPkts
10:6	Reserved: zeroes

3.6.7 Capture FIFO

A 512-byte capture FIFO can be used to capture up to first 504 bytes for packets failing any security check. The security fail event can be used as a trigger. The FIFO can also be enabled to capture the first

packet of any given SA using the CAPT_DEBUG_TRIGGER_SA1/2 control. Multiple packets can also be captured and the maximum size of the packet to be captured is configured using CAPT_DEBUG_CTRL.MAX_PKT_SIZE. This FIFO can be programmed to capture frames from either egress or ingress direction (CAPT_DEBUG_CTRL.SIDE). Frames are captured after MACsec transformation. Software can view the FIFO as 32-bit wide and 128 deep. Each 32-bit location is accessible to CSR using CAPT_DEBUG_DATA (0 to 127). Each packet is captured in the FIFO with a 64-bit administration header. The following illustration shows the layout of multiple packets in the capture FIFO.

Figure 41 • **Capture FIFO Layout**



Each stored packet is preceded by a 64-bit administration header that contains the following information.

- **ADM_HDR0.** 22 bits reserved, 1 bit truncated, 9 bit pkt_size
- **Truncated (1 bit).** Indicates the packet is truncated and only a part of the packet is captured. The captured packet could be truncated because the packet could be bigger than the MAX_PKT_SIZE programmed by software to capture.
- **Pkt_size (9 bits).** Indicates the size of the captured packet in bytes.
- **ADM_HDR1.** 32-bit security fail debug code, see section 4.4.1.

The status of the capture FIFO can be accessed using the CAPT_DEBUG_STATUS register (PKT_COUNT, FULL, WR_PTR).

Use the following steps to capture frames.

1. Decide the SIDE and MAX_PKT_SIZE and program in CAPT_DEBUG_CTRL.
2. Enable the SA to capture the first packet. For enabling first packet capture on any SA, program CAPT_DEBUG_TRIGGER_SA1/SA2 = 0xFFFFFFFF. To enable first packet capture on SA index [0], program CAPT_DEBUG_TRIGGER_SA1 = 0x1
3. Enable the capture by programming CAPT_DEBUG_TRIGGER.ENABLE = 1.
4. Send frames.
5. Keep polling CAPT_DEBUG_STATUS to see if any frames have been captured (PKT_COUNT, FULL, WR_PTR).
6. If PKT_COUNT > 0, then frames have been captured, read CAPT_DEBUG_TRIGGER_SA1/SA2 to confirm if the packet for that SA has been captured. Bits will fall back to 0b automatically when a packet is captured for the SA.
7. Stop the capture by programming CAPT_DEBUG_TRIGGER.ENABLE = 0 to enable software to access the FIFO.
8. Read CAPT_DEBUG_DATA (0 to 127) to read the packet from the capture FIFO.

3.6.8 Flow Control Buffer

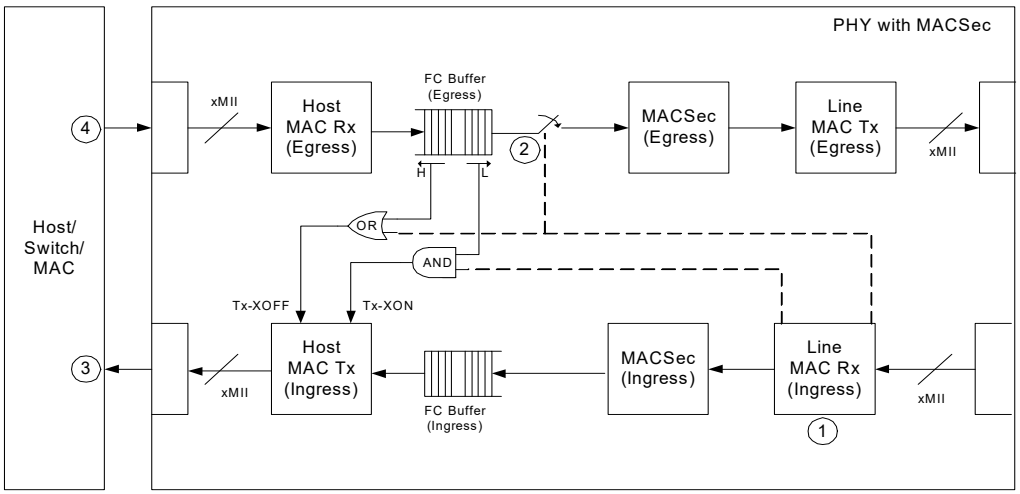
The following list provides an overview of the flow control buffer functionality in the VSC8564-11 device.

- Frame buffering in egress to handle frame expansion by MACsec and flow control back-pressure to host/switch ASIC.
- Frame buffering in ingress to handle pause frame insertion (from host MAC) and rate adaptation.
- Cut-through mode of operation.
- Configurable pause reaction (including pause timer handling) for line received pause frames.
- Pause generation triggers to host MAC based on configurable XOFF/XON thresholds.
- Control queue and data queue with strict priority scheduling in egress with highest priority given to control queue.
- Transmit MAC control frames irrespective of pause state.
- Rate adaptation between line and host clocks for PPM compensation.
- Rate difference between line and host clocks based on LAN/WAN modes.
- Flow control (back-pressure) feedback from MACsec block by compensating gap between frames.
- Pass link fault/LF/RF/LPI in both directions using special control word in-band with frames.
- EEE controller state machine for activating LPI and wake-up.
- 4X MTU buffering in egress.
- Ingress buffer for pause frame insertion by host MAC.
- ECC support in RAM's.
- Frame drops recorded for statistics.
- Sticky bits and interrupt.

3.6.8.1 Flow Control Handling

This section describes the basic flow control mode of operation. Buffering provided handles frame expansion and its own latency. Buffering required for long interconnects that depend upon cable/fiber length need to be provided separately. The following illustration shows the sequence of events when a pause frame is received from line.

Figure 42 • **Line Back-Pressure by Remote Link Partner**



The following steps describe the sequence of events depicted in the illustration.

1. Pause frame (XOFF) is received by PHY at line MAC Rx. This frame is internally consumed by MAC. The MAC Rx signals the Tx FC buffer with pause received indication and pause quanta.
2. The Tx FC buffer goes to pause state at the next frame boundary. Pause timer will be maintained by Tx FC buffer and is started only after it goes to pause state, which may be immediate in some cases. The Tx FC buffer drain rate is 0 and fill rate can be max port speed. The Tx FC buffer signals XOFF to host MAC Tx to schedule a pause transmission upstream. This signaling is shown via the optional OR gate. Without back-pressured from the remote link partner the Tx FC buffer uses XOFF/XON thresholds to signal XOFF/XON to host MAC Tx to manage frame expansion due to MACsec.

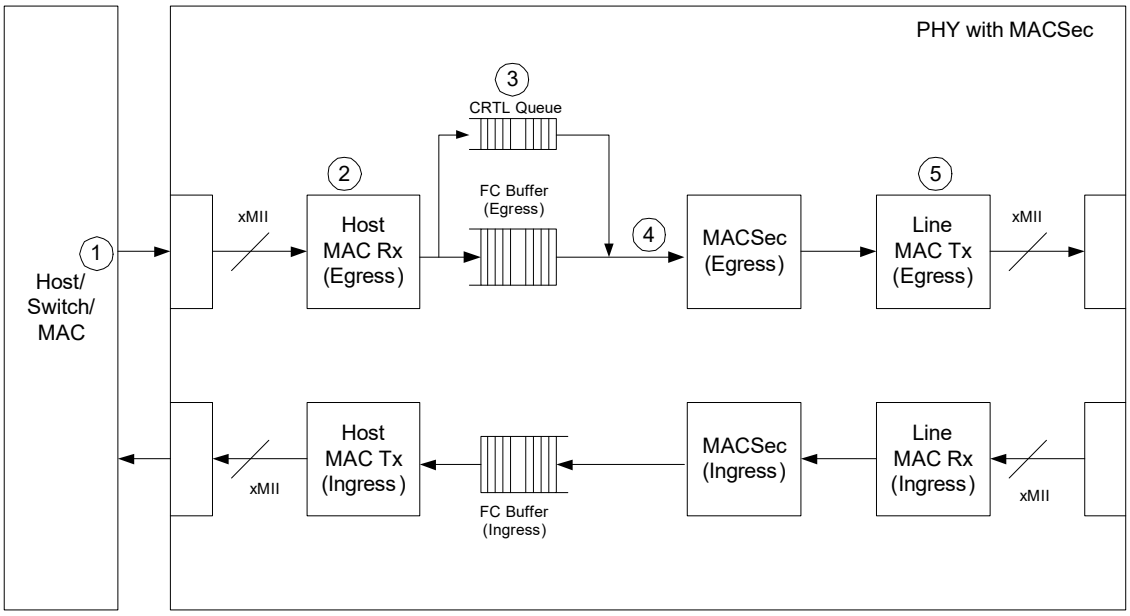
3. The host MAC Tx can schedule a pause frame for transmission at the next frame boundary. The Tx FC buffer needs to be able to hold at least one jumbo frame until XOFF pause is scheduled so that it can continue to receive data downstream. The XOFF frame is then received by host/switch.
4. The host device can only stop transmission at next frame boundary because it may have started transmitting a second jumbo frame.

The following configuration signals control the basic flow control mode.

- **PAUSE_REACT_ENA.** Enables pause reaction and pause timer maintenance in egress flow control buffer. Set to 1.
- **PAUSE_GEN_ENA.** Enables XON and XOFF pause frame signaling to host MAC based on XON and XOFF thresholds. Set to 1.
- **INCLUDE_PAUSE_RCVD_IN_PAUSE_GEN.** Enables the optional OR and AND gate. Set to 1. If not enabled the pause gen signaling to host MAC is purely based on XOFF/XON thresholds.

The following illustration shows the sequence of events when a pause frame is received from host.

Figure 43 • **Host Back-Pressure by Remote Link Partner**



The following steps describe the sequence of events depicted in the illustration.

1. Host experiences congestion in ingress and sends pause (XOFF) to line.
2. Host MAC Rx receives pause frame. It is not enabled to react on received pause frames so it passes the pause frame to Tx FC buffer.
3. Tx FC buffer maintains two logical queues, one for data and one for MAC control frames. If a data frame is already scheduled and in progress, it passes on MAC control frames at the next boundary to quickly relay MAC control frames to line, despite the presence of other data frames in the data queue.
4. Tx FC buffer transmits any or all control frames in the control queue.
5. Pause frame passes through the MACsec block. The MACsec egress block detects frame as a control frame and does not encrypt it. Frame eventually passes through the line MAC Tx block and the rest of the PHY blocks.

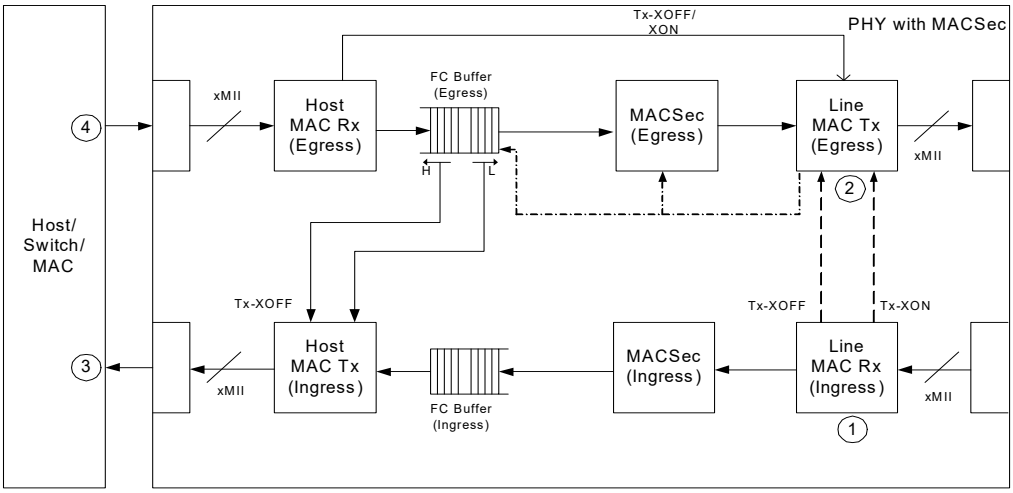
TX_CTRL_QUEUE_ENA determines if the control queue is enabled in the egress flow control buffer. This should be set to 1 in basic flow control mode. The physical memory of egress FC buffer can be partitioned between data and control queues using TX_CTRL_QUEUE_START/END and TX_DATA_QUEUE_START/END configuration fields.

3.6.8.2 Advanced Flow Control Handling

The following illustration shows the sequence of events when the PHY is configured to the advanced flow control mode of operation. PAUSE_GEN_ENA needs to be set to 1 and other configuration bits of FC

buffer, such as PAUSE_REAhT_ENA, INCLUDE_PAUSE_RCVD_IN_PAUSE_GEN, and TX_CTRL_QUEUE_ENA, need to be set to 0. All other configurations for this mode are part of line MAC and host MAC.

Figure 44 • **Advanced Flow Control Handling**



The following steps describe the sequence of events depicted in the illustration.

3.6.8.2.1 PHY Back-Pressured by Remote Link partner

1. Pause frame (XOFF) is received by PHY at line MAC Rx. This frame is internally consumed by MAC. Line MAC Rx signals line MAC Tx with pause received indication and pause quanta.
2. Line MAC Tx goes to pause state at the next frame boundary. Line MAC Tx stalls to pause the pipeline. Pause timer maintained by line MAC Tx is started only after it goes to pause state. The Tx FC buffer signals XOFF/XON to host MAC Tx based on XOFF/XON threshold.

3.6.8.2.2 Host Back-Pressuring Remote Link Partner

3. System pause is consumed by host MAC Rx. Pause timer maintained in host MAC Rx (instead of Tx) for egress direction to generate XOFF/XON pause gen signal for line MAC Tx.
4. Line MAC Tx stalls to send pause frame (either XOFF or XON). This path will work irrespective of whether line MAC is in pause state.

3.6.8.3 Frame Drop Statistics

The following 32-bit counters provide frame drop statistics. These counters roll over to 0 when the maximum value is reached.

3.6.8.3.1 TX_CTRL_QUEUE_OVERFLOW_DROP_CNT

Number of control frame drops due to overflow in the control queue of the egress flow control buffer.

3.6.8.3.2 TX_CTRL_QUEUE_UNDERFLOW_DROP_CNT

Number of control frame drops due to underflow in the control queue of the egress flow control buffer.

3.6.8.3.3 TX_CTRL_UNCORRECTED_FRM_DROP_CNT

Number of control frames aborted due to ECC check fail during reading from RAM in egress flow control buffer.

3.6.8.3.4 TX_DATA_QUEUE_OVERFLOW_DROP_CNT

Number of data frame drops due to overflow in the data queue of the egress flow control buffer.

3.6.8.3.5 TX_DATA_QUEUE_UNDERFLOW_DROP_CNT

Number of data frame drops due to underflow in the data queue of the egress flow control buffer.

3.6.8.3.6 TX_DATA_UNCORRECTED_FRM_DROP_CNT

Number of data frames aborted due to ECC check fail during reading from RAM in egress flow control buffer.

3.6.8.3.7 RX_OVERFLOW_DROP_CNT

Number of frame drops due to overflow in the ingress flow control buffer.

3.6.8.3.8 RX_UNDERFLOW_DROP_CNT.

Number of frame drops due to underflow in the ingress flow control buffer.

3.6.8.3.9 RX_UNCORRECTED_FRM_DROP_CNT.

Number of frames aborted due to ECC check fail during reading from RAM in ingress flow control buffer.

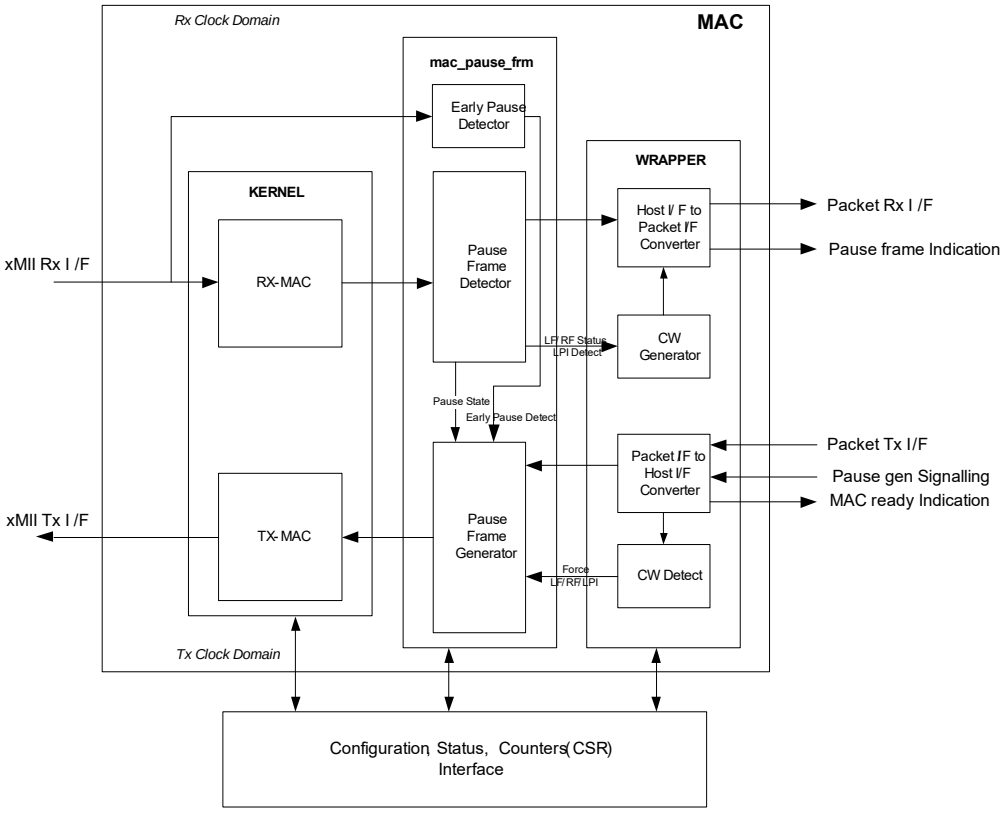
3.6.9 Media Access Control

This section describes the media access control sub layer (MAC) block. There are two instances of MAC block in each channel. One instance, which interfaces with MACsec and PCS/PMA, is called Line MAC and other instance which interfaces with FC Buffer and PHY XS is called Host MAC.

The MAC is defined in IEEE 802.3, clauses 3 and 4. The purpose of the MAC is to control the MACsec block access to the physical layer. In other words, it takes frames from the MACsec and converts those to a continuous byte stream on the xMII interface. In doing so, it is responsible for frame CRC generation and checking, preamble insertion and extraction, and pause frame generation and detection. The MAC block also contains the counters for an SNMP management information base (MIB) statistics module.

The MAC block supports frame sizes up to 10240 bytes in both receive and transmit directions. The maximum frame size is controlled by the host. The maximum frame size can also be set to the standard 1518 bytes or 1522 bytes, if desired. Maximum frame length restrictions are not enforced in the transmit direction. The following illustration shows the block diagram of MAC.

Figure 45 • **MAC Block Diagram**



3.6.9.1 MAC Transmit

The transmit section of the MAC contains three blocks, packet interface wrapper, pause frame generator, and MAC Tx kernel. All three blocks operate off the same clock, TX_MAC_CLK.

The MAC Tx kernel block handles the reconciliation sublayer functions as per IEEE 802.3.

- Calculates the CRC for pause frames generated by the pause frame generator.
- Converts MAC frames to the xMII format and adds control characters for framing as required by IEEE 802.3.
- Generates the interframe gap (IFG) on the xMII using the deficit idle count algorithm to achieve an average IPG of 12 bytes.
- Shapes all the traffic to go out with an average IPG of 12 bytes after MACsec frame expansion.
- Analyzes each packet and increments statistical counters used for RMON support.

The Pause Frame Generator (PFG) block performs the following two major functions.

- Requests packets from the upstream blocks, when packets are present and the Tx direction is not in the pause state (because a pause frame has been received in the Rx direction). They are forwarded to the MAC Tx kernel block for further processing.
- Generates flow control packets. Pause frames are generated based upon seeing the MAC_PAUSE_FRM_GEN signal. For the Host MAC this signal is generated by the FC buffer based upon programmable XOFF/XON threshold values in the FC buffer. In advance flow control mode of operation the line MAC can also generate pause frames based on MAC_PAUSE_FRM_GEN signal from Host MAC to relay pause frames that are deleted in Host MAC in this mode.

When the pause frame generator sees the MAC_PAUSE_FRM_GEN signal asserted, it generates pause frames using settings in configuration registers. Part of the pause frame is the pause value, which specifies how long the link partner (the network entity that the pause frame is destined for) stops sending traffic. The pause value specifies the requested delay in bit times and uses the equation 512 × PAUSE_VALUE.

After the PFG starts generating pause frames, it continues to generate pause frames at specified intervals until the de-assertion of the MAC_PAUSE_FRM_GEN signal. When this signal is deasserted, the PFG does one of two things, depending upon the configuration in MAC_TX_PAUSE_MODE. In normal mode, the PFG stops sending pause frames. This causes the link partner to start sending frames again after its pause frame timer has expired. In XON mode, the PFG generates a single pause frame with a pause value of 0 and sends it to the link partner. This causes the link partner to start sending frames again right away.

The PFG contains a configurable pause frame interval register, MAC_TX_PAUSE_INTERVAL. This register controls the time between generated pause frames when the FC buffer continues to request that pause frames be generated.

The packet interface wrapper handles the following functions:

- Provides the packet interfacing support to MACsec and FC buffer blocks. On this packet interface, frames are transported without preamble and FCS.
- Supports LF/RF/LPI generation on xMII interface through special control word received on packet interface. This special control word is received on packet interface if relaying of LF/RF/LPI is desired in MACsec subsystem.
- Padding of frames whose length is less than 64 bytes. This is required for padding of MACsec short length frames whose length is less than 64 bytes. This padding is enabled by configuring ENABLE_TX_PADDING in host MAC.
- Standard preamble insertion.
- FCS insertion.

3.6.9.2 MAC Receive

The receive section of the MAC contains three blocks, MAC Rx kernel, pause frame detector, and packet interface wrapper. All three blocks operate off the same clock, RX_MAC_CLK.

The MAC Rx kernel receives the byte stream from the xMII interface and handles the reconciliation sub layer processing to convert them to frames sent over the host interface. It checks the CRC of each frame for validity and abort marks any frame with an invalid CRC. A variety of length checks are performed,

including looking for short frames (less than 64 bytes), oversized, and jabber frames (longer than the configured maximum). VLAN tagging is supported up to three VLAN tags. Length checks are adjusted accordingly when VLAN tags are encountered. The Rx kernel supports counters in support of RMON statistics.

The pause frame detector (PFD) detects and reacts to valid pause frames received by the MAC from the xMII interface. The PFD reacts to PAUSE frames with a DMAC equal to either the multicast address (01-80-c2-00-00-01) or the address of the MAC (MAC_ADDRESS_LSB/MSB register value) in accordance with IEEE 802.3-2008, Annex 31B. Pause frames that are too short, or have invalid CRC, are abort marked and ignored by the PFD. Pause frames carry a pause value that indicates the desired pause time in units of pause quanta, where 1 pause-quantum equals 512 bit times. Because the data path in the MAC is 8 bytes (or 64 bits) wide, the extracted pause value is multiplied by 8 and stored in the pause counter. A signal from the PFG indicates if a packet is currently being transmitted.

After the current packet has completed or if there is no packet, the PFD tells the PFG to stop requesting packets (XOFF) and the pause counter is decremented by one for each MAC Rx clock cycle. When the counter reaches 0, the PFG is instructed that it may resume requesting packets from the upstream blocks. Pause frames must have a destination address equal to either the multicast address (01-80-c2-00-00-01) or the address of the MAC (MAC_ADDRESS_LSB/MSB register value). If there is no match, then the pause frame is ignored. If a pause frame is received while the Tx direction is already being paused (because a valid pause frame was already received and the pause counter had not yet counted down to 0), the pause counter is simply updated with the new value. If the received pause value is 0, then the state machine transitions immediately to END_PAUSE and frames are again requested from the upstream blocks.

The packet interface wrapper handles the following functions:

- Provides the packet interfacing support to MACsec and FC buffer blocks. On this packet interface, frames are transported without preamble and FCS.
- Supports LF/RF/LPI indication on packet interface through special control word. This special control word is relayed to other MAC if relaying of LF/RF/LPI is desired.
- Preamble strip on packet interface.
- FCS check and strip.

3.6.9.3 RMON Statistical Counters

The following counters count the number of bytes or frames received or transmitted. The counters count continuously and are only cleared if the device is reset or the counter is written with 0 through the CPU interface. These counters roll-over to 0 when the maximum value is reached. Unless specified otherwise, each counter is 32 bits.

- RX_IN_BYTES_CNT (40 bits) counts the total bytes received including preamble
- RX_OK_BYTES_CNT (40 bits) counts the number of bytes received in valid frames
- RX_BAD_BYTES_CNT counts the number of bytes received in invalid frames
- TX_OUT_BYTES_CNT (40 bits) counts the total number of bytes transmitted including preamble
- TX_OK_BYTES_CNT (40 bits) counts the number of bytes in successfully transmitted frames

The following counters are based on the type of frame received or transmitted.

- RX_PAUSE_CNT counts the number of pause frames received
- RX_UNSUP_OPCODE_CNT counts the number of control frames received with unsupported opcodes
- RX_UC_CNT counts the number of unicast frames received
- RX_MC_CNT counts the number of multicast frames received
- RX_BC_CNT counts the number of broadcast frames received
- TX_PAUSE_CNT counts the number of pause frames transmitted
- TX_UC_CNT counts the number of unicast frames transmitted
- TX_MC_CNT counts the number of multicast frames transmitted
- TX_BC_CNT counts the number of broadcast frames transmitted

The following error counters are provided.

- RX_SYMBOL_ERR_CNT counts the number of symbol errors received
- RX_CRC_ERR_CNT counts the number of frames received with CRC errors

- RX_UNDERSIZE_CNT counts the number of undersized frames received with valid CRC
- RX_FRAGMENTS_CNT counts the number of undersized frames received with invalid CRC
- RX_IN_RANGE_LENGTH_ERR_CNT counts the number of frames where the length field does not match the frame length
- RX_OUT_OF_RANGE_LENGTH_ERR_CNT counts the number of frames with an illegal length field
- RX_OVERSIZE_CNT counts the number of oversize frames with valid CRC
- RX_JABBERS_CNT counts the number of oversize frames with an invalid CRC
- RX_XGMII_PROT_ERR_CNT counts the number of XGMII protocol errors detected.

The following size histogram counters are provided for both transmit and receive directions.

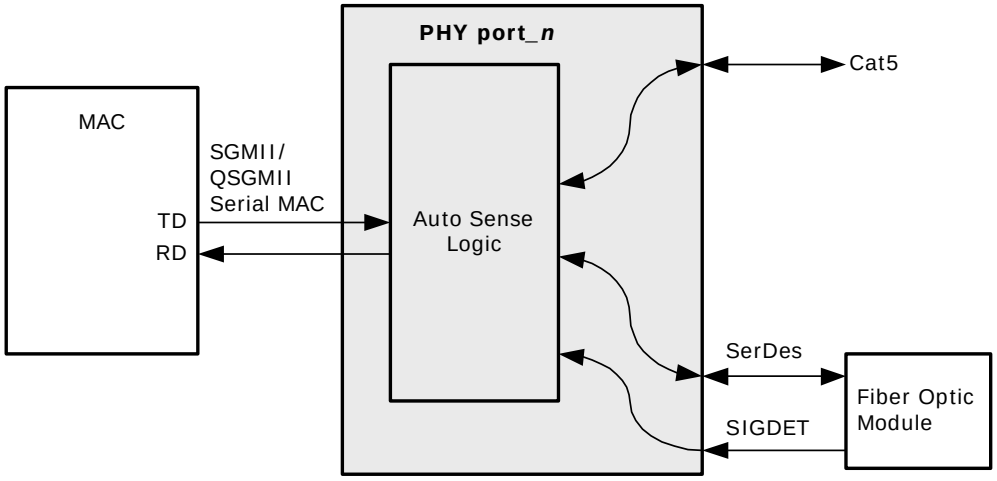
- Frames with 64-byte payloads
- Frames with 65-byte to 127-byte payloads
- Frames with 128-byte to 255-byte payloads
- Frames with 256-byte to 511-byte payloads
- Frames with 512-byte to 1023-byte payloads
- Frames with 1024-byte to 1518-byte payloads
- Frames with 1519-byte to maximum size payloads

Frame size counters also count invalid frames, as long as they are not short frames, fragments, long frames, or jabber frames. Long frames are defined as those greater than MAX_LEN bytes.

3.7 Automatic Media Sense Interface Mode

Automatic media sense (AMS) mode automatically sets the media interface to Cat5 mode or SerDes mode. The active media mode chosen is based on the automatic media sense preferences set in the device register 23, bit 11. The following illustration shows a block diagram of AMS functionality on ports 0 through 3 of the VSC8564-11 device.

Figure 46 • **Automatic Media Sense Block Diagram**



When both the SerDes and Cat5 media interfaces attempt to establish a link, the preferred media interface overrides a linkup of the nonpreferred media interface. For example, if the preference is set for SerDes mode and Cat5 media establishes a link, Cat5 becomes the active media interface. However, after the SerDes media interface establishes a link, the Cat5 interface drops its link because the preference was set for SerDes mode. In this scenario, the SerDes preference determines the active media source until the SerDes link is lost. Also, Cat5 media cannot link up unless there is no SerDes

media link established. The following table shows the possible link conditions based on preference settings.

Table 25 • **AMS Media Preferences**

Preference Setting	Cat5 Linked, Fiber Not Linked	SerDes Linked, Cat5 Not Linked	Cat5 Linked, SerDes Attempts to Link	SerDes Linked, Cat5 Attempts to Link	Both Cat5 and SerDes Attempt to Link
SerDes	Cat5	SerDes	SerDes	SerDes	SerDes
Cat5	Cat5	SerDes	Cat5	Cat5	Cat5

The status of the media mode selected by the AMS can be read from device register 20E1, bits 7:6. It indicates whether copper media, SerDes media, or no media is selected. Each PHY has four automatic media sense modes. The difference between the modes is based on the SerDes media modes:

- SGMII or QSGMII MAC to AMS and 1000BASE-X SerDes
- SGMII or QSGMII MAC to AMS and 100BASE-FX SerDes
- SGMII or QSGMII MAC to AMS and SGMII (protocol transfer)

For more information about SerDes media mode functionality with AMS enabled, see SerDes Media Interface, page 12.

3.8 Reference Clock

The device reference clock supports both 25 MHz and 125 MHz clock signals. It can be either differential or single-ended. If differential, it must be capacitively coupled and LVDS compatible.

3.8.1 Configuring the Reference Clock

The REFCLK_SEL2 pin configures the reference clock speed. The following table shows the functionality and associated reference clock frequency.

Table 26 • **REFCLK Frequency Selection**

REFCLK_SEL2	Frequency
0	25 MHz
1	125 MHz

3.8.2 Single-Ended REFCLK Input

To use a single-ended reference clock, an external resistor network is required. The purpose of the network is to limit the amplitude and to adjust the center of the swing. The configurations for a single-ended REFCLK, with the clock centered at 1 V and a 500 mV peak-to-peak swing, are shown in the following illustrations.

Figure 47 • **2.5 V CMOS Single-Ended REFCLK Input Resistor Network**

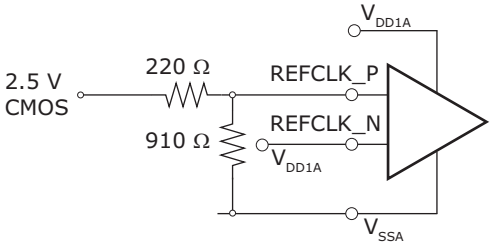


Figure 48 • **3.3 V CMOS Single-Ended REFCLK Input Resistor Network**

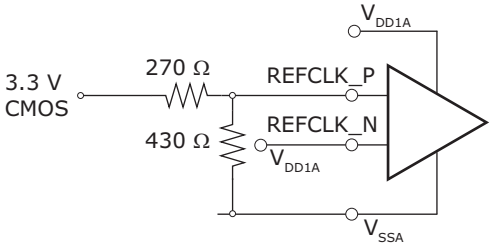
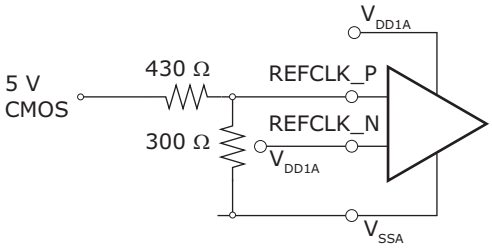


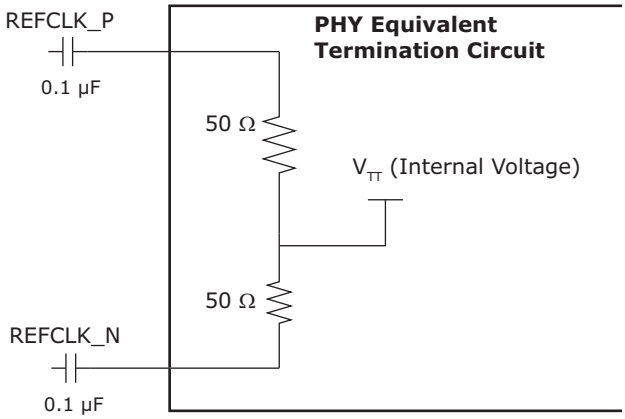
Figure 49 • **5 V CMOS Single-Ended REFCLK Input Resistor Network**



3.8.3 Differential REFCLK Input

AC coupling is required when using a differential REFCLK. Differential clocks must be capacitively coupled and LVDS-compatible. The following illustration shows the configuration.

Figure 50 • **AC Coupling for REFCLK Input**

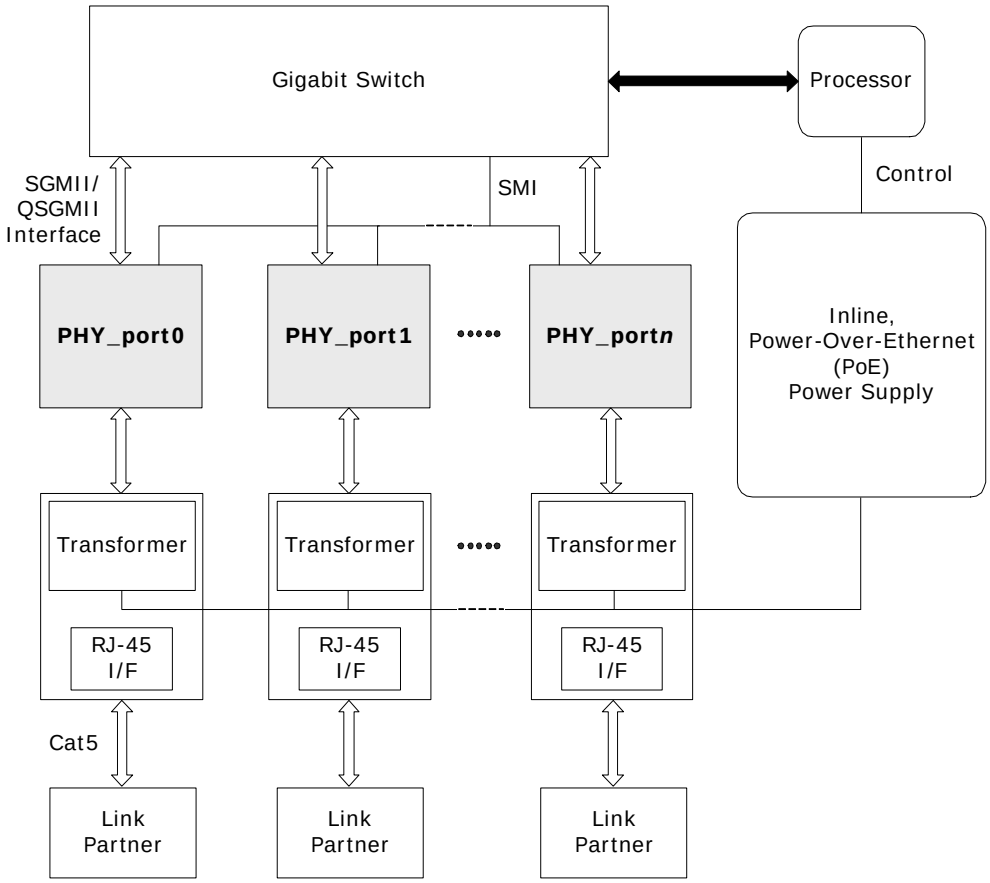


3.9 Ethernet Inline Powered Devices

The VSC8564-11 can detect legacy inline powered devices in Ethernet network applications. Inline powered detection capability is useful in systems that enable IP phones and other devices (such as wireless access points) to receive power directly from their Ethernet cable, similar to office digital phones receiving power from a private branch exchange (PBX) office switch over telephone cabling. This type of setup eliminates the need for an external power supply and enables the inline powered device to remain active during a power outage, assuming that the Ethernet switch is connected to an uninterrupted power supply, battery, back-up power generator, or other uninterruptable power source.

For more information about legacy inline powered device detection, visit the Cisco Web site at www.cisco.com. The following illustration shows an example of an inline powered Ethernet switch application.

Figure 51 • **Inline Powered Ethernet Switch Diagram**



The following procedure describes the process that an Ethernet switch must perform to process inline power requests made by a link partner (LP) that is, in turn, capable of receiving inline power:

1. Enable the inline powered device detection mode on each VSC8564-11 PHY using its serial management interface. Set register bit 23E1.10 to 1.
2. Ensure that the VSC8564-11 autonegotiation enable bit (register 0.12) is also set to 1. In the application, the device sends a special fast link pulse (FLP) signal to the LP. Reading register bit 23E1.9:8 returns 00 during the search for devices that require power over Ethernet (PoE).
3. The VSC8564-11 PHY monitors its inputs for the FLP signal looped back by the LP. An LP capable of receiving PoE loops back the FLP pulses when the LP is in a powered down state. This is reported when VSC8564-11 register bit 23E1.9:8 reads back 01. It can also be verified as an inline power detection interrupt by reading VSC8564-11 register bit 26.9, which should be a 1, and which is subsequently cleared and the interrupt de-asserted after the read. When an LP device does not loop back the FLP after a specific time, VSC8564-11 register bit 23E1.9:8 automatically resets to 10.
4. If the VSC8564-11 PHY reports that the LP requires PoE, the Ethernet switch must enable inline power on this port, externally of the PHY.
5. The PHY automatically disables inline powered device detection when the VSC8564-11 register bits 23E1.9:8 automatically reset to 10, and then automatically changes to its normal autonegotiation process. A link is then autonegotiated and established when the link status bit is set (register bit 1.2 is set to 1).
6. In the event of a link failure (indicated when VSC8564-11 register bit 1.2 reads 0), it is recommended that the inline power be disabled to the inline powered device external to the PHY. The VSC8564-11 PHY disables its normal autonegotiation process and re-enables its inline powered device detection mode.

3.10 IEEE 802.3af PoE Support

The VSC8564-11 device is compatible with designs that are intended for use in systems that supply power to data terminal equipment (DTE) by means of the MDI or twisted pair cable, as described in IEEE 802.3af Clause 33.

3.11 ActiPHY Power Management

In addition to the IEEE-specified power-down control bit (device register bit 0.11), the device also includes an ActiPHY power management mode for each PHY. This mode enables support for power-sensitive applications. It utilizes a signal-detect function that monitors the media interface for the presence of a link to determine when to automatically power-down the PHY. The PHY wakes up at a programmable interval and attempts to wake up the link partner PHY by sending a burst of FLP over copper media.

The ActiPHY power management mode in the VSC8564-11 is enabled on a per-port basis during normal operation at any time by setting register bit 28.6 to 1.

The following operating states are possible when ActiPHY mode is enabled:

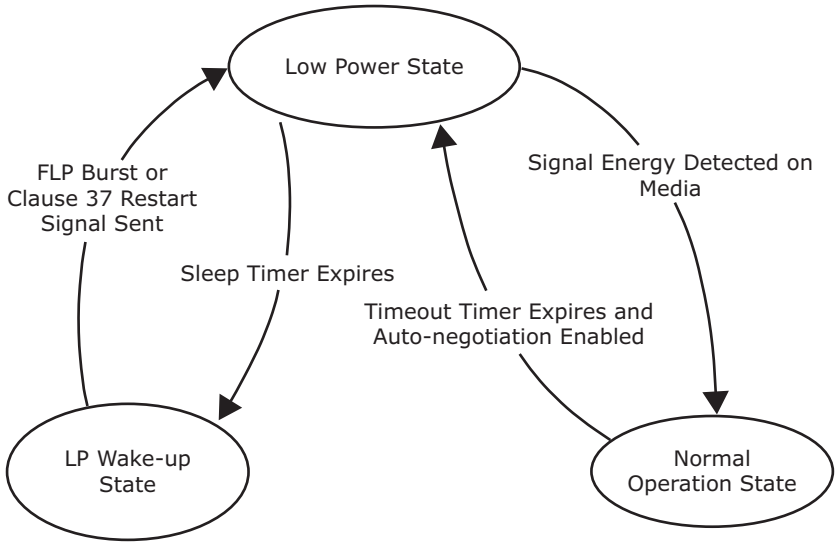
- Low power state
- Link partner wake-up state
- Normal operating state (link-up state)

The VSC8564-11 switches between the low power state and LP wake-up state at a programmable rate (the default is two seconds) until signal energy has been detected on the media interface pins. When signal energy is detected, the PHY enters the normal operating state. If the PHY is in its normal operating state and the link fails, the PHY returns to the low power state after the expiration of the link status time-out timer. After reset, the PHY enters the low power state.

When autonegotiation is enabled in the PHY, the ActiPHY state machine operates as described. When autonegotiation is disabled and the link is forced to use 10BASE-T or 100BASE-TX modes while the PHY is in its low power state, the PHY continues to transition between the low power and LP wake-up states until signal energy is detected on the media pins. At that time, the PHY transitions to the normal operating state and stays in that state even when the link is dropped. When autonegotiation is disabled while the PHY is in the normal operation state, the PHY stays in that state when the link is dropped and does not transition back to the low power state.

The following illustration shows the relationship between ActiPHY states and timers.

Figure 52 • **ActiPHY State Diagram**



3.11.1 Low Power State

In the low power state, all major digital blocks are powered down. However, the SMI interface (MDC, MDIO, and MDINT) functionality is provided.

In this state, the PHY monitors the media interface pins for signal energy. The PHY comes out of low power state and transitions to the normal operating state when signal energy is detected on the media. This happens when the PHY is connected to one of the following:

- Autonegotiation-capable link partner
- Another PHY in enhanced ActiPHY LP wake-up state

In the absence of signal energy on the media pins, the PHY periodically transitions from low-power state to LP wake-up state, based on the programmable sleep timer (register bits 20E1.14:13). The actual sleep time duration is randomized from –80 ms to 60 ms to avoid two linked PHYs in ActiPHY mode entering a lock-up state during operation.

3.11.2 Link Partner Wake-Up State

In the link partner wake-up state, the PHY attempts to wake up the link partner. Up to three complete FLP bursts are sent on alternating pairs A and B of the Cat5 media for a duration based on the wake-up timer, which is set using register bits 20E1.12:11.

In this state, SMI interface (MDC, MDIO, and MDINT) functionality is provided.

After sending signal energy on the relevant media, the PHY returns to the low power state.

3.11.3 Normal Operating State

In the normal operating state, the PHY establishes a link with a link partner. When the media is unplugged or the link partner is powered down, the PHY waits for the duration of the programmable link status time-out timer, which is set using register bit 28.7 and bit 28.2. It then enters the low power state.

3.12 SPI I/O Register Access

The VSC8564-11 device provides a bidirectional SPI I/O interface for register access to handle MACsec communication to the device. The device uses one slave select (SS) per slave for a simple slave design, and to share the SCLK, MOSI, and MISO signals. The SPI I/O port is fully independent of either the SPI time stamp input or output ports.

The following illustrations show the write and read cycle format supported by the VSC8564-11 device, with LSB_FIRST=0, BIG_ENDIAN=1, and PADDING _BYTES=3. No other formats are supported.

Figure 53 • **SPI Write Cycles**

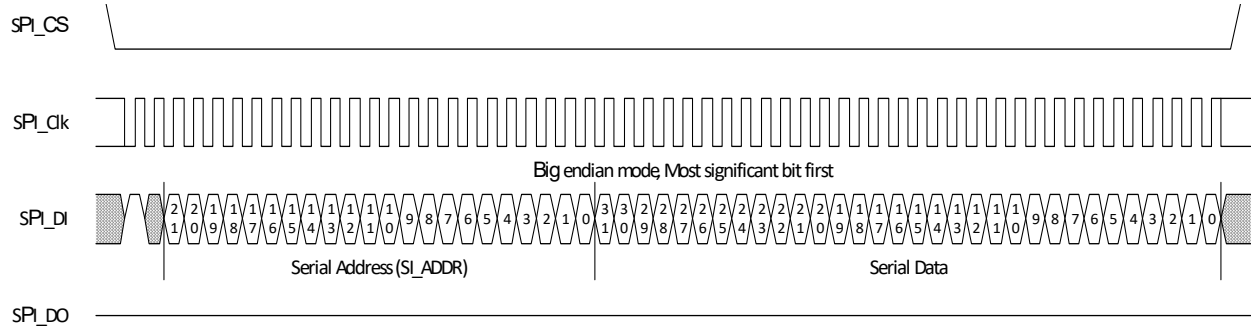
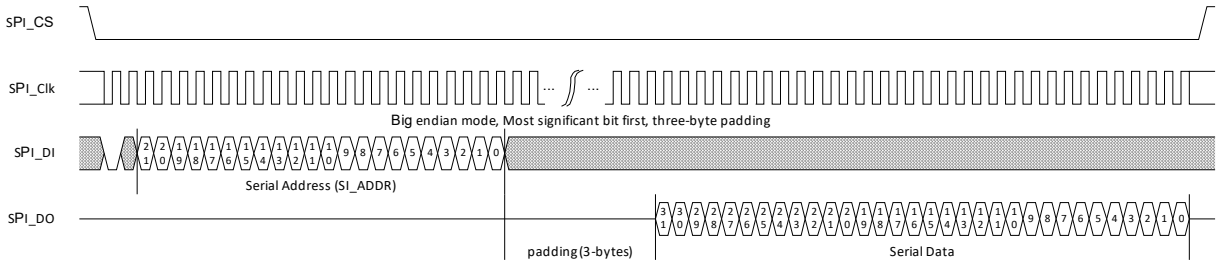


Figure 54 • **SPI Read Cycle**



A 25 MHz SPI operating rate is used to access the CSR address space.

The 22-bit address (indicated as SI_ADDR), is composed of a 2-bit ring select, an 8-bit Target ID, and a 12-bit register address. This register address represents a word address where a word is 32 bits. The SPI data is 32 bits and is consistent with this mapping.

Table 27 • **SI_ADDR Mapping**

Bit	Description
21:20	CSR ring select 00: Ring 0 01: Reserved 10: Reserved 11: Reserved
19:14	Target ID[7:2]
13:12	Target ID [1:0] for most targets CSR register address[13:12] for MACsec INGR/EGR Targets
11:0	CSR register address[11:0]

The 2-bit ring select (SI_ADDR[21:20]) selects the CSR ring. A coding of 00 selects ring 0. Coding of 01, 10, and 11 are reserved.

SI_ADDR[19:14] maps to Target ID[7:2] and SI_ADDR[11:0] maps to CSR register address bits 11:0. The Target ID[1:0] and CSR register address bits 13:12 depends on Target ID[5:3].

Target ID[5:3] bits set to 111 access the MACsec INGR or MACsec EGR registers. In this case, Target ID[1:0] is hard-coded to 00 and the CSR address bits 13:12 is supplied by SI_ADDR[13:12]. In all other cases, Target ID[1:0] is supplied by SI_ADDR[13:12] and the CSR address bits 13:12 is hard-coded to 00.

The Chip ID, Extended Chip ID, and Revision Code can be read at Target ID 0x40, address 0xFFF.

3.13 Media Recovered Clock Outputs

For Synchronous Ethernet applications, the VSC8564-11 includes two recovered clock output pins, RCVRDCLK1 and RCVRDCLK2, controlled by registers 23G and 24G, respectively. The recovered clock pins are synchronized to the clock of the active media link.

To enable recovered clock output, set register 23G or 24G, bit 15, to 1. By default, the recovered clock output pins are disabled and held low, including when NRESET is asserted. Registers 23G and 24G also control the PHY port for clock output, the clock source, the clock frequency (either 25 MHz or 31.25 MHz or 125 MHz), and squelch conditions.

Note: When EEE is enabled on a link, the use of the recovered clock output is not recommended due to long holdovers occurring during EEE quiet/refresh cycles.

3.13.1 Clock Selection Settings

On each pin, the recovered clock supports the following sources, as set by registers 23G or 24G, bits 2:0:

- Fiber SerDes media
- Copper media
- Copper transmitter TCLK output (RCVRDCLK1 only)

Note: When using the automatic media sense feature, the recovered clock output cannot automatically change between each active media. Changing the media source must be managed through the recovered clock register settings.

Adjust the squelch level to enable 1000BASE-T master mode recovered clock for SyncE operation. This is accomplished by changing the 23G and 24G register bits 5:4 to 01. This setting also provides clock out for 10BASE-T operation. For 1000BASE-T master mode, the clock is based on the VSC8564-11 REFCLK input, which is a local clock.

3.13.2 Clock Output Squelch

Under certain conditions, the PHY outputs a clock based on the REFCLK_P and REFCLK_N pins, such as when there is no link present or during autonegotiation. To prevent an undesirable clock from appearing on the recovered clock pins, the VSC8564-11 squelches, or inhibits, the clock output based on any of the following criteria:

- No link is detected (the link status register 1, bit 2 = 0).
- The link is found to be unstable using the fast link failure detection feature. The GPIO9/FASTLINK-FAIL pin is asserted high when enabled.
- The active link is in 10BASE-T or in 1000BASE-T master mode. These modes produce unreliable recovered clock sources.
- CLK_SQUELCH_IN is enabled to squelch the clock.

Use registers 23G or 24G, bits 5:4 to configure the clock squelch criteria. These registers can also disable the squelch feature. The CLK_SQUELCH_IN pin controls the squelching of the clock. Both RCVRDCLK1 and RCVRDCLK2 are squelched when the CLK_SQUELCH_IN pin is high.

3.14 Serial Management Interface

The VSC8564-11 device includes an IEEE 802.3-compliant serial management interface (SMI) that is affected by use of its MDC and MDIO pins. The SMI provides access to device control and status registers. The register set that controls the SMI consists of 32 16-bit registers, including all required IEEE-specified registers. Also, there are additional pages of registers accessible using device register 31.

Energy efficient Ethernet control registers are available through the SMI using Clause 45 registers and Clause 22 register access in registers 13 through 14. For more information, see Table 51, page 87 and Table 118, page 127.

The SMI is a synchronous serial interface with input data to the VSC8564-11 on the MDIO pin that is clocked on the rising edge of the MDC pin. It is a multiple-target bus that incorporates open-collector drivers along with an external pull-up to share the MDIO data line between multiple PHY chips. The output data is sent on the MDIO pin on the rising edge of the MDC signal. The interface can be clocked at a rate from 0 MHz to 12.5 MHz, depending on the total load on MDIO. An external 2-kΩ pull-up resistor is required on the MDIO pin.

3.14.1 SMI Frames

Data is transferred over the SMI using 32-bit frames with an optional, arbitrary-length preamble. Before the first frame can be sent, at least two clock pulses on MDC must be provided with the MDIO signal at logic one to initialize the SMI state machine. The following illustrations show the SMI frame format for read and write operations.

Figure 55 • **SMI Read Frame**

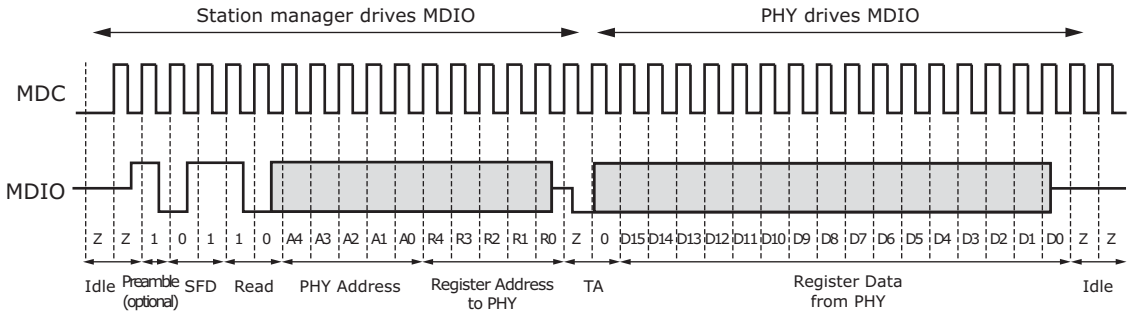
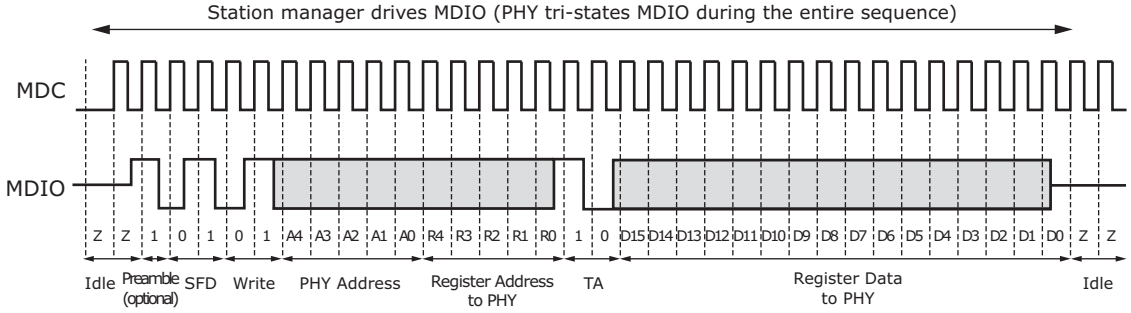


Figure 56 • **SMI Write Frame**



The following list provides additional information about the terms used in the SMI read and write timing diagrams.

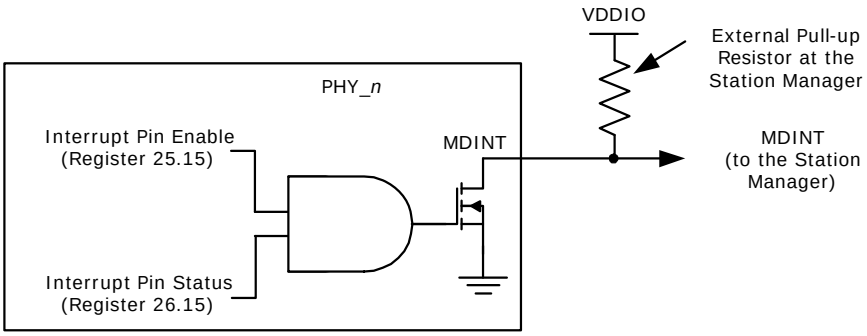
- **Idle** During idle, the MDIO node goes to a high-impedance state. This allows an external pull-up resistor to pull the MDIO node up to a logical 1 state. Because the idle mode does not contain any transitions on MDIO, the number of bits is undefined during idle.
- **Preamble** By default, preambles are not expected or required. The preamble is a string of ones. If it exists, the preamble must be at least 1 bit; otherwise, it can be of an arbitrary length.
- **Start of Frame (SFD)** A pattern of 01 indicates the start of frame. If the pattern is not 01, all following bits are ignored until the next preamble pattern is detected.
- **Read or Write Opcode** A pattern of 10 indicates a read. A 01 pattern indicates a write. If the bits are not either 01 or 10, all following bits are ignored until the next preamble pattern is detected.
- **PHY Address** The particular VSC8564-11 responds to a message frame only when the received PHY address matches its physical address. The physical address is 5 bits long (4:0).
- **Register Address** The next five bits are the register address.
- **Turnaround** The two bits used to avoid signal contention when a read operation is performed on the MDIO are called the turnaround (TA) bits. During read operations, the VSC8564-11 drives the second TA bit, a logical 0.
- **Data** The 16-bits read from or written to the device are considered the data or data stream. When data is read from a PHY, it is valid at the output from one rising edge of MDC to the next rising edge of MDC. When data is written to the PHY, it must be valid around the rising edge of MDC.
- **Idle** The sequence is repeated.

3.14.2 SMI Interrupt

The SMI includes an output interrupt signal, MDINT, for signaling the station manager when certain events occur in the VSC8564-11.

The MDINT pin is configured for open-drain (active-low). Tie the pin to a pull-up resistor to VDDIO. The following illustration shows the configuration.

Figure 57 • **MDINT Configured as an Open-Drain (Active-Low) Pin**



When a PHY generates an interrupt, the MDINT pin is asserted by driving low if the interrupt pin enable bit (MII register 25.15) is set.

3.15 LED Interface

The LED interface supports the following configurations: direct drive, basic serial LED mode, and enhanced serial LED mode. The polarity of the LED outputs is programmable and can be changed through register 17E2, bits 13:10. The default polarity is active low.

Direct drive mode provides four LED signals per port, LED0_[0:3] through LED3_[0:3]. The mode and function of each LED signal can be configured independently. When serial LED mode is enabled, the direct drive pins not used by the serial LED interface remain available.

In basic serial LED mode, all signals that can be displayed on LEDs are sent as LED_Data and LED_CLK for external processing. In enhanced serial LED mode, up to four LED signals per port can be sent as LED_Data, LED_CLK, LED_LD, and LED_Pulse. The following sections provide detailed information about the various LED modes.

Note: LED number is listed using the convention, LED<LED#>_<Port#>.

The following table shows the bit 9 settings for register 14G that are used to control the LED behavior for all the LEDs in VSC8564-11.

Table 28 • **LED Drive State**

Setting	Active	Not Active
14G.9 = 1 (default)	Ground	Tristate
14G.9 = 0 (alternate setting)	Ground	V_{DD}

3.15.1 LED Modes

Each LED pin can be configured to display different status information that can be selected by setting the LED mode in register 29. The modes listed in the following table are equivalent to the setting used in register 29 to configure each LED pin. The default LED state is active low and can be changed by modifying the value in register 17E2, bits 13:10. The blink/pulse-stretch is dependent on the LED behavior setting in register 30.

The following table provides a summary of the LED modes and functions.

Table 29 • **LED Mode and Function Summary**

Mode	Function Name	LED State and Description
0	Link/Activity	1: No link in any speed on any media interface. 0: Valid link at any speed on any media interface. Blink or pulse-stretch = Valid link at any speed on any media interface with activity present.

Table 29 • **LED Mode and Function Summary *(continued)***

Mode	Function Name	LED State and Description
1	Link1000/Activity	1: No link in 1000BASE-T or 1000BASE-X. 0: Valid 1000BASE-T or 1000BASE-X. Blink or pulse-stretch = Valid 1000BASE-T or 1000BASE-X link with activity present.
2	Link100/Activity	1: No link in 100BASE-TX or 100BASE-FX. 0: Valid 100BASE-TX or 100BASE-FX. Blink or pulse-stretch = Valid 100BASE-TX or 100BASE-FX link with activity present.
3	Link10/Activity	1: No link in 10BASE-T. 0: Valid 10BASE-T link. Blink or pulse-stretch = Valid 10BASE-T link with activity present.
4	Link100/1000/Activity	1: No link in 100BASE-TX, 100BASE-FX, 1000BASE-X, or 1000BASE-T. 0: Valid 100BASE-TX, 100BASE-FX, 1000BASE-X, or 1000BASE-T link. Blink or pulse-stretch = Valid 100BASE-TX, 100BASE-FX, 1000BASE-X, or 1000BASE-T link with activity present.
5	Link10/1000/Activity	1: No link in 10BASE-T, 1000BASE-X, or 1000BASE-T. 0: Valid 10BASE-T, 1000BASE-X, or 1000BASE-T link. Blink or pulse-stretch = Valid 10BASE-T, 1000BASE-X, or 1000BASE-T link with activity present.
6	Link10/100/Activity	1: No link in 10BASE-T, 100BASE-FX, or 100BASE-TX. 0: Valid 10BASE-T, 100BASE-FX, or 100BASE-TX link. Blink or pulse-stretch = Valid 10BASE-T, 100BASE-FX, or 100BASE-TX link with activity present.
7	Link100BASE-FX/1000BASE-X/ Activity	1: No link in 100BASE-FX or 1000BASE-X. 0: Valid 100BASE-FX or 1000BASE-X link. Blink or pulse-stretch = Valid 100BASE-FX or 1000BASE-X link with activity present.
8	Duplex/Collision	1: Link established in half-duplex mode, or no link established. 0: Link established in full-duplex mode. Blink or pulse-stretch = Link established in half-duplex mode but collisions are present.
9	Collision	1: No collision detected. Blink or pulse-stretch = Collision detected.
10	Activity	1: No activity present. Blink or pulse-stretch = Activity present (becomes TX activity present when register bit 30.14 is set to 1).
11	100BASE-FX/1000BASE-X Fiber Activity	1: No 100BASE-FX or 1000BASE-X activity present. Blink or pulse-stretch = 100BASE-FX or 1000BASE-X activity present (becomes Rx activity present when register bit 30.14 is set to 1).
12	Autonegotiation Fault	1: No autonegotiation fault present. 0: Autonegotiation fault occurred.
13	Serial Mode	Serial stream. See Basic Serial LED Mode, page 65. Only relevant on PHY port 0 and reserved in others.
14	Force LED Off	1: De-asserts the LED[1].
15	Force LED On	0: Asserts the LED[1].

1. Setting this mode suppresses LED blinking after reset.

3.15.2 Extended LED Modes

In addition to the LED modes in register 29, there are also additional LED modes that are enabled on the LED0_[3:0] pins whenever the corresponding register 19E1, bits 15 to 12 are set to 1. Each of these bits enables extended modes on a specific LED pin and these extended modes are shown in the following table. For example, LED0 = mode 17 means that register 19E1 bit 12 = 1 and register 29 bits 3 to 0 = 0001.

The following table provides a summary of the extended LED modes and functions.

Table 30 • **Extended LED Mode and Function Summary**

Mode	Function Name	LED State and Description
16	Link1000BASE-X Activity	1: No link in 1000BASE-X. 0: Valid 1000BASE-X link.
17	Link100BASE-FX Activity	1: No link in 100BASE-FX. 0: Valid 100BASE-FX link.
18	1000BASE-X Activity	1: No 1000BASE-X activity present. Blink or pulse-stretch = 1000BASE-X activity present.
19	100BASE-FX Activity	1: No 100BASE-FX activity present. Blink or pulse-stretch = 100BASE-FX activity present.
20	Force LED Off	1: De-asserts the LED.
21	Force LED On	0: Asserts the LED. LED pulsing is disabled in this mode.
22	Fast Link Fail	1: Enable fast link fail on the LED pin 0: Disable

3.15.3 LED Behavior

Several LED behaviors can be programmed into the VSC8564-11. Use the settings in register 30 and 19E1 to program LED behavior, which includes the following.

3.15.3.1 LED Combine

Enables an LED to display the status for a combination of primary and secondary modes. This can be enabled or disabled for each LED pin. For example, a copper link running in 1000BASE-T mode and activity present can be displayed with one LED by configuring an LED pin to Link1000/Activity mode. The LED asserts when linked to a 1000BASE-T partner and also blinks or performs pulse-stretch when activity is either transmitted by the PHY or received by the Link Partner. When disabled, the combine feature only provides status of the selected primary function. In this example, only Link1000 asserts the LED, and the secondary mode, activity, does not display when the combine feature is disabled.

3.15.3.2 LED Blink or Pulse-Stretch

This behavior is used for activity and collision indication. This can be uniquely configured for each LED pin. Activity and collision events can occur randomly and intermittently throughout the link-up period. Blink is a 50% duty cycle oscillation of asserting and de-asserting an LED pin. Pulse-stretch guarantees that an LED is asserted and de-asserted for a specific period of time when activity is either present or not present. These rates can also be configured using a register setting.

3.15.3.3 Rate of LED Blink or Pulse-Stretch

This behavior controls the LED blink rate or pulse-stretch length when blink/pulse-stretch is enabled on an LED pin. The blink rate, which alternates between a high and low voltage level at a 50% duty cycle, can be set to 2.5 Hz, 5 Hz, 10 Hz, or 20 Hz. For pulse-stretch, the rate can be set to 50 ms, 100 ms, 200 ms, or 400 ms. The blink rate selection for PHY0 globally sets the rate used for all LED pins on all PHY ports.

3.15.3.4 LED Pulsing Enable

To provide additional power savings, the LEDs (when asserted) can be pulsed at 5 kHz, 20% duty cycle.

3.15.3.5 LED Blink After Reset

The LEDs will blink for one second after power-up and after any time all resets have been de-asserted. This can be disabled through register 19E1, bit 11 = 0.

3.15.3.6 Fiber LED Disable

This bit controls whether the LEDs indicate the fiber and copper status (default) or the copper status only.

3.15.3.7 Pulse Programmable Control

These bits add the ability to width and frequency of LED pulses. This feature facilitates power reduction options.

3.15.3.8 Fast Link Failure

For more information about this feature, see Fast Link Failure Indication, page 66.

3.15.4 Basic Serial LED Mode

Optionally, the VSC8564-11 can be configured so that access to all its LED signals is available through two pins. This option is enabled by setting LED0 on PHY0 to serial LED mode in register 29, bits 3:0 to 0xD. When serial LED mode is enabled, the LED0_0 pin becomes the serial data pin, and the LED1_0 pin becomes the serial clock pin. All other LED pins can still be configured normally. The serial LED mode clocks the 48 LED status bits on the rising edge of the serial clock.

The LED behavior settings can also be used in serial LED mode. The controls are used on a per-PHY basis, where the LED combine and LED blink or pulse-stretch setting of LED0_n for each PHY is used to control the behavior of each bit of the serial LED stream for each corresponding PHY. To configure LED behavior, set device register 30.

The following table shows the 48-bit serial output bitstream of each LED signal. The individual signals can be clocked in the following order.

Table 31 • **LED Serial Bitstream Order**

Output	PHY0	PHY1	PHY2	PHY3
Link/activity	1	13	25	37
Link1000/activity	2	14	26	38
Link100/activity	3	15	27	39
Link10/activity	4	16	28	40
Fiber link/activity	5	17	29	41
Duplex/collision	6	18	30	42
Collision	7	19	31	43
Activity	8	20	32	44
Fiber activity	9	21	33	45
Tx activity	10	22	34	46
Rx activity	11	23	35	47
Autonegotiation fault	12	24	36	48

3.15.5 Enhanced Serial LED Mode

VSC8564-11 can be configured to output up to four LED signals per port on a serial stream that can be de-serialized externally to drive LEDs on the system board. In enhanced serial LED mode, the port 0 and port 1 LED output pins serve the following functions:

- LED0_0/LED0_1: LED_DATA
- LED1_0/LED1_1: LED_CLK
- LED2_0/LED2_1: LED_LD
- LED3_0/LED3_1: LED_PULSE

The serial LED_DATA is shifted out on the falling edge of LED_CLK and is latched in the external serial-to-parallel converter on the rising edge of LED_CLK. The falling edge of LED_LD signal can be used to shift the data from the shift register in the converter to the parallel output drive register. When a separate parallel output drive register is not used in the external serial-to-parallel converter, the LEDs will blink at a high frequency as the data bits are being shifted through, which may be undesirable. LED pin functionality is controlled by setting register 25G, bits 7:1.

The LED_PULSE signal provides a 5 kHz pulse stream whose duty cycle can be modulated to turn on/off LEDs at a high rate. This signal can be tied to the output enable signal of the serial-to-parallel converter to provide the LED dimming functionality to save energy. The LED_PULSE duty cycle is controlled by setting register 25G, bits 15:8.

3.15.6 LED Port Swapping

For additional hardware configurations, the VSC8564-11 can have its LED port order swapped. This is a useful feature to help simplify PCB layout design. Register 25G bit 0 controls the LED port swapping mode. LED port swapping only applies to the direct-drive LEDs and not to any serial LED output modes.

3.16 Fast Link Failure Indication

To aid Synchronous Ethernet applications, the VSC8564-11 can indicate the onset of a link failure in less than 1 ms (worst-case <3 ms). By comparison, the IEEE 802.3 standard establishes a delay of up to 750 ms before indicating that a 1000BASE-T link is no longer present. A fast link failure indication is critical to support ports used in a synchronization timing link application. The fast link failure indication works for all copper media speeds, but not for fiber media. Fast link failure is supported for each PHY port through the GPIO9/FASTLINK-FAIL pin.

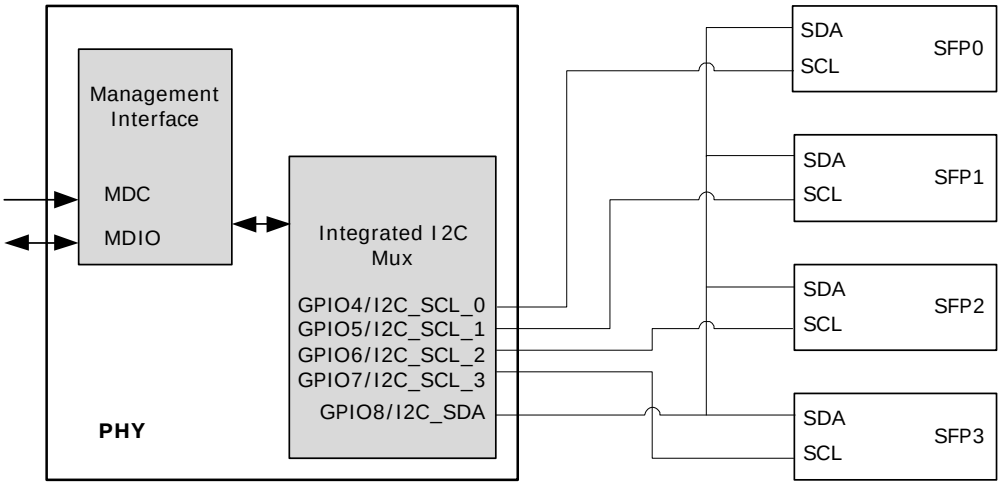
Note: For all links except 1000BASE-T, the fast link failure indication matches the link status register (address 1, bit 2). For 1000BASE-T links, the link failure is based on a circuit that analyzes the integrity of the link, and at the indication of failure, will assert.

Note: The Fast Link Failure Indication should not be used when EEE is enabled on a link.

3.17 Integrated Two-Wire Serial Multiplexer

The VSC8564-11 includes an integrated quad two-wire serial multiplexer (MUX), eliminating the need for an external two-wire serial device for the control and status of SFP or PoE modules. There are five two-wire serial controller pins: four clocks and one shared data pin. Each SFP or PoE connects to the multipurpose GPIO[7:4]_I2C_SCL_[3:0] and GPIO8/I2C_SDA device pins, which must be configured to the corresponding two-wire serial function. For more information about configuring the pins, see Two-Wire Serial MUX Control 2, page 122. For SFP modules, VSC8564-11 can also provide control for the MODULE_DETECT and TX_DIS module pins using the multipurpose LED and GPIO pins.

Figure 58 • **Two-Wire Serial MUX with SFP Control and Status**



3.17.1 Read/Write Access Using the Two-Wire Serial MUX

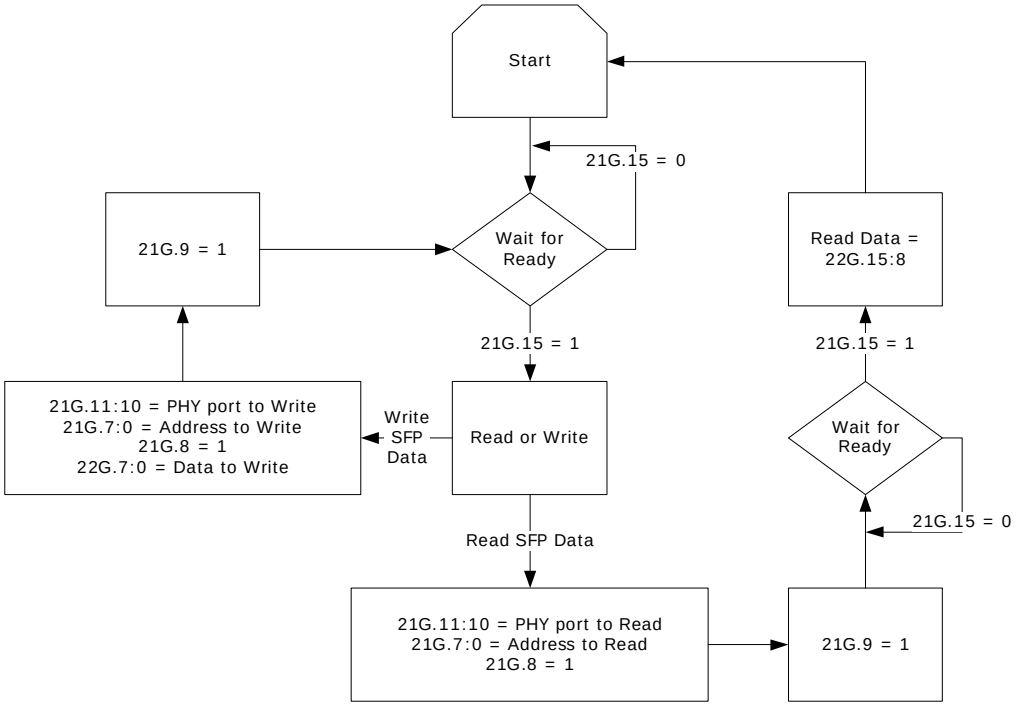
Using the integrated two-wire serial MUX, the VSC8564-11 device can read and write to an SFP or PoE module through the SCL and SDA pins. If the ability is required to write to the slave two-wire serial device, refer to the device's specific datasheet for more information.

Note: The VSC8564-11 device does not automatically increment the two-wire serial address. Each desired address must be intentionally set.

Main control of the integrated two-wire serial MUX is available through register 20G. The two-wire serial MUX pins are enabled or disabled using register 20G bits 3:0. Register 20G bits 15:9 set the two-wire serial device address (the default is 0xA0). Using register 20G bits 5:4, the two-wire serial frequency can be changed from 100 kHz to other speeds, such as 50 kHz, 100 kHz (the default), 400 kHz, and 2 MHz. Registers 21G and 22G provide status and control of the read/write process.

Clock stretching is not supported so the connected devices must be able to operate at the selected serial frequency without wait states. The following illustration shows the read and write register flow.

Figure 59 • **Two-Wire Serial MUX Read and Write Register Flow**



To read a value from a specific address of the two-wire serial slave device:

1. Read the VSC8564-11 device register 21G bit 15, and ensure that it is set.
2. Write the PHY port address to be read to register 21G bits 11:10.
3. Write the two-wire serial address to be read to register 21G bits 7:0.
4. Set both register 21G bits 8 and 9 to 1.
5. When register 21G bit 15 changes to 1, read the 8-bit data value found at register 22G bits 15:8. This is the contents of the address just read by the PHY.

To write a value to a specific address of the two-wire serial slave device:

1. Read the VSC8564-11 device register 21G bit 15 and ensure that it is set.
2. Write the PHY port address to be written to register 21G bits 11:10.
3. Write the address to be written to register 21G bits 7:0.
4. Set register 21 bit 8 to 0.
5. Set register 22G bits 7:0 with the 8-bit value to be written to the slave device.
6. Set register 21G bit 9 to 1.

To avoid collisions during read and write transactions on the two-wire serial bus, always wait until register 21G bit 15 changes to 1 before performing another two-wire serial read or write operation.

3.18 GPIO Pins

The VSC8564-11 provides 14 multiplexed general purpose input/output (GPIO) pins. All device GPIO pins and their behavior are controlled using registers. The following table shows an overview of the register controls for GPIO pins. For more information, see General Purpose Registers, page 116.

Table 32 • **Register Bits for GPIO Control and Status**

GPIO Pin	GPIO_ctrl	GPIO Input	GPIO Output	GPIO Output Enable
GPIO0/SIGDET0	13G.1:0	15G.0	16G.0	17G.0
GPIO1/SIGDET1	13G.3:2	15G.1	16G.1	17G.1
GPIO2/SIGDET2	13G.5:4	15G.2	16G.2	17G.2
GPIO3/SIGDET3	13G.7:6	15G.3	16G.3	17G.3

Table 32 • **Register Bits for GPIO Control and Status *(continued)***

GPIO Pin	GPIO_ctrl	GPIO Input	GPIO Output	GPIO Output Enable
GPIO4/I2C_SCL_0	13G.9:8.	15G.4	16G.4	17G.4
GPIO5/I2C_SCL_1	13G.11:10	15G.5	16G.5	17G.5
GPIO6/I2C_SCL_2	13G.13:12	15G.6	16G.6	17G.6
GPIO7/I2C_SCL_3	13G.15:14	15G.7	16G.7	17G.7
GPIO8/I2C_SDA	14G.1:0	15G.8	16G.8	17G.8
GPIO9/FASTLINK_FAIL	14G.3:2	15G.9	16G.9	17G.9
GPIO10	14G.5:4	15G.10	16G.10	17G.10
GPIO11	14G.7:6	15G.11	16G.11	17G.11
GPIO12	14G.15:14	15G.12	16G.12	17G.12
GPIO13	14G.15:14	15G.13	16G.13	17G.13

3.19 Testing Features

The VSC8564-11 device includes several testing features designed to facilitate performing system-level debugging and in-system production testing. This section describes the available features.

3.19.1 Ethernet Packet Generator

The Ethernet packet generator (EPG) can be used at each of the 10/100/1000BASE-T speed settings for copper Cat5 media and fiber media to isolate problems between the MAC and the VSC8564-11, or between a locally connected PHY and its remote link partner. Enabling the EPG feature effectively disables all MAC interface transmit pins and selects the EPG as the source for all data transmitted onto the twisted pair interface. This feature is not used when the SerDes media is set to pass-through mode.

Important The EPG is intended for use with laboratory or in-system testing equipment only. Do not use the EPG testing feature when the VSC8564-11 is connected to a live network.

To enable the VSC8564-11 EPG feature, set the device register bit 29E1.15 to 1.

When the EPG is enabled, packet loss occurs during transmission of packets from the MAC to the PHY. However, the PHY receive output pins to the MAC are still active when the EPG is enabled. When it is necessary to disable the MAC receive pins as well, set the register bit 0.10 to 1.

When the device register bit 29E1.14 is set to 1, the PHY begins transmitting Ethernet packets based on the settings in registers 29E1 and 30E1. These registers set:

- Source and destination addresses for each packet
- Packet size
- Interpacket gap
- FCS state
- Transmit duration
- Payload pattern

When register bit 29E1.13 is set to 0, register bit 29E1.14 is cleared automatically after 30,000,000 packets are transmitted.

3.19.2 CRC Counters

Cyclical redundancy check (CRC) counters are available in all PHYs in VSC8564-11. They monitor traffic on the copper and fiber media interfaces and on the MAC SerDes interface.

The device CRC counters operate in the 100BASE-FX/1000BASE-X over SerDes mode as well as in the 10/100/1000BASE-T mode as follows:

After receiving a packet on the media interface, register bit 15 in register 18E1, register 21E3, or register 28E3 is set and cleared after being read.

The packet then is counted by either the good CRC counter or the bad CRC counter.

Both CRC counters are also automatically cleared when read.

The good CRC counter's highest value is 9,999 packets. After this value is reached, the counter clears on the 10,000th packet and continues to count additional packets beyond that value. The bad CRC counter stops counting when it reaches its maximum counter limit of 255 packets.

3.19.2.1 Copper Interface CRC Counters

Two separate counters are available and reside at the output of the copper interface PCSs before any MACsec packet processing. There is a 14-bit good CRC counter available through register bits 18E1.13:0 and a separate 8-bit bad CRC counter available in register bits 23E1.7:0.

3.19.2.2 SerDes Fiber Media Receive CRC Counters

Two separate CRC counters are available and reside at the output of the SerDes media interface PCSs before any MACsec packet processing. To select the SerDes Fiber media receive CRC counters, set register bits 29E3.15:14 to 00. There is a 14-bit good CRC counter available through register bits 28E3.13:0 and a separate 8-bit bad CRC counter available in register bits 29E3.7:0.

3.19.2.3 SerDes Fiber Media Transmit Counters

Two fiber media transmit counters are available and reside at the input to the SerDes media interface PCSs after any MACsec packet processing. To select the SerDes Fiber media transmit CRC counters, set register 22E3.15:14 to 00. Register bits 21E3.13:0 are the good CRC packet counters and register bits 22E3.7:0 are the CRC error counters.

3.19.2.4 MAC Interface Transmit CRC Counters

Two MAC interface transmit counters are available and reside at the output of the QSGMII/SGMII MAC-interface PCS before any MACsec packet processing. To select these counters, set register 22E3.15:14 to 01. Register bits 21E3.13:0 are the good CRC packet counters and register bits 22E3.7:0 are the CRC error counters.

3.19.2.5 MAC Interface Receive CRC Counters

Two MAC interface receive counters are available and reside at the input of the QSGMII/SGMII MAC-interface PCS after any MACsec packet processing. To select these counters, set register 29E3.15:14 to 01. Register bits 28E3.13:0 are the good CRC packet counters and register bits 29E3.7:0 are the CRC error counters.

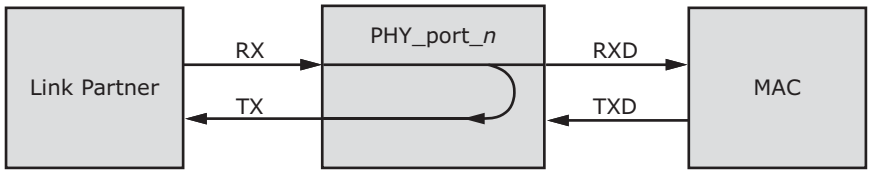
3.19.3 Loopbacks

Loopbacks described herein are for test use only, and are not recommended for use on operational links. Furthermore, the 1588 TSU block should be bypassed whenever loopbacks are enabled or disabled. Changing the packet datapath with loopbacks while the 1588 engine is processing traffic is not recommended.

3.19.3.1 Far-End Loopback

The far-end loopback testing feature is enabled by setting register bit 23.3 to 1. When enabled, it forces incoming data from a link partner on the current media interface, into the MAC interface of the PHY, to be retransmitted back to the link partner on the media interface as shown in the following illustration. In addition, the incoming data also appears on the receive data pins of the MAC interface. Data present on the transmit data pins of the MAC interface is ignored when using this testing feature.

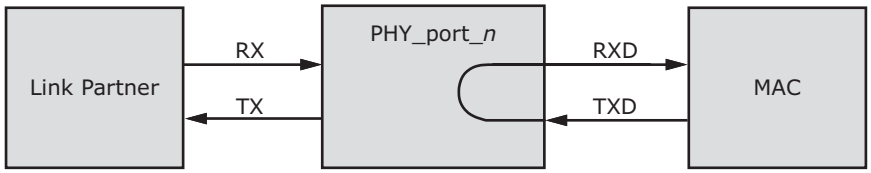
Figure 60 • **Far-End Loopback Diagram**



3.19.3.2 Near-End Loopback

When the near-end loopback testing feature is enabled, transmitted data (TXD) is looped back in the PCS block onto the receive data signals (RXD), as shown in the following illustration. When using this testing feature, no data is transmitted over the network. To enable near-end loopback, set the device register bit 0.14 to 1.

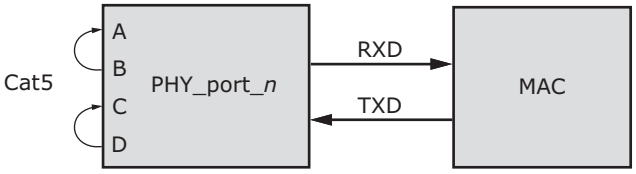
Figure 61 • **Near-End Loopback Diagram**



3.19.3.3 Connector Loopback

The connector loopback testing feature allows the twisted pair interface to be looped back externally. When using this feature, the PHY must be connected to a loopback connector or a loopback cable. Connect pair A to pair B, and pair C to pair D, as shown in the following illustration. The connector loopback feature functions at all available interface speeds.

Figure 62 • **Connector Loopback Diagram**



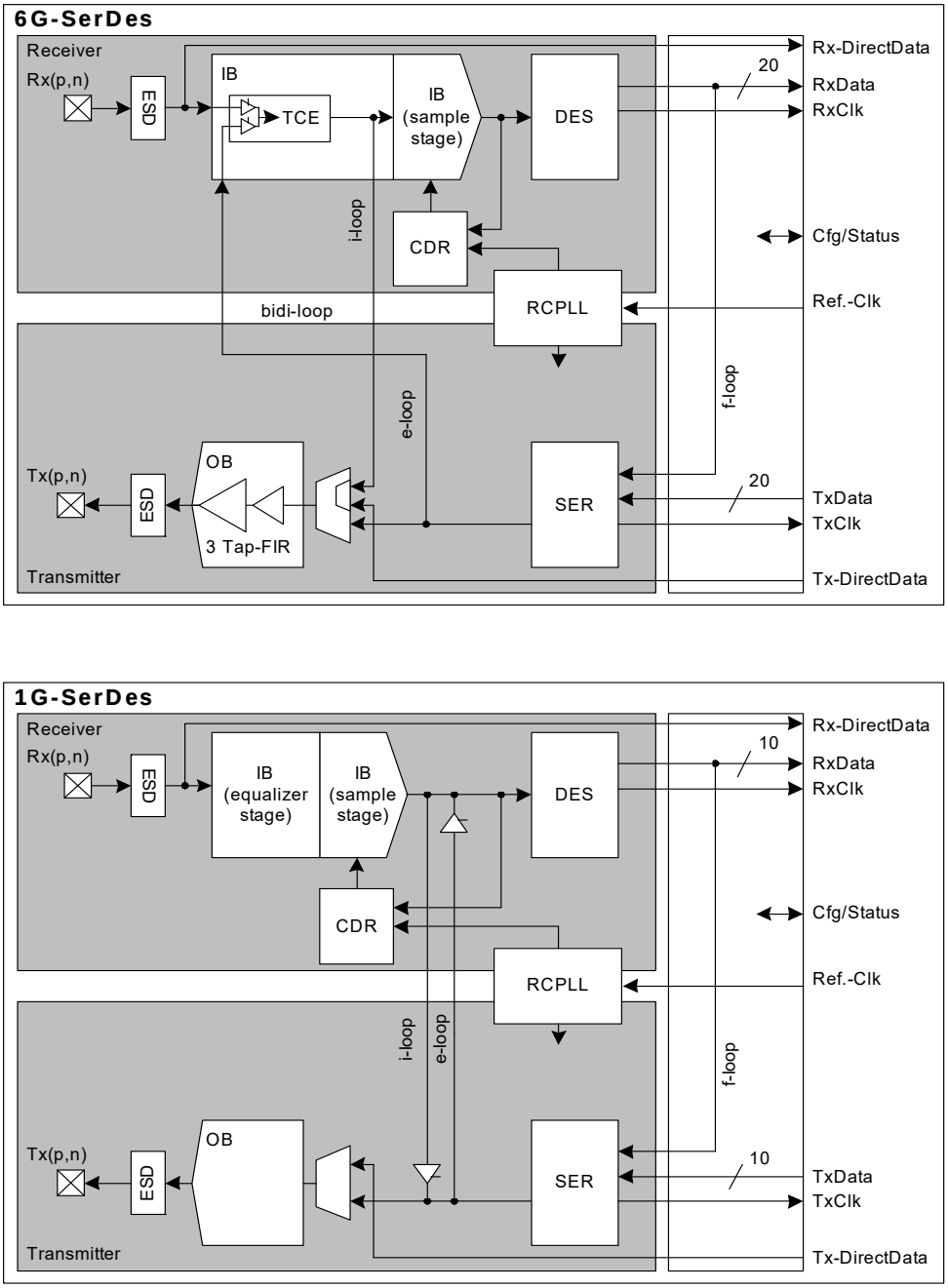
When using the connector loopback testing feature, the device autonegotiation, speed, and duplex configuration is set using device registers 0, 4, and 9. For 1000BASE-T connector loopback, the following additional writes are required. Execute the additional writes in the following order:

1. Enable the 1000BASE-T connector loopback. Set register bit 24.0 to 1.
2. Disable pair swap correction. Set register bit 18.5 to 1.

3.19.3.4 SerDes Loopbacks

For test purposes, the SerDes and SerDes macro interfaces provides several data loops. The following illustration shows the SerDes loopbacks.

Figure 63 • **Data Loops of the SerDes Macro**



3.19.3.4.1 SGMII Mode

When the MAC interface is configured in SGMII mode, write the following 16-bit value to register 18G:

Bits 15:12 0x9

Bits 11:8: Port address (0x0 to 0x3)

Bits 7:4: Loopback type

Bits 3:0: 0x2

where loopback type is:

0x0: No loopback

0x2: Input loopback

0x4: Facility loopback

0x8: Equipment loopback

3.19.3.4.2 QSGMII Mode

When the MAC interface is configured in QSGMII mode, write the following 16-bit value to register 18G:

Bits 15:12 0x9

Bits 11:8: Port address (0xC)

Bits 7:4: Loopback type

Bits 3:0: 0x2

where loopback type is:

0x0: No loopback

0x2: Input loopback

0x4: Facility loopback

0x8: Equipment loopback

Note: Loopback configuration affects all ports associated with a QSGMII. Individual port loopback within a QSGMII is not possible.

3.19.3.4.3 Fiber Media Port Mode

When the SerDes is configured as a fiber media port, write the following 16-bit value to register 18G:

Bits 15:12: 0x8

Bits 11:8: Port address

Bits 7:4: Loopback type

Bits 3:0: 0x2

where port address is:

0x1: Fiber0 port

0x2: Fiber1 port

0x4: Fiber2 port

0x8: Fiber3 port

Port addresses for fiber media SerDes can be OR'ed together to address multiple ports using a single command. bit 18G.15 will be cleared when the internal configuration is complete.

3.19.3.4.4 Facility Loop

The recovered and de-multiplexer deserializer data output is looped back to the serializer data input and replaces the data delivered by the digital core. This test loop provides the possibility to test the complete analog macro data path from outside including input buffer, clock and data recovery, serialization and output buffer. The data received by the input buffer must be transmitted by the output buffer after some delay.

3.19.3.4.5 Equipment Loop

The 1-bit data stream at the serializer output is looped back to the deserializer and replaces the received data stream from the input buffer. This test loop provides the possibility to verify the digital data path internally. The transmit data goes through the serialization, the clock and data recovery and deserialization before the data is fed back to the digital core.

Note: After entering equipment loopback mode, the following workaround should be run with set= 1 option in case external signal is not present; when exiting equipment loopback mode, the set= 0 option should be run.

SGMII/QSGMII SerDes

```
PhyWrite(<phy>, 31, 0x52b5);
PhyWrite(<phy>, 16, 0xa68c);
tmp17 = PhyRead(<phy>,17);
if (set)
tmp17 |= 0x0010; //Set SigDet as desired, Set bit 4
else // clear SigDet
tmp17 &= 0xffef; //Clear SigDet, bit 4
PhyWrite(<phy>, 17, tmp17);
PhyWrite(<phy>, 16, 0x868c);
PhyWrite(<phy>, 31, 0x0);
```

Fiber Media SerDes

```
PhyWrite(<phy>, 31, 0x52b5);
PhyWrite(<phy>, 16, 0xa68a);
tmp17 = PhyRead(<phy>,17);
if (set)
tmp17 |= 0x0010; //Set SigDet as desired, Set bit 4
else // clear SigDet
tmp17 &= 0xffef; //Clear SigDet, bit 4
PhyWrite(<phy>, 17, tmp17);
PhyWrite(<phy>, 16, 0x868a);
PhyWrite(<phy>, 31, 0x0);
```

3.19.3.4.6 Input Loop

The received 1-bit data stream of the input buffer is looped back asynchronously to the output buffer. This test loop provides the possibility to test only the analog parts of the SGMII interface because only the input and output buffer are part of this loop.

Note: When the enhanced SerDes macro is in input loopback, the output is inverted relative to the input.

The following table shows the SerDes macro address map.

Table 33 • **SerDes Macro Address Map**

SerDes Macro	Physical Address (s)	Interface Logical Type (p)	Address
SerDes0	0x0	Fiber0	0x1
SerDes1	0x1	SGMII1	0x1
SerDes2	0x2	Fiber1	0x2
SerDes3	0x3	SGMII2	0x2
SerDes4	0x4	Fiber2	0x4
SerDes5	0x5	SGMII3	0x3
SerDes6	0x6	Fiber3	0x8

3.19.4 VeriPHY Cable Diagnostics

VSC8564-11 includes a comprehensive suite of cable diagnostic functions that are available using SMI reads and writes. These functions enable cable operating conditions and status to be accessed and checked. The VeriPHY suite has the ability to identify the cable length and operating conditions and to isolate common faults that can occur on the Cat5 twisted pair cabling.

For the functional details of the VeriPHY suite and the operating instructions, see the *ENT-AN0125, PHY, Integrated PHY-Switch VeriPHY - Cable Diagnostics Feature* Application Note.

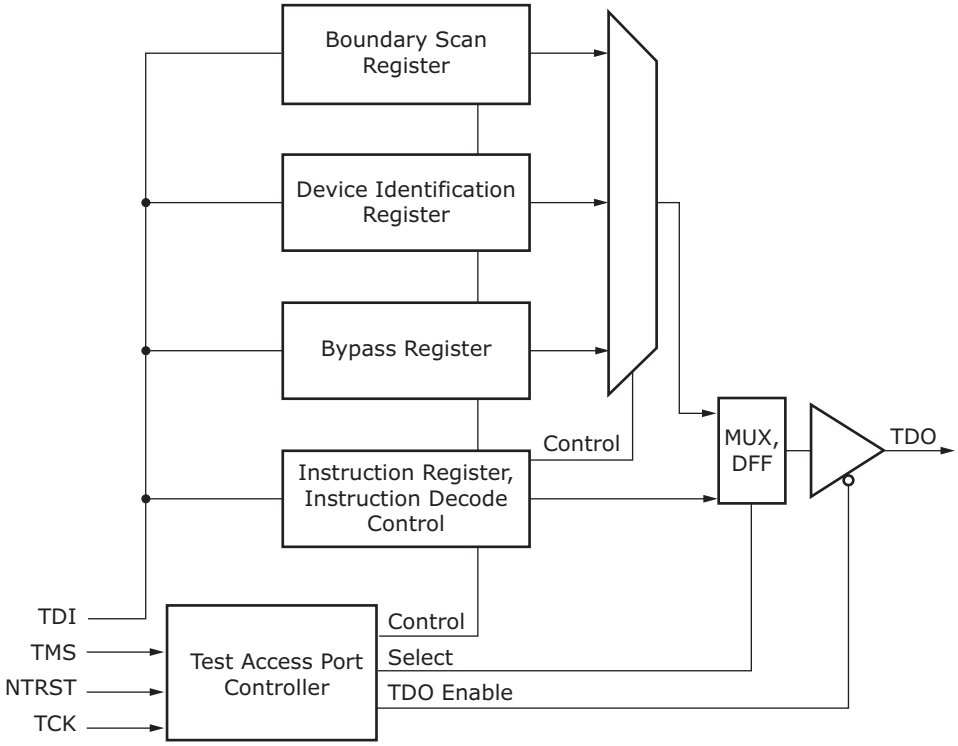
3.19.5 JTAG Boundary Scan

The VSC8564-11 supports the test access port (TAP) and boundary scan architecture described in IEEE 1149.1. The device includes an IEEE 1149.1-compliant test interface, referred to as a JTAG TAP interface.

The JTAG boundary scan logic on the VSC8564-11, accessed using its TAP interface, consists of a boundary scan register and other logic control blocks. The TAP controller includes all IEEE-required signals (TMS, TCK, TDI, and TDO), in addition to the optional asynchronous reset signal TRST. The following illustration shows the TAP and boundary scan architecture.

Important When JTAG is not in use, the TRST pin must be tied to ground with a pull-down resistor for normal operation.

Figure 64 • **Test Access Port and Boundary Scan Architecture**



After a TAP reset, the device identification register is serially connected between TDI and TDO by default. The TAP instruction register is loaded either from a shift register when a new instruction is shifted in, or, if there is no new instruction in the shift register, a default value of 6'b100000 (IDCODE) is loaded. Using this method, there is always a valid code in the instruction register, and the problem of toggling instruction bits during a shift is avoided. Unused codes are mapped to the BYPASS instruction.

3.19.6 JTAG Instruction Codes

The VSC8564-11 supports the following instruction codes:

Table 34 • **JTAG Instruction Codes**

Instruction Code	Description
BYPASS	The bypass register contains a single shift-register stage and is used to provide a minimum-length serial path (one TCK clock period) between TDI and TDO to bypass the device when no test operation is required.

Table 34 • **JTAG Instruction Codes *(continued)***

Instruction Code	Description
CLAMP	Allows the state of the signals driven from the component pins to be determined from the boundary scan register while the bypass register is selected as the serial path between TDI and TDO. While the CLAMP instruction is selected, the signals driven from the component pins do not change.
EXTEST	Allows tests of the off-chip circuitry and board-level interconnections by sampling input pins and loading data onto output pins. Outputs are driven by the contents of the boundary scan cells, which have to be updated with valid values, with the PRELOAD instruction, prior to the EXTEST instruction.
HIGHZ	Places the component in a state in which all of its system logic outputs are placed in a high-impedance state. In this state, an in-circuit test system can drive signals onto the connections normally driven by a component output without incurring a risk of damage to the component. This makes it possible to use a board where not all of the components are compatible with the IEEE 1149.1 standard.
IDCODE	Provides the version number (bits 31:28), device family ID (bits 27:12), and the manufacturer identity (bits 11:1) to be serially read from the device.
SAMPLE/PRELOAD	Allows a snapshot of inputs and outputs during normal system operation to be taken and examined. It also allows data values to be loaded into the boundary scan cells prior to the selection of other boundary scan test instructions.
USERCODE	Provides the version number (bits 31:28), part number (bits 27:12), and the manufacturer identity (bits 11:1) to be serially read from the device.

The following tables provide information about the IDCODE and USERCODE binary values stored in the device JTAG registers.

Table 35 • **IDCODE JTAG Device Identification Register Descriptions**

Description	Device Version	Family ID	Manufacturing Identity	LSB
Bit field	31–28	27–12	11–1	0
Binary value	0000	1000 0101 1000 0100	000 0111 0100	1

Table 36 • **USERCODE JTAG Device Identification Register Descriptions**

Description	Device Version	Model Number	Manufacturing Identity	LSB
Bit field	31–28	27–12	11–1	0
Binary value	0001	1000 0101 1000 0100	000 0111 0100	1

The following table provides information about the location and IEEE compliance of the JTAG instruction codes used in the VSC8564-11. Instructions not explicitly listed in the table are reserved. For more information about these IEEE specifications, visit the IEEE Web site at www.IEEE.org.

Table 37 • **JTAG Instruction Code IEEE Compliance**

Instruction	Code	Selected Register	Register Width	IEEE 1149.1
EXTEST	6'b000000	Boundary Scan	161	Mandatory
SAMPLE/PRELOAD	6'b000001	Boundary Scan	161	Mandatory
IDCODE	6'b100000	Device Identification	32	Optional
USERCODE	6'b100101	Device Identification	32	Optional
CLAMP	6'b000010	Bypass Register	1	Optional
HIGHZ	6'b000101	Bypass Register	1	Optional
BYPASS	6'b111111	Bypass Register	1	Mandatory

3.19.7 Boundary Scan Register Cell Order

All inputs and outputs are observed in the boundary scan register cells. All outputs are additionally driven by the contents of boundary scan register cells. Bidirectional pins have all three related boundary scan register cells: input, output, and control.

The complete boundary scan cell order is available as a BSDL file format on the Microsemi Web site at www.microsemi.com.

3.20 100BASE-FX Far-End Fault Indication (FEFI)

The VSC8564-11 device implements Far-End Fault Indication (FEFI) generation and detection per IEEE 802.3-2005 clause 24.3.2.5 and 24.3.2.6 in 100BASE-FX.

FEFI enables stations on both ends of a pair of fibers to be informed when there is a problem with one of the fibers. Without this capability, it is impossible for a fiber interface to detect a problem that affects only its transmit fiber.

When FEFI is supported and enabled, a loss of receive signal (link) causes the transmitter to generate a Far End Fault pattern to inform the device at the far end of the fiber pair that a fault has occurred. When the local receiver again detects a signal, the local transmitter automatically returns to normal operation.

If a Far End Fault pattern is received by a fiber interface that supports Far End Fault and has the feature enabled, it causes link status “down.”

100BASE-FX far-end fault generation force/forceval pair forces the generation of a 100BASE-FX far-end fault or suppresses the automatic generation of the 100BASE-FX far-end fault. This is controlled by 23E3.1:0, which defaults to 00. Bit 1 forces 100BASE-FX far-end fault generation on when 23E3.0 is 1 or off when 23E3.0 is 0.

100BASE-FX far-end fault detection can be determined by reading status bit 27E3.13. This is a sticky bit that indicates the 100BASE-FX far-end fault has been detected since this register was last read. This register is cleared upon reading if 100BASE-FX far-end fault is no longer detected.

3.20.1 100BASE-FX Halt Code Transmission and Reception

The VSC8564-11 device supports transmission and reception of halt code words in 100BASE-FX mode. There are three separate scripts provided to initiate transmission of halt code words, stop transmission of halt code words and detect reception of halt code words.

3.21 Configuration

The VSC8564-11 can be configured by setting internal memory registers using the management interface. To configure the device, perform the following steps:

1. COMA_MODE active, drive high.
2. Apply power.
3. Apply RefClk.
4. Release reset, drive high. Power and clock must be stable before releasing reset.
5. Wait 120 ms minimum.
6. Apply init scripts from PHY_API (required for production release, optional for board testing).
7. Configure register 19G for MAC mode (to access register 19G, register 31 must be 0x10). Read register 19G. Set bits 15:14, MAC configuration as follows:
   00: SGMII
   01: QSGMII
   10: Reserved
   11: Reserved
   Write new register 19G.
8. Configure register 18G for MAC on all PHY writes:
   SGMII: 0x80F0
   QSGMII: 0x80E0
9. Read register 18G until bit 15 equals 0.
10. If Fiber Media on all PHYs configure register 18G by writing:
    Media 1000BASE-X, Protocol Transfer: 0x8FC1
    Media 100BASE-FX: 0x8FD1
11. If Fiber Media read register 18G till bit 15 equals 0.
12. Configure register 23 for MAC and Media mode (to access register 23, register 31 must be 0). Read register 23. Set bits 10:8 as follows:
    000: Copper
    001: Protocol Transfer
    010: 1000BASE-X
    011: 100BASE-FX
    Write new register 23.
13. Software reset. Read register 0 (to access register 0, register 31 must be 0). Set bit 15 to 1. Write new register 0.
14. Read register 0 until bit 15 equals 0.
15. Apply Enhanced SerDes patch from PHY_API (required).
16. Release the COMA_MODE pin, drive low.

Note: All MAC interfaces must be the same — all QSGMII or SGMII.

3.21.1 Initialization

The COMA_MODE pin provides an optional feature that may be used to control when the PHYs become active. The typical usage is to keep the PHYs from becoming active before they have been fully initialized. For more information, see Configuration, page 77. By not being active until after complete initialization keeps links from going up and down. Alternatively the COMA_MODE pin may be connected low (ground) and the PHYs will be fully active once out of reset.

4 Registers

This section provides information about how to configure the VSC8564-11 device using its internal memory registers and the management interface. The registers marked reserved and factory test should not be read or written to, because doing so may produce undesired effects.

The default value documented for registers is based on the value at reset; however, in some cases, that value may change immediately after reset.

The access type for each register is shown using the following abbreviations:

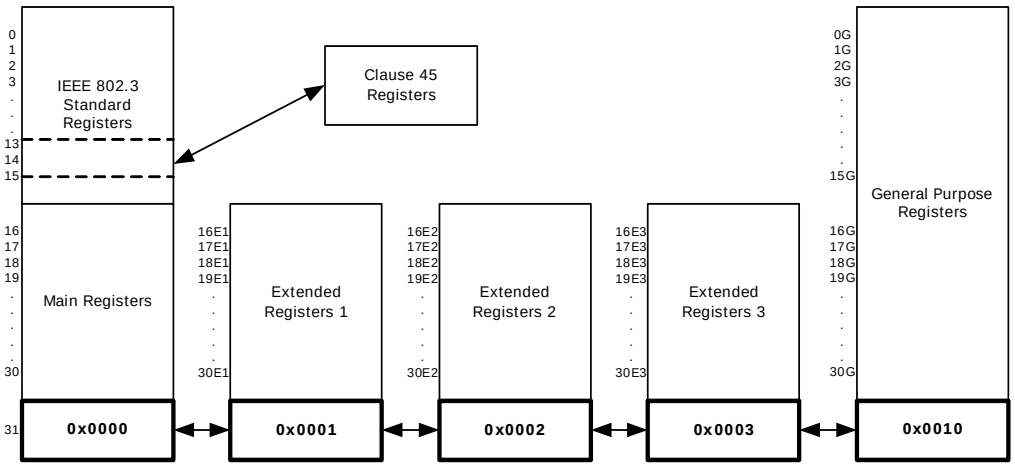
- RO: Read Only
- ROCR: Read Only, Clear on Read
- RO/LH: Read Only, Latch High
- RO/LL: Read Only, Latch Low
- R/W: Read and Write
- RWSC: Read Write Self Clearing

The VSC8564-11 uses several different types of registers:

- IEEE Clause 22 device registers with addresses from 0 to 31
- Four pages of extended registers with addresses from 16E1–30E1, 16E2–30E2, 16E3–30E3, and 16E4-30E4
- General-purpose registers with addresses from 0G to 30G
- IEEE Clause 45 devices registers accessible through the Clause 22 registers 13 and 14 to support IEEE 802.3az-2010 energy efficient Ethernet registers and IEEE 802.3bf-2011 registers

The following illustration shows the relationship between the device registers and their address spaces.

Figure 65 • **Register Space Diagram**



Reserved Registers

For main registers 16–31, extended registers 16E1–30E1, 16E2–30E2, 16E3–30E3, 16E4-30E4, and general purpose registers 0G–30G, any bits marked as Reserved should be processed as read-only and their states as undefined.

Reserved Bits

In writing to registers with reserved bits, use a read-modify-then-write technique, where the entire register is read but only the intended bits to be changed are modified. Reserved bits cannot be changed and their read state cannot be considered static or unchanging.

4.1 Register and Bit Conventions

This document refers to registers by their address and bit number in decimal notation. A range of bits is indicated with a colon. For example, a reference to address 26, bits 15 through 14 is shown as 26.15:14.

A register with an E and a number attached (example 27E1) means it is a register contained within extended register page number 1. A register with a G attached (example 13G) means it is a GPIO page register.

Bit numbering follows the IEEE standard with bit 15 being the most significant bit and bit 0 being the least significant bit.

4.2 IEEE 802.3 and Main Registers

In the VSC8564-11, the page space of the standard registers consists of the IEEE 802.3 standard registers and the Microsemi standard registers. The following table lists the names of the registers associated with the addresses as specified by IEEE 802.3.

Table 38 • **IEEE 802.3 Registers**

Address	Name
0	Mode Control
1	Mode Status
2	PHY Identifier 1
3	PHY Identifier 2
4	Autonegotiation Advertisement
5	Autonegotiation Link Partner Ability
6	Autonegotiation Expansion
7	Autonegotiation Next-Page Transmit
8	Autonegotiation Link Partner Next-Page Receive
9	1000BASE-T Control
10	1000BASE-T Status
11–12	Reserved
13	Clause 45 Access Registers from IEEE 802.3 Table 22-6 and 22.24.3.11-12 and Annex 22D
14	Clause 45 Access Registers from IEEE 802.3 Table 22-6 and 22.24.3.11-12 and Annex 22D
15	1000BASE-T Status Extension 1

The following table lists the names of the registers in the main page space of the device. These registers are accessible only when register address 31 is set to 0x0000.

Table 39 • **Main Registers**

Address	Name
16	100BASE-TX status extension
17	1000BASE-T status extension 2
18	Bypass control
19	Error Counter 1
20	Error Counter 2
21	Error Counter 3
22	Extended control and status
23	Extended PHY control 1

Table 39 • **Main Registers *(continued)***

Address	Name
24	Extended PHY control 2
25	Interrupt mask
26	Interrupt status
27	Reserved
28	Auxiliary control and status
29	LED mode select
30	LED behavior
31	Extended register page access

4.2.1 Mode Control

The device register at memory address 0 controls several aspects of VSC8564-11 functionality. The following table shows the available bit settings in this register and what they control.

Table 40 • **Mode Control, Address 0 (0x00)**

Bit	Name	Access	Description	Default
15	Software reset	R/W	Self-clearing. Restores all serial management interface (SMI) registers to default state, except for sticky and super-sticky bits. 1: Reset asserted. 0: Reset de-asserted. Wait 1 µs after setting this bit to initiate another SMI register access.	0
14	Loopback	R/W	1: Loopback enabled. 0: Loopback disabled. When loop back is enabled, the device functions at the current speed setting and with the current duplex mode setting (bits 6, 8, and 13 of this register).	0
13	Forced speed selection LSB	R/W	Least significant bit. MSB is bit 6. 00: 10 Mbps. 01: 100 Mbps. 10: 1000 Mbps. 11: Reserved.	0
12	Autonegotiation enable	R/W	1: Autonegotiation enabled. 0: Autonegotiation disabled.	1
11	Power-down	R/W	1: Power-down enabled.	0
10	Isolate	R/W	1: Disable MAC interface outputs and ignore MAC interface inputs.	0
9	Restart autonegotiation	R/W	Self-clearing bit. 1: Restart autonegotiation on media interface.	0
8	Duplex[1]	R/W	1: Full-duplex. 0: Half-duplex.	0
7	Collision test enable	R/W	1: Collision test enabled.	0
6	Forced speed selection MSB	R/W	Most significant bit. LSB is bit 13.[2] 00: 10 Mbps. 01: 100 Mbps. 10: 1000 Mbps. 11: Reserved.	10

Table 40 • **Mode Control, Address 0 (0x00) *(continued)***

Bit	Name	Access	Description	Default
5	Unidirectional enable	R/W	When bit 0.12 = 1 or bit 0.8 = 0, this bit is ignored. When bit 0.12 = 0 and bit 0.8 = 1, the behavior is as follows: 1: Enable transmit from media independent interface regardless of whether the PHY has determined that a valid link has been established. 0: Enable transmit from media independent interface only when the PHY has determined that a valid link has been established. **Note:** This bit is only applicable in 100BASE-FX and 1000BASE-X fiber media modes.	0
4:0	Reserved		Reserved.	00000

1. Half-duplex is not supported when the MACsec unit is operating or if the legacy-MAC EEE feature is enabled.
2. Before selecting the 1000 Mbps forced speed mode, manually configure the PHY as master or slave by setting bit 11 in register 9 (1000BASE-T Control). Each time the link drops, the PHY needs to be powered down manually to enable it to link up again using the master/slave setting specified in register 9.11.

4.2.2 Mode Status

The register at address 1 in the device main registers space allows you to read the currently enabled mode setting. The following table shows possible readouts of this register.

Table 41 • **Mode Status, Address 1 (0x01)**

Bit	Name	Access	Description	Default
15	100BASE-T4 capability	RO	1: 100BASE-T4 capable.	0
14	100BASE-TX FDX capability	RO	1: 100BASE-TX FDX capable.	1
13	100BASE-TX HDX capability	RO	1: 100BASE-TX HDX capable.	1
12	10BASE-T FDX capability	RO	1: 10BASE-T FDX capable.	1
11	10BASE-T HDX capability	RO	1: 10BASE-T HDX capable.	1
10	100BASE-T2 FDX capability	RO	1: 100BASE-T2 FDX capable.	0
9	100BASE-T2 HDX capability	RO	1: 100BASE-T2 HDX capable.	0
8	Extended status enable	RO	1: Extended status information present in register 15.	1
7	Unidirectional ability	RO	1: PHY able to transmit from media independent interface regardless of whether the PHY has determined that a valid link has been established. 0: PHY able to transmit from media independent interface only when the PHY has determined that a valid link has been established. **Note:** This bit is only applicable to 100BASE-FX and 1000BASE-X fiber media modes.	1
6	Preamble suppression capability	RO	1: MF preamble can be suppressed. 0: MF required.	1

Table 41 • **Mode Status, Address 1 (0x01) *(continued)***

Bit	Name	Access	Description	Default
5	Autonegotiation complete	RO	1: Autonegotiation complete.	0
4	Remote fault	RO	Latches high. 1: Far-end fault detected.	0
3	Autonegotiation capability	RO	1: Autonegotiation capable.	1
2	Link status	RO	Latches low. 1: Link is up.	0
1	Jabber detect	RO	Latches high. 1: Jabber condition detected.	0
0	Extended capability	RO	1: Extended register capable.	1

4.2.3 Device Identification

All 16 bits in both register 2 and register 3 in the VSC8564-11 are used to provide information associated with aspects of the device identification. The following tables list the expected readouts.

Table 42 • **Identifier 1, Address 2 (0x02)**

Bit	Name	Access	Description	Default
15:0	Organizationally unique identifier (OUI)	RO	OUI most significant bits (3:18)	0×0007

Table 43 • **Identifier 2, Address 3 (0x03)**

Bit	Name	Access	Description	Default
15:10	OUI	RO	OUI least significant bits (19:24)	000001
9:4	Microsemi model number	RO	VSC8564-11 (0x3C)	111100
3:0	Device revision number	RO	Revision B	0001

4.2.4 Autonegotiation Advertisement

The bits in address 4 in the main registers space control the VSC8564-11 ability to notify other devices of the status of its autonegotiation feature. The following table shows the available settings and readouts.

Table 44 • **Device Autonegotiation Advertisement, Address 4 (0x04)**

Bit	Name	Access	Description	Default
15	Next page transmission request	R/W	1: Request enabled	0
14	Reserved	RO	Reserved	0
13	Transmit remote fault	R/W	1: Enabled	0
12	Reserved	R/W	Reserved	0
11	Advertise asymmetric pause	R/W	1: Advertises asymmetric pause	0
10	Advertise symmetric pause	R/W	1: Advertises symmetric pause	0
9	Advertise100BASE-T4	R/W	1: Advertises 100BASE-T4	0
8	Advertise100BASE-TX FDX	R/W	1: Advertise 100BASE-TX FDX	1
7	Advertise100BASE-TX HDX	R/W	1: Advertises 100BASE-TX HDX	1
6	Advertise10BASE-T FDX	R/W	1: Advertises 10BASE-T FDX	1

Table 44 • **Device Autonegotiation Advertisement, Address 4 (0x04) *(continued)***

Bit	Name	Access	Description	Default
5	Advertise10BASE-T HDX	R/W	1: Advertises 10BASE-T HDX	1
4:0	Advertise selector	R/W		00001

4.2.5 Link Partner Autonegotiation Capability

The bits in main register 5 can be used to determine if the Cat5 link partner (LP) used with the VSC8564-11 is compatible with the autonegotiation functionality.

Table 45 • **Autonegotiation Link Partner Ability, Address 5 (0x05)**

Bit	Name	Access	Description	Default
15	LP next page transmission request	RO	1: Requested	0
14	LP acknowledge	RO	1: Acknowledge	0
13	LP remote fault	RO	1: Remote fault	0
12	Reserved	RO	Reserved	0
11	LP advertise asymmetric pause	RO	1: Capable of asymmetric pause	0
10	LP advertise symmetric pause	RO	1: Capable of symmetric pause	0
9	LP advertise 100BASE-T4	RO	1: Capable of 100BASE-T4	0
8	LP advertise 100BASE-TX FDX	RO	1: Capable of 100BASE-TX FDX	0
7	LP advertise 100BASE-TX HDX	RO	1: Capable of 100BASE-TX HDX	0
6	LP advertise 10BASE-T FDX	RO	1: Capable of 10BASE-T FDX	0
5	LP advertise 10BASE-T HDX	RO	1: Capable of 10BASE-T HDX	0
4:0	LP advertise selector	RO		00000

4.2.6 Autonegotiation Expansion

The bits in main register 6 work together with those in register 5 to indicate the status of the LP autonegotiation functioning. The following table shows the available settings and readouts.

Table 46 • **Autonegotiation Expansion, Address 6 (0x06)**

Bit	Name	Access	Description	Default
15:5	Reserved	RO	Reserved.	All zeros
4	Parallel detection fault	RO	This bit latches high. 1: Parallel detection fault.	0
3	LP next page capable	RO	1: LP is next page capable.	0
2	Local PHY next page capable	RO	1: Local PHY is next page capable.	1
1	Page received	RO	This bit latches low. 1: New page is received.	0
0	LP is autonegotiation capable	RO	1: LP is capable of autonegotiation.	0

4.2.7 Transmit Autonegotiation Next Page

The settings in register 7 in the main registers space provide information about the number of pages in an autonegotiation sequence. The following table shows the settings available.

Table 47 • **Autonegotiation Next Page Transmit, Address 7 (0x07)**

Bit	Name	Access	Description	Default
15	Next page	R/W	1: More pages follow	0
14	Reserved	RO	Reserved	0
13	Message page	R/W	1: Message page 0: Unformatted page	1
12	Acknowledge 2	R/W	1: Complies with request 0: Cannot comply with request	0
11	Toggle	RO	1: Previous transmitted LCW = 0 0: Previous transmitted LCW = 1	0
10:0	Message/unformatted code	R/W		00000000001

4.2.8 Autonegotiation Link Partner Next Page Receive

The bits in register 8 of the main register space work together with register 7 to determine certain aspects of the LP autonegotiation. The following table shows the possible readouts.

Table 48 • **Autonegotiation LP Next Page Receive, Address 8 (0x08)**

Bit	Name	Access	Description	Default
15	LP next page	RO	1: More pages follow	0
14	Acknowledge	RO	1: LP acknowledge	0
13	LP message page	RO	1: Message page 0: Unformatted page	0
12	LP acknowledge 2	RO	1: LP complies with request	0
11	LP toggle	RO	1: Previous transmitted LCW = 0 0: Previous transmitted LCW = 1	0
10:0	LP message/unformatted code	RO		All zeros

4.2.9 1000BASE-T Control

The VSC8564-11's 1000BASE-T functionality is controlled by the bits in register 9 of the main register space. The following table shows the settings and readouts available.

Table 49 • **1000BASE-T Control, Address 9 (0x09)**

Bit	Name	Access	Description	Default
15:13	Transmitter test mode	R/W	000: Normal 001: Mode 1: Transmit waveform test 010: Mode 2: Transmit jitter test as master 011: Mode 3: Transmit jitter test as slave 100: Mode 4: Transmitter distortion test 101–111: Reserved	000
12	Master/slave manual configuration	R/W	1: Master/slave manual configuration enabled	0

Table 49 • **1000BASE-T Control, Address 9 (0x09) *(continued)***

Bit	Name	Access	Description	Default
11	Master/slave value	R/W	This register is only valid when bit 9.12 is set to 1. 1: Configure PHY as master during negotiation 0: Configure PHY as slave during negotiation	0
10	Port type	R/W	1: Multi-port device 0: Single-port device	1
9	1000BASE-T FDX capability	R/W	1: PHY is 1000BASE-T FDX capable	1
8	1000BASE-T HDX capability	R/W	1: PHY is 1000BASE-T HDX capable	1
7:0	Reserved	R/W	Reserved	0x00

Note: Transmitter test mode (bits 15:13) operates in the manner described in IEEE 802.3 section 40.6.1.1.2. When using any of the transmitter test modes, the automatic media sense feature must be disabled. For more information, see Extended PHY Control Set 1, page 91.

4.2.10 1000BASE-T Status

The bits in register 10 of the main register space can be read to obtain the status of the 1000BASE-T communications enabled in the device. The following table shows the readouts.

Table 50 • **1000BASE-T Status, Address 10 (0x0A)**

Bit	Name	Access	Description	Default
15	Master/slave configuration fault	RO	This bit latches high. 1: Master/slave configuration fault detected 0: No master/slave configuration fault detected	0
14	Master/slave configuration resolution[1]	RO	1: Local PHY configuration resolved to master 0: Local PHY configuration resolved to slave	1
13	Local receiver status	RO	1: Local receiver is operating normally	0
12	Remote receiver status	RO	1: Remote receiver OK	0
11	LP 1000BASE-T FDX capability	RO	1: LP 1000BASE-T FDX capable	0
10	LP 1000BASE-T HDX capability	RO	1: LP 1000BASE-T HDX capable	0
9:8	Reserved	RO	Reserved	00
7:0	Idle error count	RO	Self-clearing register	0x00

1. Indicates initial state and PCS scrambler in use. It does not change if Ring Resiliency is being used and the timing Master/Slave relationship is changed.

4.2.11 MMD Access Control Register

The bits in register 13 of the main register space are a window to the EEE registers as defined in IEEE 802.3az-2010 Clause 45.

Table 51 • **MMD EEE Access, Address 13 (0x0D)**

Bit	Name	Access	Description
15:14	Function	R/W	00: Address 01: Data, no post increment 10: Data, post increment for read and write 11: Data, post increment for write only
13:5	Reserved	R/W	Reserved
4:0	DVAD	R/W	Device address as defined in IEEE 802.3az-2010 table 45–1

4.2.12 MMD Address or Data Register

The bits in register 14 of the main register space are a window to the EEE registers as defined in IEEE 802.3az-2010 Clause 45.

Table 52 • **MMD Address or Data Register, Address 14 (0x0E)**

Bit	Name	Access	Description
15:0	Register Address/Data	R/W	When register 13.15:14 = 2'b00, address of register of the device that is specified by 13.4:0. Otherwise, the data to be written to or read from the register.

4.2.13 1000BASE-T Status Extension 1

Register 15 provides additional information about the operation of the device 1000BASE-T communications. The following table shows the readouts available.

Table 53 • **1000BASE-T Status Extension 1, Address 15 (0x0F)**

Bit	Name	Access	Description	Default
15	1000BASE-X FDX capability	RO	1: PHY is 1000BASE-X FDX capable	0
14	1000BASE-X HDX capability	RO	1: PHY is 1000BASE-X HDX capable	0
13	1000BASE-T FDX capability	RO	1: PHY is 1000BASE-T FDX capable	1
12	1000BASE-T HDX capability	RO	1: PHY is 1000BASE-T HDX capable	1
11:0	Reserved	RO	Reserved	0x000

4.2.14 100BASE-TX/FX Status Extension

Register 16 in the main registers page space of the VSC8564-11 provides additional information about the status of the device's 100BASE-TX/100BASE-FX operation.

Table 54 • **100BASE-TX/FX Status Extension, Address 16 (0x10)**

Bit	Name	Access	Description	Default
15	100BASE-TX/FX Descrambler	RO	1: Descrambler locked	0
14	100BASE-TX/FX lock error	RO	Self-clearing bit. 1: Lock error detected	0

Table 54 • **100BASE-TX/FX Status Extension, Address 16 (0x10) *(continued)***

Bit	Name	Access	Description	Default
13	100BASE-TX/FX disconnect state	RO	Self-clearing bit. 1: PHY 100BASE-TX link disconnect detected	0
12	100BASE-TX/FX current link status	RO	1: PHY 100BASE-TX link active	0
11	100BASE-TX/FX receive error	RO	Self-clearing bit. 1: Receive error detected	0
10	100BASE-TX/FX transmit error	RO	Self-clearing bit. 1: Transmit error detected	0
9	100BASE-TX/FX SSD error	RO	Self-clearing bit. 1: Start-of-stream delimiter error detected	0
8	100BASE-TX/FX ESD error	RO	Self-clearing bit. 1: End-of-stream delimiter error detected	0
7:0	Reserved	RO	Reserved	

4.2.15 1000BASE-T Status Extension 2

The second status extension register is at address 17 in the device main registers space. It provides information about another set of parameters associated with 1000BASE-T communications. For information about the first status extension register, see Table 53, page 87.

Table 55 • **1000BASE-T Status Extension 2, Address 17 (0x11)**

Bit	Name	Access	Description	Default
15	1000BASE-T descrambler	RO	1: Descrambler locked.	0
14	1000BASE-T lock error	RO	Self-clearing bit. 1: Lock error detected	0
13	1000BASE-T disconnect state	RO	Self-clearing bit. 1: PHY 1000BASE-T link disconnect detected	0
12	1000BASE-T current link status	RO	1: PHY 1000BASE-T link active	0
11	1000BASE-T receive error	RO	Self-clearing bit. 1: Receive error detected	0
10	1000BASE-T transmit error	RO	Self-clearing bit. 1: Transmit error detected	0
9	1000BASE-T SSD error	RO	Self-clearing bit. 1: Start-of-stream delimiter error detected	0
8	1000BASE-T ESD error	RO	Self-clearing bit. 1: End-of-stream delimiter error detected	0
7	1000BASE-T carrier extension error	RO	Self-clearing bit. 1: Carrier extension error detected	0
6	Non-compliant BCM5400 detected	RO	1: Non-compliant BCM5400 link partner detected	0
5	MDI crossover error	RO	1: MDI crossover error was detected	0

Table 55 • **1000BASE-T Status Extension 2, Address 17 (0x11) *(continued)***

Bit	Name	Access	Description	Default
4:0	Reserved	RO	Reserved	

4.2.16 Bypass Control

The bits in this register control aspects of functionality in effect when the device is disabled for the purpose of traffic bypass. The following table shows the settings available.

Table 56 • **Bypass Control, Address 18 (0x12)**

Bit	Name	Access	Description	Default
15	Transmit disable	R/W	1: PHY transmitter disabled	0
14	4B5B encoder/decoder	R/W	1: Bypass 4B/5B encoder/decoder	0
13	Scrambler	R/W	1: Bypass scrambler	0
12	Descrambler	R/W	1: Bypass descrambler	0
11	PCS receive	R/W	1: Bypass PCS receiver	0
10	PCS transmit	R/W	1: Bypass PCS transmit	0
9	LFI timer	R/W	1: Bypass Link Fail Inhibit (LFI) timer	0
8	Reserved	RO	Reserved	
7	HP Auto-MDIX at forced 10/100	R/W	Sticky bit. 1: Disable HP Auto-MDIX at forced 10/100 speeds	1
6	Non-compliant BCM5400 detect disable	R/W	Sticky bit. 1: Disable non-compliant BCM5400 detection	0
5	Disable pair swap correction (HP Auto-MDIX when autonegotiation enabled)	R/W	Sticky bit. 1: Disable the automatic pair swap correction	0
4	Disable polarity correction	R/W	Sticky bit. 1: Disable polarity inversion correction on each subchannel	0
3	Parallel detect control	R/W	Sticky bit. 1: Do not ignore advertised ability 0: Ignore advertised ability	1
2	Pulse shaping filter	R/W	1: Disable pulse shaping filter	0
1	Disable automatic 1000BASE-T next page exchange	R/W	Sticky bit. 1: Disable automatic 1000BASE T next page exchanges	0
0	Reserved	RO	Reserved	

Note: If bit 18.1 is set to 1 in this register, automatic exchange of next pages is disabled, and control is returned to the user through the SMI after the base page is exchanged. The user then must send the correct sequence of next pages to the link partner, determine the common capabilities, and force the device into the correct configuration following the successful exchange of pages.

4.2.17 Error Counter 1

The bits in register 19 provide an error counter. The following table shows the settings available.

Table 57 • **Extended Control and Status, Address 19 (0x13)**

Bit	Name	Access	Description	Default
15:8	Reserved	RO	Reserved.	
7:0	100/1000 receive error counter	RO	8-bit counter that saturates when it reaches 255. These bits are self-clearing when read.	0x00

4.2.18 Error Counter 2

The bits in register 20 provide an error counter. The following table shows the settings available.

Table 58 • **Extended Control and Status, Address 20 (0x14)**

Bit	Name	Access	Description	Default
15:8	Reserved	RO	Reserved.	
7:0	100/1000 false carrier counter	RO	8-bit counter that saturates when it reaches 255. These bits are self-clearing when read.	0x00

4.2.19 Error Counter 3

The bits in register 21 provide an error counter. The following table shows the settings available.

Table 59 • **Extended Control and Status, Address 21 (0x15)**

Bit	Name	Access	Description	Default
15:8	Reserved	RO	Reserved.	
7:0	Copper media link disconnect counter	RO	8-bit counter that saturates when it reaches 255. These bits are self-clearing when read.	0x00

4.2.20 Extended Control and Status

The bits in register 22 provide additional device control and readouts. The following table shows the settings available.

Table 60 • **Extended Control and Status, Address 22 (0x16)**

Bit	Name	Access	Description	Default
15	Force 10BASE-T link high	R/W	Sticky bit. 1: Bypass link integrity test 0: Enable link integrity test	0
14	Jabber detect disable	R/W	Sticky bit. 1: Disable jabber detect	0
13	Disable 10BASE-T echo	R/W	Sticky bit. 1: Disable 10BASE-T echo	1
12	Disable SQE mode	R/W	Sticky bit. 1: Disable SQE mode	1

Table 60 • **Extended Control and Status, Address 22 (0x16) *(continued)***

Bit	Name	Access	Description	Default
11:10	10BASE-T squelch control	R/W	Sticky bit. 00: Normal squelch 01: Low squelch 10: High squelch 11: Reserved	00
9	Sticky reset enable	R/W	Super-sticky bit. 1: Enabled	1
8	EOF Error	RO	This bit is self-clearing. 1: EOF error detected	0
7	10BASE-T disconnect state	RO	This bit is self-clearing. 1: 10BASE-T link disconnect detected	0
6	10BASE-T link status	RO	1: 10BASE-T link active	0
5:1	Reserved	RO	Reserved	
0	SMI broadcast write	R/W	Sticky bit. 1: Enabled	0

The following information applies to the extended control and status bits:

- When bit 22.15 is set, the link integrity state machine is bypassed and the PHY is forced into a link pass status.
- When bits 22.11:10 are set to 00, the squelch threshold levels are based on the IEEE standard for 10BASE-T. When set to 01, the squelch level is decreased, which can improve the bit error rate performance on long loops. When set to 10, the squelch level is increased and can improve the bit error rate in high-noise environments.
- When bit 22.9 is set, all sticky register bits retain their values during a software reset. Clearing this bit causes all sticky register bits to change to their default values upon software reset. Super-sticky bits retain their values upon software reset regardless of the setting of bit 22.9.
- When bit 22.0 is set, if a write to any PHY register (registers 0–31, including extended registers), the same write is broadcast to all PHYs. For example, if bit 22.0 is set to 1 and a write to PHY0 is executed (register 0 is set to 0x1040), all PHYs' register 0s are set to 0x1040. Disabling this bit restores normal PHY write operation. Reads are still possible when this bit is set, but the value that is read corresponds only to the particular PHY being addressed.

4.2.21 Extended PHY Control Set 1

The following table shows the settings available.

Table 61 • **Extended PHY Control 1, Address 23 (0x17)**

Bit	Name	Access	Description	Default
15:13	Reserved	R/W	Reserved	0
12	MAC interface mode	R/W	Super-sticky bit. 0: SGMII 1: 1000BASE-X. **Note:** Register 19G.15:14 must be = 00 for this selection to be valid.	0
11	AMS preference	R/W	Super-sticky bit. 1: Cat5 copper preferred. 0: SerDes fiber/SFP preferred.	0

Table 61 • **Extended PHY Control 1, Address 23 (0x17) *(continued)***

Bit	Name	Access	Description	Default
10:8	Media operating mode	R/W	Super-sticky bits. 000: Cat5 copper only. 001: SerDes fiber/SFP protocol transfer mode only. 010: 1000BASE-X fiber/SFP media only with autonegotiation performed by the PHY. 011: 100BASE-FX fiber/SFP on the fiber media pins only. 101: Automatic media sense (AMS) with Cat5 media or SerDes fiber/SFP protocol transfer mode. 110: AMS with Cat5 media or 1000BASE-X fiber/SFP media with autonegotiation performed by PHY. 111: AMS with Cat5 media or 100BASE-FX fiber/SFP media. 100: Reserved.	000
7:6	Force AMS override	R/W	00: Normal AMS selection 01: Force AMS to select SerDes media only 10: Force AMS to select copper media only 11: Reserved	00
5:4	Reserved	RO	Reserved.	
3	Far-end loopback mode	R/W	1: Enabled.	0
2:0	Reserved	RO	Reserved.	

Note: After configuring bits 13:8 of the extended PHY control register set 1, a software reset (register 0, bit 15) must be written to change the device operating mode. On read, these bits only indicate the actual operating mode and not the pending operating mode setting before a software reset has taken place.

4.2.22 Extended PHY Control Set 2

The second set of extended controls is located in register 24 in the main register space for the device. The following table shows the settings and readouts available.

Table 62 • **Extended PHY Control 2, Address 24 (0x18)**

Bit	Name	Access	Description	Default
15:13	100BASE-TX edge rate control	R/W	Sticky bit. 011: +5 edge rate (slowest) 010: +4 edge rate 001: +3 edge rate 000: +2 edge rate 111: +1 edge rate 110: Default edge rate 101: –1 edge rate 100: –2 edge rate (fastest)	000
12	PICMG 2.16 reduced power mode	R/W	Sticky bit. 1: Enabled	0
11:6	Reserved	RO	Reserved	

Table 62 • **Extended PHY Control 2, Address 24 (0x18) *(continued)***

Bit	Name	Access	Description	Default
5:4	Jumbo packet mode	R/W	Sticky bit. 00: Normal IEEE 1.5 kB packet length 01: 9 kB jumbo packet length (12 kB with 60 ppm or better reference clock) 10: 12 kB jumbo packet length (16 kB with 70 ppm or better reference clock) 11: Reserved	00
3:1	Reserved	RO	Reserved	
0	1000BASE-T connector loopback	R/W	1: Enabled	0

Note: When bits 5:4 are set to jumbo packet mode, the default maximum packet values are based on 100 ppm driven reference clock to the device. Controlling the ppm offset between the MAC and the PHY as specified in the bit description results in a higher jumbo packet length.

4.2.23 Interrupt Mask

These bits control the device interrupt mask. The following table shows the settings available.

Table 63 • **Interrupt Mask, Address 25 (0x19)**

Bit	Name	Access	Description	Default
15	MDINT interrupt status enable	R/W	Sticky bit. 1: Enabled.	0
14	Speed state change mask	R/W	Sticky bit. 1: Enabled.	0
13	Link state change mask	R/W	Sticky bit. 1: Enabled.	0
12	FDX state change mask	R/W	Sticky bit. 1: Enabled.	0
11	Autonegotiation error mask	R/W	Sticky bit. 1: Enabled.	0
10	Autonegotiation complete mask	R/W	Sticky bit. 1: Enabled.	0
9	Inline powered device (PoE) detect mask	R/W	Sticky bit. 1: Enabled.	0
8	Symbol error interrupt mask	R/W	Sticky bit. 1: Enabled.	0
7	Fast link failure interrupt mask	R/W	Sticky bit. 1: Enabled.	0
6	Reserved	R/W	Reserved	0
5	Extended interrupt mask	R/W	Sticky bit. 1: Enabled	0
4	AMS media changed mask[1]	R/W	Sticky bit. 1: Enabled.	0
3	False carrier interrupt mask	R/W	Sticky bit. 1: Enabled.	0
2	Link speed downshift detect mask	R/W	Sticky bit. 1: Enabled.	0
1	Master/Slave resolution error mask	R/W	Sticky bit. 1: Enabled.	0
0	RX_ER interrupt mask	R/W	Sticky bit. 1: Enabled.	0

1. If hardware interrupts are not used, the mask can still be set and the status polled for changes.

Note: When bit 25.15 is set, the MDINT pin is enabled. When enabled, the state of this pin reflects the state of bit 26.15. Clearing this bit only inhibits the MDINT pin from being asserted. Also, before enabling this bit, read register 26 to clear any previously inactive interrupts pending that will cause bit 26.15 to be set.

4.2.24 Interrupt Status

The status of interrupts already written to the device is available for reading from register 26 in the main registers space. The following table shows the expected readouts.

Table 64 • **Interrupt Status, Address 26 (0x1A)**

Bit	Name	Access	Description	Default
15	Interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0
14	Speed state change status	RO	Self-clearing bit. 1: Interrupt pending.	0
13	Link state change status	RO	Self-clearing bit. 1: Interrupt pending.	0
12	FDX state change status	RO	Self-clearing bit. 1: Interrupt pending.	0
11	Autonegotiation error status	RO	Self-clearing bit. 1: Interrupt pending.	0
10	Autonegotiation complete status	RO	Self-clearing bit. 1: Interrupt pending.	0
9	Inline powered device detect status	RO	Self-clearing bit. 1: Interrupt pending.	0
8	Symbol error status	RO	Self-clearing bit. 1: Interrupt pending.	0
7	Fast link failure detect status	RO	Self-clearing bit. 1: Interrupt pending.	0
6	Reserved	RO		0
5	Extended interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0
4	AMS media changed status[1]	RO	Self-clearing bit. 1: Interrupt pending.	0
3	False carrier interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0
2	Link speed downshift detect status	RO	Self-clearing bit. 1: Interrupt pending.	0
1	Master/Slave resolution error status	RO	Self-clearing bit. 1: Interrupt pending.	0
0	RX_ER interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0

1. If hardware interrupts are not used, the mask can still be set and the status polled for changes.

The following information applies to the interrupt status bits:

- All set bits in this register are cleared after being read (self-clearing). If bit 26.15 is set, the cause of the interrupt can be read by reading bits 26.14:0.
- For bits 26.14 and 26.12, bit 0.12 must be set for this interrupt to assert.
- For bit 26.2, bits 4.8:5 must be set for this interrupt to assert.
- For bit 26.0, this interrupt will not occur when RX_ER is used for carrier-extension decoding of a link partner's data transmission.

4.2.25 Device Auxiliary Control and Status

Register 28 provides control and status information for several device functions not controlled or monitored by other device registers. The following table shows the settings available and the expected readouts.

Table 65 • **Auxiliary Control and Status, Address 28 (0x1C)**

Bit	Name	Access	Description	Default
15	Autonegotiation complete	RO	Duplicate of bit 1.5 when autonegotiation is enabled, otherwise this is the current link status	0

Table 65 • **Auxiliary Control and Status, Address 28 (0x1C)** ***(continued)***

Bit	Name	Access	Description	Default
14	Autonegotiation disabled	RO	Inverted duplicate of bit 0.12 or AMS-enabled with 100BASE-FX operating mode selected	0
13[1]	HP Auto-MDIX crossover indication	RO	1: HP Auto-MDIX crossover performed internally	0
12	CD pair swap	RO	1: CD pairs are swapped	0
11	A polarity inversion	RO	1: Polarity swap on pair A	0
10	B polarity inversion	RO	1: Polarity swap on pair B	0
9	C polarity inversion	RO	1: Polarity swap on pair C	0
8	D polarity inversion	RO	1: Polarity swap on pair D	0
7	ActiPHY link status time-out control [1]	R/W	Sticky bit. Bits 7 and 2 are part of the ActiPHY Link Status time-out control. Bit 7 is the MSB. 00: 2.3 seconds 01: 3.3 seconds 10: 4.3 seconds 11: 5.3 seconds	0
6	ActiPHY mode enable	R/W	Sticky bit. 1: Enabled	0
5	FDX status	RO	1: Full-duplex 0: Half-duplex	00
4:3	Speed status	RO	00: Speed is 10BASE-T 01: Speed is 100BASE-TX or 100BASE-FX 10: Speed is 1000BASE-T or 1000BASE-X 11: Reserved	0
2	ActiPHY link status time-out control [0]	R/W	Sticky bit. Bits 7 and 2 are part of the ActiPHY Link Status time-out control. Bit 7 is the MSB. 00: 2.3 seconds 01: 3.3 seconds 10: 4.3 seconds 11: 5.3 seconds	1
1:0	Media mode status	RO	00: No media selected 01: Copper media selected 10: SerDes (Fiber) media selected 11: Reserved	00

1. In 1000BT mode, if Force MDI crossover is performed while link is up, the 1000BT link must be re-negotiated in order for this bit to reflect the actual Auto-MDIX setting.

4.2.26 LED Mode Select

The device LED outputs are controlled using the bits in register 29 of the main register space. The following table shows the information needed to access the functionality of each of the outputs. For more

information about LED modes, see Table 29, page 62. For information about enabling the extended LED mode bits in Register 19E1 bits 13 to 12, see Table 30, page 64.

Table 66 • **LED Mode Select, Address 29 (0x1D)**

Bit	Name	Access	Description	Default
15:12	LED3 mode select	R/W	Sticky bit. Select from LED modes 0–15.	1000
11:8	LED2 mode select	R/W	Sticky bit. Select from LED modes 0–15.	0000
7:4	LED1 mode select	R/W	Sticky bit. Select from LED modes 0–15.	0010
3:0	LED0 mode select	R/W	Sticky bit. Select from LED modes 0–15.	0001

4.2.27 LED Behavior

The bits in register 30 control and enable you to read the status of the pulse or blink rate of the device LEDs. The following table shows the settings you can write to the register or read from the register.

Table 67 • **LED Behavior, Address 30 (0x1E)**

Bit	Name	Access	Description	Default
15	Copper and fiber LED combine disable	R/W	Sticky bit 0: Combine enabled (Copper/Fiber on link/linkXXXX/activity LED) 1: Disable combination (link/linkXXXX/activity LED; indicates copper only)	0
14	Activity output select	R/W	Sticky bit 1: Activity LED becomes TX_Activity and fiber activity LED becomes RX_Activity 0: Tx and Rx activity both displayed on activity LEDs	0
13	Reserved	RO	Reserved	
12	LED pulsing enable	R/W	Sticky bit 0: Normal operation 1: LEDs pulse with a 5 kHz, programmable duty cycle when active	0
11:10	LED blink/pulse-stretch rate	R/W	Sticky bit 00: 2.5 Hz blink rate/400 ms pulse-stretch 01: 5 Hz blink rate/200 ms pulse-stretch 10: 10 Hz blink rate/100 ms pulse-stretch 11: 20 Hz blink rate/50 ms pulse-stretch The blink rate selection for PHY0 globally sets the rate used for all LED pins on all PHY ports	01
9	Reserved	RO	Reserved	
8	LED3 pulse-stretch/blink select	R/W	Sticky bit 1: Pulse-stretch 0: Blink	0
7	LED2 pulse-stretch/blink select	R/W	Sticky bit 1: Pulse-stretch 0: Blink	0
6	LED1 pulse-stretch/blink select	R/W	Sticky bit 1: Pulse-stretch 0: Blink	0

Table 67 • **LED Behavior, Address 30 (0x1E)** ***(continued)***

Bit	Name	Access	Description	Default
5	LED0 pulse-stretch/blink select	R/W	Sticky bit 1: Pulse-stretch 0: Blink	0
4	Reserved	RO	Reserved	
3	LED3 combine feature disable	R/W	Sticky bit 0: Combine enabled (link/activity, duplex/collision) 1: Disable combination (link only, duplex only)	0
2	LED2 combine feature disable	R/W	Sticky bit 0: Combine enabled (link/activity, duplex/collision) 1: Disable combination (link only, duplex only)	0
1	LED1 combine feature disable	R/W	Sticky bit 0: Combine enabled (link/activity, duplex/collision) 1: Disable combination (link only, duplex only)	0
0	LED0 combine feature disable	R/W	Sticky bit 0: Combine enabled (link/activity, duplex/collision) 1: Disable combination (link only, duplex only)	0

Note: Bits 30.11:10 are active only in port 0 and affect the behavior of LEDs for all the ports.

4.2.28 Extended Page Access

To provide functionality beyond the IEEE 802.3-specified registers and main device registers, the VSC8564-11 includes an extended set of registers that provide an additional 15 register spaces.

The register at address 31 controls the access to the extended registers for the VSC8564-11. Accessing the GPIO page register space is similar to accessing the extended page registers. The following table shows the settings available.

Table 68 • **Extended/GPIO Register Page Access, Address 31 (0x1F)**

Bit	Name	Access	Description	Default
15:0	Extended/GPIO page register access	R/W	0x0000: Register 16–30 accesses main register space. Writing 0x0000 to register 31 restores the main register access. 0x0001: Registers 16–30 access extended register space 1 0x0002: Registers 16–30 access extended register space 2 0x0003: Registers 16–30 access extended register space 3 0x0004: Registers 16-30 access extended register space 4 0x0010: Registers 0–30 access GPIO register space	0x0000

4.3 Extended Page 1 Registers

To access the extended page 1 registers (16E1–30E1), enable extended register access by writing 0x0001 to register 31. Writing 0x0000 to register 31 restores the main register access.

When extended page 1 register access is enabled, reads and writes to registers 16–30 affect the extended registers 16E1–30E1 instead of those same registers in the IEEE-specified register space. Registers 0–15 are not affected by the state of the extended page register access.

Table 69 • **Extended Registers Page 1 Space**

Address	Name
16E1	SerDes Media Control
17E1	Reserved
18E1	Cu Media CRC good counter
19E1	Extended mode and SIGDET control
20E1	Extended PHY control 3 (ActiPHY)
21E1–22E1	Reserved
23E1	Extended PHY control 4 (PoE and CRC error counter)
24E1	Reserved
25E1	Reserved
26E1	Reserved
27E1–28E1	Reserved
29E1	Ethernet packet generator (EPG) 1
30E1	EPG 2

4.3.1 SerDes Media Control

Register 16E1 controls some functions of the SerDes media interface on ports 0–3. These settings are only valid for those ports. The following table shows the setting available in this register.

Table 70 • **SerDes Media Control, Address 16E1 (0x10)**

Bit	Name	Access	Description	Default
15:14	Transmit remote fault	R/W	Remote fault indication sent to link partner (LP)	00
13:12	Link partner (LP) remote fault	RO	Remote fault bits sent by LP during autonegotiation	00
11:10	Reserved	RO	Reserved	
9	Allow 1000BASE-X link-up	R/W	Sticky bit. 1: Allow 1000BASE-X fiber media link-up capability 0: Suppress 1000BASE-X fiber media link-up capability	1
8	Allow 100BASE-FX link-up	R/W	Sticky bit. 1: Allow 100BASE-FX fiber media link-up capability 0: Suppress 100BASE-FX fiber media link-up capability	1
7	Reserved	RO	Reserved	
6	Far end fault detected in 100BASE-FX	RO	Self-clearing bit. 1: Far end fault in 100BASE-FX detected	0
5:0	Reserved	RO	Reserved	

4.3.2 Cu Media CRC Good Counter

Register 18E1 makes it possible to read the contents of the CRC good counter for packets that are received on the Cu media interface; the number of CRC routines that have executed successfully. The following table shows the expected readouts.

Table 71 • **Cu Media CRC Good Counter, Address 18E1 (0x12)**

Bit	Name	Access	Description	Default
15	Packet since last read	RO	Self-clearing bit. 1: Packet received since last read.	0
14	Reserved	RO	Reserved.	
13:0	Cu Media CRC good counter contents	RO	Self-clearing bit. Counter containing the number of packets with valid CRCs modulo 10,000; this counter does not saturate and will roll over to zero on the next good packet received after 9,999.	0x000

4.3.3 Extended Mode Control

Register 19E1 controls the extended LED and other chip modes. The following table shows the settings available.

Table 72 • **Extended Mode Control, Address 19E1 (0x13)**

Bit	Name	Access	Description	Default
15	LED3 Extended Mode	R/W	1: See Extended LED Modes, page 64	0
14	LED2 Extended Mode	R/W	1: See Extended LED Modes, page 64	0
13	LED1 Extended Mode	R/W	1: See Extended LED Modes, page 64	0
12	LED0 Extended Mode	R/W	1: See Extended LED Modes, page 64	0
11	LED Reset Blink Suppress	R/W	1: Blink LEDs after COMA_MODE is de-asserted 0: Suppress LED blink after COMA_MODE is de-asserted	0
10:5	Reserved	RO	Reserved	0
4	Fast link failure	R/W	Enable fast link failure pin. This must be done from PHY0 only. 1: Enabled 0: Disabled (GPIO9 pin becomes general purpose I/O)	0
3:2	Force MDI crossover	R/W	00: Normal HP Auto-MDIX operation 01: Reserved 10: Copper media forced to MDI 11: Copper media forced MDI-X	00
1	Reserved	RO	Reserved	
0	GPIO[3:0]/SIGDET[3:0] pin polarity	R/W	SIGDET pin polarity 1: Active low 0: Active high	0

4.3.4 ActiPHY Control

Register 20E1 controls the device ActiPHY sleep timer, its wake-up timer, and its link speed downshifting feature. The following table shows the settings available.

Table 73 • **Extended PHY Control 3, Address 20E1 (0x14)**

Bit	Name	Access	Description	Default
15	Disable carrier extension	R/W	1: Disable carrier extension in 1000BASE-T copper links	1
14:13	ActiPHY sleep timer	R/W	Sticky bit. 00: 1 second 01: 2 seconds 10: 3 seconds 11: 4 seconds	01
12:11	ActiPHY wake-up timer	R/W	Sticky bit. 00: 160 ms 01: 400 ms 10: 800 ms 11: 2 seconds	00
10	Slow MDC	R/W	1: Indicates that MDC runs at less than 10 MHz (use of this bit is optional and indicated when MDC runs at less than 1 MHz)	0
9	PHY address reversal	R/W	Reverse PHY address Enabling causes physical PHY 0 to have address of 3, PHY 1 address of 2, PHY 2 address of 1, and PHY 3 address of 0. Changing this bit to 1 should initially be done from PHY 0 and changing to 0 from PHY3 1: Enabled 0: Disabled Valid only on PHY0	0
8	Reserved	RO	Reserved	
7:6	Media mode status	RO	00: No media selected 01: Copper media selected 10: SerDes media selected 11: Reserved	00
5	Enable 10BASE-T no preamble mode	R/W	Sticky bit. 1: 10BASE-T will assert RX_DV indication when data is presented to the receiver even without a preamble preceding it	0
4	Enable link speed autodownshift feature	R/W	Sticky bit. 1: Enable auto link speed downshift from 1000BASE-T	0

Table 73 • **Extended PHY Control 3, Address 20E1 (0x14) *(continued)***

Bit	Name	Access	Description	Default
3:2	Link speed auto downshift control	R/W	Sticky bit. 00: Downshift after 2 failed 1000BASE-T autonegotiation attempts 01: Downshift after 3 failed 1000BASE-T autonegotiation attempts 10: Downshift after 4 failed 1000BASE-T autonegotiation attempts 11: Downshift after 5 failed 1000BASE-T autonegotiation attempts	01
1	Link speed auto downshift status	RO	0: No downshift 1: Downshift is required or has occurred	0
0	Reserved	RO	Reserved	

4.3.5 PoE and Miscellaneous Functionality

The register at address 23E1 controls various aspects of inline powering and the CRC error counter in the VSC8564-11.

Table 74 • **Extended PHY Control 4, Address 23E1 (0x17)**

Bit	Name	Access	Description	Default
15:11	PHY address	RO	Internal PHY address. 00000: PHY 0 00001: PHY 1 00010: PHY 2 00011: PHY 3 others: Reserved	
10	Inline powered device detection	R/W	Sticky bit. 1: Enabled	0
9:8	Inline powered device detection status	RO	Only valid when bit 10 is set. 00: Searching for devices 01: Device found; requires inline power 10: Device found; does not require inline power 11: Reserved	00
7:0	Cu Media CRC error counter	RO	Self-clearing bit	

CRC error counter for packets received on the Cu media interface. The value saturates at 0xFF and subsequently clears when read and restarts count.0x00

4.3.6 Ethernet Packet Generator Control 1

The EPG control register provides access to and control of various aspects of the EPG testing feature. There are two separate EPG control registers. The following table shows the settings available in the first register.

Table 75 • **EPG Control Register 1, Address 29E1 (0x1D)**

Bit	Name	Access	Description	Default
15	EPG enable	R/W	1: Enable EPG	0
14	EPG run or stop	R/W	1: Run EPG	0

Table 75 • **EPG Control Register 1, Address 29E1 (0x1D)** ***(continued)***

Bit	Name	Access	Description	Default
13	Transmission duration	R/W	1: Continuous (sends in 10,000-packet increments) 0: Send 30,000,000 packets and stop	0
12:11	Packet length	R/W	00: 125 bytes 01: 64 bytes 10: 1518 bytes 11: 10,000 bytes (jumbo packet)	0
10	Interpacket gap	R/W	Bit times 1: 8,192 0: 96	0
9:6	Destination address	R/W	Lowest nibble of the 6-byte destination address	0001
5:2	Source address	R/W	Lowest nibble of the 6-byte source address	0000
1	Payload type	R/W	1: Randomly generated payload pattern 0: Fixed based on payload pattern	0
0	Bad frame check sequence (FCS) generation	R/W	1: Generate packets with bad FCS 0: Generate packets with good FCS	0

The following information applies to the EPG control number 1:

- Do not run the EPG when the VSC8564-11 is connected to a live network.
- bit 29E1.13 (continuous EPG mode control): When enabled, this mode causes the device to send continuous packets. When disabled, the device continues to send packets only until it reaches the next 10,000-packet increment mark. It then ceases to send packets.
- The 6-byte destination address in bits 9:6 is assigned one of 16 addresses in the range of 0xFF FF FF FF FF F0 through 0xFF FF FF FF FF FF.
- The 6-byte source address in bits 5:2 is assigned one of 16 addresses in the range of 0xFF FF FF FF FF F0 through 0xFF FF FF FF FF FF.
- If any of bits 13:0 are changed while the EPG is running (bit 14 is set to 1), bit 14 must be cleared and then set back to 1 for the change to take effect and to restart the EPG.

4.3.7 Ethernet Packet Generator Control 2

Register 30E1 consists of the second set of bits that provide access to and control over the various aspects of the EPG testing feature. The following table shows the settings available.

Table 76 • **EPG Control Register 2, Address 30E1 (0x1E)**

Bit	Name	Access	Description	Default
15:0	EPG packet payload	R/W	Data pattern repeated in the payload of packets generated by the EPG	0x00

Note: If any of bits 15:0 in this register are changed while the EPG is running (bit 14 of register 29E1 is set to 1), that bit (29E1.14) must first be cleared and then set back to 1 for the change to take effect and to restart the EPG.

4.4 Extended Page 2 Registers

To access the extended page 2 registers (16E2–30E2), enable extended register access by writing 0x0002 to register 31. For more information, see Table 68, page 97.

When extended page 2 register access is enabled, reads and writes to registers 16–30 affect the extended registers 16E2–30E2 instead of those same registers in the IEEE-specified register space. Registers 0–15 are not affected by the state of the extended page register access.

Writing 0x0000 to register 31 restores the main register access.

The following table lists the addresses and register names in the extended register page 2 space. These registers are accessible only when the device register 31 is set to 0x0002.

Table 77 • **Extended Registers Page 2 Space**

Address	Name
16E2	Cu PMD Transmit Control
17E2	EEE Control
18E2	Extended Chip ID
19E2	Entropy data
20E2-27E2	Reserved
28E2	Extended Interrupt Mask
29E2	Extended Interrupt Status
30E2	Ring Resiliency Control

4.4.1 Cu PMD Transmit Control

The register at address 16E2 consists of the bits that provide control over the amplitude settings for the transmit side Cu PMD interface. These bits provide the ability to make small adjustments in the signal amplitude to compensate for minor variations in the magnetics from different vendors. Extreme caution must be exercised when changing these settings from the default values as they have a direct impact on the signal quality. Changing these settings also affects the linearity and harmonic distortion of the transmitted signals. For help with changing these values, contact your Microsemi representative.

Table 78 • **Cu PMD Transmit Control, Address 16E2 (0x10)**

Bit	Name	Access	Description	Default
15:12	1000BASE-T signal amplitude trim[1]	R/W	1000BASE-T signal amplitude 1111: -1.7% 1110: -2.6% 1101: -3.5% 1100: -4.4% 1011: -5.3% 1010: -7% 1001: -8.8% 1000: -10.6% 0111: 5.5% 0110: 4.6% 0101: 3.7% 0100: 2.8% 0011: 1.9% 0010: 1% 0001: 0.1% 0000: -0.8%	0000

Table 78 • **Cu PMD Transmit Control, Address 16E2 (0x10)** ***(continued)***

Bit	Name	Access	Description	Default
11:8	100BASE-TX signal amplitude trim[2]	R/W	100BASE-TX signal amplitude 1111: -1.7% 1110: -2.6% 1101: -3.5% 1100: -4.4% 1011: -5.3% 1010: -7% 1001: -8.8% 1000: -10.6% 0111 5.5% 0110: 4.6% 0101: 3.7% 0100: 2.8% 0011: 1.9% 0010: 1% 0001: 0.1% 0000: -0.8%	0010
7:4	10BASE-T signal amplitude trim[3]	R/W	10BASE-T signal amplitude 1111: -7% 1110: -7.9% 1101: -8.8% 1100: -9.7% 1011: -10.6% 1010: -11.5% 1001: -12.4% 1000: -13.3% 0111: 0% 0110: -0.7% 0101: -1.6% 0100: -2.5% 0011: -3.4% 0010: -4.3% 0001: -5.2% 0000: -6.1%	1011
3:0	10BASE-Te signal amplitude trim	R/W	10BASE-Te signal amplitude 1111: -30.45% 1110: -31.1% 1101: -31.75% 1100: -32.4% 1011: -33.05% 1010: -33.7% 1001: -34.35% 1000: -35% 0111: -25.25% 0110: -25.9% 0101: -26.55% 0100: -27.2% 0011: -27.85% 0010: -28.5% 0001: -29.15% 0000: -29.8%	1110

1. Changes to 1000BASE-T amplitude may result in unpredictable side effects.
2. Adjust 100BASE-TX to specific magnetics.
3. Amplitude is limited by V_{CC} (2.5 V).

4.4.2 EEE Control

The register at address 17E2 consists of the bits that provide additional control over the chip behavior in energy efficient Ethernet (IEEE 802.3az-2010) mode for debug.

Table 79 • **EEE Control, Address 17E2 (0x11)**

Bit	Name	Access	Description	Default
15	Enable 10BASE-Te	R/W	Sticky bit. Enable energy efficient (IEEE 802.3az-2010) 10BASE-Te operating mode.	0
14	Enable LED in fiber unidirectional mode	R/W	Sticky bit. 1: Enable LED functions in fiber unidirectional mode.	0
13:10	Invert LED polarity	R/W	Sticky bit. Invert polarity of LED[3:0]_[3:0] signals. Default is to drive an active low signal on the LED pins. This also applies to enhanced serial LED mode. For more information, see Enhanced Serial LED Mode, page 65.	0000
9	Reserved	RO	Reserved.	
8	Link status	RO	1: Link is up.	0
7	1000BASE-T EEE enable	RO	1: EEE is enabled for 1000BASE-T.	0
6	100BASE-TX EEE enable	RO	1: EEE is enabled for 100BASE-TX.	0
5	Enable 1000BASE-T force mode	R/W	Sticky bit. 1: Enable 1000BASE-T force mode to allow PHY to link-up in 1000BASE-T mode without forcing master/slave when register 0, bits 6 and 13 are set to 2'b10.	0
4	Force transmit LPI[1]	R/W	Sticky bit. 1: Enable the EPG to transmit LPI on the MDI, ignore data from the MAC interface. 0: Transmit idles being received from the MAC.	0
3	Inhibit 100BASE-TX transmit EEE LPI	R/W	Sticky bit. 1: Disable transmission of EEE LPI on transmit path MDI in 100BASE-TX mode when receiving LPI from MAC.	0
2	Inhibit 100BASE-TX receive EEE LPI	R/W	Sticky bit. 1: Disable transmission of EEE LPI on receive path MAC interface in 100BASE-TX mode when receiving LPI from the MDI.	0
1	Inhibit 1000BASE-T transmit EEE LPI	R/W	Sticky bit. 1: Disable transmission of EEE LPI on transmit path MDI in 1000BASE-T mode when receiving LPI from MAC.	0
0	Inhibit 1000BASE-T receive EEE LPI	R/W	Sticky bit. 1: Disable transmission of EEE LPI on receive path MAC interface in 1000BASE-T mode when receiving LPI from the MDI.	0

1. Register 17E2 bits 4:0 are for debugging purposes only, not for operational use

4.4.3 Extended Chip ID, Address 18E2 (0x12)

The following table shows the register settings for the extended chip ID at address 18E2.

Table 80 • **Extended Chip ID, Address 18E2 (0x12)**

Bit	Name	Access	Description	Default
15	Industrial temperature capable	RO	VSC8564-11 1: Industrial temperature capable 0: Commercial temperature capable	0
15	Industrial temperature capable	RO	VSC8564-14 1: Industrial temperature capable 0: Commercial temperature capable	1
14	Quad/dual device	RO	1: Quad device 0: Dual device	1
13	Reserved	RO	Reserved	0
12	MACsec capable	RO	1: MACsec capable 0: Not MACsec capable	1
11	Reserved	RO	Reserved	0
10	Dual media device	RO	1: Dual media capable 0: Not dual media capable	1
9	Reserved	RO	Reserved	0
8	MACsec 256-bit keys capable	RO	1: MACsec 256-bit key capable 0: MACsec 128-bit key capable	1
7:0	Extended chip ID	RO	Dash number of VSC8564-11 in BCD	0x11
7:0	Extended chip ID	RO	Dash number of VSC8564-14 in BCD	0x14

4.4.4 Entropy Data, Address 19E2 (0x13)

The following table shows the register settings for the entropy data at address 19E2.

Table 81 • **Entropy Data, Address 19E2 (0x13)**

Bit	Name	Access	Description	Default
15:0	Entropy data	RO	Random data that can be added to an entropy pool	

4.4.5 Extended Interrupt Mask, Address 28E2 (0x1C)

The following table shows the register settings for the extended interrupt mask at address 28E2.

Table 82 • **Extended Interrupt Mask, Address 28E2 (0x1C)**

Bit	Name	Access	Description	Default
15:11	Reserved	R/W	Reserved.	00000
10	Mem integrity ring control interrupt mask	R/W	Sticky bit. 1: Enabled.	0
9	MACsec egress interrupt mask	R/W	Sticky bit. 1: Enabled.	0
8	MACsec ingress interrupt mask	R/W	Sticky bit. 1: Enabled.	0
7	MACsec flow control buffer interrupt mask	R/W	Sticky bit. 1: Enabled.	0
6	MACsec line MAC interrupt mask	R/W	Sticky bit. 1: Enabled.	0
5	MACsec host MAC interrupt mask	R/W	Sticky bit. 1: Enabled.	0

Table 82 • **Extended Interrupt Mask, Address 28E2 (0x1C) *(continued)***

Bit	Name	Access	Description	Default
4	RR switchover complete interrupt mask	R/W	Sticky bit. 1: Enabled.	0
3	EEE link fail interrupt mask	R/W	Sticky bit. 1: Enabled.	0
2	EEE Rx TQ timer interrupt mask	R/W	Sticky bit. 1: Enabled.	0
1	EEE wait quiet/Rx TS timer interrupt mask	R/W	Sticky bit. 1: Enabled.	0
0	EEE wake error interrupt mask	R/W	Sticky bit. 1: Enabled.	0

4.4.6 Extended Interrupt Status, Address 29E2 (0x1D)

The following table shows the register settings for the extended interrupt status at address 29E2.

Table 83 • **Extended Interrupt Status, Address 29E2 (0x1D)**

Bit	Name	Access	Description	Default
15:11	Reserved	RO	Reserved.	00000
10	Mem integrity ring control interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0
9	MACsec egress interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0
8	MACsec ingress interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0
7	MACsec flow control buffer interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0
6	MACsec line MAC interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0
5	MACsec host MAC interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0
4	RR switchover complete interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0
3	EEE link fail interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0
2	EEE Rx TQ timer interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0
1	EEE wait quiet/Rx TS timer interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0
0	EEE wake error interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0

4.4.7 Ring Resiliency Control (0x1E)

The following table shows the register settings for the ring resiliency controls at address 30E2.

Table 84 • **Ring Resiliency, Address 30E2 (0x1E)**

Bit	Name	Access	Description	Default
15	Ring resiliency startup enable (master TR enable)	R/W	Sticky	0

Table 84 • **Ring Resiliency, Address 30E2 (0x1E) *(continued)***

Bit	Name	Access	Description	Default
14	Advertise ring resiliency	R/W	Sticky	0
13	LP ring resiliency advertisement	RO		0
12	Force ring resiliency enable (override autoneg)	R/W	Sticky	0
11:6	Reserved	RO	Reserved	000000
5:4	Ring resiliency status	RO	Ring resiliency status 00: Timing slave[1] 10: Timing slave becoming master 11: Timing master[1] 01: Timing master becoming slave	00
3:1	Reserved	RO	Reserved	000
0	Start switchover (only when not in progress)	RWSC		0

1. Reflects autoneg master/slave at initial link-up.

4.5 Extended Page 3 Registers

To access the extended page 3 registers (16E3–30E3), enable extended register access by writing 0x0003 to register 31. For more information, see Table 68, page 97.

When extended page 3 register access is enabled, reads and writes to registers 16–30 affect the extended registers 16E3–30E3 instead of those same registers in the IEEE-specified register space. Registers 0–15 are not affected by the state of the extended page register access.

Writing 0x0000 to register 31 restores the main register access.

The following table lists the addresses and register names in the extended register page 3 space. These registers are accessible only when the device register 31 is set to 0x0003.

Table 85 • **Extended Registers Page 3 Space**

Address	Name
16E3	MAC SerDes PCS Control
17E3	MAC SerDes PCS Status
18E3	MAC SerDes Clause 37 Advertised Ability
19E3	MAC SerDes Clause 37 Link Partner Ability
20E3	MAC SerDes Status
21E3	Media/MAC SerDes Transmit Good Packet Counter
22E3	Media/MAC SerDes Transmit CRC Error Counter
23E3	Media SerDes PCS Control
24E3	Media SerDes PCS Status
25E3	Media SerDes Clause 37 Advertised Ability
26E3	Media SerDes Clause 37 Link Partner Ability
27E3	Media/MAC SerDes Receive SerDes status

Table 85 • **Extended Registers Page 3 Space *(continued)***

Address	Name
28E3	Media/MAC SerDes Receive CRC Good Counter
29E3	Media CRC Error Counter
30E3	Reserved

4.5.1 MAC SerDes PCS Control

The register at address 16E3 consists of the bits that provide access to and control over MAC SerDes PCS block. The following table shows the settings available.

Table 86 • **MAC SerDes PCS Control, Address 16E3 (0x10)**

Bit	Name	Access	Description	Default
15	MAC interface disable	R/W	Sticky bit. 1: 1000BASE-X MAC interface disable when media link down.	0
14	MAC interface restart	R/W	Sticky bit. 1: 1000BASE-X MAC interface restart on media link change.	0
13	MAC interface PD enable	R/W	Sticky bit. 1: MAC interface autonegotiation parallel detect enable.	0
12	MAC interface autonegotiation restart	R/W	Self-clearing bit. 1: Restart MAC interface autonegotiation.	0
11	Force advertised ability	R/W	1: Force 16-bit advertised ability from register 18E3.	0
10:9	SGMII input preamble for 100BASE-FX	R/W	This is a sticky bit. 00: No SGMII preamble required. 01: One-Byte SGMII preamble required. 10: Two-Byte SGMII preamble required. 11: Reserved.	00
8	SGMII output preamble	R/W	This is a sticky bit. 0: No SGMII preamble. 1: Two-Byte SGMII preamble.	1
7	MAC SerDes autonegotiation enable	R/W	This is a sticky bit. 1: MAC SerDes ANEG enable.	0
6	SerDes polarity at input of MAC	R/W	This is a sticky bit. 1: Invert polarity of signal received at input of MAC.	0
5	SerDes polarity at output of MAC	R/W	1: Invert polarity of signal at output of MAC.	0
4	Fast link status enable	R/W	1: Use fast link fail indication as link status indication to MAC SerDes. 0: Use normal link status indication to MAC SerDes.	0
3	Reserved	R/W	Reserved.	0

Table 86 • **MAC SerDes PCS Control, Address 16E3 (0x10) *(continued)***

Bit	Name	Access	Description	Default
2	Inhibit MAC odd-start delay	R/W	This is a sticky bit. 1: Inhibits delay of 1 byte when receive packet begins on an odd-byte boundary (causes the first 0x55 byte of preamble to be removed on odd-byte alignment) 0: Allows delay on odd-byte aligned packets preserving all preamble bytes but introducing a delay variation between naturally even-byte aligned and odd-byte aligned packets.	1
1:0	Reserved	RO	Reserved.	0

4.5.2 MAC SerDes PCS Status

The register at address 17E3 consists of the bits that provide status from the MAC SerDes PCS block. The following table shows the settings available.

Table 87 • **MAC SerDes PCS Status, Address 17E3 (0x11)**

Bit	Name	Access	Description
15	MAC sync status failed	RO	1: Sync status on MAC SerDes has failed since last read
14	MAC cgbad received	RO	1: an invalid code-group was received on the MAC SerDes since last read
13	Reserved	RO	Reserved
12	SGMII alignment error	RO	1: SGMII alignment error occurred
11	MAC interface LP autonegotiation restart	RO	1: MAC interface link partner autonegotiation restart request occurred
10	Reserved	RO	Reserved
9:8	MAC remote fault	RO	01, 10, and 11: Remote fault detected from MAC 00: No remote fault detected from MAC
7	Asymmetric pause advertisement	RO	1: Asymmetric pause advertised by MAC
6	Symmetric pause advertisement	RO	1: Symmetric pause advertised by MAC
5	Full duplex advertisement	RO	1: Full duplex advertised by MAC
4	Half duplex advertisement	RO	1: Half duplex advertised by MAC
3	MAC interface LP autonegotiation capable	RO	1: MAC interface link partner autonegotiation capable
2	MAC interface link status	RO	1: MAC interface link status connected
1	MAC interface autonegotiation complete	RO	1: MAC interface autonegotiation complete
0	MAC interface PCS signal detect	RO	1: MAC interface PCS signal detect present

4.5.3 MAC SerDes Clause 37 Advertised Ability

The register at address 18E3 consists of the bits that provide access to and control over MAC SerDes Clause 37 advertised ability. The following table shows the settings available.

Table 88 • **MAC SerDes Cl37 Advertised Ability, Address 18E3 (0x12)**

Bit	Name	Access	Description	Default
15:0	MAC SerDes advertised ability	R/W	Current configuration code word being advertised (this register is read/write if 16E3.11 = 1)[1]	0x0000

1. The read value for this register is N/A for protocol transfer mode when 16E3.11 is not set.

4.5.4 MAC SerDes Clause 37 Link Partner Ability

The register at address 19E3 consists of the bits that provide status of the MAC SerDes link partner's Clause 37 advertised ability. The following table shows the settings available.

Table 89 • **MAC SerDes Cl37 LP Ability, Address 19E3 (0x13)**

Bit	Name	Access	Description
15:0	MAC SerDes LP ability	RO	Last configuration code word received from link partner

4.5.5 MAC SerDes Status

The register at address 20E3 consists of the bits that provide access to MAC SerDes status. The following table shows the settings available.

Table 90 • **MAC SerDes Status, Address 20E3 (0x14)**

Bit	Name	Access	Description
15	Comma realigned	RO	Self-clearing bit. Sticky bit. 1: MAC SerDes receiver comma was realigned.
14	SerDes signal detect	RO	Self-clearing bit. Sticky bit. 1: SerDes signal detection occurred.
13	QSGMII sync status	RO	Only applies on PHY0
12	MAC comma detect	RO	Self-clearing bit. Sticky bit. 1: Comma detected, cleared when comma not detected, reset to 1 upon read.
11:8	MAC comma position	RO	MAC comma-alignment position from 0 to 9. These bits are N/A for QSGMII.
7:0	Reserved	RO	Reserved.

4.5.6 Media/MAC SerDes Transmit Good Packet Counter

The register at address 21E3 consists of the bits that provide status of the media and MAC SerDes transmit good packet counter. The following table shows the settings available.

Table 91 • **Media/MAC SerDes Tx Good Packet Counter, Address 21E3 (0x15)**

Bit	Name	Access	Description
15	Tx good packet counter active	RO	1: Transmit good packet counter active
14	Reserved	RO	Reserved
13:0	Tx good packet count	RO	Transmit good packet count modulo 10000

4.5.7 Media/MAC SerDes Transmit CRC Error Counter

The register at address 22E3 consists of the bits that provide status of the media and MAC SerDes transmit packet count that had a CRC error. The following table shows the settings available.

Table 92 • **Media/MAC SerDes Tx CRC Error Counter, Address 22E3 (0x16)**

Bit	Name	Access	Description
15:14	Tx counter select	R/W	Selects between fiber media and MAC SerDes transmit counters[1] 00: Selects fiber media SerDes transmit counters 01: Selects MAC SerDes transmit counters others: Reserved
13	Tx preamble fix	R/W	Removes extraneous byte of preamble for egress frames. Only removes one byte if there are more than eight bytes present in the preamble.
12:8	Reserved	RO	Reserved
7:0	Tx CRC packet count	RO	Transmit CRC packet count (saturates at 255)

1. The counters are only operational when the media link state is up, irrespective of selecting media SerDes or MAC SerDes.

4.5.8 Media SerDes PCS Control

The register at address 23E3 consists of the bits that provide access to and control over Media SerDes PCS control. The following table shows the settings available.

Table 93 • **Media SerDes PCS Control, Address 23E3 (0x17)**

Bit	Name	Access	Description	Default
15:14	Remote fault to media	RO	Remote fault indication sent to media in most recent clause 37 auto-negotiation exchange.	
13	Media interface autonegotiation parallel-detection[1]	R/W	Sticky bit. 1: SerDes media autonegotiation parallel detect enabled.	0
12	Disable carrier extension	R/W	Disable carrier extension in 1000BASE-X fiber links.	1
11	Force advertised ability	R/W	1: Force 16-bit advertised ability from register 25E3.15:0.	0
10:7	Reserved	RO	Reserved.	
6	Polarity reversal input	R/W	This is a sticky bit. Media SerDes polarity reversal input. 0: No polarity reversal (default). 1: Polarity reversed.	0
5	Polarity reversal output	R/W	This is a sticky bit. Media SerDes polarity reversal output. 0: No polarity reversal (default). 1: Polarity reversed.	0

Table 93 • **Media SerDes PCS Control, Address 23E3 (0x17) *(continued)***

Bit	Name	Access	Description	Default
4	Inhibit odd-start delay	R/W	This is a sticky bit. 1: Inhibits delay of one byte when transmit packet begins on an odd-byte boundary (causes the first 0x55 byte of preamble to be removed on odd-byte alignment). 0: Allows delay on odd-byte aligned packets preserving all preamble bytes but introducing a delay variation between naturally even-byte aligned and odd-byte aligned packets.	1
3	Reserved	RO	Reserved.	
2	100BASE-FX force HLS	R/W	1: Forces 100BASE-FX to transmit Halt Line State (HLS) continuously. 0: Normal 100BASE-FX transmit operation.	0
1	100BASE-FX force FEFI	R/W	1: Forces 100BASE-FX Far-End Fault Indication (FEFI) as specified by bit 0. 0: Normal automatic operation of FEFI in 100BASE-FX.	0
0	100BASE-FX FEFI force value	R/W	1: Forces FEFI on when bit 1 is asserted. 0: Suppresses FEFI when bit 1 is asserted.	0

1. Only applicable when clause 37 auto-negotiation is enabled. Enabling parallel detection along with clause 37 auto-negotiation functionality requires local PHY to advertise full-duplex operation.

4.5.9 Media SerDes PCS Status

The register at address 24E3 consists of the bits that provide status of the Media SerDes PCS block. The following table shows the settings available.

Table 94 • **Media SerDes PCS Status, Address 24E3 (0x18)**

Bit	Name	Access	Description
15	Sync status failed	RO	1: Sync status on fiber-media SerDes has failed since last read
14	cgbad received	RO	1: Invalid code-group was received on the fiber-media SerDes since last read
13	SerDes protocol transfer	RO	100 Mb or 100BASE-FX link status
12	SerDes protocol transfer	RO	10 Mb link status
11	Media interface link partner autonegotiation restart	RO	1: Media interface link partner autonegotiation restart request occurred
10	Reserved	RO	Reserved
9:8	Remote fault detected	RO	01, 10, 11: Remote fault detected from link partner

Table 94 • **Media SerDes PCS Status, Address 24E3 (0x18) *(continued)***

Bit	Name	Access	Description
7	Link partner asymmetric pause	RO	1: Asymmetric pause advertised by link partner
6	Link partner symmetric pause	RO	1: Symmetric pause advertised by link partner
5	Link partner full duplex advertisement	RO	1: Full duplex advertised by link partner
4	Link partner half duplex advertisement	RO	1: Half duplex advertised by link partner
3	Link partner autonegotiation capable	RO	1: Media interface link partner autonegotiation capable
2	Media interface link status	RO	1: Media interface link status
1	Media interface autonegotiation complete	RO	1: Media interface autonegotiation complete
0	Media interface signal detect	RO	1: Media interface signal detect

4.5.10 Media SerDes Clause 37 Advertised Ability

The register at address 25E3 consists of the bits that provide access to and control over Media SerDes Clause 37 advertised ability. The following table shows the settings available.

Table 95 • **Media SerDes Cl37 Advertised Ability, Address 25E3 (0x19)**

Bit	Name	Access	Description	Default
15:0	Media SerDes advertised ability	R/W	Current configuration code word being advertised. This register is read/write when 23E3.11 = 1.[1]	0x0000

1. The read value for this register is N/A for protocol transfer mode when 23E3.11 is not set.

4.5.11 Media SerDes Clause 37 Link Partner Ability

The register at address 26E3 consists of the bits that provide status of the media SerDes link partner's Clause 37 advertised ability. The following table shows the settings available.

Table 96 • **MAC SerDes Cl37 LP Ability, Address 26E3 (0x1A)**

Bit	Name	Access	Description
15:0	Media SerDes LP ability	RO	Last configuration code word received from link partner

4.5.12 Media SerDes Status

The register at address 27E3 consists of the bits that provide access to Media SerDes status. The following table shows the settings available.

Table 97 • **Media SerDes Status, Address 27E3 (0x1B)**

Bit	Name	Access	Description
15	K28.5 comma realignment	RO	Self-clearing bit. 1: K28.5 comma re-alignment has occurred.
14	Signal detect	RO	Self-clearing bit. Sticky bit. 1: SerDes media signal detect.

Table 97 • **Media SerDes Status, Address 27E3 (0x1B)** ***(continued)***

Bit	Name	Access	Description
13	100BASE-FX FEFI detect	RO	1: 100BASE-FX far-end fault detected from link partner since last read.
12	Comma detect	RO	Self-clearing bit. Sticky bit. 1: Comma detected, cleared when comma not detected, reset to 1 upon read.
11:8	Comma position	RO	Fiber media SerDes comma-alignment position from 0 to 9.
7	100BASE-FX HLS detected	RO	1: 100BASE-FX Halt Line-State (HLS) detected since last read.
6:0	Reserved	RO	Reserved.

4.5.13 Media/MAC SerDes Receive CRC Good Counter

Register 28E3 makes it possible to read the contents of the CRC good counter for packets that are received on the Fiber media and MAC interfaces; the number of packets that have been received successfully. The following table shows the expected readouts.

Table 98 • **Media/MAC SerDes Receive CRC Good Counter, Address 28E3 (0x1C)**

Bit	Name	Access	Description	Default
15	Packet since last read	RO	Self-clearing bit. 1: Packet received since last read.	0
14	Reserved	RO	Reserved.	
13:0	Media/MAC SerDes Receive CRC good counter contents	RO	Self-clearing bit. Counter containing the number of packets with valid CRCs. This counter does not saturate and will roll over to 0 when the count reaches 10,000 packets.	0x000

4.5.14 Media/MAC SerDes Receive CRC Error Counter

Register 29E3 makes it possible to read the contents of the CRC error counter for packets that are received on the Fiber media and MAC interfaces. The following table shows the expected readouts.

Table 99 • **Media/MAC SerDes Receive CRC Error Counter, Address 29E3 (0x1D)**

Bit	Name	Access	Description	Default
15:14	Rx counter select	RW	Selects between fiber media and MAC SerDes receive counters.[1] 00: Selects fiber media SerDes receive counters. 01: Selects MAC SerDes receive counters. others: Reserved.	
13:8	Reserved	RO	Reserved.	
7:0	Media/MAC Receive CRC error counter	RO	Self-clearing bit. CRC error counter for packets received on the Fiber media or MAC interfaces. The value saturates at 0xFF and subsequently clears when read and restarts count.	0x00

1. The counters are only operational when the media link state is up, irrespective of selecting media SerDes or MAC SerDes.

4.6 Extended Page 4 Registers

To access the extended page 4 registers (16E4–30E4), enable extended register access by writing 0x0004 to register 31. For more information, see Table 68, page 97.

When extended page 4 register access is enabled, reads and writes to registers 16–30 affect the extended registers 16E4–30E4 instead of those same registers in the IEEE-specified register space. Registers 0–15 are not affected by the state of the extended page register access.

Writing 0x0000 to register 31 restores the main register access.

The following table lists the addresses and register names in the extended register page 4 space. These registers are accessible only when the device register 31 is set to 0x0004.

Table 100 • **Extended Registers Page 4 Space**

Address	Name
16E4–20E4	CSR Access Controls and Status
22E4–25E4	Reserved

4.6.1 CSR Access Controls and Status

The following tables show the CSR ring access controls and status registers.

Table 101 • **CSR Buffer, Address 17E4**

Bit	Access	Description
15:0	RWSC	CSR Data_LSB[15:0]

Table 102 • **CSR Buffer, Address 18E4**

Bit	Access	Description
15:0	RWSC	CSR Data_MSB[31:16]

4.7 General Purpose Registers

Accessing the general purpose register space is similar to accessing the extended page registers. Set register 31 to 0x0010. This sets all 32 registers to the general purpose register space.

To restore main register page access, write 0x0000 to register 31.

This register space is global in nature to all four PHY's in the VSC8564-11 device.

The following table lists the addresses and register names in the general purpose register page space. These registers are accessible only when the device register 31 is set to 0x0010. All general purpose register bits are super-sticky.

Table 103 • **General Purpose Registers Page Space**

Address	Name
0G–12G	Reserved
13G	LED/SIGDET/GPIO Control
14G	GPIO Control 2
15G	GPIO Input
16G	GPIO Output
17G	GPIO Output Enable

Table 103 • **General Purpose Registers Page Space *(continued)***

Address	Name
18G	Micro Command
19G	MAC Mode and Fast Link Configuration
20G	Two-Wire Serial MUX Control 1
21G	Two-Wire Serial MUX Control 2
22G	Two-Wire Serial MUX Data Read/Write
23G	Recovered Clock 1 Control
24G	Recovered Clock 2 Control
25G	Enhanced LED Control
26G	Reserved
27G	Reserved
28G	Reserved
29G	Global Interrupt Status
30G	Reserved

4.7.1 Reserved General Purpose Address Space

The bits in registers 0G to 12G and 30G of the general purpose register space are reserved.

4.7.2 LED/SIGDET/GPIO Control

The LED control bits configure the LED[3:0]_[31:0] pins to function as either LED control pins for each PHY, or as general purpose I/O pins. The SIGDET control bits configure the GPIO[3:0]/SIGDET[3:0] pins to function either as signal detect pins for each fiber media port, or as GPIOs. The following table shows the values that can be written.

Table 104 • **LED/SIGDET/GPIO Control, Address 13G (0x0D)**

Bit	Name	Access	Description	Default
15:14	GPIO7/I2C_SCL_3	R/W	00: SCL for PHY3 01: Reserved 10: Reserved 11: Controlled by MII registers 15G to 17G	00
13:12	GPIO6/I2C_SCL_2	R/W	00: SCL for PHY2 01: Reserved 10: Reserved 11: Controlled by MII registers 15G to 17G	00
11:10	GPIO5/I2C_SCL_1	R/W	00: SCL for PHY1 01: Reserved 10: Reserved 11: Controlled by MII registers 15G to 17G	00
9:8	GPIO4/I2C_SCL_0	R/W	00: SCL for PHY0 01: Reserved 10: Reserved 11: Controlled by MII registers 15G to 17G	00
7:6	GPIO3/SIGDET3 control	R/W	00: SIGDET operation 01: Reserved 10: Reserved 11: Controlled by MII registers 15G to 17G	00

Table 104 • **LED/SIGDET/GPIO Control, Address 13G (0x0D)** ***(continued)***

Bit	Name	Access	Description	Default
5:4	GPIO2/SIGDET2 control	R/W	00: SIGDET operation 01: Reserved 10: Reserved 11: Controlled by MII registers 15G to 17G	00
3:2	GPIO1/SIGDET1 control	R/W	00: SIGDET operation 01: Reserved 10: Reserved 11: Controlled by MII registers 15G to 17G	00
1:0	GPIO0/SIGDET0 control	R/W	00: SIGDET operation 01: Reserved 10: Reserved 11: Controlled by MII registers 15G to 17G	00

4.7.3 GPIO Control 2

The GPIO control 2 register configures the functionality of the COMA_MODE pins, and provides control for possible GPIO pin options.

Table 105 • **GPIO Control 2, Address 14G (0x0E)**

Bit	Name	Access	Description	Default
15:14	GPIO12 and GPIO13	R/W	GPIO12 and GPIO13 control. 00: Reserved. 01: Reserved. 10: Reserved. 11: GPIO12/GPIO13 operation. Controlled by MII registers 15G to 17G.	
13	COMA_MODE output enable (active low)	R/W	1: COMA_MODE pin is an input. 0: COMA_MODE pin is an output.	1
12	COMA_MODE output data	R/W	Value to output on the COMA_MODE pin when it is configured as an output.	0
11	COMA_MODE input data	RO	Data read from the COMA_MODE pin.	
10	Tri-state enable for two-wire serial bus	R/W	1: Tri-states two-wire serial bus output signals instead of driving them high. This allows those signals to be pulled above VDD25 using an external pull-up resistor. 0: Drive two-wire serial bus output signals to high and low values as appropriate.	1
9	Tri-state enable for LEDs	R/W	1: Tri-state LED output signals instead of driving them high. This allows the signals to be pulled above V_{DDIO} using an external pull-up resistor. 0: Drive LED bus output signals to high and low values.	1
8	PPS 1-3 output enable	RW	PPS 1-3 output enable (must be 0 to allow SPI daisy-chain input).	0
7:6	GPIO11	R/W	GPIO11 control. 00: Reserved 01: Reserved 10: Reserved 11: Controlled by MII registers 15G to 17G	

Table 105 • **GPIO Control 2, Address 14G (0x0E)** ***(continued)***

Bit	Name	Access	Description	Default
5:4	GPIO10	R/W	GPIO10 control. 00: Reserved 01: Reserved 10: Reserved 11: Controlled by MII registers 15G to 17G	
3:2	GPIO9/FASTLINK_FAIL	R/W	GPIO9/FASTLINK_FAIL control. 00: FASTLINK_FAIL operation 01: Reserved 10: Reserved 11: Controlled by MII registers 15G to 17G	
1:0	GPIO8/I2C_SDA	R/W	GPIO8/I2C_SDA control. 00: I2C_SDA operation 01: Reserved 10: Reserved 11: Controlled by MII registers 15G to 17G	

4.7.4 GPIO Input

The input register contains information about the input to the device GPIO pins. Read from this register to access the data on the device GPIO pins. The following table shows the readout you can expect.

Table 106 • **GPIO Input, Address 15G (0x0F)**

Bit	Name	Access	Description	Default
15:14	Reserved	RO	Reserved	
13	GPIO13	R/W	GPIO13 input	0
12	GPIO12	R/W	GPIO12 input	0
11	GPIO11	R/W	GPIO11 input	0
10	GPIO10	R/W	GPIO10 input	0
9	GPIO9/FASTLINK_FAIL	R/W	GPIO9/FASTLINK_FAIL input	0
8	GPIO8/I2C_SDA	R/W	GPIO8/I2C_SDA input	0
7	GPIO7/I2C_SCL_3	R/W	GPIO7/I2C_SCL_3 input	0
6	GPIO6/I2C_SCL_2	R/W	GPIO6/I2C_SCL_2 input	0
5	GPIO5/I2C_SCL_1	R/W	GPIO5/I2C_SCL_1 input	0
4	GPIO4/I2C_SCL_0	R/W	GPIO4/I2C_SCL_0 input	0
3	GPIO3/SIGDET3	R/W	GPIO3/SIGDET3 input	0
2	GPIO2/SIGDET2	R/W	GPIO2/SIGDET2 input	0
1	GPIO1/SIGDET1	R/W	GPIO1/SIGDET1 input	0
0	GPIO0/SIGDET0	R/W	GPIO0/SIGDET0 input	0

4.7.5 GPIO Output

The output register allows you to access and control the output from the device GPIO pins. The following table shows the values you can write.

Table 107 • **GPIO Output, Address 16G (0x10)**

Bit	Name	Access	Description	Default
15:14	Reserved	RO	Reserved	
13	GPIO13	R/W	GPIO13 output	0
12	GPIO12	R/W	GPIO12 output	0
11	GPIO11	R/W	GPIO11 output	0
10	GPIO10	R/W	GPIO10 output	0
9	GPIO9/FASTLINK_FAIL	R/W	GPIO9/FASTLINK_FAIL output	0
8	GPIO8/I2C_SDA	R/W	GPIO8/I2C_SDA output	0
7	GPIO7/I2C_SCL_3	R/W	GPIO7/I2C_SCL_3 output	0
6	GPIO6/I2C_SCL_2	R/W	GPIO6/I2C_SCL_2 output	0
5	GPIO5/I2C_SCL_1	R/W	GPIO5/I2C_SCL_1 output	0
4	GPIO4/I2C_SCL_0	R/W	GPIO4/I2C_SCL_0 output	0
3	GPIO3/SIGDET3	R/W	GPIO3/SIGDET3 output	0
2	GPIO2/SIGDET2	R/W	GPIO2/SIGDET2 output	0
1	GPIO1/SIGDET1	R/W	GPIO1/SIGDET1 output	0
0	GPIO0/SIGDET0	R/W	GPIO0/SIGDET0 output	0

4.7.6 GPIO Pin Configuration

Register 17G in the GPIO register space controls whether a particular GPIO pin functions as an input or an output. The following table shows the settings available.

Table 108 • **GPIO Input/Output Configuration, Address 17G (0x11)**

Bit	Name	Access	Description	Default
15:14	Reserved	RO	Reserved	
13	GPIO13	R/W	GPIO13 output enable	0
12	GPIO12	R/W	GPIO12 output enable	0
11	GPIO11	R/W	GPIO11 output enable	0
10	GPIO10	R/W	GPIO10 output enable	0
9	GPIO9/FASTLINK_FAIL	R/W	GPIO9/FASTLINK_FAIL output enable	0
8	GPIO8/I2C_SDA	R/W	GPIO8/I2C_SDA output enable	0
7	GPIO7/I2C_SCL_3	R/W	GPIO7/I2C_SCL_3 output enable	0
6	GPIO6/I2C_SCL_2	R/W	GPIO6/I2C_SCL_2 output enable	0
5	GPIO5/I2C_SCL_1	R/W	GPIO5/I2C_SCL_1 output enable	0
4	GPIO4/I2C_SCL_0	R/W	GPIO4/I2C_SCL_0 output enable	0
3	GPIO3/SIGDET3	R/W	GPIO3/SIGDET3 output enable	0
2	GPIO2/SIGDET2	R/W	GPIO2/SIGDET2 output enable	0
1	GPIO1/SIGDET1	R/W	GPIO1/SIGDET1 output enable	0

Table 108 • **GPIO Input/Output Configuration, Address 17G (0x11) *(continued)***

Bit	Name	Access	Description	Default
0	GPIO0/SIGDET0	R/W	GPIO0/SIGDET0 output	0

4.7.7 Microprocessor Command

Register 18G is a command register. Bit 15 tells the internal processor to execute the command. When bit 15 is cleared the command has completed. Software needs to wait until bit 15 = 0 before proceeding with the next PHY register access. Bit 14 = 1 typically indicates an error condition where the squelch patch was not loaded. Use the following steps to execute the command:

1. Write desired command
2. Check bit 15 (move existing text)
3. Check bit 14 (if set, then error)

Commands may take up to 25 ms to complete before bit 15 changes to 0.

Note: All MAC interfaces must be the same — all QSGMII or SGMII.

Table 109 • **Microprocessor Command Register, Address 18G**

Command	Setting
Enable four MAC SGMII ports	0x80F0
Enable four MAC QSGMII ports	0x80E0
Enable four Media 1000BASE-X ports	0x8FC1[1]
Enable four Media 100BASE-FX ports	0x8FD1[2]

1. The “F” in the command has a bit representing each of the four PHYs. To exclude a PHY from the configuration, set its bit to 0. For example, the configuration of PHY 3 and PHY 2 to 1000BASE-X would be 1100 or a “C” and the command would be 0x8CC1.

4.7.8 MAC Configuration and Fast Link

Register 19G in the GPIO register space controls the MAC interface mode and the selection of the source PHY for the fast link failure indication. The following table shows the settings available for the GPIO9/FASTLINK-FAIL pin.

Table 110 • **MAC Configuration and Fast Link Register, Address 19G (0x13)**

Bit	Name	Access	Description	Default
15:14	MAC configuration	R/W	Select MAC interface mode 00: SGMII 01: QSGMII 10: Reserved 11: Reserved	00
13:4	Reserved	RO	Reserved	
3:0	Fast link failure port setting	R/W	Select fast link failure PHY source 0000: Port0 0001: Port1 0010: Port2 0011: Port3 1100–1111: Output disabled	0xF

4.7.9 Two-Wire Serial MUX Control 1

The following table shows the settings available to control the integrated two-wire serial MUX.

Table 111 • **Two-Wire Serial MUX Control 1, Address 20G (0x14)**

Bit	Name	Access	Description	Default
15:9	Two-wire serial device address	R/W	Top 7 bits of the 8-bit address sent out on the two wire serial stream. The bottom bit is the read/write signal, which is controlled by register 21G, bit 8. SFPs use 0xA0.	0xA0
8:6	Reserved	RO	Reserved.	
5:4	Two-wire serial SCL clock frequency	R/W	00: 50 kHz 01: 100 kHz 10: 400 kHz 11: 2 MHz	01
3	Two-wire serial MUX port 3 enable	R/W	1: Enabled. 0: Two-wire serial disabled. Becomes GPIO pin.	0
2	Two-wire serial MUX port 2 enable	R/W	1: Enabled. 0: Two-wire serial disabled. Becomes GPIO pin.	0
1	Two-wire serial MUX port 1 enable	R/W	1: Enabled. 0: Two-wire serial disabled. Becomes GPIO pin.	0
0	Two-wire serial MUX port 0 enable	R/W	1: Enabled. 0: Two-wire serial disabled. Two-wire serial MUX port 0 becomes GPIO pin if serial LED function is enabled, regardless of the settings of this bit.	0

4.7.10 Two-Wire Serial MUX Control 2

Register 21G is used to control the two-wire serial MUX for status and control of two-wire serial slave devices.

Table 112 • **Two-Wire Serial MUX Interface Status and Control, Address 21G (0x15)**

Bit	Name	Access	Description	Default
15	Two-wire serial MUX ready	RO	1: Two-wire serial MUX is ready for read or write	
14:12	Reserved	RO	Reserved	
11:10	PHY port Address	R/W	Specific PHY port being addressed.	00
9	Enable two-wire serial MUX access	R/W	Self-clearing bit. 1: Execute read or write through the two-wire serial MUX based on the settings of register bit 21G.8	0
8	Two-wire serial MUX read or write	R/W	1: Read from two-wire serial MUX 0: Write to two-wire serial MUX	1
7:0	Two-wire serial MUX address	R/W	Sets the address of the two-wire serial MUX used to direct read or write operations.	0x00

4.7.11 Two-Wire Serial MUX Data Read/Write

Register 22G in the extended register space enables access to the two-wire serial MUX.

Table 113 • **Two-Wire Serial MUX Data Read/Write, Address 22G (0x16)**

Bit	Name	Access	Description	Default
15:8	Two-wire serial MUX read data	RO	Eight-bit data read from two-wire serial MUX; requires setting both register 21G.9 and 21G.8 to 1.	
7:0	Two-wire serial MUX write data	R/W	Eight-bit data to be written to two-wire serial MUX.	0x00

4.7.12 Recovered Clock 1 Control

Register 23G in the extended register space controls the functionality of the recovered clock 1 output signal.

Table 114 • **Recovered Clock 1 Control, Address 23G (0x17)**

Bit	Name	Access	Description	Default
15	Enable RCVRDCLK1	R/W	1: Enable recovered clock 1 output 0: Disable recovered clock 1 output	0
14:11	Clock source select	R/W	Select bits for source PHY for recovered clock: 0000: PHY0 0001: PHY1 0010: PHY2 0011: PHY3 0100–1111: Reserved	0000
10:8	Clock frequency select	R/W	Select output clock frequency: 000: 25 MHz output clock 001: 125 MHz output clock 010: 31.25 MHz output clock 011–111: Reserved	000
7:6	Reserved	RO	Reserved.	

Table 114 • **Recovered Clock 1 Control, Address 23G (0x17) *(continued)***

Bit	Name	Access	Description	Default
5:4	Clock squelch level	R/W	Select clock squelch level 00: Automatically squelch clock to low when the link is not up, is unstable, is up in a mode that does not support the generation of a recovered clock (1000BASE-T master or 10BASE-T), or is up in EEE mode (100BASE-TX or 1000BASE-T slave). 01: Same as 00 except that the clock is also generated in 1000BASE-T master and 10BASE-T link-up modes. This mode also generates a recovered clock output in EEE mode during reception of LP_IDLE. 10: Squelch only when the link is not up. 11: Disable clock squelch. **Note:** A clock from the SerDes or Cu PHY will be output on the recovered clock output in this mode when the link is down. When the CLK_SQUELCH_IN pin is set high, it squelches the recovered clocks regardless of bit settings.	
3	Reserved	RO	Reserved.	
2:0	Clock selection for specified PHY	R/W	000: Serial media recovered clock 001: Copper PHY recovered clock 010: Copper PHY transmitter TCLK 011–111: Reserved	000

4.7.13 Recovered Clock 2 Control

Register 24G in the extended register space controls the functionality of the recovered clock 2 output signal.

Table 115 • **Recovered Clock 2 Control, Address 24G (0x18)**

Bit	Name	Access	Description	Default
15	Enable RCVRDCLK2	R/W	Enable recovered clock 2 output	0
14:11	Clock source select	R/W	Select bits for source PHY for recovered clock: 0000: PHY0 0001: PHY1 0010: PHY2 0011: PHY3 0100–1111: Reserved	0000
10:8	Clock frequency select	R/W	Select output clock frequency: 000: 25 MHz output clock 001: 125 MHz output clock 010: 31.25 MHz output clock 011–111: Reserved	000
7:6	Reserved	RO	Reserved	

Table 115 • **Recovered Clock 2 Control, Address 24G (0x18) *(continued)***

Bit	Name	Access	Description	Default
5:4	Clock squelch level	R/W	Select clock squelch level: 00: Automatically squelch clock to low when the link is not up, is unstable, is up in a mode that does not support the generation of a recovered clock (1000BASE-T master or 10BASE-T), or is up in EEE mode (100BASE-TX or 1000BASE-T slave). 01: Same as 00 except that the clock is also generated in 1000BASE-T master and 10BASE-T link-up modes. This mode also generates a recovered clock output in EEE mode during reception of LP_IDLE 10: Squelch only when the link is not up 11: Disable clock squelch. **Note:** A clock from the SerDes or Cu PHY will be output on the recovered clock output in this mode when the link is down. When the CLK_SQUELCH_IN pin is set high, it squelches the recovered clocks regardless of bit settings.	
3	Reserved	RO	Reserved	
2:0	Clock selection for specified PHY	R/W	000: Serial media recovered clock 001: Copper PHY recovered clock 010–111: Reserved	000

4.7.14 Enhanced LED Control

The following table contains the bits to control advanced functionality of the parallel and serial LED signals.

Table 116 • **Enhanced LED Control, Address 25G (0x19)**

Bit	Name	Access	Description	Default
15:8	LED pulsing duty cycle control	R/W	Programmable control for LED pulsing duty cycle when bit 30.12 is set to 1. Valid settings are between 0 and 198. A setting of 0 corresponds to a 0.5% duty cycle and 198 corresponds to a 99.5% duty cycle. Intermediate values change the duty cycle in 0.5% increments	00
7	Port 1 enhanced serial LED output enable	R/W	Enable the enhanced serial LED output functionality for port 1 LED pins. 1: Enhanced serial LED outputs 0: Normal function	0
6	Port 0 enhanced serial LED output enable	R/W	Enable the enhanced serial LED output functionality for port 0 LED pins. 1: Enhanced serial LED outputs 0: Normal function	0

Table 116 • **Enhanced LED Control, Address 25G (0x19) *(continued)***

Bit	Name	Access	Description	Default
5:3	Serial LED frame rate selection	R/W	Select frame rate of serial LED stream 000: 2500 Hz frame rate 001: 1000 Hz frame rate 010: 500 Hz frame rate 011: 250 Hz frame rate 100: 200 Hz frame rate 101: 125 Hz frame rate 110: 40 Hz frame rate 111: Output basic serial LED stream See Table 31, page 65.	
2:1	Serial LED select	R/W	Select which LEDs from each PHY to enable on the serial stream 00: Enable all four LEDs of each PHY 01: Enable LEDs 2, 1 and 0 of each PHY 10: Enable LEDs 1 and 0 of each PHY 11: Enable LED 0 of each PHY	00
0	LED port swapping	R/W	See LED Port Swapping, page 66.	

4.7.15 Global Interrupt Status

The following table contains the interrupt status from the various sources to indicate which one caused that last interrupt on the pin.

Table 117 • **Global Interrupt Status, Address 29G (0x1D)**

Bit	Name	Access	Description
15:12	Reserved	RO	Reserved
11:8	Reserved	RO	Reserved
7:4	Reserved	RO	Reserved
3	PHY3 interrupt source[2]	RO	PHY3 interrupt source indication 0: PHY3 caused the interrupt 1: PHY3 did not cause the interrupt
2	PHY2 interrupt source[2]	RO	PHY2 interrupt source indication 0: PHY2 caused the interrupt 1: PHY2 did not cause the interrupt
1	PHY1 interrupt source[1]	RO	PHY1 interrupt source indication 0: PHY1 caused the interrupt 1: PHY1 did not cause the interrupt
0	PHY0 interrupt source[2]	RO	PHY0 interrupt source indication 0: PHY0 caused the interrupt 1: PHY0 did not cause the interrupt

1. This bit is set to 1 when the corresponding PHY's Interrupt Status register 26 (0x1A) is read.

4.8 Clause 45 Registers to Support Energy Efficient Ethernet and 802.3bf

This section describes the Clause 45 registers that are required to support energy efficient Ethernet. Access to these registers is through the IEEE standard registers 13 and 14 (MMD access control and MMD data or address registers) as described in section 4.2.11 and 4.2.12.

The following table lists the addresses and register names in the Clause 45 register page space. When the link is down, 0 is the value returned for the x.180x addresses.

Table 118 • **Clause 45 Registers Page Space**

Address	Name
1.1	PMA/PMD status 1
1.1800	TimeSync PMA/PMD capability
1.1801	Tx maximum delay through PHY (PMA/PMD/PCS, until MACsec block)
1.1803	Tx minimum delay through PHY (PMA/PMD/PCS, until MACsec block)
1.1805	Rx maximum delay through PHY (PMA/PMD/PCS, until MACsec block)
1.1807	Rx minimum delay through PHY (PMA/PMD/PCS, until MACsec block)
3.1	PCS status 1
3.1800	TimeSync PCS capability
3.1801	Tx maximum delay through MACsec
3.1803	Tx minimum delay through MACsec
3.1805	Rx maximum delay t hrough MACsec
3.1807	Rx minimum delay through MACsec
3.20	EEE capability
3.22	EEE wake error counter
4.1800	TimeSync PHY XS Capability
4.1801	Tx maximum delay through xMII (SGMII, QSGMII, including FIFO variations)
4.1803	Tx minimum delay through xMII (SGMII, QSGMII, including FIFO variations)
4.1805	Rx maximum delay through xMII (SGMII, QSGMII, including FIFO variations)
4.1807	Rx minimum delay through xMII (SGMII, QSGMII, including FIFO variations)
7.60	EEE advertisement
7.61	EEE link partner advertisement

4.8.1 PMA/PMD Status 1

The following table shows the bit descriptions for the PMA/PMD Status 1 register.

Table 119 • **PMA/PMD Status 1**

Bit	Name	Access	Description
15:3	Reserved	RO	Reserved
2	PMD/PMA receive link status	RO/LL	1: PMA/PMD receive link up 0: PMA/PMD receive link down
1:0	Reserved	RO	Reserved

4.8.2 PCS Status 1

The bits in the PCS Status 1 register provide a status of the EEE operation from the PCS for the link that is currently active.

Table 120 • **PCS Status 1, Address 3.1**

Bit	Name	Access	Description
15:12	Reserved	RO	Reserved
11	Tx LPI received	RO/LH	1: Tx PCS has received LPI 0: LPI not received
10	Rx LPI received	RO/LH	1: Rx PCS has received LPI 0: LPI not received
9	Tx LPI indication	RO	1: Tx PCS is currently receiving LPI 0: PCS is not currently receiving LPI
8	Rx LPI indication	RO	1: Rx PCS is currently receiving LPI 0: PCS is not currently receiving LPI
7:3	Reserved	RO	Reserved
2	PCS receive link status	RO/LL	1: PCS receive link up 0: PCS receive link down
1:0	Reserved	RO	Reserved

4.8.3 EEE Capability

This register is used to indicate the capability of the PCS to support EEE functions for each PHY type. The following table shows the bit assignments for the EEE capability register.

Table 121 • **EEE Capability, Address 3.20**

Bit	Name	Access	Description
15:3	Reserved	RO	Reserved
2	1000BASE-T EEE	RO	1: EEE is supported for 1000BASE-T 0: EEE is not supported for 1000BASE-T
1	100BASE-TX EEE	RO	1: EEE is supported for 100BASE-TX 0: EEE is not supported for 100BASE-TX
0	Reserved	RO	Reserved

4.8.4 EEE Wake Error Counter

This register is used by PHY types that support EEE to count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type. The definition of the fault event to be counted is defined for each PHY and can occur during a refresh or a wakeup as defined by the PHY. This 16-bit counter is reset to all zeros when the EEE wake error counter is read or when the PHY undergoes hardware or software reset.

Table 122 • **EEE Wake Error Counter, Address 3.22**

Bit	Name	Access	Description
15:0	Wake error counter	RO	Count of wake time faults for a PHY

4.8.5 EEE Advertisement

This register defines the EEE advertisement that is sent in the unformatted next page following a EEE technology message code. The following table shows the bit assignments for the EEE advertisement register.

Table 123 • **EEE Advertisement, Address 7.60**

Bit	Name	Access	Description	Default
15:3	Reserved	RO	Reserved	
2	1000BASE-T EEE	R/W	1: Advertise that the 1000BASE-T has EEE capability 0: Do not advertise that the 1000BASE-T has EEE capability	0
1	100BASE-TX EEE	R/W	1: Advertise that the 100BASE-TX has EEE capability 0: Do not advertise that the 100BASE-TX has EEE capability	0
0	Reserved	RO	Reserved	

4.8.6 EEE Link Partner Advertisement

All the bits in the EEE LP Advertisement register are read only. A write to the EEE LP advertisement register has no effect. When the AN process has been completed, this register will reflect the contents of the link partner's EEE advertisement register. The following table shows the bit assignments for the EEE advertisement register.

Table 124 • **EEE Advertisement, Address 7.61**

Bit	Name	Access	Description
15:3	Reserved	RO	Reserved
2	1000BASE-T EEE	RO	1: Link partner is advertising EEE capability for 1000BASE-T 0: Link partner is not advertising EEE capability for 1000BASE-T
1	100BASE-TX EEE	RO	1: Link partner is advertising EEE capability for 100BASE-TX 0: Link partner is not advertising EEE capability for 100BASE-TX
0	Reserved	RO	Reserved

The following table shows the bit assignments for the 802.3bf registers. When the link is down, 0 is the value returned. Register 1.1801 would be device address of 1 and register address of 1801.

Table 125 • **802.3bf Registers**

Register	Name	Function
1.1800	PMA/PMD Time Sync capable	Bit 1: PMA/PMD Time Sync Tx capable Bit 0: PMA/PMD Time Sync Rx capable
1.1801	PMA/PMD delay Tx max	Tx maximum delay through PHY (PMA/PMD/PCS, until MACsec block)
1.1803	PMA/PMD delay Tx min	Tx minimum delay through PHY (PMA/PMD/PCS, until MACsec block
1.1805	PMA/PMD delay Rx max	Rx maximum delay through PHY (PMA/PMD/PCS, until MACsec block)

Table 125 • **802.3bf Registers *(continued)***

Register	Name	Function
1.1807	PMA/PMD delay Rx min	Rx minimum delay through PHY (PMA/PMD/PCS, until MACsec block)
3.1800	PCS Time Sync capable	Bit 1: PCS Time Sync Tx capable bit 0: PCS Time Sync Rx capable
3.1801	PCS delay Tx max low	Tx maximum delay through MACsec lower bits
3.1802	PCS delay Tx max high	Tx maximum delay through MACsec upper bits
3.1803	PCS delay Tx min low	Tx minimum delay through MACsec lower bits
3.1804	PCS delay Tx min high	Tx minimum delay through MACsec upper bits
3.1805	PCS delay Rx max low	Rx maximum delay through MACsec lower bits
3.1806	PCS delay Rx max high	Rx maximum delay through MACsec upper bits
3.1807	PCS delay Rx min low	Rx minimum delay through MACsec lower bits
3.1808	PCS delay Rx min high	Rx minimum delay through MACsec upper bits
4.1800	PHY XS Time Sync capable	Bit 1: PHY XS Time Sync Tx capable Bit 0: PHY XS Time Sync Rx capable
4.1801	PHY XS delay Tx max	Tx maximum delay through xMII (SGMII, QSGMII, including FIFO variations)
4.1803	PHY XS delay Tx min	Tx minimum delay through xMII (SGMII, QSGMII, including FIFO variations)
4.1805	PHY XS delay Rx max	Rx maximum delay through xMII (SGMII, QSGMII, including FIFO variations)
4.1807	PHY XS delay Rx min	Rx minimum delay through xMII (SGMII, QSGMII, including FIFO variations)

5 Electrical Specifications

This section provides the DC characteristics, AC characteristics, recommended operating conditions, and stress ratings for the VSC8564-11 device.

5.1 DC Characteristics

This section contains the DC specifications for the VSC8564-11 device.

5.1.1 VDD25 and VDDMDIO (2.5 V)

The following table shows the DC specifications for the pins referenced to V_{VDD25} and $V_{VDDMDIO}$ when it is set to 2.5 V. The specifications listed in the following table are valid only when V_{VDD1} = 1.0 V, V_{VDD1A} = 1.0 V, and V_{VDD25A} = 2.5 V.

Table 126 • **VDD25 and VDDMDIO**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage, LVTTL	V_{OH_TTL}	2.0	2.8	V	I_{OH} = –1 mA
Output high voltage, open drain	V_{OH_OD}	2.0	2.8	V	I_{OH} = –100 µA
Output low voltage	V_{OL}	–0.3	0.4	V	I_{OL} = 4 mA
Input high voltage	V_{IH}	1.85	3.3	V	Except SMI pins
Input high voltage	V_{IH}	1.88	3.3	V	SMI pins
Input low voltage	V_{IL}	–0.3	0.7	V	
Input leakage current	I_{ILEAK}	–32	32	µA	Internal resistor included (except GPIO, LED, and COMA_MODE)
Input leakage current	I_{ILEAK}	–76	32	µA	Internal resistor included (GPIO, LED, and COMA_MODE)
Output leakage current	I_{OLEAK}	–32	32	µA	Internal resistor included (except GPIO, LED, and COMA_MODE)
Output leakage current	I_{OLEAK}	–76	32	µA	Internal resistor included (GPIO, LED, and COMA_MODE)

5.1.2 VDDMDIO (1.2 V)

The following table shows the DC specifications for the pins referenced to $V_{VDDMDIO}$ when it is set to 1.2 V. The specifications listed in the following table are valid only when V_{VDD1} = 1.0 V, V_{VDD1A} = 1.0 V, V_{VDD25} = 2.5 V, V_{VDD25A} = 2.5 V, and $V_{VDDMDIO}$= 1.2 V.

Table 127 • **VDDMDIO**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage, open drain	V_{OH}	1.0	1.5	V	I_{OH} = –100 µA
Output low voltage, open drain	V_{OL}	–0.3	0.25	V	I_{OL} = 4 mA

Table 127 • **VDDMDIO *(continued)***

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Input high voltage	V_{IH}	0.9	1.5	V	
Input low voltage	V_{IL}	–0.3	0.36	V	
Input leakage current	I_{ILEAK}	–32	32	µA	Internal resistor included
Output leakage current	I_{OLEAK}	–32	32	µA	Internal resistor included

5.1.3 Supply Voltage

The following table shows the supply voltage specifications.

Table 128 • **Supply Voltage Specifications**

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Power supply voltage for digital logic	V_{DD1}	0.95	1	1.05	V
Power supply voltage for analog logic	V_{DD1A}	0.95	1	1.05	V
Power supply voltage for digital supply	V_{DD25}	2.375	2.5	2.625	V
Power supply voltage for analog supply	V_{DD25A}	2.375	2.5	2.625	V
1.2 V MDIO internal supply	V_{DDMDIO}	1.19	1.2	2.625	V
2.5 V MDIO internal supply	V_{DDMDIO}	1.19	2.5	2.625	V

5.1.4 LED and GPIO

The following table shows the DC specifications for the LED and GPIO pins.

Table 129 • **LED and GPIO**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage for LED pins, LVTTL	V_{OH}	1.7	2.8	V	V_{VDD25} = 2.5 V I_{OH} = –24 mA
Output low voltage for LED pins, LVTTL	V_{OL}	–0.3	0.6	V	V_{VDD25} = 2.5 V I_{OL} = 24 mA
Output high voltage for GPIO pins, LVTTL	V_{OH}	1.7	2.8	V	V_{VDD25} = 2.5 V I_{OH} = –12 mA
Output low voltage for GPIO pins, LVTTL	V_{OL}	–0.3	0.6	V	V_{VDD25} = 2.5 V I_{OL} = 12 mA

5.1.5 Internal Pull-Up or Pull-Down Resistors

Internal pull-up or pull-down resistors are specified in the following table. For more information about signals with internal pull-up or pull-down resistors, see Pins by Function, page 153.

All internal pull-up resistors are connected to their respective I/O supply.

Table 130 • **Internal Pull-Up or Pull-Down Resistors**

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Internal pull-up resistor (GPIO, LED, and COMA_MODE)	R_{PU1}	33	53	90	kΩ
Internal pull-up resistor, all others	R_{PU2}	96	120	144	kΩ
Internal pull-down resistor	R_{PD}	96	120	144	kΩ

5.1.6 Reference Clock

The following table shows the DC specifications for a differential reference clock input signal.

Table 131 • **Reference Clock DC Characteristics**

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Input voltage range	V_{IP},V_{IN}	–25		1260	mV
Input differential peak-to-peak voltage	$\|V_{ID}\|$	150(1)		1200	mV
Input common-mode voltage	V_{ICM}	0		1200(2)	mV
Differential input impedance	R_I		100		Ω

1. To meet jitter specifications, the minimum $|V_{ID}|$ must be 400 mV. When using a single-ended clock input, the REFCLK_P low voltage must be less than V_{DDA} – 200 mV, and the high voltage level must be greater than V_{DDA} + 200 mV.
2. The maximum common-mode voltage is provided without a differential signal. The common-mode voltage is only limited by the maximum and minimum input voltage range and by the differential amplitude of the input signal.

5.1.7 SerDes Interface (SGMII)

The SerDes output drivers are designed to operate in SGMII/LVDS mode. The SGMII/LVDS mode meets or exceeds the DC requirements of Serial-GMII Specification Revision 1.9 (ENG-46158), unless otherwise noted. The following table lists the DC specifications for the SGMII driver. The values are valid for all configurations, unless stated otherwise.

Table 132 • **SerDes Driver DC Specifications**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage, V_{OA} or V_{OB}	V_{OH}		1050	mV	R_L = 100 Ω ±1%
Output low voltage, V_{OA} or V_{OB}	V_{OL}	0		mV	R_L = 100 Ω ±1%
Output differential peak voltage	$\|V_{OD}\|$	350	450	mV	V_{DD_VS} = 1.0 V R_L = 100 Ω ±1%
Output differential peak voltage, fiber media 1000BASE-X	$\|V_{OD}\|$	350	450	mV	V_{DD_VS} = 1.0 V R_L = 100 Ω ±1%
Output offset voltage(1)	V_{OS}	420	580	mV	V_{DD_VS} = 1.0 V R_L = 100 Ω ±1%
DC output impedance, differential	R_O	80	140	Ω	V_C = 1.0 V See Figure 68, page 134
R_O mismatch between A and B, SGMII mode(2)	ΔR_O		10	%	V_C = 1.0 V See Figure 68, page 134
Change in $\|V_{OD}\|$ between 0 and 1, SGMII mode	$\Delta\|V_{OD}\|$		25	mV	R_L = 100 Ω ±1%
Change in V_{OS} between 0 and 1, SGMII mode	ΔV_{OS}		25	mV	R_L = 100 Ω ±1%
Output current, driver shorted to GND, SGMII mode	$\|I_{OSA}\|$, $\|I_{OSB}\|$		40	mA	
Output current, drivers shorted together, SGMII mode	$\|I_{OSAB}\|$		12	mA	

1. Requires AC-coupling for SGMII compliance.
2. Matching of reflection coefficients. For more information about test methods, see IEEE Std 1596.3-1996.

Figure 66 • **SGMII DC Transmit Test Circuit**

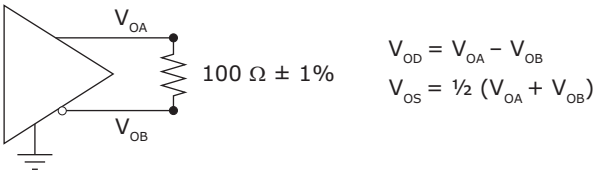
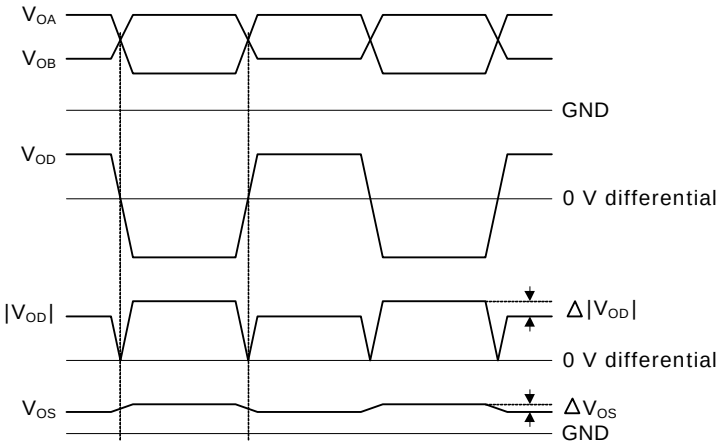


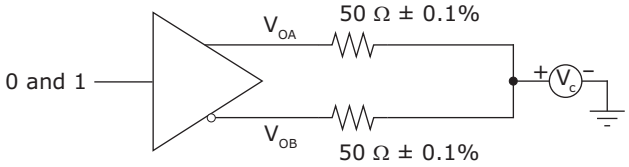
Figure 67 • **SGMII DC Definitions**



$$\Delta|V_{OD}| = | \, |V_{OAH} - V_{OBL}| - |V_{OBH} - V_{OAL}| \, |$$

$$\Delta V_{OS} = | \, ½(V_{OAH} + V_{OBL}) - ½(V_{OAL} + V_{OBH}) \, |$$

Figure 68 • **SGMII DC Driver Output Impedance Test Circuit**



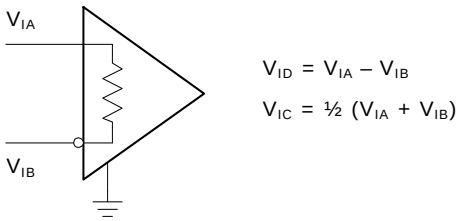
The following table lists the DC specifications for the SGMII receivers.

Table 133 • **SerDes Receiver DC Specifications**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Input voltage range, V_{IA} or V_{IB}	V_I	–25	1250	mV	
Input differential peak voltage	$\|V_{ID}\|$	50	1000	mV	
Input common-mode voltage(1)	V_{ICM}	0	V_{DD_A}(2)	mV	Without any differential signal
Receiver differential input impedance	R_I	80	120	Ω	
Input differential hysteresis, SGMII mode	V_{HYST}	25		mV	

1. SGMII compliancy requires external AC-coupling. When interfacing with specific Microsemi devices, DC-coupling is possible. For more information, contact your local Microsemi sales representative.
2. The common-mode voltage is only limited by the maximum and minimum input voltage range and the input signal's differential amplitude.

Figure 69 • **SGMII DC Input Definitions**



5.1.8 Enhanced SerDes Interface (QSGMII)

All DC specifications for the enhanced SerDes interface operating in QSGMII mode meet or exceed the requirements specified for CEI-6G-SR according to OIF-CEI-02.0 requirements where applicable.

The enhanced SerDes interface supports the following operating modes: SGMII, QSGMII, and SFP. The following table shows the DC specifications for the enhanced SerDes driver.

Table 134 • **Enhanced SerDes Driver DC Specifications**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Signaling speed	T_{BAUD}	5.0 – 100 ppm		5.0 + 100 ppm	Gbps	Signaling speed
Differential peak-to-peak output voltage	V_{OD}			30	mV	Tx disabled
Differential peak output voltage, SFP mode	$\|V_{ODp}\|$	250		400	mV	V_{DD_VS} = 1.0 V R_L = 100 Ω ±1% maximum drive
Differential peak output voltage, QSGMII mode	$\|V_{ODp}\|$	400		900	mV	
Differential peak output voltage, SGMII mode(1)	$\|V_{ODp}\|$	150		400	mV	V_{DD_VS} = 1.0 V R_L = 100 Ω ±1%
DC output impedance, differential	R_O	80	100	140	Ω	V_C = 1.0 V See Figure 68, page 134
R_O mismatch between A and B, SGMII mode(2)	ΔR_O			10	%	V_C = 1.0 V See Figure 68, page 134
Change in $\|V_{OD}\|$ between 0 and 1, SGMII mode	$\Delta\|V_{OD}\|$			25	mV	R_L = 100 Ω ±1%
Change in V_{OS} between 0 and 1, SGMII mode	$\Delta\|V_{OS}\|$			25	mV	R_L = 100 Ω ±1%
Output current, drivers shorted to ground, SGMII and QSGMII modes	$\|I_{OSA}\|$, $\|I_{OSB}\|$			40	mA	
Output current, drivers shorted together, SGMII and QSGMII modes	$\|I_{OSAB}\|$			12	mA	

1. Voltage is adjustable in 64 steps.
2. Matching of reflection coefficients. For more information about test methods, see IEEE Std 1596.3-1996.

The following table lists the DC specifications for the enhanced SerDes receiver.

Table 135 • **Enhanced SerDes Receiver DC Specifications**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Input voltage range, V_{IA} or V_{IB}	V_I	–0.25		1.20	V	
Input differential peak-to-peak voltage	$\|V_{ID}\|$	100		1600	mV	
Input common-mode voltage	V_{ICM}	VDDA – 100	VDDA	VDDA + 100	mV	Load-type 2 (DC-coupled)
Receiver differential input impedance	R_I	80	100	120	Ω	

5.1.9 Current Consumption

The following table shows the estimated current consumption values for each mode, assuming the MACsec functions are disabled. Add significant margin above the values for sizing power supplies. Add values from tables for the MACsec blocks to calculate total typical and maximum current for each power supply with those functions enabled.

Table 136 • **Current Consumption (MACsec Disabled)**

Mode	Typical				Maximum				Unit	Condition
	1 V Digital	1 V Analog	2.5 V Digital	2.5 V Analog	1 V Digital	1 V Analog	2.5 V Digital	2.5 V Analog		
Reset	105	130	9	2	910	190	11	4	mA	
Power down	175	200	9	21	1015	260	11	23	mA	
1000BASE-T	460	230	10	445	1890	270	15	500	mA	4-port SGMII
100BASE-TX	255	215	10	290	1525	245	15	310	mA	4-port SGMII
10BASE-T	200	210	10	230	1420	240	15	245	mA	4-port SGMII
10BASE-Te	200	210	10	215	1420	240	15	210	mA	4-port SGMII
1000BASE-X	225	275	10	21	1430	300	15	25	mA	4-port SGMII
100BASE-FX	200	270	10	21	1400	290	15	25	mA	4-port SGMII
1000BASE-T	450	185	10	445	1885	225	15	515	mA	4-port QSGMII
100BASE-TX	250	165	9	290	1520	200	15	325	mA	4-port QSGMII
10BASE-T	200	165	10	230	1415	195	15	260	mA	4-port QSGMII
10BASE-Te	195	165	10	215	1415	195	15	225	mA	4-port QSGMII
1000BASE-X	225	230	11	21	1425	255	15	40	mA	4-port QSGMII
100BASE-FX	200	225	10	22	1395	245	15	40	mA	4-port QSGMII

The following table shows the MACsec current consumption values .

Table 137 • **MACsec Current Consumption**

Mode	1 V Digital	Unit	Condition
1000BASE-T	160	mA	4-port SGMII/QSGMII
100BASE-TX	120	mA	4-port SGMII/QSGMII
10BASE-T	120	mA	4-port SGMII/QSGMII

Table 137 • **MACsec Current Consumption *(continued)***

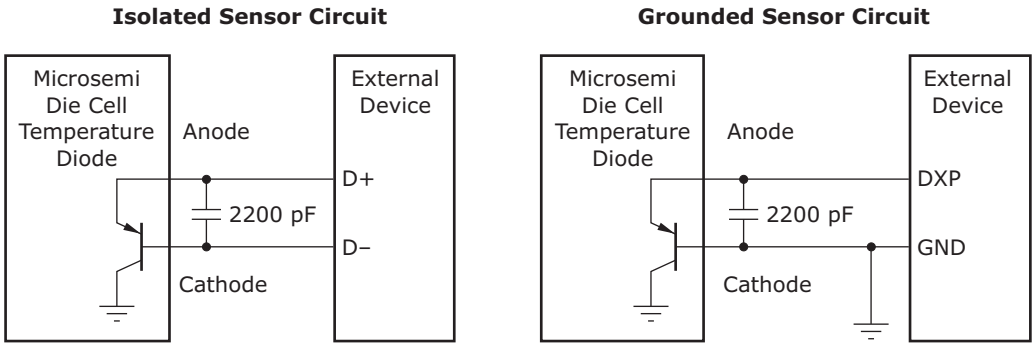
Mode	1 V Digital	Unit	Condition
10BASE-Te	120	mA	4-port SGMII/QSGMII
1000BASE-X	160	mA	4-port SGMII/QSGMII
100BASE-FX	120	mA	4-port SGMII/QSGMII

5.1.10 Thermal Diode

The VSC8564-11 device includes an on-die diode and internal circuitry for monitoring die temperature (junction temperature). The operation and accuracy of the diode is not guaranteed and should only be used as a reference.

The on-die thermal diode requires an external thermal sensor, located on the board or in a stand-alone measurement kit. Temperature measurement using a thermal diode is very sensitive to noise. The following illustration shows a generic application design.

Figure 70 • **Thermal Diode**



Note: Microsemi does not support or recommend operation of the thermal diode under reverse bias.

The following table provides the diode parameter and interface specifications with the pins connected internally to VSS in the device.

Table 138 • **Thermal Diode Parameters**

Parameter	Symbol	Typical	Maximum	Unit
Forward bias current	I_{FW}	See note[1]	1	mA
Diode ideality factor	n	1.008		

1. Typical value is device dependent.

The ideality factor, n, represents the deviation from ideal diode behavior as exemplified by the diode equation.

$$:I_{FW} = I_S \times \left(e^{V_d \times \frac{q}{nkT}} - 1 \right)$$

where, Is = saturation current, q = electron charge, Vd = voltage across the diode, k = Boltzmann Constant, and T = absolute temperature (Kelvin).

5.2 AC Characteristics

This section provides the AC specifications for the VSC8564-11 device.

5.2.1 Reference Clock

The following table shows the AC specifications for a 125 MHz differential reference clock source. Performance is guaranteed for 125 MHz differential clocks only; however, 125 MHz single-ended clocks are also supported for QSGMII interfaces.

25 MHz clock implementations are available but are limited to SGMII interfaces. For more information, contact your Microsemi representative.

Table 139 • **Reference Clock AC Characteristics for QSGMII 125 MHz Differential Clock**

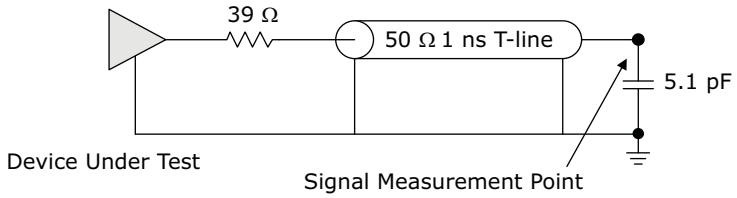
Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Reference clock frequency, REFCLK_SEL2 = 1	f		125.00		MHz	±100 ppm Jitter < 1 ps RMS
Duty cycle	DC	40	50	60	%	
Rise time and fall time	t_R, t_F			1.5	ns	20% to 80% threshold
RefClk input RMS jitter requirement, bandwidth between 12 kHz and 500 kHz(1)				20	ps	Meets jitter generation of 1G output data per IEEE 802.3z
RefClk input RMS jitter requirement, bandwidth between 500 kHz and 15 MHz(1)				4	ps	Meets jitter generation of 1G output data per IEEE 802.3z
RefClk input RMS jitter requirement, bandwidth between 15 MHz and 40 MHz(1)				20	ps	Meets jitter generation of 1G output data per IEEE 802.3z
RefClk input RMS jitter requirement, bandwidth between 40 MHz and 80 MHz(1)				100	ps	Meets jitter generation of 1G output data per IEEE 802.3z
Jitter gain from RefClk to SerDes output, bandwidth between 0.1 MHz and 0.1 MHz				0.3	dB	
Jitter gain from RefClk to SerDes output, bandwidth between 0.1 MHz and 7 MHz			1	3	dB	
Jitter gain from RefClk to SerDes output, bandwidth above 7 MHz		1–20 × log (f/7 MHz)		3–20 × log (f/7 MHz)	dB	

1. Maximum RMS sinusoidal jitter allowed at the RefClk input when swept through the given bandwidth.

5.2.2 Recovered Clock

This section provides the AC characteristics for the recovered clock output signals. The following illustration shows the test circuit for the recovered clock output signals.

Figure 71 • **Test Circuit for Recovered Clock Output Signals**



The following table shows the AC specifications for the RCVRDCLK1 and RCVRDCLK2 outputs.

Table 140 • **Recovered Clock AC Characteristics**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Recovered clock frequency	*f*		125.00		MHz	
Recovered clock frequency	*f*		31.25		MHz	
Recovered clock frequency	*f*		25.00		MHz	
Recovered clock cycle time	t_{RCYC}		8.0		ns	
Recovered clock cycle time	t_{RCYC}		32.0		ns	
Recovered clock cycle time	t_{RCYC}		40.0		ns	
Duty cycle	DC	45	50	55	%	
Clock rise time and fall time	t_R, t_F			1.0	ns	20% to 80%
Peak-to-peak jitter, copper media interface, 1000BASE-T slave mode	JPP_{CLK_Cu}			400	ps	10k samples
Peak-to-peak jitter, fiber media interface, 100BASE-FX	JPP_{CLK_FiFX}			1.2	ns	10k samples
Peak-to-peak jitter, fiber media interface, 1000BASE-X	JPP_{CLK_FiX}			200	ps	10k samples

5.2.3 SerDes Outputs

The values listed in the following table are valid for all configurations, unless otherwise noted.

Table 141 • **SerDes Outputs AC Specifications**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
V_{OD} ringing compared to V_S, SGMII mode	V_{RING}		±10	%	RL = 100 Ω ±1%
V_{OD} rise time and fall time, SGMII mode	t_R, t_F	100	200	ps	20% to 80% of V_S RL = 100 Ω ±1%
Differential peak-to-peak output voltage	V_{OD}		30	mV	Tx disabled

Table 141 • SerDes Outputs AC Specifications *(continued)*

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Differential output return loss, 50 MHz to 625 MHz	R_{LO_DIFF}	≥10		dB	RL = 100 Ω ±1%
Differential output return loss, 625 MHz to 1250 MHz	R_{LO_DIFF}	10–10 × log (*f*/625 MHz)		dB	RL = 100 Ω ±1%
Common-mode return loss, 50 MHz to 625 MHz	RL_{OCM}	6		dB	
Interpair skew, SGMII mode	t_{SKEW}		20	ps	

5.2.4 SerDes Driver Jitter

The following table lists the jitter characteristics for the SerDes output driver.

Table 142 • SerDes Driver Jitter Characteristics

Parameter	Symbol	Maximum	Unit	Condition
Total jitter	TJ_O	192	ps	Measured according to IEEE 802.3.38.5
Deterministic jitter	DJ_O	80	ps	Measured according to IEEE 802.3.38.5

5.2.5 SerDes Inputs

The following table lists the AC specifications for the SerDes inputs.

Table 143 • SerDes Input AC Specifications

Parameter	Maximum	Unit	Condition
Differential input return loss, 50 MHz to 625 MHz	≥10	dB	RL = 100 Ω ±1%
Differential input return loss, 625 MHz to 1250 MHz	10–10 × log (*f*/625 MHz)	dB	RL = 100 Ω ±1%

5.2.6 SerDes Receiver Jitter Tolerance

The following table lists jitter tolerances for the SerDes receiver.

Table 144 • SerDes Receiver Jitter Tolerance

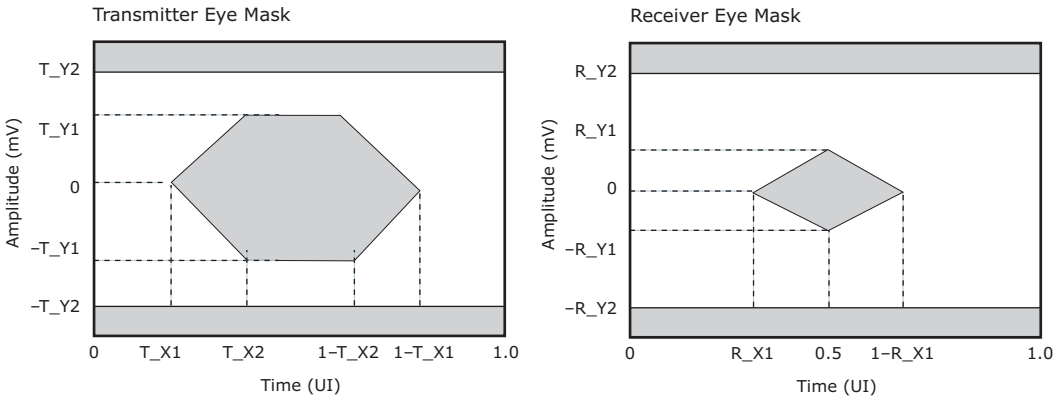
Parameter	Symbol	Minimum	Unit	Condition
Total jitter tolerance, greater than 637 kHz, SFP mode	TJT_I	600	ps	Measured according to IEEE 802.3 38.6.8
Deterministic jitter tolerance, greater than 637 kHz, SFP mode	DJT_I	370	ps	Measured according to IEEE 802.3 38.6.8
Cycle distortion jitter tolerance, 100BASE-FX mode	JT_{CD}	1.4	ns	Measured according to ISO/IEC 9314-3:1990
Data-dependent jitter tolerance, 100BASE-FX mode	DDJ	2.2	ns	Measured according to ISO/IEC 9314-3:1990
Random peak-to-peak jitter tolerance, 100BASE-FX mode	RJT	2.27	ns	Measured according to ISO/IEC 9314-3:1990

5.2.7 Enhanced SerDes Interface

All AC specifications for the enhanced SerDes interface are compliant with QSGMII Specification Revision 1.3 and meet or exceed the requirements in the standard. They are also compliant with the OIF-CEI-02.0 requirements where applicable.

The enhanced SerDes interface supports the following modes of operation: SGMII, QSGMII, and SFP. The values in the tables in the following sections apply to the QSGMII modes listed in the condition column and are based on the test circuit shown in Figure 66, page 134. The transmit and receive eye specifications relate to the eye diagrams shown in the following illustration, with the compliance load as defined in the test circuit.

Figure 72 • **QSGMII Transient Parameters**



5.2.7.1 Enhanced SerDes Outputs

The following table provides the AC specifications for the enhanced SerDes outputs in SGMII mode.

Table 145 • **Enhanced SerDes Outputs AC Specifications, SGMII Mode**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Unit interval, 1.25G mode	UI				800 ps
V_{OD} ringing compared to V_S	V_{RING}		±10	%	R_L = 100 Ω ±1%
V_{OD} rise time and fall time	t_R, t_F	100	200	ps	20% to 80% of V_S R_L = 100 Ω ±1%
Differential output return loss, 50 MHz to 625 MHz	RL_{O_DIFF}	≥10		dB	R_L = 100 Ω ±1%
Differential output return loss, 625 MHz to 1250 MHz	RL_{O_DIFF}	10–10 × log (*f*/625 MHz)		dB	R_L = 100 Ω ±1%
Common-mode return loss, 50 MHz to 625 MHz	RL_{OCM}	6		dB	
Intrapair skew	t_{SKEW}		20	ps	

The enhanced SerDes transmitter operating in QSGMII mode complies with the AC characteristics specified for CEI-6G-SR interfaces according to OIF-CEI-02.0 with some modifications as specified by Cisco's QSGMII specification.

Table 146 • **Enhanced SerDes Outputs AC Specifications, QSGMII Mode**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Signaling speed	T_{BAUD}	5.0 – 100 ppm	5.0 + 100 ppm	Gbps	

Table 146 • Enhanced SerDes Outputs AC Specifications, QSGMII Mode *(continued)*

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Differential output return loss	RLO_{SDD22}	8		dB	100 MHz to 2.5 GHz R_L = 100 Ω ± 1%
Differential output return loss	RLO_{SDD22}	8-16.6 x log(f/2.5)		dB	2.5 GHz to 5 GHz R_L = 100 Ω ± 1%
Common-mode output return loss	RLO_{CM}	6		dB	100 MHz to 2.5 GHz R_L = 100 Ω ± 1%
Transition time	t_{TR}, t_{TF}	30		ps	20% to 80%
Random jitter	RJ		0.15	UI_{P-P}	
Deterministic jitter	DJ		0.15	UI_{P-P}	Measured according to OIF-CEI-02.0/CEI-6G-SR.
Duty cycle of distortion (part of DJ)	DCD		0.05	UI_{P-P}	
Total jitter	TJ		0.30	UI_{P-P}	Measured according to OIF-CEI-02.0/CEI-6G-SR.
Eye mask X1	X1		0.15	UI_{P-P}	Near-end
Eye mask X2	X2		0.40	UI_{P-P}	Near-end
Eye mask Y1	Y1	200		mV	Near-end
Eye mask Y2	Y2		450	mV	Near-end

5.2.7.2 Enhanced SerDes Inputs

The enhanced SerDes operating in QSGMII mode complies to the AC characteristics as specified for CEI-6G-SR interfaces according to OIF-CEI-02.0 with some modifications as specified by Cisco's QSGMII specification. The following table lists the AC specifications for the enhanced SerDes inputs in SGMII mode.

Table 147 • Enhanced SerDes Input AC Specifications, SGMII Mode

Parameter	Symbol	Minimum	Unit	Condition
Unit interval, 1.25G	UI		ps	800 ps
Differential input return loss, 50 MHz to 625 MHz	RL_{I_DIFF}	10	dB	R_L = 100 Ω ±1%
Common-mode input return loss, 50 MHz to 625 MHz	RL_{ICM}	6	dB	

5.2.7.3 Enhanced SerDes Inputs

The following table lists the AC specifications for the enhanced SerDes inputs in QSGMII mode.

Table 148 • Enhanced SerDes Inputs AC Specifications, QSGMII Mode

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Signaling speed	T_{BAUD}	5.0 – 100 ppm	5.0 + 100 ppm	Gbps	
Differential input return loss	RLI_{SDD11}	8		dB	100 MHz to 2.5 GHz
Differential input return loss	RLI_{SDD11}	8-16.6 x log(f/2.5)		dB	2.5 GHz to 5 GHz
Common-mode input return loss	RL_{SCC11}	6		dB	100 MHz to 2.5 GHz

Table 148 • **Enhanced SerDes Inputs AC Specifications, QSGMII Mode**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Bounded high-probability jitter	RBHPJ		0.45	UI_{P-P}	Uncorrelated bounded high-probability jitter (0.15 UI) + correlated bounded high-probability jitter (0.3 UI)
Sinusoidal jitter max	SJ_{MAX}		5	UI_{P-P}	
Sinusoidal jitter, HF	SJ_{HF}		0.05	UI_{P-P}	
Total jitter	TJ		0.60	UI_{P-P}	Does not include sinusoidal jitter, link operates at BER of 10^{-15}
Eye mask X1	R_X1		0.30	UI_{P-P}	
Eye mask Y1	R_Y1		50	mV	
Eye mask Y2	R_Y2		450	mV	

5.2.7.4 Enhanced SerDes Receiver Jitter Tolerance

The following table lists the jitter tolerance for the enhanced SerDes receiver in QSGMII mode.

Table 149 • **Enhanced SerDes Receiver Jitter Tolerance**

Parameter	Symbol	Minimum	Unit	Condition
Total jitter tolerance, greater than 637 kHz, SFP mode	TJT_I	600	ps	Measured according to IEEE 802.3 38.6.8
Deterministic jitter tolerance, greater than 637 kHz, SFP mode	DJT_I	370	ps	Measured according to IEEE 802.3 38.6.8
Cycle distortion jitter tolerance, 100BASE-FX mode	JT_{CD}	1.4	ns	Measured according to ISO/IEC 9314-3:1990
Data-dependent jitter tolerance, 100BASE-FX mode	DDJ	2.2	ns	Measured according to ISO/IEC 9314-3:1990
Random peak-to-peak jitter tolerance, 100BASE-FX mode	RJT	2.27	ns	Measured according to ISO/IEC 9314-3:1990

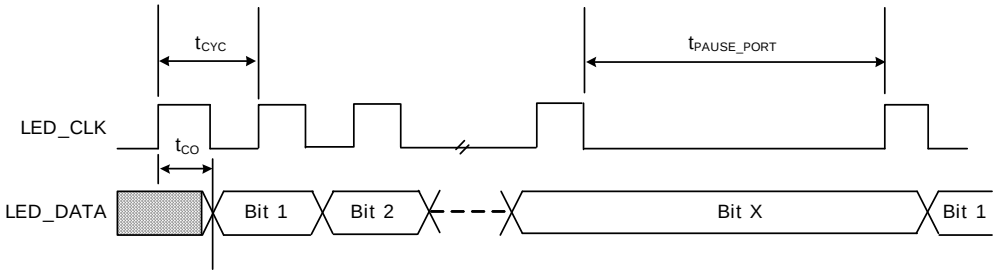
5.2.8 Basic Serial LEDs

This section contains the AC specifications for the basic serial LEDs.

Table 150 • **Basic Serial LEDs AC Characteristics**

Parameter	Symbol	Typical	Unit
LED_CLK cycle time	t_{CYC}	1024	ns
Pause between LED port sequences	t_{PAUSE_PORT}	3072	ns
Pause between LED bit sequences	t_{PAUSE_BIT}	25.541632	ms
LED_CLK to LED_DATA	t_{CO}	1	ns

Figure 73 • **Basic Serial LED Timing**



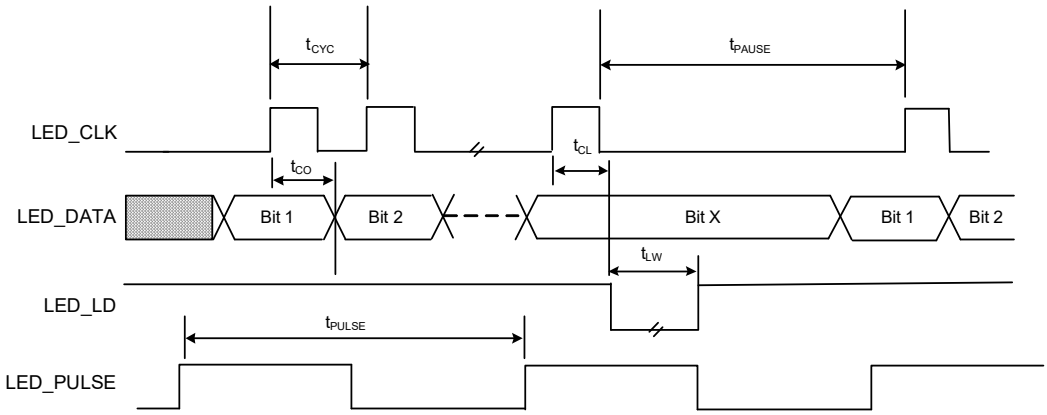
5.2.9 Enhanced Serial LEDs

This section contains the AC specifications for the enhanced serial LEDs. The duty cycle of the LED_PULSE signal is programmable and can be varied between 0.5% and 99.5%.

Table 151 • **Enhanced Serial LEDs AC Characteristics**

Parameter	Symbol	Minimum	Typical	Maximum	Unit
LED_CLK cycle time	t_{CYC}		256		ns
Pause between LED_DATA bit sequences	t_{PAUSE}	0.396		24.996	ms
LED_CLK to LED_DATA	t_{CO}		127		ns
LED_CLK to LED_LD	t_{CL}		256		ns
LED_LD pulse width	t_{LW}		128		ns
LED_PULSE cycle time	t_{PULSE}	199		201	µs

Figure 74 • **Enhanced Serial LED Timing**



5.2.10 Serial CPU Interface (SI) for Slave Mode

All serial CPU interface (SI) slave mode timing requirements are specified relative to the input low and input high threshold levels. The following illustrations show the timing parameters and measurement points for SI input and output data.

Figure 75 • **SI Input Data Timing Diagram for Slave Mode**

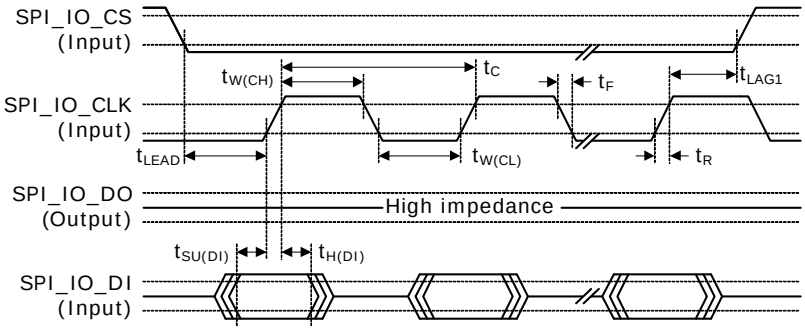
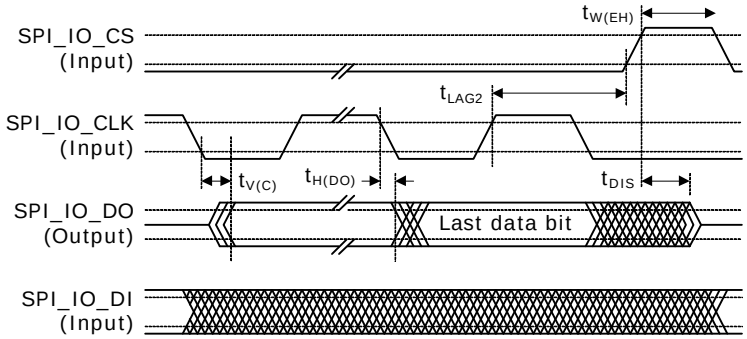


Figure 76 • **SI Output Data Timing Diagram for Slave Mode**



All SI signals comply with the specifications shown in the following table. The SI input timing requirements are requested at the pins of the device.

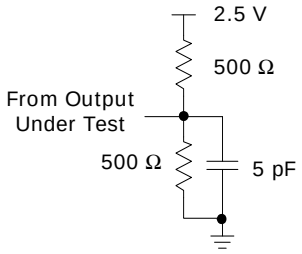
Table 152 • **SI Timing Specifications for Slave Mode**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Clock frequency	f		25	MHz	
Clock cycle time	t_C	40		ns	
Clock time high	$t_{W(CH)}$	16		ns	
Clock time low	$t_{W(CL)}$	16		ns	
Clock rise time and fall time	t_R, t_F		10	ns	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$
DI setup time to clock	$t_{SU(DI)}$	4		ns	
DI hold time from clock	$t_{H(DI)}$	4		ns	
Enable active before first clock	t_{LEAD}	10		ns	
Enable inactive after clock (input cycle)[1]	t_{LAG1}	25		ns	
Enable inactive after clock (output cycle)	t_{LAG2}	See note(2)		ns	
Enable inactive width	$t_{W(EH)}$	20		ns	
DO valid after clock	$t_{V(C)}$		20	ns	C_L = 30 pF
DO hold time from clock	$t_{H(DO)}$	0		ns	C_L = 0 pF
DO disable time[3]	t_{DIS}		15	ns	See the following illustration

1. t_{LAG1} is defined only for write operations to the device, not for read operations.
2. The last rising edge on the clock is necessary for the external master to read in the data. The lag time depends on the necessary hold time on the external master data input.
3. Pin begins to float when a 300 mV change from the loaded V_{OH} or V_{OL} level occurs.

The following illustration shows the test circuit for the SI_DO disable time.

Figure 77 • **Test Circuit for SI_DO Disable**



5.2.11 JTAG Interface

This section provides the AC specifications for the JTAG interface. The specifications meet or exceed the requirements of IEEE 1149.1-2001. The JTAG receive signal requirements are requested at the pin of the device. The JTAG_TRST signal is asynchronous to the clock, and does not have a setup or hold time requirement.

Table 153 • **JTAG Interface AC Specifications**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
TCK frequency	f		10	MHz	
TCK cycle time	t_C	100		ns	
TCK high time	$t_{W(CH)}$	40		ns	
TCK low time	$t_{W(CL)}$	40		ns	
Setup time to TCK rising	t_{SU}	10		ns	
Hold time from TCK rising	t_H	10		ns	
TDO valid after TCK falling	$t_{V(C)}$		28	ns	C_L = 10 pF
TDO hold time from TCK falling	$t_{H(TDO)}$	0		ns	C_L = 0 pF
TDO disable time(1)	t_{DIS}		30	ns	
TRST time low	$t_{W(TL)}$	30		ns	

1. The pin begins to float when a 300 mV change from the actual V_{OH}/V_{OL} level occurs.

Figure 78 • **JTAG Interface Timing Diagram**

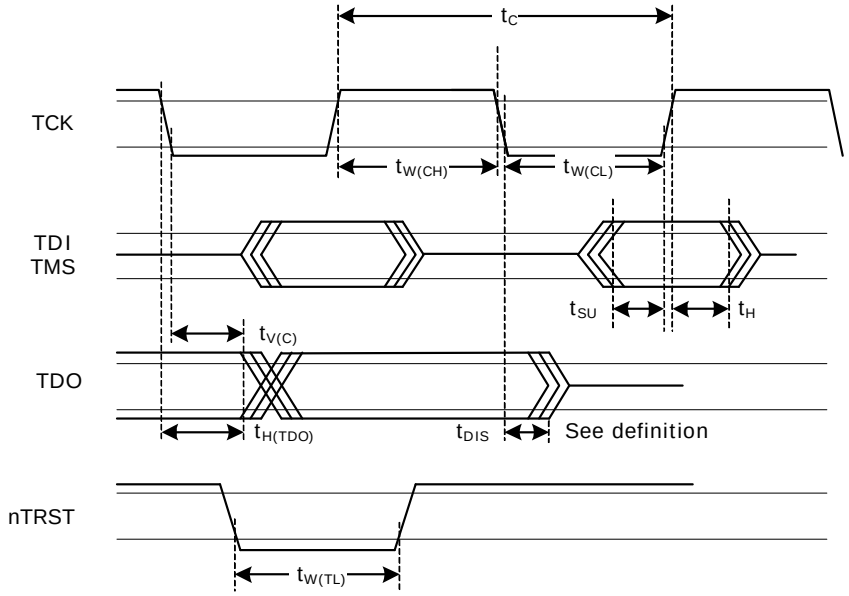
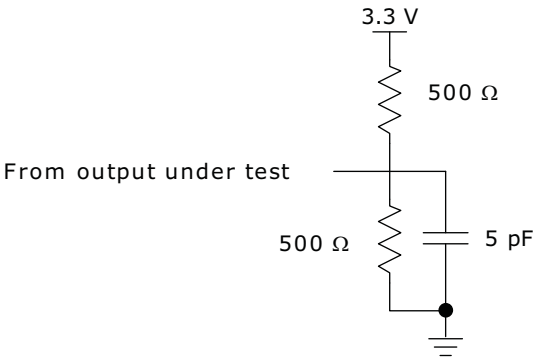


Figure 79 • **Test Circuit for TDO Disable Time**



5.2.12 Serial Management Interface

This section contains the AC specifications for the serial management interface (SMI).

Table 154 • **Serial Management Interface AC Characteristics**

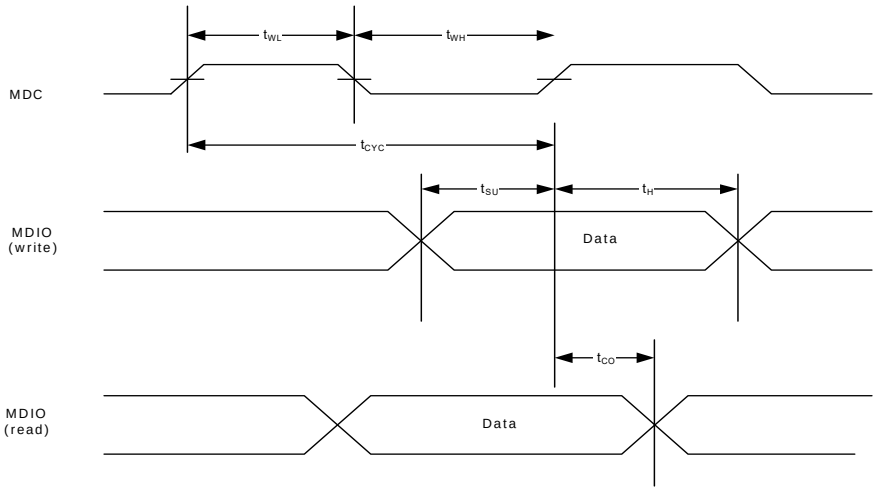
Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
MDC frequency(1)	f_{CLK}		2.5	12.5	MHz	
MDC cycle time	t_{CYC}	80	400		ns	
MDC time high	t_{WH}	20	50		ns	
MDC time low	t_{WL}	20	50		ns	
Setup to MDC rising	t_{SU}	10			ns	
Hold from MDC rising	t_H	10			ns	

Table 154 • **Serial Management Interface AC Characteristics *(continued)***

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
MDC rise time	t_R			100 t_{CYC} × 10%(1)	ns	MDC = 0: 1 MHz MDC = 1: MHz – f_{CLK} maximum
MDC fall time	t_F			100 t_{CYC} × 10%(1)	ns	
MDC to MDIO valid	t_{CO}		10	300	ns	Time-dependent on the value of the external pull-up resistor on the MDIO pin

1. For f_{CLK} above 1 MHz, the minimum rise time and fall time is in relation to the frequency of the MDC clock period. For example, if f_{CLK} is 2 MHz, the minimum clock rise time and fall time is 50 ns.

Figure 80 • **Serial Management Interface Timing**



5.2.13 Reset Timing

This section contains the AC specifications that apply to device reset functionality. The signal applied to the NRESET input must comply with the specifications listed in the following table.

Table 155 • **Reset Timing Specifications**

Parameter	Symbol	Minimum	Maximum	Unit
NRESET assertion time after power supplies and clock stabilize	t_W	2		ms
Recovery time from reset inactive to device fully active	t_{REC}		105	ms
NRESET pulse width	$t_{W(RL)}$	100		ns
Wait time between NRESET de-assert and access of the SMI interface	t_{WAIT}	105		ms

The following table shows the PHY latency in MACsec bypass mode, measured between the media interface and SGMII MAC interface pins.

Table 156 • **PHY Latency in SGMII Mode**

Mode	Transmit (egress) ns			Receive (ingress) ns			
	Minimum	Typical	Maximum	Minimum	Typical	Maximum	Unit
1000BASE-T	212 – 16	212	212 + 16	321 – 16	321	321 + 16	ns
100BASE-TX	581 – 80	581	581 + 80	485 – 40	485	485 + 40	ns
10BASE-T	4075 – 400	4075	4075 + 400	3375 – 200	3375	3375 + 200	ns
1000BASE-X	210 – 16	210	210 + 16	192 – 16	192	192 + 16	ns
100BASE-FX	531 – 40	531	531 + 40	430 – 16	430	430 + 16	ns

5.3 Operating Conditions

The following table shows the recommended operating conditions for the device.

Table 157 • **Recommended Operating Conditions**

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Power supply voltage for core supply	V_{VDD1}	0.95	1.00	1.05	V
Power supply voltage for analog circuits	V_{VDD1A}	0.95	1.00	1.05	V
Power supply voltage for digital I/O	V_{VDD25}	2.38	2.50	2.62	V
Power supply voltage for analog circuits	V_{VDD25A}	2.38	2.50	2.62	V
2.5 V Power supply voltage for SMI	V_{VDD_MDIO}	2.38	2.50	2.62	V
1.2 V Power supply voltage for SMI	V_{VDD_MDIO}	1.14	1.2	1.26	V
VSC8564-11 operating temperature(1)	T	0		125	°C
VSC8564-14 operating temperature(1)	T	–40		125	°C

1. Minimum specification is ambient temperature, and the maximum is junction temperature. For carrier class applications, the maximum operating temperature is 110 °C junction.

5.4 Stress Ratings

This section contains the stress ratings for the VSC8564-11 device.

Warning Stresses listed in the following table may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Table 158 • **Stress Ratings**

Parameter	Symbol	Minimum	Maximum	Unit
Power supply voltage for core supply	V_{VDD1}	–0.3	1.10	V
Power supply voltage for analog circuits	V_{VDD1A}	–0.3	1.10	V
Power supply voltage for analog circuits	V_{VDD25A}	–0.3	2.75	V
Power supply voltage for digital I/O	V_{VDD25}	–0.3	2.75	V
Power supply voltage for SMI	V_{VDD_MDIO}	–0.3	2.75	V
Input voltage for GPIO and logic input pins			3.3	V
Storage temperature	T_S	–55	125	°C

Table 158 • **Stress Ratings *(continued)***

Parameter	Symbol	Minimum	Maximum	Unit
Electrostatic discharge voltage, charged device model	V_{ESD_CDM}	–250	250	V
Electrostatic discharge voltage, human body model, VDD_MDIO pin	V_{ESD_HBM}	–1000	1000	V
Electrostatic discharge voltage, human body model, all pins except the VDD_MDIO pin	V_{ESD_HBM}	See note(1)		V

1. This device has completed all required testing as specified in the JEDEC standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*, and complies with a Class 2 rating. The definition of Class 2 is any part that passes an ESD pulse of 2000 V, but fails an ESD pulse of 4000 V.

Warning This device can be damaged by electrostatic discharge (ESD) voltage. Microsemi recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

6 Pin Descriptions

The device has 256 pins, which are described in this section.

The pin information is also provided as an attached Microsoft Excel file so that you can copy it electronically. In Acrobat, double-click the attachment icon.

6.1 Pin Identifications

This section contains the pin descriptions for the device. The following table provides notations for definitions of the various pin types.

Table 159 • **Pin Type Symbol Definitions**

Symbol	Pin Type	Description
3V	Power	3.3 V-tolerant pin.
ABIAS	Analog bias	Analog bias pin.
ADIFF	Analog differential	Analog differential signal pair.
I	Input	Input without on-chip pull-up or pull-down resistor.
I/O	Bidirectional	Bidirectional input or output signal.
NC	No connect	No connect pins must be left floating.
O	Output	Output signal.
OD	Open drain	Open drain output.
OS	Open source	Open source output.
PD	Pull-down	On-chip pull-down resistor to VSS.
PU	Pull-up	On-chip pull-up resistor.
ST	Schmitt-trigger	Input has Schmitt-trigger circuitry.

6.2 Pin Diagram

The following illustration shows the pin diagram for the device. For clarity, the device is shown in two halves, the top left and top right.

Figure 81 • **Top-Left Pin Diagram**

	1	2	3	4	5	6	7	8
A	NC_1	TXVPA_3	TXVPB_3	TXVPC_3	TXVPD_3	TXVPA_2	TXVPB_2	TXVPC_2
B	VSS_1	TXVNA_3	TXVNB_3	TXVNC_3	TXVND_3	TXVNA_2	TXVNB_2	TXVNC_2
C	REFCLK_N	VDD25A_1	THERMDA	VDD25A_2	VSS_3	VDD25A_3	VDD1A_1	VDD1A_2
D	REFCLK_P	THERMDC_VSS	REF_FILT_A	REF_REXT_A	VSS_6	VSS_7	VSS_8	VSS_9
E	REFCLK_SEL2	TMS	TRST	VDD25A_6	VDD1_1	VSS_14	VSS_15	VSS_16
F	TDO	TDI	TCK	VSS_20	VDD1_3	VSS_21	VSS_22	VSS_23
G	LED0_PHY0	LED1_PHY0	LED2_PHY0	LED3_PHY0	VDD1_5	VSS_27	VSS_28	VSS_29
H	LED0_PHY1	LED1_PHY1	LED2_PHY1	LED3_PHY1	VDD1_7	VSS_33	VSS_34	VSS_35
J	LED0_PHY2	LED1_PHY2	LED2_PHY2	LED3_PHY2	VDD1_9	VSS_39	VSS_40	VSS_41
K	LED0_PHY3	LED1_PHY3	LED2_PHY3	LED3_PHY3	VDD1_11	VSS_45	VSS_46	VSS_47
L	RESERVED_5	RESERVED_73	COMA_MODE	RESERVED_3	VDD1_13	VSS_51	VSS_52	VSS_53
M	RESERVED_6	MDINT	NRESET	VDD25_2	VDD1_15	VSS_57	VSS_58	VSS_59
N	RESERVED_7	MDIO	RESERVED_71	RESERVED_72	VDD1_17	VSS_63	VSS_64	VSS_65
P	RESERVED_8	MDC	VDD_MDIO	RESERVED_4	VDD25A_8	VDD1A_5	VDD1A_6	VDD1A_7
R	VSS	FIBROP_3	FIBRIP_3	RDP_3	TDP_3	FIBROP_2	FIBRIP_2	RDP_2
T	NC_3	FIBRON_3	FIBRIN_3	RDN_3	TDN_3	FIBRON_2	FIBRIN_2	RDN_2

Figure 82 • **Top-Right Pin Diagram**

9	10	11	12	13	14	15	16	
TXVPD_2	TXVPA_1	TXVPB_1	TXVPC_1	TXVPD_1	TXVPA_0	TXVPB_0	NC_2	A
TXVND_2	TXVNA_1	TXVNB_1	TXVNC_1	TXVND_1	TXVNA_0	TXVNB_0	VSS_2	B
VDD1A_3	RESERVED_1	VDD25A_4	VSS_4	VDD1A_4	VDD25A_5	TXVNC_0	TXVPC_0	C
VSS_10	VSS_11	VSS_12	VSS_13	RESERVED_2	VSS	TXVND_0	TXVPD_0	D
VSS_17	VSS_18	VSS_19	VDD1_2	VDD25A_7	RESERVED_74	CLK_SQUELCH_IN	GPIO14	E
VSS_24	VSS_25	VSS_26	VDD1_4	PHYADD1	PHYADD4	SPI_IO_DO	RCVRDCLK1	F
VSS_30	VSS_31	VSS_32	VDD1_6	PHYADD2	PHYADD3	SPI_IO_DI	RCVRDCLK2	G
VSS_36	VSS_37	VSS_38	VDD1_8	VDD25_1	GPIO13	SPI_IO_CLK	VSS	H
VSS_42	VSS_43	VSS_44	VDD1_10	SPI_IO_CS	GPIO12	RESERVED_18	RESERVED_19	J
VSS_48	VSS_49	VSS_50	VDD1_12	GPIO8/I2C_SDA	GPIO9/FASTLINK-FAIL	GPIO10	GPIO11	K
VSS_54	VSS_55	VSS_56	VDD1_14	GPIO4/I2C_SCL_0	GPIO5/I2C_SCL_1	GPIO6/I2C_SCL_2	GPIO7/I2C_SCL_3	L
VSS_60	VSS_61	VSS_62	VDD1_16	VDD25_3	SIGDET1/GPIO1	SIGDET2/GPIO2	SIGDET3/GPIO3	M
VSS_66	VSS_67	VSS_68	VDD1_18	SerDes_Rext_1	SIGDET0/GPIO0	TDP_0	TDN_0	N
VDD1A_8	VDD1A_9	VDD1A_10	VDD25A_9	VDD25A_10	SerDes_Rext_0	RDP_0	RDN_0	P
TDP_2	FIBROP_1	FIBRIP_1	RDP_1	TDP_1	FIBROP_0	FIBRIP_0	VSS_70	R
TDN_2	FIBRON_1	FIBRIN_1	RDN_1	TDN_1	FIBRON_0	FIBRIN_0	NC_4	T

6.3 Pins by Function

This section contains the functional pin descriptions for the device.

6.3.1 GPIO

The following table lists the General Purpose Input/Output (GPIO) pins.

Table 160 • **GPIO Pins**

Name	Pin	Type	Description
GPIO10	K15	I/O, PU, 3 V	Can be configured to serve as general purpose input/output (GPIO).
GPIO11	K16	I/O, PU, 3 V	Can be configured to serve as general purpose input/output (GPIO)
GPIO12	J14	I/O, PU, 3 V	Can be configured to serve as general purpose input/output (GPIO)
GPIO13	H14	I/O, PU, 3 V	Can be configured to serve as general purpose input/output (GPIO)
GPIO14	E16	I/O, PU, 3 V	Can be configured to serve as general purpose input/output (GPIO)

6.3.2 GPIO and Two-Wire Serial

The following table lists the GPIO and two-wire serial pins.

Table 161 • **GPIO and Two-Wire Serial Pins**

Name	Pin	Type	Description
GPIO4/I2C_SCL_0	L13	I/O, PU, 3 V	General purpose input/output (GPIO). The two-wire serial controller pins can be configured to serve as GPIOs.
GPIO5/I2C_SCL_1	L14	I/O, PU, 3 V	General purpose input/output (GPIO). The two-wire serial controller pins can be configured to serve as GPIOs.
GPIO6/I2C_SCL_2	L15	I/O, PU, 3 V	General purpose input/output (GPIO). The two-wire serial controller pins can be configured to serve as GPIOs.
GPIO7/I2C_SCL_3	L16	I/O, PU, 3 V	General purpose input/output (GPIO). The two-wire serial controller pins can be configured to serve as GPIOs.
GPIO8/I2C_SDA	K13	I/O, PU, 3 V	General purpose input/output (GPIO). The two-wire serial controller pins can be configured to serve as GPIOs.
GPIO9/FASTLINK-FAIL	K14	I/O, PU, 3 V	General purpose input/output (GPIO). The two-wire serial controller and fast link fail pins can be configured to serve as GPIOs.

6.3.3 JTAG

The following table lists the JTAG test pins.

Table 162 • **JTAG Pins**

Name	Pin	Type	Description
TCK	F3	I, PU, ST, 3 V	JTAG test clock input.
TDI	F2	I, PU, ST, 3 V	JTAG test serial data input.
TDO	F1	O	JTAG test serial data output.
TMS	E2	I, PU, ST, 3 V	JTAG test mode select.
TRST	E3	I, PU, ST, 3 V	JTAG reset. **Important** When JTAG is not in use, this pin must be tied to ground with a pull-down resistor for normal operation.

6.3.4 Miscellaneous

The following table lists the miscellaneous pins.

Table 163 • **Miscellaneous Pins**

Name	Pin	Type	Description
CLK_SQUELCH_IN	E15	I, PU, 3 V	Input control to squelch recovered clock.

Table 163 • **Miscellaneous Pins *(continued)***

Name	Pin	Type	Description
COMA_MODE	L3	I, PU, 3 V	When this pin is asserted high, all PHYs are held in a powered down state. When de-asserted low, all PHYs are powered up and resume normal operation. This signal is also used to synchronize the operation of multiple chips on the same PCB to provide visual synchronization for LEDs driven by separate chips. For more information, see Initialization, page 78. For more information about a typical bring-up example, see Configuration, page 77.
LED0_PHY[0:3] LED1_PHY[0:3] LED2_PHY[0:3] LED3_PHY[0:3]	G1, H1, J1, K1 G2, H2, J2, K2 G3, H3, J3, K3 G4, H4, J4, K4	O	LED direct-drive outputs. All LEDs pins are active-low. A serial LED stream can also be implemented. For more information, see LED Mode Select, page 95.
NC_[1:4]	A1, A16, T1, T16	NC	No connect.
NRESET	M3	I, PD, ST, 3 V	Device reset. Active low input that powers down the device and sets all register bits to their default state.
PHYADD1	F13	I, PU, 3V	Device SMI address bit 1. Normally tied to VSS unless an address offset of 0x2 is used by a specific system's station manager. For more information, see PHY Addressing, page 13.
PHYADD[2:4]	G13, G14, F14	I, PD, 3 V	Device SMI address bits 4:2. For more information, see PHY Addressing, page 13.
RCVRDCLK1 RCVRDCLK2	F16 G16	O	Clock output can be enabled or disabled and also output a clock frequency of 125 MHz or 25 MHz based on the selected active recovered media programmed for this pin. This pin is not active when NRESET is asserted. When disabled, the pin is held low.
REF_FILT_A	D3	ABIAS	Reference filter connects to an external 1 µF capacitor to analog ground.
REF_REXT_A	D4	ABIAS	Reference external connects to an external 2 kΩ (1%) resistor to analog ground.
REFCLK_N REFCLK_P	C1 D1	I, ADIFF	125 MHz or 25 MHz reference clock input pair. Must be capacitively coupled and LVDS compatible.
REFCLK_SEL2	E1	I, PU, 3 V	Selects the reference clock speed. 0: 25 MHz (VSS) 1: 125 MHz (2.5 V) Use 125 MHz for typical applications.
RESERVED_[1:8]	C10, D13, L4, P4, L1, M1, N1, P1		Reserved. Leave unconnected.
RESERVED_[18:19]	J15, J16		Reserved. Leave unconnected.
RESERVED_[71:74]	N3, N4, L2, E14		Reserved. Leave unconnected.
THERMDA	C3	A	Thermal diode anode.

Table 163 • **Miscellaneous Pins *(continued)***

Name	Pin	Type	Description
THERMDC_VSS	D2	A	Thermal diode cathode connected to device ground. Temperature sensor must be chosen accordingly.

6.3.5 Power Supply and Ground

The following table lists the power supply and ground pins and associated functional pins. All power supply pins must be connected to their respective voltage input, even if certain functions are not used for a specific application. No power supply sequencing is required. However, clock and power must be stable before releasing the NRESET pin.

Table 164 • **Power Supply and Ground Pins**

Name	Pin	Description
VDD_MDIO	P3	1.2 V or 2.5 V power for SMI pins.
VDD1_[1:18]	E5, E12, F5, F12, G5, G12, H5, H12, J5, J12, K5, K12, L5, L12, M5, M12, N5, N12	1.0 V internal digital logic.
VDD1A_[1:10]	C7, C8, C9, C13, P6, P7, P8, P9, P10, P11	1.0 V analog power requiring additional PCB power supply filtering. Associated with the QSGMII/SGMII MAC receiver output pins.
VDD25_[1:3]	H13, M4, M13	2.5 V general digital power supply. Associated with the LED, GPIO, JTAG, twisted pair interface, reference filter, reference external supply connect, and recovered clock pins.
VDD25A_[1:10]	C2, C4, C6, C11, C14, E4, E13, P5, P12, P13	2.5 V general analog power supply.
VSS	D14, H16, R1	Ground.
VSS_[1:4]	B1, B16, C5, C12	Ground.
VSS_[6:68]	D5, D6, D7, D8, D9, D10, D11, D12, E6, E7, E8, E9, E10, E11, F4, F6, F7, F8, F9, F10, F11, G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11, L6, L7, L8, L9, L10, L11, M6, M7, M8, M9, M10, M11, N6, N7, N8, N9, N10, N11	Ground.
VSS_70	R16	Ground.

6.3.6 SerDes MAC Interface

The following table lists the SerDes MAC interface pins. Leave unused SerDes transceive pairs unconnected.

Table 165 • **SerDes MAC Interface Pins**

Name	Pin	Type	Description
RDN_0 RDP_0	P16 P15	O, ADIFF	PHY0 QSGMII/SGMII/SerDes MAC receiver output pair.

Table 165 • **SerDes MAC Interface Pins *(continued)***

Name	Pin	Type	Description
RDN_1[:3] RDP_[1:3]	T12, T8, T4 R12, R8, R4	O, ADIFF	SGMII/SerDes MAC receiver output pair.
SerDes_Rext_0 SerDes_Rext_1	P14 N13	ABIAS	SerDes bias pins. Connect a 620 Ω 1% resistor across these pins.
TDN_0 TDP_0	N16 N15	I, ADIFF	PHY0 QSGMII/SGMII/SerDes MAC transmitter input pair.
TDN_[1:3] TDP_[1:3]	T13, T9, T5 R13, R9, R5	I, ADIFF	SGMII/SerDes MAC transmitter input pair.

6.3.7 SerDes Media Interface

The following table lists the SerDes media interface pins. Leave unused SerDes transceive pairs unconnected.

Table 166 • **SerDes Media Interface Pins**

Name	Pin	Type	Description
FIBRIN_[0:3]	T15, T11, T7, T3	I, ADIFF	SerDes media receiver input pair.
FIBRIP_[0:3]	R15, R11, R7, R3	I, ADIFF	SerDes media receiver input pair.
FIBRON_[0:3]	T14, T10, T6, T2	O, ADIFF	SerDes media transmitter output pair.
FIBROP_[0:3]	R14, R10, R6, R2	O, ADIFF	SerDes media transmitter output pair.

6.3.8 Serial Management Interface

The following table lists the serial management interface (SMI) pins. The SMI pins are referenced to VDD_MDIO and can be set to either 1.2 V or 2.5 V. This interface must be set to the appropriate voltage that VDD_MDIO is set to.

Table 167 • **SMI Pins**

Name	Pin	Type	Description
MDC[1]	P2	I, PU	Management data clock. A 0 MHz to 12.5 MHz reference input is used to clock serial MDIO data into and out of the PHY.
MDINT	M2	I/O, OD	Management interrupt signal. These pins can be tied together in a wired-OR configuration with a single pull-up resistor.
MDIO[1, 2]	N2	I/O, OD	Management data input/output pin. Serial data is written or read from this pin bidirectionally between the PHY and Station Manager, synchronously on the positive edge of MDC. One external pull-up resistor is required at the Station Manager, and its value depends on the MDC clock frequency and the total sum of the capacitive loads from the MDIO pins.

1. 3.3 V input tolerant when supply VDD_MDIO is at 2.5 V, and 2.5 V input tolerant when VDD_MDIO is at 1.2 V.
2. When the PHY drives read data on MDIO, it can only source 2.5 V to the MDIO pin.

6.3.9 SIGDET/GPIO

The following table lists the GPIO and signal detect pins.

Table 168 • **SIGDET/GPIO Pins**

Name	Pin	Type	Description
SIGDET0/GPIO0	N14	I/O, PU, 3 V	General purpose input/output (GPIO). The multipurpose SIGDET and fast link fail pins can be configured to serve as GPIOs.
SIGDET1/GPIO1	M14	I/O, PU, 3 V	General purpose input/output (GPIO). The multipurpose SIGDET and fast link fail pins can be configured to serve as GPIOs.
SIGDET2/GPIO2	M15	I/O, PU, 3 V	General purpose input/output (GPIO). The multipurpose SIGDET and fast link fail pins can be configured to serve as GPIOs.
SIGDET3/GPIO3	M16	I/O, PU, 3 V	General purpose input/output (GPIO). The multipurpose SIGDET and fast link fail pins can be configured to serve as GPIOs.

6.3.10 SPI Interface

The following table lists the SPI interface pins.

Table 169 • **SPI Interface Pins**

Name	Pin	Type	Description
SPI_IO_CLK	H15	I/O, PU, 3 V	Serial peripheral interface clock input from external device
SPI_IO_CS	J13	I/O, PU, 3 V	Serial peripheral interface chip select
SPI_IO_DI	G15	I/O, PU, 3 V	Serial peripheral interface data input
SPI_IO_DO	F15	I/O, PU, 3 V	Serial peripheral interface data output

6.3.11 Twisted Pair Interface

The following table lists the twisted pair interface pins.

Table 170 • **Twisted Pair Interface Pins**

Name	Pin	Type	Description
TXVNA_[0:3]	B14, B10, B6, B2	ADIFF	TX/RX channel A negative signal
TXVNB_[0:3]	B15, B11, B7, B3	ADIFF	TX/RX channel B negative signal
TXVNC_[0:3]	C15, B12, B8, B4	ADIFF	TX/RX channel C negative signal
TXVND_[0:3]	D15, B13, B9, B5	ADIFF	TX/RX channel D negative signal
TXVPA_[0:3]	A14, A10, A6, A2	ADIFF	TX/RX channel A positive signal
TXVPB_[0:3]	A15, A11, A7, A3	ADIFF	TX/RX channel B positive signal
TXVPC_[0:3]	C16, A12, A8, A4	ADIFF	TX/RX channel C positive signal
TXVPD_[0:3]	D16, A13, A9, A5	ADIFF	TX/RX channel D positive signal

7 Package Information

VSC8564XKS-11 and VSC8564XKS-14 are packaged in a lead-free (Pb-free), 256-pin, plastic ball grid array (BGA) with a 17 mm × 17 mm body size, 1 mm pin pitch, and 1.8 mm maximum height.

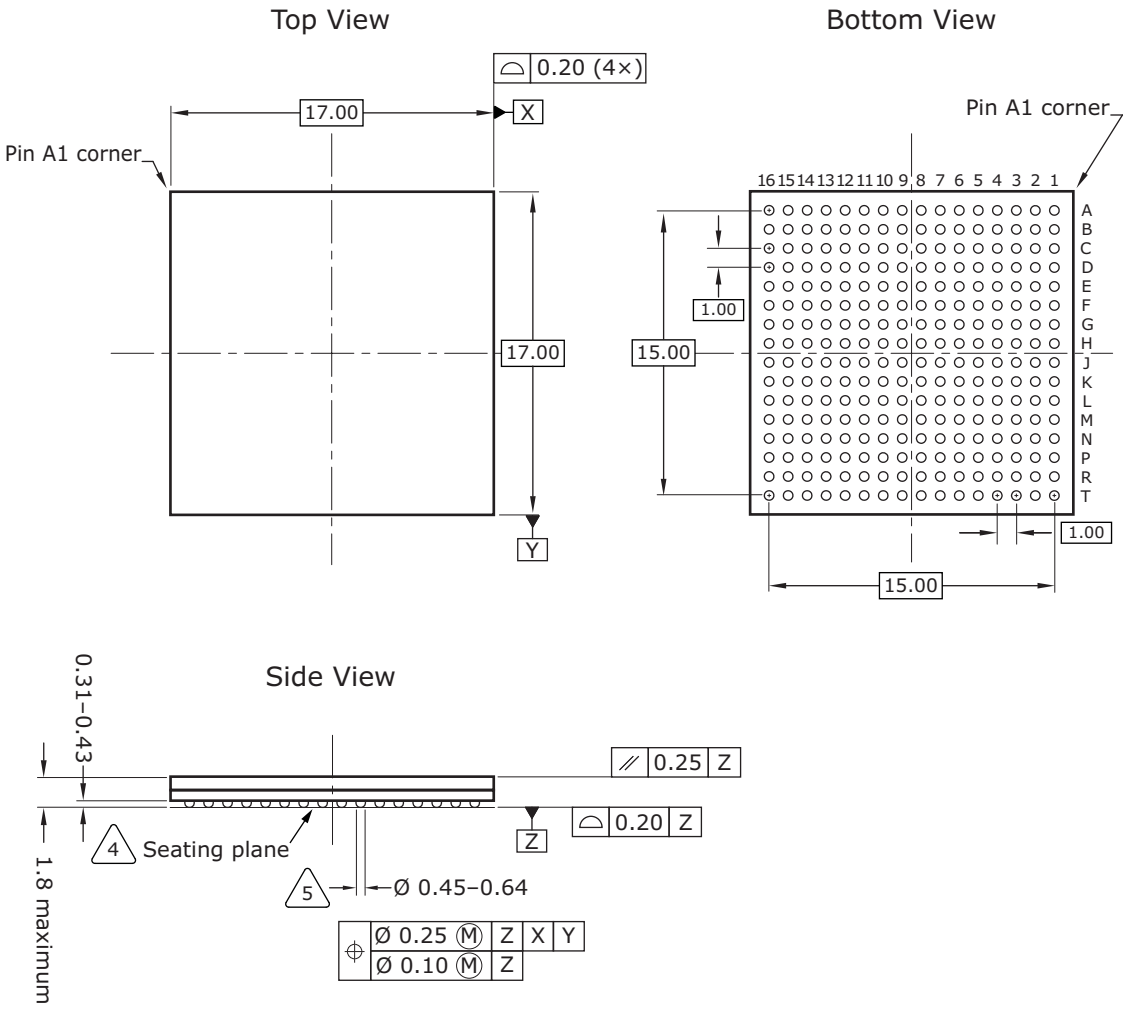
Lead-free products from Microsemi comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

This section provides the package drawing, thermal specifications, and moisture sensitivity rating for the device.

7.1 Package Drawing

The following illustration shows the package drawing for the device. The drawing contains the top view, bottom view, side view, dimensions, tolerances, and notes.

Figure 83 • **Package Drawing**



Notes

1. All dimensions and tolerances are in millimeters (mm).
2. Ball diameter is 0.50 mm.
3. Radial true position is represented by typical values.
4. Primary datum Z and seating plane are defined by the spherical crowns of the solder balls.
5. Dimension is measured at the maximum solder ball diameter, parallel to primary datum Z.

7.2 Thermal Specifications

Thermal specifications for this device are based on the JEDEC JESD51 family of documents. These documents are available on the JEDEC Web site at www.jedec.org. The thermal specifications are modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p

PCB). For more information about the thermal measurement method used for this device, see the JESD51-1 standard.

Table 171 • **Thermal Resistances**

Symbol	°C/W	Parameter
θ_{JCtop}	5.1	Die junction to package case top
θ_{JB}	10.5	Die junction to printed circuit board
θ_{JA}	19.6	Die junction to ambient
θ_{JMA} at 1 m/s	16.3	Die junction to moving air measured at an air speed of 1 m/s
θ_{JMA} at 2 m/s	14.2	Die junction to moving air measured at an air speed of 2 m/s

To achieve results similar to the modeled thermal measurements, the guidelines for board design described in the JESD51 family of publications must be applied. For information about applications using BGA packages, see the following:

- JESD51-2A, *Integrated Circuits Thermal Test Method Environmental Conditions, Natural Convection (Still Air)*
- JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions, Forced Convection (Moving Air)*
- JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions, Junction-to-Board*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

7.3 Moisture Sensitivity

This device is rated moisture sensitivity level 4 as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

8 Design Considerations

This section provides information about design considerations for the VSC8564-11 device.

8.1 Clause 45 register address post-increment

Clause 45 register address post-increment only works when reading registers and only when extended page access register 31 is set to 0.

The workaround is to access registers individually.

8.2 Clause 45, register 7.60

Clause 45, register 7.60 bit 10 always reads back value 1. However per IEEE 802.3z, reserved bits should read back value 0.

This has a minor implication on software that needs to ignore bit 10 in the read-back value of clause 45 register 7.60.

8.3 10BASE-T signal amplitude

10BASE-T signal amplitude can be lower than the minimum specified in IEEE 802.3 paragraph 14.3.1.2.1 (2.2 V) at low supply voltages. Additionally, associated templates may be marginal or have failures.

This issue is not estimated to present any system level impact. Performance is not impaired with cables up to 130 m with various link partners.

8.4 10BASE-T Half-Duplex linkup after initial reset from power up

After initial power-on, register 0 Mode Control of port 0 of the device may contain all zeros and thus operate in forced 10BASE-T half-duplex mode.

The workaround is to perform a software reset of port 0 using register 0 bit 15 to restore the power-on default values. For more information, see Mode Control, page 81.

8.5 Link performance in 100BASE-TX and 1000BASE-T modes

PHY ports may exhibit sub-optimal performance under certain environmental and cabling conditions without proper initialization.

Furthermore, under worst-case operating conditions while in 100BASE-TX mode, the PHY cannot compensate for the limits of attenuation and phase distortion introduced at maximum cable lengths, or compensate for worst-case baseline wander introduced by 100BASE-TX “killer” packets.

Contact Microsemi for a script that needs to be applied during system initialization

8.6 Clause 36 PCS incompatibilities in 1000BASE-X media mode

While operating in 1000BASE-X media mode, certain Media Access Controllers may reject Carrier Extension patterns in ingress frame traffic, in violation of the Clause 36 PCS specification.

The workaround to ensure no frame errors with such link-partner MACs is to disable Carrier Extensions in 1000BASE-X mode by setting register 23E3 bit 12.

8.7 1000BASE-X parallel detect mode with Clause 37 auto-negotiation enabled

When connected to a forced-mode link partner and attempting auto-negotiation, the PHY in 1000BASE-X parallel detect mode requires a minimum 250 millisecond IDLE stream in order to establish a link. If the PHY port is programmed with 1000BASE-X parallel detect-enabled (MAC-side register 16E3 bit 13, or media-side register 23E3 bit 13), then a forced-mode link partner sending traffic with an inter-packet gap less than 250 milliseconds will not allow the local device's PCS to transition from a link-down to link-up state.

8.8 Near-end loopback non-functional in protocol transfer mode

Near-end loopback does not work correctly when the device is configured in protocol transfer mode.

This is a debug feature and does not have any effect on the normal operation of the device.

8.9 Far-end loopback requires disabling Tx preamble fix for 1000M traffic

Any traffic flowing at 1000 Mbps on the port when far-end loopback is enabled may be dropped if Tx preamble fixing (22E3 bit 13) is also enabled.

The workaround for this issue is to clear bit 22E3.13 before using far-end loopback. Once loopback operation is disabled, then 22E3 bit 13 should be set again before flowing traffic.

8.10 VTSS_MACSEC_uncontrolled_counters_get show incorrect counter values

The counter value displayed by vtss_macsec_uncontrolled_counters_get is incorrect. When protectframes == false, the controlled port counter will not include untagged frames. This is considered a minor bug because the protectframes == false control is provided to facilitate MACsec deployment and is not the usual MACsec mode of operation.

The Microsemi API will return NULL values for counter return when protectframes == false to indicate that there is a bug in this function and this function is not available.

8.11 Controlled port counter if_in_octets does not get set correctly

When validateFrames == Disabled, InOctetsValidated/Decrypted is not incremented (as per standard). As a result, the if_in_octets calculation of a controlled port is incorrect. This is considered a minor bug because the validateFrames == Disabled control is provided to facilitate MACsec deployment and is not the usual MACsec mode of operation.

The Microsemi API will return NULL values for if_in_octets calculations to indicate there is a bug in this function.

8.12 LED Duplex/Collision function not working when in protocol transfer mode 10/100 Mbps

When a PHY port is configured for protocol transfer mode of operation, the Duplex/Collision function of an LED does not properly indicate if the link is full-duplex.

Because protocol transfer mode is used with copper SFP modules, the PHY-copper SFP link will always operate in full-duplex mode, and thus the PHY LED duplex indicator has little real-world significance.

8.13 Fast Link Failover indication delay when using interrupts

Whenever the fast link failure interrupt mask is enabled (register 25, bit 7), MDINT will assert at the onset of a link failure in less than 6 ms typical (8 ms, worst-case).

8.14 Anomalous Fast Link Failure indication in 1000BT Energy Efficient Ethernet mode

When a port is linked in 1000BT in EEE mode, the Fast Link Failure indication may falsely assert while processing bursting traffic. EEE should be disabled when FLF indication is in use.

8.15 Anomalous PCS error indications in Energy Efficient Ethernet mode

When a port is processing traffic with EEE enabled on the link, certain PCS errors (such as false carriers, spurious start-of-stream detection, and idle errors) and EEE wake errors may occur. There is no effect on traffic bit error rate, but some error indications should not be used while EEE is enabled. These error indications include false carrier interrupts (interrupt status, register 26 bit 3), receive error interrupts (interrupt status, register 26 bit 0), and EEE wake error interrupts.

Contact Microsemi for a script that needs to be applied during system initialization if EEE will be enabled.

8.16 Auto-Negotiation Management Register Test failures

MII register 10 bit 15 (Master/Slave Configuration Fault) does not self-clear before a subsequent 1000BT link up attempt. This is a minor bug, and can be worked around by reading the register twice to ensure bit 15 status shows the correct 1000BT auto-negotiation result.

MII register 4 bit field 4:0 (Reserved Selector Fields) will accept values other than IEEE 802.3 Ethernet code values to be transmitted by the PHY during auto-negotiation base page exchange. This is a minor bug because it requires deliberate misconfiguration of the selector field in register 4, which the PHY API does not perform.

8.17 Changing speed from 1 Gbps to 100 Mbps hangs MACsec engine

When MACsec is enabled and traffic is flowing, the flow control buffer inside the MACsec engine may hang when the PHY media speed is changed. The workaround is to poll the flow control buffer overflow status bit from the MACsec engine, and if the buffer overflow bit is set, command a soft reset of the MACsec engine and then reconfigure it.

8.18 Non-standard preamble frames discarded by MACsec engine

When MACsec is enabled, the PHY only processes incoming frames with preamble lengths less than or equal to 8 bytes. Frames with longer preambles are discarded by the MACsec IP block and do not appear at the external MAC interface of the device.

8.19 Pause control frames pause_timer may be exceeded by MACsec engine

When MACsec is enabled, a pause control frame's pause_timer value may be marginally exceeded before the PHY resumes transmission of MAC client frames.

This issue has no real-world impact to observable delays in traffic from the PHY device because the threshold of failure is on the order of microseconds.

8.20 MACsec engine may shrink the minimum 100M IPG during wire-speed transmission

When MACsec is enabled and transmitting in 100 Mbps mode, the PHY may transmit frames with InterPacketGap as low as 72 bit times during frame transmissions at line speed. However, the PHY maintains an average InterPacketGap of 96 bit times as per the IEEE 802.3 standard. Thus, there is marginal impact on frequency offset tolerance between link partner PHYs when operating at 100 Mbps.

8.21 Operate MACsec with flow control to handle bandwidth expansion

Because MACsec processing results in frame expansion, flow control must be enabled to manage bandwidth at the host interface. When MACsec is enabled, the Unified API enables advanced flow control handling (see Advanced Flow Control Handling, page 48).

The host MAC to which the PHY is connected must also have flow control enabled in order to react to PAUSE commands from the PHY. If flow control is disabled, egress traffic originating from the PHY client at wire speed may result in truncated (invalid) frames.

This is only a practical issue during testing scenarios because this invalid frame error only occurs when flow control is disabled, which would not be useful in a real-world network.

The workaround and recommended method to operate MACsec is with pause control enabled such that the PHY pauses host egress traffic when utilization exceeds the available bandwidth of the line.

8.22 Frames with nibbles after the FCS may be discarded by MACsec engine

When MACsec is enabled, ingress traffic in 10 Mbps or 100 Mbps mode received with an extra nibble following a valid FCS field may be dropped. This scenario only happens during MACsec operation in a half-duplex collision-domain. In the rare event that collision occurs at the byte after FCS, the IP packet is dropped by the PHY and retransmission requested.

9 Ordering Information

The device is offered with two operating temperature ranges. The range for VSC8564-11 is 0 °C ambient to 125 °C junction. The range for VSC8564-14 is –40 °C ambient to 125 °C junction.

VSC8564XKS-11 and VSC8564XKS-14 are packaged in a lead-free (Pb-free), 256-pin, plastic ball grid array (BGA) with a 17 mm × 17 mm body size, 1 mm pin pitch, and 1.8 mm maximum height.

Lead-free products from Microsemi comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

The following table lists the ordering information.

Table 172 • **Ordering Information**

Part Order Number	Description
VSC8564XKS-11	Lead-free, 256-pin, plastic BGA with a 17 mm × 17 mm body size, 1 mm pin pitch, and 1.8 mm maximum height. The operating temperature is 0 °C ambient to 125 °C junction[1].
VSC8564XKS-14	Lead-free, 256-pin, plastic BGA with a 17 mm × 17 mm body size, 1 mm pin pitch, and 1.8 mm maximum height. The operating temperature is –40 °C ambient to 125 °C junction[1].

1. For carrier class applications, the maximum operating temperature is 110 °C junction.

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