ZL30256
3-Channel, 10-Input, 18-Output General-Purpose Jitter Attenuator

Data Sheet

Block Diagram page 7. Register Map section 9.3

October 2020

Features

- **One, Two or Three DPLL Channels**
  - Programmable bandwidth, 14Hz to 470Hz
  - Freerun or holdover on loss of all inputs
  - Hitless reference switching
  - High-resolution holdover averaging
  - Per-DPLL phase adjustment, 1ps resolution
  - Programmable tracking range, phase-slope limiting, frequency-change limiting and other advanced features
- **Input Clocks**
  - Accepts up to 10 differential or CMOS inputs
  - Any input frequency from 1kHz to 900MHz
  - Per-input activity and frequency monitoring
  - Automatic or manual reference switching
  - Revertive or nonrevertive switching
  - Input-input phase measurement, 1ps resolution
  - Input-DPLL phase measurement, 1ps resolution
  - Per-input phase adjustment, 1ps resolution
- **Output Clock Frequency Generation**
  - Any output frequency from 1Hz to 1045MHz (180MHz max for Synth0)
  - High-resolution fractional frequency conversion with 0ppm error
  - Synthesizers 1 & 2 have integer and fractional dividers to make a total of 5 frequency families
  - Output jitter from Synth 1 & 2 is <0.3ps RMS
  - Output jitter from fractional dividers is typically < 1ps RMS, many frequencies <0.5ps RMS
  - Each HPOUTP/N pair can be LVDS, LVPECL, HCSL, 2xCMOS, HSTL or programmable diff.
  - In 2xCMOS mode, the P and N pins can be different frequencies (e.g. 125MHz and 25MHz)
  - Four output banks each with VDDO pin; CMOS output voltages from 1.5V to 3.3V
  - Per-synthesizer phase adjust, 1ps resolution
  - Per-output programmable duty cycle
  - Precise output alignment circuitry and per-output phase adjustment
  - Per-output enable/disable and glitchless start/stop (stop high or low)
- **Local Oscillator**
  - Operates from a single low-cost XO: 23.75-25MHz, 47.5-50MHz, 114.285-125MHz
- **General Features**
  - Automatic self-configuration at power-up from internal Flash memory
  - Input-to-output alignment <200ps (ext feedback)
  - Internal compensation (1ppt) for local oscillator frequency error in DPLLs and input monitors
  - Numerically controlled oscillator behavior in each DPLL and each fractional output divider
  - Easy-to-configure design requires no external VCXO or loop filter components
  - 7 GPIO pins with many possible behaviors
  - SPI or I^2C processor Interface
  - 1.8V and 3.3V core VDD voltages
  - Power: 1.3W for 2 inputs, 1 synth, 6 LVDS out
  - Easy-to-use evaluation/programming software

Ordering Information

ZL30256LFG7	80-lead LGA NiAu (Pb-free) Package size: 11 x 11 mm	Trays

-40°C to +85°C

Applications

- Jitter attenuation, frequency conversion, and frequency synthesis in a wide variety of system types

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1. Block Diagram

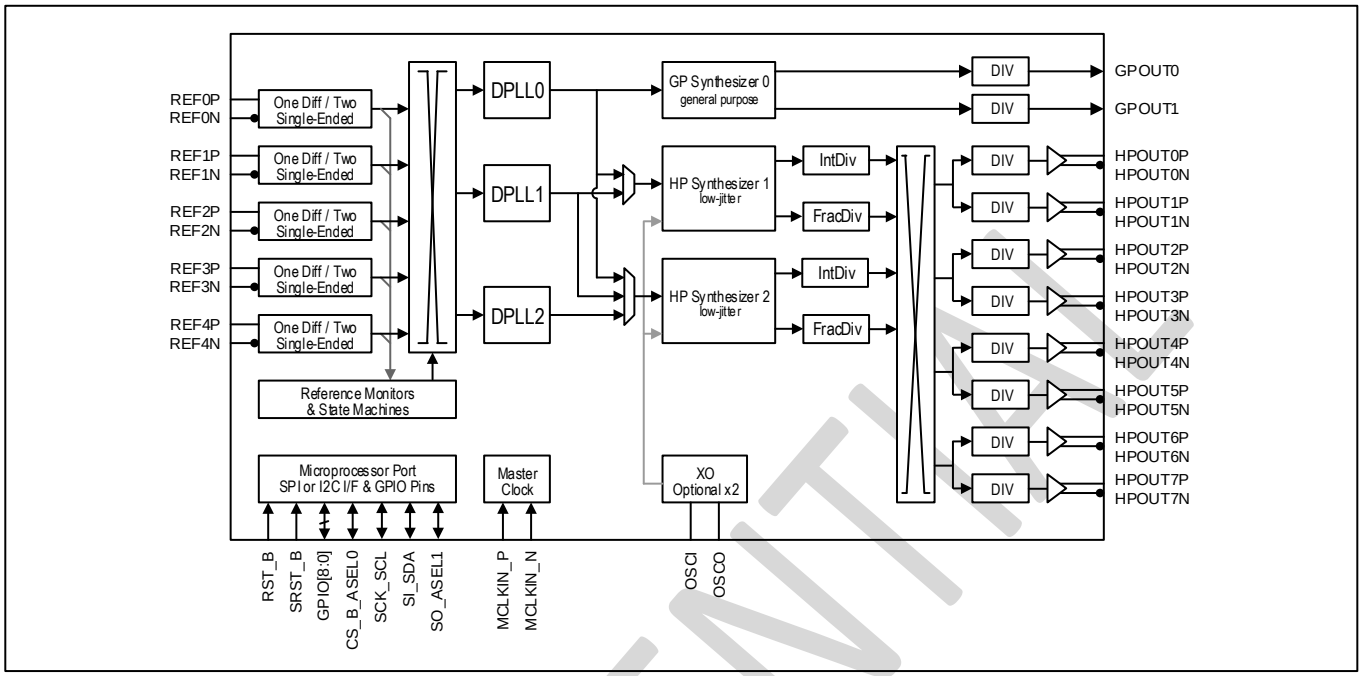


Figure 1 - Functional Block Diagram

2. Application Example

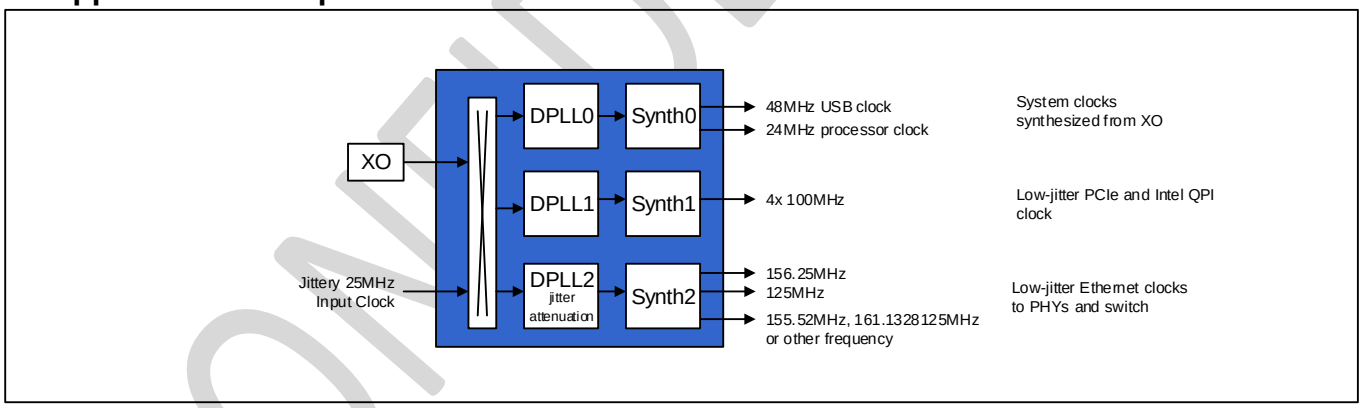


Figure 2 – Application Example

3. Detailed Features

3.1 Input Block Features

- Ten input reference pins; each can accept a CMOS signal or the POS side of a differential pair; or two can be paired to accept both sides of a differential pair (see Figure 5)
- Input clocks can be any frequency from 1kHz up to 900MHz (180MHz max for CMOS inputs)
- Inputs constantly monitored by programmable frequency and single-cycle monitors
- Single-cycle monitor can quickly disqualify a reference when measured period is incorrect
- Frequency measurement (ppb or Hz) and monitoring (coarse, fine, and frequency-step monitors)
- Optional input clock invalidation on GPIO assertion to react to LOS signals from PHYs
- Input-to-input phase measurement, 1ps resolution
- Input-to-DPLL phase measurement, 1ps resolution
- Per-input phase adjustment, 1ps resolution

3.2 DPLL Features

- One, two or three full-featured DPLLs
- Very high-resolution DPLL architecture
- State machine automatically transitions among freerun, tracking and holdover states
- Revertive or nonrevertive reference selection algorithm
- Programmable bandwidth from 14Hz to 470Hz
- Less than 0.25dB gain peaking
- Programmable phase-slope limiting (PSL)
- Programmable frequency rate-of-change limiting (FCL)
- Programmable tracking range (i.e. hold-in range)
- Truly hitless reference switching
- Per-DPLL phase adjustment, 1ps resolution
- High-resolution frequency and phase measurement
- Fast detection of input clock failure and transition to holdover mode
- High-resolution holdover frequency averaging

3.3 Synthesizer Features

- Any-to-any frequency conversion with 0ppm error
- Two low-jitter synthesizers (Synth1, Synth2) with very high-resolution fractional scaling (i.e. non-integer multiplication)
- Two output dividers per low-jitter synthesizer: one integer (4 to 15 plus half divides 4.5 to 7.5) and one 40-bit fractional
- One general-purpose synthesizer (Synth0)
- A total of five output frequency families
- Easy-to-configure, completely encapsulated design requires no external VCXO or loop filter components

3.4 Low-Jitter Output Clock Features

- Up to 16 single-ended outputs (up to 8 differential outputs) from Synth1 and Synth2
- Each output can be one differential output or two CMOS outputs
- Output clocks can be any frequency from 1Hz to 1045MHz (250MHz max for CMOS and HSTL outputs)
- Output jitter from Synth1 and Synth2 integer dividers is <0.3ps RMS
- Output jitter from fractional dividers is <1ps RMS, many frequencies <0.5ps RMS
- In CMOS mode, the HPOUTxN frequency can be an integer divisor of the HPOUTxP frequency (Example 1: HPOUT3P 125MHz, HPOUT3N 25MHz. Example 2: HPOUT2P 25MHz, HPOUT2N 1Hz)
- Outputs directly interface (DC coupled) with LVDS, LVPECL, HSTL, HCSL and CMOS components
- Can produce clock frequencies for microprocessors, ASICs, FPGAs and other components
- Can produce PCIe clocks
- Sophisticated output-to-output phase alignment
- Per-synthesizer phase adjustment, 1ps resolution

- Per-output phase adjustment
- Per-output duty cycle / pulse width configuration
- Per-output enable/disable
- Per-output glitchless start/stop (stop high or low)

3.5 General-Purpose Output Clock Features

- Two CMOS outputs from Synth0
- Any frequency from 1Hz to 180MHz
- Output jitter is typically 20-30ps
- Useful for applications where the component or system receiving the signal has low bandwidth such as a central timing IC

3.6 Local Oscillator

- Operates from a single low-cost XO (jitter reference for the device). Acceptable frequencies: 23.75MHz to 25MHz, 47.5MHz to 50MHz, 114.285MHz to 125MHz. Best jitter: ≥48MHz.

3.7 General Features

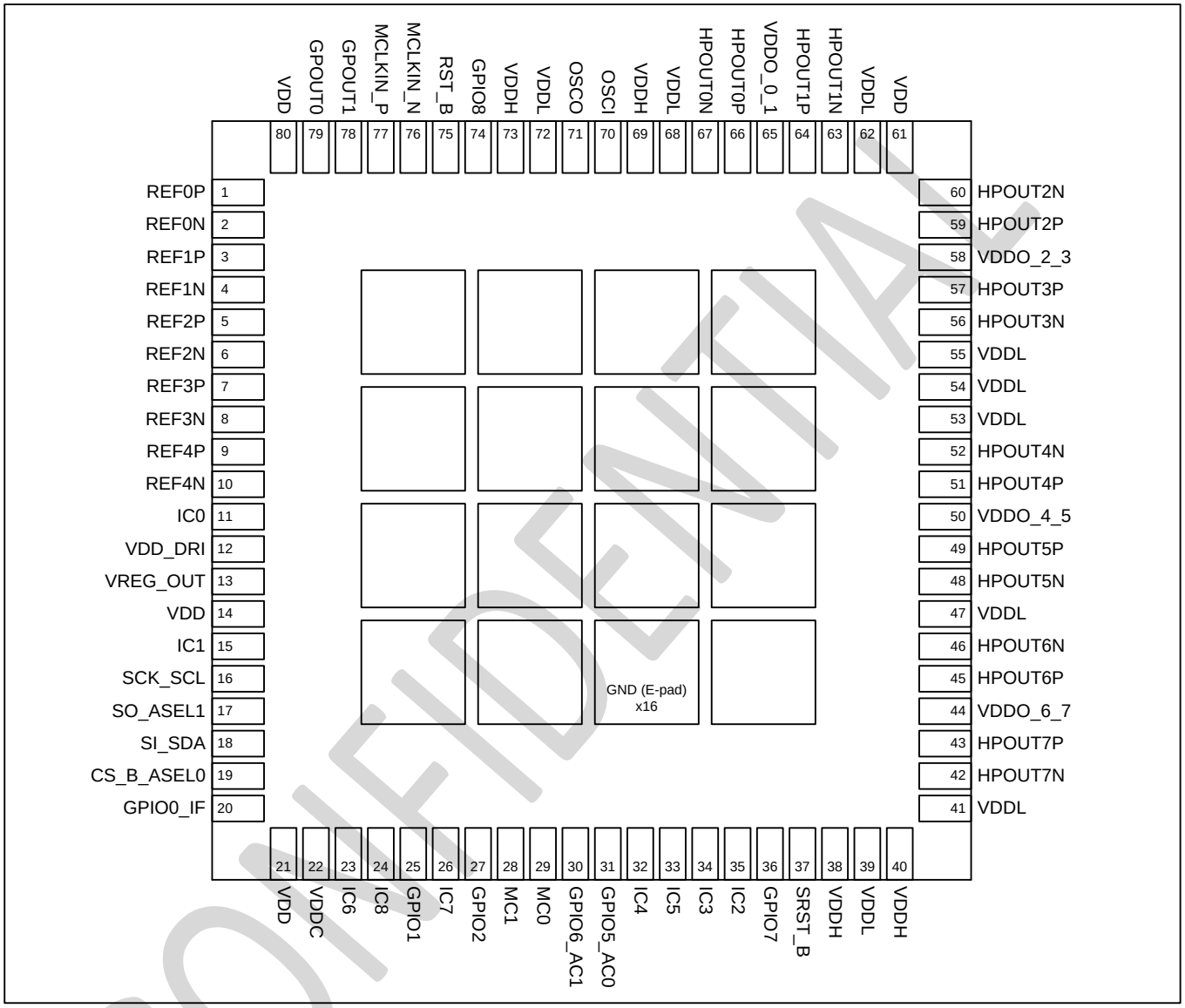
- Automatic self-configuration at power-up from internal Flash memory
- Input-to-output alignment <200ps with external feedback
- Generates output SYNC signals: 1PPS (IEEE 1588), 2kHz or 8kHz (SONET/SDH) or other frequency
- JESD204B clocking: device clock and SYSREF signal generation with skew adjustment
- Internal compensation for local oscillator frequency error in DPLLs and input monitors, 1ppt resolution
- Numerically controlled oscillator (NCO) behavior allows system software to steer DPLL frequency or fractional output divider frequency with resolution better than 0.005ppt
- Seven general-purpose I/O pins each with many possible status and control options
- SPI or I^2C serial microprocessor interface

3.8 Evaluation Software

- Simple, intuitive Windows-based graphical user interface
- Supports all device features and register fields
- Makes lab evaluation of the device quick and easy
- Generates configuration scripts to be stored in internal Flash memory
- Generates full or partial configuration scripts to be run on a system processor
- Works with or without an evaluation board

4. Pin Diagram

80-lead LGA, 0.5mm pitch



5. Pin Descriptions

All device inputs and outputs are LVCMOS unless described otherwise. The Type column uses the following symbols: I – input, O – output, A – analog, P – power supply pin. All GPIO and SPI/I²C interface pins have Schmitt-trigger inputs and have output drivers that can be disabled (high impedance). See diagram in section 13 for pin locations by number.

Table 1 - Pin Descriptions

Pin #	Name	Type	Description
Input References			
1 2 3 4 5 6 7 8 9 10	REF0P REF0N REF1P REF1N REF2P REF2N REF3P REF3N REF4P REF4N	I	**Input References (CMOS, LVDS, LVPECL, CML, HCSL)** Each REFxP/REFxN pair can accept a differential signal or up to two single-ended signals. Single-ended signals can be CMOS or one side of a differential signal, as shown in Figure 5c (this is called single-ended LVPECL mode). Recommended termination circuitry for all of these options is shown in Figure 5. Input frequency range for LVPECL, LVDS, HCSL, CML is from 1kHz to 900MHz for both differential mode and single-ended LVPECL mode. Input frequency range for LVCMOS is from 1kHz to 180MHz. Unused REF inputs should have ref_config.enable=0 and be left floating. When a REFxP/REFxN pair is used to receive one CMOS signal and one single-ended LVPECL signal, the CMOS pin must be wired to the REFxP pin, the single-ended LVPECL signal must be wired to the REFxN pin, and the ref_config.lvpecl_en bits set appropriately.
Output Clocks			
66 67 64 63 59 60 57 56 51 52 49 48 45 46 43 42	HPOUT0P HPOUT0N HPOUT1P HPOUT1N HPOUT2P HPOUT2N HPOUT3P HPOUT3N HPOUT4P HPOUT4N HPOUT5P HPOUT5N HPOUT6P HPOUT6N HPOUT7P HPOUT7N	O	**High Performance (Low Jitter) Outputs Clocks** LVDS, LVPECL, HCSL, HSTL or 1 or 2 CMOS. Programmable frequency and drive strength. See Table 8, Table 9 and Table 10 for electrical specifications for LVDS, LVPECL and HCSL, respectively. See Table 11 for electrical specifications for interfacing to CMOS and HSTL inputs on neighboring devices.
79 78	GPOUT0 GPOUT1	O	**General Purpose Outputs** Synth0 outputs. CMOS output frequency range is from 1Hz to 180MHz. The power supply for these is VDD.
Control and Status			
75	RST_B	I	**Power-on Reset.** A logic low at this input resets the device. To ensure proper operation, the device must be reset after power-up by driving the RST_B pin low. It is not acceptable to use an external R-C network to hold RST_B low during power-up. The RST_B pin should be held low for at least 2 ms. This pin has an internal 33kΩ pullup to VDD. Device registers can be accessed 1.1s after power-up or reset.

Pin #	Name	Type	Description
37	SRST_B	I	**Synthesizer Reset.** Wire this pin to the RST_B pin.
20 25 27	GPIO0_IF GPIO1 GPIO2	I/O	**General Purpose Input and Output pins / Interface Select** *General-Purpose I/O:* These are general-purpose pins managed by the internal processor based on device configuration. Recommended usage of GPIO include: • DPLL lock indicators • DPLL holdover indicators • Reference fail indicators • Reference select control or monitor • Differential output clock enable (any set of outputs) • High performance LVCMOS outputs enable • Host Interrupt Output: flags changes of device status prompting the processor to read the enabled interrupt service registers (ISR). GPIO0_IF has an internal 33kΩ pulldown to VSS. GPIO[2:1] each have an internal 33kΩ pullup to VDD. If not used, GPIOs can be left unconnected. *Interface Select:* Just after reset, the GPIO0_IF pin specifies the host interface: 0=SPI, 1=I2C The GPIO0_IF pin must be at the correct logic level to specify the desired host interface type for 550ms after reset. Then it can be used for normal GPIO functions. If an external pullup or pulldown resistor is used on this pin it should be 1kΩ. Note: GPIO pins are numbered 0, 1, 2 and 5, 6, 7 and 8. GPIO pins 3 and 4 are not available.
31 30 36 74	GPIO5_AC0 GPIO6_AC1 GPIO7 GPIO8	I/O	**General Purpose Input and Output pins / Auto-Configure.** *General-Purpose I/O:* After SRST_B is high these are general-purpose I/O pins dedicated to Synth1, Synth2 and the HPOUT dividers and drivers. *Auto-Configure*: On the rising edge of SRST_B, GPIO[6:5] behave as AC[1:0] and specify a custom configuration stored in internal Flash. 00 = configuration 0 01 = configuration 1 10 = configuration 2 11 = factory default state (no configuration) GPIO8 must be low on the rising edge of SRST_B for proper operation.
Host Interface (SPI or I2C Slave)			
16	SCK_SCL	I/O	**Clock for Serial Interface.** Provides clock for the SPI microprocessor interface. This pin is also the serial clock line (SCL) when the host interface is configured for I2C mode. This pin has an internal 33kΩ pullup to VDD. In I2C mode this pin should be externally pulled high by 1kΩ to 5kΩ resistor. See the I2C bus specification for sizing guidance for this resistor, referred to as R_P in that specification.
18	SI_SDA	I/O	**Serial Interface Input.** Serial interface input stream. The serial data stream holds the access command, the address and the write data bits. This pin is also the serial data line (SDA) when the host interface is configured for I2C mode. This pin has an internal 33kΩ pullup to VDD. In I2C mode this pin should be externally pulled high by 1kΩ to 5kΩ resistor. See the I2C bus specification for sizing guidance for this resistor, referred to as R_P in that specification.

Pin #	Name	Type	Description
17	SO_ASEL1	I/O	**Serial Interface Output.** Serial interface output stream. As an output the serial stream holds the read data bits. This pin is also bit 1 of the device's I2C slave address (ASEL1) when the host interface is configured for I2C mode.
19	CS_B_ASEL0	I	**Chip Select for Serial Interface.** SPI chip select (active low). This pin is also bit 0 of the device's I2C slave address (ASEL0) when the host interface is configured for I2C mode. This pin has an internal 33kΩ pullup to VDD.
Master Clock			
29 28	MC0 MC1	I	**Master Clock Frequency Select** These pins should be pulled high or low to specify the master clock frequency as follows: MC[1:0]=00=47.5MHz-50MHz 01=23.75MHz-25MHz 1x=114.285M-125MHz Each of these pins has an internal 33kΩ pullup to VDD.
77 76	MCLKIN_P MCLKIN_N	I	**Core Master Clock** An external low-jitter XO must be wired to MCLKIN_P and to the OSCI pin. Recommended wiring is XO to source-series termination resistor and then equal traces from the resistor to the OSCI and MCLKIN_P pins. No board-level design work is required to account for the different threshold voltages of the MCLKIN and OSCI pins; they clock separate sections of the device. MCLKIN_N is DC-biased to VDD/2 using a 10kΩ resistor to VDD and a 10kΩ resistor to VSS.
70 71	OSCI OSCO	I A-O	**Synth1 and Synth2 Reference Clock (Jitter Reference)** An external low-jitter XO is wired to OSCI and to the MCLKIN_P pin. Recommended wiring is XO (3.3V or 2.5V) to source-series termination resistor and then equal traces from the resistor to the OSCI and MCLKIN_P pins. No board-level design work is required to account for the different threshold voltages of the MCLKIN and OSCI pins; they clock separate sections of the device. See Table 5 and its Note 1. OSCO should be left unconnected.
Miscellaneous			
11	IC0	A-I/O	**Internal Connection.** Leave unconnected. Do not attach to any routing.
15	IC1	I	**Internal Connection.** Pull down with 1kΩ resistor.
35 34	IC2 IC3	I/O	**Internal Connection.** Pull up with 1kΩ resistor. Use a dedicated resistor for each pin and place the resistor close to the device with minimal stub.
32 33	IC4 IC5	I/O	**Internal Connection.** Leave unconnected. Do not attach to any routing.
23	IC6	I	**Internal Connection.** Leave unconnected.
26	IC7	I	**Internal Connection.** Pull down with 1kΩ resistor.
24	IC8	I	**Internal Connection.** Leave unconnected.
Power and Ground			
12	VDD_DRI	P	**Power Supply.** 1.8V ±5%. Associated with core operation (internal regulator block).
13	VREG_OUT	P	**Core Regulator Output.** 1.2V. Connect to an external capacitor to VSS and connect to VDDC pin. Associated with core operation (internal regulator block).
22	VDDC	P	**Core Power Supply.** Connect to VREG_OUT pin. Associated with core operation.
14 21	VDD	P	**Power Supply.** 3.3V ±5%. Associated with REF input reference signals, GPOUTx output clocks signals, host

Pin #	Name	Type	Description
61 80			interface signals, GPIO[2:0] and MC[1:0] signals.
38 40 69 73	VDDH	P	**Power Supply.** 3.3V ±5%. Associated with Synth1, Synth2 and HPOUT dividers.
39 41 47 53 54 55 62 68 72	VDDL	P	**Power Supply.** 1.8V ±5%. Associated with Synth1, Synth2 and HPOUT dividers.
65	VDDO_0_1	P	**Output Power Supply.** 1.5V ±5% to VDDH. For pins HPOUT0P/N and HPOUT1P/N.
58	VDDO_2_3	P	**Output Power Supply.** 1.5V ±5% to VDDH. For pins HPOUT2P/N and HPOUT3P/N.
50	VDDO_4_5	P	**Output Power Supply.** 1.5V ±5% to VDDH. For pins HPOUT4P/N and HPOUT5P/N.
44	VDDO_6_7	P	**Output Power Supply.** 1.5V ±5% to VDDH. For pins HPOUT6P/N and HPOUT7P/N.
E-pads qty 16	VSS	P	**Ground.** 0 Volts. Each of the 16 pads on the device should be soldered to a corresponding pad on the board. The board pads should be wired directly to board ground plane(s) for proper thermal performance. Any vias in the board pad should be filled to prevent solder migration into the vias during reflow.

6. Functional Description

6.1 Input References

6.1.1 Input Sources

The device has ten inputs (single-ended or differential) as possible references for the DPLLs. See Figure 5 for connection options and recommended external components.

The device synchronizes (locks) to any input reference which is a 1 kHz multiple, or any input reference which is an M/N x 1 kHz multiple (FEC rate) where M and N are 16 bits wide. In some cases M/N x 1 Hz, M/N x 10 Hz and M/N x 100 Hz are supported.

The device input reference frequency is programmed during initialization. The input reference frequency can be changed when the input reference is not the active source for a DPLL.

The device accepts an input reference with a maximum frequency of 180MHz through single-ended LVCMOS inputs or 900MHz frequency through differential inputs.

If the frequency of an input reference exceeds 400MHz, the reference must be internally divided by 2 before being fed to a DPLL (refer to ref_config registers).

Unused input references can be disabled to reduce power consumption.

6.1.2 Input Reference Monitoring

The input references are monitored by reference monitor indicators which are independent for each reference. They indicate abnormal behavior of the reference signal, for example; drift from its nominal frequency or excessive jitter.

6.1.2.1 Input Loss of Signal Monitor (LOS)

LOS is an external signal, fed to one of the GPIO[2:0] pins. LOS is typically generated by a PHY device whose recovered clock is fed to one of the reference inputs. The PHY device will generate a LOS signal when it cannot reliably extract the clock from the line. The user can set one of the GPIO pins as a LOS input by programming the corresponding GPIO register.

The GPIO inputs are read approximately every 10 ms to 25 ms.

6.1.2.2 Input Coarse Frequency Monitor (CFM)

The CFM monitors the input reference frequency for 100ms so that it can quickly detect large changes in frequency. The CFM limit for each input reference can be specified in the ref_cfm mailbox register with a threshold from 0.1% to 50%. If the CFM limit is exceeded, then CFM failure is declared for the corresponding reference.

For frequencies below 16 kHz, the CFM and SCM limits should be set to the same value for proper operation.

6.1.2.3 Input Precise Frequency Monitor (PFM)

The PFM block measures the frequency accuracy of the reference and updates the indicator bit. To prevent PFM from being falsely triggered by jitter/wander at the reference input, PFM averages frequency for approximately 10 seconds and indicates failure when the measured frequency exceeds the limit specified in the ref_pfm_disqualify register. To ensure an accurate frequency measurement, the PFM measurement interval is re-started if phase or frequency irregularities are detected by SCM or CFM. The PFM provides a level of hysteresis to prevent a failure indication from toggling between valid and invalid for input references that are on the edge of the acceptance range. The PFM limit should be set as described in ref_pfm_disqualify and ref_pfm_qualify mailbox registers. The resolution of these registers is 5ppb (0.005ppm).

When determining the frequency accuracy of the reference input, the PFM uses a local oscillator's frequency as its reference. When split-XO behavior is disabled the reference is the XO wired to the MCLKIN_P and OSCI pins. When split XO behavior is enabled the reference is the TCXO or OCXO for all regular reference inputs, and the reference is the XO for the TCXO/OCXO inputs.

In both cases the *absolute* PFM acceptance and rejection frequency offsets are shifted by the reference oscillator's frequency offset. This is accounted for in the acceptance and rejection requirements as described in Telcordia GR-1244 section 3.4.1. An example of the acceptance and rejection ranges for the Stratum 3 application (acceptance in the range of ±9.2 ppm, rejection at ±12 ppm given a ±4.6 ppm freerun frequency accuracy of a Stratum 3 reference oscillator) is shown in the figure below.

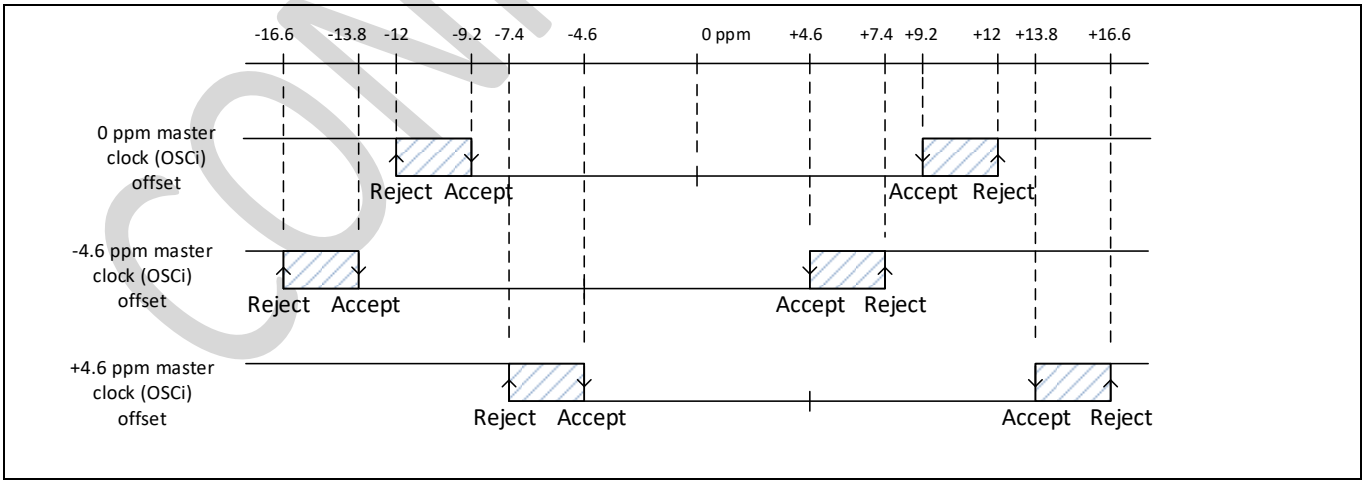


Figure 3 - Frequency Acceptance and Rejection Ranges

6.1.2.4 Input Single Cycle Monitor (SCM)

This detector measures the rising-edge-to-rising-edge and falling-edge-to-falling-edge periods of the input reference. If either exceeds the predefined SCM limit then an SCM failure is declared. The SCM limit for each input reference can be selected in the ref_scm mailbox register with standard settings from 0.1% to 50%. A new fine SCM option is also available that allows the SCM limit to be specified in ~1.25ns steps.

For frequencies below 16 kHz, the CFM and SCM limits should be set to the same value for proper operation.

For frequencies above 400MHz, SCM (and the GST) should not be used.

6.1.2.5 Input Step Frequency Monitor (SFM)

When enabled this monitor looks for a sudden frequency change on the input reference. If the input reference frequency changes in either direction by more than the configurable threshold in 1 second then an SFM failure is declared. The SFM limit for each input reference (ref_sfm mailbox register) can be any value from ±1ppm to ±250ppm (step 1ppm) with respect to the input reference frequency in the previous 1-second interval. Because this monitor has a measurement time of only 1 second it is useful for detecting sudden upstream clocking rearrangements more quickly than the PFM but for frequency errors smaller than the CFM or SCM can detect. An SFM failure sets the ref_mon_status_x.sfm status bit that can only be cleared by external software writing to the appropriate bit in the ref_sfm_clr_0_3 or ref_sfm_clr_4 registers.

6.1.2.6 Input Guard Soak Timer (GST)

When selected, the guard soak timer adds extra time to qualify and disqualify a reference. The default time to wait to qualify a reference is 200ms after the CFM and SCM limits have been satisfied. When disqualifying a reference, the time starts after a CFM or SCM failure is detected and before the reference is disqualified. The default disqualification time is 50ms. A PFM failure does not affect this timer.

When a reference is currently qualified and a failure occurs, the timer for disqualification is started. When the timer reaches the programmed threshold the reference is disqualified. If at any time between the starting of the timer and reaching the programmed threshold the input reference returns to a good state then the disqualification timer is reset.

When a reference is currently disqualified and the reference returns to good status, the timer for qualification is started. When the timer reaches the programmed threshold the reference is qualified. If at any time between the starting of the timer and reaching the programmed threshold the input reference returns to a failure state then the qualification timer is reset.

For frequencies above 400MHz, the GST should not be used because the single cycle monitor (SCM) will never be valid.

It is possible to mask an individual reference monitor from triggering a reference failure by setting the corresponding bits in the ref_mon_th_mask_x and ref_mon_tl_mask_x registers.

6.1.2.7 Input Frequency Reporting

The device reports the measured frequency of each input reference in Hz in the ref_freq_x registers. The value is a running average and therefore, for a stable input reference, become more accurate over time as averaging has a filtering effect on input noise.

The frequencies of the references can be read in Hz or in fractional frequency offset (ppb, ppm) vs. their user-specified nominal frequencies.

For debug it is often useful to read the reference frequencies in Hz. If, for example, a reference is expected to be 25MHz but a frequency read indicates the incoming clock signal is actually 1MHz then the problem is with the source of the clock signal and not with the device. This can be done by issuing a read command by setting ref_freq_cmd::latch to 01. The lsb of the ref_freq_x registers for this type of read is 1Hz.

When the nominal frequency of the incoming clock signal is correct, it is often more useful to read the reference's fractional frequency offset ([actual – expected] / expected) in ppm or ppb. This can be done by issuing a read command by setting ref_freq_cmd::latch to 10. The lsb of the ref_freq_x registers for this type of read is 2^{-32}.

All reference frequencies are latched at the same instant using the read frequency command.

All input reference frequency measurements use a local oscillator's frequency as its reference. When split-XO behavior is disabled the reference is the XO wired to the MCLKIN_P and OSCI pins. When split XO behavior is enabled the reference is the TCXO or OCXO for all regular reference inputs, and the reference is the XO for the TCXO/OCXO inputs.

Any frequency error in the local oscillator results in a similar error in input reference frequncy measurements. To get input reference frequency measurements relative to an input reference traceable to a Primary Reference Clock (PRC), system software can do the following:

1. Lock a DPLL to the known-good reference (KGR)
2. Read the DPLL's frequency offset relative to the local oscillator from dpll_df_offset_x (with dpll_df_ctrl_x::ref_ofst=0). Call this value DPLLvLO
3. Read an input reference's frequency offset relative to the local oscillator from the ref_freq_x register. Call this value REFvLO
4. Calculate REFvKGR = REFvLO – DPLLvLO

6.1.2.8 Oscillator Frequency Compensation for Input Monitors and Frequency Measurement

Whenever the frequency error of the master clock is known, that error can be mathematically compensated in the input reference monitors and frequency reporting. The master_clk_ofst register should be written according to the formula in the register description.

6.1.2.9 Input Reference Monitoring Interrupt Generation

A block diagram describing how reference monitoring blocks interact and how they generate an interrupt is shown in Figure 4. As can be seen from the block diagram the reference monitoring interrupt generation is separate from reference monitoring DPLL control which is described in the next section. The purpose of this is to allow user full flexibility during forced reference (manual) control.

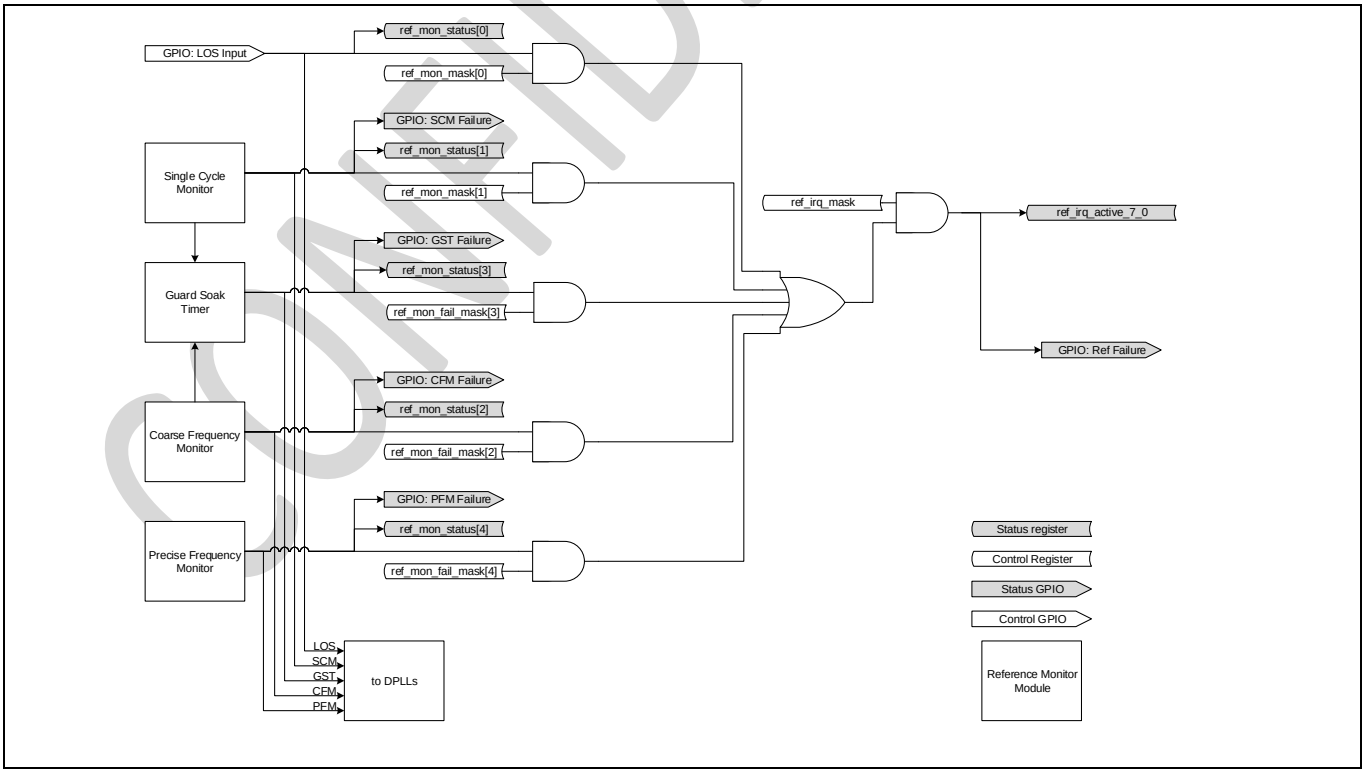


Figure 4 - Reference Monitoring Interrupt Generation

6.1.3 Input Gapped Clocks

The device supports locking to input gapped clocks.

6.1.4 Input Buffers

The device has ten single ended reference inputs and each reference input pair, REFxP and REFxN, can be used as a differential input for a total of five differential inputs. By default all reference inputs are single-ended. This can be changed by programming the ref_config mailbox register.

Each input pair can terminate two LVCMOS inputs, one differential input or two LVDS/LVPECL/HCSL inputs where only the positive signal of a differential pair is fed to the input pins, as shown in Figure 5. Figure 5c shows how to terminate two differential inputs by taking only the positive signal out of each differential pair. In this case the device's common mode voltage (VREF-PECL) is set at 55% of VDD so the common mode voltage has to be created with external biasing resistors (10kΩ to VDD in parallel with 12.7kΩ to VSS) as in Figure 5c which shows as an example how to terminate LVDS signals. An LVDS driver typically requires a DC path through the 100Ω termination resistor; therefore AC coupling has to be implemented after the termination resistor. For other differential formats the 100Ω resistor should be replaced with appropriate termination resistor(s): LVPECL with 127Ω and 82Ω resistors connected in Thevenin termination, source terminated HCSL without any termination required, and CML with 50Ω pullup resistors. It should be noted that common mode voltage is different for the regular differential input (Figure 5a) where it needs to be between 1V to 1.2V (LVDS standard).

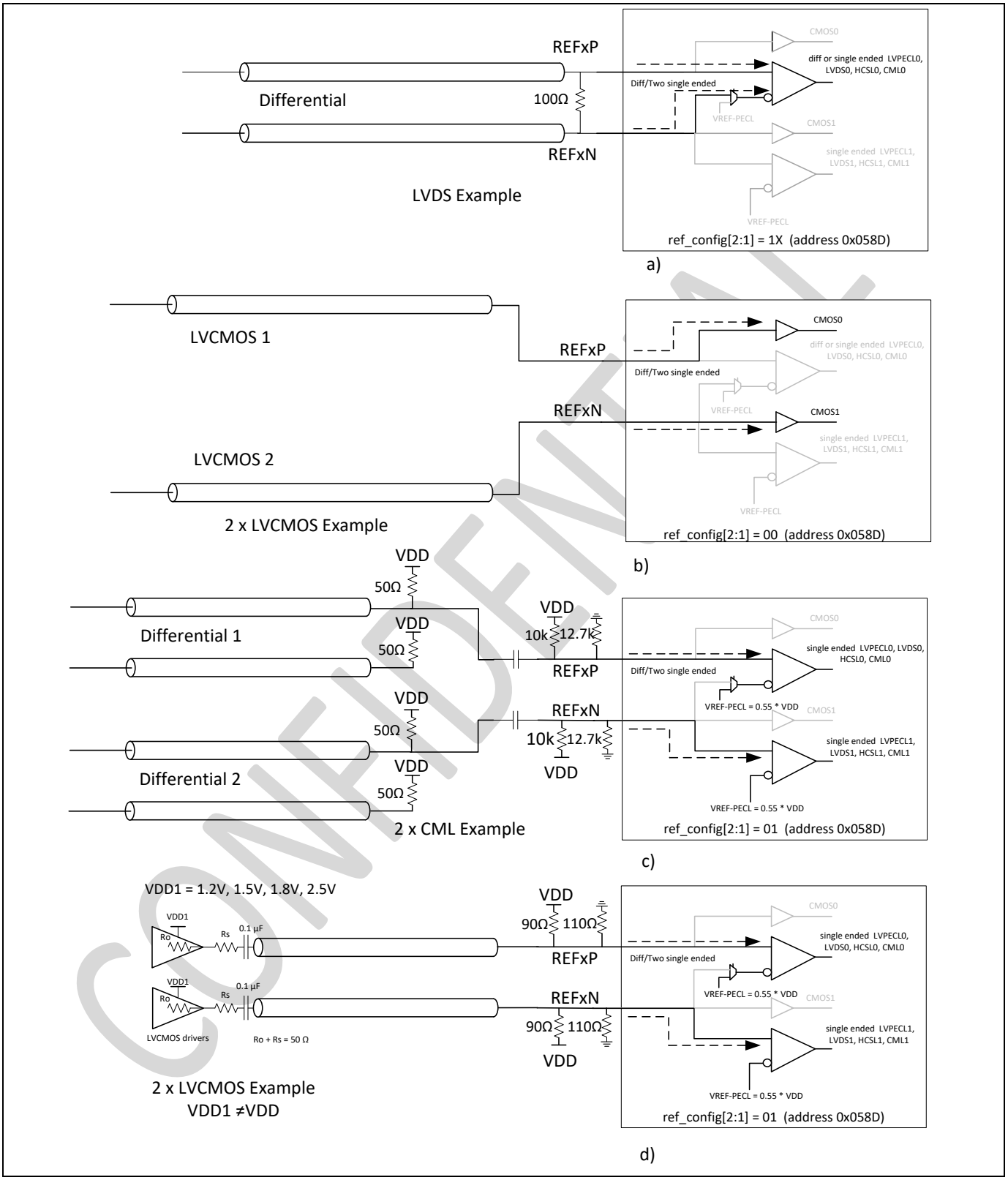


Figure 5 - Input Buffers and Termination

The input frequency range for differential signal is 1kHz to 900MHz. For single-ended LVCMOS inputs it is: 1kHz to 180MHz.

When terminating an LVPECL signal, it is necessary either to adjust termination resistors for DC coupling or to AC-couple the LVPECL driver because the device's differential receivers have different common mode (bias) voltage than typical LVPECL receivers. For a DC-coupled line, Thevenin termination (182Ω and 68Ω resistors for a 3.3V supply or 127Ω and 82Ω resistors for a 2.5V supply) provide 50Ω equivalent termination as well as biasing the differential receiver, as shown in the upper half of Figure 6 For an AC-coupled line, Thevenin termination with 127Ω and 82Ω resistors for 3.3V supply and 82Ω and 127Ω resistors for 2.5V supply should be used, as shown in the lower half of Figure 6. The values of the AC coupling capacitors will depend on the minimum reference clock frequency. The value of 10nF is good for input clock frequencies above 100MHz. For lower clock frequencies capacitor values will have to be increased accordingly.

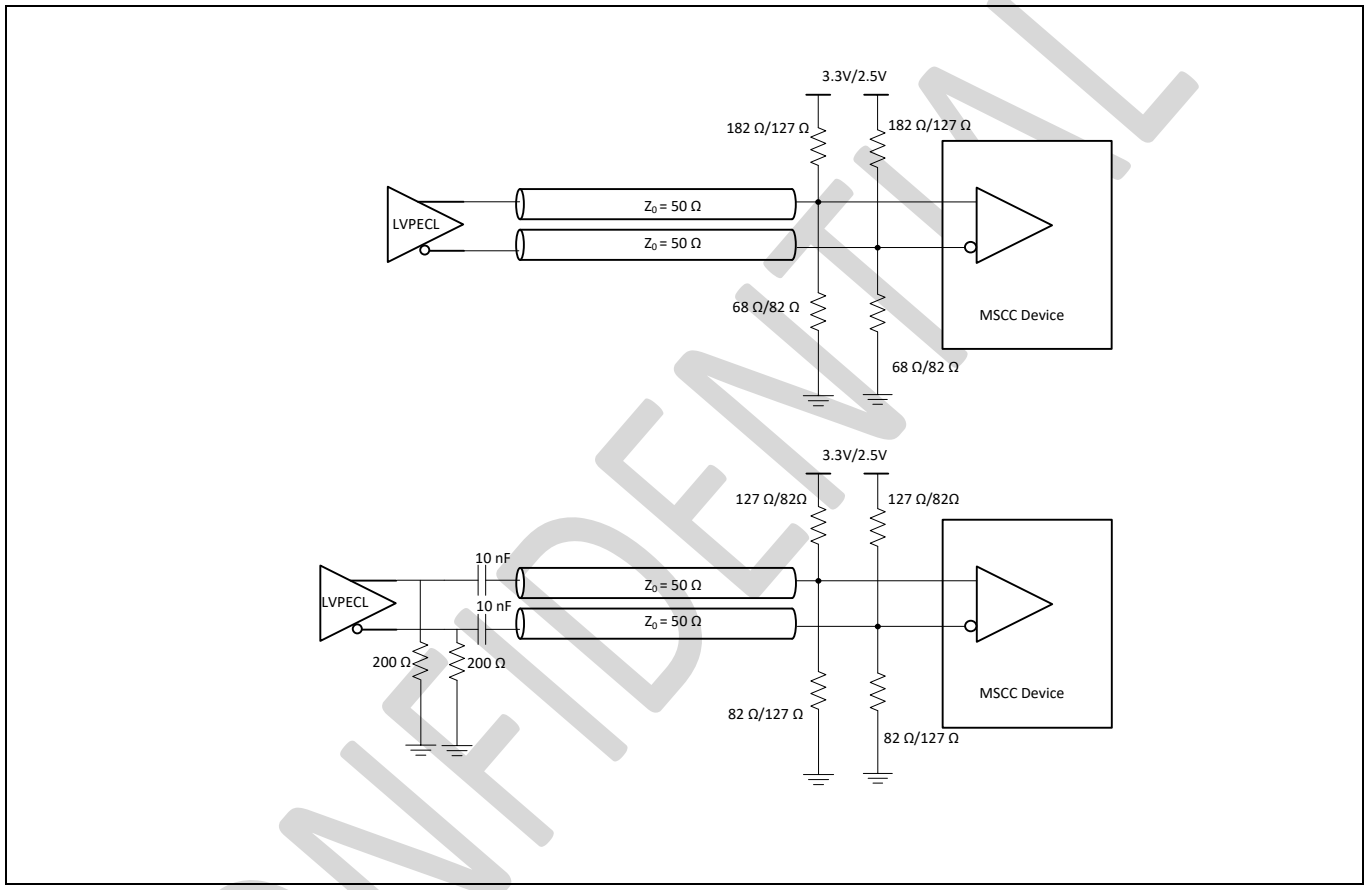


Figure 6 – Input Differential DC and AC Coupled LVPECL Termination

Terminations for DC and AC coupled LVDS lines are shown in figure below. Differential input biasing is provided by the LVDS driver in case of DC coupling whereas for AC coupling the DC bias is generated by 12kΩ and 8.2kΩ resistors. In both cases, the line is terminated with a 100Ω resistor.

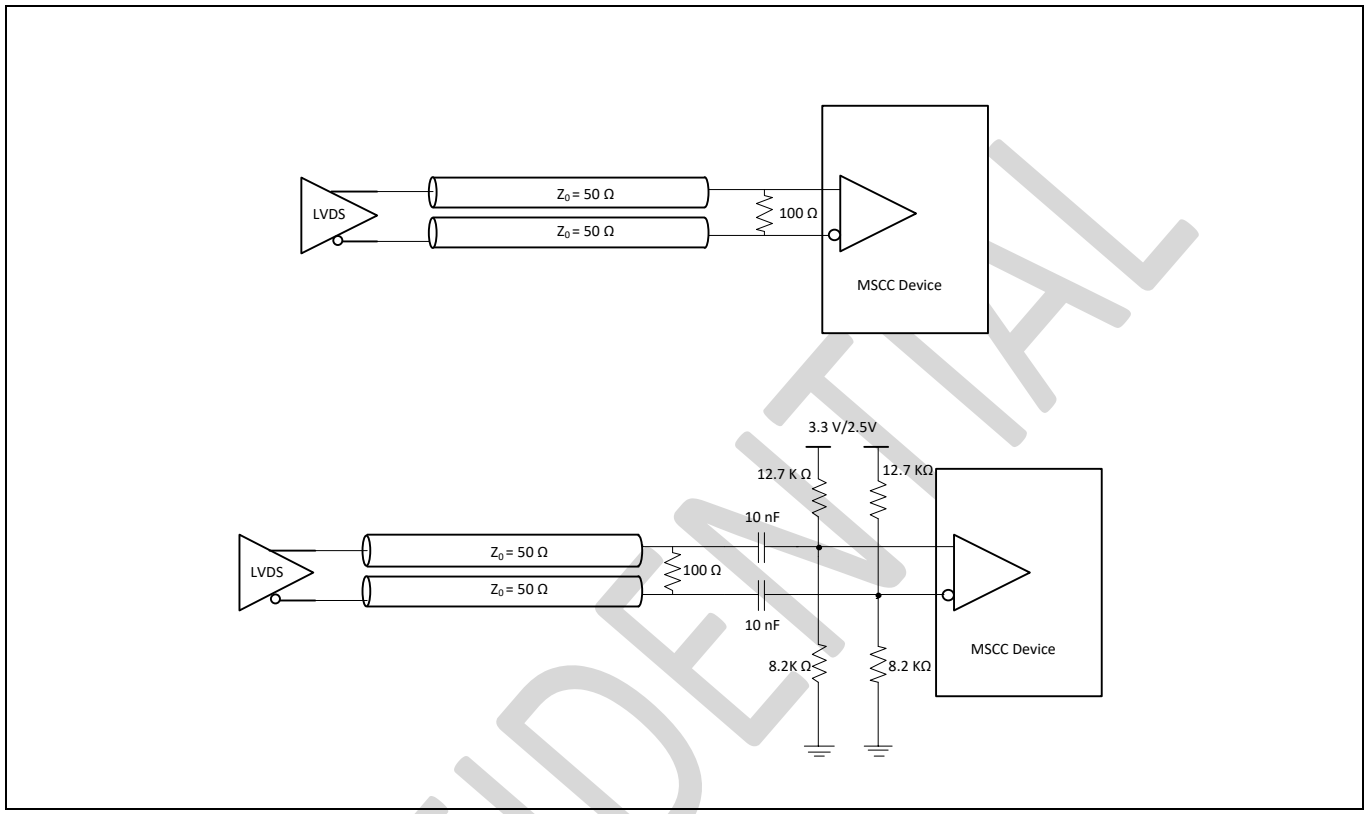


Figure 7 – Input Differential DC and AC Coupled LVDS Termination

The transmission line for an LVCMOS signal should be terminated at the source with a series resistor of approximately 22Ω as shown in the figure below. Consult the data sheet for the signal driver to determine its output impedance and set the series resistor to 50Ω minus the driver output impedance.

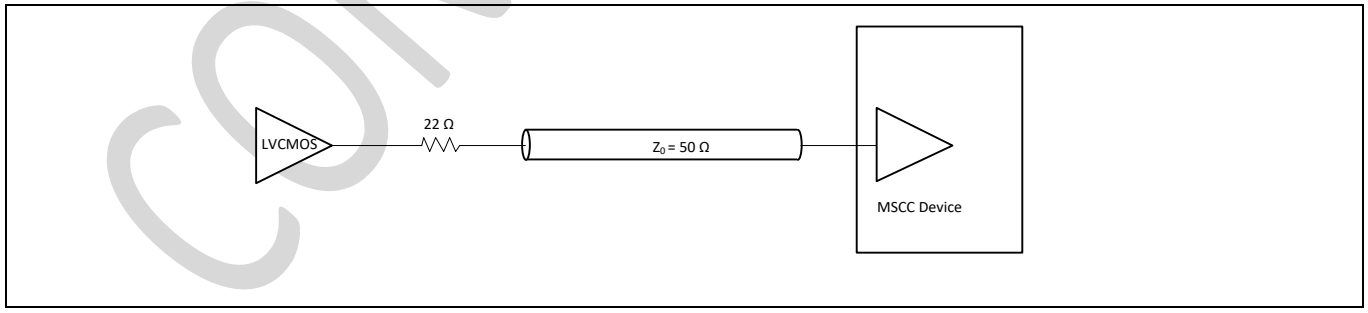


Figure 8 – Input Single Ended LVCMOS Termination

6.1.5 Input-to-Input Phase Offset Measurement

The device offers two input-to-input phase offset measurement tools. Each tool can be configured to measure the phase difference between any two signals among the ten REF signals and two HP-Synth feedback signals. The regular tool is used when both signals are ≥8kHz and coverges faster. The low-frequency tool is used when one or both of the signals is <8kHz.

For both tools the resolution of the measurement is 0.01ps. The frequencies of the two clocks do not have to be the same, but the clocks need to be frequency-locked, and the frequency of one must be an integer multiple of the other (for example 125MHz and 25MHz). The maximum phase offset that can be measured is equal to the smaller input clock period. For example, in the case of 125MHz and 25MHz inputs, the maximum phase offset that can be measured is 1/125MHz = 8ns.

The procedure for input-to-input phase offset measurement with the regular tool is as follows:

- Configure input references to be measured.
- Specify the input references (ref_idx_0 and ref_idx_1) in the pherr_meas_refsel register. The ref_idx_0 field should specify the higher-frequency input.
- Start the phase offset measurement by setting the enable bit (bit 0) in the pherr_meas_ctrl register.
- Request the current phase offset by setting the read bit (bit 0) in the pherr_read_rqst register and wait until the device toggles this bit to zero.
- Read the measured phase offset in the pherr_data register.

This feature is further described in section 6.5.4 in conjunction with output phase adjustment.

The procedure for input-to-input phase offset measurement with the low-frequency tool is as follows:

- Configure input references to be measured.
- Specify the input references (ref_idx_0 and ref_idx_1) in the pherr_low_freq_refsel register. The ref_idx_0 field should specify the higher-frequency input.
- Start the phase offset measurement by setting the enable bit (bit 0) in the pherr_low_freq_ctrl register.
- Request the current phase offset by setting the read bit (bit 0) in the pherr_read_rqst register and wait until the device toggles this bit to zero.
- Read the measured phase offset in the pherr_low_freq_data register.

Notes:

1. The pherr_read_rqst register is shared by the two tools.
2. In lab situations for testing this feature it is important to have a difference between master clock oscillator frequency offset and the frequency offset of the REFs. In other words, the REF signals should not be frequency-locked to the master clock signal. Convergence time and accuracy can be adversely affected if they are frequency-locked.
3. For the low-frequency tool, the measured value is not affected by the value of the ref_phase_offset_compensation mailbox register.
4. The three input signal format configurations (CMOS, single-ended LVPECL and differential, selected by ref_config::lvpecl_en and diff_en) have internal delays that differ by 100-300ps. High-accuracy, high-precision system designs are encouraged to use the same signal format for best measurements (and same drive strength and rise/fall times for the incoming signals).

6.1.6 Input-to-DPLL Phase Offset Measurement

Input-to-DPLL phase offset measurement allows user to read the phase offset between a DPLL's input reference and the DPLL's output. This feature can be used not only while the DPLL is locked to the input reference but also during pull-in. The resolution of this feature is 0.01ps and it is provided in 48-bit register dpll_phase_err_data_x (where x is the DPLL number).

6.1.7 Input Phase Adjustment

Input phase offset adjustment can be used to adjust the phase of input references with resolution of 1ps and maximum range of ±2.1ms. Each input reference has its own independent adjustment which can be programmed in the ref_phase_offset_compensation mailbox register.

6.2 Input-Output Special Formats

6.2.1 Input-Output Reference-Sync Pair

6.2.1.1 Input Operation

The loop bandwidth of a PLL needs to be at least 10 times lower than the frequency of the signal the PLL is locked to. Therefore when a PLL is locked to a 1Hz (1PPS) reference, its loop bandwidth needs to be less than 0.1Hz which requires use of very stable master clock such as a TCXO or OCXO.

The device can provide significant cost savings because it can synchronize to a reference clock of any frequency (typically higher than 1kHz) plus a sync signal (1PPS). This is referred to as a Ref-Sync pair. In this case the loop bandwidth of the PLL is governed by the input clock frequency which is presumably much higher than 1Hz (typically higher than 1kHz). This allows much wider loop bandwidth and faster lock time. Hence Ref-Sync pair behavior requires only a low-cost XO for the master clock of the DPLL. The timing diagram of the Ref-Sync pair is shown in the following figure.

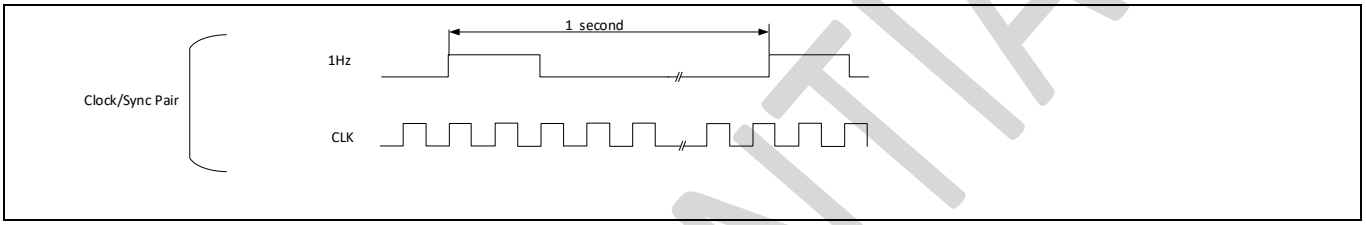


Figure 9 - Reference-Sync Pair

The device can synchronize to a Ref-Sync pair by enabling this feature for a particular reference input and by specifying which input has the Sync signal in the ref_sync mailbox register. Although Figure 9 shows the Sync pulse aligned to the rising edge of the clock, the device can be programmed in the ref_sync_misc mailbox register to lock to a Ref-Sync pair where the Sync pulse is aligned with the falling edge of the reference clock. Duty cycle of the Sync pulse does not have to be 50%. Any duty cycle is accepted as long as the width of the pulse is more than 5ns.

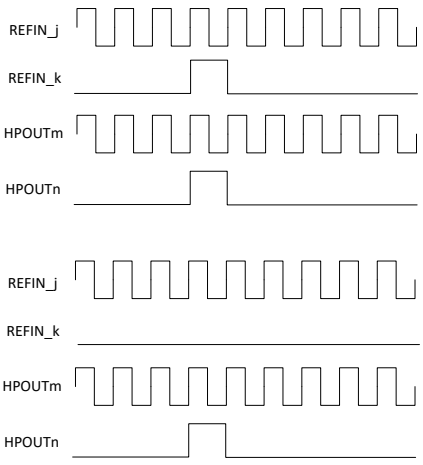
The device can terminate up to 5 Ref-Sync pairs (on 10 inputs) and each DPLL can synchronize to any of the Ref-Sync pairs. When an input is used as a Sync input, it is important to remove this reference from all automatic reference selection priority lists in the device (see section 6.3.2). If the Sync input is not qualified the Ref input is treated like a normal reference input. When a DPLL's selected reference is a Ref-Sync pair, it is assumed that output clock and sync phase should match input Ref-Sync phase, and the state of TIE-clear is ignored.

The timing of when a DPLL remeasures the phase of the Sync signal is configurable in the dpll_fp_first_realign and dpll_fp_realign_intvl registers. The Sync signal phase can be measured only once, two times with a programmable interval in between, repeatly at a programmable interval, or continuously. The dpll_fp_lock_thresh register specifies an optional Sync phase-lock criteria that is applied in addition to regular Clock phase-lock criteria.

Note that another DPLL can be configured to lock to only the Ref signal without considering the Sync signal if that other DPLL has dpll_ctrl_x::ignore_sync=1.

6.2.1.2 Output Operation

The device can also generate a Ref-Sync pair, and an example of output frame pulse alignment is shown in Figure 10.



If the input reference and sync pulse are present the output clock and sync pulse will be aligned to corresponding input signals

If the input pulse disappears, the output sync pulse will stay at the same position as before the input pulse disappeared. However, if the input pulse was not present from the beginning the output sync pulse will have arbitrary position.

Figure 10 - Output Frame Pulse Alignment

In this example, the reference is on REF_j and the sync pulse is on REF_k where j ≠ k. The output clock is on HPOUTm and the output sync pulse is on HPOUTn where m ≠ n. Any two input references can be used for Ref-Sync pairing, but the output clock and output frame pulse must be on the same synthesizer. Although Figure 10 shows single-ended outputs, the clock and sync pulse can be generated on differential or mixed (one single-ended and the other differential) outputs as well.

6.3 Digital Phase Locked Loop (DPLL)

The device supports one, two or three independent digital PLLs. All available DPLLs are enabled by default. Each DPLL can be enabled/disabled through the host registers.

6.3.1 DPLL Input Monitoring Masks

Each DPLL has its own reference switching (dpll_ref_sw_mask) and holdover (dpll_ref_ho_mask) mask mailbox registers which are used to prevent reference monitoring circuit form triggering the DPLL to switch references or to go into the holdover state. Please note that the GST bit should not be unmasked (GST trigger enabled) without unmasking either the SCM or the CFM or both bits. The reference switching mask is used only in the automatic control mode. In forced reference mode this register is ignored. The holdover mask register is active in both: automatic and forced reference modes.

Refer to the dpll_ref_prio_x mailbox registers.

6.3.2 DPLL Input Reference Priority

For each DPLL, each input reference can be assigned a local priority value (0 to 9) to allow system designers to specify the priority of each input references. The priorities are relative to each other, with lower numbers being the higher priority. Value “1111" disables the ability to select the reference (i.e., don’t use for synchronization). If two or more inputs are given the same priority number, those inputs are ranked by input number (i.e., REF0P is higher priority than REF0N). The default reference selection priority is equal to its reference number (i.e., REF0P is highest priority and REF4N is the lowest priority).

When two or more same-priority references are the highest-priority valid inputs, DPLL reference switching among those inputs is nonrevertive. But if a higher-priority reference becomes valid the DPLL will switch to the higher-priority reference (a revertive switch).

6.3.3 DPLL Input Pull-In, Hold-In Range

Pull-in/hold-in range is programmable in the dpll_range mailbox register. When the input reference frequency offset exceeds the pull-in/hold-in limit a notification can be generated. Refer to the **flhit** bits in the dpll_mon_status_x status registers.

6.3.4 DPLL Input Tolerance Criteria

Input tolerance indicates that the device tolerates certain jitter, wander and phase transients at its input reference while maintaining outputs within an expected performance and without experiencing any alarms, reference switching or holdover conditions. Input tolerance is associated with input reference source characteristics and the standards associated with the input reference type.

6.3.5 DPLL Input Advance and Delay

The DPLL phase may be advanced or delayed. There are two resolution-and-range options available. The fine option has resolution of 1ps and maximum change per update of ±2.1ms. The coarse option has resolution of 1ns and maximum change per update of ±2 seconds. This feature uses the dpll_tie_data_x and dpll_tie_ctrl_x registers. See also the dpll_tie and dpll_tie_wr_thresh mailbox registers. This phase adjustment feature acts as if the input signal is ahead or behind its true location by the programmed amount; therefore any changes to the phase adjustment are filtered through the DPLL bandwidth. Each advance or delay is relative to the current DPLL phase; therefore, changes can be commanded sequentially so that cumulative phase offset is unlimited. The value applied will be retained for all inputs and all modes of operation of the DPLL, and is only cleared by the user.

6.3.6 DPLL Phase Slope Limiter

A sudden phase change at the input of the DPLL can occur due to a reference rearrangement upstream in the timing chain. Some applications may be sensitive to fast phase transients and mitigating them with DPLL loop bandwidth reduction may not be possible. In such cases the DPLLs offer Phase Slope Limiter (PSL) behavior, which limits the DPLL output phase change per unit time to a specified value.

The phase slope limit can be adjusted in the dpll_psl mailbox register from 1ns/s to 65535ns/s. These low PSL values can be very useful to slow input clock phase transients. They can also be used to limit the frequency offset (compared with the master clock) since phase slope is in units of ns/s, which is equivalent to ppb (parts per billion). Care must be taken when setting a low PSL value that the oscillator is sufficiently stable. Care must also be taken when wander transfer is important to ensure that the PSL does not impact any expected input-to-output wander transfer behavior.

When the DPLL phase changing is limited by the PSL setting a notification can be generated. See the **pslhit** bits in the dpll_mon_status_x status registers.

6.3.7 DPLL Core Modes

The DPLL in the device support five modes: freerun, forced holdover, automatic, forced reference lock and numerically controlled oscillator (NCO). To lock the DPLL to a reference, automatic or forced reference mode should be used. In each of the locked modes, there are three states: acquiring, locked and holdover. The acquiring state is temporary state between the availability of a reference and the completion of the locking process. In the automatic mode, the DPLL may transition between the states depending on the availability of the references. In forced reference mode, the device will go into holdover if the reference selected is unavailable even if other references are available. The availability of a reference is determined by the reference qualification process. In the holdover mode or holdover state, the device provides output clocks which are not locked to an external reference signal, but are based on an estimate of the frequency during the previous time in the locked state. To force the DPLL into the holdover state, even with good references present, the forced holdover mode is used.

In addition, the DPLL can be put into the freerun mode. This is used when synchronization to an input reference is not required or is not possible. Typically, this is used immediately following system power-up. In the freerun mode, the device provides timing and synchronization signals which are based on the master clock frequency offset only, and are not synchronized to the input reference signals. The freerun accuracy of the output clock is equal to the accuracy of the master clock. Therefore if a ±20ppm freerun output clock is required, the master clock must also be ±20ppm.

The freerun mode:

- The DPLL has to generate all its output clocks based only on the device master clock.
- The DPLL will not lock or switch to a reference or go into holdover.
- The reference switch mask and the reference holdover mask are ignored.

The forced holdover mode:

- All references are ignored and the DPLL must go to holdover (at the frequency offset of the most recent selected reference)
- The reference switch mask and the reference holdover mask are ignored.

The forced reference lock mode:

- The DPLL will try to lock to the host-specified reference.
- The reference switch mask is ignored. No reference switching will be performed.
- If the holdover mask is set, then the DPLL switches to holdover if the selected reference fails.
- If the holdover mask is not set, then the DPLL attempts to lock to the selected reference, even if it is failing one of the reference monitors. The input frequency tracking will be limited by the pull-in/hold-in settings of the DPLL.

The automatic mode:

- Reference selection and holdover are automatically handled by the DPLL, based on the holdover and reference switch masks.
- If the reference switch mask is set, then a reference is selected based on availability and priority. If all enabled references are bad, then the DPLL enters holdover.
- If the holdover mask is set (and the reference switch mask cleared), then the DPLL switches to holdover on reference failure.
- If neither the reference switch nor the holdover masks are set, then the device continues to try to lock to a failed reference. The input frequency tracking is limited by the pull-in/hold-in settings of the DPLL.

The NCO mode:

- Similar to freerun mode but with frequency control. The output clock is the configured frequency with a frequency offset specified by the dpll_df_offset_x register. This write-only register changes the output frequency offset of the DPLL.

6.3.8 DPLL Status Indicators

The DPLL provides lock and holdover indicators in the dpll_mon_status_x::lock and ho bits. The DPLL also provides state information in the dpll_state_refsel_x::state field. The dpll_mon_th_sticky_x::state_ch sticky bits indicate when a DPLL state change has occurred.

6.3.9 DPLL Bandwidth (Jitter/Wander Transfer)

Loop bandwidth is set by programming the dpll_bw_fixed mailbox register for one of five loop bandwidths: 14Hz, 29Hz, 61Hz, 130Hz, 380Hz or 470Hz.

The DPLL locks to an input reference and provides a stable low-jitter output clock when the selected loop bandwidth is less than 1/30th the input reference frequency. As an example, a DPLL fed with a 19.44MHz reference can have loop bandwidth up to the maximum of 470Hz. For a 1kHz input reference, the DPLL loop bandwidth can be up to 14Hz. For an 8kHz reference the recommended maximum loop bandwidth is 61Hz.

6.3.10 DPLL Programmable Damping

The device supports programmable damping and phase gain using the dpll_damping mailbox register. A common value is the default value of 0x5 for gain peaking < 0.25dB.

6.3.11 DPLL Lock Time and Fast Lock Methods

Without enabling special fast lock behaviors, DPLL lock time is dependent on the DPLL loop bandwidth. The device has a lock time of less than 2s for loop bandwidths ≥10Hz and phase slope limit set to unlimited.

Lock and loss-of-lock thresholds are independently configurable for hysteresis if desired. Refer to dpll_phase_good, dpll_phase_bad and dpll_duration_good mailbox registers for more details.

6.3.12 DPLL Hitless Reference Switching

Referring to Table 21 the device is able to switch between input references with typical performance of 0.6 ns. Note that the device will transition through the holdover state when switching between input references. The switching

between input references may be fully automated when an old input reference fails (is disqualified) and a new input reference is available (is qualified).

6.3.13 DPLL Holdover Capability

6.3.13.1 Holdover Stability

The holdover accuracy depends on the core DPLL filter bandwidth as well as the additional holdover filter bandwidth and holdover storage delay.

Without considering the additional holdover filter bandwidth and storage delay, the following performance is typical:

- Initial accuracy of 2 ppb when the core DPLL filter bandwidth is ≥10Hz (line card applications)

6.3.13.2 Hitless Entry and Exit from Holdover

The device has typical entry-into-holdover MTIE of 0.6ns and typical exit-from-holdover MTIE of 0.6ns. Holdover entry and exit can be fully automated when a DPLL's input reference fails (is disqualified) and a new input reference is available (is qualified).

6.3.13.3 Additional, Post-DPLL Holdover Options

In addition to the holdover benefits gained through the DPLL filter bandwidth there is a separate holdover filter bandwidth and holdover storage delay controlled using dpll_ho_filter and dpll_ho_delay mailbox registers.

The post-DPLL holdover filter bandwidth may be set very narrow (as low as 1.7mHz) even when the core DPLL bandwidth is higher or the local oscillator is less stable.

The post-DPLL holdover storage delay is a history of the previous post-DPLL holdover filter bandwidth values. When the DPLL enters holdover it can use the most recently computed holdover value, or can go back in history to an earlier value. If a transient has just occurred on an input reference, causing the entry to holdover, it is beneficial to use a holdover value that was computed before the start of the transient. Therefore the holdover storage delay is generally set based on the expected types of transients on the input references. Care should be taken not to go too far back in time using the holdover storage delay register since the local oscillator frequency offset may have drifted since then due to temperature or ageing effects. Holdover storage values from more than one hour earlier are available.

6.3.13.4 Additional, Post-DPLL Holdover Filter Details

If the input reference is noisy (has jitter and wander), the quality of the holdover value depends on the input jitter and wander and on the loop bandwidth of the DPLL because the holdover value is taken from the DPLL low-pass filter. A narrower DPLL bandwidth gives better attenuation of the noise and more accurate holdover value. As explained previously, a narrower loop bandwidth require a more stable (more expensive) master clock and requires longer lock time. The post-DPLL holdover filter solves this problem because it is not part of the loop, as shown in the simplified block diagram in Figure 11, so it can be freely adjusted without affecting any loop parameters.

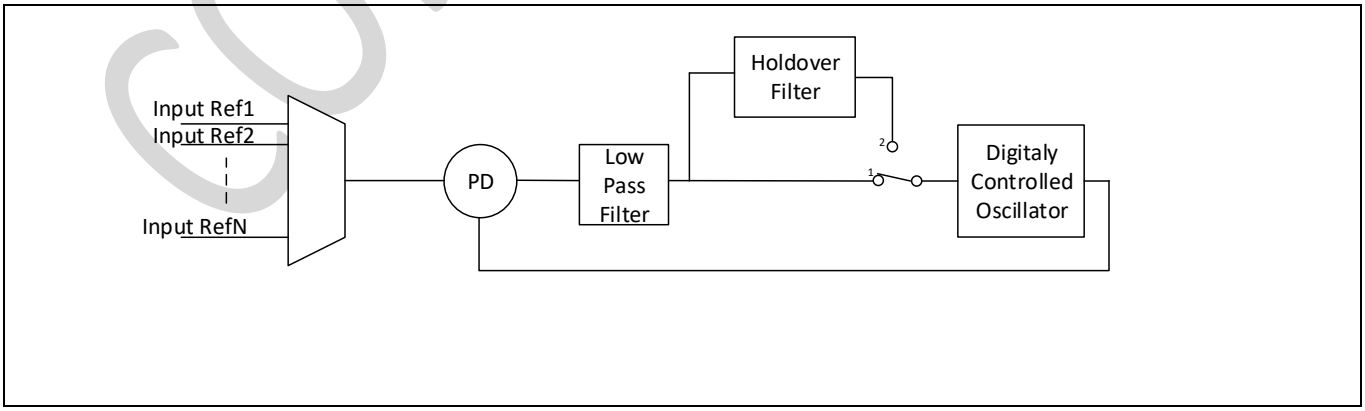


Figure 11 - Simplified Block Diagram of the Holdover Filter

The functionality of the holdover filter can be illustrated with the following example.

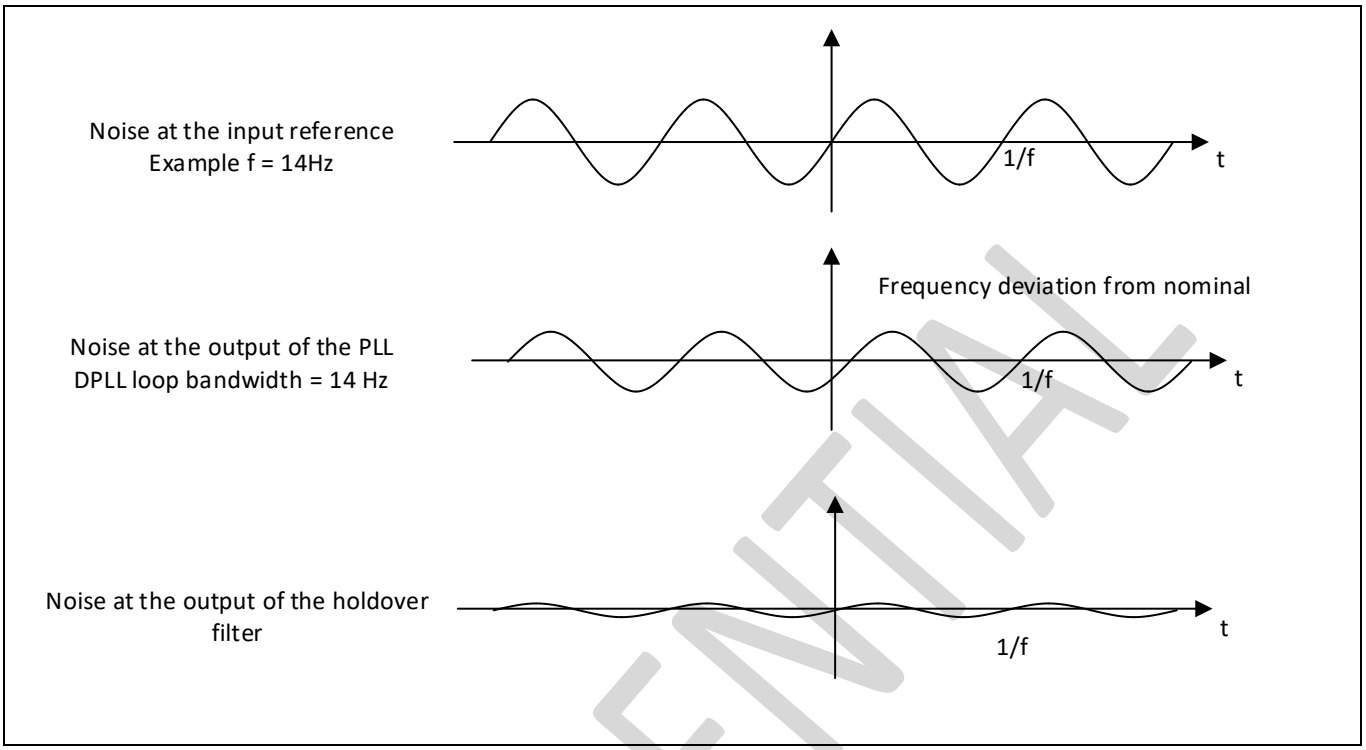


Figure 12 - Benefits of Holdover Filter

If the input reference is modulated by sinusoidal jitter, the instantaneous frequency of the input clock is also changed in a sinusoidal fashion. This is shown in the top plot of the Figure 12. If the loop bandwidth of the DPLL is set to 14Hz and if the jitter happens to have same frequency, the DPLL passes the jitter with only 3dB attenuation and the output frequency deviates 3dB less than the input frequency (middle plot). If the DPLL goes into holdover state its output frequency can equal the nominal frequency only at the zero crossing of the sine wave, which is highly unlikely to occur. Hence assuming the jitter frequency is constant, the holdover value depends on the amplitude of the input jitter—the higher the amplitude, the lower the holdover accuracy. Deviation of the frequency can be calculated as

$$Dfm = \pi * fm * ja \text{ [in UIpp]}$$

where the fm is frequency of the jitter (14 Hz in our example) and ja is jitter amplitude in unit intervals .

If an additional filter (holdover filter) is added which is not part of the loop then the DPLL can filter jitter for the holdover value without affecting the loop performance. Then when the DPLL goes into holdover it takes its value from the holdover filter, which is much more accurate (closer to nominal) than the value from the loop filter.

When the holdover filter is enabled the Digitally Controlled Oscillator will use the value from the holdover filter (position 2 of the switch in Figure 11). The holdover filter bandwidth can be set in the dpll_ho_filter mailbox register. If the value in this register is 0x00 the holdover filter is not used and the holdover value in this case is based on the DPLL loop bandwidth.

For applications that use DPLL NCO mode for IEEE 1588 timing over packet, the dpll_ho_filter::nco_en bit specifies whether the holdover filter is updated while the DPLL is in NCO mode.

The dpll_mon_status_x::ho_ready bit indicates when the internally calculated holover average is ready.

6.3.13.5 User Holdover Compensation Support

System software can provide advanced holdover compensation schemes to reduce the effects of temperature variation or ageing of the local oscillator while in the holdover state or holdover mode. To support this operation the DPLL has several support tools.

During locked operation the user can read the core DPLL frequency offset from the dpll_df_offset_x register. With this information system software can learn the ageing characteristics of the local oscillator. Additionally, when combined with a temperature sensor, system software can learn the temperature characteristics of the local oscillator. System software then writes the desired frequency offset to the dpll_df_manual_x register. This offset is then used in freerun, forced holdover mode, holdover state, and NCO mode. .

6.3.14 DPLL Output Frequency Offset and Master Clock Frequency Adjustment

The device allows adjustment of the output frequency of each DPLL with resolution of 2^{-48} (~0.0000035 ppb) and allowable range of ±1% (±0.4% for DPLL0 when GP-Synth is enabled) as shown in Figure 13. It also supports fine DPLL frequency adjustment to compensate for any known master XO frequency error. The output frequency adjustment (Δf_0 in the figure, dpll_df_offset_x register) would typically be used in applications such as IEEE-1588 plus SyncE hybrid mode where the DPLL is locked to Synchronous Ethernet but the output frequency needs to track IEEE-1588. Since Synchronous Ethernet and IEEE-1588 are generally not sourced from the same primary reference clock, there will be a small and variable frequency offset between them which must be constantly updated. The frequency offset can be programmed through device registers, or one of the GPIOs can be configured to cause the device to add or subtract a pre-programmed frequency offset each time the GPIO pin is toggled.

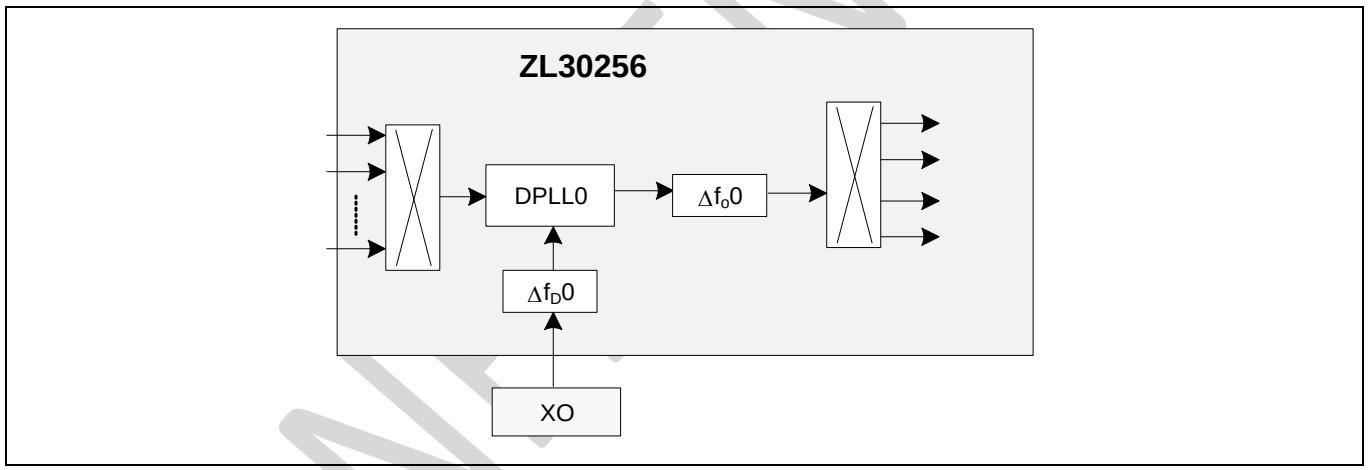


Figure 13 - Output and XO Frequency Adjustment

The master clock frequency adjustment (Δf_D in the figure, dpll_df_manual_x register) would be used in applications which need to constantly adjust for variation of XO frequency with temperature or aging. This feature works in conjunction with offset from nominal frequency offset feature described in section 6.8.2.3. The major differences are that the nominal frequency offset feature should be done only once at power-up and it applies to all DPLLs. The fine DPLL master clock frequency adjustment can be done any time during normal operation and it is available on a per-DPLL basis. The changes should be very small to reduce disturbances at the output. If a bigger frequency step is required it should be split into multiple smaller frequency steps applied over time.

6.3.15 DPLL Supervision & Management

6.3.15.1 DPLL Management Mode Comparisons

In unmanaged mode of operation, the DPLL state (locked, holdover, acquiring) and the selected reference are automatically set by the internal state machine of the device. It is based on availability of a valid reference and on the reference's selection priority.

In managed mode of operation, the DPLL state and the selected reference are manually set by the user.

The device allows for smooth transitions between managed and unmanaged modes. Hence if the DPLL is in managed mode, for example locked to REF1P reference, and then is switched to unmanaged mode of operation, the state machine keeps the DPLL locked to REF1P and it does not force reference switching to any other reference unless REF1P is disqualified by its input monitors.

Each DPLL has its own independent state control and reference selection state machine.

6.3.15.2 DPLL Unmanaged Mode

The unmanaged mode combines the functionality of the normal state with automatic holdover and automatic reference switching. In this mode, transitioning from one state to another is controlled by the device internal state machine.

The on-chip state machine monitors the input reference status bits and makes decisions to perform reference switches or to change to the holdover state.

The reference switching state machine is based on the internal clock monitoring of each of the available input references and their priorities.

The state machine selects a reference source based on its priority value defined in a control register and the current availability of the reference. If all the references are available, the reference with the highest priority is selected; if this reference fails, the next highest priority valid reference is selected, and so on.

In unmanaged mode, the state machine only reacts to reference failure indicators and performs reference switching anytime one of the following conditions takes place, assuming they are not masked with their corresponding mask bits:

- LOS detected a failure and refswitch mask LOS is at logic “1”
- SCM detected a failure and refswitch mask SCM is at logic “1”
- CFM detected a failure and refswitch mask CFM is at logic “1"
- GST is triggered and refswitch mask GST is at logic “1"
- PFM detected a failure and refswitch mask PFM is at logic “1"
- SFM detected a failure and refswitch mask SFM is at logic “1"

In unmanaged mode, the device automatically selects a valid reference input. If the current reference used for synchronization fails, the state machine switches to another valid reference. If all the available references fail, then the device enters the holdover state under one of the following conditions if they are not masked with their corresponding mask bits:

- LOS detected a failure and holdover mask LOS is at logic “1”
- SCM detected a failure and holdover mask SCM is at logic “1”
- CFM detected a failure and holdover mask CFM is at logic “1"
- GST is triggered and holdover mask GST is at logic “1"
- PFM detected a failure and holdover mask PFM is at logic “1"
- SFM detected a failure and holdover mask SFM is at logic “1"

In unmanaged mode of operation, the state machine automatically recovers from holdover when the conditions to enter holdover are not present.

The reference selection is based on reference priority. The current active reference for each DPLL can be read from DPLLx Reference Selection Status register.

If neither the reference switch nor the holdover masks are set, then the device continually tries to lock to a failed reference subject to the limits of the pull-in/hold-in range.

6.3.15.3 DPLL Managed (Manual) Mode

In managed mode, the device does not auto-select among the reference inputs. Instead the user specifies which reference input to use, and if that reference fails the DPLL enters the holdover state without switching to another reference.

The user (external software) monitors the device status bits. Based on the status information, the user makes a decision to force holdover or to perform a reference switch. In managed mode the active reference input is selected

based on reference selection control bits. If the user sets the device to lock to a failed reference, the device stays in holdover and only locks to that reference if it becomes valid.

The state machine only reacts to failure indicators and goes into holdover under one of the following conditions if they are not masked with their corresponding mask bits:

- LOS detected a failure and holdover mask LOS is at logic “1”
- SCM detected a failure and holdover mask SCM is at logic “1”
- CFM detected a failure and holdover mask CFM is at logic “1"
- GST is triggered and holdover mask GST is at logic “1"
- PFM detected a failure and holdover mask PFM is at logic “1"
- SFM detected a failure and holdover mask SFM is at logic “1"

The state machine automatically recovers from holdover when the conditions to enter holdover are not present.

Time-critical transitions for entry into holdover and exit from holdover are managed by the internal state machine. A change of the reference select bits triggers an internal state transition into holdover and then an exit into Normal state and locking to the new reference.

If neither the reference switch nor the holdover masks are set, then the device continually tries to lock to a failed reference subject to the limits of the pull-in/hold-in range.

6.3.16 DPLL Jitter/Wander Generation

The wander generation is dominated by the high-pass filter characteristics of the local oscillator above the programmed DPLL filter bandwidth.

The jitter generation performance is provided in section 11.

6.3.17 DPLL Frequency and Phase Reporting

The frequency offset of the DPLL vs. the master clock oscillator can be read from the dpll_df_offset_x register by initiating a read using the fields of the dpll_df_ctrl_x register with read_sem=1 and ref_ofst=0. The frequency offset of the DPLL vs. the input reference it is tracking can be read from the dpll_df_offset_x register using the fields of the dpll_df_ctrl_x register with read_sem=1 and ref_ofst=1. The resolution of both values is 2^{-48} (~0.0000035ppb or 3.5E-15). In addition, for precise DPLL-to-DPLL comparisons, the frequences of all DPLLs can be latched at the same instant using dpll_freq_cmd::latch.

The phase offset of the DPLL vs. the input reference it is tracking can be read from the dpll_phase_err_data_x register. The resolution of this register is 0.01ps.

6.4 Input-Output Conversion

6.4.1 Input-to-Output and Output-to-Output Phase Alignment

6.4.1.1 Phase Alignment Control

When the output clock is locked to a jitter-free and wander-free input clock, input-to-output latency is expected to have a typical error of 0ns. This is accomplished within the device using advanced, automatic precision input-output alignment routines at initialization. See Table 16 for alignment specifications.

Additionally, there are user-accessible phase adjustments that allow for input-to-output and output-to-output latency corrections to compensate for PCB load delay, as detailed in section 6.3.5 DPLL Input Advance and Delay and section 6.6.3 HPOUT Phase Alignment and Phase Adjustment.

Note that when the device is initially configured with DPLL(s) in NCO mode, GPOUTs are not automatically aligned with HPOUTs. An easy work-around for this is to initially configure the device with DPLL(s) in any other mode, for example freerun. The device then aligns all outputs. Then system software can change DPLL mode to NCO as needed. Note that when outputs are 1Hz or 0.5Hz the alignment step can take several seconds; therefore, system software should wait at least 5 seconds before changing DPLLs to NCO mode.

6.4.1.2 External Feedback

The PLL architecture allows for implementation of an external feedback path where one of the output clocks signals is externally wired to one of the reference inputs. External feedback automatically maintains tight alignment of output phase with reference input phase, dynamically compensating for changes in PCB trace delay and external buffer delay caused by changes in temperature.

It is recommended that the DPLLs be fully configured before enabling external feedback. If a synthesizer or DPLL in the external feedback path need to be reconfigured, disable external feedback before changing the parameters and then enable external feedback again.

For the DPLL0-Synth0 path, external feedback is enabled by first wiring a GPOUT pin (or a signal downstream of a GPOUT pin, such as a fanout buffer output) to a REF pin, then specifying the REF pin in ext_fb_sel::ref and then setting the ext_fb_ctrl::en bit.

For Synth1 and Synth2, regardless which DPLL each is connected to, external feedback is enabled by first wiring an HPOUT pin or a signal downstream of a GPOUT pin, such as a fanout buffer output) to a REF pin. Then the HPOUT pin must be specified in hp_fb_out_x::idx and the REF pin must be specified in hp_fb_ref_x::idx. Finally external feedback is enabled by setting hp_ctrl_x::ext_fb=1. By default the device configures the feedback REF frequency and the feedback HPOUT medium-speed and low-speed dividers for a low frequency (typically a few hundred kHz). After external feedback is enabled, the settings for REF and HPOUT should not be changed. Note that only an HPOUT internally connected to the synthesizer's integer divider can be used. Using an HPOUT internally connected to the synthesizer's fractional divider is not supported.

If the feedback frequency chosen by the device causes an unwanted spur in output signal phase noise plots or has any other undesirable effect, the HPOUT medium-speed divider and low-speed divider values can be set manually before enabling external feedback. The hp_fb_msdiv_x and hp_fb_lsdiv_x registers provide this capability.

Before choosing external feedback, the user should consider the input-output alignment performance that the device achieves without external feedback, shown in Table 16. Because the device uses an inside-the-package feedback similar to external feedback, input-output alignment performance without external feedback is as good as with external feedback, especially for Synth1 and Synth2. Therefore Microsemi recommends external feedback only for special cases, such as when the outputs of a fanout buffer downstream of the device should be aligned with an input reference.

Note that external feedback can only be implemented with regular clock signal. It cannot be implemented with a Ref-Sync pair.

6.4.2 Rate Conversion Function and FEC Support

The DPLL provides frequency up-scaling and down-scaling functions. It has the ability to switch from normal rate (before FEC is negotiated) to FEC rate and vice versa.

The DPLL supports:

Simple rate conversion (e.g. take in 19.44MHz and create 255/238 FEC SONET/SDH clock of 666.51MHz)

Double rate conversion (e.g. take in 19.44MHz and create FEC 10GbE clock of 644.5313MHz, which is 66/64 x 625MHz, or create 690.5692MHz which is 255/238 x 66/64 x 625MHz)

The following is just an example of the frequencies that can be supported at the input and output independently (many more frequencies can be supported):

GbE:

- 25MHz
- 125MHz

XAUI (chip-to-chip interface, which is a common chassis-to-chassis interface):

- 156.25MHz or x2 or x4 version

OC-192/STM-64:

- 155.52MHz or x2 or x4 version
- 155.52MHz x 255/237 (standard EFEC for long reach) or x2 or x4 version
- 155.52MHz x 255/238 (standard GFEC for long reach) or x2 or x4 version

10 GbE:

- 156.25MHz which is 125MHz x 10/8 or x2 or x4 version
- 155.52MHz x 66/64 or x2 or x4 version

Long reach 10GE might require the following frequencies with simple rate conversion: (156.25MHz x 255/237) and (156.25MHz x 255/238).

The following frequencies with double rate conversion: (155.52MHz x 66/64 x 255/237) or (155.52MHz x 66/64 x 255/238) and (156.25MHz x 66/64 x 255/238) or (156.25MHz x 66/64 x 255/238). Also, user can use x2 or x4 version of the listed frequencies.

When using a DPLL path for frequency conversion, some specific scenarios have behavior limitations. The scenarios are:

(a) from an integer multiple of 0.25Hz to a frequency that is not an integer multiple of 0.25Hz

(b) from a frequency that is not an integer multiple of 0.25Hz to an integer multiple of 0.25Hz

(c) between two frequencies that are not integer multiples of 0.25Hz and are not integer multiples of a common divisor.

There are two behavior limitations in these scenarios. First, the frequency conversion is not exactly 0ppm. Instead there is a very small frequency error in the range of 3E-16 to 3E-18. Second, when hitless switching is disabled (dpll_ctrl_x::tie_clear=1) the DPLL path will not have input-to-output phase alignment and will have a large phase change during reference switching. The size of the phase change is on the order of 10us by default (due to ~100kHz internal DPLL feedback frequency) but can be reduced to the order of 100ns (with register settings to increase internal DPLL feedback frequency to ~10MHz). Contact Microsemi timing applications support for help with these register settings. Such limitations on one DPLL do not affect the other DPLLs if the other DPLLs are not configured for one of the scenarios (a) through (c) above.

6.4.3 Mapping DPLLs to Synthesizers

One DPLL may be mapped to more than one Synthesizer concurrently. The following combinations are supported:

- DPLL0 to Synth0, DPLL1 to Synth1, DPLL2 to Synth2
- DPLL0 to Synth0 and Synth1, DPLL2 to Synth2
- DPLL0 to Synth0 and Synth2, DPLL1 to Synth1
- DPLL0 to Synth0, DPLL1 to Synth1 and Synth2
- DPLL0 to Synth0 and Synth1 and Synth2

Synth0 is always connected to DPLL0. The source for Synth1 is specified by hp_ctrl_1::dpll and the source for Synth2 I specified by hp_ctrl_2::dpll. If the source for a synthesizer is changed during runtime it is best to disable and then re-enable the synthesizer by clearing then setting the hp_ctrl_x::en bit after the change to maintain proper input-to-output phase alignment.

Phase alignment of very low frequency HPOUT signals (<1kHz) when SynthX is connected to DPLLY (X≠y) is not supported.

6.5 Output Frequency Synthesizers

The frequency synthesis engines can generate any clock frequency in a range as shown below:

- Synthesizer 0: 730MHz to 950MHz
- Synthesizer 1: 3.715GHz to 4.18GHz
- Synthesizer 2: 3.715GHz to 4.18GHz

The frequency for Synth0 is programmed as B * K * M / N Hz where B, M and N are 16-bit registers and K is a 24-bit register.

The frequency for Synth1 and Synth2 is programmed as B * M / N where B, M and N are 32-bit registers.

As shown in Figure 1, Synth1 and Synth2 each have an integer divider and a fractional divider. The integer divider can divide the Synthesizer frequency by integers 4 to 15 plus half-divides of 4.5, 5.5, 6.5 and 7.5. The integer divider is the lowest jitter path. The fractional dividers are described in section 6.5.2.

6.5.1 Synth0 Frequency Offset

The frequency offset of the general-purpose synthesizer (Synth0) can be adjusted with resolution of 2^{-48} (~0.0000035 ppb or 3.5E-15) in the gp_df_offset_manual register. The adjustment affects the frequency offset of both GPOUT0 and GPOUT1 outputs.

6.5.2 Synth1 and Synth2 Fractional Dividers

The fractional divider performs zero ppm non-integer frequency conversion. The fractional divider jitter performance varies from about 0.4ps to nearly 2ps rms (12kHz to 20MHz band) depending on exact frequency plan. For most frequency plans the fractional divider jitter is <1ps rms.

The output clock from the fractional divider has good phase noise on rising edges but worse phase noise on falling edges and can have non-50% duty cycle. Applications that only use clock signal rising edges can use the fractional divider's output clock directly. For applications that care about 50% duty cycle and/or the phase noise of both rising edges and falling edges, the fractional divider should be further divided by the per-output medium-speed dividers. The per-output low-speed dividers can be used to further divide if very low frequencies are needed.

The maximum output frequency for the fractional divider is $f_{VCO}/10$. Including the need for a post-divide in the medium-speed divider, the maximum frequency for a 50% duty-cycle output clock signal is $f_{VCO}/20$. The minimum output frequency for the fractional divider is $f_{VCO}/32$. The output frequency of the fractional divider is specified in the hp_fdiv_base_x, hp_fdiv_num_x (numerator) and hp_fdiv_den_x (denominator) registers. The fractional output divider is enabled by setting hp_ctrl_x.fdiv_en.

6.5.3 NCO Behavior in the Fractional Dividers

System software can steer output frequencies derived from the fractional output divider with high resolution by manipulating the divider's hp_fdiv_base_x value. This steering creates a fractional frequency offset (in ppb or ppm) for the output of the synthesizer's fractional output divider that is different than the fractional frequency offset of the synthesizer's integer divider (example: Synth0 integer divider output is 0ppm and Synth0 fractional divider output can be manipulated to be 0ppm or -4ppm or +10ppb or any desired offset).

(Note: Fractional frequency offset (FFO) is defined as (actual_frequency – nominal_frequency) / nominal_frequency. FFO is a unitless number but is typically expressed in parts per billion (ppb), parts per million (ppm) or percent.)

6.5.4 Synth0 Phase Adjustment

The Synth0 synthesizer can advance or delay simultaneously the outputs connected to it with 1ps step size. The size of the phase shift is programmed in the gp_fine_shift register. The maximum phase offset that can be programmed in one step is 10ns. This procedure can be repeated so that cumulative phase offset is unlimited. To mitigate disturbance of the device receiving the output clock signal during the output phase adjustment, the user can specify how long it takes for the phase to move to its final position in the gp_fine_shift_intvl register. This prevents discrete phase steps at the output. Instead the phase moves gradually to its final position.

6.5.5 Synth1 and Synth2 Phase Adjustment

Each of Synth1 and Synth2 can have their phase advanced or delayed with 1ps step size and 2.1ms range in the hp_fine_shift_x register. Unlike the Synth0 phase adjustment described in 6.5.4, successive phase adjustment values written to this register are not cumulative. (In other words, writing phase X to this register and then writing phase Y results in final phase of Y, not X+Y.) The entire phase adjustment is provided to device logic immediately when written, but the rate of change of phase is subject to DPLL loop dynamics.

6.5.6 Synth1 and Synth2 Lowest Jitter Using Fractional Output Divider Feedback

Synth1 and Synth2 achieve their lowest possible output jitter (50-60fs rms lower) when configured with APLL feedback through the fractional output divider. Figure 14 illustrates this configuration, which is hereafter referred to as FDIV feedback.

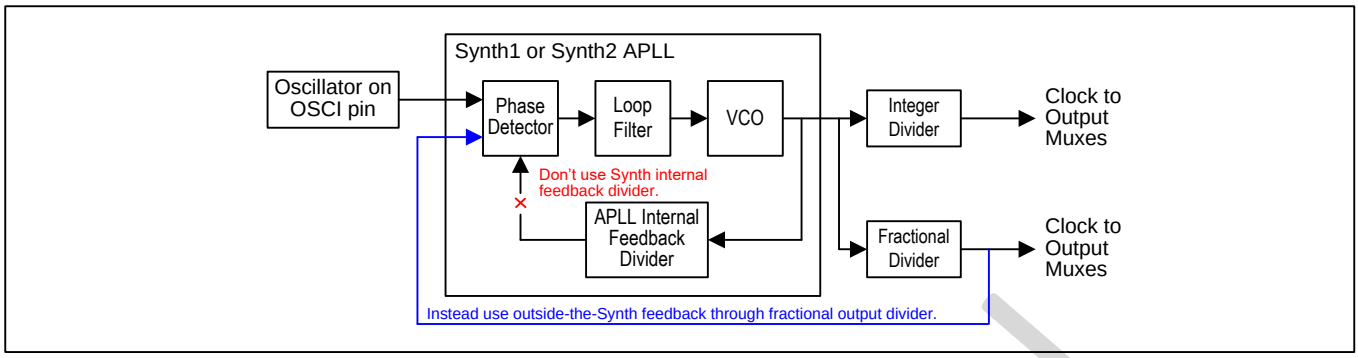


Figure 14 - Synthesizer FDIV Feedback Concept

There are costs to using this configuration, since it uses internal resources in unexpected ways. When FDIV feedback is enabled for Synth1, the Synth1 APLL feedback path is through the fractional output divider and the HPOUT0 output divider. Therefore HPOUT0 and HPOUT1 (same source bank as HPOUT0) must be configured for frequencies related to the master clock oscillator. Since such frequencies are not typically useful in system designs, HPOUT0 and HPOUT1 typically are not useable when Synth1 is configured for FDIV feedback. Figure 15 shows Synth1 FDIV feedback.

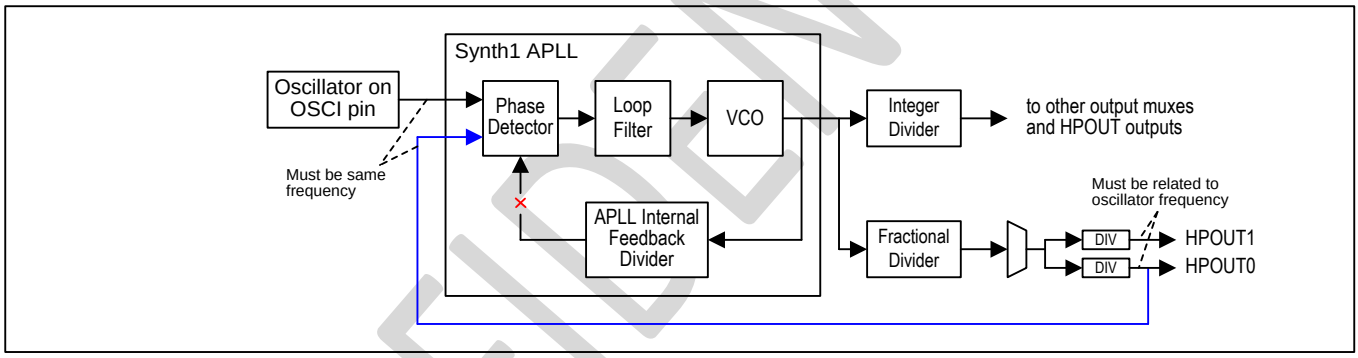


Figure 15 - Synth1 FDIV Feedback

When FDIV feedback is enabled for Synth2, all eight HPOUT outputs are useable, but Synth1 loses it internal feedback to DPLL1. Therefore if Synth1 is needed for the application then the DPLL1-Synth1 path must be configured for external feedback from an HPOUT output connected to Synth1 to a REF input configured to be DPLL1's feedback input. See section 6.4.1.2 for details about external feedback. Synth1 cannot be internally connected to DPLL0 when FDIV feedback is enabled for Synth2.

When FDIV feedback is used and the master clock oscillator is ≤ 50MHz, the OSCI clock doubler (section 6.8.2.2) should be enabled for lowest possible output jitter. When the master clock oscillator is >50MHz the OSCI clock doubler cannot be used. But in FDIV feedback configuration, a Synth input doubler can and should be enabled for lowest possible output jitter. Note that it is invalid to enable both the OSCI doubler and the Synth input doubler at the same time.

FDIV feedback is enabled by enabling and configuring the fractional output divider (section 6.5.2) and then setting hp_ctrl_x.fdiv_fb_en=1. The Synth input doubler is enabled by setting hp_ctrl_x.fdiv_fb_dbl=1.

6.5.7 Synth0 Disable/Enable Procedure for Specific Register Changes

When Synth0 is enabled in an application, the following register fields should not be changed except by using a specific procedure: gp_ctrl::en, gp_freq_base, gp_freq_mult, gp_freq_m, gp_freq_n and central_freq_offset.

The procedure is as follows:

1. Disable GP-Synth0 by setting gp_ctrl::en=0.

2. Change any of the registers listed above.
3. Read 0x80002600, change bits 21:19 to 0x2, and write the updated value to 0x80002600.
4. Wait at least 25ms
5. Change bits 21:19 to 0x0 and write the updated value to 0x80002600.
6. Enable GP-Synth0 by setting gp_ctrl::en=1.

Reading and writing these 0x8000xxxx addresses requires the procedures described in ZLAN-728.

6.6 HPOUT Output Clocks

The device has eight HPOUT output clock signal pairs that each can be locked to Synth1 integer divider, Synth1 fractional divider, Synth2 integer divider or Synth2 fractional divider. Each output pair has individual divider, enable and signal format controls. In CMOS mode each signal pair can become two CMOS outputs, allowing the device to have up to 18 output clock signals (16 HPOUT plus 2 GPOUT). Also in CMOS mode, the HPOUTxN pin can have an additional divider allowing the HPOUTxN frequency to be an integer divisor of the HPOUTxP frequency (example: HPOUT3P 125MHz and HPOUT3N 25MHz). The outputs can be aligned relative to each other, and the phases of output signals can be adjusted dynamically with high resolution.

6.6.1 HPOUT Enable, Signal Format, Voltage and Interfacing

To use an output, the output driver must be enabled in hp_out_ctrl_x::format and the per-output dividers must be enabled by setting the **en_x** bit in hp_out_en. The per-output dividers include the medium-speed divider, the low-speed divider and the associated phase adjustment/alignment circuitry and start/stop logic.

Each output pair can be disabled or configured as LVDS, LVPECL, HCSL, HSTL, or one or two CMOS outputs. When an output is disabled it is high impedance, and the output driver is in a low-power state. In CMOS mode, the HPOUTxN pin can be disabled, in-phase or inverted vs. the HPOUTxP pin. The clock to the output driver can inverted. The CMOS/HSTL output driver can be set to any of four drive strengths.

When the output driver is in LVDS mode. V_{OD} is forced to 400mV. V_{CM} can be configured in the hp_out_diff_x register, but the default value is typically used to get V_{CM}=1.23V for LVDS.

When the output driver is in programmable differential mode the output swing (V_{OD}) can be configured in the hp_out_diff_x register to any value from 300mV to 900mV in 100mV steps, and the common-mode voltage can be configured to any voltage from 1.0V to 2.1V in 0.1V steps. Together these fields allow the output signal to be customized to meet the requirements of the clock receiver and minimize the need for external components. By default, programmable differential mode provides 800mV LVPECL signal swing with a 1.23V common mode voltage. This gives a signal that can be AC-coupled (after a 100Ω termination resistor) to receivers that are LVPECL or that require a larger signal swing than LVDS. The output driver can also be configured for LVPECL output with standard 2.0V common-mode voltage.

In both LVDS mode and programmable differential mode the output driver requires a DC path between HPOUTxP and HPOUTxN for proper operation. This DC path is often a 100Ω termination resistor placed as close as possible to the receiver inputs to terminate the differential signal as shown in Figure 16 parts a) and b). If the receiver requires a common-mode voltage that cannot be matched by the output driver then the POS and NEG signals can be AC-coupled to the receiver after the 100Ω resistor as shown in Figure 16 part b). For the case where the receiver already has a 100Ω termination resistor *and* AC-coupling is required, a resistor can be placed between HPOUTxP and HPOUTxN as close as possible to the device to provide the required DC path as shown in Figure 16 part c). This resistor can be 100Ω for double-termination of the signal. Or it can be up to 200Ω in which case the signal is single-terminated by the 100Ω resistor at the receiver and the signal amplitude at the receiver is larger than the double-termination case.

HCSL mode requires a DC path through a 50Ω resistor to ground on each of HPOUTxP and HPOUTxN.

Outputs are grouped into four power supply banks, VDDO_0_1 through VDDO_6_7, to allow CMOS or HSTL signal swing from 1.5V to 3.3V for glueless interfacing to neighboring components. Each power supply bank has two outputs.

If an output is configured for HSTL mode then a 1.5V power supply voltage is typically used to get a standards-compliant HSTL output. Note that LVDS, LVPECL and HCSL signal formats must have a power supply of 2.5V or 3.3V.

Figure 16 shows recommended interface circuitry for the various output signal formats.

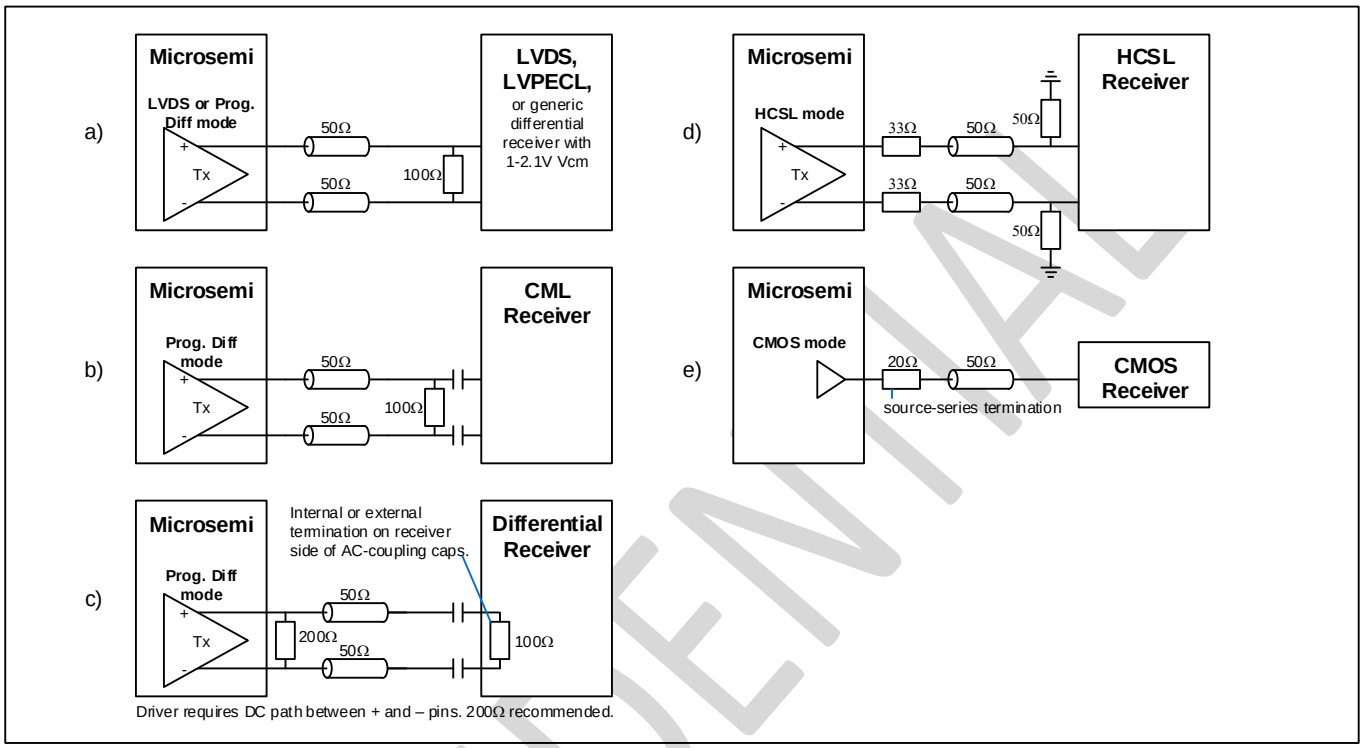


Figure 16 - Example External Components for Output Signals

6.6.2 HPOUT Frequency Configuration

The frequency of each output is determined by the configuration of the source synthesizer, the synthesizer's output dividers, and the per-output dividers. Each bank of outputs can be connected to either Synth1 or Synth2 integer divider or fractional divider usuing the appropriate bank_xy field in hp_out_mux.

Each output pair has two output dividers, a 7-bit medium-speed divider (hp_out_msdiv_x) and a 25-bit low-speed output divider (hp_out_lsdiv_x). These dividers are in series, medium-speed divider first then output divider. These dividers produce signals with 50% duty cycle for all divider values including odd numbers. The low-speed divider can only be used if the medium-speed divider is used (i.e. medium-speed divider set to divide by ≥ 2). The maximum input frequency for the medium-speed divider is 750MHz.

Since each output has its own independent dividers, the device can output families of related frequencies that have a synthesizer divider frequency as a common multiple. For example, for Ethernet clocks, a 625MHz clock from a synthesizer integer divider can be divided by four for one output to get 156.25MHz, divided by five for another output to get 125MHz, and divided by 25 for another output to get 25MHz. Similarly, for SDH/SONET clocks, a 622.08MHz clock can be divided by 4 to get 155.52MHz, by 8 to get 77.76MHz, by 16 to get 38.88MHz or by 32 to get 19.44MHz.

Two Different Frequencies in 2xCMOS Mode

When an output is in 2xCMOS mode it can be configured using the **neglsd** bit in the hp_out_lsctrl_x register to have the frequency of the HPOUTxN clock be an integer divisor of the frequency of the HPOUTxP clock. Examples of where this can be useful:

- 125MHz on HPOUTxP and 25MHz on HPOUTxN for Ethernet applications

- 77.76MHz on HPOUTxP and 19.44MHz on HPOUTxN for SONET/SDH applications
- 25MHz on HPOUTxP and 1Hz on HPOUTxN

An output can be configured to operate like this by setting the low-speed divider value to HPOUTxP_freq / HPOUTxN_freq and enabling the two-frequency mode. Here are some notes about this two-frequency configuration option:

- In this mode only the medium speed divider is used to create the HPOUTxP frequency. The low-speed divider is then used to divide the HPOUTxP frequency down to the HPOUTxN frequency. This means that the lowest HPOUTxP frequency is the synthesizer's integer divider or fractional divider frequency divided by 128.
- An additional constraint is that the medium-speed divider must be configured to divide by 2 or more.

6.6.3 HPOUT Phase Alignment and Phase Adjustment

All outputs that are enabled (hp_out_en::en_x=1) and configured to follow Synth1 (using hp_out_mux fields) are aligned automatically when Synth1 is enabled (hp_ctrl_1::en set to 1). Similarly all outputs configured to follow Synth2 are aligned automatically when Synth2 is enabled. An output that is configured and enabled after its synthesizer is enabled is not aligned to the other outputs from that synthesizer to avoid phase hits on the other outputs. Alignment of HPOUT outputs from a synthesizer can be forced by setting hp_ctrl_x::en low and then high.

The phase of an output signal can be shifted by 180° by inverting the polarity. In addition, the phase can be adjusted using the hp_out_shift_x register in units of bank source clock cycles. For example, if the bank source clock is 625MHz (from Synth1 integer divider for example) then one bank source clock cycle is 1.6ns, the smallest phase adjustment is 0.8ns, and the adjustment range is ±5.6ns.

In addition to the per-output controls mentioned above, the phase of all outputs derived from the same synthesizer can be controlled with 1ps resolution. See section 6.5.5 for details.

In addition, one or more HPOUT outputs that are 1PPS can have their phase adjusted up to 1UI using the phase_step_ctrl, phase_step_data and phase_step_mask_hp registers. The phase_step_data register is a signed integer with units of medium-speed divider (MSDIV) periods. The maximum phase step amplitude is limited to ±49% of a UI, i.e. ±0.49s.

Note that outputs internally connected to the Synth's integer divider are tightly aligned, but outputs internally connected to the Synth's fractional divider are aligned with a phase offset. To tightly align outputs from the fractional divider, system software can measure this phase offset using input-vs-input phase measurement (section 6.1.5) and corrected it by temporarily changing the fractional divider value and then changing it back. For example, a 10ns phase change can be accomplished by changing the fractional divider value by 10ppb for one 1 second, or by 1ppb for 10 seconds.

6.6.4 HPOUT Duty Cycle / Pulse Width Adjustment

For output frequencies less than or equal to 141.666MHz, the duty cycle of the output clock can be modified using the hp_out_width_x register. This behavior is only available when medium-speed divider is dividing by 2 or more and low-speed divider is dividing by 3 or more. By default the output clock is 50%. Otherwise the clock signal is a pulse with a width 1 to 255 medium-speed divider output clock periods. For normal polarity outputs, the pulse is high and the signal is low the remainder of the cycle. For inverse polarity outputs, the pulse is low and the signal is high the remainder of the cycle.

Note that duty cycle adjustment is done in the low-speed divider, and both HPOUTxP and HPOUTxN can be configured to follow either the medium-speed divider or the low-speed divider. When an output is configure for two-frequency mode the HPOUTxN pin has duty cycle adjustment but the HPOUTxP pin does not. This allows a higher-speed 50% duty cycle clock signal to be output on the HPOUTxP pin and a lower-speed frame/phase/time pulse (e.g. 2kHz, 8kHz or 1PPS) to be output on the HPOUTxN pin at the same time.

Note that duty cycle adjustment moves the output clock rising edge. There are cases where signals with non-50% duty cycles cannot be rising-edge aligned.

An output configured for CMOS or HSTL signal format should not be configured to have a duty cycle with high time shorter than 2ns or low time shorter than 2ns.

6.6.5 HPOUT Clock Start/Stop and Squelch

6.6.5.1 HPOUT Start/Stop

Output clocks can be stopped high or low or high-impedance. One use for this behavior is to ensure “glitchless” output clock operation while the output is reconfigured or phase aligned with some other signal.

Each output has an hp_out_stop_x control register with fields to control this behavior. The stop mode field specifies whether the output clock signal stops high, low, or high-impedance. The stop source field specifies the source of the stop signal. Options include control bits or one of the GPIO[8:5] pins. The device is configurable to simultaneously stop and start any subset of the HPOUT outputs.

When the stop mode is Stop High and the stop signal is asserted, the output clock is stopped after the next rising edge of the output clock. When the stop mode is Stop Low and the stop signal is asserted, the output clock is stopped after the next falling edge of the output clock. When the output is stopped, the output driver can optionally go high-impedance. Internally the clock signal continues to toggle while the output is stopped. When the stop signal is deasserted, the output clock resumes on the opposite edge that it stopped on. Low-speed output clocks can take long intervals before being stopped after the stop signal goes active. For example, a 1 Hz output could take up to 1 second to stop.

When the output polarity is inverted the output stops on the opposite polarity that is specified by the stop mode field.

Generally the medium-speed divider must be dividing by 2 or more for this function to operate correctly since medium-speed divider set to 1 bypasses the start-stop circuits.

When medium-speed divider is set 1, the device does provide a “stop high then go high-impedance” behavior that can be used to make outputs high-impedance, but the action won’t necessarily be glitchless. To use this behavior to get “stop *low* then go-impedance” behavior, the output can be set to inverse polarity.

Note that when the output is configured for two-frequency mode the start-stop logic is bypassed for the HPOUTxN pin, and HPOUTxN may not start/stop without glitches.

Each output has a status register (hp_out_mon_status_x) with a **stopd** status bit that indicates stopped or not stopped and sticky registers (hp_out_th_sticky_x and hp_out_tl_sticky_x) with bits to indicate when **stopd** has changed states.

6.6.5.2 HPOUT Squelch

Each HPOUT can be configured to be squelched (stopped) under a user-selectable condition. When the appropriate bit is set in hp_squelch_mask the output participates in the squelch. The squelch is caused by the setting of the out_squelch_ctrl::en bit.

This **en** bit can simply be set by system software to squelch outputs, but the more interesting capability is when this bit is controlled by a GPIO. As an example, to squelch outputs when DPLL0 loses all inputs and enters holdover configure the device as follows:

- Configure GPIO0 as a status that follows dpll_mon_status_0.ho by setting gpio_select_0::page=2, gpio_select_0::offset=0x18, gpio_select_0::bit=1 and gpio_config_0::ctrl=011.
- Wire GPIO0 to GPIO1
- Configure GPIO1 to control out_squelch_ctrl::en by setting gpio_select_1::page=4, gpio_select_1::offset=0x4C, gpio_select_1::bit=0 and gpio_config_1::ctrl=010.

6.7 GPOUT Output Clocks

The GPOUT0 and GPOUT1 output clock signals are single-ended outputs that are always locked to Synth0. Each GPOUT has its own divider, enable, polarity, phase and pulse width (duty cycle) controls.

6.7.1 GPOUT Phase Adjustment

Each GPOUT may be advanced or delayed in steps of 1 VCO cycle. This feature has a range of 1 UI per update and unlimited lifetime updates. All adjustments are aligned to the Synth0 VCO clock.

Per output phase step is initialized by programming the phase_step_ctrl register and the step size and the selected output(s) are specified in the phase_step_data and phase_step_mask_gp registers. The phase steps are cumulative and unlimited. The device saves information of the phase offset up to ±1/2 period of the output clock. For example if the output clock is 100MHz (10ns period) and if the phase step is 11ns, a later read of the phase gives a value of 1ns. Therefore information about additional delay must be saved in system software (if needed).

In addition to the per-output controls mentioned above, the phase of Synth0 can be controlled with 1ps resolution to affect the phase of both GPOUT pins. See section 6.5.4 for details.

6.7.2 GPOUT Clock Polarity

The device supports programming per-output clock polarity of the GPOUTx pin using the **polarity** bit in the gp_out_ctrl_x register.

In the following scenario, the output clock polarity feature is not supported without additional configuration:

- The synthesizer output is configured with a post-divider value ≤ 24

To correctly enable the output clock polarity the user must first configure the output frequency and desired polarity with post divider value > 24, and then second set the post divider to the proper value ≤ 24.

6.7.3 GPOUT Duty Cycle / Pulse Width Adjustment

The default output clock duty cycle is 50/50. The user may program the output pulse width (duty cycle) of the GPOUTx pin in the gp_out_width_x register. This may be useful for 1PPS outputs when a duty cycle other than 50/50 is required, such as setting the pulse high time to 1UI of a companion clock.

6.7.4 GPOUT Output Drivers

The GPOUT single-ended driver (CMOS) supports a maximum clock frequency of 180MHz. GPOUT outputs should be terminated at the source with 22Ω resistors as shown in Figure 17.

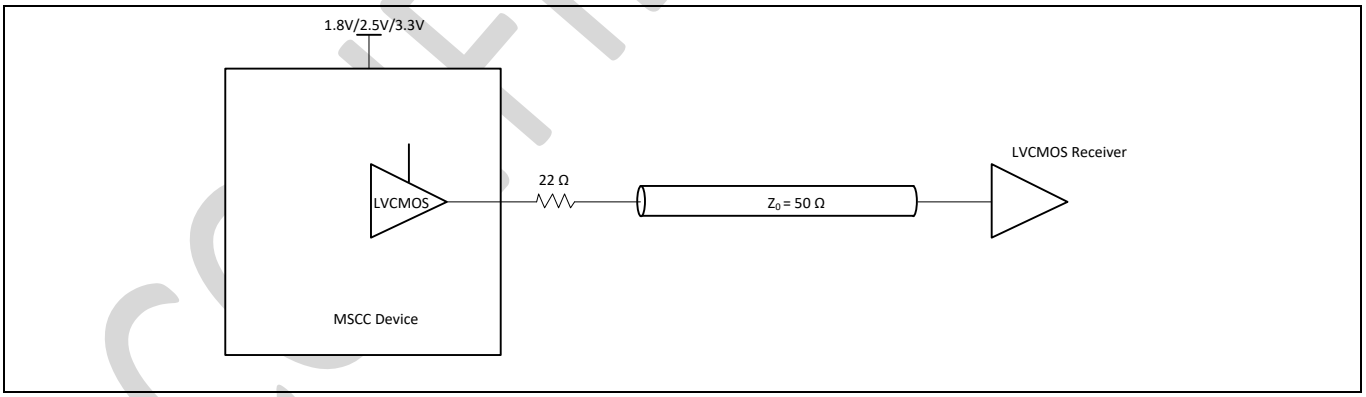


Figure 17 - Example External Components for GPOUT Driving CMOS Receiver

6.7.5 GPOUT Output Squelch

Each GPOUT can be configured to be squelched (stopped) under a user-selectable condition. When the appropriate bit is set in gp_squelch_mask the output participates in the squelch. The squelch is caused by the setting of the out_squelch_ctrl::en bit.

This **en** bit can simply be set by system software to squelch outputs, but the more interesting capability is when this bit is controlled by a GPIO. See section 6.6.5.2 for an example configuration where outputs are squelched when DPLL0 loses all inputs and enters holdover.

6.8 System Clock

The device internal system clocks are generated from the device master clock signal wired to the OSCI and MCLKIN_P pins.

6.8.1 Master Clock Interface

When using a clock oscillator as the master timing source, connect the oscillator's output clock to the OSCI and MCLKIN_P pins. Recommended wiring is XO to source-series termination resistor and then short-as-possible equal-length traces from the resistor to the OSCI and MCLKIN_P pins.

The jitter on output clock signals depends on the phase noise and frequency of the oscillator. For the device to operate with the lowest possible output jitter, the external oscillator should have the following characteristics:

- Phase Jitter: less than 0.1ps RMS over the 12kHz to 5MHz integration band
- Frequency: The higher the better, all else being equal

Several vendors offer XO products with the required jitter. Three good choices from Vectron are the 114.285MHz VCC1-1537-114M285, the 49.152MHz VCC1-1545-49M152, and the 48MHz Vectron VCC1-9003-48M0000. Each of these is a standard VCC1 XO but with a max jitter specification of 0.1ps RMS over the 12kHz to 5MHz integration band.

6.8.2 Master Clock Frequency Selection

The frequency of the master clock on the OSCI and MCLKIN_P pins is specified by the MC0 and MC1 pins.

6.8.2.1 Nominal Master Clock Frequencies

The device supports nominal XO frequencies of 25MHz, 50MHz and 125MHz. The 25MHz and 50MHz nominal frequencies can have offsets down to -5% to support 24.576MHz and 49.152MHz, for example. The 125MHz nominal frequency can have offsets down to -9% to support 114.285MHz, for example.

6.8.2.2 OSCI Clock Doubler

The device provides an optional clock doubler for the path from the OSCI pin to Synth1 and Synth2. Generally this doubler should be enabled when the signal on the OSCI pin is 50MHz or lower. This doubles the input clock frequency to Synth1 and Synth2 which reduces their random jitter with little or no adverse effect for most frequency plans. Note that the doubler causes a spur at the OSCI frequency. If this spur falls within the output jitter band of interest then the doubler can be disabled if needed.

6.8.2.3 Offset from Nominal Frequencies

Offset from nominal is programmed by writing the central_freq_offset register. For example, when using 24.576MHz or 49.152MHz oscillators, the user should maintain the default value of the central_freq_offset register (0x046AAAAB).

For a 114.285MHz oscillator the value should be 0x180072B0.

For 25MHz, 50MHz and 125MHz oscillators the central_freq_offset register should be programmed to 0x00000000.

6.9 Power Supply

The device power supply can be split into five distinct groups. The Synth1 and Synth2 synthesizers and dividers are powered from VDDH=3.3V and VDDL=1.8V. All HPOUT outputs can be independently powered with 1.5V, 1.8V, 2.5V or 3.3V on the VDDO supplies. (The 1.5V and 1.8V options only apply for CMOS and HSTL output signal formats). All the other device inputs and outputs are powered from VDD=3.3V supply. The device core is powered from a 1.8V supply on the VDD_DRI pin.

6.9.1 Power Up/Down Sequence

Due to the multi-power-supply nature of the device, some I/Os have parasitic diodes between a lower-voltage supply and a higher-voltage supply. When ramping power supplies up or down, care must be taken to avoid forward-biasing these diodes because it could cause latchup. Two methods are available to prevent this. The first method is to place a Schottky diode external to the device between the lower-voltage supply and the higher-voltage

supply to force the higher-voltage supply to be within one parasitic diode drop of the lower-voltage supply. The second method is to ramp up the higher-voltage supply first and then ramp up the lower-voltage supply.

Important Note: The voltages on VDDL, VDD_DRI, and all VDDOx pins must not exceed VDDH. Not complying with this requirement may damage the device.

6.9.2 Power Supply Filtering

Jitter levels on the output clocks may increase if the device is exposed to excessive noise on its power pins. For optimal jitter performance, the device should be isolated from noise on power planes connected to its 3.3V and 1.8 V supply pins. Microsemi application note ZLAN-649 provides power supply filtering recommendations.

6.9.3 Power Calculator

The GUI software for the device includes a useful power calculator that estimates power utilization for a specific configuration or application.

6.9.4 Reset and Configuration Circuit

To ensure proper operation, the device must be reset after power-up by driving the RST_B pin low. It is not acceptable to use an external R-C network to hold RST_B low during power-up. The RST_B pin should be held low for at least 2ms. Following reset, the device will operate under specified default settings. The SRST_b pin must always be wired directly to the RST_b pin.

The RST_B input has Schmidt trigger properties to prevent level bouncing.

General purpose I/O pins GPIO0_IF, GPIO5_AC0 and GPIO6_AC1 are used to configure the device on power up. GPIO0_IF must be held at the desired level for at least 550ms after RST_B goes high. Then it can used for normal GPIO functions as described in Section 8. GPIO5_AC0 and GPIO6_AC1 are latched on the rising edge of SRST_B. Then they can be used for normal GPIO functions. If an external pullup or pulldown resistor is used on any of these pins it should be 1kΩ.

By default all outputs are disabled to allow programing of required frequencies before enabling the outputs.

6.9.5 VDD_DRI, VREG_OUT and VDDC

Figure 18 highlights the recommended circuitry for VDD_DRI and VREG_OUT.

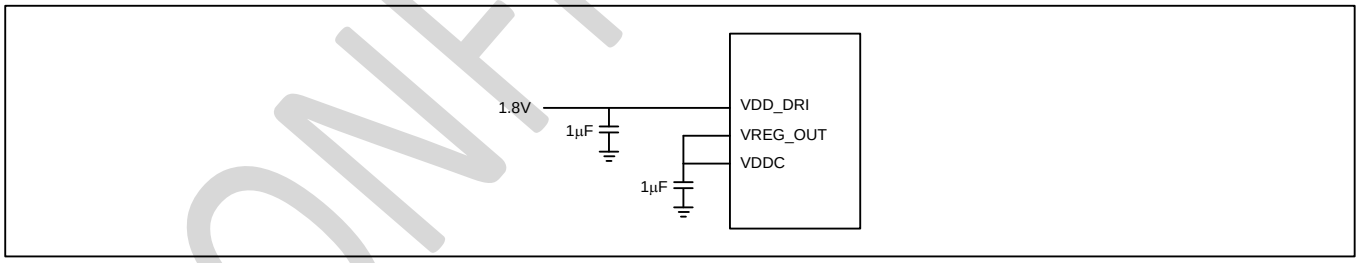


Figure 18 - External Connection of VDD_DRI, VREG_OUT and VDDC

7. Configuration and Control

The SPI/I²C host interface allows field programmability of the device's configuration registers. As an example, the user might start the device at nominal synchronous Ethernet rate, and then switch to an OTN FEC rate after the link's FEC rate is negotiated.

7.1 Pre-Configured Default Values on Power-Up

Upon power up, device registers will have values as described in the Register Map section. If the device should start up with settings different from default it can be pre-configured (pre-programmed) by Microsemi. The device can be pre-configured with up to three different custom configurations. Any of the three custom configurations can

be selected just after reset using the GPIO5_AC0 and GPIO6_AC1 pins as described in Table 1. The values of these pins are ignored if the device is not pre-configured.

7.2 Register Configuration

This section refers to configuration registers that are set by the user to control operation of the device.

7.2.1 Input Reference Configuration

The following parameters can be configured for the reference input:

- Input reference frequency
- Default input reference selection
- Reference selection priority
- Automatic or manual reference switching
- Glitchless or hitless reference switching
- Reference switch based on single cycle monitor, coarse frequency monitor, precise frequency monitor, step frequency monitor and guard soak timer

7.2.2 DPLL Configuration

The following parameters can be configured for each DPLL:

- Input reference
- Loop bandwidth
- Phase slope limiter
- Pull-in range

7.2.3 Output Multiplexer Configuration

The following parameter can be configured:

- Select which DPLL drives which Synthesizer

7.2.4 Synthesizer Configuration

The following parameters can be configured for each Synthesizer:

- Synthesizers can be configured to be locked to any DPLL or disabled
- Synthesizer frequency:
  - Synthesizer 0: 730MHz to 950MHz
  - Synthesizer 1: 3.715GHz to 4.18GHz
  - Synthesizer 2: 3.715GHz to 4.18GHz

7.2.5 Output Dividers and Output Phase Offset (skew) Configuration

The following parameters can be configured:

- Output divider enable/disable
- Divider value
- Output phase offset
- Output pulse width

7.2.6 Output Drivers Configuration

The following parameters can be configured:

- Output enable/disable
- Output start/stop, (stop high, stop low, stop high-impedance)
- Output driver type (LVDS, LVPECL, programmable differential, HCSL, CMOS, HSTL)

7.3 GPIO Configuration

The device GPIO are configured using the SPI/I^2C. Each GPIO pin can be programmed independently to be:

General Input: In this mode system software can read the logic level of the corresponding pin (either high or low). For example the logic level of GPIO0 is reflected in the register gpio_in_status_2_0, bit 0.

General Output: In this mode system software can configure a GPIO pin to drive either high or low. For example GPIO0 would drive the value specified in register gpio_out_2_0, bit 0.

Control Inputs: In this mode the user can control the device function via GPIOs. For example, the function controlled by GPIO0 is selected by configuring gpio_select_0. Nearly any device function that is controllable through the device registers can be controlled via GPIO. A small subset of control functions is shown below:

- Select DPLL reference
- External Loss Of Signal (LOS) indications
- Enable/disable differential and single ended outputs
- Enable/disable TIE Clear
- Stop/start output clocks

Status Outputs: In this mode the device can connect a status value from any of the device status registers to the corresponding GPIO pin. For example GPIO0 will mirror a bit from the status register specified in register gpio_select_0. A subset of status messages is listed below:

- DPLL loss of lock indicators
- DPLL holdover indicators
- Reference 0 to 9 fail indicators

Loss of Signal (LOS) input: This function can be used to indicate to the device that one of the input references has failed. When the active input is forced to indicate failure the DPLL may be programmed to automatically enter the holdover state or some alternate action. For example GPIO0 can be used to indicate a reference failure by programming gpio_select_0.

The GPIO outputs are updated and the GPIO inputs are read by the device approximately every 10ms to 25ms.

7.4 Ready Status

System software can start to configure the device registers 1.1s after power-up or reset.

7.5 Time to Output Clocks Valid

When a device configures itself from internal flash memory at power-up or reset, there is a delay before output clock signals are present (visible).

For the GPOOUT signals from GP synthesizer, the output clocks are present typically within 0.5 seconds (high frequency clock) to 1 second (low frequency clock, such as 1PPS) depending on the clock frequency.

For the HPOUT signals from HPSynthX internally connected to DPLLX, the output clocks are present typically within 0.5 seconds (high frequency clock) to 1 second (low frequency clock, such as 1PPS) depending on the clock frequency.

For the HPOUT signals from HPSynthX internally connected to DPLLY (where X and Y are different values), the output clocks are present typically within 4.5 seconds (high frequency clock) to 5 seconds (low frequency clock, such as 1PPS) depending on the clock frequency.

These times are independent of the input reference qualification configuration (such as input PFM), that determines when the DPLL transitions out of FREERUN/HOLDOVER to lock onto a qualified input reference clock. These times are independent of the DPLL configuration (such as lock declaration criteria and bandwidth), that determines when the DPLL enters the PHASE_LOCK state. These programmable input and DPLL configuration options (such as configuring PFM for 10 seconds) may mean the output clock is present after power-up or reset, but is free-running / traceable to the local oscillator, prior to the DPLL locking to an input.

Similar times can be expected when system software configures the device immediately after power-up or reset unless additional delay is caused by the system software.

8. Host Interface

A host processor controls and receives status from the Microsemi device using either a SPI or I²C interface.

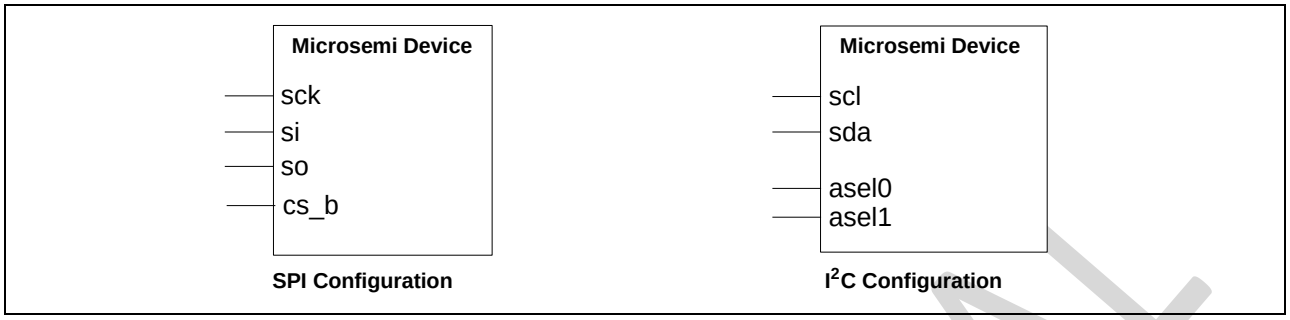


Figure 1. **Serial Interface Configuration**

The selection between I²C and SPI interfaces is performed at start-up using the GPIO0 pin. The GPIO0 pin must be held at the required level for 550ms after the de-assertion of the RST_B pin, after which time it can be released and used as a regular GPIO.

GPIO[0]	Serial Interface
0	SPI
1	I2C

Table 2 - Serial Interface Selection

Both interfaces use a seven-bit address field. The device register space is divided into multiple pages of 127 registers each. Page 0 has addresses 0x000 to 0x07E, Page 1 has addresses 0x080 to 0x0FE and so on. The host selects between the pages by writing to the Page Select register (address 0x7F on each page). For example, writing a 0x03 to the page select register makes registers 0x180 to 0x1FE available through the host interface.

The device registers are divided into direct-access and indirect-access (mailbox) registers. The direct-access registers (Pages 0 to 10 and 14) are accessed simply by reading or writing specific memory locations. For example to set DPLL0 to freerun mode system software should write to the dpll_ctrl_0 register. The mailbox access registers (Pages 11 and 12) have shared address space. For example Page 11 is shared among all input references. To initialize one of the input references the user needs to specify which input reference needs to be updated (ref_mb_mask register) to program all the other registers that need to be modified and finally issue the write command by setting the **wr** bit high in the ref_mb_sem (reference mailbox semaphore) register. The device then reads the mailbox and clears the **wr** bit in the ref_mb_sem register. The behavior of Page 12 for DPLLs is similar.

8.1 Serial Peripheral Interface

The serial peripheral interface (SPI) allows read/write access to the device's registers.

The serial peripheral interface supports half-duplex processor mode which means that during a write cycle to the device, output data from the **SO**_ASEL1 pin must be ignored. Similarly, the input data on the **SI**_SDA pin is ignored by the device during a read cycle.

The SPI interface supports two modes of access: Most Significant bit (MSb) first transmission and Least Significant bit (LSb) first transmission. The mode is automatically selected based on the state of **SCK**_SCL pin when the **CS_B**_ASEL0 pin is active. If the **SCK**_SCL pin is low during **CS_B**_ASEL0 activation, then MSb-first timing is selected. If the **SCK**_SCL pin is high during **CS_B**_ASEL0 activation, then LSb-first timing is assumed.

The SPI port expects 1 bit to differentiate between read and write operation followed by 7-bit addressing and 8-bit data transmission. During SPI access, the **CS_B**_ASEL0 pin must be held low until the operation is complete.

Burst read/write mode is also supported by leaving the chip select signal **CS_B**_ASEL0 low after a read or a write. The register address is automatically incremented after each data byte is read or written.

Functional waveforms for the LSb-first and MSb-first modes, and burst mode are shown in Figure 19, Figure 20 and Figure 21. Timing characteristics are shown in Table 20 and Figure 33.

8.1.1 Least Significant Bit (LSb) First Transmission Mode

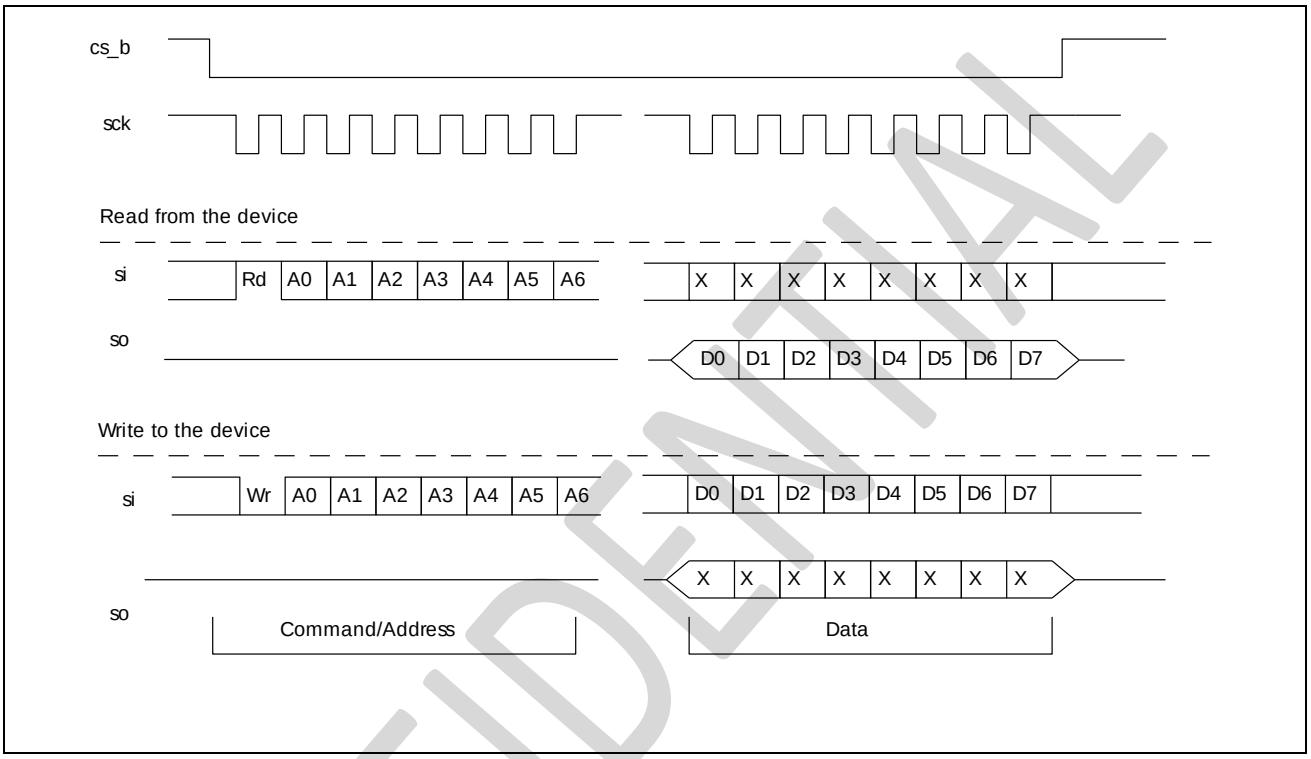


Figure 19 - Serial Peripheral Interface Functional Waveform – LSB First Mode

8.1.2 Most Significant Bit (MSb) First Transmission Mode

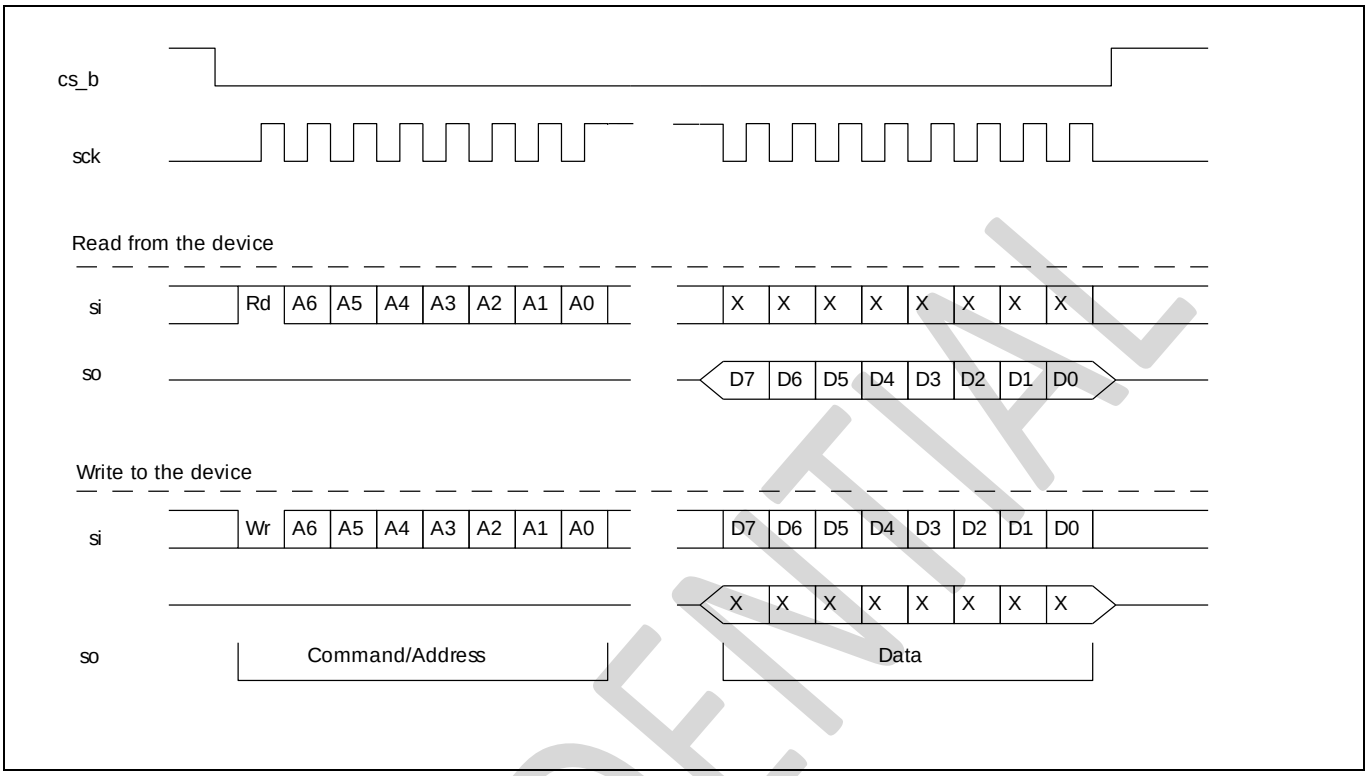


Figure 20 - Serial Peripheral Interface Functional Waveform – MSB First Mode

8.1.3 SPI Burst Mode Operation

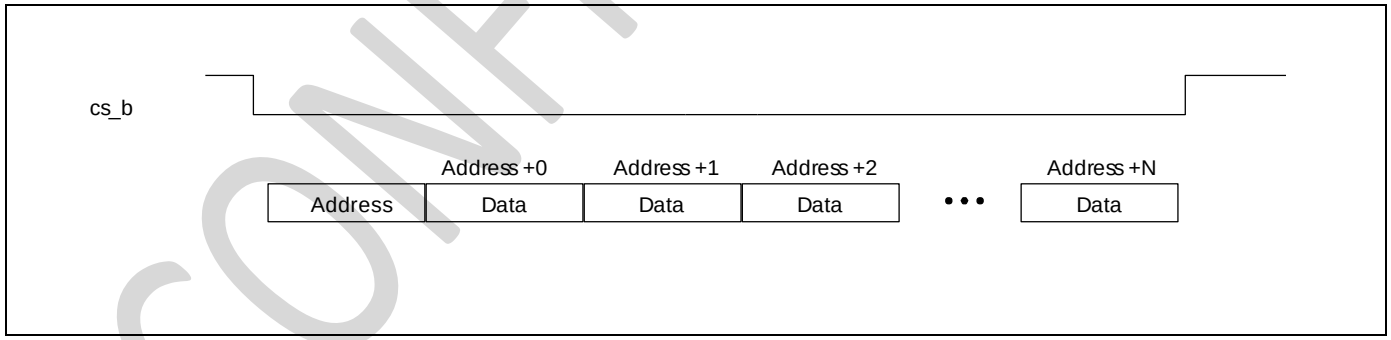


Figure 21 - Example of the Burst Mode Operation

8.1.4 Interfacing to a 2.5V SPI Bus

The supply voltage for the SPI interface pins is VDD, which is always 3.3V. But it *is* possible to interface the device to a 2.5V SPI bus. On the SO_ASEL1 pin (SPI data out) an external resistor divider can be used to reduce signal amplitude to 2.5V. For the SPI input pins SCK_SCL, SI_SDA, and CS_B_ASEL0, the min V_{IH} spec is shown in Table 7. The SPI master must have a min V_{OH} spec greater than or equal to this min V_{IH} spec for reliable 2.5V communication on these three pins.

8.2 I²C Interface

The I²C controller supports version 2.1 (January 2000) of the Philips I²C bus specification. The port operates in slave mode with 7-bit addressing, and can operate in Standard (100kbits/s) and Fast (400kbits/s) modes. Burst mode is supported in both standard and fast modes.

Data is transferred MSb first and occurs in 1 byte blocks. As shown in Figure 22, a write command consists of a 7-bit device (slave) address, a R/W indicator bit, a 7-bit register address (0x00 - 0x7F), and 8-bits of data.

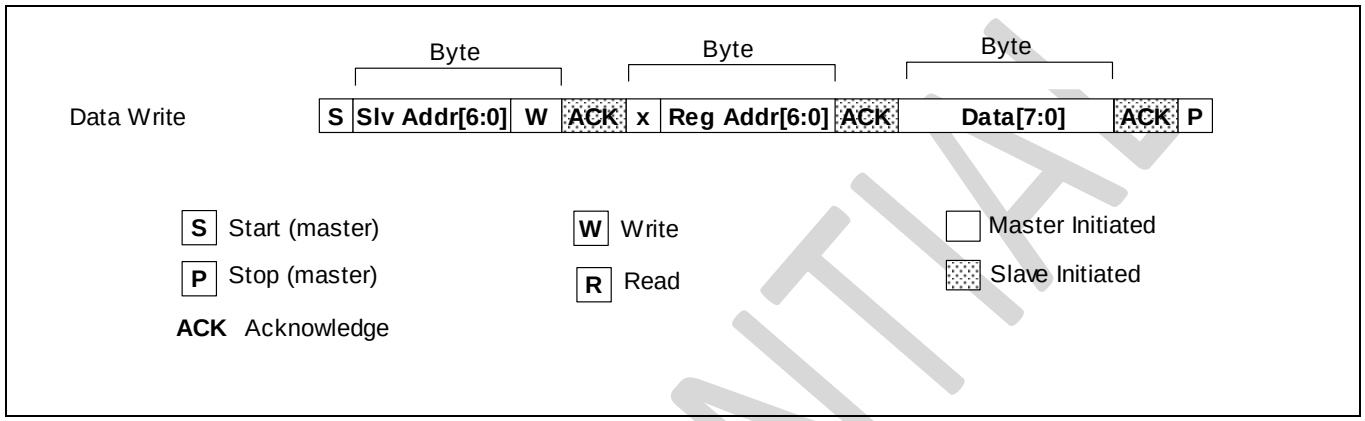


Figure 22 - I²C Data Write Protocol

A read is performed in two stages. A data write is used to set the register address, then a data read is performed to retrieve the data from the set address. This is shown in following figure.

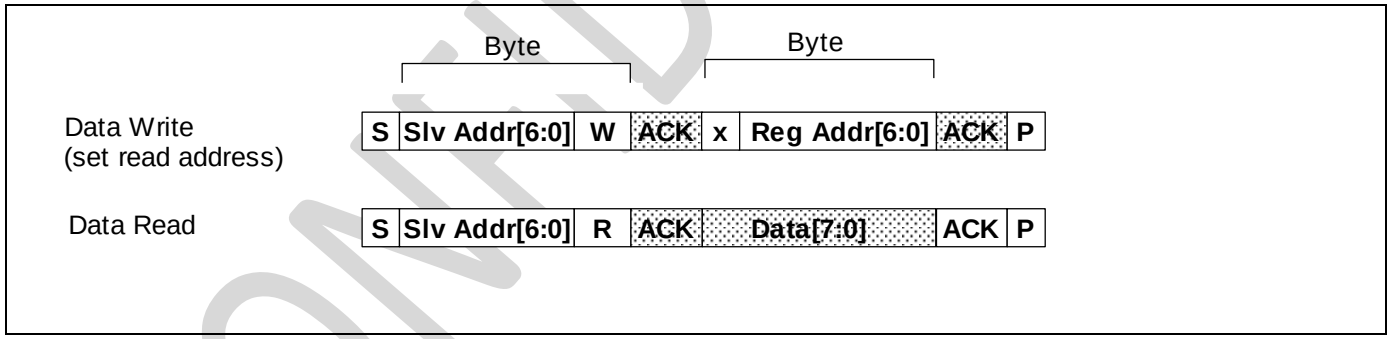


Figure 23 - I²C Data Read Protocol

The 7-bit device (slave) address contains a 5-bit fixed address plus variable bits which are set with the **asel0,** and **asel1** pins. This allows multiple devices to share the same I²C bus. The address configuration is shown in following figure.

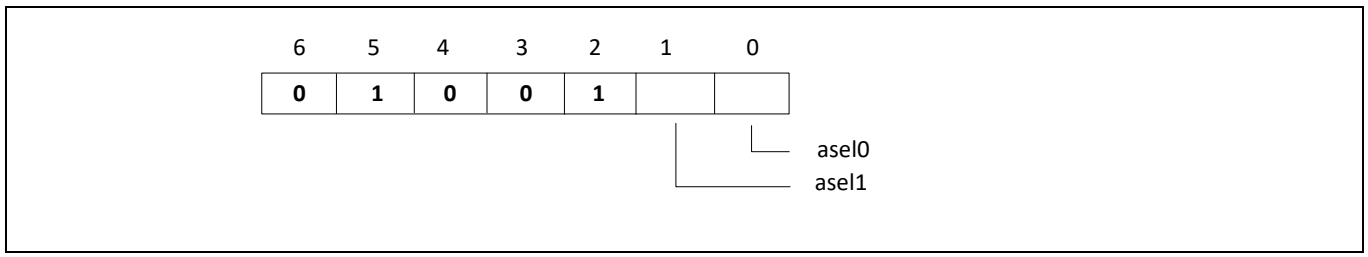


Figure 24 - I²C 7-Bit Slave Address

The device also supports burst mode which allows multiple data write or read operations with a single specified address. This is shown in Figure 25 (write) and Figure 23 (read). The first data byte is written/read to/from the specified address, and subsequent data bytes are written/read using an automatically incremented address. The maximum auto increment address of a burst operation is 0x7F and operations beyond this limit will be ignored. In other words, the auto increment address does not wrap around to 0x00 after reaching 0x7F.

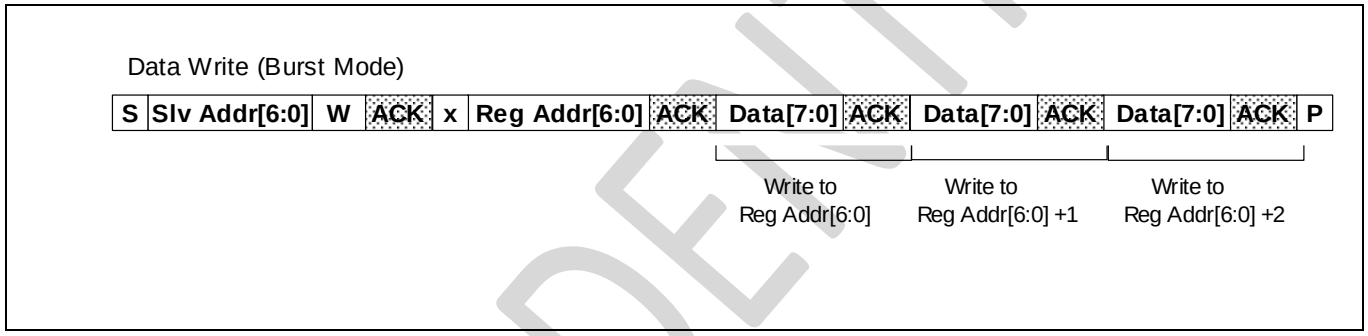


Figure 25 - I²C Data Write Burst Mode

9. Register Map

The device is controlled by accessing registers through the serial interface (SPI or I²C). The device can be configured to operate in unmanaged (automatic) mode which minimizes its interaction with system software, or it can operate in a managed (manual) mode where the system software controls operation of the device.

The register map is big-endian format.

A simple way to generate configuration for the device is to use the evaluation software (GUI) which can operate standalone (without an evaluation board). Through the GUI the user can quickly set all required parameters and save the configuration to a text file which can then be used by the system processor to load and configure the device.

9.1 Multi-byte Register Values

The device register map is based on 8-bit register access, so register values that require more than 8 bits are spread out over multiple registers and accessed in 8-bit segments. When accessing multi-byte register values, it is important that the registers are accessed in the proper order. The 8-bit register containing the most significant byte (MSB) must be accessed first, and the register containing the least significant byte (LSB) must be accessed last. An example of a multi-byte register is shown in Figure 26. When writing a multi-byte value, the value is latched when the LSB is written.

In this example the central_freq_offset register is written with the default value of 0x046AAAAB, a 32-bit value spread over four 8-bit registers. The MSB is contained in address 0x000B and the LSB in 0x000E. When reading or writing this multi-byte value, the MSB must be accessed first, then the middle bytes, and the LSB last.

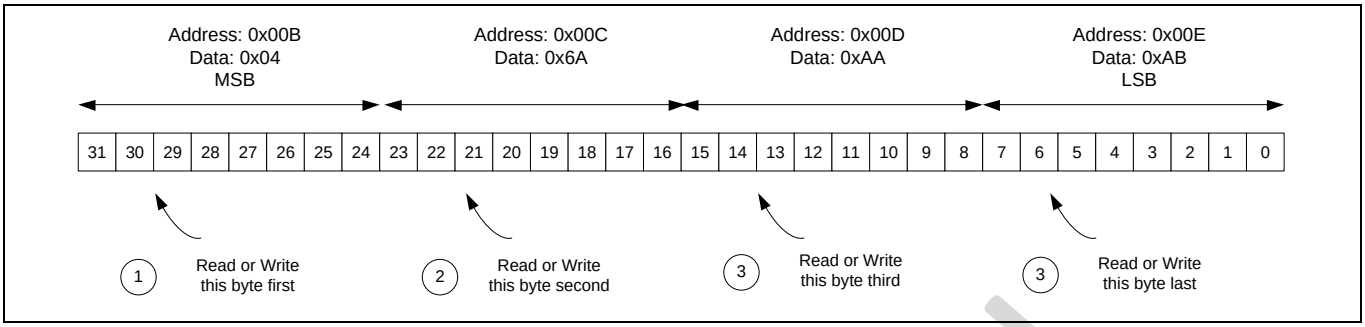


Figure 26 - Accessing Multi-byte Register Value

9.1.1 Time Between Two Write Accesses to the Same Register

The user should not write to the same register faster than 25ms. Some registers that control state machine or system clock operation require larger delays after writing in order for the state and configurations to be updated. One example is the register central_freq_offset requires much longer time, but this register should not be changed dynamically. Other examples include those related to precise input-output alignment.

The dpll_df_offset_x registers can be written with a minimum wait time of 600 microseconds between write accesses to the same register to support NCO operation.

For the page selection register (at addresses 0x07F, 0x0FF, 0x17F, …,0x6FF), there is no waiting time required between write accesses.

9.1.2 Time After Change to State Machine or System-Clock Related Configuration

The user should wait for appropriate time after configuration of state machine or system clock related configuration prior to updating other registers. One example is the register central_freq_offset. Other examples include those related to precise input-output alignment.

9.2 Sticky Read

Some status registers are defined as Sticky Read (StickyR, Type=S in the tables below). The procedure for accessing these registers is:

- write 0x01 to sticky_lock register at address 0x180
- clear status registers by writing 0x00 to them
- write 0x00 to sticky_lock at address 0x180
- wait for 25ms
- read the status register(s)

9.3 Register Map List Summary

The following tables provides a summary of the registers available for status and configuration of the device.

0x000	Register Map Page 0, General
0x080	Register Map Page 1, GPIOs
0x100	Register Map Page 2, Status
0x180	Register Map Page 3, Sticky
0x200	Register Map Page 4, Ctrl
0x280	Register Map Page 5, Ref Freq
0x300	Register Map Page 6, DPLL
0x400	Register Map Page 8, GP Synth
0x480	Register Map Page 9, HP Synth
0x500	Register Map Page 10, HPOUT
0x580	Register Map Page 11, Ref Mailbox
0x600	Register Map Page 12, DPLL Mailbox
0x700	Register Map Page 14, Misc

Register Map Page 0, General

Address	Name	Default	Type
0x0000	info	0x20	R
0x0001:0x0002	id	0x0000	R
0x0005:0x0006	fw_ver	Contact Microchip	R
0x0007:0x000A	custom_config_ver	0xFFFFFFFF	R/W
0x000B:0x000E	central_freq_offset	0x046AAAAB	R/W
0x0011	auto_config_sel	0x03	R
0x0019:0x001A	gpio_at_startup	0x0000	R
0x0026:0x002A	master_clk_ofst	0x0000000000	R/W
0x002C	osci_ctrl	0x02	R/W
0x007E	uport	0x00	R/W
0x007F	page_sel	0x00	R/W

Register Map Page 1, GPIOs

Address	Name	Default	Type
0x0080	gpio_irq_config	0x00	R/W
0x0082	gpio_out_2_0	0x00	R/W
0x0084	gpio_freeze_2_0	0x00	R/W
0x0088:0x0089	gpio_select_0	0x0000	R/W
0x008A	gpio_config_0	0x00	R/W
0x008B:0x008C	gpio_select_1	0x0000	R/W
0x008D	gpio_config_1	0x00	R/W
0x008E:0x008F	gpio_select_2	0x0000	R/W
0x0090	gpio_config_2	0x00	R/W
0x0097	gpio_select_5	0x00	R/W
0x0098	gpio_config_5	0x00	R/W
0x0099	gpio_select_6	0x00	R/W
0x009A	gpio_config_6	0x00	R/W
0x009B	gpio_select_7	0x00	R/W
0x009C	gpio_config_7	0x00	R/W
0x009D	gpio_select_8	0x00	R/W
0x009E	gpio_config_8	0x00	R/W
0x00A8	ref_irq_mask_3_0	0x00	R/W
0x00A9	ref_irq_mask_4	0x00	R/W
0x00AB	dpll_irq_mask	0x00	R/W
0x00AC	synth_irq_mask	0x00	R/W
0x00AD	hp_out_irq_mask	0x00	R/W
0x00B0	ref_mon_th_mask_0P	0x00	R/W
0x00B1	ref_mon_tl_mask_0P	0x00	R/W
0x00B2	ref_mon_th_mask_0N	0x00	R/W
0x00B3	ref_mon_tl_mask_0N	0x00	R/W
0x00B4	ref_mon_th_mask_1P	0x00	R/W
0x00B5	ref_mon_tl_mask_1P	0x00	R/W
0x00B6	ref_mon_th_mask_1N	0x00	R/W
0x00B7	ref_mon_tl_mask_1N	0x00	R/W
0x00B8	ref_mon_th_mask_2P	0x00	R/W
0x00B9	ref_mon_tl_mask_2P	0x00	R/W
0x00BA	ref_mon_th_mask_2N	0x00	R/W
0x00BB	ref_mon_tl_mask_2N	0x00	R/W
0x00BC	ref_mon_th_mask_3P	0x00	R/W
0x00BD	ref_mon_tl_mask_3P	0x00	R/W
0x00BE	ref_mon_th_mask_3N	0x00	R/W
0x00BF	ref_mon_tl_mask_3N	0x00	R/W

Address	Name	Default	Type
0x00C0	ref_mon_th_mask_4P	0x00	R/W
0x00C1	ref_mon_tl_mask_4P	0x00	R/W
0x00C2	ref_mon_th_mask_4N	0x00	R/W
0x00C3	ref_mon_tl_mask_4N	0x00	R/W
0x00D0	dpll_mon_th_mask_0	0x00	R/W
0x00D1	dpll_mon_tl_mask_0	0x00	R/W
0x00D2	dpll_mon_th_mask_1	0x00	R/W
0x00D3	dpll_mon_tl_mask_1	0x00	R/W
0x00D4	dpll_mon_th_mask_2	0x00	R/W
0x00D5	dpll_mon_tl_mask_2	0x00	R/W
0x00D6	dpll_mon_th_mask_3	0x00	R/W
0x00D7	dpll_mon_tl_mask_3	0x00	R/W
0x00D8	dpll_mon_th_mask_4	0x00	R/W
0x00D9	dpll_mon_tl_mask_4	0x00	R/W
0x00DA	dpll_mon_th_mask_5	0x00	R/W
0x00DB	dpll_mon_tl_mask_5	0x00	R/W
0x00E0	gp_mon_th_mask	0x00	R/W
0x00E1	gp_mon_tl_mask	0x00	R/W
0x00E2	hp_mon_th_mask_1	0x00	R/W
0x00E3	hp_mon_tl_mask_1	0x00	R/W
0x00E4	hp_mon_th_mask_2	0x00	R/W
0x00E5	hp_mon_tl_mask_2	0x00	R/W
0x00E6	hp_out_th_mask_0	0x00	R/W
0x00E7	hp_out_tl_mask_0	0x00	R/W
0x00E8	hp_out_th_mask_1	0x00	R/W
0x00E9	hp_out_tl_mask_1	0x00	R/W
0x00EA	hp_out_th_mask_2	0x00	R/W
0x00EB	hp_out_tl_mask_2	0x00	R/W
0x00EC	hp_out_th_mask_3	0x00	R/W
0x00ED	hp_out_tl_mask_3	0x00	R/W
0x00EE	hp_out_th_mask_4	0x00	R/W
0x00EF	hp_out_tl_mask_4	0x00	R/W
0x00F0	hp_out_th_mask_5	0x00	R/W
0x00F1	hp_out_tl_mask_5	0x00	R/W
0x00F2	hp_out_th_mask_6	0x00	R/W
0x00F3	hp_out_tl_mask_6	0x00	R/W
0x00F4	hp_out_th_mask_7	0x00	R/W
0x00F5	hp_out_tl_mask_7	0x00	R/W
0x00FE	uport	0x00	R/W
0x00FF	page_sel	0x00	R/W

Register Map Page 2, Status

Address	Name	Default	Type
0x0100	gpio_in_status_2_0	0x00	R
0x0101	gpio_in_status_8_5	0x00	R
0x0108	ref_mon_status_0P	0x00	R
0x0109	ref_mon_status_0N	0x00	R
0x010A	ref_mon_status_1P	0x00	R
0x010B	ref_mon_status_1N	0x00	R
0x010C	ref_mon_status_2P	0x00	R
0x010D	ref_mon_status_2N	0x00	R
0x010E	ref_mon_status_3P	0x00	R
0x010F	ref_mon_status_3N	0x00	R

Address	Name	Default	Type
0x0110	ref_mon_status_4P	0x00	R
0x0111	ref_mon_status_4N	0x00	R
0x0118	dpll_mon_status_0	0x00	R
0x0119	dpll_mon_status_1	0x00	R
0x011A	dpll_mon_status_2	0x00	R
0x011B	dpll_mon_status_3	0x00	R
0x011C	dpll_mon_status_4	0x00	R
0x011D	dpll_mon_status_5	0x00	R
0x0120	dpll_state_refsel_0	0x00	R
0x0121	dpll_state_refsel_1	0x00	R
0x0122	dpll_state_refsel_2	0x00	R
0x0123	dpll_state_refsel_3	0x00	R
0x0130	dpll_df_timer_status	0x00	R
0x013F	synth_fine_shift_status	0x00	R
0x0140	gp_mon_status	0x00	R
0x0141	hp_mon_status_1	0x00	R
0x0142	hp_mon_status_2	0x00	R
0x0143	hp_out_mon_status_0	0x00	R
0x0144	hp_out_mon_status_1	0x00	R
0x0145	hp_out_mon_status_2	0x00	R
0x0146	hp_out_mon_status_3	0x00	R
0x0147	hp_out_mon_status_4	0x00	R
0x0148	hp_out_mon_status_5	0x00	R
0x0149	hp_out_mon_status_6	0x00	R
0x014A	hp_out_mon_status_7	0x00	R
0x0150	hp_fb_msdiv_sel_1	0x00	R
0x0151:0x0154	hp_fb_lsdiv_sel_1	0x00000000	R
0x0158	hp_fb_msdiv_sel_2	0x00	R
0x0159:0x015C	hp_fb_lsdiv_sel_2	0x00000000	R
0x017E	uport	0x00	R/W
0x017F	page_sel	0x00	R/W

Register Map Page 3, Sticky

Address	Name	Default	Type
0x0180	sticky_lock	0x00	R/W
0x0181	gpio_latch_status_8_5	0x00	S
0x018A	dpll_fast_lock_sticky	0x00	S
0x018B	dpll_fast_lock_phase_sticky	0x00	S
0x018C	dpll_fast_lock_freq_sticky	0x00	S
0x018D	dpll_tie_wr_sticky	0x00	S
0x0190	gp_out_phase_step_sticky	0x00	S
0x0191	hp_out_phase_step_sticky	0x00	S
0x01A8	ref_irq_active_3_0	0x00	S
0x01A9	ref_irq_active_4	0x00	S
0x01AB	dpll_irq_active	0x00	S
0x01AC	synth_irq_active	0x00	S
0x01AD	hp_out_irq_active	0x00	S
0x01B0	ref_mon_th_sticky_0P	0x00	S
0x01B1	ref_mon_tl_sticky_0P	0x00	S
0x01B2	ref_mon_th_sticky_0N	0x00	S
0x01B3	ref_mon_tl_sticky_0N	0x00	S
0x01B4	ref_mon_th_sticky_1P	0x00	S
0x01B5	ref_mon_tl_sticky_1P	0x00	S

Address	Name	Default	Type
0x01B6	ref_mon_th_sticky_1N	0x00	S
0x01B7	ref_mon_tl_sticky_1N	0x00	S
0x01B8	ref_mon_th_sticky_2P	0x00	S
0x01B9	ref_mon_tl_sticky_2P	0x00	S
0x01BA	ref_mon_th_sticky_2N	0x00	S
0x01BB	ref_mon_tl_sticky_2N	0x00	S
0x01BC	ref_mon_th_sticky_3P	0x00	S
0x01BD	ref_mon_tl_sticky_3P	0x00	S
0x01BE	ref_mon_th_sticky_3N	0x00	S
0x01BF	ref_mon_tl_sticky_3N	0x00	S
0x01C0	ref_mon_th_sticky_4P	0x00	S
0x01C1	ref_mon_tl_sticky_4P	0x00	S
0x01C2	ref_mon_th_sticky_4N	0x00	S
0x01C3	ref_mon_tl_sticky_4N	0x00	S
0x01D0	dpll_mon_th_sticky_0	0x00	S
0x01D1	dpll_mon_tl_sticky_0	0x00	S
0x01D2	dpll_mon_th_sticky_1	0x00	S
0x01D3	dpll_mon_tl_sticky_1	0x00	S
0x01D4	dpll_mon_th_sticky_2	0x00	S
0x01D5	dpll_mon_tl_sticky_2	0x00	S
0x01D6	dpll_mon_th_sticky_3	0x00	S
0x01D7	dpll_mon_tl_sticky_3	0x00	S
0x01D8	dpll_mon_th_sticky_4	0x00	S
0x01D9	dpll_mon_tl_sticky_4	0x00	S
0x01DA	dpll_mon_th_sticky_5	0x00	S
0x01DB	dpll_mon_tl_sticky_5	0x00	S
0x01E0	gp_mon_th_sticky	0x00	S
0x01E1	gp_mon_tl_sticky	0x00	S
0x01E2	hp_mon_th_sticky_1	0x00	S
0x01E3	hp_mon_tl_sticky_1	0x00	S
0x01E4	hp_mon_th_sticky_2	0x00	S
0x01E5	hp_mon_tl_sticky_2	0x00	S
0x01E6	hp_out_th_sticky_0	0x00	S
0x01E7	hp_out_tl_sticky_0	0x00	S
0x01E8	hp_out_th_sticky_1	0x00	S
0x01E9	hp_out_tl_sticky_1	0x00	S
0x01EA	hp_out_th_sticky_2	0x00	S
0x01EB	hp_out_tl_sticky_2	0x00	S
0x01EC	hp_out_th_sticky_3	0x00	S
0x01ED	hp_out_tl_sticky_3	0x00	S
0x01EE	hp_out_th_sticky_4	0x00	S
0x01EF	hp_out_tl_sticky_4	0x00	S
0x01F0	hp_out_th_sticky_5	0x00	S
0x01F1	hp_out_tl_sticky_5	0x00	S
0x01F2	hp_out_th_sticky_6	0x00	S
0x01F3	hp_out_tl_sticky_6	0x00	S
0x01F4	hp_out_th_sticky_7	0x00	S
0x01F5	hp_out_tl_sticky_7	0x00	S
0x01FE	uport	0x00	R/W
0x01FF	page_sel	0x00	R/W

Register Map Page 4, Ctrl

Address	Name	Default	Type
0x0200	ref_los_3_0	0x00	R/W
0x0201	ref_los_4	0x00	R/W
0x0203	ref_sfm_clr_3_0	0x00	R/W
0x0204	ref_sfm_clr_4	0x00	R/W
0x0205	ref_freq_cmd	0x00	R/W
0x0206	dpll_freq_cmd	0x00	R/W
0x0208	dpll_enable	0x03	R/W
0x020B	ext_fb_ctrl	0x00	R/W
0x020C	ext_fb_sel	0x00	R/W
0x0210	dpll_mode_refsel_0	0x00	R/W
0x0211	dpll_ctrl_0	0x02	R/W
0x0212	dpll_cmd_0	0x00	R/W
0x0214	dpll_mode_refsel_1	0x00	R/W
0x0215	dpll_ctrl_1	0x02	R/W
0x0216	dpll_cmd_1	0x00	R/W
0x0218	dpll_mode_refsel_2	0x00	R/W
0x0219	dpll_ctrl_2	0x02	R/W
0x021A	dpll_cmd_2	0x00	R/W
0x021C	dpll_mode_refsel_3	0x00	R/W
0x021D	dpll_ctrl_3	0x00	R/W
0x021E	dpll_cmd_3	0x00	R/W
0x0230	phase_step_ctrl	0x00	R/W
0x0234:0x0237	phase_step_data	0x00000000	R/W
0x0238	phase_step_mask_gp	0x00	R/W
0x0239	phase_step_mask_hp	0x00	R/W
0x023E	phase_step_max	0x31	R/W
0x024C	out_squelch_ctrl	0x00	R/W
0x024D	gp_squelch_mask	0x00	R/W
0x024E	hp_squelch_mask	0x00	R/W
0x024F	pherr_low_freq_ctrl	0x00	R/W
0x0250	pherr_meas_ctrl	0x00	R/W
0x0251	pherr_meas_refsel	0x98	R/W
0x0252:0x0257	pherr_data	0x000000000000	R
0x0258	pherr_low_freq_refsel	0x98	R/W
0x0259:0x025E	pherr_low_freq_data	0x000000000000	R
0x025F	pherr_read_rqst	0x00	R/W
0x0260	dpll_phase_err_read_mask	0x00	R/W
0x0261:0x0266	dpll_phase_err_data_0	0x000000000000	R
0x0267:0x026C	dpll_phase_err_data_1	0x000000000000	R
0x026D:0x0272	dpll_phase_err_data_2	0x000000000000	R
0x0273:0x0278	dpll_phase_err_data_3	0x000000000000	R
0x027E	uport	0x00	R/W
0x027F	page_sel	0x00	R/W

Register Map Page 5, Ref Freq

Address	Name	Default	Type
0x0280:0x0283	ref_freq_0P	0x00000000	R
0x0284:0x0287	ref_freq_0N	0x00000000	R
0x0288:0x028B	ref_freq_1P	0x00000000	R
0x028C:0x028F	ref_freq_1N	0x00000000	R
0x0290:0x0293	ref_freq_2P	0x00000000	R
0x0294:0x0297	ref_freq_2N	0x00000000	R

Address	Name	Default	Type
0x0298:0x029B	ref_freq_3P	0x00000000	R
0x029C:0x029F	ref_freq_3N	0x00000000	R
0x02A0:0x02A3	ref_freq_4P	0x00000000	R
0x02A4:0x02A7	ref_freq_4N	0x00000000	R
0x02FE	uport	0x00	R/W
0x02FF	page_sel	0x00	R/W

Register Map Page 6, DPLL

Address	Name	Default	Type
0x0300:0x0305	dpll_df_offset_0	0x000000000000	R/W
0x0306	dpll_df_ctrl_0	0x00	R/W
0x0307:0x030B	dpll_df_manual_0	0x0000000000	R/W
0x030C:0x0310	dpll_df_temp_0	0x0000000000	R/W
0x0311:0x0312	dpll_df_timer_0	0x0000	R/W
0x0313:0x0316	dpll_tie_data_0	0x00000000	R/W
0x0317	dpll_tie_ctrl_0	0x00	R/W
0x0320:0x0325	dpll_df_offset_1	0x000000000000	R/W
0x0326	dpll_df_ctrl_1	0x00	R/W
0x0327:0x032B	dpll_df_manual_1	0x0000000000	R/W
0x032C:0x0330	dpll_df_temp_1	0x0000000000	R/W
0x0331:0x0332	dpll_df_timer_1	0x0000	R/W
0x0333:0x0336	dpll_tie_data_1	0x00000000	R/W
0x0337	dpll_tie_ctrl_1	0x00	R/W
0x0340:0x0345	dpll_df_offset_2	0x000000000000	R/W
0x0346	dpll_df_ctrl_2	0x00	R/W
0x0347:0x034B	dpll_df_manual_2	0x0000000000	R/W
0x034C:0x0350	dpll_df_temp_2	0x0000000000	R/W
0x0351:0x0352	dpll_df_timer_2	0x0000	R/W
0x0353:0x0356	dpll_tie_data_2	0x00000000	R/W
0x0357	dpll_tie_ctrl_2	0x00	R/W
0x0360:0x0365	dpll_df_offset_3	0x000000000000	R/W
0x0366	dpll_df_ctrl_3	0x00	R/W
0x0368:0x036D	dpll_df_offset_4	0x000000000000	R/W
0x036E	dpll_df_ctrl_4	0x00	R/W
0x0370:0x0375	dpll_df_offset_5	0x000000000000	R/W
0x0376	dpll_df_ctrl_5	0x00	R/W
0x037E	uport	0x00	R/W
0x037F	page_sel	0x00	R/W

Register Map Page 8, GP Synth

Address	Name	Default	Type
0x0400	gp_ctrl	0x00	R/W
0x0401	gp_cmd	0x00	R/W
0x0404:0x0405	gp_freq_base	0x1F40	R/W
0x0406:0x0408	gp_freq_mult	0x017BB0	R/W
0x0409:0x040A	gp_freq_m	0x0001	R/W
0x040B:0x040C	gp_freq_n	0x0001	R/W
0x040D:0x040E	gp_fine_shift	0x0000	R/W
0x040F	gp_fine_shift_intvl	0x01	R/W
0x0410:0x0414	gp_df_offset_manual	0x0000000000	R/W
0x0420	gp_out_ctrl_0	0x00	R/W
0x0422:0x0425	gp_out_div_0	0x00000005	R/W
0x0426:0x0429	gp_out_width_0	0x00000000	R/W

Address	Name	Default	Type
0x0430	gp_out_ctrl_1	0x00	R/W
0x0432:0x0435	gp_out_div_1	0x00000028	R/W
0x0436:0x0439	gp_out_width_1	0x00000000	R/W
0x0450	gp_out_en	0x00	R/W
0x0451	gp_out_drive	0x0F	R/W
0x047E	uport	0x00	R/W
0x047F	page_sel	0x00	R/W

Register Map Page 9, HP Synth

Address	Name	Default	Type
0x0480	hp_ctrl_1	0x10	R/W
0x0481	hp_src_1	0x03	R/W
0x0482	hp_misc_1	0x00	R/W
0x0484:0x0487	hp_freq_base_1	0xDF847580	R/W
0x0488:0x048B	hp_freq_m_1	0x00000001	R/W
0x048C:0x048F	hp_freq_n_1	0x00000001	R/W
0x0490	hp_hsdiv_1	0x04	R/W
0x0491:0x0494	hp_fdiv_base_1	0x0BEBC200	R/W
0x0495:0x0498	hp_fdiv_num_1	0x00000001	R/W
0x0499:0x049C	hp_fdiv_den_1	0x00000001	R/W
0x04A4:0x04A7	hp_fine_shift_1	0x00000000	R/W
0x04A8	hp_fb_msdiv_1	0x00	R/W
0x04A9:0x04AC	hp_fb_lsdiv_1	0x00000000	R/W
0x04AD	hp_fb_ref_1	0x00	R/W
0x04AE	hp_fb_out_1	0x00	R/W
0x04B0	hp_ctrl_2	0x20	R/W
0x04B1	hp_src_2	0x03	R/W
0x04B2	hp_misc_2	0x00	R/W
0x04B4:0x04B7	hp_freq_base_2	0xDF847580	R/W
0x04B8:0x04BB	hp_freq_m_2	0x00000001	R/W
0x04BC:0x04BF	hp_freq_n_2	0x00000001	R/W
0x04C0	hp_hsdiv_2	0x04	R/W
0x04C1:0x04C4	hp_fdiv_base_2	0x0BEBC200	R/W
0x04C5:0x04C8	hp_fdiv_num_2	0x00000001	R/W
0x04C9:0x04CC	hp_fdiv_den_2	0x00000001	R/W
0x04D4:0x04D7	hp_fine_shift_2	0x00000000	R/W
0x04D8	hp_fb_msdiv_2	0x00	R/W
0x04D9:0x04DC	hp_fb_lsdiv_2	0x00000000	R/W
0x04DD	hp_fb_ref_2	0x00	R/W
0x04DE	hp_fb_out_2	0x00	R/W
0x04E0	hp_out_en	0xFF	R/W
0x04E1	hp_out_mux	0x00	R/W
0x04E2	hp_stop_ctrl	0x00	R/W
0x04FE	uport	0x00	R/W
0x04FF	page_sel	0x00	R/W

Register Map Page 10, HPOUT

Address	Name	Default	Type
0x0500	hp_out_msdiv_0	0x04	R/W
0x0501:0x0504	hp_out_lsdiv_0	0x00000001	R/W
0x0505	hp_out_ctrl_0	0x00	R/W
0x0506	hp_out_diff_0	0x05	R/W
0x0507	hp_out_reg_0	0x00	R/W

Address	Name	Default	Type
0x0508	hp_out_lsctrl_0	0x00	R/W
0x0509	hp_out_width_0	0x00	R/W
0x050A	hp_out_shift_0	0x00	R/W
0x050B	hp_out_stop_0	0x0C	R/W
0x0510	hp_out_msdiv_1	0x04	R/W
0x0511:0x0514	hp_out_lsdiv_1	0x00000001	R/W
0x0515	hp_out_ctrl_1	0x00	R/W
0x0516	hp_out_diff_1	0x05	R/W
0x0517	hp_out_reg_1	0x00	R/W
0x0518	hp_out_lsctrl_1	0x00	R/W
0x0519	hp_out_width_1	0x00	R/W
0x051A	hp_out_shift_1	0x00	R/W
0x051B	hp_out_stop_1	0x0C	R/W
0x0520	hp_out_msdiv_2	0x04	R/W
0x0521:0x0524	hp_out_lsdiv_2	0x00000001	R/W
0x0525	hp_out_ctrl_2	0x00	R/W
0x0526	hp_out_diff_2	0x05	R/W
0x0527	hp_out_reg_2	0x00	R/W
0x0528	hp_out_lsctrl_2	0x00	R/W
0x0529	hp_out_width_2	0x00	R/W
0x052A	hp_out_shift_2	0x00	R/W
0x052B	hp_out_stop_2	0x0C	R/W
0x0530	hp_out_msdiv_3	0x04	R/W
0x0531:0x0534	hp_out_lsdiv_3	0x00000001	R/W
0x0535	hp_out_ctrl_3	0x00	R/W
0x0536	hp_out_diff_3	0x05	R/W
0x0537	hp_out_reg_3	0x00	R/W
0x0538	hp_out_lsctrl_3	0x00	R/W
0x0539	hp_out_width_3	0x00	R/W
0x053A	hp_out_shift_3	0x00	R/W
0x053B	hp_out_stop_3	0x0C	R/W
0x0540	hp_out_msdiv_4	0x04	R/W
0x0541:0x0544	hp_out_lsdiv_4	0x00000001	R/W
0x0545	hp_out_ctrl_4	0x00	R/W
0x0546	hp_out_diff_4	0x05	R/W
0x0547	hp_out_reg_4	0x00	R/W
0x0548	hp_out_lsctrl_4	0x00	R/W
0x0549	hp_out_width_4	0x00	R/W
0x054A	hp_out_shift_4	0x00	R/W
0x054B	hp_out_stop_4	0x0C	R/W
0x0550	hp_out_msdiv_5	0x04	R/W
0x0551:0x0554	hp_out_lsdiv_5	0x00000001	R/W
0x0555	hp_out_ctrl_5	0x00	R/W
0x0556	hp_out_diff_5	0x05	R/W
0x0557	hp_out_reg_5	0x00	R/W
0x0558	hp_out_lsctrl_5	0x00	R/W
0x0559	hp_out_width_5	0x00	R/W
0x055A	hp_out_shift_5	0x00	R/W
0x055B	hp_out_stop_5	0x0C	R/W
0x0560	hp_out_msdiv_6	0x04	R/W
0x0561:0x0564	hp_out_lsdiv_6	0x00000001	R/W
0x0565	hp_out_ctrl_6	0x00	R/W
0x0566	hp_out_diff_6	0x05	R/W

Address	Name	Default	Type
0x0567	hp_out_reg_6	0x00	R/W
0x0568	hp_out_lsctrl_6	0x00	R/W
0x0569	hp_out_width_6	0x00	R/W
0x056A	hp_out_shift_6	0x00	R/W
0x056B	hp_out_stop_6	0x0C	R/W
0x0570	hp_out_msdiv_7	0x04	R/W
0x0571:0x0574	hp_out_lsdiv_7	0x00000001	R/W
0x0575	hp_out_ctrl_7	0x00	R/W
0x0576	hp_out_diff_7	0x05	R/W
0x0577	hp_out_reg_7	0x00	R/W
0x0578	hp_out_lsctrl_7	0x00	R/W
0x0579	hp_out_width_7	0x00	R/W
0x057A	hp_out_shift_7	0x00	R/W
0x057B	hp_out_stop_7	0x0C	R/W
0x057E	uport	0x00	R/W
0x057F	page_sel	0x00	R/W

Register Map Page 11, Ref Mailbox

Address	Name	Default	Type
0x0582:0x0583	ref_mb_mask	0x0001	R/W
0x0584	ref_mb_sem	0x00	R/W
0x0585:0x0586	ref_freq_base	0x1F40	R/W
0x0587:0x0588	ref_freq_mult	0x0001	R/W
0x0589:0x058A	ref_ratio_m	0x0001	R/W
0x058B:0x058C	ref_ratio_n	0x0001	R/W
0x058D	ref_config	0x01	R/W
0x0590	ref_scm	0x05	R/W
0x0591	ref_cfm	0x05	R/W
0x0592:0x0593	ref_gst_disqual	0x0005	R/W
0x0594:0x0595	ref_gst_qual	0x0014	R/W
0x0596	ref_sfm	0x00	R/W
0x0597	ref_pfm_ctrl	0x00	R/W
0x0598:0x0599	ref_pfm_disqualify	0x6568	R/W
0x059A:0x059B	ref_pfm_qualify	0x4E48	R/W
0x059C:0x059D	ref_pfm_period	0x0000	R/W
0x059E	ref_pfm_filter_limit	0x28	R/W
0x05A0	ref_sync	0x00	R/W
0x05A1	ref_sync_misc	0x00	R/W
0x05A2	ref_sync_offset_comp	0x00	R/W
0x05A3:0x05A6	ref_phase_offset_compensation	0x00000000	R/W
0x05A8:0x05AB	ref_scm_fine	0x00000000	R/W
0x05FE	uport	0x00	R/W
0x05FF	page_sel	0x00	R/W

Register Map Page 12, DPLL Mailbox

Address	Name	Default	Type
0x0602:0x0603	dpll_mb_mask	0x0001	R/W
0x0604	dpll_mb_sem	0x00	R/W
0x0605	dpll_bw_fixed	0x00	R/W
0x0607	dpll_config	0x00	R/W
0x0608:0x0609	dpll_psl	0x0000	R/W
0x060E:0x060F	dpll_range	0x0078	R/W
0x0610	dpll_ref_sw_mask	0x08	R/W

Address	Name	Default	Type
0x0611	dpll_ref_ho_mask	0x17	R/W
0x0614	dpll_ref_prio_0	0x10	R/W
0x0615	dpll_ref_prio_1	0x32	R/W
0x0616	dpll_ref_prio_2	0x54	R/W
0x0617	dpll_ref_prio_3	0x76	R/W
0x0618	dpll_ref_prio_4	0x98	R/W
0x061C	dpll_ho_filter	0x00	R/W
0x061D	dpll_ho_delay	0x4C	R/W
0x0620	dpll_fast_lock_ctrl	0x01	R/W
0x0621	dpll_fast_lock_phase_err	0xFF	R/W
0x0622	dpll_fast_lock_freq_err	0x04	R/W
0x0623:0x0624	dpll_fast_lock_ideal_time	0x0000	R/W
0x0626:0x0627	dpll_fast_lock_fol	0x07D0	R/W
0x062E	dpll_damping	0x00	R/W
0x0630:0x0633	dpll_phase_bad	0x02255100	R/W
0x0634:0x0637	dpll_phase_good	0x02255100	R/W
0x0638	dpll_duration_good	0x09	R/W
0x0639	dpll_lock_delay	0x00	R/W
0x063A	dpll_tie	0x00	R/W
0x063B	dpll_tie_wr_thresh	0x00	R/W
0x063C	dpll_fp_first_realign	0x7F	R/W
0x063D	dpll_fp_realign_intvl	0x00	R/W
0x063E	dpll_fp_lock_thresh	0x00	R/W
0x067E	uport	0x00	R/W
0x067F	page_sel	0x00	R/W

Register Map Page 14, Misc

Address	Name	Default	Type
0x0706	psrg_ctrl	0x00	R/W
0x0730:0x074F	Available for customer use	0x00	R/W

9.3.1 Register List Page 0, General

Address:	0x0000	
Name:	info	
Default:	0x20	
Type:	R	
Bit Field	Function Name	Description
7	ready	This bit should be ignored. System software should wait 1.1s after power-up or reset before writing device registers.
6:0	reserved	

Address:	0x0001:0x0002	
Name:	id	
Default:	0x0000	
Type:	R	
Bit Field	Function Name	Description
15:0		Chip identification number. 0x1CB8: ZL30256

Address:	0x0005:0x0006
Name:	fw_ver
Default:	contact Microchip
Type:	R

Bit Field	Function Name	Description
15	fw_dirty	Firmware dirty indicator. This bit is set when the firmware is built from source code that has not been checked-in to the firmware repository. This bit should never be set in released firmware.
14:0	fw_revision	Firmware revision number. This field indicates the firmware revision of the source code used to build this image.

Address:	0x0007:0x000A
Name:	custom_config_ver
Default:	0xFFFFFFFF
Type:	R/W

Bit Field	Function Name	Description
31:0		This register is intended (but not limited) to be used as configuration version number. Up to 3 custom register configurations can be programmed into the device. This register is for customer use and is ignored by the device.

Address:	0x000B:0x000E
Name:	central_freq_offset
Default:	0x046AAAAB
Type:	R/W

Bit Field	Function Name	Description
31:0		Device central frequency offset. This value is used to compensate for the oscillator's offset from a nominal frequency value. Expressed in steps of 2^-32 slower than nominal frequency. Changing this register resets all REFs, DPLLs, and synthesizers. It is only intended to be written once before configuring the rest of the device. The nominal oscillator frequency is set using the device MC[1:0] pins: 00: 50MHz 01: 25MHz 1x: 125MHz The value to be programmed in this register is calculated with the following formula: central_freq_offset = round(((f_nom / f_osc) - 1) * 2^32) f_osc - represents real oscillator frequency f_nom - represents nominal oscillator frequency Example: When using a 24.576MHz master clock, set MC[1:0] = 01. central_freq_offset = round(((25e6 / 24.576e6) - 1) * 2^32) = 0x046AAAAB Note: When MC[1:0] = 1x (125MHz), the default value of this register will be 0x180072B0 (114.285MHz). Note: This register should not be programmed greater than 0x20DC71C7 (slower than nominal - 10%).

Address:	0x0011	
Name:	auto_config_sel	
Default:	0x03	
Type:	R	
Bit Field	Function Name	Description
7:2	reserved	
1:0	sel	0-2: Register defaults came from auto configuration record 3: Register defaults match data sheet (no auto configuration programmed or CRC error)

Address:	0x0019:0x001A	
Name:	gpio_at_startup	
Default:	0x0000	
Type:	R/W	
Bit Field	Function Name	Description
15:9	reserved	
8	gpio8	See description for gpio0.
7	gpio7	See description for gpio0.
6	gpio6	See description for gpio0.
5	gpio5	See description for gpio0.
4	mc1	The value of MC1 latched at device startup.
3	mc0	The value of MC0 latched at device startup.
2	gpio2	See description for gpio0.
1	gpio1	See description for gpio0.
0	gpio0	The value of GPIO0 latched at device startup.

Address:	0x0026:0x002A	
Name:	master_clk_ofst	
Default:	0x0000000000	
Type:	R/W	
Bit Field	Function Name	Description
39:0		Master clock offset compensation. This register is intended to be used to compensate for known oscillator ageing. The compensation value will affect the following reference monitors: SCM, CFM, PFM, and SFM. It also affects reference frequency measurements; see register 0x205 (ref_freq_cmd) for further details. This register does not affect any DPLL operations. This register is a signed value with LSB=2^-48. This register must be programmed with the known change in oscillator frequency. E.g., if the oscillator frequency changes by -5.4ppb (slows down): master_clk_ofst = -5.4 * 10^-9 * 2^48 master_clk_ofst = 0xFFFFE8CEA4

Address:	0x002C	
Name:	osci_ctrl	
Default:	0x02	
Type:	R/W	
Bit Field	Function Name	Description
7:3	reserved	
2	dbl_en	0: OSCI doubler disabled 1: OSCI doubler enabled. The OSCI doubler must only be enabled when the master clock is <= 50MHz.

1:0	osci_mode	00: OSCI disabled / powered down 01: reserved 10: OSCI enabled as single-ended input for external oscillator signal; OSCO must be left floating 11: reserved

Address:	0x007E	
Name:	uport	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	lockout	When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing.
6:1	reserved	
0	status	This field indicates if microport attempted access had not been successful. The register content will be 0x00 if the access had been successful.

Address:	0x007F	
Name:	page_sel	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		Unsigned binary value of these bits represents selected page for SPI/I2C access: 0x00: page 0 (first 128 bytes) 0x01: page 1 (second 128 bytes) 0x02: page 2 (third 128 bytes) 0x03: page 3 (fourth 128 bytes) 0x04: page 4 (fifth 128 bytes) 0x05: page 5 (sixth 128 bytes) 0x06: page 6 (seventh 128 bytes) 0x07: page 7 (eighth 128 bytes) 0x08: page 8 (ninth 128 bytes) 0x09: page 9 (tenth 128 bytes) 0x0A: page 10 (eleventh 128 bytes) 0x0B: page 11 (twelfth 128 bytes) 0x0C: page 12 (thirteenth 128 bytes) 0x0D-0xFF: reserved

9.3.2 Register List Page 1, GPIOs

Address:	0x0080	
Name:	gpio_irq_config	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:3	reserved	
2	high_z	Note: This register should be written before enabling IRQ mode in gpio_config_n. 0: The device actively drives the GPIO IRQ pin low when the interrupt is inactive. 1: The device puts the GPIO IRQ pin in high-z mode when the interrupt is inactive.
1	active_high	0: The GPIO IRQ pin will be high when the interrupt is inactive

		(active-low mode). 1: The GPIO IRQ pin will be high when the interrupt is active (active-high mode).
0	level_trig	0: The GPIO IRQ pin is in edge-triggered mode. When an interrupt occurs, the device will generate a short pulse on the GPIO IRQ pin then return it to the inactive state immediately. Once the interrupt has been acknowledged, new interrupts can be generated. 1: The GPIO IRQ pin is in level-triggered mode. The GPIO IRQ pin will stay low or high (depending on the active_high bit) until the interrupt has been acknowledged. New interrupts cannot be generated until the host has acknowledged the current one by clearing the sticky bits in registers: 0x1A8 (ref_irq_active_3_0) 0x1A9 (ref_irq_active_4) 0x1AB (dpll_irq_active) 0x1AC (synth_irq_active) For both modes, interrupts are generated whenever the status changes (0-to-1 or 1-to-0).

Address:	0x0082	
Name:	gpio_out_2_0	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:3	reserved	
2	gpio2	Note: If a bit is assigned to a logic level, and its corresponding output enable bit is set to '1', the same logic level appears at the corresponding bit position of the GPIO output pin. Sets the output value on pin GPIO2.
1	gpio1	Sets the output value on pin GPIO1.
0	gpio0	Sets the output value on pin GPIO0.

Address:	0x0084	
Name:	gpio_freeze_2_0	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:3	reserved	
2	gpio2	See description for gpio0.
1	gpio1	See description for gpio0.
0	gpio0	Freeze the value in register 0x100, bit 0 (gpio_in_status_2_0::gpio0) if GPIO0 is configured as input, control or LOS mode.

Address:	0x0088:0x0089	
Name:	gpio_select_0	
Default:	0x0000	
Type:	R/W	
Bit Field	Function Name	Description
15	reserved	
14:12	bit	Note: The fields in this register are only useful when GPIO0 is configured as a Status, Control, or LOS.

		This field works with the page and offset field to select a single bit in the host register map. Specifically, this field selects the bit position of the selected register byte.
11:8	page	This field works with the bit and offset fields to select a single bit in the host register map. Specifically, this field selects the page.
7	reserved	
6:0	offset	When GPIO0 is configured as as a Status or Control, then this field works with the bit and page fields to select a single bit in the host register map. Specifically, this field selects the offset within the page. When GPIO0 is configured as an LOS, then this field selects the target reference.

Address:	0x008A	
Name:	gpio_config_0	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:3	reserved	
2:0	ctrl	This field determines the mode of operation for GPIO0. Register 0x088-0x089 (gpio_select_0) should be set before writing this register, if the mode being set requires additional configuration. 000: Input The logic value sensed on GPIO0 is reflected in register 0x100, bit 0 (gpio_in_status_2_0::gpio0). 001: Output GPIO0 actively drives the value specified in register 0x082, bit 0 (gpio_out_2_0::gpio0). 010: Control Certain device functions can be actively controlled via GPIO0. The device function to be controlled is selected by configuring register gpio_select_0. Whenever a change is detected on GPIO0 or the selected host register bit, then the device ORs together the GPIO and register bit values before applying the corresponding configuration. In this mode, the selected host register bit must be a R/W type. 011: Status The device status can be actively supervised via GPIO0. The device mirrors the host register bit, specified in register gpio_select_0, onto GPIO0. Typically, the selected host register bit is a status bit (either R or S type) in this mode. 100: IRQ No matter how many GPIOs are configured to IRQ mode, only the GPIO that most recently configured will generate interrupts. If the latest GPIO is then configured to other modes, the next latest GPIO will become active and generate interrupts. GPIO interrupt is disabled only if all the GPIOs are set to non-IRQ modes. 101: LOS The input reference specified by register 0x089, bits 6:0 (gpio_select_0::offset) can be forced into failure via GPIO0

		control.

Address:	0x008B:0x008C	
Name:	gpio_select_1	
Default:	0x0000	
Type:	R/W	
Bit Field	Function Name	Description
15	reserved	
14:12	bit	See description for register at Address 0x088, bits 14:12 (gpio_select_0::bit).
11:8	page	See description for register at Address 0x088, bits 11:8 (gpio_select_0::page).
7	reserved	
6:0	offset	See description for register at Address 0x088, bits 6:0 (gpio_select_0::offset).

Address:	0x008D	
Name:	gpio_config_1	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:3	reserved	
2:0	ctrl	See description for register at Address 0x08A, bits 2:0 (gpio_config_0::ctrl).

Address:	0x008E:0x008F	
Name:	gpio_select_2	
Default:	0x0000	
Type:	R/W	
Bit Field	Function Name	Description
15	reserved	
14:12	bit	See description for register at Address 0x088, bits 14:12 (gpio_select_0::bit).
11:8	page	See description for register at Address 0x088, bits 11:8 (gpio_select_0::page).
7	reserved	
6:0	offset	See description for register at Address 0x088, bits 6:0 (gpio_select_0::offset).

Address:	0x0090	
Name:	gpio_config_2	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:3	reserved	
2:0	ctrl	See description for register at Address 0x08A, bits 2:0 (gpio_config_0::ctrl).

Address:	0x0097	
Name:	gpio_select_5	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		When register gpio_config_5::ctrl is set to 1xx to configure GPIO5 as a status output, this register is programmed with an 8-

		bit code to specify the specific status indicator. 0x42: HP-Synth1 lock status 0x44: HP-Synth1 frequency too high status 0x46: HP-Synth1 frequency too low status 0x4A: HP-Synth2 lock status 0x4C: HP-Synth2 frequency too high status 0x4E: HP-Synth2 frequency too low status 0x80: HPOUT0 stopped 0x85: HPOUT0 state (only useful for very low HPOUT0 frequency such as 1Hz) 0x88: HPOUT1 stopped 0x8D: HPOUT1 state 0x98: HPOUT2 stopped 0x9D: HPOUT2 state 0xA0: HPOUT3 stopped 0xA5: HPOUT3 state 0xA8: HPOUT4 stopped 0xAD: HPOUT4 state 0xB0: HPOUT5 stopped 0xB5: HPOUT5 state 0xC0: HPOUT6 stopped 0xC5: HPOUT6 state 0xC8: HPOUT7 stopped 0xCD: HPOUT7 state (only useful for very low HPOUT7 frequency such as 1Hz)

Address:	0x0098	
Name:	gpio_config_5	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:3	reserved	
2:0	ctrl	000: General-purpose input 001: General-purpose input - inverted polarity 010: General-purpose output driving low 011: General-purpose output driving high 100: Status output - non-inverted polarity 101: Status output - inverted polarity of the status bit it follows 110: Status output - 0 drives low, 1 high impedance 111: Status output - 0 high impedance, 1 drives low

Address:	0x0099	
Name:	gpio_select_6	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		See description for register at Address 0x097 (gpio_select_5).

Address:	0x009A	
Name:	gpio_config_6	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:3	reserved	
2:0	ctrl	See description for register at Address 0x098, bits 2:0 (gpio_config_5::ctrl).

Address:	0x009B	
Name:	gpio_select_7	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		See description for register at Address 0x097 (gpio_select_5).

Address:	0x009C	
Name:	gpio_config_7	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:3	reserved	
2:0	ctrl	See description for register at Address 0x098, bits 2:0 (gpio_config_5::ctrl).

Address:	0x009D	
Name:	gpio_select_8	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		See description for register at Address 0x097 (gpio_select_5).

Address:	0x009E	
Name:	gpio_config_8	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:3	reserved	
2:0	ctrl	See description for register at Address 0x098, bits 2:0 (gpio_config_5::ctrl).

Address:	0x00A8	
Name:	ref_irq_mask_3_0	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	mask_3N	See description for mask_0P.
6	mask_3P	See description for mask_0P.
5	mask_2N	See description for mask_0P.
4	mask_2P	See description for mask_0P.
3	mask_1N	See description for mask_0P.
2	mask_1P	See description for mask_0P.
1	mask_0N	See description for mask_0P.
0	mask_0P	This bit is only considered when GPIO interrupt (IRQ) is turned on. It determines if a GPIO interrupt is generated when REF0P status changes. 0: A REF0P status change will not generate a GPIO interrupt. Register 0x1A8 bit 0 (ref_irq_active_3_0::irq_0P) will not be set. 1: Certain REF0P status changes will generate a GPIO interrupt. Register 0x1A8 bit 0 (ref_irq_active_3_0::irq_0P) will be set to 1. See register 0x0B0 (ref_mon_th_mask_0P) and 0x0B1 (ref_mon_tl_mask_0P) to configure which status changes will generate a GPIO interrupt.

Address:	0x00A9	
Name:	ref_irq_mask_4	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:2	reserved	
1	mask_4N	See description for register at Address 0x0A8, bit 0 (ref_irq_mask_3_0::mask_0P).
0	mask_4P	See description for register at Address 0x0A8, bit 0 (ref_irq_mask_3_0::mask_0P).

Address:	0x00AB	
Name:	dpll_irq_mask	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	reserved	
3	mask_3	See description for mask_0.
2	mask_2	See description for mask_0.
1	mask_1	See description for mask_0.
0	mask_0	This bit is only considered when GPIO interrupt (IRQ) is turned on. It determines if a GPIO interrupt is generated when DPLL0 status changes. 0: A DPLL0 status change will not generate a GPIO interrupt. Register 0x1AB bit 0 (dpll_irq_active::irq_0) will not be set. 1: Certain DPLL0 status changes will generate a GPIO interrupt. Register 0x1AB bit 0 (dpll_irq_active::irq_0) will be set to 1. See register 0x0D0 (dpll_mon_th_mask_0) to configure which status changes will generate a GPIO interrupt.

Address:	0x00AC	
Name:	synth_irq_mask	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:3	reserved	
2	mask_2	See description for mask_0.
1	mask_1	See description for mask_0.
0	mask_0	This bit is only considered when GPIO interrupt (IRQ) is turned on. It determines if a GPIO interrupt is generated when synth0 status changes. 0: A synth0 status change will not generate a GPIO interrupt. Register 0x1AC bit 0 (synth_irq_active::irq_0) will not be set. 1: Certain synth0 status changes will generate a GPIO interrupt. Register 0x1AC bit 0 (synth_irq_active::irq_0) will be set to 1. See register 0x0E0 (gp_mon_th_mask_0) to configure which status changes will generate a GPIO interrupt.

Address:	0x00AD	
Name:	hp_out_irq_mask	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	mask_7	See description for mask_0.
6	mask_6	See description for mask_0.

5	mask_5	See description for mask_0.
4	mask_4	See description for mask_0.
3	mask_3	See description for mask_0.
2	mask_2	See description for mask_0.
1	mask_1	See description for mask_0.
0	mask_0	This bit is only considered when GPIO interrupt (IRQ) is turned on. It determines if a GPIO interrupt is generated when HPOUT0 status changes. 0: A HPOUT0 status change will not generate a GPIO interrupt. Register 0x1AD bit 0 (hp_out_irq_active::irq_0) will not be set. 1: Certain HPOUT0 status changes will generate a GPIO interrupt. Register 0x1AD bit 0 (hp_out_irq_active::irq_0) will be set to 1. See registers 0x0E6 (hp_out_th_mask_0) and 0x0E7 (hp_out_tl_mask_0) to configure which status changes will generate a GPIO interrupt.

Address:	0x00B0	
Name:	ref_mon_th_mask_0P	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	0: REF0P SFM status transitions 0->1 are masked. 1: REF0P SFM status transitions 0->1 are unmasked. A GPIO interrupt will be generated and register 0x1A8 bit 0 (ref_irq_active_3_0::irq_0P) will be set to 1.
4	pfm	0: REF0P PFM status transitions 0->1 are masked. 1: REF0P PFM status transitions 0->1 are unmasked. A GPIO interrupt will be generated and register 0x1A8 bit 0 (ref_irq_active_3_0::irq_0P) will be set to 1.
3	gst	0: REF0P GST status transitions 0->1 are masked. 1: REF0P GST status transitions 0->1 are unmasked. A GPIO interrupt will be generated and register 0x1A8 bit 0 (ref_irq_active_3_0::irq_0P) will be set to 1.
2	cfm	0: REF0P CFM status transitions 0->1 are masked. 1: REF0P CFM status transitions 0->1 are unmasked. A GPIO interrupt will be generated and register 0x1A8 bit 0 (ref_irq_active_3_0::irq_0P) will be set to 1.
1	scm	0: REF0P SCM status transitions 0->1 are masked. 1: REF0P SCM status transitions 0->1 are unmasked. A GPIO interrupt will be generated and register 0x1A8 bit 0 (ref_irq_active_3_0::irq_0P) will be set to 1.
0	los	0: REF0P LOS status transitions 0->1 are masked. 1: REF0P LOS status transitions 0->1 are unmasked. A GPIO interrupt will be generated and register 0x1A8 bit 0 (ref_irq_active_3_0::irq_0P) will be set to 1.

Address:	0x00B1	
Name:	ref_mon_tl_mask_0P	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	0: REF0P SFM status transitions 1->0 are masked. 1: REF0P SFM status transitions 1->0 are unmasked. A GPIO interrupt will be generated and register 0x1A8 bit 0

		(ref_irq_active_3_0::fail_0P) will be set to 1.
4	pfm	0: REF0P PFM status transitions 1->0 are masked. 1: REF0P PFM status transitions 1->0 are unmasked. A GPIO interrupt will be generated and register 0x1A8 bit 0 (ref_irq_active_3_0::irq_0P) will be set to 1.
3	gst	0: REF0P GST status transitions 1->0 are masked. 1: REF0P GST status transitions 1->0 are unmasked. A GPIO interrupt will be generated and register 0x1A8 bit 0 (ref_irq_active_3_0::irq_0P) will be set to 1.
2	cfm	0: REF0P CFM status transitions 1->0 are masked. 1: REF0P CFM status transitions 1->0 are unmasked. A GPIO interrupt will be generated and register 0x1A8 bit 0 (ref_irq_active_3_0::irq_0P) will be set to 1.
1	scm	0: REF0P SCM status transitions 1->0 are masked. 1: REF0P SCM status transitions 1->0 are unmasked. A GPIO interrupt will be generated and register 0x1A8 bit 0 (ref_irq_active_3_0::irq_0P) will be set to 1.
0	los	0: REF0P LOS status transitions 1->0 are masked. 1: REF0P LOS status transitions 1->0 are unmasked. A GPIO interrupt will be generated and register 0x1A8 bit 0 (ref_irq_active_3_0::irq_0P) will be set to 1.

Address:	0x00B2	
Name:	ref_mon_th_mask_0N	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x0B0, bit 5 (ref_mon_th_mask_0P::sfm).
4	pfm	See description for register at Address 0x0B0, bit 4 (ref_mon_th_mask_0P::pfm).
3	gst	See description for register at Address 0x0B0, bit 3 (ref_mon_th_mask_0P::gst).
2	cfm	See description for register at Address 0x0B0, bit 2 (ref_mon_th_mask_0P::cfm).
1	scm	See description for register at Address 0x0B0, bit 1 (ref_mon_th_mask_0P::scm).
0	los	See description for register at Address 0x0B0, bit 0 (ref_mon_th_mask_0P::los).

Address:	0x00B3	
Name:	ref_mon_tl_mask_0N	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x0B1, bit 5 (ref_mon_tl_mask_0P::sfm).
4	pfm	See description for register at Address 0x0B1, bit 4 (ref_mon_tl_mask_0P::pfm).
3	gst	See description for register at Address 0x0B1, bit 3 (ref_mon_tl_mask_0P::gst).
2	cfm	See description for register at Address 0x0B1, bit 2 (ref_mon_tl_mask_0P::cfm).
1	scm	See description for register at Address 0x0B1, bit 1

		(ref_mon_tl_mask_0P::scm).
0	los	See description for register at Address 0x0B1, bit 0 (ref_mon_tl_mask_0P::los).

Address:	0x00B4	
Name:	ref_mon_th_mask_1P	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x0B0, bit 5 (ref_mon_th_mask_0P::sfm).
4	pfm	See description for register at Address 0x0B0, bit 4 (ref_mon_th_mask_0P::pfm).
3	gst	See description for register at Address 0x0B0, bit 3 (ref_mon_th_mask_0P::gst).
2	cfm	See description for register at Address 0x0B0, bit 2 (ref_mon_th_mask_0P::cfm).
1	scm	See description for register at Address 0x0B0, bit 1 (ref_mon_th_mask_0P::scm).
0	los	See description for register at Address 0x0B0, bit 0 (ref_mon_th_mask_0P::los).

Address:	0x00B5	
Name:	ref_mon_tl_mask_1P	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x0B1, bit 5 (ref_mon_tl_mask_0P::sfm).
4	pfm	See description for register at Address 0x0B1, bit 4 (ref_mon_tl_mask_0P::pfm).
3	gst	See description for register at Address 0x0B1, bit 3 (ref_mon_tl_mask_0P::gst).
2	cfm	See description for register at Address 0x0B1, bit 2 (ref_mon_tl_mask_0P::cfm).
1	scm	See description for register at Address 0x0B1, bit 1 (ref_mon_tl_mask_0P::scm).
0	los	See description for register at Address 0x0B1, bit 0 (ref_mon_tl_mask_0P::los).

Address:	0x00B6	
Name:	ref_mon_th_mask_1N	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x0B0, bit 5 (ref_mon_th_mask_0P::sfm).
4	pfm	See description for register at Address 0x0B0, bit 4 (ref_mon_th_mask_0P::pfm).
3	gst	See description for register at Address 0x0B0, bit 3 (ref_mon_th_mask_0P::gst).
2	cfm	See description for register at Address 0x0B0, bit 2

		(ref_mon_th_mask_0P::cfm).
1	scm	See description for register at Address 0x0B0, bit 1 (ref_mon_th_mask_0P::scm).
0	los	See description for register at Address 0x0B0, bit 0 (ref_mon_th_mask_0P::los).

Address:	0x00B7	
Name:	ref_mon_tl_mask_1N	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x0B1, bit 5 (ref_mon_tl_mask_0P::sfm).
4	pfm	See description for register at Address 0x0B1, bit 4 (ref_mon_tl_mask_0P::pfm).
3	gst	See description for register at Address 0x0B1, bit 3 (ref_mon_tl_mask_0P::gst).
2	cfm	See description for register at Address 0x0B1, bit 2 (ref_mon_tl_mask_0P::cfm).
1	scm	See description for register at Address 0x0B1, bit 1 (ref_mon_tl_mask_0P::scm).
0	los	See description for register at Address 0x0B1, bit 0 (ref_mon_tl_mask_0P::los).

Address:	0x00B8	
Name:	ref_mon_th_mask_2P	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x0B0, bit 5 (ref_mon_th_mask_0P::sfm).
4	pfm	See description for register at Address 0x0B0, bit 4 (ref_mon_th_mask_0P::pfm).
3	gst	See description for register at Address 0x0B0, bit 3 (ref_mon_th_mask_0P::gst).
2	cfm	See description for register at Address 0x0B0, bit 2 (ref_mon_th_mask_0P::cfm).
1	scm	See description for register at Address 0x0B0, bit 1 (ref_mon_th_mask_0P::scm).
0	los	See description for register at Address 0x0B0, bit 0 (ref_mon_th_mask_0P::los).

Address:	0x00B9	
Name:	ref_mon_tl_mask_2P	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x0B1, bit 5 (ref_mon_tl_mask_0P::sfm).
4	pfm	See description for register at Address 0x0B1, bit 4 (ref_mon_tl_mask_0P::pfm).
3	gst	See description for register at Address 0x0B1, bit 3

		(ref_mon_tl_mask_0P::gst).
2	cfm	See description for register at Address 0x0B1, bit 2 (ref_mon_tl_mask_0P::cfm).
1	scm	See description for register at Address 0x0B1, bit 1 (ref_mon_tl_mask_0P::scm).
0	los	See description for register at Address 0x0B1, bit 0 (ref_mon_tl_mask_0P::los).

Address:	0x00BA	
Name:	ref_mon_th_mask_2N	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x0B0, bit 5 (ref_mon_th_mask_0P::sfm).
4	pfm	See description for register at Address 0x0B0, bit 4 (ref_mon_th_mask_0P::pfm).
3	gst	See description for register at Address 0x0B0, bit 3 (ref_mon_th_mask_0P::gst).
2	cfm	See description for register at Address 0x0B0, bit 2 (ref_mon_th_mask_0P::cfm).
1	scm	See description for register at Address 0x0B0, bit 1 (ref_mon_th_mask_0P::scm).
0	los	See description for register at Address 0x0B0, bit 0 (ref_mon_th_mask_0P::los).

Address:	0x00BB	
Name:	ref_mon_tl_mask_2N	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x0B1, bit 5 (ref_mon_tl_mask_0P::sfm).
4	pfm	See description for register at Address 0x0B1, bit 4 (ref_mon_tl_mask_0P::pfm).
3	gst	See description for register at Address 0x0B1, bit 3 (ref_mon_tl_mask_0P::gst).
2	cfm	See description for register at Address 0x0B1, bit 2 (ref_mon_tl_mask_0P::cfm).
1	scm	See description for register at Address 0x0B1, bit 1 (ref_mon_tl_mask_0P::scm).
0	los	See description for register at Address 0x0B1, bit 0 (ref_mon_tl_mask_0P::los).

Address:	0x00BC	
Name:	ref_mon_th_mask_3P	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x0B0, bit 5 (ref_mon_th_mask_0P::sfm).
4	pfm	See description for register at Address 0x0B0, bit 4

		(ref_mon_th_mask_0P::pfm).
3	gst	See description for register at Address 0x0B0, bit 3 (ref_mon_th_mask_0P::gst).
2	cfm	See description for register at Address 0x0B0, bit 2 (ref_mon_th_mask_0P::cfm).
1	scm	See description for register at Address 0x0B0, bit 1 (ref_mon_th_mask_0P::scm).
0	los	See description for register at Address 0x0B0, bit 0 (ref_mon_th_mask_0P::los).

Address:	0x00BD	
Name:	ref_mon_tl_mask_3P	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x0B1, bit 5 (ref_mon_tl_mask_0P::sfm).
4	pfm	See description for register at Address 0x0B1, bit 4 (ref_mon_tl_mask_0P::pfm).
3	gst	See description for register at Address 0x0B1, bit 3 (ref_mon_tl_mask_0P::gst).
2	cfm	See description for register at Address 0x0B1, bit 2 (ref_mon_tl_mask_0P::cfm).
1	scm	See description for register at Address 0x0B1, bit 1 (ref_mon_tl_mask_0P::scm).
0	los	See description for register at Address 0x0B1, bit 0 (ref_mon_tl_mask_0P::los).

Address:	0x00BE	
Name:	ref_mon_th_mask_3N	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x0B0, bit 5 (ref_mon_th_mask_0P::sfm).
4	pfm	See description for register at Address 0x0B0, bit 4 (ref_mon_th_mask_0P::pfm).
3	gst	See description for register at Address 0x0B0, bit 3 (ref_mon_th_mask_0P::gst).
2	cfm	See description for register at Address 0x0B0, bit 2 (ref_mon_th_mask_0P::cfm).
1	scm	See description for register at Address 0x0B0, bit 1 (ref_mon_th_mask_0P::scm).
0	los	See description for register at Address 0x0B0, bit 0 (ref_mon_th_mask_0P::los).

Address:	0x00BF	
Name:	ref_mon_tl_mask_3N	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x0B1, bit 5

		(ref_mon_tl_mask_0P::sfm).
4	pfm	See description for register at Address 0x0B1, bit 4 (ref_mon_tl_mask_0P::pfm).
3	gst	See description for register at Address 0x0B1, bit 3 (ref_mon_tl_mask_0P::gst).
2	cfm	See description for register at Address 0x0B1, bit 2 (ref_mon_tl_mask_0P::cfm).
1	scm	See description for register at Address 0x0B1, bit 1 (ref_mon_tl_mask_0P::scm).
0	los	See description for register at Address 0x0B1, bit 0 (ref_mon_tl_mask_0P::los).

Address:	0x00C0	
Name:	ref_mon_th_mask_4P	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x0B0, bit 5 (ref_mon_th_mask_0P::sfm).
4	pfm	See description for register at Address 0x0B0, bit 4 (ref_mon_th_mask_0P::pfm).
3	gst	See description for register at Address 0x0B0, bit 3 (ref_mon_th_mask_0P::gst).
2	cfm	See description for register at Address 0x0B0, bit 2 (ref_mon_th_mask_0P::cfm).
1	scm	See description for register at Address 0x0B0, bit 1 (ref_mon_th_mask_0P::scm).
0	los	See description for register at Address 0x0B0, bit 0 (ref_mon_th_mask_0P::los).

Address:	0x00C1	
Name:	ref_mon_tl_mask_4P	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x0B1, bit 5 (ref_mon_tl_mask_0P::sfm).
4	pfm	See description for register at Address 0x0B1, bit 4 (ref_mon_tl_mask_0P::pfm).
3	gst	See description for register at Address 0x0B1, bit 3 (ref_mon_tl_mask_0P::gst).
2	cfm	See description for register at Address 0x0B1, bit 2 (ref_mon_tl_mask_0P::cfm).
1	scm	See description for register at Address 0x0B1, bit 1 (ref_mon_tl_mask_0P::scm).
0	los	See description for register at Address 0x0B1, bit 0 (ref_mon_tl_mask_0P::los).

Address:	0x00C2	
Name:	ref_mon_th_mask_4N	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x0B0, bit 5 (ref_mon_th_mask_0P::sfm).
4	pfm	See description for register at Address 0x0B0, bit 4 (ref_mon_th_mask_0P::pfm).
3	gst	See description for register at Address 0x0B0, bit 3 (ref_mon_th_mask_0P::gst).
2	cfm	See description for register at Address 0x0B0, bit 2 (ref_mon_th_mask_0P::cfm).
1	scm	See description for register at Address 0x0B0, bit 1 (ref_mon_th_mask_0P::scm).
0	los	See description for register at Address 0x0B0, bit 0 (ref_mon_th_mask_0P::los).

Address:	0x00C3	
Name:	ref_mon_tl_mask_4N	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x0B1, bit 5 (ref_mon_tl_mask_0P::sfm).
4	pfm	See description for register at Address 0x0B1, bit 4 (ref_mon_tl_mask_0P::pfm).
3	gst	See description for register at Address 0x0B1, bit 3 (ref_mon_tl_mask_0P::gst).
2	cfm	See description for register at Address 0x0B1, bit 2 (ref_mon_tl_mask_0P::cfm).
1	scm	See description for register at Address 0x0B1, bit 1 (ref_mon_tl_mask_0P::scm).
0	los	See description for register at Address 0x0B1, bit 0 (ref_mon_tl_mask_0P::los).

Address:	0x00D0	
Name:	dpll_mon_th_mask_0	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	pslhit	0: DPLL0 phase slope limit status transitions 0->1 are masked. 1: DPLL0 phase slope limit status transitions 0->1 are unmasked. A GPIO interrupt will be generated and register 0x1AB bit 0 (dpll_irq_active::irq_0) will be set to 1.
6	state_ch	0: DPLL0 state changes are masked. 1: DPLL0 state changes are unmasked. A GPIO interrupt will be generated and register 0x1AB bit 0 (dpll_irq_active::irq_0) will be set to 1.
5	flhit	0: DPLL0 pull-in/hold-in range limit status transitions 0->1 are masked. 1: DPLL0 pull-in/hold-in range limit status transitions 0->1 are unmasked. A GPIO interrupt will be generated and register 0x1AB bit 0 (dpll_irq_active::irq_0) will be set to 1.

4:3	reserved	
2	ho_ready	0: DPLL0 holdover ready status transitions 0->1 are masked. 1: DPLL0 holdover ready status transitions 0->1 are unmasked. A GPIO interrupt will be generated and register 0x1AB bit 0 (dpll_irq_active::irq_0) will be set to 1.
1	ho	0: DPLL0 holdover status transitions 0->1 are masked. 1: DPLL0 holdover status transitions 0->1 are unmasked. A GPIO interrupt will be generated and register 0x1AB bit 0 (dpll_irq_active::irq_0) will be set to 1.
0	lock	0: DPLL0 lock status transitions 0->1 are masked. 1: DPLL0 lock status transitions 0->1 are unmasked. A GPIO interrupt will be generated and register 0x1AB bit 0 (dpll_irq_active::irq_0) will be set to 1.

Address:	0x00D1	
Name:	dpll_mon_tl_mask_0	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	pslhit	0: DPLL0 phase slope limit status transitions 1->0 are masked. 1: DPLL0 phase slope limit status transitions 1->0 are unmasked. A GPIO interrupt will be generated and register 0x1AB bit 0 (dpll_irq_active::irq_0) will be set to 1.
6	reserved	
5	flhit	0: DPLL0 pull-in/hold-in range limit status transitions 1->0 are masked. 1: DPLL0 pull-in/hold-in range limit status transitions 1->0 are unmasked. A GPIO interrupt will be generated and register 0x1AB bit 0 (dpll_irq_active::irq_0) will be set to 1.
4:3	reserved	
2	ho_ready	0: DPLL0 holdover ready status transitions 1->0 are masked. 1: DPLL0 holdover ready status transitions 1->0 are unmasked. A GPIO interrupt will be generated and register 0x1AB bit 0 (dpll_irq_active::irq_0) will be set to 1.
1	ho	0: DPLL0 holdover status transitions 1->0 are masked. 1: DPLL0 holdover status transitions 1->0 are unmasked. A GPIO interrupt will be generated and register 0x1AB bit 0 (dpll_irq_active::irq_0) will be set to 1.
0	lock	0: DPLL0 lock status transitions 1->0 are masked. 1: DPLL0 lock status transitions 1->0 are unmasked. A GPIO interrupt will be generated and register 0x1AB bit 0 (dpll_irq_active::irq_0) will be set to 1.

Address:	0x00D2	
Name:	dpll_mon_th_mask_1	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	pslhit	See description for register at Address 0x0D0, bit 7 (dpll_mon_th_mask_0::pslhit).
6	state_ch	See description for register at Address 0x0D0, bit 6 (dpll_mon_th_mask_0::state_ch).
5	flhit	See description for register at Address 0x0D0, bit 5 (dpll_mon_th_mask_0::flhit).
4:3	reserved	
2	ho_ready	See description for register at Address 0x0D0, bit 2

		(dpll_mon_th_mask_0::ho_ready).
1	ho	See description for register at Address 0x0D0, bit 1 (dpll_mon_th_mask_0::ho).
0	lock	See description for register at Address 0x0D0, bit 0 (dpll_mon_th_mask_0::lock).

Address:	0x00D3	
Name:	dpll_mon_tl_mask_1	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	pslhit	See description for register at Address 0x0D1, bit 7 (dpll_mon_tl_mask_0::pslhit).
6	reserved	
5	flhit	See description for register at Address 0x0D1, bit 5 (dpll_mon_tl_mask_0::flhit).
4:3	reserved	
2	ho_ready	See description for register at Address 0x0D1, bit 2 (dpll_mon_tl_mask_0::ho_ready).
1	ho	See description for register at Address 0x0D1, bit 1 (dpll_mon_tl_mask_0::ho).
0	lock	See description for register at Address 0x0D1, bit 0 (dpll_mon_tl_mask_0::lock).

Address:	0x00D4	
Name:	dpll_mon_th_mask_2	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	pslhit	See description for register at Address 0x0D0, bit 7 (dpll_mon_th_mask_0::pslhit).
6	state_ch	See description for register at Address 0x0D0, bit 6 (dpll_mon_th_mask_0::state_ch).
5	flhit	See description for register at Address 0x0D0, bit 5 (dpll_mon_th_mask_0::flhit).
4:3	reserved	
2	ho_ready	See description for register at Address 0x0D0, bit 2 (dpll_mon_th_mask_0::ho_ready).
1	ho	See description for register at Address 0x0D0, bit 1 (dpll_mon_th_mask_0::ho).
0	lock	See description for register at Address 0x0D0, bit 0 (dpll_mon_th_mask_0::lock).

Address:	0x00D5	
Name:	dpll_mon_tl_mask_2	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	pslhit	See description for register at Address 0x0D1, bit 7 (dpll_mon_tl_mask_0::pslhit).
6	reserved	
5	flhit	See description for register at Address 0x0D1, bit 5 (dpll_mon_tl_mask_0::flhit).
4:3	reserved	
2	ho_ready	See description for register at Address 0x0D1, bit 2

		(dpll_mon_tl_mask_0::ho_ready).
1	ho	See description for register at Address 0x0D1, bit 1 (dpll_mon_tl_mask_0::ho).
0	lock	See description for register at Address 0x0D1, bit 0 (dpll_mon_tl_mask_0::lock).

Address:	0x00D6	
Name:	dpll_mon_th_mask_3	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	pslhit	See description for register at Address 0x0D0, bit 7 (dpll_mon_th_mask_0::pslhit).
6	state_ch	See description for register at Address 0x0D0, bit 6 (dpll_mon_th_mask_0::state_ch).
5	flhit	See description for register at Address 0x0D0, bit 5 (dpll_mon_th_mask_0::flhit).
4:3	reserved	
2	ho_ready	See description for register at Address 0x0D0, bit 2 (dpll_mon_th_mask_0::ho_ready).
1	ho	See description for register at Address 0x0D0, bit 1 (dpll_mon_th_mask_0::ho).
0	lock	See description for register at Address 0x0D0, bit 0 (dpll_mon_th_mask_0::lock).

Address:	0x00D7	
Name:	dpll_mon_tl_mask_3	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	pslhit	See description for register at Address 0x0D1, bit 7 (dpll_mon_tl_mask_0::pslhit).
6	reserved	
5	flhit	See description for register at Address 0x0D1, bit 5 (dpll_mon_tl_mask_0::flhit).
4:3	reserved	
2	ho_ready	See description for register at Address 0x0D1, bit 2 (dpll_mon_tl_mask_0::ho_ready).
1	ho	See description for register at Address 0x0D1, bit 1 (dpll_mon_tl_mask_0::ho).
0	lock	See description for register at Address 0x0D1, bit 0 (dpll_mon_tl_mask_0::lock).

Address:	0x00D8	
Name:	dpll_mon_th_mask_4	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	pslhit	See description for register at address 0x0D0, bit 7 (dpll_mon_th_mask_0::pslhit).
6	state_ch	See description for register at address 0x0D0, bit 6 (dpll_mon_th_mask_0::state_ch).
5	flhit	See description for register at address 0x0D0, bit 5 (dpll_mon_th_mask_0::flhit).

4:3	reserved	
2	ho_ready	See description for register at address 0x0D0, bit 2 (dpll_mon_th_mask_0::ho_ready).
1	ho	See description for register at address 0x0D0, bit 1 (dpll_mon_th_mask_0::ho).
0	lock	See description for register at address 0x0D0, bit 0 (dpll_mon_th_mask_0::lock).

Address:	0x00D9	
Name:	dpll_mon_tl_mask_4	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	pslhit	See description for register at address 0x0D1, bit 7 (dpll_mon_tl_mask_0::pslhit).
6	reserved	
5	flhit	See description for register at address 0x0D1, bit 5 (dpll_mon_tl_mask_0::flhit).
4:3	reserved	
2	ho_ready	See description for register at address 0x0D1, bit 2 (dpll_mon_tl_mask_0::ho_ready).
1	ho	See description for register at address 0x0D1, bit 1 (dpll_mon_tl_mask_0::ho).
0	lock	See description for register at address 0x0D1, bit 0 (dpll_mon_tl_mask_0::lock).

Address:	0x00DA	
Name:	dpll_mon_th_mask_5	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	pslhit	See description for register at address 0x0D0, bit 7 (dpll_mon_th_mask_0::pslhit).
6	state_ch	See description for register at address 0x0D0, bit 6 (dpll_mon_th_mask_0::state_ch).
5	flhit	See description for register at address 0x0D0, bit 5 (dpll_mon_th_mask_0::flhit).
4:3	reserved	
2	ho_ready	See description for register at address 0x0D0, bit 2 (dpll_mon_th_mask_0::ho_ready).
1	ho	See description for register at address 0x0D0, bit 1 (dpll_mon_th_mask_0::ho).
0	lock	See description for register at address 0x0D0, bit 0 (dpll_mon_th_mask_0::lock).

Address:	0x00DB	
Name:	dpll_mon_tl_mask_5	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	pslhit	See description for register at address 0x0D1, bit 7 (dpll_mon_tl_mask_0::pslhit).
6	reserved	
5	flhit	See description for register at address 0x0D1, bit 5 (dpll_mon_tl_mask_0::flhit).

4:3	reserved	
2	ho_ready	See description for register at address 0x0D1, bit 2 (dpll_mon_tl_mask_0::ho_ready).
1	ho	See description for register at address 0x0D1, bit 1 (dpll_mon_tl_mask_0::ho).
0	lock	See description for register at address 0x0D1, bit 0 (dpll_mon_tl_mask_0::lock).

Address:	0x00E0	
Name:	gp_mon_th_mask	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	
5	io_align_done_1	See description for io_align_done_0.
4	io_align_done_0	0: GPOUT0 I/O alignment status transitions 0->1 are masked. 1: GPOUT0 I/O alignment status transitions 0->1 are unmasked. A GPIO interrupt will be generated and register 0x1AC bit 0 (synth_irq_active::irq_0) will be set to 1.
3	reserved	
2	lock	0: GP-Synth0 lock status transitions 0->1 are masked. 1: GP-Synth0 lock status transitions 0->1 are unmasked. A GPIO interrupt will be generated and register 0x1AC bit 0 (synth_irq_active::irq_0) will be set to 1.
1:0	reserved	

Address:	0x00E1	
Name:	gp_mon_tl_mask	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:3	reserved	
2	lock	0: GP-Synth0 lock status transitions 1->0 are masked. 1: GP-Synth0 lock status transitions 1->0 are unmasked. A GPIO interrupt will be generated and register 0x1AC bit 0 (synth_irq_active::irq_0) will be set to 1.
1:0	reserved	

Address:	0x00E2	
Name:	hp_mon_th_mask_1	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:3	reserved	
2	freq_lo	0: HP-Synth1 frequency too low transitions 0->1 are masked. 1: HP-Synth1 frequency too low transitions 0->1 are unmasked. A GPIO interrupt will be generated and register 0x1AC bit 1 (synth_irq_active::irq_0) will be set to 1.
1	freq_hi	0: HP-Synth1 frequency too high transitions 0->1 are masked. 1: HP-Synth1 frequency too high transitions 0->1 are unmasked. A GPIO interrupt will be generated and register 0x1AC bit 1 (synth_irq_active::irq_0) will be set to 1.
0	lock	0: HP-Synth1 lock transitions 0->1 are masked. 1: HP-Synth1 lock transitions 0->1 are unmasked. A GPIO interrupt will be generated and register 0x1AC bit 1 (synth_irq_active::irq_0) will be set to 1.

Address:	0x00E3	
Name:	hp_mon_tl_mask_1	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:3	reserved	
2	freq_lo	0: HP-Synth1 frequency too low transitions 1->0 are masked. 1: HP-Synth1 frequency too low transitions 1->0 are unmasked. A GPIO interrupt will be generated and register 0x1AC bit 1 (synth_irq_active::irq_0) will be set to 1.
1	freq_hi	0: HP-Synth1 frequency too high transitions 1->0 are masked. 1: HP-Synth1 frequency too high transitions 1->0 are unmasked. A GPIO interrupt will be generated and register 0x1AC bit 1 (synth_irq_active::irq_0) will be set to 1.
0	lock	0: HP-Synth1 lock transitions 1->0 are masked. 1: HP-Synth1 lock transitions 1->0 are unmasked. A GPIO interrupt will be generated and register 0x1AC bit 1 (synth_irq_active::irq_0) will be set to 1.

Address:	0x00E4	
Name:	hp_mon_th_mask_2	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:3	reserved	
2	freq_lo	See description for register at Address 0x0E2, bit 2 (hp_mon_th_mask_1::freq_lo).
1	freq_hi	See description for register at Address 0x0E2, bit 1 (hp_mon_th_mask_1::freq_hi).
0	lock	See description for register at Address 0x0E2, bit 0 (hp_mon_th_mask_1::lock).

Address:	0x00E5	
Name:	hp_mon_tl_mask_2	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:3	reserved	
2	freq_lo	See description for register at Address 0x0E3, bit 2 (hp_mon_tl_mask_1::freq_lo).
1	freq_hi	See description for register at Address 0x0E3, bit 1 (hp_mon_tl_mask_1::freq_hi).
0	lock	See description for register at Address 0x0E3, bit 0 (hp_mon_tl_mask_1::lock).

Address:	0x00E6	
Name:	hp_out_th_mask_0	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	0: HPOUT0 low-speed clock transitions 0->1 are masked. 1: HPOUT0 low-speed clock transitions 0->1 are unmasked. A GPIO interrupt will be generated and register 0x1AD bit 1 (hp_out_irq_active::irq_0) will be set to 1.

0	stopd	0: HPOUT0 stopped transitions 0->1 are masked. 1: HPOUT0 stopped transitions 0->1 are unmasked. A GPIO interrupt will be generated and register 0x1AD bit 1 (hp_out_irq_active::irq_0) will be set to 1.

Address:	0x00E7	
Name:	hp_out_tl_mask_0	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	0: HPOUT0 low-speed clock transitions 1->0 are masked. 1: HPOUT0 low-speed clock transitions 1->0 are unmasked. A GPIO interrupt will be generated and register 0x1AD bit 1 (hp_out_irq_active::irq_0) will be set to 1.
0	stopd	0: HPOUT0 stopped transitions 1->0 are masked. 1: HPOUT0 stopped transitions 1->0 are unmasked. A GPIO interrupt will be generated and register 0x1AD bit 1 (hp_out_irq_active::irq_0) will be set to 1.

Address:	0x00E8	
Name:	hp_out_th_mask_1	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x0E6, bit 1 (hp_out_th_mask_0::lsclk).
0	stopd	See description for register at Address 0x0E6, bit 0 (hp_out_th_mask_0::stopd).

Address:	0x00E9	
Name:	hp_out_tl_mask_1	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x0E7, bit 1 (hp_out_th_mask_0::lsclk).
0	stopd	See description for register at Address 0x0E7, bit 0 (hp_out_th_mask_0::stopd).

Address:	0x00EA	
Name:	hp_out_th_mask_2	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x0E6, bit 1 (hp_out_th_mask_0::lsclk).
0	stopd	See description for register at Address 0x0E6, bit 0 (hp_out_th_mask_0::stopd).

Address:	0x00EB	
Name:	hp_out_tl_mask_2	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x0E7, bit 1 (hp_out_th_mask_0::lsclk).
0	stopd	See description for register at Address 0x0E7, bit 0 (hp_out_th_mask_0::stopd).

Address:	0x00EC	
Name:	hp_out_th_mask_3	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x0E6, bit 1 (hp_out_th_mask_0::lsclk).
0	stopd	See description for register at Address 0x0E6, bit 0 (hp_out_th_mask_0::stopd).

Address:	0x00ED	
Name:	hp_out_tl_mask_3	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x0E7, bit 1 (hp_out_th_mask_0::lsclk).
0	stopd	See description for register at Address 0x0E7, bit 0 (hp_out_th_mask_0::stopd).

Address:	0x00EE	
Name:	hp_out_th_mask_4	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x0E6, bit 1 (hp_out_th_mask_0::lsclk).
0	stopd	See description for register at Address 0x0E6, bit 0 (hp_out_th_mask_0::stopd).

Address:	0x00EF	
Name:	hp_out_tl_mask_4	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x0E7, bit 1 (hp_out_th_mask_0::lsclk).
0	stopd	See description for register at Address 0x0E7, bit 0 (hp_out_th_mask_0::stopd).

Address:	0x00F0	
Name:	hp_out_th_mask_5	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x0E6, bit 1 (hp_out_th_mask_0::lsclk).
0	stopd	See description for register at Address 0x0E6, bit 0 (hp_out_th_mask_0::stopd).

Address:	0x00F1	
Name:	hp_out_tl_mask_5	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x0E7, bit 1 (hp_out_th_mask_0::lsclk).
0	stopd	See description for register at Address 0x0E7, bit 0 (hp_out_th_mask_0::stopd).

Address:	0x00F2	
Name:	hp_out_th_mask_6	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x0E6, bit 1 (hp_out_th_mask_0::lsclk).
0	stopd	See description for register at Address 0x0E6, bit 0 (hp_out_th_mask_0::stopd).

Address:	0x00F3	
Name:	hp_out_tl_mask_6	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x0E7, bit 1 (hp_out_th_mask_0::lsclk).
0	stopd	See description for register at Address 0x0E7, bit 0 (hp_out_th_mask_0::stopd).

Address:	0x00F4	
Name:	hp_out_th_mask_7	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x0E6, bit 1 (hp_out_th_mask_0::lsclk).
0	stopd	See description for register at Address 0x0E6, bit 0 (hp_out_th_mask_0::stopd).

Address:	0x00F5	
Name:	hp_out_tl_mask_7	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x0E7, bit 1 (hp_out_th_mask_0::lsclk).
0	stopd	See description for register at Address 0x0E7, bit 0 (hp_out_th_mask_0::stopd).

Address:	0x00FE	
Name:	uport	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	lockout	When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing.
6:1	reserved	
0	status	This field indicates if microport attempted access had not been successful. The register content will be 0x00 if the access had been successful.

Address:	0x00FF	
Name:	page_sel	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		Unsigned binary value of these bits represents selected page for SPI/I2C access: 0x00: page 0 (first 128 bytes) 0x01: page 1 (second 128 bytes) 0x02: page 2 (third 128 bytes) 0x03: page 3 (fourth 128 bytes) 0x04: page 4 (fifth 128 bytes) 0x05: page 5 (sixth 128 bytes) 0x06: page 6 (seventh 128 bytes) 0x07: page 7 (eighth 128 bytes) 0x08: page 8 (ninth 128 bytes) 0x09: page 9 (tenth 128 bytes) 0x0A: page 10 (eleventh 128 bytes) 0x0B: page 11 (twelfth 128 bytes) 0x0C: page 12 (thirteenth 128 bytes) 0x0D-0xFF: reserved

9.3.3 Register List Page 2, Status

Address:	0x0100	
Name:	gpio_in_status_2_0	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7:3	reserved	
2	gpio2	See description for gpio0.
1	gpio1	See description for gpio0.
0	gpio0	Logic value seen on pin GPIO0 if it is configured as input, control

		or LOS mode.

Address:	0x0101	
Name:	gpio_in_status_8_5	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7:4	reserved	
3	gpio8	See description for gpio5.
2	gpio7	See description for gpio5.
1	gpio6	See description for gpio5.
0	gpio5	Logic value seen on pin GPIO5 if it is configured as input or status mode.

Address:	0x0108	
Name:	ref_mon_status_0P	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	0: No SFM failure on REF0P. 1: SFM failure on REF0P detected. Note: This bit will not clear to 0 automatically. To clear this bit to 0, set register at Address 0x0203 bit 0 (ref_sfm_clr_3_0::clr_0P) to 1.
4	pfm	0: No PFM failure on REF0P. 1: PFM failure on REF0P detected.
3	gst	0: No GST failure on REF0P. 1: GST failure on REF0P detected.
2	cfm	0: No CFM failure on REF0P. 1: CFM failure on REF0P detected.
1	scm	0: No SCM failure on REF0P. 1: SCM failure on REF0P detected.
0	los	0: No LOS failure on REF0P. 1: LOS failure on REF0P detected.

Address:	0x0109	
Name:	ref_mon_status_0N	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at address 0x108, bit 5 (ref_mon_status_0P::sfm).
4	pfm	See description for register at address 0x108, bit 4 (ref_mon_status_0P::pfm).
3	gst	See description for register at address 0x108, bit 3 (ref_mon_status_0P::gst).
2	cfm	See description for register at address 0x108, bit 2 (ref_mon_status_0P::cfm).
1	scm	See description for register at address 0x108, bit 1 (ref_mon_status_0P::scm).
0	los	See description for register at address 0x108, bit 0 (ref_mon_status_0P::los).

Address:	0x010A	
Name:	ref_mon_status_1P	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at address 0x108, bit 5 (ref_mon_status_0P::sfm).
4	pfm	See description for register at address 0x108, bit 4 (ref_mon_status_0P::pfm).
3	gst	See description for register at address 0x108, bit 3 (ref_mon_status_0P::gst).
2	cfm	See description for register at address 0x108, bit 2 (ref_mon_status_0P::cfm).
1	scm	See description for register at address 0x108, bit 1 (ref_mon_status_0P::scm).
0	los	See description for register at address 0x108, bit 0 (ref_mon_status_0P::los).

Address:	0x010B	
Name:	ref_mon_status_1N	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at address 0x108, bit 5 (ref_mon_status_0P::sfm).
4	pfm	See description for register at address 0x108, bit 4 (ref_mon_status_0P::pfm).
3	gst	See description for register at address 0x108, bit 3 (ref_mon_status_0P::gst).
2	cfm	See description for register at address 0x108, bit 2 (ref_mon_status_0P::cfm).
1	scm	See description for register at address 0x108, bit 1 (ref_mon_status_0P::scm).
0	los	See description for register at address 0x108, bit 0 (ref_mon_status_0P::los).

Address:	0x010C	
Name:	ref_mon_status_2P	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at address 0x108, bit 5 (ref_mon_status_0P::sfm).
4	pfm	See description for register at address 0x108, bit 4 (ref_mon_status_0P::pfm).
3	gst	See description for register at address 0x108, bit 3 (ref_mon_status_0P::gst).
2	cfm	See description for register at address 0x108, bit 2 (ref_mon_status_0P::cfm).
1	scm	See description for register at address 0x108, bit 1 (ref_mon_status_0P::scm).

0	los	See description for register at address 0x108, bit 0 (ref_mon_status_0P::los).

Address:	0x010D	
Name:	ref_mon_status_2N	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at address 0x108, bit 5 (ref_mon_status_0P::sfm).
4	pfm	See description for register at address 0x108, bit 4 (ref_mon_status_0P::pfm).
3	gst	See description for register at address 0x108, bit 3 (ref_mon_status_0P::gst).
2	cfm	See description for register at address 0x108, bit 2 (ref_mon_status_0P::cfm).
1	scm	See description for register at address 0x108, bit 1 (ref_mon_status_0P::scm).
0	los	See description for register at address 0x108, bit 0 (ref_mon_status_0P::los).

Address:	0x010E	
Name:	ref_mon_status_3P	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at address 0x108, bit 5 (ref_mon_status_0P::sfm).
4	pfm	See description for register at address 0x108, bit 4 (ref_mon_status_0P::pfm).
3	gst	See description for register at address 0x108, bit 3 (ref_mon_status_0P::gst).
2	cfm	See description for register at address 0x108, bit 2 (ref_mon_status_0P::cfm).
1	scm	See description for register at address 0x108, bit 1 (ref_mon_status_0P::scm).
0	los	See description for register at address 0x108, bit 0 (ref_mon_status_0P::los).

Address:	0x010F	
Name:	ref_mon_status_3N	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at address 0x108, bit 5 (ref_mon_status_0P::sfm).
4	pfm	See description for register at address 0x108, bit 4 (ref_mon_status_0P::pfm).
3	gst	See description for register at address 0x108, bit 3 (ref_mon_status_0P::gst).
2	cfm	See description for register at address 0x108, bit 2 (ref_mon_status_0P::cfm).

1	scm	See description for register at address 0x108, bit 1 (ref_mon_status_0P::scm).
0	los	See description for register at address 0x108, bit 0 (ref_mon_status_0P::los).

Address:	0x0110	
Name:	ref_mon_status_4P	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at address 0x108, bit 5 (ref_mon_status_0P::sfm).
4	pfm	See description for register at address 0x108, bit 4 (ref_mon_status_0P::pfm).
3	gst	See description for register at address 0x108, bit 3 (ref_mon_status_0P::gst).
2	cfm	See description for register at address 0x108, bit 2 (ref_mon_status_0P::cfm).
1	scm	See description for register at address 0x108, bit 1 (ref_mon_status_0P::scm).
0	los	See description for register at address 0x108, bit 0 (ref_mon_status_0P::los).

Address:	0x0111	
Name:	ref_mon_status_4N	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at address 0x108, bit 5 (ref_mon_status_0P::sfm).
4	pfm	See description for register at address 0x108, bit 4 (ref_mon_status_0P::pfm).
3	gst	See description for register at address 0x108, bit 3 (ref_mon_status_0P::gst).
2	cfm	See description for register at address 0x108, bit 2 (ref_mon_status_0P::cfm).
1	scm	See description for register at address 0x108, bit 1 (ref_mon_status_0P::scm).
0	los	See description for register at address 0x108, bit 0 (ref_mon_status_0P::los).

Address:	0x0118	
Name:	dpll_mon_status_0	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7	pslhit	0: DPLL0 is below the configured phase slope limit. 1: DPLL0 has hit the configured phase slope limit.
6	reserved	
5	flhit	0: DPLL0 is within the configured pull-in/hold-in range limit. 1: DPLL0 has hit the specified pull-in/hold-in range limit.
4:3	reserved	
2	ho_ready	0: DPLL0 holdover storage delay requirements not met

		1: DPLL0 holdover value will have the programmed storage delay applied This bit is cleared when the DPLL is forced to freerun, upon DPLL change of REF, and upon DPLL exit from holdover. See mailbox register at Address 0x61D (dpll_ho_delay) for details on holdover storage delay.
1	ho	0: DPLL0 is not in holdover 1: DPLL0 is in holdover
0	lock	0: DPLL0 is not locked 1: DPLL0 is locked

Address:	0x0119	
Name:	dpll_mon_status_1	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7	pslhit	See description for register at Address 0x118, bit 7 (dpll_mon_status_0::pslhit).
6	reserved	
5	flhit	See description for register at Address 0x118, bit 5 (dpll_mon_status_0::flhit).
4:3	reserved	
2	ho_ready	See description for register at Address 0x118, bit 2 (dpll_mon_status_0::ho_ready).
1	ho	See description for register at Address 0x118, bit 1 (dpll_mon_status_0::ho).
0	lock	See description for register at Address 0x118, bit 0 (dpll_mon_status_0::lock).

Address:	0x011A	
Name:	dpll_mon_status_2	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7	pslhit	See description for register at Address 0x118, bit 7 (dpll_mon_status_0::pslhit).
6	reserved	
5	flhit	See description for register at Address 0x118, bit 5 (dpll_mon_status_0::flhit).
4:3	reserved	
2	ho_ready	See description for register at Address 0x118, bit 2 (dpll_mon_status_0::ho_ready).
1	ho	See description for register at Address 0x118, bit 1 (dpll_mon_status_0::ho).
0	lock	See description for register at Address 0x118, bit 0 (dpll_mon_status_0::lock).

Address:	0x011B	
Name:	dpll_mon_status_3	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7	pslhit	See description for register at Address 0x118, bit 7 (dpll_mon_status_0::pslhit).

6	reserved	
5	flhit	See description for register at Address 0x118, bit 5 (dpll_mon_status_0::flhit).
4:3	reserved	
2	ho_ready	See description for register at Address 0x118, bit 2 (dpll_mon_status_0::ho_ready).
1	ho	See description for register at Address 0x118, bit 1 (dpll_mon_status_0::ho).
0	lock	See description for register at Address 0x118, bit 0 (dpll_mon_status_0::lock).

Address:	0x011C	
Name:	dpll_mon_status_4	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7	pslhit	See description for register at address 0x118, bit 7 (dpll_mon_status_0::pslhit).
6	reserved	
5	flhit	See description for register at address 0x118, bit 5 (dpll_mon_status_0::flhit).
4:3	reserved	
2	ho_ready	See description for register at address 0x118, bit 2 (dpll_mon_status_0::ho_ready).
1	ho	See description for register at address 0x118, bit 1 (dpll_mon_status_0::ho).
0	lock	See description for register at address 0x118, bit 0 (dpll_mon_status_0::lock).
Address:	0x011D	
Name:	dpll_mon_status_5	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7	pslhit	See description for register at address 0x118, bit 7 (dpll_mon_status_0::pslhit).
6	reserved	
5	flhit	See description for register at address 0x118, bit 5 (dpll_mon_status_0::flhit).
4:3	reserved	
2	ho_ready	See description for register at address 0x118, bit 2 (dpll_mon_status_0::ho_ready).
1	ho	See description for register at address 0x118, bit 1 (dpll_mon_status_0::ho).
0	lock	See description for register at address 0x118, bit 0 (dpll_mon_status_0::lock).

Address:	0x0120	
Name:	dpll_state_refsel_0	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7:4	refsel	Indicates the reference selected by DPLL0.
3	reserved	
2:0	state	0: FREERUN (or NCO mode) 1: HOLDOVER

		2: FAST_LOCK 3: ACQUIRING 4: LOCK

Address:	0x0121	
Name:	dpll_state_refsel_1	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7:4	refsel	See description for register at Address 0x120, bits 7:4 (dpll_state_refsel_0::refsel).
3	reserved	
2:0	state	See description for register at Address 0x120, bits 2:0 (dpll_state_refsel_0::state).

Address:	0x0122	
Name:	dpll_state_refsel_2	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7:4	refsel	See description for register at Address 0x120, bits 7:4 (dpll_state_refsel_0::refsel).
3	reserved	
2:0	state	See description for register at Address 0x120, bits 2:0 (dpll_state_refsel_0::state).

Address:	0x0123	
Name:	dpll_state_refsel_3	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7:4	refsel	See description for register at Address 0x120, bits 7:4 (dpll_state_refsel_0::refsel).
3	reserved	
2:0	state	See description for register at Address 0x120, bits 2:0 (dpll_state_refsel_0::state).

Address:	0x0130	
Name:	dpll_df_timer_status	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7:3	reserved	
2	timer_2	See description for timer_0.
1	timer_1	See description for timer_0.
0	timer_0	0: DPLL0 temporary df is not being applied. 1: DPLL0 temporary df is being applied. Note: See register at Addresses 0x30C-0x310 (dpll_df_temp_0) and register at Addresses 0x311-0x312 (dpll_df_timer_0) for more details.

Address:	0x013F	
Name:	synth_fine_shift_status	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7:1	reserved	
0	synth0	0: GP-Synth0 fine phase shift is not in-progress. 1: GP-Synth0 fine phase shift in-progress.

Address:	0x0140	
Name:	gp_mon_status	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7:6	reserved	
5	io_align_done_1	See description for io_align_done_0.
4	io_align_done_0	0: GPOUT0 I/O alignment has not completed. 1: GPOUT0 I/O alignment completed. This bit will be cleared when GPOUT0 or GP-Synth0 is disabled.
3	reserved	
2	lock	0: GP-Synth0 is not locked (VCO frequency is out of the correct range). 1: GP-Synth0 is locked (VCO frequency is in the correct range).
1:0	reserved	

Address:	0x0141	
Name:	hp_mon_status_1	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7:3	reserved	
2	freq_lo	0: HP-Synth1 is not reporting its input frequency is too low. 1: HP-Synth1 is reporting its input frequency is too low.
1	freq_hi	0: HP-Synth1 is not reporting its input frequency is too high. 1: HP-Synth1 is reporting its input frequency is too high.
0	lock	0: HP-Synth1 is not locked (VCO frequency is out of the correct range). 1: HP-Synth1 is locked (VCO frequency is in the correct range).

Address:	0x0142	
Name:	hp_mon_status_2	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7:3	reserved	
2	freq_lo	See description for register at Address 0x141, bit 2 (hp_mon_status_1::freq_lo).
1	freq_hi	See description for register at Address 0x141, bit 1 (hp_mon_status_1::freq_hi).
0	lock	See description for register at Address 0x141, bit 0 (hp_mon_status_1::lock).

Address:	0x0143	
Name:	hp_out_mon_status_0	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	0: HPOUT0 is low. 1: HPOUT0 is high. This bit is typically only useful when HPOUT0 is stopped or has very low frequency such as 1Hz. This bit must be enabled by setting hp_out_lsctrl_0::srlsen=1 (see register 0x508, bit 7).
0	stopd	0: HPOUT0 is not stopped. 1: HPOUT0 is stopped.

Address:	0x0144	
Name:	hp_out_mon_status_1	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x143, bit 1 (hp_out_mon_status_0::lsclk).
0	stopd	See description for register at Address 0x143, bit 0 (hp_out_mon_status_0::stopd).

Address:	0x0145	
Name:	hp_out_mon_status_2	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x143, bit 1 (hp_out_mon_status_0::lsclk).
0	stopd	See description for register at Address 0x143, bit 0 (hp_out_mon_status_0::stopd).

Address:	0x0146	
Name:	hp_out_mon_status_3	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x143, bit 1 (hp_out_mon_status_0::lsclk).
0	stopd	See description for register at Address 0x143, bit 0 (hp_out_mon_status_0::stopd).

Address:	0x0147	
Name:	hp_out_mon_status_4	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x143, bit 1 (hp_out_mon_status_0::lsclk).

0	stopd	See description for register at Address 0x143, bit 0 (hp_out_mon_status_0::stopd).

Address:	0x0148	
Name:	hp_out_mon_status_5	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x143, bit 1 (hp_out_mon_status_0::lsclk).
0	stopd	See description for register at Address 0x143, bit 0 (hp_out_mon_status_0::stopd).

Address:	0x0149	
Name:	hp_out_mon_status_6	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x143, bit 1 (hp_out_mon_status_0::lsclk).
0	stopd	See description for register at Address 0x143, bit 0 (hp_out_mon_status_0::stopd).

Address:	0x014A	
Name:	hp_out_mon_status_7	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x143, bit 1 (hp_out_mon_status_0::lsclk).
0	stopd	See description for register at Address 0x143, bit 0 (hp_out_mon_status_0::stopd).

Address:	0x0150	
Name:	hp_fb_msdiv_sel_1	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7:0		HP-Synth1 feedback signal MSDIV value. This register will read back 0x00 if HP-Synth1 is disabled.

Address:	0x0151:0x0154	
Name:	hp_fb_lsdiv_sel_1	
Default:	0x00000000	
Type:	R	
Bit Field	Function Name	Description
31:0		HP-Synth1 feedback signal LSDIV value. Bits 31:26 will always be 0. This register will read back 0x00000000 if HP-Synth1 is disabled.

Address:	0x0158	
Name:	hp_fb_msdiv_sel_2	
Default:	0x00	
Type:	R	
Bit Field	Function Name	Description
7:0		See description for register at Address 0x150 (hp_fb_msdiv_sel_1).

Address:	0x0159:0x015C	
Name:	hp_fb_lsdiv_sel_2	
Default:	0x00000000	
Type:	R	
Bit Field	Function Name	Description
31:0		See description for register at Addresses 0x151-0x154 (hp_fb_lsdiv_sel_1).

Address:	0x017E	
Name:	uport	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	lockout	When set, this field causes all other uport registers to be host read-only. When zero, all registers are open for writing.
6:1	reserved	
0	status	This field indicates if microport attempted access had not been successful. The register content will be 0x00 if the access had been successful.

Address:	0x017F	
Name:	page_sel	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		Unsigned binary value of these bits represents selected page for SPI/I2C access: 0x00: page 0 (first 128 bytes) 0x01: page 1 (second 128 bytes) 0x02: page 2 (third 128 bytes) 0x03: page 3 (fourth 128 bytes) 0x04: page 4 (fifth 128 bytes) 0x05: page 5 (sixth 128 bytes) 0x06: page 6 (seventh 128 bytes) 0x07: page 7 (eighth 128 bytes) 0x08: page 8 (ninth 128 bytes) 0x09: page 9 (tenth 128 bytes) 0x0A: page 10 (eleventh 128 bytes) 0x0B: page 11 (twelfth 128 bytes) 0x0C: page 12 (thirteenth 128 bytes) 0x0D-0xFF: reserved

9.3.4 Register List Page 3, Sticky

Address:	0x0180	
Name:	sticky_lock	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		This register needs to be set to a non-zero value prior to clearing sticky bits, to avoid race condition that can happen when the internal processor updates the register while the host clears the bit. Having non-zero value in this register will prevent the internal processor from updating the sticky bit registers. For proper sticky bit monitoring, the following procedure is recommended: 1) Write non-zero value into this register 2) Clear sticky bits in other registers 3) Write 0 into this register 4) Read sticky bits status registers

Address:	0x0181	
Name:	gpio_latch_status_8_5	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:4	reserved	
3	gpio8	See gpio5 bit description below.
2	gpio7	See gpio5 bit description below.
1	gpio6	See gpio5 bit description below.
0	gpio5	0: GPIO5 has not changed state since the last time this bit was written with a 0. 1: GPIO5 has changed state, either 0->1 or 1->0.

Address:	0x018A	
Name:	dpll_fast_lock_sticky	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:6	reserved	
5	dpll_5	See dpll_0 bit description below.
4	dpll_4	See dpll_0 bit description below.
3	dpll_3	See dpll_0 bit description below.
2	dpll_2	See dpll_0 bit description below.
1	dpll_1	See dpll_0 bit description below.
0	dpll_0	0: DPLL0 has no unacknowledged fast lock state entry status. 1: DPLL0 entered fast lock state, not yet acknowledged.

Address:	0x018B	
Name:	dpll_fast_lock_phase_sticky	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:4	reserved	
3	dpll_3	0: DPLL3 has no unacknowledged fast lock phase error status. 1: DPLL3 fast lock phase error threshold exceeded, not yet acknowledged.

2	dpll_2	0: DPLL2 has no unacknowledged fast lock phase error status. 1: DPLL2 fast lock phase error threshold exceeded, not yet acknowledged.
1	dpll_1	0: DPLL1 has no unacknowledged fast lock phase error status. 1: DPLL1 fast lock phase error threshold exceeded, not yet acknowledged.
0	dpll_0	0: DPLL0 has no unacknowledged fast lock phase error status. 1: DPLL0 fast lock phase error threshold exceeded, not yet acknowledged.

Address:	0x018C	
Name:	dpll_fast_lock_freq_sticky	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:4	reserved	
3	dpll_3	0: DPLL3 has no unacknowledged fast lock frequency error status. 1: DPLL3 fast lock frequency error threshold exceeded, not yet acknowledged.
2	dpll_2	0: DPLL2 has no unacknowledged fast lock frequency error status. 1: DPLL2 fast lock frequency error threshold exceeded, not yet acknowledged.
1	dpll_1	0: DPLL1 has no unacknowledged fast lock frequency error status. 1: DPLL1 fast lock frequency error threshold exceeded, not yet acknowledged.
0	dpll_0	0: DPLL0 has no unacknowledged fast lock frequency error status. 1: DPLL0 fast lock frequency error threshold exceeded, not yet acknowledged.

Address:	0x018D	
Name:	dpll_tie_wr_sticky	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:3	reserved	
2	dpll_2	0: DPLL2 has no unacknowledged TIE write status. 1: DPLL2 TIE write completed, not yet acknowledged.
1	dpll_1	0: DPLL1 has no unacknowledged TIE write status. 1: DPLL1 TIE write completed, not yet acknowledged.
0	dpll_0	0: DPLL0 has no unacknowledged TIE write status. 1: DPLL0 TIE write completed, not yet acknowledged.

Address:	0x0190	
Name:	gp_out_phase_step_sticky	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:2	reserved	
1	out_1	0: GPOUT1 has no unacknowledged phase step status. 1: GPOUT1 phase step has completed, not yet acknowledged.
0	out_0	0: GPOUT0 has no unacknowledged phase step status. 1: GPOUT0 phase step has completed, not yet acknowledged.

Address:	0x0191	
Name:	hp_out_phase_step_sticky	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7	out_7	See out_0 bit description below.
6	out_6	See out_0 bit description below.
5	out_5	See out_0 bit description below.
4	out_4	See out_0 bit description below.
3	out_3	See out_0 bit description below.
2	out_2	See out_0 bit description below.
1	out_1	See out_0 bit description below.
0	out_0	0: HPOUT0 has no unacknowledged phase step status. 1: HPOUT0 phase step has completed, not yet acknowledged.

Address:	0x01A8	
Name:	ref_irq_active_3_0	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7	irq_3N	See irq_0P bit description below.
6	irq_3P	See irq_0P bit description below.
5	irq_2N	See irq_0P bit description below.
4	irq_2P	See irq_0P bit description below.
3	irq_1N	See irq_0P bit description below.
2	irq_1P	See irq_0P bit description below.
1	irq_0N	See irq_0P bit description below.
0	irq_0P	0: REF0P has no unacknowledged interrupts. 1: REF0P interrupt has occurred, not yet acknowledged.

Address:	0x01A9	
Name:	ref_irq_active_4	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:2	reserved	
1	irq_4N	See description for register at Address 0x1A8, bit 0 (ref_irq_active_3_0::irq_0P).
0	irq_4P	See description for register at Address 0x1A8, bit 0 (ref_irq_active_3_0::irq_0P).

Address:	0x01AB	
Name:	dpll_irq_active	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:6	reserved	
5	irq_5	See irq_0 bit description below.
4	irq_4	See irq_0 bit description below.
3	irq_3	See irq_0 bit description below.
2	irq_2	See irq_0 bit description below.
1	irq_1	See irq_0 bit description below.
0	irq_0	0: DPLL0 has no unacknowledged interrupts. 1: DPLL0 interrupt has occurred, not yet acknowledged.

Address:	0x01AC	
Name:	synth_irq_active	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:3	reserved	
2	irq_2	See irq_0 bit description below.
1	irq_1	See irq_0 bit description below.
0	irq_0	0: synth0 has no unacknowledged interrupts. 1: synth0 interrupt has occurred, not yet acknowledged.

Address:	0x01AD	
Name:	hp_out_irq_active	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7	irq_7	See irq_0 bit description below.
6	irq_6	See irq_0 bit description below.
5	irq_5	See irq_0 bit description below.
4	irq_4	See irq_0 bit description below.
3	irq_3	See irq_0 bit description below.
2	irq_2	See irq_0 bit description below.
1	irq_1	See irq_0 bit description below.
0	irq_0	0: HPOUT0 has no unacknowledged interrupts. 1: HPOUT0 interrupt has occurred, not yet acknowledged.

Address:	0x01B0	
Name:	ref_mon_th_sticky_0P	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	0: REF0P SFM failure status has not transitioned 0->1. 1: REF0P SFM failure status transitioned 0->1, not yet acknowledged.
4	pfm	0: REF0P PFM failure status has not transitioned 0->1. 1: REF0P PFM failure status transitioned 0->1, not yet acknowledged.
3	gst	0: REF0P GST failure status has not transitioned 0->1. 1: REF0P GST failure status transitioned 0->1, not yet acknowledged.
2	cfm	0: REF0P CFM failure status has not transitioned 0->1. 1: REF0P CFM failure status transitioned 0->1, not yet acknowledged.
1	scm	0: REF0P SCM failure status has not transitioned 0->1. 1: REF0P SCM failure status transitioned 0->1, not yet acknowledged.
0	los	0: REF0P LOS failure status has not transitioned 0->1. 1: REF0P LOS failure status transitioned 0->1, not yet acknowledged.

Address:	0x01B1	
Name:	ref_mon_tl_sticky_0P	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	0: REF0P SFM failure status has not transitioned 1->0. 1: REF0P SFM failure status transitioned 1->0, not yet acknowledged.
4	pfm	0: REF0P PFM failure status has not transitioned 1->0. 1: REF0P PFM failure status transitioned 1->0, not yet acknowledged.
3	gst	0: REF0P GST failure status has not transitioned 1->0. 1: REF0P GST failure status transitioned 1->0, not yet acknowledged.
2	cfm	0: REF0P CFM failure status has not transitioned 1->0. 1: REF0P CFM failure status transitioned 1->0, not yet acknowledged.
1	scm	0: REF0P SCM failure status has not transitioned 1->0. 1: REF0P SCM failure status transitioned 1->0, not yet acknowledged.
0	los	0: REF0P LOS failure status has not transitioned 1->0. 1: REF0P LOS failure status transitioned 1->0, not yet acknowledged.

Address:	0x01B2	
Name:	ref_mon_th_sticky_0N	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x1B0, bit 5 (ref_mon_th_sticky_0P::sfm).
4	pfm	See description for register at Address 0x1B0, bit 4 (ref_mon_th_sticky_0P::pfm).
3	gst	See description for register at Address 0x1B0, bit 3 (ref_mon_th_sticky_0P::gst).
2	cfm	See description for register at Address 0x1B0, bit 2 (ref_mon_th_sticky_0P::cfm).
1	scm	See description for register at Address 0x1B0, bit 1 (ref_mon_th_sticky_0P::scm).
0	los	See description for register at Address 0x1B0, bit 0 (ref_mon_th_sticky_0P::los).

Address:	0x01B3	
Name:	ref_mon_tl_sticky_0N	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x1B1, bit 5 (ref_mon_tl_sticky_0P::sfm).
4	pfm	See description for register at Address 0x1B1, bit 4 (ref_mon_tl_sticky_0P::pfm).
3	gst	See description for register at Address 0x1B1, bit 3 (ref_mon_tl_sticky_0P::gst).

2	cfm	See description for register at Address 0x1B1, bit 2 (ref_mon_tl_sticky_0P::cfm).
1	scm	See description for register at Address 0x1B1, bit 1 (ref_mon_tl_sticky_0P::scm).
0	los	See description for register at Address 0x1B1, bit 0 (ref_mon_tl_sticky_0P::los).

Address:	0x01B4	
Name:	ref_mon_th_sticky_1P	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x1B0, bit 5 (ref_mon_th_sticky_0P::sfm).
4	pfm	See description for register at Address 0x1B0, bit 4 (ref_mon_th_sticky_0P::pfm).
3	gst	See description for register at Address 0x1B0, bit 3 (ref_mon_th_sticky_0P::gst).
2	cfm	See description for register at Address 0x1B0, bit 2 (ref_mon_th_sticky_0P::cfm).
1	scm	See description for register at Address 0x1B0, bit 1 (ref_mon_th_sticky_0P::scm).
0	los	See description for register at Address 0x1B0, bit 0 (ref_mon_th_sticky_0P::los).

Address:	0x01B5	
Name:	ref_mon_tl_sticky_1P	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x1B1, bit 5 (ref_mon_tl_sticky_0P::sfm).
4	pfm	See description for register at Address 0x1B1, bit 4 (ref_mon_tl_sticky_0P::pfm).
3	gst	See description for register at Address 0x1B1, bit 3 (ref_mon_tl_sticky_0P::gst).
2	cfm	See description for register at Address 0x1B1, bit 2 (ref_mon_tl_sticky_0P::cfm).
1	scm	See description for register at Address 0x1B1, bit 1 (ref_mon_tl_sticky_0P::scm).
0	los	See description for register at Address 0x1B1, bit 0 (ref_mon_tl_sticky_0P::los).

Address:	0x01B6	
Name:	ref_mon_th_sticky_1N	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x1B0, bit 5 (ref_mon_th_sticky_0P::sfm).
4	pfm	See description for register at Address 0x1B0, bit 4 (ref_mon_th_sticky_0P::pfm).

3	gst	See description for register at Address 0x1B0, bit 3 (ref_mon_th_sticky_0P::gst).
2	cfm	See description for register at Address 0x1B0, bit 2 (ref_mon_th_sticky_0P::cfm).
1	scm	See description for register at Address 0x1B0, bit 1 (ref_mon_th_sticky_0P::scm).
0	los	See description for register at Address 0x1B0, bit 0 (ref_mon_th_sticky_0P::los).

Address:	0x01B7	
Name:	ref_mon_tl_sticky_1N	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x1B1, bit 5 (ref_mon_tl_sticky_0P::sfm).
4	pfm	See description for register at Address 0x1B1, bit 4 (ref_mon_tl_sticky_0P::pfm).
3	gst	See description for register at Address 0x1B1, bit 3 (ref_mon_tl_sticky_0P::gst).
2	cfm	See description for register at Address 0x1B1, bit 2 (ref_mon_tl_sticky_0P::cfm).
1	scm	See description for register at Address 0x1B1, bit 1 (ref_mon_tl_sticky_0P::scm).
0	los	See description for register at Address 0x1B1, bit 0 (ref_mon_tl_sticky_0P::los).

Address:	0x01B8	
Name:	ref_mon_th_sticky_2P	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x1B0, bit 5 (ref_mon_th_sticky_0P::sfm).
4	pfm	See description for register at Address 0x1B0, bit 4 (ref_mon_th_sticky_0P::pfm).
3	gst	See description for register at Address 0x1B0, bit 3 (ref_mon_th_sticky_0P::gst).
2	cfm	See description for register at Address 0x1B0, bit 2 (ref_mon_th_sticky_0P::cfm).
1	scm	See description for register at Address 0x1B0, bit 1 (ref_mon_th_sticky_0P::scm).
0	los	See description for register at Address 0x1B0, bit 0 (ref_mon_th_sticky_0P::los).

Address:	0x01B9	
Name:	ref_mon_tl_sticky_2P	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x1B1, bit 5 (ref_mon_tl_sticky_0P::sfm).

4	pfm	See description for register at Address 0x1B1, bit 4 (ref_mon_tl_sticky_0P::pfm).
3	gst	See description for register at Address 0x1B1, bit 3 (ref_mon_tl_sticky_0P::gst).
2	cfm	See description for register at Address 0x1B1, bit 2 (ref_mon_tl_sticky_0P::cfm).
1	scm	See description for register at Address 0x1B1, bit 1 (ref_mon_tl_sticky_0P::scm).
0	los	See description for register at Address 0x1B1, bit 0 (ref_mon_tl_sticky_0P::los).

Address:	0x01BA	
Name:	ref_mon_th_sticky_2N	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x1B0, bit 5 (ref_mon_th_sticky_0P::sfm).
4	pfm	See description for register at Address 0x1B0, bit 4 (ref_mon_th_sticky_0P::pfm).
3	gst	See description for register at Address 0x1B0, bit 3 (ref_mon_th_sticky_0P::gst).
2	cfm	See description for register at Address 0x1B0, bit 2 (ref_mon_th_sticky_0P::cfm).
1	scm	See description for register at Address 0x1B0, bit 1 (ref_mon_th_sticky_0P::scm).
0	los	See description for register at Address 0x1B0, bit 0 (ref_mon_th_sticky_0P::los).

Address:	0x01BB	
Name:	ref_mon_tl_sticky_2N	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x1B1, bit 5 (ref_mon_tl_sticky_0P::sfm).
4	pfm	See description for register at Address 0x1B1, bit 4 (ref_mon_tl_sticky_0P::pfm).
3	gst	See description for register at Address 0x1B1, bit 3 (ref_mon_tl_sticky_0P::gst).
2	cfm	See description for register at Address 0x1B1, bit 2 (ref_mon_tl_sticky_0P::cfm).
1	scm	See description for register at Address 0x1B1, bit 1 (ref_mon_tl_sticky_0P::scm).
0	los	See description for register at Address 0x1B1, bit 0 (ref_mon_tl_sticky_0P::los).

Address:	0x01BC	
Name:	ref_mon_th_sticky_3P	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:6	reserved	

5	sfm	See description for register at Address 0x1B0, bit 5 (ref_mon_th_sticky_0P::sfm).
4	pfm	See description for register at Address 0x1B0, bit 4 (ref_mon_th_sticky_0P::pfm).
3	gst	See description for register at Address 0x1B0, bit 3 (ref_mon_th_sticky_0P::gst).
2	cfm	See description for register at Address 0x1B0, bit 2 (ref_mon_th_sticky_0P::cfm).
1	scm	See description for register at Address 0x1B0, bit 1 (ref_mon_th_sticky_0P::scm).
0	los	See description for register at Address 0x1B0, bit 0 (ref_mon_th_sticky_0P::los).

Address:	0x01BD	
Name:	ref_mon_tl_sticky_3P	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x1B1, bit 5 (ref_mon_tl_sticky_0P::sfm).
4	pfm	See description for register at Address 0x1B1, bit 4 (ref_mon_tl_sticky_0P::pfm).
3	gst	See description for register at Address 0x1B1, bit 3 (ref_mon_tl_sticky_0P::gst).
2	cfm	See description for register at Address 0x1B1, bit 2 (ref_mon_tl_sticky_0P::cfm).
1	scm	See description for register at Address 0x1B1, bit 1 (ref_mon_tl_sticky_0P::scm).
0	los	See description for register at Address 0x1B1, bit 0 (ref_mon_tl_sticky_0P::los).

Address:	0x01BE	
Name:	ref_mon_th_sticky_3N	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x1B0, bit 5 (ref_mon_th_sticky_0P::sfm).
4	pfm	See description for register at Address 0x1B0, bit 4 (ref_mon_th_sticky_0P::pfm).
3	gst	See description for register at Address 0x1B0, bit 3 (ref_mon_th_sticky_0P::gst).
2	cfm	See description for register at Address 0x1B0, bit 2 (ref_mon_th_sticky_0P::cfm).
1	scm	See description for register at Address 0x1B0, bit 1 (ref_mon_th_sticky_0P::scm).
0	los	See description for register at Address 0x1B0, bit 0 (ref_mon_th_sticky_0P::los).

Address:	0x01BF	
Name:	ref_mon_tl_sticky_3N	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x1B1, bit 5 (ref_mon_tl_sticky_0P::sfm).
4	pfm	See description for register at Address 0x1B1, bit 4 (ref_mon_tl_sticky_0P::pfm).
3	gst	See description for register at Address 0x1B1, bit 3 (ref_mon_tl_sticky_0P::gst).
2	cfm	See description for register at Address 0x1B1, bit 2 (ref_mon_tl_sticky_0P::cfm).
1	scm	See description for register at Address 0x1B1, bit 1 (ref_mon_tl_sticky_0P::scm).
0	los	See description for register at Address 0x1B1, bit 0 (ref_mon_tl_sticky_0P::los).

Address:	0x01C0	
Name:	ref_mon_th_sticky_4P	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x1B0, bit 5 (ref_mon_th_sticky_0P::sfm).
4	pfm	See description for register at Address 0x1B0, bit 4 (ref_mon_th_sticky_0P::pfm).
3	gst	See description for register at Address 0x1B0, bit 3 (ref_mon_th_sticky_0P::gst).
2	cfm	See description for register at Address 0x1B0, bit 2 (ref_mon_th_sticky_0P::cfm).
1	scm	See description for register at Address 0x1B0, bit 1 (ref_mon_th_sticky_0P::scm).
0	los	See description for register at Address 0x1B0, bit 0 (ref_mon_th_sticky_0P::los).

Address:	0x01C1	
Name:	ref_mon_tl_sticky_4P	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x1B1, bit 5 (ref_mon_tl_sticky_0P::sfm).
4	pfm	See description for register at Address 0x1B1, bit 4 (ref_mon_tl_sticky_0P::pfm).
3	gst	See description for register at Address 0x1B1, bit 3 (ref_mon_tl_sticky_0P::gst).
2	cfm	See description for register at Address 0x1B1, bit 2 (ref_mon_tl_sticky_0P::cfm).
1	scm	See description for register at Address 0x1B1, bit 1 (ref_mon_tl_sticky_0P::scm).
0	los	See description for register at Address 0x1B1, bit 0

		(ref_mon_tl_sticky_0P::los).

Address:	0x01C2	
Name:	ref_mon_th_sticky_4N	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x1B0, bit 5 (ref_mon_th_sticky_0P::sfm).
4	pfm	See description for register at Address 0x1B0, bit 4 (ref_mon_th_sticky_0P::pfm).
3	gst	See description for register at Address 0x1B0, bit 3 (ref_mon_th_sticky_0P::gst).
2	cfm	See description for register at Address 0x1B0, bit 2 (ref_mon_th_sticky_0P::cfm).
1	scm	See description for register at Address 0x1B0, bit 1 (ref_mon_th_sticky_0P::scm).
0	los	See description for register at Address 0x1B0, bit 0 (ref_mon_th_sticky_0P::los).

Address:	0x01C3	
Name:	ref_mon_tl_sticky_4N	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	See description for register at Address 0x1B1, bit 5 (ref_mon_tl_sticky_0P::sfm).
4	pfm	See description for register at Address 0x1B1, bit 4 (ref_mon_tl_sticky_0P::pfm).
3	gst	See description for register at Address 0x1B1, bit 3 (ref_mon_tl_sticky_0P::gst).
2	cfm	See description for register at Address 0x1B1, bit 2 (ref_mon_tl_sticky_0P::cfm).
1	scm	See description for register at Address 0x1B1, bit 1 (ref_mon_tl_sticky_0P::scm).
0	los	See description for register at Address 0x1B1, bit 0 (ref_mon_tl_sticky_0P::los).

Address:	0x01D0	
Name:	dpll_mon_th_sticky_0	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7	pslhit	0: DPLL0 phase slope limit failure status has not transitioned 0->1. 1: DPLL0 phase slope limit failure status transitioned 0->1, not yet acknowledged.
6	state_ch	0: DPLL0 state transition has not occurred. 1: DPLL0 state transition has occurred, not yet acknowledged.
5	flhit	0: DPLL0 pull-in/hold-in range limit failure status has not transitioned 0->1. 1: DPLL0 pull-in/hold-in range limit failure status transitioned 0->1, not yet acknowledged.

4:3	reserved	
2	ho_ready	0: DPLL0 holdover ready status has not transitioned 0->1. 1: DPLL0 holdover ready status transitioned 0->1, not yet acknowledged.
1	ho	0: DPLL0 holdover status has not transitioned 0->1. 1: DPLL0 holdover status transitioned 0->1, not yet acknowledged.
0	lock	0: DPLL0 lock status has not transitioned 0->1. 1: DPLL0 lock status transitioned 0->1, not yet acknowledged.

Address:	0x01D1	
Name:	dpll_mon_tl_sticky_0	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7	pslhit	0: DPLL0 phase slope limit failure status has not transitioned 1->0. 1: DPLL0 phase slope limit failure status transitioned 1->0, not yet acknowledged.
6	reserved	
5	flhit	0: DPLL0 pull-in/hold-in range limit failure status has not transitioned 1->0. 1: DPLL0 pull-in/hold-in range limit failure status transitioned 1->0, not yet acknowledged.
4:3	reserved	
2	ho_ready	0: DPLL0 holdover ready status has not transitioned 1->0. 1: DPLL0 holdover ready status transitioned 1->0, not yet acknowledged.
1	ho	0: DPLL0 holdover status has not transitioned 1->0. 1: DPLL0 holdover status transitioned 1->0, not yet acknowledged.
0	lock	0: DPLL0 lock status has not transitioned 1->0. 1: DPLL0 lock status transitioned 1->0, not yet acknowledged.

Address:	0x01D2	
Name:	dpll_mon_th_sticky_1	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7	pslhit	See description for register at Address 0x1D0, bit 7 (dpll_mon_th_sticky_0::pslhit).
6	state_ch	See description for register at Address 0x1D0, bit 6 (dpll_mon_th_sticky_0::state_ch).
5	flhit	See description for register at Address 0x1D0, bit 5 (dpll_mon_th_sticky_0::flhit).
4:3	reserved	
2	ho_ready	See description for register at Address 0x1D0, bit 2 (dpll_mon_th_sticky_0::ho_ready).
1	ho	See description for register at Address 0x1D0, bit 1 (dpll_mon_th_sticky_0::ho).
0	lock	See description for register at Address 0x1D0, bit 0 (dpll_mon_th_sticky_0::lock).

Address:	0x01D3	
Name:	dpll_mon_tl_sticky_1	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7	pslhit	See description for register at Address 0x1D1, bit 7 (dpll_mon_tl_sticky_0::pslhit).
6	reserved	
5	flhit	See description for register at Address 0x1D1, bit 5 (dpll_mon_tl_sticky_0::flhit).
4:3	reserved	
2	ho_ready	See description for register at Address 0x1D1, bit 2 (dpll_mon_tl_sticky_0::ho_ready).
1	ho	See description for register at Address 0x1D1, bit 1 (dpll_mon_tl_sticky_0::ho).
0	lock	See description for register at Address 0x1D1, bit 0 (dpll_mon_tl_sticky_0::lock).

Address:	0x01D4	
Name:	dpll_mon_th_sticky_2	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7	pslhit	See description for register at Address 0x1D0, bit 7 (dpll_mon_th_sticky_0::pslhit).
6	state_ch	See description for register at Address 0x1D0, bit 6 (dpll_mon_th_sticky_0::state_ch).
5	flhit	See description for register at Address 0x1D0, bit 5 (dpll_mon_th_sticky_0::flhit).
4:3	reserved	
2	ho_ready	See description for register at Address 0x1D0, bit 2 (dpll_mon_th_sticky_0::ho_ready).
1	ho	See description for register at Address 0x1D0, bit 1 (dpll_mon_th_sticky_0::ho).
0	lock	See description for register at Address 0x1D0, bit 0 (dpll_mon_th_sticky_0::lock).

Address:	0x01D5	
Name:	dpll_mon_tl_sticky_2	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7	pslhit	See description for register at Address 0x1D1, bit 7 (dpll_mon_tl_sticky_0::pslhit).
6	reserved	
5	flhit	See description for register at Address 0x1D1, bit 5 (dpll_mon_tl_sticky_0::flhit).
4:3	reserved	
2	ho_ready	See description for register at Address 0x1D1, bit 2 (dpll_mon_tl_sticky_0::ho_ready).
1	ho	See description for register at Address 0x1D1, bit 1 (dpll_mon_tl_sticky_0::ho).
0	lock	See description for register at Address 0x1D1, bit 0 (dpll_mon_tl_sticky_0::lock).

Address:	0x01D6	
Name:	dpll_mon_th_sticky_3	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7	pslhit	See description for register at Address 0x1D0, bit 7 (dpll_mon_th_sticky_0::pslhit).
6	state_ch	See description for register at Address 0x1D0, bit 6 (dpll_mon_th_sticky_0::state_ch).
5	flhit	See description for register at Address 0x1D0, bit 5 (dpll_mon_th_sticky_0::flhit).
4:3	reserved	
2	ho_ready	See description for register at Address 0x1D0, bit 2 (dpll_mon_th_sticky_0::ho_ready).
1	ho	See description for register at Address 0x1D0, bit 1 (dpll_mon_th_sticky_0::ho).
0	lock	See description for register at Address 0x1D0, bit 0 (dpll_mon_th_sticky_0::lock).

Address:	0x01D7	
Name:	dpll_mon_tl_sticky_3	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7	pslhit	See description for register at Address 0x1D1, bit 7 (dpll_mon_tl_sticky_0::pslhit).
6	reserved	
5	flhit	See description for register at Address 0x1D1, bit 5 (dpll_mon_tl_sticky_0::flhit).
4:3	reserved	
2	ho_ready	See description for register at Address 0x1D1, bit 2 (dpll_mon_tl_sticky_0::ho_ready).
1	ho	See description for register at Address 0x1D1, bit 1 (dpll_mon_tl_sticky_0::ho).
0	lock	See description for register at Address 0x1D1, bit 0 (dpll_mon_tl_sticky_0::lock).

Address:	0x01D8	
Name:	dpll_mon_th_sticky_4	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7	pslhit	See description for register at address 0x1D0, bit 7 (dpll_mon_th_sticky_0::pslhit).
6	state_ch	See description for register at address 0x1D0, bit 6 (dpll_mon_th_sticky_0::state_ch).
5	flhit	See description for register at address 0x1D0, bit 5 (dpll_mon_th_sticky_0::flhit).
4:3	reserved	
2	ho_ready	See description for register at address 0x1D0, bit 2 (dpll_mon_th_sticky_0::ho_ready).
1	ho	See description for register at address 0x1D0, bit 1 (dpll_mon_th_sticky_0::ho).
0	lock	See description for register at address 0x1D0, bit 0 (dpll_mon_th_sticky_0::lock).

Address:	0x01D9	
Name:	dpll_mon_tl_sticky_4	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7	pslhit	See description for register at address 0x1D1, bit 7 (dpll_mon_tl_sticky_0::pslhit).
6	reserved	
5	flhit	See description for register at address 0x1D1, bit 5 (dpll_mon_tl_sticky_0::flhit).
4:3	reserved	
2	ho_ready	See description for register at address 0x1D1, bit 2 (dpll_mon_tl_sticky_0::ho_ready).
1	ho	See description for register at address 0x1D1, bit 1 (dpll_mon_tl_sticky_0::ho).
0	lock	See description for register at address 0x1D1, bit 0 (dpll_mon_tl_sticky_0::lock).

Address:	0x01DA	
Name:	dpll_mon_th_sticky_5	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7	pslhit	See description for register at address 0x1D0, bit 7 (dpll_mon_th_sticky_0::pslhit).
6	state_ch	See description for register at address 0x1D0, bit 6 (dpll_mon_th_sticky_0::state_ch).
5	flhit	See description for register at address 0x1D0, bit 5 (dpll_mon_th_sticky_0::flhit).
4:3	reserved	
2	ho_ready	See description for register at address 0x1D0, bit 2 (dpll_mon_th_sticky_0::ho_ready).
1	ho	See description for register at address 0x1D0, bit 1 (dpll_mon_th_sticky_0::ho).
0	lock	See description for register at address 0x1D0, bit 0 (dpll_mon_th_sticky_0::lock).

Address:	0x01DB	
Name:	dpll_mon_tl_sticky_5	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7	pslhit	See description for register at address 0x1D1, bit 7 (dpll_mon_tl_sticky_0::pslhit).
6	reserved	
5	flhit	See description for register at address 0x1D1, bit 5 (dpll_mon_tl_sticky_0::flhit).
4:3	reserved	
2	ho_ready	See description for register at address 0x1D1, bit 2 (dpll_mon_tl_sticky_0::ho_ready).
1	ho	See description for register at address 0x1D1, bit 1 (dpll_mon_tl_sticky_0::ho).
0	lock	See description for register at address 0x1D1, bit 0 (dpll_mon_tl_sticky_0::lock).

Address:	0x01E0	
Name:	gp_mon_th_sticky	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:6	reserved	
5	io_align_done_1	See description for io_align_done_0.
4	io_align_done_0	0: GPOUT0 I/O alignment status has not transitioned 0->1. 1: GPOUT0 I/O alignment status transitioned 0->1, not yet acknowledged.
3	reserved	
2	lock	0: GP-Synth0 lock status has not transitioned 0->1. 1: GP-Synth0 lock status transitioned 0->1, not yet acknowledged.
1:0	reserved	

Address:	0x01E1	
Name:	gp_mon_tl_sticky	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:3	reserved	
2	lock	0: GP-Synth0 lock status has not transitioned 1->0. 1: GP-Synth0 lock status transitioned 1->0, not yet acknowledged.
1:0	reserved	

Address:	0x01E2	
Name:	hp_mon_th_sticky_1	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:3	reserved	
2	freq_lo	0: synth1 frequency too low has not transitioned 0->1. 1: synth1 frequency too low has transitioned 0->1, not yet acknowledged.
1	freq_hi	0: synth1 frequency too high has not transitioned 0->1. 1: synth1 frequency too high has transitioned 0->1, not yet acknowledged.
0	lock	0: synth1 lock status has not transitioned 0->1. 1: synth1 lock status has transitioned 0->1, not yet acknowledged.

Address:	0x01E3	
Name:	hp_mon_tl_sticky_1	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:3	reserved	
2	freq_lo	0: synth1 frequency too low has not transitioned 1->0. 1: synth1 frequency too low has transitioned 1->0, not yet acknowledged.
1	freq_hi	0: synth1 frequency too high has not transitioned 1->0. 1: synth1 frequency too high has transitioned 1->0, not yet

		acknowledged.
0	lock	0: synth1 lock status has not transitioned 1->0. 1: synth1 lock status has transitioned 1->0, not yet acknowledged.

Address:	0x01E4	
Name:	hp_mon_th_sticky_2	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:3	reserved	
2	freq_lo	See description for register at Address 0x1E2, bit 2 (hp_mon_th_sticky_1::freq_lo).
1	freq_hi	See description for register at Address 0x1E2, bit 1 (hp_mon_th_sticky_1::freq_hi).
0	lock	See description for register at Address 0x1E2, bit 0 (hp_mon_th_sticky_1::lock).

Address:	0x01E5	
Name:	hp_mon_tl_sticky_2	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:3	reserved	
2	freq_lo	See description for register at Address 0x1E3, bit 2 (hp_mon_tl_sticky_1::freq_lo).
1	freq_hi	See description for register at Address 0x1E3, bit 1 (hp_mon_tl_sticky_1::freq_hi).
0	lock	See description for register at Address 0x1E3, bit 0 (hp_mon_tl_sticky_1::lock).

Address:	0x01E6	
Name:	hp_out_th_sticky_0	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	0: HPOUT0 state has not transitioned 0->1. 1: HPOUT0 state has transitioned 0->1, not yet acknowledged.
0	stopd	0: HPOUT0 stopped status has not transitioned 0->1. 1: HPOUT0 stopped status has transitioned 0->1, not yet acknowledged.

Address:	0x01E7	
Name:	hp_out_tl_sticky_0	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	0: HPOUT0 state has not transitioned 1->0. 1: HPOUT0 state has transitioned 1->0, not yet acknowledged.
0	stopd	0: HPOUT0 stopped status has not transitioned 1->0. 1: HPOUT0 stopped status has transitioned 1->0, not yet acknowledged.

Address:	0x01E8	
Name:	hp_out_th_sticky_1	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x1E6, bit 1 (hp_out_th_sticky_0::lsclk).
0	stopd	See description for register at Address 0x1E6, bit 0 (hp_out_th_sticky_0::stopd).

Address:	0x01E9	
Name:	hp_out_tl_sticky_1	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x1E7, bit 1 (hp_out_tl_sticky_0::lsclk).
0	stopd	See description for register at Address 0x1E7, bit 0 (hp_out_tl_sticky_0::stopd).

Address:	0x01EA	
Name:	hp_out_th_sticky_2	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x1E6, bit 1 (hp_out_th_sticky_0::lsclk).
0	stopd	See description for register at Address 0x1E6, bit 0 (hp_out_th_sticky_0::stopd).

Address:	0x01EB	
Name:	hp_out_tl_sticky_2	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x1E7, bit 1 (hp_out_tl_sticky_0::lsclk).
0	stopd	See description for register at Address 0x1E7, bit 0 (hp_out_tl_sticky_0::stopd).

Address:	0x01EC	
Name:	hp_out_th_sticky_3	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x1E6, bit 1 (hp_out_th_sticky_0::lsclk).
0	stopd	See description for register at Address 0x1E6, bit 0 (hp_out_th_sticky_0::stopd).

Address:	0x01ED	
Name:	hp_out_tl_sticky_3	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x1E7, bit 1 (hp_out_tl_sticky_0::lsclk).
0	stopd	See description for register at Address 0x1E7, bit 0 (hp_out_tl_sticky_0::stopd).

Address:	0x01EE	
Name:	hp_out_th_sticky_4	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x1E6, bit 1 (hp_out_th_sticky_0::lsclk).
0	stopd	See description for register at Address 0x1E6, bit 0 (hp_out_th_sticky_0::stopd).

Address:	0x01EF	
Name:	hp_out_tl_sticky_4	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x1E7, bit 1 (hp_out_tl_sticky_0::lsclk).
0	stopd	See description for register at Address 0x1E7, bit 0 (hp_out_tl_sticky_0::stopd).

Address:	0x01F0	
Name:	hp_out_th_sticky_5	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x1E6, bit 1 (hp_out_th_sticky_0::lsclk).
0	stopd	See description for register at Address 0x1E6, bit 0 (hp_out_th_sticky_0::stopd).

Address:	0x01F1	
Name:	hp_out_tl_sticky_5	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x1E7, bit 1 (hp_out_tl_sticky_0::lsclk).
0	stopd	See description for register at Address 0x1E7, bit 0 (hp_out_tl_sticky_0::stopd).

Address:	0x01F2	
Name:	hp_out_th_sticky_6	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x1E6, bit 1 (hp_out_th_sticky_0::lsclk).
0	stopd	See description for register at Address 0x1E6, bit 0 (hp_out_th_sticky_0::stopd).

Address:	0x01F3	
Name:	hp_out_tl_sticky_6	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x1E7, bit 1 (hp_out_tl_sticky_0::lsclk).
0	stopd	See description for register at Address 0x1E7, bit 0 (hp_out_tl_sticky_0::stopd).

Address:	0x01F4	
Name:	hp_out_th_sticky_7	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x1E6, bit 1 (hp_out_th_sticky_0::lsclk).
0	stopd	See description for register at Address 0x1E6, bit 0 (hp_out_th_sticky_0::stopd).

Address:	0x01F5	
Name:	hp_out_tl_sticky_7	
Default:	0x00	
Type:	S	
Bit Field	Function Name	Description
7:2	reserved	
1	lsclk	See description for register at Address 0x1E7, bit 1 (hp_out_tl_sticky_0::lsclk).
0	stopd	See description for register at Address 0x1E7, bit 0 (hp_out_tl_sticky_0::stopd).

Address:	0x01FE	
Name:	uport	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	lockout	When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing.
6:1	reserved	
0	status	This field indicates if microport attempted access had not been successful. The register content will be 0x00 if the access had been successful.

Address:	0x01FF	
Name:	page_sel	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		Unsigned binary value of these bits represents selected page for SPI/I2C access: 0x00: page 0 (first 128 bytes) 0x01: page 1 (second 128 bytes) 0x02: page 2 (third 128 bytes) 0x03: page 3 (fourth 128 bytes) 0x04: page 4 (fifth 128 bytes) 0x05: page 5 (sixth 128 bytes) 0x06: page 6 (seventh 128 bytes) 0x07: page 7 (eighth 128 bytes) 0x08: page 8 (ninth 128 bytes) 0x09: page 9 (tenth 128 bytes) 0x0A: page 10 (eleventh 128 bytes) 0x0B: page 11 (twelfth 128 bytes) 0x0C: page 12 (thirteenth 128 bytes) 0x0D-0xFF: reserved

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Address:	0x0200	
Name:	ref_los_3_0	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	los_3N	See description for los_0P.
6	los_3P	See description for los_0P.
5	los_2N	See description for los_0P.
4	los_2P	See description for los_0P.
3	los_1N	See description for los_0P.
2	los_1P	See description for los_0P.
1	los_0N	See description for los_0P.
0	los_0P	REF0P external Loss Of Signal (LOS) - indicator to DPLLs that REF0P has failed. Internally in the DPLLs this signal is used for reference monitor indicator, reference switching or holdover entry and for ISR generation.

Address:	0x0201	
Name:	ref_los_4	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:2	reserved	
1	los_4N	See description for register at Address 0x200, bit 0 (ref_los_3_0::los_0P).
0	los_4P	See description for register at Address 0x200, bit 0 (ref_los_3_0::los_0P).

Address:	0x0203	
Name:	ref_sfm_clr_3_0	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	clr_3N	See description for clr_0P.
6	clr_3P	See description for clr_0P.
5	clr_2N	See description for clr_0P.
4	clr_2P	See description for clr_0P.
3	clr_1N	See description for clr_0P.
2	clr_1P	See description for clr_0P.
1	clr_0N	See description for clr_0P.
0	clr_0P	0: Ready for clear SFM operation. 1: Clear the SFM status bit in register at Address 0x108 bit 5 (ref_mon_status_0P::sfm). Note: The host should wait for this bit to read 0 before writing a 1 to it.

Address:	0x0204	
Name:	ref_sfm_clr_4	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:2	reserved	
1	clr_4N	See description for register at Address 0x203, bit 0 (ref_sfm_clr_3_0::clr_0P).
0	clr_4P	See description for register at Address 0x203, bit 0 (ref_sfm_clr_3_0::clr_0P).

Address:	0x0205	
Name:	ref_freq_cmd	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:2	reserved	
1:0	latch	00: Previous reference frequency latch operation complete. 01: Request a reference frequency latch operation. The measured frequency (in integer Hz) for all references will be written to registers 0x280-0x2A7. 10: Request a reference frequency offset latch operation. The measured offset (in units of 2^-32, signed) for all references will be written to register 0x280-0x2A7. 11: Invalid Note: The host should wait for this bitfield to read 00, then write a non-zero value to it to ensure the data is coherent.

Address:	0x0206	
Name:	dpll_freq_cmd	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:1	reserved	
0	latch	0: Previous DPLL frequency command complete. 1: Request a DPLL frequency latch operation. All DPLL df offsets

		will be latched at the same instant and written to registers 0x300-305, 0x320-0x325, etc. (dpll_df_offset_x). The frequency value reported will be the option selected in registers 0x306, 0x326, etc. (dpll_df_ctrl_x::cmd). Note: The host should wait for this bit to read 0, then write 1 to it to ensure the data is coherent.

Address:	0x0208	
Name:	dpll_enable	
Default:	0x03	
Type:	R/W	
Bit Field	Function Name	Description
7:2	reserved	
1:0	num	0: All DPLLs disabled. n: DPLL0 to DPLL(n-1) enabled. If n is greater than the highest numbered DPLL, all DPLLs will be enabled.

Address:	0x020B	
Name:	ext_fb_ctrl	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:1	reserved	
0	en	0: DPLL0-Synth0 external feedback is disabled 1: DPLL0-Synth0 external feedback is enabled Before modifying this bit, Synth0 should be disabled. After modifying this bit, Synth0 can then be re-enabled. See section 6.4.1.2 for external feedback controls for other paths.

Address:	0x020C	
Name:	ext_fb_sel	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	ref	Sets the reference to use as the DPLL0-Synth0 external feedback source. An invalid reference number will disable external feedback. See section 6.4.1.2 for external feedback controls for other paths.
3:0	reserved	

Address:	0x0210	
Name:	dpll_mode_refsel_0	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	ref	Specifies which reference the DPLL0 is forced to select, when the mode bitfield is set to '010' (forced reference lock mode). When this forced reference fails, DPLL0 will go to holdover mode. An invalid reference number will select REF0P. When DPLL0 is not in forced reference lock mode, this bitfield is ignored. 0000: REF0P 0001: REF0N 0010: REF1P

		0011: REF1N 0100: REF2P 0101: REF2N 0110: REF3P 0111: REF3N 1000: REF4P 1001: REF4N 1010: HP-Synth1 output 1011: HP-Synth2 output 1100-1111: Invalid Note that when a synthesizer output is specified output-to-output alignment between this DPLL and the source synthesizer is only achieved for output clocks that are an integer multiple (including 1) of the frequency from the synthesizer, which is synthesizer VCO frequency divided by (hp_fb_msdiv_sel_x * hp_fb_lsdiv_sel_x) where x is the synthesizer number.
3	reserved	
2:0	mode	000: Freerun mode 001: Forced holodover mode 010: Forced reference lock mode 011: Automatic mode 100: NCO mode 101-111: Invalid (automatic mode)

Address:	0x0211	
Name:	dpll_ctrl_0	
Default:	0x02	
Type:	R/W	
Bit Field	Function Name	Description
7:5	reserved	
4	ignore_sync	0: DPLL0 will phase lock to a ref-sync input. 1: DPLL0 will ignore the sync input of a ref sync pair. Note that if ignore_sync is changed from 0 to 1 while the DPLL is tracking an input, the DPLL's phase target continues to be determined by the last observed sync phase to avoid a sudden phase change. To give the DPLL a phase target determined only by the ref signal, set ignore_sync=1 then change DPLL mode to holdover and then back to desired mode.
3	nco_hybrid_en	0: DPLL0 will work in NCO mode if it is set to NCO mode by dpll_mode_refsel_0 (0x210). 1: DPLL0 will work in NCO-hybrid mode if it is set to NCO mode by dpll_mode_refsel_0 (0x210). Under this mode, in addition to the delta frequency offset specifed by dpll_df_offset_0 (register 0x300-0x305), an additional offset provided by a special SyncE DPLL will be applied as well. This SyncE DPLL is DPLL3. It is fully configurable but cannot be used to drive synthesizers by default. If the DPLL is being switched from lock mode to NCO-hybrid mode, this bit must be set to 1 prior to changing the dpll_mode_refsel_0 register.
2	nco_auto_read	0: DPLL0 automatic NCO read is disabled. 1: DPLL0 automatic NCO read is enabled. When switching to forced holdover or NCO modes, an NCO read operation is automatically performed. The device will write DPLL0's frequency offset to register 0x300-0x305 (dpll_df_offset_0).

1	Reserved	
0	tie_clear	0: DPLL0 will not align its output to the reset position. This represents "hitless" reference switching mode. 1: DPLL0 will align its outputs to the reset position (specified by appropriate phase shift selection). This bit should be set when initial output to input alignment is desired after numerous reference rearrangements.

Address:	0x0212	
Name:	dpll_cmd_0	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:1		
0	ref_sync_align	0: DPLL0 ref-sync alignment computation complete. 1: Request a new ref-sync alignment computation for DPLL0. The device clears the bit once the computation is complete. Note that it might still take some time for the alignment to occur, after the computation is complete. Note: To avoid race conditions, the other fields in this register byte should only be written when this bit is clear.

Address:	0x0214	
Name:	dpll_mode_refsel_1	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	ref	See description for register at Address 0x210, bits 7:4 (dpll_mode_refsel_0::ref).
3	reserved	
2:0	mode	See description for register at Address 0x210, bits 2:0 (dpll_mode_refsel_0::mode).

Address:	0x0215	
Name:	dpll_ctrl_1	
Default:	0x02	
Type:	R/W	
Bit Field	Function Name	Description
7:5	reserved	
4	ignore_sync	See description for register at Address 0x211, bit 4 (dpll_ctrl_0::ignore_sync).
3	nco_hybrid_en	See description for register at Address 0x211, bit 3 (dpll_ctrl_0::nco_hybrid_en).
2	nco_auto_read	See description for register at Address 0x211, bit 2 (dpll_ctrl_0::nco_auto_read).
1	reserved	
0	tie_clear	See description for register at Address 0x211, bit 0 (dpll_ctrl_0::tie_clear).

Address:	0x0216	
Name:	dpll_cmd_1	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:1		

0	ref_sync_align	See description for register at Address 0x212, bit 0 (dpll_cmd_0::ref_sync_align).

Address:	0x0218	
Name:	dpll_mode_refsel_2	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	ref	See description for register at Address 0x210, bits 7:4 (dpll_mode_refsel_0::ref).
3	reserved	
2:0	mode	See description for register at Address 0x210, bits 2:0 (dpll_mode_refsel_0::mode).

Address:	0x0219	
Name:	dpll_ctrl_2	
Default:	0x02	
Type:	R/W	
Bit Field	Function Name	Description
7:5	reserved	
4	ignore_sync	See description for register at Address 0x211, bit 4 (dpll_ctrl_0::ignore_sync).
3	nco_hybrid_en	See description for register at Address 0x211, bit 3 (dpll_ctrl_0::nco_hybrid_en).
2	nco_auto_read	See description for register at Address 0x211, bit 2 (dpll_ctrl_0::nco_auto_read).
1	reserved	
0	tie_clear	See description for register at Address 0x211, bit 0 (dpll_ctrl_0::tie_clear).

Address:	0x021A	
Name:	dpll_cmd_2	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:1		
0	ref_sync_align	See description for register at Address 0x212, bit 0 (dpll_cmd_0::ref_sync_align).

Address:	0x021C	
Name:	dpll_mode_refsel_3	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	ref	See description for register at Address 0x210, bits 7:4 (dpll_mode_refsel_0::ref).
3	reserved	
2:0	mode	See description for register at Address 0x210, bits 2:0 (dpll_mode_refsel_0::mode).

Address:	0x021D	
Name:	dpll_ctrl_3	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:5	reserved	
4	ignore_sync	See description for register at Address 0x211, bit 4 (dpll_ctrl_0::ignore_sync). This register field is ignored for DPLL3.
3	reserved	
2	nco_auto_read	See description for register at Address 0x211, bit 2 (dpll_ctrl_0::nco_auto_read).
1	reserved	
0	tie_clear	See description for register at Address 0x211, bit 0 (dpll_ctrl_0::tie_clear).

Address:	0x021E	
Name:	dpll_cmd_3	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:1		
0	ref_sync_align	See description for register at Address 0x212, bit 0 (dpll_cmd_0::ref_sync_align).

Address:	0x0230	
Name:	phase_step_ctrl	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:2	reserved	
1:0	op	This field selects the phase step operation to perform. When the device has latched the data in registers 0x234-0x237 (phase_step_data) and 0x23E (phase_step_max), this field is cleared to 00. To prevent race conditions, the host only writes non-zero values to this field, while the device only writes zero. The host controller should read this field prior to writing, and only write to this field when it contains the value 00. Available operations are: 00: Previous operation complete; new operation can be requested 01: Request a phase step reset 10: Request a phase step read 11: Request a phase step write For reset and write operations, reading 00 in this bitfield does not guarantee that the operation has completed. Sticky registers 0x190-0x191 must be used to determine if these operations have finished. Phase step reset: Clears all previously applied phase steps. For HPOUTs, first do a phase step read and only do the phase step reset if the value read is non-zero. Phase step read:

		Read the current phase step offset for the specified post divider. The post divider to read is selected with registers 0x238 (phase_step_mask_gp) or 0x239 (phase_step_mask_hp), and only one bit should be set. The result is returned in registers 0x234-0x237 (phase_step_data). The returned value will be within +/-1 output clock period (LSDIV period for HPOUTs). The results are valid when this bitfield reads 00. Phase step write: Apply a phase step offset to the specified post dividers. The post dividers to write are selected with registers 0x238 (phase_step_mask_gp) or 0x239 (phase_step_mask_hp), and multiple bits may be set. The desired phase step offset value must be written to registers 0x234-0x237 (phase_step_data) prior to writing this field. Internally, the offset will be modded to +/-1 output clock period (LSDIV period for HPOUTs). Phase step writes are cumulative; subsequent phase steps are added to the previous accumulated phase step offset. For HPOUTs, the phase step will only be applied when the output uses LSDIV >= 2. Also for HPOUTs, do not write a phase step of 0.

Address:	0x0234:0x0237	
Name:	phase_step_data	
Default:	0x00000000	
Type:	R/W	
Bit Field	Function Name	Description
31:0		This register contains the argument or results of a phase step operation. For details, see the phase_step_ctrl register. This register should not be read or written while a phase step operation is in progress. This register must only be read or written when register 0x230, bits 1:0 (phase_step_ctrl::op) is zero. The phase step contained in this register is a 32-bit signed word with the MSB at the lowest Address. The signed representation is in 2's complement form. A positive value will move the output phase earlier in time (more to the left on a scope). A negative value will move the output phase later in time (more to the right on a scope). The units of this register are: - LSB = 1 VCO cycle, for steps performed on GP outputs; OR - LSB = 1 MSDIV cycle for steps performed on HP outputs.

Address:	0x0238	
Name:	phase_step_mask_gp	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:2	reserved	
1	out_1	See description for out_0.
0	out_0	0: Phase step operations will not affect GPOUT0. 1: Phase step operation requested on GPOUT0.

Address:	0x0239	
Name:	phase_step_mask_hp	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	out_7	See description for out_0.
6	out_6	See description for out_0.
5	out_5	See description for out_0.
4	out_4	See description for out_0.
3	out_3	See description for out_0.
2	out_2	See description for out_0.
1	out_1	See description for out_0.
0	out_0	0: Phase step operations will not affect HPOUT0. 1: Phase step operation requested on HPOUT0. At least one HPOUT0P or HPOUT0N must be configured to use LSDIV. Note: Phase step can only be used on HPOUT outputs with output frequency of <=10Hz.

Address:	0x023E	
Name:	phase_step_max	
Default:	0x31	
Type:	R/W	
Bit Field	Function Name	Description
7:0		This register contains a numerical value which specifies the maximum phase step to be applied to an output clock/frame pulse. This value is specified as a percentage of the output clock/frame pulse period. This value must be between 1 and 49.

Address:	0x024C	
Name:	out_squelch_ctrl	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:1	reserved	
0	en	0: Outputs not squelched. 1: Squelch all outputs configured in register 0x24D (gp_squelch_mask) and 0x24E (hp_squelch_mask).

Address:	0x024D	
Name:	gp_squelch_mask	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:2	reserved	
1	out_1	See description for out_0.
0	out_0	0: GPOUT0 will not be squelched. 1: GPOUT0 will be squelched when register 0x24C bit 0 (out_squelch_ctrl::en) is set to 1.

Address:	0x024E	
Name:	hp_squelch_mask	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	out_7	See description for out_0.
6	out_6	See description for out_0.
5	out_5	See description for out_0.
4	out_4	See description for out_0.
3	out_3	See description for out_0.
2	out_2	See description for out_0.
1	out_1	See description for out_0.
0	out_0	0: HPOUT0 will not be squelched. 1: HPOUT0 will be squelched when register 0x24C bit 0 (out_squelch_ctrl::en) is set to 1. This uses the stop clock functionality configured in register 0x50B (hp_out_stop_0). Bits 6:3 (src) in that register must be set to 0001 for squelch to function correctly.

Address:	0x024F	
Name:	pherr_low_freq_ctrl	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	avg_time	A temporal parameter for phase error measurement. If this bitfield is set to 0, it is treated as value 16 in the equation below. Averaging time = 2^(avg_time - 1) / min(input_freq, 40Hz) Where input_freq is the lowest input frequency reference programmed in register 0x258 (pherr_low_freq_refsel). Note: the averaging algorithm has a maximum tolerance for input phase-steps, D(ns) <= 640 * 2^(32-2*avg_time). The averaging algorithm goes unstable for input phase-steps > D. The avg_time field should be set so that D is larger than the maximum expected input phase-step, or the low-frequency phase measurement tool should be disabled-then-reenabled after a large input phase-step.
3:1	reserved	
0	en	0: Disable low-frequency phase error measurement and clear all measurement history. 1: Start the low-frequency phase error measurement and continue updating the measurement. The current measurement can be latched using register 0x25F bit 0 (pherr_read_rqst::rd), and the result will be written to register 0x259-0x25E (pherr_low_freq_data).

Address:	0x0250	
Name:	pherr_meas_ctrl	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	avg_time	A temporal parameter for phase error measurement. If this bitfield is set to 0, it is treated as value 16 in the equation below.

		Averaging time = 2^(avg_time - 1) * 286.72us Note: the averaging algorithm has a maximum tolerance for input phase-steps, D(ns) <= 5 * 2^(32-2*avg_time). The averaging algorithm goes unstable for input phase-steps > D. The avg_time field should be set so that D is larger than the maximum expected input phase-step, or the higher-frequency phase measurement tool should be disabled-then-reenabled after a large input phase-step.
3:1	reserved	
0	en	0: Disable phase error measurement and clear all measurement history. 1: Start the phase error measurement and continue updating the measurement. The current measurement can be latched using register 0x25F bit 0 (pherr_read_rqst::rd), and the result will be written to register 0x252-0x257 (pherr_data).

Address:	0x0251	
Name:	pherr_meas_refsel	
Default:	0x98	
Type:	R/W	
Bit Field	Function Name	Description
7:4	ref_idx_1	Set the second signal phase measurement. See the ref_idx_0 field below for decodes.
3:0	ref_idx_0	Set the first signal for phase measurement. 0000=REF0P 0001=REF0N 0010=REF1P 0011=REF1N 0100=REF2P 0101=REF2N 0110=REF3P 0111=REF3N 1000=REF4P 1001=REF4N 1010=HP-Synth1 1011=HP-Synth2 Note that phase measurement including an HP-Synth source should not be started until at least 5 seconds after the synth is enabled.

Address:	0x0252:0x0257	
Name:	pherr_data	
Default:	0x000000000000	
Type:	R	
Bit Field	Function Name	Description
47:0		Phase error data in units of 0.01ps. This data is updated only upon request. The data in this register is only valid if register 0x250, bit 0 (pherr_read_rqst::rd) has become 0. A positive value means the phase of ref_idx_0 is earlier in time (more to the left on a scope) than ref_idx_1. A negative value means the phase of ref_idx_0 later in time (more to the right on a scope) than ref_idx_1.

Address:	0x0258	
Name:	pherr_low_freq_refsel	
Default:	0x98	
Type:	R/W	
Bit Field	Function Name	Description
7:4	ref_idx_1	Set the second input reference for input-vs-input low-frequency phase error measurement.
3:0	ref_idx_0	Set the first input reference for input-vs-input low-frequency phase error measurement. 0000=REF0P 0001=REF0N 0010=REF1P 0011=REF1N 0100=REF2P 0101=REF2N 0110=REF3P 0111=REF3N 1000=REF4P 1001=REF4N 1010=HP-Synth1 1011=HP-Synth2 Note that phase measurement including an HP-Synth source should not be started until at least 5 seconds after the synth is enabled. The ref_idx_0 field should specify the higher-freqeuncy input.

Address:	0x0259:0x025E	
Name:	pherr_low_freq_data	
Default:	0x000000000000	
Type:	R	
Bit Field	Function Name	Description
47:0		Phase error data in units of 0.01ps. This data is updated only upon request. The data in this register is only valid if register 0x25F, bit 0 (pherr_read_rqst::rd) has become 0. A positive value means the phase of ref_idx_0 is earlier in time (more to the left on a scope) than ref_idx_1. A negative value means the phase of ref_idx_0 later in time (more to the right on a scope) than ref_idx_1.

Address:	0x025F	
Name:	pherr_read_rqst	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:1	reserved	
0	rd	The host sets this bit to 1 to request a read of the current phase error measurement. The device will set this bit to 0 when the data has been successfully latched into the register at Addresses 0x252-0x257 (pherr_data) and 0x261-0x272 (dpll_phase_err_data_x).

Address:	0x0260	
Name:	dpll_phase_err_read_mask	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	reserved	
3	dpll3	See description for dpll0.
2	dpll2	See description for dpll0.
1	dpll1	See description for dpll0.
0	dpll0	When the host initializes a phase error read request through the register pherr_read_rqst (0x025F), this bit determines whether the instantaneous phase error between DPLL0 and its input reference will be latched into dpll_phase_err_data_0 (0x0261-0x0266). If this bit is set, the phase error will be latched.

Address:	0x0261:0x0266	
Name:	dpll_phase_err_data_0	
Default:	0x000000000000	
Type:	R	
Bit Field	Function Name	Description
47:0		This register stores the readback phase error data when the host issues a phase error read request through the register pherr_read_rqst (0x025F). The unit is 0.01ps. The range is +/-0.5 cycle of the input reference. A positive value means the phase of DPLL0 is earlier in time (more to the left on a scope) than its input reference. A negative value means the phase of DPLL0 later in time (more to the right on a scope) than its input reference.

Address:	0x0267:0x026C	
Name:	dpll_phase_err_data_1	
Default:	0x000000000000	
Type:	R	
Bit Field	Function Name	Description
47:0		See description for register at Addresses 0x261-0x266 (dpll_phase_err_data_0).

Address:	0x026D:0x0272	
Name:	dpll_phase_err_data_2	
Default:	0x000000000000	
Type:	R	
Bit Field	Function Name	Description
47:0		See description for register at Addresses 0x261-0x266 (dpll_phase_err_data_0).

Address:	0x0273:0x0278	
Name:	dpll_phase_err_data_3	
Default:	0x000000000000	
Type:	R	
Bit Field	Function Name	Description
47:0		See description for register at Addresses 0x261-0x266 (dpll_phase_err_data_0).

Address:	0x027E	
Name:	uport	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	lockout	When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing.
6:1	reserved	
0	status	This field indicates if microport attempted access had not been successful. The register content will be 0x00 if the access had been successful.

Address:	0x027F	
Name:	page_sel	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		Unsigned binary value of these bits represents selected page for SPI/I2C access: 0x00: page 0 (first 128 bytes) 0x01: page 1 (second 128 bytes) 0x02: page 2 (third 128 bytes) 0x03: page 3 (fourth 128 bytes) 0x04: page 4 (fifth 128 bytes) 0x05: page 5 (sixth 128 bytes) 0x06: page 6 (seventh 128 bytes) 0x07: page 7 (eighth 128 bytes) 0x08: page 8 (ninth 128 bytes) 0x09: page 9 (tenth 128 bytes) 0x0A: page 10 (eleventh 128 bytes) 0x0B: page 11 (twelfth 128 bytes) 0x0C: page 12 (thirteenth 128 bytes) 0x0D-0xFF: reserved

9.3.6 Register List Page 5, Ref Freq

Address:	0x0280:0x0283	
Name:	ref_freq_0P	
Default:	0x00000000	
Type:	R	
Bit Field	Function Name	Description
31:0		See register 0x205 bits 1:0 (ref_freq_cmd::latch) for details on how this register is data-filled. For a reference frequency read, LSB=1Hz (unsigned). For a reference offset read, LSB=2^-32 (signed) and FFO=ref_freq_0P * 1/(2^32). Note that the estimated error for these measurements (difference between reported value and true value) is dependent on input frequency: error[FFO] = ref_freq * 1.5 * (central_freq_offset + 2^32) / (2^56 * 800e6) where central_freq_offset is the value in registers 0x00B-0x00E.

		The estimated error in integer Hz is: error[Hz] = error[FFO] * ref_freq When split-XO behavior is disabled, the measured frequency offset is with respect to the XO wired to the MCLKIN_P and OSCI pins. When split-XO behavior is enabled: (a) for regular inputs the offset is with respect to the selected TCXO/OCXO (b) for TCXO/OCXO inputs the offset is with respect to the XO wired to the MCLKIN_P and OSCI pins.

Address: Name: Default: Type:	0x0284:0x0287 ref_freq_0N 0x00000000 R	
Bit Field	Function Name	Description
31:0		See description for register at Addresses 0x280-0x283 (ref_freq_0P).

Address: Name: Default: Type:	0x0288:0x028B ref_freq_1P 0x00000000 R	
Bit Field	Function Name	Description
31:0		See description for register at Addresses 0x280-0x283 (ref_freq_0P).

Address: Name: Default: Type:	0x028C:0x028F ref_freq_1N 0x00000000 R	
Bit Field	Function Name	Description
31:0		See description for register at Addresses 0x280-0x283 (ref_freq_0P).

Address: Name: Default: Type:	0x0290:0x0293 ref_freq_2P 0x00000000 R	
Bit Field	Function Name	Description
31:0		See description for register at Addresses 0x280-0x283 (ref_freq_0P).

Address: Name: Default: Type:	0x0294:0x0297 ref_freq_2N 0x00000000 R	
Bit Field	Function Name	Description
31:0		See description for register at Addresses 0x280-0x283 (ref_freq_0P).

Address:	0x0298:0x029B	
Name:	ref_freq_3P	
Default:	0x00000000	
Type:	R	
Bit Field	Function Name	Description
31:0		See description for register at Addresses 0x280-0x283 (ref_freq_0P).

Address:	0x029C:0x029F	
Name:	ref_freq_3N	
Default:	0x00000000	
Type:	R	
Bit Field	Function Name	Description
31:0		See description for register at Addresses 0x280-0x283 (ref_freq_0P).

Address:	0x02A0:0x02A3	
Name:	ref_freq_4P	
Default:	0x00000000	
Type:	R	
Bit Field	Function Name	Description
31:0		See description for register at Addresses 0x280-0x283 (ref_freq_0P).

Address:	0x02A4:0x02A7	
Name:	ref_freq_4N	
Default:	0x00000000	
Type:	R	
Bit Field	Function Name	Description
31:0		See description for register at Addresses 0x280-0x283 (ref_freq_0P).

Address:	0x02FE	
Name:	uport	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	lockout	When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing.
6:1	reserved	
0	status	This field indicates if microport attempted access had not been successful. The register content will be 0x00 if the access had been successful.

Address:	0x02FF	
Name:	page_sel	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		Unsigned binary value of these bits represents selected page for SPI/I2C access: 0x00: page 0 (first 128 bytes) 0x01: page 1 (second 128 bytes) 0x02: page 2 (third 128 bytes) 0x03: page 3 (fourth 128 bytes) 0x04: page 4 (fifth 128 bytes)

		0x05: page 5 (sixth 128 bytes) 0x06: page 6 (seventh 128 bytes) 0x07: page 7 (eighth 128 bytes) 0x08: page 8 (ninth 128 bytes) 0x09: page 9 (tenth 128 bytes) 0x0A: page 10 (eleventh 128 bytes) 0x0B: page 11 (twelfth 128 bytes) 0x0C: page 12 (thirteenth 128 bytes) 0x0D-0xFF: reserved

9.3.7 Register List Page 6, DPLL

Address:	0x0300:0x0305	
Name:	dpll_df_offset_0	
Default:	0x000000000000	
Type:	R/W	
Bit Field	Function Name	Description
47:0		When DPLL0 is programmed into NCO mode (dpll_mode_refsel_0 register), this register contains a 2's complement binary value of delta frequency offset. This register controls delta frequency of synthesizers that are associated with DPLL0. Delta frequency is expressed in steps of +/- 2^-48 of nominal setting. The output frequency should be calculated as per formula: f_out = (1 - X/2^48)*f_nom where, X is 2's complement number specified in this register, f_nom is the nominal frequency set by Bs, Ks, Ms, Ns and postdivider number for particular Synthesizer and f_out is the desired output frequency Note 1: The delta frequency offset should not exceed +/-1% of the nominal value (+/-0.4% for DPLL0 when GP-Synth is enabled) Note 2: This register can be written as fast as once per 600us, but no faster. Note 3: This register should not be written while a read operation is pending. Note 4: The read value of this register during NCO mode is the value latched just prior to entering NCO mode.

Address:	0x0306	
Name:	dpll_df_ctrl_0	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:5	reserved	
4	read_sem	Set to 1 to perform a manual df offset read. When the operation has completed, the result is written to registers 0x300-0x305 (dpll_df_offset_0), then the device sets this bit to 0. The host always writes a 1 value, while the device writes 0. To avoid race conditions, the host should check this bit for a 0 value, before writing to it.
3	ref_ofst	0: DPLL0 df offset read will be based on cmd bitfield. 1: DPLL0 df offset read will be the frequency offset of DPLL0 with respect to its input reference (NOT the master clock). The cmd

		bitfield will be ignored for manual reads, but used for automatic NCO reads.
2:0	cmd	Sets the type of delta frequency read operation for manual reads (by setting read_sem to 1) and automatic NCO reads (when dpll_ctrl_0::nco_auto_read is 1). All of the options listed below are the frequency offset of DPLL0 with respect to the master clock. Normal operation: x00: Read the accumulated I-part (iMemory) x01: Read the output of the holdover filter (filtered iMemory) x10: Read the sum of the P and I-parts (delta frequency) x11: Read P-part only Holdover: 0xx: Read the output of the holdover filter (returns I-part when holdover filter is bypassed) 100: Read the accumulated I-part, latched before entering holdover 101: Read the output of the holdover filter (returns 0 when holdover filter is bypassed) 110: Read the sum of the P and I-parts, latched before entering holdover 111: Read P-part only, latched before entering holdover NCO (all reads represent values latched before entering NCO, unless otherwise noted): x00: Read the accumulated I-part x01: Read the output of the holdover filter. If NCO holdover updates are enabled (see mailbox register 0x61C, bit 4), this will be the current output of the holdover filter. 010: Depends on previous state... Normal: Read the sum of the P and I-parts Holdover: Read the output of the holdover filter 110: Read the sum of the P and I-parts x11: Read P-part only

Address:	0x0307:0x030B	
Name:	dpll_df_manual_0	
Default:	0x0000000000	
Type:	R/W	
Bit Field	Function Name	Description
39:0		Manual delta frequency offset adjustment for DPLL0. If the DPLL is in freerun, holdover or NCO mode, this additional frequency offset will be applied to the DPLL output. If the DPLL is lock state, changing this offset may cause the DPLL to lose lock. This signed value is specified in steps of 2^-48. The frequency offset should be calculated as per formula: f_offset = f_nom * (-X) / 2^48 where, X is 2's complement number specified in this register, f_nom is the nominal output frequency and f_offset is the desired frequency offset to the output. Note: this register is used for infrequent corrections of any known frequency error of the master clock oscillator wired to the OSCI

		and MCLKIN_P pins. The dpll_df_offset_0 register should be used for frequent frequency updates in NCO mode.

Address:	0x030C:0x0310	
Name:	dpll_df_temp_0	
Default:	0x0000000000	
Type:	R/W	
Bit Field	Function Name	Description
39:0		Temporary delta frequency offset adjustment for DPLL0. This frequency offset is only applied for the time specified in registers 0x311-0x312 (dpll_df_timer_0). If the DPLL is in freerun, holdover or NCO mode, this additional frequency offset will be applied to the DPLL output. If the DPLL is lock state, changing this offset may cause the DPLL to lose lock. This signed value is specified in steps of 2^-48. The frequency offset should be calculated as per formula: f_offset = f_nom * (-X) / 2^48 where, X is 2's complement number specified in this register, f_nom is the nominal output frequency and f_offset is the desired frequency offset to the output.

Address:	0x0311:0x0312	
Name:	dpll_df_timer_0	
Default:	0x0000	
Type:	R/W	
Bit Field	Function Name	Description
15:0		Timer for DPLL0 temporary delta frequency offset. Writing this register will restart the timer with the programmed value. Writing 0x0000 to this register will immediately stop applying the temporary delta frequency offset. The register at Address 0x12B, bit 0 (dpll_df_timer_status::timer_0) will be set to 1 while the temporary df is being applied. LSB = 286.72us * (2^32 + central_freq_offset) / 2^32

Address:	0x0313:0x0316	
Name:	dpll_tie_data_0	
Default:	0x00000000	
Type:	R/W	
Bit Field	Function Name	Description
31:0		This register contains the argument or results of a DPLL0 time interval error (TIE) control operation. This is a 2's-complement signed integer. The resolution depends on register 0x317 bit 3 (dpll_tie_ctrl_0::resolution). For TIE-read, a positive value means the phase of DPLL0 is earlier in time (more to the left on a scope) than its input reference. A negative value means the phase of DPLL0 later in time (more to the right on a scope) than its input reference. For TIE-write, a positive value will move the phase of DPLL0 is earlier in time (more to the left on a scope) with respect to its input reference. A negative value will move the phase of DPLL0 later in time (more to the right on a scope) with respect to its input reference.

		See register 0x317 (dpll_tie_ctrl_0) for details on TIE control operations. This register should only be read or written when register 0x317 bits 1:0 (dpll_tie_ctrl_0::op) == 00.

Address:	0x0317	
Name:	dpll_tie_ctrl_0	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	reserved	
3	resolution	This field specifies the resolution of register 0x313-0x316 (dpll_tie_data_0) for TIE-write operations. It does NOT apply to TIE-read. 0: Nanoseconds (acceptable range: -2s to 2s) 1: Picoseconds (acceptable range: -2.1ms to 2.1ms)
2	reserved	
1:0	op	This field selects a time interval error (TIE) related operation to perform. When the operation request has been latched by the device, this bitfield reads 00. To prevent race conditions, the host only writes non-zero values to this register, while the device only writes zero. The host controller should read this register prior to writing, and should only write to this bitfield when it contains value 00. All operations provided by this register are only valid when DPLL0 is in forced reference or automatic or mode (see register 0x210) with a valid, qualified reference. If an operation is requested on DPLL0 in another mode of operation (e.g., NCO mode), then the operation will be delayed until DPLL0 is configured to forced reference or automatic mode with a qualified reference. Available operations are: 00: Previous operation complete / new operation can be requested 01: Request a Snap MTIE operation (only available for GPOUTs) 10: Request to read TIE 11: Request to write TIE Snap MTIE: When the input reference is 1Hz, the DPLL0 bandwidth must be <= 30 mHz. With such a low bandwidth and a low edge rate it would take a very long time to do zero phase alignment between the input and output. This operation allows the user to perform an instantaneous I/O alignment. This alignment zeros out hitless reference switch TIE and Write TIE offsets, but excludes post-divider phase steps and fine phase shifts. The instantaneous alignment is completed when this bitfield reads 00. This operation will only affect GPOUTs. TIE-read: Reads the TIE between the input reference and output, not including post-divider phase steps and fine phase shifts. The results are returned in registers 0x313-0x316 (dpll_tie_data_0). The results are valid when this bitfield reads 00. The return value "wraps around" such that the range is -1s to 1s.

		TIE-write: Write the TIE between the input reference and output. The desired TIE value is written to registers 0x313-0x316 (dpll_tie_data_0) prior to writing this bitfield. See resolution bit description for allowed ranges. Another TIE-write request can be made only after this bitfield reads 00. Register 0x18D (dpll_tie_wr_sticky) can be used to determine when the requested TIE has been fully applied to the output. TIE-write operations are cumulative; subsequent writes are added to the previous TIE.

Address: Name: Default: Type:	0x0320:0x0325 dpll_df_offset_1 0x000000000000 R/W	
Bit Field	Function Name	Description
47:0		See description for register at Addresses 0x300-0x305 (dpll_df_offset_0).

Address: Name: Default: Type:	0x0326 dpll_df_ctrl_1 0x00 R/W	
Bit Field	Function Name	Description
7:5	reserved	
4	read_sem	See description for register at Address 0x306, bit 4 (dpll_df_ctrl_0::read_sem).
3	ref_ofst	See description for register at Address 0x306, bit 3 (dpll_df_ctrl_0::ref_ofst).
2:0	cmd	See description for register at Address 0x306, bits 2:0 (dpll_df_ctrl_0::cmd).

Address: Name: Default: Type:	0x0327:0x032B dpll_df_manual_1 0x0000000000 R/W	
Bit Field	Function Name	Description
39:0		See description for register at Addresses 0x307-0x30B (dpll_df_manual_0).

Address: Name: Default: Type:	0x032C:0x0330 dpll_df_temp_1 0x0000000000 R/W	
Bit Field	Function Name	Description
39:0		See description for register at Addresses 0x30C-0x310 (dpll_df_temp_0).

Address: Name: Default: Type:	0x0331:0x0332 dpll_df_timer_1 0x0000 R/W	
Bit Field	Function Name	Description
15:0		See description for register at Addresses 0x311-0x312 (dpll_df_timer_0).

Address:	0x0333:0x0336	
Name:	dpll_tie_data_1	
Default:	0x00000000	
Type:	R/W	
Bit Field	Function Name	Description
31:0		See description for register at Addresses 0x313-0x316 (dpll_tie_data_0).

Address:	0x0337	
Name:	dpll_tie_ctrl_1	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	reserved	
3	resolution	See description for register at Address 0x317, bit 3 (dpll_tie_ctrl_0::resolution).
2	reserved	
1:0	op	See description for register at Address 0x317, bits 1:0 (dpll_tie_ctrl_0::op).

Address:	0x0340:0x0345	
Name:	dpll_df_offset_2	
Default:	0x000000000000	
Type:	R/W	
Bit Field	Function Name	Description
47:0		See description for register at Addresses 0x300-0x305 (dpll_df_offset_0).

Address:	0x0346	
Name:	dpll_df_ctrl_2	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:5	reserved	
4	read_sem	See description for register at Address 0x306, bit 4 (dpll_df_ctrl_0::read_sem).
3	ref_ofst	See description for register at Address 0x306, bit 3 (dpll_df_ctrl_0::ref_ofst).
2:0	cmd	See description for register at Address 0x306, bits 2:0 (dpll_df_ctrl_0::cmd).

Address:	0x0347:0x034B	
Name:	dpll_df_manual_2	
Default:	0x0000000000	
Type:	R/W	
Bit Field	Function Name	Description
39:0		See description for register at Addresses 0x307-0x30B (dpll_df_manual_0).

Address:	0x034C:0x0350	
Name:	dpll_df_temp_2	
Default:	0x0000000000	
Type:	R/W	
Bit Field	Function Name	Description
39:0		See description for register at Addresses 0x30C-0x310

		(dpll_df_temp_0).

Address:	0x0351:0x0352	
Name:	dpll_df_timer_2	
Default:	0x0000	
Type:	R/W	
Bit Field	Function Name	Description
15:0		See description for register at Addresses 0x311-0x312 (dpll_df_timer_0).

Address:	0x0353:0x0356	
Name:	dpll_tie_data_2	
Default:	0x00000000	
Type:	R/W	
Bit Field	Function Name	Description
31:0		See description for register at Addresses 0x313-0x316 (dpll_tie_data_0).

Address:	0x0357	
Name:	dpll_tie_ctrl_2	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	reserved	
3	resolution	See description for register at Address 0x317, bit 3 (dpll_tie_ctrl_0::resolution).
2	reserved	
1:0	op	See description for register at Address 0x317, bits 1:0 (dpll_tie_ctrl_0::op).

Address:	0x0360:0x0365	
Name:	dpll_df_offset_3	
Default:	0x000000000000	
Type:	R/W	
Bit Field	Function Name	Description
47:0		See description for register at Addresses 0x300-0x305 (dpll_df_offset_0).

Address:	0x0366	
Name:	dpll_df_ctrl_3	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:5	reserved	
4	read_sem	See description for register at Address 0x306, bit 4 (dpll_df_ctrl_0::read_sem).
3	ref_ofst	See description for register at Address 0x306, bit 3 (dpll_df_ctrl_0::ref_ofst).
2:0	cmd	See description for register at Address 0x306, bits 2:0 (dpll_df_ctrl_0::cmd).

Address:	0x0368:0x036D	
Name:	dpll_df_offset_4	
Default:	0x000000000000	
Type:	R/W	
Bit Field	Function Name	Description
47:0		See description for register at Addresses 0x300-0x305 (dpll_df_offset_0).

Address:	0x036E	
Name:	dpll_df_ctrl_4	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:5	reserved	
4	read_sem	See description for register at Address 0x306, bit 4 (dpll_df_ctrl_0::read_sem).
3	ref_ofst	See description for register at Address 0x306, bit 3 (dpll_df_ctrl_0::ref_ofst).
2:0	cmd	See description for register at Address 0x306, bits 2:0 (dpll_df_ctrl_0::cmd).

Address:	0x0370:0x0375	
Name:	dpll_df_offset_5	
Default:	0x000000000000	
Type:	R/W	
Bit Field	Function Name	Description
47:0		See description for register at Addresses 0x300-0x305 (dpll_df_offset_0).

Address:	0x0376	
Name:	dpll_df_ctrl_5	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:5	reserved	
4	read_sem	See description for register at Address 0x306, bit 4 (dpll_df_ctrl_0::read_sem).
3	ref_ofst	See description for register at Address 0x306, bit 3 (dpll_df_ctrl_0::ref_ofst).
2:0	cmd	See description for register at Address 0x306, bits 2:0 (dpll_df_ctrl_0::cmd).

Address:	0x037E	
Name:	uport	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	lockout	When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing.
6:1	reserved	
0	status	This field indicates if microport attempted access had not been successful. The register content will be 0x00 if the access had been successful.

Address:	0x037F	
Name:	page_sel	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		Unsigned binary value of these bits represents selected page for SPI/I2C access: 0x00: page 0 (first 128 bytes) 0x01: page 1 (second 128 bytes) 0x02: page 2 (third 128 bytes) 0x03: page 3 (fourth 128 bytes) 0x04: page 4 (fifth 128 bytes) 0x05: page 5 (sixth 128 bytes) 0x06: page 6 (seventh 128 bytes) 0x07: page 7 (eighth 128 bytes) 0x08: page 8 (ninth 128 bytes) 0x09: page 9 (tenth 128 bytes) 0x0A: page 10 (eleventh 128 bytes) 0x0B: page 11 (twelfth 128 bytes) 0x0C: page 12 (thirteenth 128 bytes) 0x0D-0xFF: reserved

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Address:	0x0400	
Name:	gp_ctrl	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:1	reserved	
0	en	0: GP-Synth0 disabled 1: GP-Synth0 enabled

Address:	0x0401	
Name:	gp_cmd	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:1	reserved	
0	fine_shift_en	This bit applies a fine phase shift to the GP synth. The amount of shift is specified by the register at Addresses 0x40D-0x40E (gp_fine_shift). When the operation request has been latched by the device, this bit reads 0. To prevent race conditions, the host writes only non-zero values to this register, while the device only writes zero. The host controller should read this bit prior to writing, and should only write to this bitfield when it contains value 0.

Address:	0x0404:0x0405	
Name:	gp_freq_base	
Default:	0x1F40	
Type:	R/W	
Bit Field	Function Name	Description
15:0		Sets the synthesizer VCO base frequency (Bs), in Hz. The final VCO frequency is given by: fvco = Bs x Ks x Ms / Ns

Address:	0x0406:0x0408	
Name:	gp_freq_mult	
Default:	0x017BB0	
Type:	R/W	
Bit Field	Function Name	Description
23:0		Sets the synthesizer frequency multiplier (Ks). See description for register at Addresses 0x404-0x405 (gp_freq_base) for more information.

Address:	0x0409:0x040A	
Name:	gp_freq_m	
Default:	0x0001	
Type:	R/W	
Bit Field	Function Name	Description
15:0		Sets the Ms component of the VCO frequency. See description for register at Addresses 0x404-0x405 (gp_freq_base) for more information.

Address:	0x040B:0x040C	
Name:	gp_freq_n	
Default:	0x0001	
Type:	R/W	
Bit Field	Function Name	Description
15:0		Sets the Ns component of the VCO frequency. See description for register at Addresses 0x404-0x405 (gp_freq_base) for more information.

Address:	0x040D:0x040E	
Name:	gp_fine_shift	
Default:	0x0000	
Type:	R/W	
Bit Field	Function Name	Description
15:0		Specifies the amount of fine phase shift that will be applied to the GP synth. This number is a 16-bit signed integer with LSB=1ps. See register at Address 0x401, bit 0 (gp_cmd::fine_shift_en) for more details. A positive value will move the phase of GP-Synth0 later in time (more to the right on a scope) with respect to DPLL0. A negative value will move the GP-Synth0 earlier in time (more to the left on a scope) with respect to DPLL0.

Address:	0x040F	
Name:	gp_fine_shift_intvl	
Default:	0x01	
Type:	R/W	
Bit Field	Function Name	Description
7:0		The total amount of time that the fine phase shift operation needs. The unit is 286.72us.

Address:	0x0410:0x0414	
Name:	gp_df_offset_manual	
Default:	0x0000000000	
Type:	R/W	
Bit Field	Function Name	Description
39:0		Manual delta frequency offset adjustment for Synth0. This offset is applied in addition to any offset applied by the DPLL. This register contains a 2's complement binary value in steps of 2^-48. The frequency offset should be calculated as per formula: f_offset = - (X/2^48)*f_nom where, X is 2's complement number specified in this register, f_nom is the nominal frequency set by Bs, Ks, Ms, Ns and postdivider number for Synth0 and f_offset is the desired frequency offset for the output. Note 1: This register can be written as fast as once per 600us, but no faster. Note 2: The offset frequency is based on the master clock. If the master clock experiences frequency drift, the offset frequency will be affected.

Address:	0x0420	
Name:	gp_out_ctrl_0	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:5	reserved	
4	polarity	0: Regular (non-inverse) polarity 1: Inverse polarity
3:0	reserved	

Address:	0x0422:0x0425	
Name:	gp_out_div_0	
Default:	0x00000005	
Type:	R/W	
Bit Field	Function Name	Description
31:0		Sets the GPOUT0 divider value, in units of VCO cycles.

Address:	0x0426:0x0429	
Name:	gp_out_width_0	
Default:	0x00000000	
Type:	R/W	
Bit Field	Function Name	Description
31:0		Sets the width of the GPOUT0 high pulse, in units of Synth0 VCO cycles. A value of 0 will default to 50% duty cycle. Note that duty cycles other than 50% are not available when register at Addresses 0x422-0x425 (gp_out_div_0) is <= 8. Note that for proper phase alignment of GPOUTs with freq < 250Hz, GPOUTs must start with 50% duty cycle. After alignment is complete (signaled by 0x140 (gp_mon_status) bit 4 or bit 5), duty cycle can be changed without affecting phase alignment.

Address:	0x0430	
Name:	gp_out_ctrl_1	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:5	reserved	
4	polarity	See description for register at Address 0x420, bit 4 (gp_out_ctrl_0::polarity).
3:0	reserved	

Address:	0x0432:0x0435	
Name:	gp_out_div_1	
Default:	0x00000028	
Type:	R/W	
Bit Field	Function Name	Description
31:0		See description for register at Addresses 0x422-0x425 (gp_out_div_0).

Address:	0x0436:0x0439	
Name:	gp_out_width_1	
Default:	0x00000000	
Type:	R/W	
Bit Field	Function Name	Description
31:0		See description for register at Addresses 0x426-0x429 (gp_out_width_0).

Address:	0x0450	
Name:	gp_out_en	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:2	reserved	
1	en_1	0: GPOUT1 output disabled 1: GPOUT1 output enabled Note that the enable bits in this register should be set to 1 using separate writes to this register. Setting both to 1 with the same write could result in GPOUT phase misalignment.
0	en_0	0: GPOUT0 output disabled 1: GPOUT0 output enabled

Address:	0x0451	
Name:	gp_out_drive	
Default:	0x0F	
Type:	R/W	
Bit Field	Function Name	Description
7:4	reserved	
3:2	drive_1	GPOUT1 drive strength. See drive_0 description below.
1:0	drive_0	GPOUT0 drive strength. 00: 1x 01: 2x 10: 3x 11: 4x (default)

Address:	0x047E	
Name:	uport	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	lockout	When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing.
6:1	reserved	
0	status	This field indicates if microport attempted access had not been successful. The register content will be 0x00 if the access had been successful.

Address:	0x047F	
Name:	page_sel	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		Unsigned binary value of these bits represents selected page for SPI/I2C access: 0x00: page 0 (first 128 bytes) 0x01: page 1 (second 128 bytes) 0x02: page 2 (third 128 bytes) 0x03: page 3 (fourth 128 bytes) 0x04: page 4 (fifth 128 bytes) 0x05: page 5 (sixth 128 bytes) 0x06: page 6 (seventh 128 bytes) 0x07: page 7 (eighth 128 bytes) 0x08: page 8 (ninth 128 bytes) 0x09: page 9 (tenth 128 bytes) 0x0A: page 10 (eleventh 128 bytes) 0x0B: page 11 (twelfth 128 bytes) 0x0C: page 12 (thirteenth 128 bytes) 0x0D-0xFF: reserved

9.3.9 Register List Page 9, HP

Address:	0x0480	
Name:	hp_ctrl_1	
Default:	0x10	
Type:	R/W	
Bit Field	Function Name	Description
7	fdiv_fb_dbl	0: HP-Synth1 FDIV feedback doubler disabled. 1: HP-Synth1 FDIV feedback doubler enabled (may produce lower jitter output clocks). This bit must only be enabled when the OSCI doubler is disabled. See register 0x02C bit 2 (osci_ctrl::dbl_en) for additional details.
6	ext_fb	0: DPLL1-Synth1 external feedback path disabled. 1: DPLL1-Synth1 external feedback path enabled. An HPOUT sourced from Synth1 must be connected to a REF input. The REF input is specified in register 0x4AD, bits 3:0 (hp_fb_ref_1::idx), and the HPOUT is specified in register 0x4AE, bits 2:0 (hp_fb_out_1::idx). External feedback must be used for HP-Synth1 when FDIV APLL feedback mode is enabled on HP-Synth2.

		After external feedback is enabled, the settings for the specified REF and HPOUT must not be modified. See section 6.4.1.2 for external feedback controls for other paths.
5:4	dpll	Sets the DPLL that drives HP-Synth1. 00: DPLL0 01: DPLL1 All other values are invalid.
3	fdiv_fb_en	0: HP-Synth1 FDIV feedback mode disabled. 1: HP-Synth1 FDIV feedback mode enabled. Enabling this mode can produce lower jitter output clocks. In this mode, the fractional divider is locked to the master clock frequency and must drive HP output bank 01. Therefore, the fractional divider will not be available for use, and registers 0x491-0x49C (hp_fdiv_base_1, hp_fdiv_num_1 and hp_fdiv_den_1) must not be modified. Setting this bit to 1 will update the following register values automatically. These values must not be modified while this bit is set to 1. 0x4E1 bits 1:0 (hp_out_mux::bank01) to 01 (HP-Synth1 fractional divider) 0x500 (hpout_msdiv_0) depending on master clock frequency after the OSCI doubler (23.75-25MHz = 8; 47.5-50MHz = 4; 114.285-125M = 2) The frequency output of the fractional divider will be (master_clock_freq * hpout_msdiv_0). Setting this bit to 0 will not change or revert any register values.
2	reserved	
1	fdiv_en	0: HP-Synth1 fractional output divider disabled 1: HP-Synth1 fractional output divider enabled
0	en	0: HP-Synth1 disabled 1: HP-Synth1 enabled

Address:	0x0481	
Name:	hp_src_1	
Default:	0x03	
Type:	R/W	
Bit Field	Function Name	Description
7:3	reserved	
2:0	src	Sets the HP-Synth1 clock source. 000-010: reserved 011: OSCI 100: OSCI doubled (register 0x02C, bit 2 must be set to 1 to enable the OSCI doubler) 101-111: reserved

Address:	0x0482	
Name:	hp_misc_1	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	dep_dpll_bw	This bit is only considered when HP-Synth1 is driven by DPLL0.

		0: Dependent DPLL1 bandwidth will be 14Hz. 1: Dependent DPLL1 bandwidth will be whatever was previously configured before changing HP-Synth1 to be driven by DPLL0.
6:2	reserved	
1	ext_fb_corr	0: HP-Synth1 external feedback correction disabled. 1: HP-Synth1 external feedback correction enabled. If the external feedback path is very long, the DPLL may align to the wrong edge of the feedback clock. This adds a 1 cycle correction to compensate for the delay in the feedback path.
0	reserved	

Address:	0x0484:0x0487	
Name:	hp_freq_base_1	
Default:	0xDF847580	
Type:	R/W	
Bit Field	Function Name	Description
31:0		Sets the synthesizer VCO base frequency (Bs), in Hz. The final VCO frequency is given by: f_vco = Bs x Ms / Ns The range for f_vco for HP-Synth1 is 3.715GHz to 4.18GHz.

Address:	0x0488:0x048B	
Name:	hp_freq_m_1	
Default:	0x00000001	
Type:	R/W	
Bit Field	Function Name	Description
31:0		Sets the Ms component of the VCO frequency. See description for register at Addresses 0x484-0x487 (hp_freq_base_1) for more information.

Address:	0x048C:0x048F	
Name:	hp_freq_n_1	
Default:	0x00000001	
Type:	R/W	
Bit Field	Function Name	Description
31:0		Sets the Ns component of the VCO frequency. See description for register at Addresses 0x484-0x487 (hp_freq_base_1) for more information.

Address:	0x0490	
Name:	hp_hsdiv_1	
Default:	0x04	
Type:	R/W	
Bit Field	Function Name	Description
7:4	reserved	
3:0	hsdiv	Controls HP-Synth1 high-speed integer divider. 0000: divide by 4 0001: 4.5 0010: 5 0011: 5.5 0100: 6 0101: 6.5 0110: 7 0111: 7.5 1000: 8

		1001: 9 1010: 10 1011: 11 1100: 12 1101: 13 1110: 14 1111: 15

Address:	0x0491:0x0494	
Name:	hp_fdiv_base_1	
Default:	0x0BEBC200	
Type:	R/W	
Bit Field	Function Name	Description
31:0		Sets the HP-Synth1 fractional output divider base frequency (Bs), in Hz. The final fractional divider output frequency is given by: f_FRACDIV = Bs x Ms / Ns The range for f_FRACDIV is f_vco/10 to f_vco/32.

Address:	0x0495:0x0498	
Name:	hp_fdiv_num_1	
Default:	0x00000001	
Type:	R/W	
Bit Field	Function Name	Description
31:0		Sets the Ms component of the fractional output divider frequency. See description for register at Addresses 0x491-0x494 (hp_fdiv_base_1) for more information.

Address:	0x0499:0x049C	
Name:	hp_fdiv_den_1	
Default:	0x00000001	
Type:	R/W	
Bit Field	Function Name	Description
31:0		Sets the Ns component of the fractional output divider frequency. See description for register at Addresses 0x491-0x494 (hp_fdiv_base_1) for more information.

Address:	0x04A4:0x04A7	
Name:	hp_fine_shift_1	
Default:	0x00000000	
Type:	R/W	
Bit Field	Function Name	Description
31:0		Specifies the phase of the HP-Synth1 output clocks. It affects both the integer-divider and fractional-divider outputs of the synthesizer. This number is a 32-bit signed integer with LSB of 1ps. A positive value will move the phase of HP-Synth1 is earlier in time (more to the left on a scope) with respect to its DPLL. A negative value will move the phase of HP-Synth1 later in time (more to the right on a scope) with respect to its DPLL.

Address:	0x04A8	
Name:	hp_fb_msdiv_1	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		Sets the MSDIV value for HP-Synth1 feedback signal. A value of 0x00 will cause the MSDIV value to be auto calculated. This writes the new MSDIV value immediately, so it must only be modified before HP-Synth1 is enabled. A value of 0x01 is an illegal value. When not 0=automatic this field must be >= 0x02.

Address:	0x04A9:0x04AC	
Name:	hp_fb_lsdiv_1	
Default:	0x00000000	
Type:	R/W	
Bit Field	Function Name	Description
31:0		Sets the LSDIV value for HP-Synth1 feedback signal. A value of 0x00000000 will cause the LSDIV value to be auto calculated. This writes the new LSDIV value immediately, so it must only be modified before HP-Synth1 is enabled. . A value of 0x00000001 is an illegal value. When not 0=automatic this field must be between 0x00000002 and 0x02000000.

Address:	0x04AD	
Name:	hp_fb_ref_1	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	reserved	
3:0	idx	Specifies the REF input to use when HP-Synth1 is in external feedback mode. See register 0x480, bit 6 (hp_ctrl_1::ext_fb) for additional details.

Address:	0x04AE	
Name:	hp_fb_out_1	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:3	reserved	
2:0	idx	Specifies the HPOUT to use when HP-Synth1 is in external feedback mode. See register 0x480, bit 6 (hp_ctrl_1::ext_fb) for additional details. Note that only an HPOUT internally connected to the synthesizer's integer divider can be used. Using an HPOUT internally connected to the synthesizer's fractional divider is not supported.

Address:	0x04B0	
Name:	hp_ctrl_2	
Default:	0x20	
Type:	R/W	
Bit Field	Function Name	Description
7	fdiv_fb_dbl	See description for register at Address 0x480, bit 7 (hp_ctrl_1::fdiv_fb_dbl).
6	ext_fb	0: DPLL2-Synth2 external feedback path disabled.

		1: DPLL2-Synth2 external feedback path enabled. An HPOUT sourced from Synth2 must be connect to a REF input. The REF input is specified in register 0x4DD, bits 3:0 (hp_fb_ref_2::idx), and the HPOUT is specified in register 0x4DE, bits 2:0 (hp_fb_out_2::idx). After external feedback is enabled, the settings for this REF and HPOUT must not be modified. See section 6.4.1.2 for external feedback controls for other paths.
5:4	dpll	Sets the DPLL that drives HP-Synth2. 00: DPLL0 01: DPLL1 10: DPLL2 All other values are invalid.
3	fdiv_fb_en	0: HP-Synth2 FDIV feedback mode disabled. 1: HP-Synth2 FDIV feedback mode enabled. Enabling this mode can produce lower-jitter output clocks. In this mode, HP-Synth1 must not be enabled, and the fractional divider is locked to the master clock frequency. Therefore, the fractional divider will not be available for use, and registers 0x4C1-0x4CC (hp_fdiv_base_2, hp_fdiv_num_2 and hp_fdiv_den_2) must not be modified. All output banks can be used by the HP-Synth2 integer divider.
2	reserved	
1	fdiv_en	See description for register at Address 0x480, bit 1 (hp_ctrl_1::fdiv_en).
0	en	See description for register at Address 0x480, bit 0 (hp_ctrl_1::en).

Address:	0x04B1	
Name:	hp_src_2	
Default:	0x03	
Type:	R/W	
Bit Field	Function Name	Description
7:3	reserved	
2:0	src	See description for register at Address 0x481, bits 2:0 (hp_src_1::src).

Address:	0x04B2	
Name:	hp_misc_2	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	dep_dpll_bw	See description for register at address 0x482, bit 7 (hp_misc_1::dep_dpll_bw).
6:2	reserved	
1	ext_fb_corr	See description for register at address 0x482, bit 1 (hp_misc_1::ext_fb_corr).
0	reserved	

Address:	0x04B4:0x04B7	
Name:	hp_freq_base_2	
Default:	0xDF847580	
Type:	R/W	
Bit Field	Function Name	Description
31:0		See description for register at Addresses 0x484-0x487 (hp_freq_base_1).

Address:	0x04B8:0x04BB	
Name:	hp_freq_m_2	
Default:	0x00000001	
Type:	R/W	
Bit Field	Function Name	Description
31:0		See description for register at Addresses 0x488-0x48B (hp_freq_m_1).

Address:	0x04BC:0x04BF	
Name:	hp_freq_n_2	
Default:	0x00000001	
Type:	R/W	
Bit Field	Function Name	Description
31:0		See description for register at Addresses 0x48C-0x48F (hp_freq_n_1).

Address:	0x04C0	
Name:	hp_hsdiv_2	
Default:	0x04	
Type:	R/W	
Bit Field	Function Name	Description
7:4	reserved	
3:0	hsdiv	See description for register at Address 0x490, bits 3:0 (hp_hsdiv_1::hsdiv).

Address:	0x04C1:0x04C4	
Name:	hp_fdiv_base_2	
Default:	0x0BEBC200	
Type:	R/W	
Bit Field	Function Name	Description
31:0		See description for register at Addresses 0x491-0x494 (hp_fdiv_base_1).

Address:	0x04C5:0x04C8	
Name:	hp_fdiv_num_2	
Default:	0x00000001	
Type:	R/W	
Bit Field	Function Name	Description
31:0		See description for register at Addresses 0x495-0x498 (hp_fdiv_num_1).

Address:	0x04C9:0x04CC	
Name:	hp_fdiv_den_2	
Default:	0x00000001	
Type:	R/W	
Bit Field	Function Name	Description
31:0		See description for register at Addresses 0x499-0x49C

		(hp_fdiv_den_1).

Address:	0x04D4:0x04D7	
Name:	hp_fine_shift_2	
Default:	0x00000000	
Type:	R/W	
Bit Field	Function Name	Description
31:0		See description for register at Addresses 0x4A4-0x4A7 (hp_fine_shift_1).

Address:	0x04D8	
Name:	hp_fb_msdiv_2	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		Sets the MSDIV value for HP-Synth2 feedback signal. A value of 0x00 will cause the MSDIV value to be auto calculated. This writes the new MSDIV value immediately, so it must only be modified before HP-Synth2 is enabled.

Address:	0x04D9:0x04DC	
Name:	hp_fb_lsdiv_2	
Default:	0x00000000	
Type:	R/W	
Bit Field	Function Name	Description
31:0		See description for register at Addresses 0x4A9-0x4AC (hp_fb_lsdiv_1).

Address:	0x04DD	
Name:	hp_fb_ref_2	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	reserved	
3:0	idx	Specifies the REF input to use when HP-Synth2 is in external feedback mode. See register 0x4B0, bit 6 (hp_ctrl_2::ext_fb) for additional details.

Address:	0x04DE	
Name:	hp_fb_out_2	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:3	reserved	
2:0	idx	Specifies the HPOUT to use when HP-Synth2 is in external feedback mode. See register 0x4B0, bit 6 (hp_ctrl_2::ext_fb) for additional details.

Address:	0x04E0	
Name:	hp_out_en	
Default:	0xFF	
Type:	R/W	
Bit Field	Function Name	Description
7	en_7	See description for en_0.
6	en_6	See description for en_0.

5	en_5	See description for en_0.
4	en_4	See description for en_0.
3	en_3	See description for en_0.
2	en_2	See description for en_0.
1	en_1	See description for en_0.
0	en_0	Master enable control for HPOUT0. 0: Disabled 1: Enabled

Address:	0x04E1	
Name:	hp_out_mux	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:6	bank_67	Controls how HPOUT6 and HPOUT7 are mapped. See description for bank_01.
5:4	bank_45	Controls how HPOUT4 and HPOUT5 are mapped. See description for bank_01.
3:2	bank_23	Controls how HPOUT2 and HPOUT3 are mapped. See description for bank_01.
1:0	bank_01	Controls how HPOUT0 and HPOUT1 are mapped. 00: HP-Synth1 integer divider 01: HP-Synth1 fractional divider 10: HP-Synth2 integer divider 11: HP-Synth2 fractional divider

Address:	0x04E2	
Name:	hp_stop_ctrl	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	stop_7	See description for stop_0.
6	stop_6	See description for stop_0.
5	stop_5	See description for stop_0.
4	stop_4	See description for stop_0.
3	stop_3	See description for stop_0.
2	stop_2	See description for stop_0.
1	stop_1	See description for stop_0.
0	stop_0	0: HPOUT0 not stopped 1: HPOUT0 stopped

Address:	0x04FE	
Name:	uport	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		

Address:	0x04FF	
Name:	page_sel	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		Unsigned binary value of these bits represents selected page for SPI/I2C access:

		0x00: page 0 (first 128 bytes) 0x01: page 1 (second 128 bytes) 0x02: page 2 (third 128 bytes) 0x03: page 3 (fourth 128 bytes) 0x04: page 4 (fifth 128 bytes) 0x05: page 5 (sixth 128 bytes) 0x06: page 6 (seventh 128 bytes) 0x07: page 7 (eighth 128 bytes) 0x08: page 8 (ninth 128 bytes) 0x09: page 9 (tenth 128 bytes) 0x0A: page 10 (eleventh 128 bytes) 0x0B: page 11 (twelfth 128 bytes) 0x0C: page 12 (thirteenth 128 bytes) 0x0D-0xFF: reserved

9.3.10 Register List Page 10, HP out

Address:	0x0500	
Name:	hp_out_msdiv_0	
Default:	0x04	
Type:	R/W	
Bit Field	Function Name	Description
7:0		HPOUT0 medium-speed divider value. Values 0 and 1 bypass MSDIV circuit and send undivided signal directly to output driver. Max value = 0x80

Address:	0x0501:0x0504	
Name:	hp_out_lsdiv_0	
Default:	0x00000001	
Type:	R/W	
Bit Field	Function Name	Description
31:26	reserved	
25:0	lsdiv	HPOUT0 low-speed divider value. The medium-speed divider value (hp_out_msdiv_0) must be >=2 or the low-speed divider value is ignored. Max value = 0x2000000. Low-speed divider value should be in the range 4M-25M for 1Hz or 0.5Hz outputs that participate in step-time or phase-step.

Address:	0x0505	
Name:	hp_out_ctrl_0	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	reserved	
6	pol	The clock path to the HPOUT0 driver is inverted when this bit set. This does not invert the LSDIV path to the CMOS HPOUT0N pin if that path is enabled.
5:4	drive	00: 1x 01: 2x 10: 3x 11: 4x The HPOUT CMOS/HSTL output drivers have four equal sections that can be enabled or disabled to achieve four different drive strengths from 1x to 4x. When the output power supply VDDO_x_y is 3.3V or 2.5V, the user should start with 1x and only

		increase drive strength if the output is highly loaded and signal transition time is unacceptable. When VDDO_x_y is 1.8V or 1.5V the user should start with 4x and only decrease drive strength if the output signal has unacceptable overshoot.
3:0	format	Controls HPOUT0 driver pair format. 0000: Disabled (high-impedance, low power mode) 0001: LVDS 0010: Differential 0011: HSTL 0100: Two CMOS (HPOUT0P in phase with HPOUT0N) 0101: One CMOS (HPOUT0P enabled, HPOUT0N high impedance) 0110: One CMOS (HPOUT0P high impedance, HPOUT0N enabled) 0111: Two CMOS (HPOUT0N inverted vs. HPOUT0P) 1010: HCSL All other values are reserved.

Address:	0x0506	
Name:	hp_out_diff_0	
Default:	0x05	
Type:	R/W	
Bit Field	Function Name	Description
7:4	vcm	Common-mode voltage for the differential HPOUT0 driver. 0000: 1.23V (default) – typical for LVDS and AC-coupled LVPECL 0011: 1.0V 0100: 1.1V 0101: 1.3V 0110: 1.4V 0111: 1.5V 1000: 1.6V 1001: 1.7V 1010: 1.8V 1011: 1.9V 1100: 2.0V – typical for DC-coupled LVPECL 1101: 2.1V 1111: Use this setting for HCSL signal format All other values are reserved.
3:0	vod	This field specifies the differential output voltage (VOD) for the differential output driver. In the device this field actually controls driver output current. When the specified current is driven into the required external 100Ω termination resistor, the voltage across the termination resistor is the desired VOD. VOD is equivalent to the single-ended voltage swing of the HPOUT0P pin or the HPOUT0N pin. This field is ignored and VOD is set to 400mV when register at Address 0x505, bits 3:0 (hp_out_ctrl_0::format) is set to 0001 (LVDS). 0000: 300mV (3mA driver current) 0001: 400mV – typical for LVDS 0010: 500mV 0011: 600mV 0100: 700mV

		0101: 800mV – default value, typical for LVPECL 0110: 900mV (9mA driver current) 1100: Use this setting for HCSL signal format All other values are reserved.

Address:	0x0507	
Name:	hp_out_reg_0	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	reserved	
3:0	vreg	Power supply regulator voltage for the differential HPOUT0 driver. Set this to at least VCM+VOD/2+0.5V. 0000: 2.2V (default) – typical for LVDS and AC-coupled LVPECL 0010: 2.0V 0011: 2.2V 0100: 2.25V 0101: 2.4V 0111: 2.5V 1000: 2.7V 1001: 2.75V 1010: 2.8V 1011: 2.9V – typical for DC-coupled LVPECL 1100: 3.0V 1111: Use this setting for HCSL signal format All other values are reserved.

Address:	0x0508	
Name:	hp_out_lsctrl_0	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	srlsen	This bit enables the hp_out_mon_status_0::lsclk status bit to follow the output of the HPOUT0 low-speed divider. Generally this is only useful when HPOUT0 is stopped or has very low frequency such as 1Hz.
6	reserved	
5	neglsd	This bit selects the source of the clock on the HPOUT0N pin in CMOS mode. 0: Same as HPOUT0P 1: Output of the HPOUT0 LSDIV divider This bit should only be set to 1 when register at address 0x505, bits 3:0 (hp_out_ctrl_0::format) is set to a CMOS mode, when register at address 0x505, bit 6 (hp_out_ctrl_0::pol) is set to 0, and when 0x0508 bit 4 (hp_out_lsctrl_0::lssel) is set to 0.
4	lssel	HPOUT0 clock source. This bit is only valid when register at Address 0x500 (hp_out_msdiv_0) is > 0x01. 0: HPOUT0 clock is sourced from the MSDIV divider. The LSDIV divider output can be independently selected as the source for the HPOUT0N pin (in CMOS output mode) by setting the neglsd bit to 1. 1: HPOUT0 clock is sourced from the LSDIV divider.
3:0	reserved	

Address:	0x0509	
Name:	hp_out_width_0	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		This field controls the HPOUT0 clock signal duty cycle when MSDIV>1 and LSDIV>2. 0: HPOUT0 duty cycle is 50%. 1-255: HPOUT0 clock signal is a pulse with a width of this number of MSDIV output clock periods. When register at Address 0x505, bit 6 (hp_out_ctrl_0::pol) is 0, the pulse is high and the signal is low the remainder of the cycle. When pol=1, the pulse is low and the signal is high the remainder of the cycle.

Address:	0x050A	
Name:	hp_out_shift_0	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	reserved	
3:0	shift	HPOUT0 phase shift. The adjustment is in units of bank source clock cycles. The bank source clock is specified by hp_out_mux::bank_01. For example, if the bank source is the HP-Synth integer divider and that signal frequency is 625MHz then one APLL output clock cycle is 1.6ns, the smallest phase adjustment is 0.8ns, and the adjustment range is ±5.6ns. Negative values mean earlier in time (leading) and positive values mean later in time (lagging). 0000: 0.0 bank source clock cycles 0001: 0.5 0010: 1.0 0011: 1.5 0100: 2.0 0101: 2.5 0110: 3.0 0111: 3.5 1000: -1.0 1001: -0.5 1010: -2.0 1011: -1.5 1100: -3.0 1101: -2.5 1110: -4.0 1111: -3.5

Address:	0x050B	
Name:	hp_out_stop_0	
Default:	0x0C	
Type:	R/W	
Bit Field	Function Name	Description
7	reserved	
6:3	src	HPOUT0 clock stop source: 0000: Never stop

		0001: Logical OR of register 0x4E2 bit 0 (hp_out_stop::stop_0) and register 0x4E3 bit 0 (hp_out_stopall::stop). 0010-0111: reserved 1000: GPIO5 1001: GPIO6 1010: GPIO7 1011: GPIO8 1100-1111: reserved
2	neglsd	When an output pair is configured for two different frequencies in 2xCMOS mode, this bit specifies the stop behavior for the pair. This field allows the user to trade off stop reaction time vs. possible short pulse on the HPOUT0N pin. 0: Stop when higher-speed HPOUT0P signal has the appropriate edge (see mode bitfield in this register). 1: Stop when lower-speed HPOUT0N signal has the appropriate edge. Setting this bit to 1 guarantees no short high/low time for the HPOUT0P signal and for the HPOUT0N signal, but stopping can take a long time when the HPOUT0N pin is very low frequency, such as 2kHz or even 1Hz. Setting this bit to 0 allows stopping to happen faster because it depends only on the frequency of the HPOUT0P signal, but the HPOUT0N signal may have a short high or low time when it stops. For some applications, such as when HPOUT0N is a 1 pulse per second (PPS) signal, a short high or low time when HPOUT0N stops may not matter because HPOUT0N is essentially a data signal (phase alignment or time alignment signal that is latched by a HPOUT0P signal edge) rather than a true clock signal.
1:0	mode	HPOUT0 start-stop mode. 00: Stop Low (stop after falling edge of output clock, start after rising edge of output clock) 01: Stop High (stop after rising edge of output clock, start after falling edge of output clock) 10: Stop Low then go high-impedance (stop after falling edge, start after rising edge) 11: Stop High then go high-impedance (stop after rising edge, start after falling edge) The following HPOUT0 pin(s) stop high or low as specified above for each output signal format. The output format is set with register at Address 0x505, bits 3:0 (hp_out_ctrl_0::format). Format Pin that Stops As Specified 0001 or 0010 HPOUT0P 0011 HPOUT0P 0100 HPOUT0P and HPOUT0N 0101 HPOUT0N 0110 HPOUT0P 0111 HPOUT0P

Address:	0x0510	
Name:	hp_out_msdiv_1	
Default:	0x04	
Type:	R/W	
Bit Field	Function Name	Description
7:0		See description for register at Address 0x500 (hp_out_msdiv_0).

Address:	0x0511:0x0514	
Name:	hp_out_lsdiv_1	
Default:	0x00000001	
Type:	R/W	
Bit Field	Function Name	Description
31:26	reserved	
25:0	lsdiv	See description for register at Addresses 0x501-0x504, bits 25:0 (hp_out_lsdiv_0::lsdiv).

Address:	0x0515	
Name:	hp_out_ctrl_1	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	reserved	
6	polarity	See description for register at Address 0x505, bits 3:0 (hp_out_ctrl_0::polarity).
5:4	drive	See description for register at Address 0x505, bits 5:4 (hp_out_ctrl_0::drive).
3:0	format	See description for register at Address 0x505, bits 3:0 (hp_out_ctrl_0::format).

Address:	0x0516	
Name:	hp_out_diff_1	
Default:	0x05	
Type:	R/W	
Bit Field	Function Name	Description
7:4	vcm	See description for register at Address 0x506, bits 7:4 (hp_out_diff_0::vcm).
3:0	vod	See description for register at Address 0x506, bits 3:0 (hp_out_diff_0::vod).

Address:	0x0517	
Name:	hp_out_reg_1	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	reserved	
3:0	vreg	See description for register at Address 0x507, bits 3:0 (hp_out_reg_0::vreg).

Address:	0x0518	
Name:	hp_out_lsctrl_1	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	srlsen	See description for register at Address 0x508, bit 7 (hp_out_lsctrl_0::srlsen).

6	reserved	
5	neglsd	See description for register at Address 0x508, bit 5 (hp_out_lsctrl_0::neglsd).
4	lssel	See description for register at Address 0x508, bit 4 (hp_out_lsctrl_0::lssel).
3:0	reserved	

Address:	0x0519	
Name:	hp_out_width_1	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		See description for register at Address 0x509 (hp_out_width_0).

Address:	0x051A	
Name:	hp_out_shift_1	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	reserved	
3:0	shift	See description for register at Address 0x50A, bits 3:0 (hp_out_shift_0::shift).

Address:	0x051B	
Name:	hp_out_stop_1	
Default:	0x0C	
Type:	R/W	
Bit Field	Function Name	Description
7	reserved	
6:3	src	See description for register at Address 0x50B, bits 6:3 (hp_out_stop_0::src).
2	neglsd	See description for register at Address 0x50B, bit 2 (hp_out_stop_0::neglsd).
1:0	mode	See description for register at Address 0x50B, bits 1:0 (hp_out_stop_0::mode).

Address:	0x0520	
Name:	hp_out_msdiv_2	
Default:	0x04	
Type:	R/W	
Bit Field	Function Name	Description
7:0		See description for register at Address 0x500 (hp_out_msdiv_0).

Address:	0x0521:0x0524	
Name:	hp_out_lsdiv_2	
Default:	0x00000001	
Type:	R/W	
Bit Field	Function Name	Description
31:26	reserved	
25:0	lsdiv	See description for register at Addresses 0x501-0x504, bits 25:0 (hp_out_lsdiv_0::lsdiv).

Address:	0x0525	
Name:	hp_out_ctrl_2	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	reserved	
6	polarity	See description for register at Address 0x505, bits 3:0 (hp_out_ctrl_0::polarity).
5:4	drive	See description for register at Address 0x505, bits 5:4 (hp_out_ctrl_0::drive).
3:0	format	See description for register at Address 0x505, bits 3:0 (hp_out_ctrl_0::format).

Address:	0x0526	
Name:	hp_out_diff_2	
Default:	0x05	
Type:	R/W	
Bit Field	Function Name	Description
7:4	vcm	See description for register at Address 0x506, bits 7:4 (hp_out_diff_0::vcm).
3:0	vod	See description for register at Address 0x506, bits 3:0 (hp_out_diff_0::vod).

Address:	0x0527	
Name:	hp_out_reg_2	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	reserved	
3:0	vreg	See description for register at Address 0x507, bits 3:0 (hp_out_reg_0::vreg).

Address:	0x0528	
Name:	hp_out_lsctrl_2	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	srlsen	See description for register at Address 0x508, bit 7 (hp_out_lsctrl_0::srlsen).
6	reserved	
5	neglsd	See description for register at Address 0x508, bit 5 (hp_out_lsctrl_0::neglsd).
4	lssel	See description for register at Address 0x508, bit 4 (hp_out_lsctrl_0::lssel).
3:0	reserved	

Address:	0x0529	
Name:	hp_out_width_2	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		See description for register at Address 0x509 (hp_out_width_0).

Address:	0x052A	
Name:	hp_out_shift_2	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	reserved	
3:0	shift	See description for register at Address 0x50A, bits 3:0 (hp_out_shift_0::shift).

Address:	0x052B	
Name:	hp_out_stop_2	
Default:	0x0C	
Type:	R/W	
Bit Field	Function Name	Description
7	reserved	
6:3	src	See description for register at Address 0x50B, bits 6:3 (hp_out_stop_0::src).
2	neglsd	See description for register at Address 0x50B, bit 2 (hp_out_stop_0::neglsd).
1:0	mode	See description for register at Address 0x50B, bits 1:0 (hp_out_stop_0::mode).

Address:	0x0530	
Name:	hp_out_msdiv_3	
Default:	0x04	
Type:	R/W	
Bit Field	Function Name	Description
7:0		See description for register at Address 0x500 (hp_out_msdiv_0).

Address:	0x0531:0x0534	
Name:	hp_out_lsdiv_3	
Default:	0x00000001	
Type:	R/W	
Bit Field	Function Name	Description
31:26	reserved	
25:0	lsdiv	See description for register at Addresses 0x501-0x504, bits 25:0 (hp_out_lsdiv_0::lsdiv).

Address:	0x0535	
Name:	hp_out_ctrl_3	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	reserved	
6	polarity	See description for register at Address 0x505, bits 3:0 (hp_out_ctrl_0::polarity).
5:4	drive	See description for register at Address 0x505, bits 5:4 (hp_out_ctrl_0::drive).
3:0	format	See description for register at Address 0x505, bits 3:0 (hp_out_ctrl_0::format).

Address:	0x0536	
Name:	hp_out_diff_3	
Default:	0x05	
Type:	R/W	
Bit Field	Function Name	Description
7:4	vcm	See description for register at Address 0x506, bits 7:4 (hp_out_diff_0::vcm).
3:0	vod	See description for register at Address 0x506, bits 3:0 (hp_out_diff_0::vod).

Address:	0x0537	
Name:	hp_out_reg_3	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	reserved	
3:0	vreg	See description for register at Address 0x507, bits 3:0 (hp_out_reg_0::vreg).

Address:	0x0538	
Name:	hp_out_lsctrl_3	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	srlsen	See description for register at Address 0x508, bit 7 (hp_out_lsctrl_0::srlsen).
6	reserved	
5	neglsd	See description for register at Address 0x508, bit 5 (hp_out_lsctrl_0::neglsd).
4	lssel	See description for register at Address 0x508, bit 4 (hp_out_lsctrl_0::lssel).
3:0	reserved	

Address:	0x0539	
Name:	hp_out_width_3	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		See description for register at Address 0x509 (hp_out_width_0).

Address:	0x053A	
Name:	hp_out_shift_3	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	reserved	
3:0	shift	See description for register at Address 0x50A, bits 3:0 (hp_out_shift_0::shift).

Address:	0x053B	
Name:	hp_out_stop_3	
Default:	0x0C	
Type:	R/W	
Bit Field	Function Name	Description
7	reserved	

6:3	src	See description for register at Address 0x50B, bits 6:3 (hp_out_stop_0::src).
2	neglsd	See description for register at Address 0x50B, bit 2 (hp_out_stop_0::neglsd).
1:0	mode	See description for register at Address 0x50B, bits 1:0 (hp_out_stop_0::mode).

Address:	0x0540	
Name:	hp_out_msdiv_4	
Default:	0x04	
Type:	R/W	
Bit Field	Function Name	Description
7:0		See description for register at Address 0x500 (hp_out_msdiv_0).

Address:	0x0541:0x0544	
Name:	hp_out_lsdiv_4	
Default:	0x00000001	
Type:	R/W	
Bit Field	Function Name	Description
31:26	reserved	
25:0	lsdiv	See description for register at Addresses 0x501-0x504, bits 25:0 (hp_out_lsdiv_0::lsdiv).

Address:	0x0545	
Name:	hp_out_ctrl_4	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	reserved	
6	polarity	See description for register at Address 0x505, bits 3:0 (hp_out_ctrl_0::polarity).
5:4	drive	See description for register at Address 0x505, bits 5:4 (hp_out_ctrl_0::drive).
3:0	format	See description for register at Address 0x505, bits 3:0 (hp_out_ctrl_0::format).

Address:	0x0546	
Name:	hp_out_diff_4	
Default:	0x05	
Type:	R/W	
Bit Field	Function Name	Description
7:4	vcm	See description for register at Address 0x506, bits 7:4 (hp_out_diff_0::vcm).
3:0	vod	See description for register at Address 0x506, bits 3:0 (hp_out_diff_0::vod).

Address:	0x0547	
Name:	hp_out_reg_4	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	reserved	
3:0	vreg	See description for register at Address 0x507, bits 3:0 (hp_out_reg_0::vreg).

Address:	0x0548	
Name:	hp_out_lsctrl_4	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	srlsen	See description for register at Address 0x508, bit 7 (hp_out_lsctrl_0::srlsen).
6	reserved	
5	neglsd	See description for register at Address 0x508, bit 5 (hp_out_lsctrl_0::neglsd).
4	lssel	See description for register at Address 0x508, bit 4 (hp_out_lsctrl_0::lssel).
3:0	reserved	

Address:	0x0549	
Name:	hp_out_width_4	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		See description for register at Address 0x509 (hp_out_width_0).

Address:	0x054A	
Name:	hp_out_shift_4	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	reserved	
3:0	shift	See description for register at Address 0x50A, bits 3:0 (hp_out_shift_0::shift).

Address:	0x054B	
Name:	hp_out_stop_4	
Default:	0x0C	
Type:	R/W	
Bit Field	Function Name	Description
7	reserved	
6:3	src	See description for register at Address 0x50B, bits 6:3 (hp_out_stop_0::src).
2	neglsd	See description for register at Address 0x50B, bit 2 (hp_out_stop_0::neglsd).
1:0	mode	See description for register at Address 0x50B, bits 1:0 (hp_out_stop_0::mode).

Address:	0x0550	
Name:	hp_out_msdiv_5	
Default:	0x04	
Type:	R/W	
Bit Field	Function Name	Description
7:0		See description for register at Address 0x500 (hp_out_msdiv_0).

Address:	0x0551:0x0554	
Name:	hp_out_lsdiv_5	
Default:	0x00000001	
Type:	R/W	
Bit Field	Function Name	Description
31:26	reserved	
25:0	lsdiv	See description for register at Addresses 0x501-0x504, bits 25:0 (hp_out_lsdiv_0::lsdiv).

Address:	0x0555	
Name:	hp_out_ctrl_5	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	reserved	
6	polarity	See description for register at Address 0x505, bits 3:0 (hp_out_ctrl_0::polarity).
5:4	drive	See description for register at Address 0x505, bits 5:4 (hp_out_ctrl_0::drive).
3:0	format	See description for register at Address 0x505, bits 3:0 (hp_out_ctrl_0::format).

Address:	0x0556	
Name:	hp_out_diff_5	
Default:	0x05	
Type:	R/W	
Bit Field	Function Name	Description
7:4	vcm	See description for register at Address 0x506, bits 7:4 (hp_out_diff_0::vcm).
3:0	vod	See description for register at Address 0x506, bits 3:0 (hp_out_diff_0::vod).

Address:	0x0557	
Name:	hp_out_reg_5	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	reserved	
3:0	vreg	See description for register at Address 0x507, bits 3:0 (hp_out_reg_0::vreg).

Address:	0x0558	
Name:	hp_out_lsctrl_5	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	srlsen	See description for register at Address 0x508, bit 7 (hp_out_lsctrl_0::srlsen).
6	reserved	
5	neglsd	See description for register at Address 0x508, bit 5 (hp_out_lsctrl_0::neglsd).
4	lssel	See description for register at Address 0x508, bit 4 (hp_out_lsctrl_0::lssel).
3:0	reserved	

Address:	0x0559	
Name:	hp_out_width_5	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		See description for register at Address 0x509 (hp_out_width_0).

Address:	0x055A	
Name:	hp_out_shift_5	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	reserved	
3:0	shift	See description for register at Address 0x50A, bits 3:0 (hp_out_shift_0::shift).

Address:	0x055B	
Name:	hp_out_stop_5	
Default:	0x0C	
Type:	R/W	
Bit Field	Function Name	Description
7	reserved	
6:3	src	See description for register at Address 0x50B, bits 6:3 (hp_out_stop_0::src).
2	neglsd	See description for register at Address 0x50B, bit 2 (hp_out_stop_0::neglsd).
1:0	mode	See description for register at Address 0x50B, bits 1:0 (hp_out_stop_0::mode).

Address:	0x0560	
Name:	hp_out_msdiv_6	
Default:	0x04	
Type:	R/W	
Bit Field	Function Name	Description
7:0		See description for register at Address 0x500 (hp_out_msdiv_0).

Address:	0x0561:0x0564	
Name:	hp_out_lsdiv_6	
Default:	0x00000001	
Type:	R/W	
Bit Field	Function Name	Description
31:26	reserved	
25:0	lsdiv	See description for register at Addresses 0x501-0x504, bits 25:0 (hp_out_lsdiv_0::lsdiv).

Address:	0x0565	
Name:	hp_out_ctrl_6	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	reserved	
6	polarity	See description for register at Address 0x505, bits 3:0 (hp_out_ctrl_0::polarity).
5:4	drive	See description for register at Address 0x505, bits 5:4 (hp_out_ctrl_0::drive).

3:0	format	See description for register at Address 0x505, bits 3:0 (hp_out_ctrl_0::format).

Address:	0x0566	
Name:	hp_out_diff_6	
Default:	0x05	
Type:	R/W	
Bit Field	Function Name	Description
7:4	vcm	See description for register at Address 0x506, bits 7:4 (hp_out_diff_0::vcm).
3:0	vod	See description for register at Address 0x506, bits 3:0 (hp_out_diff_0::vod).

Address:	0x0567	
Name:	hp_out_reg_6	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	reserved	
3:0	vreg	See description for register at Address 0x507, bits 3:0 (hp_out_reg_0::vreg).

Address:	0x0568	
Name:	hp_out_lsctrl_6	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	srlsen	See description for register at Address 0x508, bit 7 (hp_out_lsctrl_0::srlsen).
6	reserved	
5	neglsd	See description for register at Address 0x508, bit 5 (hp_out_lsctrl_0::neglsd).
4	lssel	See description for register at Address 0x508, bit 4 (hp_out_lsctrl_0::lssel).
3:0	reserved	

Address:	0x0569	
Name:	hp_out_width_6	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		See description for register at Address 0x509 (hp_out_width_0).

Address:	0x056A	
Name:	hp_out_shift_6	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	reserved	
3:0	shift	See description for register at Address 0x50A, bits 3:0 (hp_out_shift_0::shift).

Address:	0x056B	
Name:	hp_out_stop_6	
Default:	0x0C	
Type:	R/W	
Bit Field	Function Name	Description
7	reserved	
6:3	src	See description for register at Address 0x50B, bits 6:3 (hp_out_stop_0::src).
2	neglsd	See description for register at Address 0x50B, bit 2 (hp_out_stop_0::neglsd).
1:0	mode	See description for register at Address 0x50B, bits 1:0 (hp_out_stop_0::mode).

Address:	0x0570	
Name:	hp_out_msdiv_7	
Default:	0x04	
Type:	R/W	
Bit Field	Function Name	Description
7:0		See description for register at Address 0x500 (hp_out_msdiv_0).

Address:	0x0571:0x0574	
Name:	hp_out_lsdiv_7	
Default:	0x00000001	
Type:	R/W	
Bit Field	Function Name	Description
31:26	reserved	
25:0	lsdiv	See description for register at Addresses 0x501-0x504, bits 25:0 (hp_out_lsdiv_0::lsdiv).

Address:	0x0575	
Name:	hp_out_ctrl_7	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	reserved	
6	polarity	See description for register at Address 0x505, bits 3:0 (hp_out_ctrl_0::polarity).
5:4	drive	See description for register at Address 0x505, bits 5:4 (hp_out_ctrl_0::drive).
3:0	format	See description for register at Address 0x505, bits 3:0 (hp_out_ctrl_0::format).

Address:	0x0576	
Name:	hp_out_diff_7	
Default:	0x05	
Type:	R/W	
Bit Field	Function Name	Description
7:4	vcm	See description for register at Address 0x506, bits 7:4 (hp_out_diff_0::vcm).
3:0	vod	See description for register at Address 0x506, bits 3:0 (hp_out_diff_0::vod).

Address:	0x0577	
Name:	hp_out_reg_7	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	reserved	
3:0	vreg	See description for register at Address 0x507, bits 3:0 (hp_out_reg_0::vreg).

Address:	0x0578	
Name:	hp_out_lsctrl_7	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	srlsen	See description for register at Address 0x508, bit 7 (hp_out_lsctrl_0::srlsen).
6	reserved	
5	neglsd	See description for register at Address 0x508, bit 5 (hp_out_lsctrl_0::neglsd).
4	lssel	See description for register at Address 0x508, bit 4 (hp_out_lsctrl_0::lssel).
3:0	reserved	

Address:	0x0579	
Name:	hp_out_width_7	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		See description for register at Address 0x509 (hp_out_width_0).

Address:	0x057A	
Name:	hp_out_shift_7	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	reserved	
3:0	shift	See description for register at Address 0x50A, bits 3:0 (hp_out_shift_0::shift).

Address:	0x057B	
Name:	hp_out_stop_7	
Default:	0x0C	
Type:	R/W	
Bit Field	Function Name	Description
7	reserved	
6:3	src	See description for register at Address 0x50B, bits 6:3 (hp_out_stop_0::src).
2	neglsd	See description for register at Address 0x50B, bit 2 (hp_out_stop_0::neglsd).
1:0	mode	See description for register at Address 0x50B, bits 1:0 (hp_out_stop_0::mode).

Address:	0x057E	
Name:	uport	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	lockout	When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing.
6:1	reserved	
0	status	This field indicates if microport attempted access had not been successful. The register content will be 0x00 if the access had been successful.

Address:	0x057F	
Name:	page_sel	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		Unsigned binary value of these bits represents selected page for SPI/I2C access: 0x00: page 0 (first 128 bytes) 0x01: page 1 (second 128 bytes) 0x02: page 2 (third 128 bytes) 0x03: page 3 (fourth 128 bytes) 0x04: page 4 (fifth 128 bytes) 0x05: page 5 (sixth 128 bytes) 0x06: page 6 (seventh 128 bytes) 0x07: page 7 (eighth 128 bytes) 0x08: page 8 (ninth 128 bytes) 0x09: page 9 (tenth 128 bytes) 0x0A: page 10 (eleventh 128 bytes) 0x0B: page 11 (twelfth 128 bytes) 0x0C: page 12 (thirteenth 128 bytes) 0x0D-0xFF: reserved

9.3.11 Register List Page 11, Ref MB

Address:	0x0582:0x0583	
Name:	ref_mb_mask	
Default:	0x0001	
Type:	R/W	
Bit Field	Function Name	Description
15:10	reserved	
9:0	mask	For a write operation (see ref_mb_sem::wr bit), this field determines which input reference's configuration is modified. Multiple bits can be set to affect multiple references in a single operation. For a read operation (see ref_mb_sem::rd bit), this field determines which input reference configuration to read back from the device. One (and only one) bit should be set for a read operation.

Address:	0x0584	
Name:	ref_mb_sem	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:2	reserved	
1	rd	When this bit is written to a one by the host controller, the device will perform a read of the masked reference (see ref_mb_mask register). Only one mask bit should be set in this case. When this register reads back 0x00, then the read has completed, and the host can read back any or all of the registers on this page to determine the corresponding Input Referecence configuration.
0	wr	When this bit is written to a one by the host controller (and the read bit is zero), the device will perform a write of the masked references (see ref_mb_mask register). All of the configuration options on this page will be applied to each of the references indicated by the ref_mb_mask mask. The write is complete when this register reads back a zero.

Address:	0x0585:0x0586	
Name:	ref_freq_base	
Default:	0x1F40	
Type:	R/W	
Bit Field	Function Name	Description
15:0		Sets the input reference base frequency (Br), in Hz. The final expected input reference is given by: f_hz = Br * Kr * Mr / Nr Valid values for this registers must satisfy the rule 500MHz divided by value is an integer. Some example frequency configurations are show below: Reference Freq — ref_freq_base(Br) — ref_freq_mult(Kr) 8 kHz — 8kHz (0x07D0) — 1 (0x0001) 19.44 MHz — 8kHz(0x1F40) — 2430 (0x097E) 25 MHz — 25kHz(0x61A8) — 1000 (0x03E8)

Address:	0x0587:0x0588	
Name:	ref_freq_mult	
Default:	0x0001	
Type:	R/W	
Bit Field	Function Name	Description
15:0		Sets the input reference frequency multiple (Kr).

Address:	0x0589:0x058A	
Name:	ref_ratio_m	
Default:	0x0001	
Type:	R/W	
Bit Field	Function Name	Description
15:0		Sets the FEC ratio numerator (Mr).

Address:	0x058B:0x058C	
Name:	ref_ratio_n	
Default:	0x0001	
Type:	R/W	
Bit Field	Function Name	Description
15:0		Sets the FEC ratio denominator (Nr).

Address:	0x058D	
Name:	ref_config	
Default:	0x01	
Type:	R/W	
Bit Field	Function Name	Description
7:5	reserved	
4	pre_divide	When this bit is set, the associated reference input clock will be divided by 2 prior being processed by the DPLLs. All register programming that requires information about this reference's frequency should be done with half of the actual input frequency. When cleared, the associated reference input will not be divided prior to being processed by the DPLLs.
3	reserved	
2	diff_en	When this bit is set, the device expects a differential signal on the associated reference pins (REFxP and REFxN). When cleared, the device expects a single-ended signal on the associated REFxP and REFxN pins. This bit is ignored for REFxN mailboxes.
1	lvpecl_en	When this bit is set, the device expects a single-ended LVPECL signal on the associated REF pin. This bit is ignored if the reference is part of a differential pair (e.g., if the diff_en bit is set for REFxP, this bit is ignored on REFxP and REFxN).
0	enable	When this bit is set, the phase acquisition module of the associated reference will be enabled. When cleared, the associated phase acquisition module is disabled (powered down).

Address:	0x0590	
Name:	ref_scm	
Default:	0x05	
Type:	R/W	
Bit Field	Function Name	Description
7:5	reserved	
4	fine_en	SCM limits are configured with register at Addresses 0x5A8-0x5AB (ref_scm_fine) rather than the ref_scm::limit bitfield below. This feature should be enabled when the application requires a very small phase jump (<=100ns) to be detected on a low frequency clock.
3	reserved	
2:0	limit	Sets the Single Cycle Monitor (SCM) limit selection. When the reference fails the specified criteria, the scm bit in the associated ref_mon_status_n register will be high. Selection: 000: +/- 0.1% (input frequency units) 001: +/- 0.5% 010: +/- 1% 011: +/- 2% 100: +/- 5%

		101: +/- 10% 110: +/- 20% 111: +/- 50% Note that reference clock is sampled at 800MHz, so the measurement granularity is 1.25 ns. This imposes limitation to SCM limits that can be programmed depending on the input clock frequency: +/- 0.1% : can be programmed for frequencies below 800 kHz +/- 0.5% : below 4 MHz +/- 1% : below 8 MHz +/- 2% : below 16 MHz +/- 5% : below 40 MHz +/- 10% : below 80 MHz +/- 20% : below 160 MHz +/- 50% : below 400 MHz SCM indicator should not be used (should be masked) for reference frequencies above 400MHz or a 0.5Hz reference.

Address:	0x0591	
Name:	ref_cfm	
Default:	0x05	
Type:	R/W	
Bit Field	Function Name	Description
7:3	reserved	
2:0	limit	Sets the Coarse Frequency Monitor (CFM) limit selection. When the reference fails the specified criteria, the cfm bit in the associated ref_mon_status_n register will be high. Selection: 000: +/- 0.1% (input frequency units) 001: +/- 0.5% 010: +/- 1% 011: +/- 2% 100: +/- 5% 101: +/- 10% 110: +/- 20% 111: +/- 50%

Address:	0x0592:0x0593	
Name:	ref_gst_disqual	
Default:	0x0005	
Type:	R/W	
Bit Field	Function Name	Description
15:0		Sets the time to disqualify the reference after detecting either a CFM or SCM failure. If the Guard Soak Timer (GST) disqualify time expires and the source of the failure is still present, the gst bit in the associated ref_mon_status_n register will go high. LSB=10ms

Address:	0x0594:0x0595	
Name:	ref_gst_qual	
Default:	0x0014	
Type:	R/W	
Bit Field	Function Name	Description
15:0		Sets the time to qualify the reference after both the CFM and SCM indicators are low. If the GST qualify timer expires without detecting a CFM or SCM failure, the gst bit in the associated ref_mon_status_n register will go low. LSB=10ms

Address:	0x0596	
Name:	ref_sfm	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		Sets the step frequency monitor threshold, 0=disabled. If a reference has a sudden frequency step that exceeds this threshold, the sfm bit in the associated register at 0x108-0x111 (ref_mon_status_n) will go high. It will stay high until the associated bit in register 0x203-0x204 (ref_sfm_clr_3_0 or ref_sfm_clr_4) is set to 1. LSB=+/-1ppm.

Address:	0x0597	
Name:	ref_pfm_ctrl	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:1	reserved	
0	resolution	Sets the resolution and range of ref_pfm_disqualify (0x598-0x599) and ref_pfm_qualify (0x59A-0x59B). 0: Resolution is 0.005ppm, range is (+/-) 0.005ppm to 327.675ppm (only available for ref frequency <=20MHz). 1: Resolution is 0.05ppm, range is (+/-) 0.05ppm to 3276.75ppm. PFM should not be configured greater than the maximum pull-in range for DPLLs (+/-2100ppm).

Address:	0x0598:0x0599	
Name:	ref_pfm_disqualify	
Default:	0x6568	
Type:	R/W	
Bit Field	Function Name	Description
15:0		Sets the Precise Frequency Monitor (PFM) disqualify frequency offset, where LSB is either 0.005ppm or 0.05ppm as specified by ref_pfm_ctrl::resolution. If a reference exceeds this offset, the pfm bit in the associated ref_mon_status_n register will go high. The default value is 130ppm. It is recommended that this disqualify threshold be set smaller than the dpll tracking range set by the dpll_range mailbox register for each DPLL that my use the reference. When split-XO behavior is disabled, this offset is with respect to the XO wired to the MCLKIN_P and OSCI pins. When split-XO behavior is enabled:

		(a) for regular inputs this offset is with respect to the selected TCXO/OCXO (b) for TCXO/OCXO inputs this offset is with respect to the XO wired to the MCLKIN_P and OSCI pins.

Address:	0x059A:0x059B	
Name:	ref_pfm_qualify	
Default:	0x4E48	
Type:	R/W	
Bit Field	Function Name	Description
15:0		Sets the PFM qualify frequency offset, where LSB is either 0.005ppm or 0.05ppm as specified by ref_pfm_ctrl::resolution. If a reference is below this offset, the pfm bit in the associated ref_mon_status_n register will go low. The default value is 100ppm. When split-XO behavior is disabled, this offset is with respect to the XO wired to the MCLKIN_P and OSCI pins. When split-XO behavior is enabled: (a) for regular inputs this offset is with respect to the selected TCXO/OCXO (b) for TCXO/OCXO inputs this offset is with respect to the XO wired to the MCLKIN_P and OSCI pins. Note that when the reference offset is between the qualify and disqualify limits (hysteresis), the state of the pfm bit in the ref_mon_status_n register will not be changed.

Address:	0x059C:0x059D	
Name:	ref_pfm_period	
Default:	0x0000	
Type:	R/W	
Bit Field	Function Name	Description
15:0		This is the observation time of the precise frequency monitor. Range 1 to 2048s with 1s resolution. The default value of 0 represents 10s. After a reference signal is applied to the device the PFM takes this duration to qualify the input. This field is ignored and the period internally set to 10s for the sync input of a ref-sync pair.

Address:	0x059E	
Name:	ref_pfm_filter_limit	
Default:	0x28	
Type:	R/W	
Bit Field	Function Name	Description
7:0		The PFM filter limit represents a threshold. When the threshold is a non-zero value, and the difference between the PFM average filter output and 10 second PFM average is larger than this threshold, the PFM average filter will be replaced by 10 second PFM average output. The purpose of this is to speed up the filter reaction. The default value corresponds to a 4ppm filter limit. A value of 0 disables the filter limit check. Any other value is in units (or resolution) of 100ppb. Thus the allowed range is 100ppb to 25.5ppm. It is recommended to be used for PFM filter average time being

		larger than 10 sec. This threshold should be set to 0 (means disabled) when the average time is smaller than 10 sec.

Address:	0x05A0	
Name:	ref_sync	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	pair	This bitfield is only used when the ref_sync::mode bitfield is set to 0x1 (physical ref-sync pair mode enabled). This field indicates which input reference should be treated as the frame sync for the associated reference. An invalid value disables ref-sync pairing mode (i.e., the behavior of this reference will be the same as though the mode bitfield is programmed to 0x0). For example, if this bitfield is programmed to 0x5 for the REF0P mailbox, when a DPLL locks to REF0P, its output frame pulses will be phase aligned with the frame pulse on REF2N.
3:0	mode	This field enables a frame sync input for the reference, and selects the source of the frame information: 0x0: Ref-sync pairing mode is disabled. 0x1: Physical ref-sync pair mode is enabled. The frame sync clock phase information is derived from the reference clock indicated by the pair field, above. 0x2-0xF: Invalid (ref-sync disabled)

Address:	0x05A1	
Name:	ref_sync_misc	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:1	reserved	
0	edge_sel	Sets the expected edge alignment of an input sync relative to its associated input reference (e.g., if REF0P uses REF2N as its sync, this bit must be configured in the REF2N mailbox). 0: Sync is aligned to the rising edge of the associated input reference 1: Sync is aligned to the falling edge of the associated input reference

Address:	0x05A2	
Name:	ref_sync_offset_comp	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		Sets the compensation constant of an input sync relative to its associated input reference (e.g., if REF0P uses REF2N as its sync, this register must be configured in the REF2N mailbox). The value is specified as an 8-bit signed two's complement, in units of 0.5ns. Sync Offset [ns] = 0.5 * ref_sync_offset_comp giving a range of -64ns to +63.5ns.

Address:	0x05A3:0x05A6	
Name:	ref_phase_offset_compensation	
Default:	0x00000000	
Type:	R/W	
Bit Field	Function Name	Description
31:0		Phase offset compensation for references. The value is specified as a 32-bit signed two's complement, in units of ps. A positive value will move the phase of any DPLL that locks to this reference earlier in time (more to the left on a scope). A negative value will move the phase of any DPLL that locks to this reference later in time (more to the right on a scope). Note: When a DPLL with hitless switching enabled (dpll_ctrl_x::tie_clear=0) switches to a REF, the ref_phase_offset_compensation value has no effect on DPLL phase. This is because in hitless switching the DPLL phase should not change regardless of the phase of the new REF. AFTER the DPLL has switched to the REF, any CHANGE in ref_phase_offset_compensation affects DPLL phase.

Address:	0x05A8:0x05AB	
Name:	ref_scm_fine	
Default:	0x00000000	
Type:	R/W	
Bit Field	Function Name	Description
31:0		Fine SCM limit configuration. The units of this register depend on the real master clock frequency, and can be calculated using the register at Addresses 0x00B-0x00E (central_freq_offset). LSB = 1.25ns * (2^32 + central_freq_offset) / 2^32 For 25MHz, 50MHz and 125MHz local XO the LSB is 1.25ns. For 24.576MHz and 49.152MHz local XO the LSB is ~1.272ns. For 114.285MHz local XO the LSB is ~1.367ns. Note: for 1Hz and kHz input references, this field must be set larger than the input reference period multiplied by the worst-case frequency offset of the local oscillator connected to the MCLKIN pin. For example, if the local oscillator frequency offset spec is +/-50ppm, that offset would lead to a 50ppm measurement error of the input reference's period, which is 1s * 50ppm = 50us. In this case ref_fine_scm must be set larger than 50us (50,000ns) to avoid falsely invalidating the input reference due to frequency offset of the XO.

Address:	0x05FE	
Name:	uport	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	lockout	When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing.
6:1	reserved	

0	status	This field indicates if microport attempted access had not been successful. The register content will be 0x00 if the access had been successful.

Address:	0x05FF	
Name:	page_sel	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		Unsigned binary value of these bits represents selected page for SPI/I2C access: 0x00: page 0 (first 128 bytes) 0x01: page 1 (second 128 bytes) 0x02: page 2 (third 128 bytes) 0x03: page 3 (fourth 128 bytes) 0x04: page 4 (fifth 128 bytes) 0x05: page 5 (sixth 128 bytes) 0x06: page 6 (seventh 128 bytes) 0x07: page 7 (eighth 128 bytes) 0x08: page 8 (ninth 128 bytes) 0x09: page 9 (tenth 128 bytes) 0x0A: page 10 (eleventh 128 bytes) 0x0B: page 11 (twelfth 128 bytes) 0x0C: page 12 (thirteenth 128 bytes) 0x0D-0xFF: reserved

9.3.12 Register List Page 12, DPLL MB

Address:	0x0602:0x0603	
Name:	dpll_mb_mask	
Default:	0x0001	
Type:	R/W	
Bit Field	Function Name	Description
15:6	reserved	
5:0	mask	For a write operation (see dpll_mb_sem::wr bit), this field determines which DPLL's configuration is modified. Multiple bits can be set to affect multiple DPLLs in a single operation. For a read operation (see dpll_mb_sem::rd bit), this field determines which DPLL configuration to read back from the device. One (and only one) bit should be set for a read operation.

Address:	0x0604	
Name:	dpll_mb_sem	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:2	reserved	
1	rd	When this bit is written to a one by the host controller, the device will perform a read of the masked DPLL (see dpll_mb_mask register). Only one mask bit should be set in this case. When this register reads back 0x00, then the read has completed, and the host can read back any or all of the registers on this page to determine the corresponding DPLL configuration.
0	wr	When this bit is written to a one by the host controller (and the rd bit is zero), the device will perform a write of the masked DPLL (see dpll_mb_mask register). All of the configuration options on

		this page will be applied to each of the DPLLs indicated by the mask. The write is complete when this register reads back a zero.

Address:	0x0605	
Name:	dpll_bw_fixed	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	reserved	
3	reserved	
2:0	bw	Sets the DPLL loop filter corner frequency. 000: 14 Hz 001: 29 Hz 010: 61 Hz 011: 130 Hz 100: 380 Hz 101-110: 470Hz 111: reserved

Address:	0x0607	
Name:	dpll_config	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:6	ref_edge	Sets the DPLL selected reference edge sensitivity. 00: positive (rising) edge 01: negative (falling) edge 10: low pulse 11: high pulse The low and high pulse options select the middle between edges.
5:0	reserved	

Address:	0x0608:0x0609	
Name:	dpll_psl	
Default:	0x0000	
Type:	R/W	
Bit Field	Function Name	Description
15:0		Sets the phase slope limit, in units of ns/s. The valid range is 400ns/s to 65535ns/s. A value of 0 sets the PSL to "unlimited". If fast-lock is disabled then PSL must be set larger than twice the worst-case input frequency offset. If fast-lock is enabled then when a fast-lock phase or frequency threshold is exceeded then PSL is disabled during fast-lock.

Address:	0x060E:0x060F	
Name:	dpll_range	
Default:	0x0078	
Type:	R/W	
Bit Field	Function Name	Description
15:0		Sets the pull-in/hold-in range, in steps of 0.1ppm. (from 0.1ppm to 2100ppm, in 0.1ppm steps). Default value corresponds to 12ppm.

Address:	0x0610	
Name:	dpll_ref_sw_mask	
Default:	0x08	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	This bit acts as an enable mask for the SFM failure reference switch. See pfm bit description.
4	pfm	This bit acts as an enable mask for the PFM failure reference switch. When this bit is set, a PFM failure of the selected reference will cause the associated DPLL to perform a reference switch. When the bit is cleared, a PFM failure will be ignored by the reference switch algorithm (a switch to holdover may still be possible, see the dpll_ref_ho_mask::pfm bitfield for details). Note that the DPLL also will not switch to a reference which has a PFM failure while either the PFM reference switch or holdover mask bits are set. All fields in this register are ignored for DPLL4 and DPLL5.
3	gst	This bit acts as an enable mask for the GST failure reference switch. See pfm bit description.
2	cfm	This bit acts as an enable mask for the CFM failure reference switch. See pfm bit description.
1	scm	This bit acts as an enable mask for the SCM failure reference switch. See pfm bit description.
0	los	This bit acts as an enable mask for the LOS failure reference switch. See pfm bit description.

Address:	0x0611	
Name:	dpll_ref_ho_mask	
Default:	0x17	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	
5	sfm	This bit acts as an enable mask for the SFM holdover switch. See pfm bit description.
4	pfm	When set to high, this bit will allow selected reference PFM failure to cause associated DPLL to go to holdover. When low, selected reference PFM failure will be masked and the associated DPLL will not go to holdover due to the PFM failure. A switch to holdover will only be attempted after all reference switching options have been exhausted, regardless of the state of the dpll_ref_ho_mask bits.
3	gst	This bit acts as an enable mask for the GST holdover switch. See pfm bit description.
2	cfm	This bit acts as an enable mask for the CFM holdover switch. See pfm bit description.
1	scm	This bit acts as an enable mask for the SCM holdover switch. See pfm bit description.
0	los	This bit acts as an enable mask for the LOS holdover switch. See pfm bit description.

Address:	0x0614	
Name:	dpll_ref_prio_0	
Default:	0x10	
Type:	R/W	
Bit Field	Function Name	Description
7:4	ref_0N	When the DPLL is in automatic mode of operation (see register at address 0x210 bits 2:0, dpll_mode_refsel_x::mode bitfield), these bits set the priority of each reference for the DPLL. 0000 is highest priority and 1110 is lowest priority. Setting these bits to 1111 will disable the reference (the DPLL will never lock to it). When two references are programmed to have different priority numbers, the DPLL will perform revertive switching between them: the DPLL will always switch to the highest priority reference (lowest priority number) whenever that reference is qualified. When two references are programmed to have the same priority number, the DPLL will perform non-revertive switching between them: the DPLL will not switch to the reference with the same priority when that reference qualifies. Combinations of same and different priority numbers can be used, such that DPLL performs revertive switching between different priority references, but non-revertive switching among references with the same priority. Example: if REF0P has priority 0 (highest), REF0N, REF1P and REF1N have priority 1. Whenever REF0P is qualified, the DPLL will switch to it. If REF0P is disqualified, the DPLL will not change the currently selected reference (e.g., REF1N) even if another reference with the same priority is qualified (e.g., REF0N or REF1P). The fields in 0x0614-0x0618 are ignored for DPLL4 and DPLL5. Priority of REF0N.
3:0	ref_0P	Priority of REF0P.

Address:	0x0615	
Name:	dpll_ref_prio_1	
Default:	0x32	
Type:	R/W	
Bit Field	Function Name	Description
7:4	ref_1N	Priority of REF1N.
3:0	ref_1P	Priority of REF1P.

Address:	0x0616	
Name:	dpll_ref_prio_2	
Default:	0x54	
Type:	R/W	
Bit Field	Function Name	Description
7:4	ref_2N	Priority of REF2N.
3:0	ref_2P	Priority of REF2P.

Address:	0x0617	
Name:	dpll_ref_prio_3	
Default:	0x76	
Type:	R/W	
Bit Field	Function Name	Description
7:4	ref_3N	Priority of REF3N.
3:0	ref_3P	Priority of REF3P.

Address:	0x0618	
Name:	dpll_ref_prio_4	
Default:	0x98	
Type:	R/W	
Bit Field	Function Name	Description
7:4	ref_4N	Priority of REF4N.
3:0	ref_4P	Priority of REF4P.

Address:	0x061C	
Name:	dpll_ho_filter	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:5	reserved	
4	nco_en	0: Holdover filter is not updated while DPLL is NCO mode. 1: Holdover filter will be updated in NCO mode.
3:0	bw	This bitfield specifies the holdover filter bandwidth. The default value of 0x0 means the filter is bypassed. BW = 174.386 / (2^n * 2 * pi) Hz These are the possible settings: 0x0: Bypass 0x1: 13.9 Hz 0x2: 6.9 Hz 0x3: 3.5 Hz 0x4: 1.7 Hz 0x5: 867 mHz 0x6: 434 mHz 0x7: 217 mHz 0x8: 108 mHz 0x9: 54.2 mHz 0xA: 27.1 mHz 0xB: 13.6 mHz 0xC: 6.8 mHz 0xD: 3.4 mHz 0xE: 1.7 mHz 0xF: 0.8 mHz

Address:	0x061D	
Name:	dpll_ho_delay	
Default:	0x4C	
Type:	R/W	
Bit Field	Function Name	Description
7:0		This register specifies the DPLL holdover storage delay using the following formula: Value = round(32 * log(delay)), where delay is in ms

		Example, if desired delay is 1ms, value to be written to this register is 0x00, for 1 second the value is 0x60, and for 2 hours the value is 0xDC. The default value of 0x4C corresponds to 237ms.

Address:	0x0620	
Name:	dpll_fast_lock_ctrl	
Default:	0x01	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	
5:4	fcl_en	00: If bandwidth <= 0.1Hz, FCL is enabled; otherwise, FCL is disabled. 10: FCL is enabled, regardless of bandwidth. x1: FCL is disabled, regardless of bandwidth.
3	reserved	
2	nco_en	Controls whether fast lock is forcibly disabled during transitions out of NCO mode. 0: Fast lock is disabled during transitions out of NCO mode 1: Fast lock is allowed during transitions out of NCO mode
1	force_en	This is the control to force-enable the fast lock state. Note that the the master-control (bit 0 of this register) still has to be enabled for this control to work. This control, when enabled, will ignore the outputs of the frequency and phase error monitors.
0	en	0: Fast lock state disabled 1: Fast lock state enabled

Address:	0x0621	
Name:	dpll_fast_lock_phase_err	
Default:	0xFF	
Type:	R/W	
Bit Field	Function Name	Description
7:0		This is the phase error threshold for triggering a transition to fast-lock. The threshold is specified in steps of 250ns, with a value of zero being reserved for disabling the phase error threshold check.

Address:	0x0622	
Name:	dpll_fast_lock_freq_err	
Default:	0x04	
Type:	R/W	
Bit Field	Function Name	Description
7:0		This is the frequency error threshold for triggering a transition to fast-lock. The threshold is specified in steps of 1ppm, programmable from 1 to 255ppm. If the threshold is programmed to zero, the fast-lock frequency error check is disabled.

Address:	0x0623:0x0624	
Name:	dpll_fast_lock_ideal_time	
Default:	0x0000	
Type:	R/W	
Bit Field	Function Name	Description
15:0		Ideal time for fast lock in units of 0.01s. If the input wander is much lower than standard levels, this register can be reprogrammed to speed up the fast lock process.

		If this value is set to zero, the device use the following default values based on the DPLL bandwidth: BW <= 2 mHz : 210.0 sec 2 mHz < BW <= 5 mHz : 110.0 sec 5 mHz < BW <= 20 mHz : 100.0 sec 20 mHz < BW <= 80 mHz : 50.0 sec 80 mHz < BW <= 5 Hz : 25.0 sec 5 Hz < BW <= 10 Hz : 1.0 sec 10 Hz < BW : 0.6 sec Note that this is the target time for fast lock which is usually the first step to lock to a reference. The lock time will be longer if the value in registers 0x626-0x627 (dpll_fast_lock_fol) meets the following condition: (dpll_fast_lock_fol * 10^-6) < 0.5 * (1 / input_freq[Hz]) / (dpll_fast_lock_ideal_time * 0.01)

Address:	0x0626:0x0627	
Name:	dpll_fast_lock_fol	
Default:	0x07D0	
Type:	R/W	
Bit Field	Function Name	Description
15:0		Fast lock frequency offset limit. LSB=1ppm. This register controls the maximum frequency offset this DPLL can apply while in the fast lock mode. The default value (2000ppm) should not be changed, unless recommended by Microsemi.

Address:	0x062E	
Name:	dpll_damping	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:5	reserved	
4:0	factor	Sets the DPLL damping factor. 0: 5 1: 1 2: 2 3: 2.998801 4: 4.003204 5: 5 (default, peaking <0.25dB) 6: 6.019293 7: 7.0014 8: 8.006408 9: 8.980265 10: 10 11: 10.91089 12: 12.12678 13: 12.90994 14: 13.8675 15: 15.07557 16: 15.81139 17: 16.66667 18: 17.67767

		19: 18.89822 20: 20.41241 21: 22.36068 22: 25 23: 28.86751 24: 35.35534 25-31: 50

Address:	0x0630:0x0633	
Name:	dpll_phase_bad	
Default:	0x02255100	
Type:	R/W	
Bit Field	Function Name	Description
31:0		Sets the phase for loss-of-lock, LSB=1ps. The default value (0x02255100) is 36us. Any time the DPLL's phase offset is greater than this value, the DPLL lock indicator will go low. Programming this register to 0x00000000 will internally set the value using registers 0x634-0x637 (dpll_phase_good).

Address:	0x0634:0x0637	
Name:	dpll_phase_good	
Default:	0x02255100	
Type:	R/W	
Bit Field	Function Name	Description
31:0		Sets the phase for lock declaration, LSB=1ps. The default value (0x02255100) is 36us. The DPLL's phase offset must be less than this value for the duration programmed in register 0x638 (dpll_duration_good).

Address:	0x0638	
Name:	dpll_duration_good	
Default:	0x09	
Type:	R/W	
Bit Field	Function Name	Description
7:0		DPLL phase magnitude must be less than dpll_phase_good for the duration specified by this field for the DPLL to declare lock. The desired duration and the dpll_duration_good value are related as follows: duration[sec] = dpll_duration_good + 1 The default value (0x09) is 10s.

Address:	0x0639	
Name:	dpll_lock_delay	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		Sets the lock declaration delay time. The actual delay time will be the square of the value written to this register, giving a range of 0 to 255^2, in seconds. A value of 0 disables the lock delay timer. This register is ignored for DPLL4 and DPLL5.

Address:	0x063A	
Name:	dpll_tie	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	reserved	
3	ref_sync_after_lock	0: The DPLL will measure the sync pulse offset as soon as possible. 1: The DPLL will only measure the sync pulse offset when the programmed lock criteria is met (see registers 0x630-0x638).
2	tie_wr_meas_sync	0: A TIE-write does not affect sync pulse measurement. 1: A TIE-write will cause a sync pulse measurement to occur as soon as possible. This setting has no effect if the DPLL is locking to a clock-only input reference. This bit and ref_sync_tie_wr should always be set to the same value.
1	ref_sync_tie_wr	0: All TIE-writes are applied as soon as possible. TIE-clear is evaluated as soon as possible. 1: When the DPLL is configured to lock to a ref-sync pair, TIE-write and TIE-clear operations are delayed until the sync pulse offset has been measured. When locking to a clock-only input, TIE-write and TIE-clear operations will be applied as soon as possible. This bit and tie_wr_meas_sync should always be set to the same value.
0	switch_clear_en	This bit enables the TIE-write clear on reference switch mode of operation. The DPLL's tie_clear bit (e.g., register 0x211 bit 0 for DPLL0) must also be set to 1, or the DPLL must be configured to lock to a ref-sync pair for this feature to be enabled. When this bit is set, the corresponding DPLL will clear the accumlated TIE from all previous TIE-write operations whenever the DPLL performs a reference switch, whenever the DPLL mode is changed from NCO to either Automatic or Forced Reference, and whenever the DPLL exits the holdover state.

Address:	0x063B	
Name:	dpll_tie_wr_thresh	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		This register specifies the threshold for declaring that a TIE-write operation has completed. When the output has moved within the threshold of the expected alignment position, then the dpll_tie_wr_sticky register will indicate that the TIE-write operation has completed. When this register is programmed to the default of 0x00, the sticky bits in dpll_tie_wr_sticky will never be set. Otherwise, a non-zero value specifies the threshold in 10 ns steps (10ns to 2.55us range).

Address:	0x063C	
Name:	dpll_fp_first_realign	
Default:	0x7F	
Type:	R/W	
Bit Field	Function Name	Description
7	reserved	
6:0	time	When the DPLL is configured to lock to a ref-sync pair or clock-

		PPS sync (frame pulse), it performs phase measurements of the frame pulse and aligns its phase based on this measurement. This parameter sets the time between the first and second frame pulse phase measurements. LSB = 1 second. Values 0 and 1 are invalid. See register 0x5A0, bits 3:0 (ref_sync::mode) for additional details about reference configuration. See register 0x63D, bits 6:0 (dpll_fp_realign_intvl::time) for details about periodic phase measurements. This register is ignored for DPLL3-DPLL5.

Address:	0x063D	
Name:	dpll_fp_realign_intvl	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	continuous	0: Continuous ref-sync measurement disabled. The time bitfield in this register is used. 1: Continuous ref-sync measurement enabled. The DPLL will measure the ref-sync offset and realign as fast as possible. The time bitfield in this register is ignored. This register is ignored for DPLL3-DPLL5.
6:0	time	When the DPLL is configured to lock to a ref-sync pair, it performs phase measurements of the frame pulse and aligns its phase based on this measurement. This parameter sets the time between the periodic phase measurements, which will occur after the second measurement. LSB = 1 second. If this bitfield is programmed to zero, periodic realignment is disabled. See register 0x5A0, bits 3:0 (ref_sync::mode) for additional details about reference configuration. See register 0x63C, bits 6:0 (dpll_fp_first_realign::time) for details about first and second phase measurements. This register is ignored for DPLL3-DPLL5.

Address:	0x063E	
Name:	dpll_fp_lock_thresh	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		When the DPLL is configured to lock to a ref-sync pair or clock-PPS sync (frame pulse), it performs phase measurements of the frame pulse and aligns its phase based on this measurement. This parameter sets the phase threshold to declare lock and is logcially ANDed with all other lock criteria. LSB = 20ns. A value of 0x00 disables this feature. When the active input is clock-only, this parameter is ignored. See register 0x5A0, bits 3:0 (ref_sync::mode) for additional details about reference configuration. This register is ignored for DPLL3-DPLL5.

Address:	0x067E	
Name:	uport	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	lockout	When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing.
6:1	reserved	
0	status	This field indicates if microport attempted access had not been successful. The register content will be 0x00 if the access had been successful.

Address:	0x067F	
Name:	page_sel	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		Unsigned binary value of these bits represents selected page for SPI/I2C access: 0x00: page 0 (first 128 bytes) 0x01: page 1 (second 128 bytes) 0x02: page 2 (third 128 bytes) 0x03: page 3 (fourth 128 bytes) 0x04: page 4 (fifth 128 bytes) 0x05: page 5 (sixth 128 bytes) 0x06: page 6 (seventh 128 bytes) 0x07: page 7 (eighth 128 bytes) 0x08: page 8 (ninth 128 bytes) 0x09: page 9 (tenth 128 bytes) 0x0A: page 10 (eleventh 128 bytes) 0x0B: page 11 (twelfth 128 bytes) 0x0C: page 12 (thirteenth 128 bytes) 0x0D-0xFF: reserved

9.3.13 Register List Page 14, Misc

Address:	0x0706	
Name:	psrg_ctrl	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:1	reserved	
0	disable	0: PSRG enabled 1: PSRG disable Applications concerned with minimizing close-to-carrier phase noise should set this bit to 1.

10. Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply voltage, nominal 1.5V	VDD15	-0.3	1.65	V
Supply voltage, nominal 1.8V	VDD18	-0.3	1.98	V
Supply voltage, nominal 2.5V	VDD25	-0.3	2.75	V
Supply voltage, nominal 3.3V	VDD33	-0.3	3.63	V
Voltage on OSCI, any REF, HPOUT or GPOUT pin	VANAPIN	-0.3	3.63	V
Voltage on any digital I/O pin	VDIGPIN	-0.3	3.63	V
Storage Temperature Range	T_{ST}	-55	+125	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
* Voltages are with respect to ground (VSS) unless otherwise stated.

Note 1: The typical values listed in the tables of Section 10 are not production tested.
Note 2: Specifications to -40°C and 85°C are guaranteed by design or characterization and not production tested.

Table 3 - Recommended DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply voltage 3.3V	VDD, VDDH	3.135	3.3	3.465	V
Supply voltage 1.8V	VDD_DRI, VDDL	1.71	1.8	1.89	V
Output supply voltage	VDDO_x_y	1.425 1.71 2.375	1.5 1.8 2.5	1.575 1.89 2.625	V
		same as VDDH			
Operating temperature	T_A	-40		+85	°C

Table 4 - Electrical Characteristics: Supply Currents

Characteristics	Symbol	Min.	Typ.[1]	Max	Units	Notes
Total power, two CMOS REF inputs, Synth1 and six LVDS outputs enabled	P_{DISS}		1.3		W	
Total current on 3.3V supply	I_{DD33}		296	445	mA	Note 2
Total current on 1.8V supply	I_{DD18}		422	615	mA	Note 2
VDD supply current change from enabling or disabling Synth0	ΔI_{DDA0}		22		mA	
VDD_DRI supply current change from enabling or disabling Synth0	ΔI_{DDA0}		4		mA	
VDDH supply current change from enabling or disabling Synth2	ΔI_{DDHA2}		85		mA	
VDDL supply current change from enabling or disabling Synth2	ΔI_{DDLA2}		64		mA	
VDD supply current change from enabling or disabling a CMOS REF input clock	ΔI_{DDHCIN}		4		mA	Measured at 200MHz
VDD_DRI supply current change from enabling or disabling a CMOS REF input clock	ΔI_{DDLCIN}		0.7		mA	
VDD supply current change from enabling or disabling a differential REF input clock	ΔI_{DDHDIN}		4		mA	Measured at 800MHz
VDD_DRI supply current change from enabling or disabling a differential REF input clock	ΔI_{DDLDIN}		2.25		mA	
VDDL supply current change from enabling or disabling the Synth1 or 2 fractional output divider	ΔI_{DDLHSD}		38		mA	
VDDL supply current from enabling/disabling output divider for one HPOUT	ΔI_{DDLDIV}		13		mA	
VDDL supply current change from enabling or disabling an HPOUT for LVDS, LVPECL or HCSL	ΔI_{DDLD}		13		mA	

Characteristics	Symbol	Min.	Typ.[1]	Max	Units	Notes
VDDL supply current change from enabling or disabling an HPOUT for CMOS or HSTL	ΔI_{DDLC}		16		mA	
VDDOx supply current change from enabling or disabling an LVDS HPOUT	ΔI_{DDOD}		9		mA	
VDDOx supply current change from enabling or disabling an LVPECL HPOUT	ΔI_{DDOP}		15		mA	
VDDOx supply current change from enabling or disabling an HCSL HPOUT	ΔI_{DDOHC}		15		mA	Note 5
VDDOx supply current change from enabling or disabling a CMOS HPOUT	ΔI_{DDOC}		6		mA	Note 3
VDDOx supply current change from enabling or disabling an HSTL HPOUT	ΔI_{DDOHS}		6		mA	Note 4
VDD supply current change from enabling or disabling a GPOUT	ΔI_{DDGPO}		6		mA	Note 4

Note 1: Typical values measured at nominal supply voltages and 25°C ambient temperature.

Note 2: Max I_{DD} measurements made with all blocks enabled, 156.25MHz signals on all REF inputs, doubler off , Synth0 frequency of 781.25MHz, GPOUT outputs 156.25MHz, Synth1 and Synth2 VCO frequency of 3750MHz, Synth1 and Synth2 integer dividers dividing by 6, all MSDIV dividing by 2, all LSDIV dividing by 2, all HPOUT outputs enabled as LVPECL outputs driving 156.25MHz signals, and all VDDO at 3.3V. Typical I_{DD} measurements made with same setup as max I_{DD} but only four REF inputs enabled, Synth0 and GPOUT0-1 disabled, Synth1 and Synth2 fractional dividers disabled and only six outputs enabled with LVDS signal format. Measurements include current into VDDOx pins.

Note 3: VDDOx=3.3V, 1x drive strength, f_O=250MHz, 2pF load

Note 4: VDDOx=1.8V, 2x drive strength, f_O=100MHz, 100Ω differential termination.

Note 5: 50Ω to ground each on HPOUTxP and HPOUTxN.

Table 5 - Electrical Characteristics: OSCI Clock Input

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Input high voltage, OSCI	V_{IH}	1.2		VDDH	V	Note 1
Input low voltage, OSCI	V_{IL}			0.8	V	Note 1
Input frequency, OSCI pin to Synth input mux	f_{IN}	9.72		156.25	MHz	Synth1 or 2
Input frequency, OSCI pin to Synth bypass mux	f_{IN}			156.25	MHz	Synth1 or 2
Input leakage current	I_{IL}	-10		10	µA	
Input duty cycle, OSCI frequency ≤ 25MHz, OSCI doubler enabled		45		55	%	Note 1
Input duty cycle, all other cases		40		60	%	Note 1

Note 1: 1.0V threshold. Note that CMOS input signals from 1.8V to 3.3V can be applied directly to the OSCI pin without AC-coupling. Only the rising edge of the signal is used by the device.

Table 6 - Electrical Characteristics: Reference Inputs, REFx

Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
Single-ended CMOS input high voltage	$V_{IH-CMOS}$	$0.7 \cdot V_{DD}$			V	Notes
Single-ended CMOS input low voltage	$V_{IL-CMOS}$			$0.3 \cdot V_{DD}$	V	
Single-ended CMOS input leakage current	$I_{IL-CMOS}$	-10		10	µA	
Single-ended PECL input high voltage	$V_{IH-PECL}$	$V_{REF-PECL}$ + 0.15			V	Notes 1, 2
Single-ended PECL input low voltage	$V_{IL-PECL}$			$V_{REF-PECL}$ - 0.15	V	
Single-ended PECL input reference voltage	$V_{REF-PECL}$		$0.55 \cdot V_{DD}$		V	
Single-ended PECL input leakage current	$I_{IL-PECL}$	-10		10	µA	$V_I = V_{DD}$ or 0.8V
Differential input common mode voltage	V_{CMI}	1.1		2.0	V	Note 1,

Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
						$V_I = V_{DD}$ or 0.8V
Differential input voltage difference	V_{ID}	0.25		1.0	V	See Figure 27
Differential input leakage current	I_{IL}	-10		10	µA	See Figure 27

Note 1: Leakage current flowing out of the device pin referenced as positive

Note 2: $V_I = V_{DD}$ or 0V

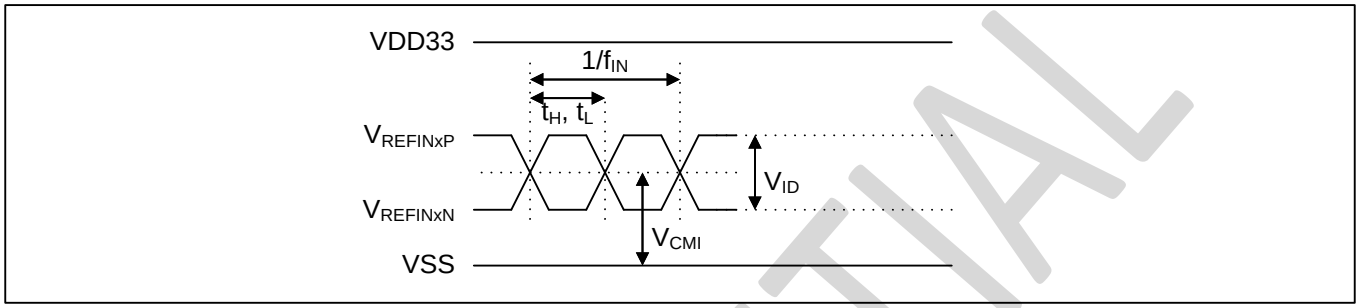


Figure 27 - Electrical Characteristics: Reference Inputs

Table 7 - Electrical Characteristics: Other Inputs and I/O (Bidirectional)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Input high voltage for MCLKIN_P, SRST_B, and GPIO[8:5] pins	$V_{IH-CMOS}$	$0.7 \cdot V_{DD}$			V	
Input low voltage for MCLKIN_P, SRST_B, and GPIO[8:5] pins	$V_{IL-CMOS}$			$0.3 \cdot V_{DD}$	V	
Input leakage current for MCLKIN_P, SRST_B, and GPIO[8:5] pins	$I_{IL-CMOS}$	-10		10	µA	Notes 1, 2
Schmitt input high voltage for CS_B_ASEL0, MC0, MC1, and RST_B pins	$V_{IH-SCHM}$	2.0			V	
Schmitt input low voltage for CS_B_ASEL0, MC0, MC1 and RST_B pins	$V_{IL-SCHM}$			0.7	V	
Schmitt input leakage current for CS_B_ASEL0, MC0, MC1 and RST_B pins (33kΩ pullup)	$I_{IL-SCHM}$	-10		160	µA	Notes 1, 2
Bidirectional Schmitt input high voltage for SI_SDA, SCK_SCL, SO_ASEL1, GPIO0_IF, GPIO1 and GPIO2 pins	$V_{IH-BIDI}$	2.0			V	
Bidirectional Schmitt input low voltage for SI_SDA, SCK_SCL, SO_ASEL1, GPIO0_IF, GPIO1 and GPIO2 pins	$V_{IL-BIDI}$			0.7	V	
Bidirectional Schmitt input leakage current for SO_ASEL1 pin	$I_{IL-BIDI}$	-10		10	µA	Notes 1, 2
Bidirectional Schmitt input leakage current for SI_SDA, SCK_SCL, GPIO1 and GPIO2 pins (33kΩ pullup)	$I_{IL-BIDI}$	-10		160	µA	Notes 1, 2
Input leakage current for GPIO0 pin (33kΩ internal pulldown)	$I_{IL-BIDI}$	-160		10	µA	Notes 1, 2

Note 1: Leakage current flowing out of the device pin referenced as positive

Note 2: $V_I = V_{DD}$ or 0V

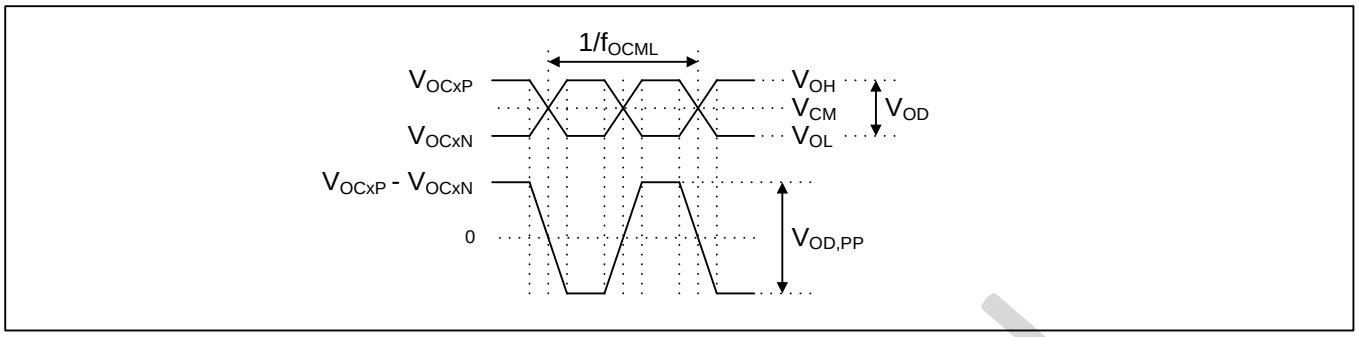


Figure 28 - Electrical Characteristics: Differential Clock Outputs

Table 8 - Electrical Characteristics: HPOUT LVDS Clock Outputs

VDDOx = 2.5V±5% or 3.3V±5% for LVDS operation.

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Output frequency	f_{OCD}			1045	MHz	
Output common-mode voltage	V_{CM}	1.13	1.2	1.37	V	Note 1. See Figure 28
Output differential voltage	V_{OD}	310	420	530	mV	Note 1. See Figure 28
Output differential swing, peak-to-peak	$V_{OD,PP}$	620	840	1060	mV_{PP}	Note 1. See Figure 28
Output rise/fall time	t_R, t_F		150		ps	20%-80%
Output duty cycle		45	50	55	%	

Note 1: Output must have 100Ω - 200Ω DC path between HPOUTxP and HPOUTxN for proper operation. See Figure 16 for recommended external components.

Table 9 - Electrical Characteristics: HPOUT LVPECL Clock Outputs

VDDOx = 2.5V±5% or 3.3V±5% for LVPECL operation.

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Output frequency	f_{OCD}			1045	MHz	
Output common-mode voltage, VDDOx=3.3V	V_{CM}	1.85	1.95	2.05	V	Note 1. See Figure 28
Output common-Mode voltage, VDDOx=2.5V	V_{CM}	1.13	1.23	1.33	V	Note 1. See Figure 28
Output differential voltage	V_{OD}	630	820	1050	mV	Note 1. See Figure 28
Output differential swing, peak-to-peak	V_{OD}	1300	1640	2100	mV_{PP}	Note 1. See Figure 28
Output rise/fall time	t_R, t_F		150		ps	20%-80%
Output duty cycle		45	50	55	%	

Note 1: Output must have 100Ω - 200Ω DC path between HPOUTxP and HPOUTxN for proper operation. See Figure 16 for recommended external components.

Table 10 - Electrical Characteristics: HPOUT HCSL Clock Outputs

VDDOx = 2.5V±5% or 3.3V±5% for HCSL operation.

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Output frequency	f_{OCHC}			250	MHz	
Output common-mode voltage	V_{CM}		V_{OD} / 2		V	Note 1. See Figure 28
Output differential voltage	V_{OD}	0.59	0.725	0.95	V	Note 1. See Figure 28
Output rise/fall time	t_R, t_F		250		ps	20%-80%
Output duty cycle		45	50	55	%	

Note 1: Each of HPOUTxP and HPOUTxN with 50Ω termination resistor to ground.

Table 11 - Electrical Characteristics: HPOUT CMOS and HSTL (Class I) Clock Outputs

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Output frequency	f_{OCMOS}	<<1Hz		250	MHz	Note 1
Output high voltage	V_{OH}	VDDOx –0.4		VDDOx	V	Notes 2, 3
Output low voltage	V_{OL}	0		0.4	V	Notes 2, 3
Output rise/fall time, VCCOx=1.8V, 4x drive strength	t_R, t_F		0.4		ns	2pF load
Output rise/fall time, VCCOx=1.8V, 4x drive strength			1.2		ns	15pF load
Output rise/fall time, VCCOx=3.3V, 1x drive strength			0.7		ns	2pF load
Output rise/fall time, VCCOx=3.3V, 1x drive strength			2.2		ns	15pF load
Output duty cycle		45	50	55	%	Note 4, 6
Output duty cycle		42	50	58	%	Notes 5, 6
Output duty cycle, HPOUTxN single-ended			50		%	
Output duty cycle, HPOUTxP single-ended			50		%	
Output current when output disabled	I_{OH}		300		µA	

Note 1: Minimum output frequency is a function of VCO frequency and output divider values and is guaranteed by design.

Note 2: For HSTL Class I, V_{OH} and V_{OL} apply for both unterminated loads and for symmetrically terminated loads, i.e. 50Ω to VDDOx/2.

Note 3: For VDDOx=3.3V and 1x drive strength, I_O=4mA. For VDDOx=1.5V and 4x drive strength, I_O=8mA.

Note 4: Output clock frequency ≤ 160MHz or VDDOx ≥ 1.8V.

Note 5: Output clock frequency > 160MHz and VDDOx < 1.8V.

Note 6: Measured differentially.

Table 12 - Electrical Characteristics: GPOUT Outputs

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
GPOUT output high voltage (I_{OH} = 1.5mA)	$V_{OH-GPOUT}$	0.8 * V_{DD}			V	Drive Setting = 1X
GPOUT output low voltage (I_{OL} = 1.5mA)	$V_{OL-GPOUT}$			0.2 * V_{DD}	V	
GPOUT output high voltage (I_{OH} = 3mA)	$V_{OH-GPOUT}$	0.8 * V_{DD}			V	Drive Setting = 2X
GPOUT output low voltage (I_{OL} = 3mA)	$V_{OL-GPOUT}$			0.2 * V_{DD}	V	
GPOUT output high voltage (I_{OH} = 4.5mA)	$V_{OH-GPOUT}$	0.8 * V_{DD}			V	Drive Setting = 3X
GPOUT output low voltage (I_{OL} = 4.5mA)	$V_{OL-GPOUT}$			0.2 * V_{DD}	V	
GPOUT output high voltage (I_{OH} = 6mA)	$V_{OH-GPOUT}$	0.8 * V_{DD}			V	Drive Setting = 4X
GPOUT output low voltage (I_{OL} = 6mA)	$V_{OL-GPOUT}$			0.2 * V_{DD}	V	

Note 1: All items in this table measured with 22Ω source series resistor and 10pF load.

Table 13 - Electrical Characteristics: Other Outputs and I/O (Bidirectional)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Bidirectional output high voltage for SO_ASEL1 pin	$V_{OH-BIDI}$	$0.8*V_{DD}$			V	I_{OH} = 6mA
Bidirectional output low voltage for SO_ASEL1 pin	$V_{OL-BIDI}$			$0.2*V_{DD}$	V	I_{OL} = 6mA
Bidirectional output low voltage for SI_SDA, SCK_SCL	$V_{OL-BIDI}$			$0.2*V_{DD}$	V	I_{OL} = 2mA
Bidirectional output high voltage for GPIO[2:0]	$V_{OH-BIDI}$	$0.8*V_{DD}$			V	I_{OH} = 2.5mA
Bidirectional output low voltage for GPIO[2:0]	$V_{OL-BIDI}$			$0.2*V_{DD}$	V	I_{OL} = 2.5mA
Bidirectional output high voltage for GPIO[8:5]	$V_{OH-BIDI}$	$0.8*V_{DD}$			V	I_{OH} = 3mA
Bidirectional output low voltage for GPIO[8:5]	$V_{OL-BIDI}$			$0.2*V_{DD}$	V	I_{OL} = 3mA

Table 14 - Electrical Characteristics: Input Timing

Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
Single ended CMOS input reference frequency for REF pins	$1/T_{TREFP}$			180	MHz	
Single ended CMOS input reference pulse width low or high for REF pins	T_{TREFW}	2.7			ns	
Single ended PECL input reference frequency for REF pins	$1/T_{TREFP}$			900	MHz	
Single ended PECL input reference pulse width low or high for REF pins	T_{TREFW}	0.55			ns	
Differential input reference frequency for REF[4:0]P/N	$1/T_{TREFP}$			900	MHz	
Differential input reference pulse width low or high for REF[4:0]P/N	T_{TREFW}	0.55			ns	
Duty Cycle for MCLKIN_P/N		40		60	%	

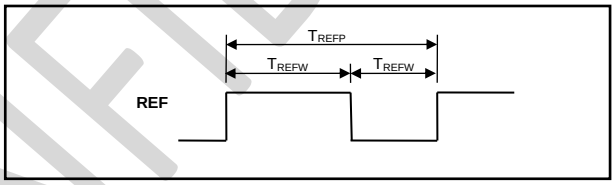


Figure 29 - Input Timing

Table 15 - Electrical Characteristics: REF-SYNC Pair Input Timing

Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
Sync lead time	$T_{SYNC-LD}$	*0*		$T_{REFP}/2 - T_{UNCERT}$	*ns*	See Figure 30
Sync lag time	$T_{SYNC-LG}$	*0*		$T_{REFP}/2 - T_{UNCERT}$	*ns*	
Sync alignment uncertainty	T_{UNCERT}	*0*	*2*	*3*	*ns*	

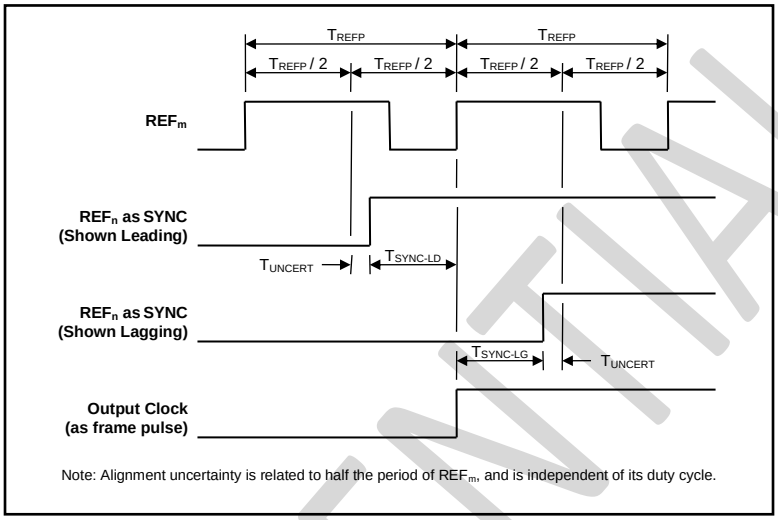


Figure 30 - REF-SYNC Pair Input Timing

Table 16 - Electrical Characteristics: Input-to-Output and Output-to-Output Timing

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Initial Output-to-Output Skew[1, 4]						1, 4
Synth1 HPOUTa to Synth1 HPOUTb skew	t_{OO-S1}	-0.023	0.07	0.18	ns	1, 3, 4
Synth2 HPOUTa to Synth2 HPOUTb skew	t_{OO-S2}	0.02	0.11	0.22	ns	1, 3, 4
Synth1 HPOUT to Synth2 HPOUT skew	$t_{OO-S1-S2}$	-0.05	0.12	0.28	ns	1, 3, 4
Diff HPOUT to CMOS HPOUT skew	$t_{OO-HPd-HPc}$	0.75	1.11	1.58	ns	1, 4, 6, 8, 9
GPOUT0 to GPOUT1 skew	$t_{OO-G0-G1}$	-1.47	0	1.61	ns	1, 2, 4
GPOUT0 to diff HPOUT skew, external feedback for DPLL0-Synth0 path	$t_{OO-G0-HPd-EFB}$	-1.31	-0.69	-0.12	ns	1, 4, 7, 8
GPOUT0 to diff HPOUT skew, without external feedback	$t_{OO-G0-HPd}$	-2.1	0	2.16	ns	1, 4, 6, 8
GPOUT0 to CMOS HPOUT skew, external feedback for DPLL0-Synth0 path	$t_{OO-G0-HPc-EFB}$	0.24	0.47	0.90	ns	1, 4, 7, 9
GPOUT0 to CMOS HPOUT skew, without external feedback	$t_{OO-G0-HPc}$	-0.87	1.10	3.12	ns	1, 4, 6, 9
Output-to-Output Skew Variation[1, 5]						1, 5
Synthx HPOUTa to Synthx HPOUTb skew variation	t_{OODV-S}		0.03	0.08	ns	1, 3, 5
Synth1 HPOUT to Synth2 HPOUT skew variation	$t_{OODV-S1-S2}$		0.04	0.09	ns	1, 3, 5
Diff HPOUT to CMOS HPOUT skew variation	$t_{OODV-HPd-HPc}$		0.43	0.55	ns	1, 5, 6, 8, 9
GPOUT0 to GPOUT1 skew variation	$t_{OODV-G0-G1}$		0.02	0.03	ns	1, 2, 5
GPOUT0 to diff HPOUT skew variation, external feedback for DPLL0-Synth0 path	$t_{OODV-G0-HPd-EFB}$		0.43	0.59	ns	1, 5, 7, 8
GPOUT0 to diff HPOUT skew variation, without external feedback	$t_{OODV-G0-HPd}$		1.03	1.43	ns	1, 5, 6, 8
GPOUT0 to CMOS HPOUT skew variation, external feedback for DPLL0-Synth0 path	$t_{OODV-G0-HPc-EFB}$		0.30	0.53	ns	1, 5, 7, 9
GPOUT0 to CMOS HPOUT skew variation, without external feedback	$t_{OODV-G0-HPc}$		0.59	1.02	ns	1, 5, 6, 9
Initial Input-to-Output Delay[1, 4]						1, 4
CMOS input to CMOS HPOUT delay	$t_{D-REF-HPc}$	0.07	0.22	0.37	ns	1, 4, 9
CMOS input to diff HPOUT delay	$t_{D-REF-HPd}$	-1.46	-0.88	-0.46	ns	1,4, 8
CMOS input to GPOUT0 delay, external feedback for DPLL0-Synth0 path	$t_{D-REF-G0}$	-0.69	-0.25	0.01	ns	1, 4, 7
CMOS input to GPOUT0 delay, without external feedback	$t_{D-REF-G0}$	-2.87	-0.88	1.10	ns	1, 4, 6
Input-to-Output Delay Variation[1, 5]						1, 5
CMOS input to CMOS HPOUT delay variation	$t_{IODV-HPc}$		0.06	0.12	ns	1, 5, 9
CMOS input to diff HPOUT delay variation	$t_{IODV-HPd}$		0.49	0.63	ns	1, 5, 8
CMOS input to GPOUT0 delay variation, external feedback for DPLL0-Synth0 path	$t_{IODV-G0-EFB}$		0.33	0.53	ns	1, 5, 7
CMOS input to GPOUT0 delay variation, without external feedback	$t_{IODV-G0}$		0.53	0.96	ns	1, 5, 6

Note 1: All specs in this table tested with Synth0 following DPLL0, Synth1 following DPLL1 and and Synth2 following DPLL2, 25MHz I/O frequencies, 3.3V CMOS input reference signals, and CMOS outputs set to 2x drive strength.

Note 2: Only applies for outputs that have the same load/termination.

Note 3: Only applies for outputs that have the same signal format, VDDO voltage. drive strength and loading/termination and that are already enabled when the Synth is enabled. Also, this spec doesn't apply to HPOUTxN when an output pair is 2xCMOS with different frequencies on HPOUTxP and HPOUTxN; in this configuration HPOUTxN lags HPOUTxP by up to 1ns.

Note 4: Initial delay and skew numbers indicate the timing relationships among the signals just after the device has been configured. Measurement is done at the same temperature and voltage used for configuration. Measured at -40°C, 25°C and 85°C and min, nominal and max VDD (all supplies varied at the same time).

Note 5: Delay variation numbers indicate how the timing relationships among the signals change as the already-configured device is exposed to all combinations of min, nominal, and max VDD (all supplies varied at the same time) and -40°C, 25°C and 85°C temperature without resetting or reconfiguring the device.

Note 6: External feedback not enabled for DPLL0 driving Synth0.

Note 7: DPLL0 has external feedback enabled with GPOUT1 wired to REF0P as the external feedback path. GPOUT1 4x drive strength.

Note 8: Tested with HPOUT programmable differential format with 1.23V V_{CM} and 800mV V_{OD}.

Note 9: Tested with HPOUT 2xCMOS with 2x drive strength and VDDOx=3.3V.

Table 17 - Electrical Characteristics: GPOUT Output Timing

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Frequency for GPOUT outputs	$f_{OUT-GPOUT}$			180	MHz	
Duty cycle for GPOUT outputs	t_{PWL}, t_{PWH}	40	50	60	%	Note 1
Rise time for GPOUT outputs (drive 4X)	t_r	800	1500	2500	ps	
Fall time for GPOUT outputs (drive 4X)	t_f	500	700	1700	ps	

Note 1: Tested at 125MHz and 180MHz.

Table 18 - Electrical Characteristics: GPIO[8:5] Clock Output Timing

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Clock output on GPIO pin, frequency	f_{OUT}			50	MHz	Note 1
Clock output on GPIO pin, rise/fall time	t_R, t_F		1.2		ns	Notes 1, 2

Note 1: To output a clock on a GPIO pin, an HPOUTx output must be configured with NEGLSD=1 and SRLSEN=1 and the GPIO must be configured as a status output following that output's LSCLK bit. Output jitter is not guaranteed for clock signals on GPIO pins but is typically 1 to 5ps rms 12kHz to 20MHz.

Note 2: 20%-80%, 15pF load.

Table 19 - Electrical Characteristics: SPI Slave Interface Timing

Characteristics (Notes 1 to 3)	Symbol	Min.	Typ.	Max.	Units	Notes
SCLK frequency				12.5	MHz	See Figure 31 and Figure 32
SCLK period	tcyc	80			ns	
SCLK high time	tclkh	40			ns	
SCLK low time	tclkl	40			ns	
SI setup time to SCLK rising edge	trxs	8			ns	
SI hold time from SCLK rising edge	trxh	8			ns	
SO data valid time from SCLK falling edge	txd			25	ns	
CS_B rise to output high impedance	tohz			60	ns	
CS_B setup to SCLK falling edge (LSB first)	tcssi	16			ns	See Figure 31
CS_B hold from SCLK falling edge (LSB first)	tcshi	8			ns	
CS_B setup to SCLK falling edge (MSB first)	tcssm	16			ns	See Figure 32
CS_B hold from SCLK falling edge (MSB first)	tcshm	8			ns	

* Values are over Recommended Operating Conditions

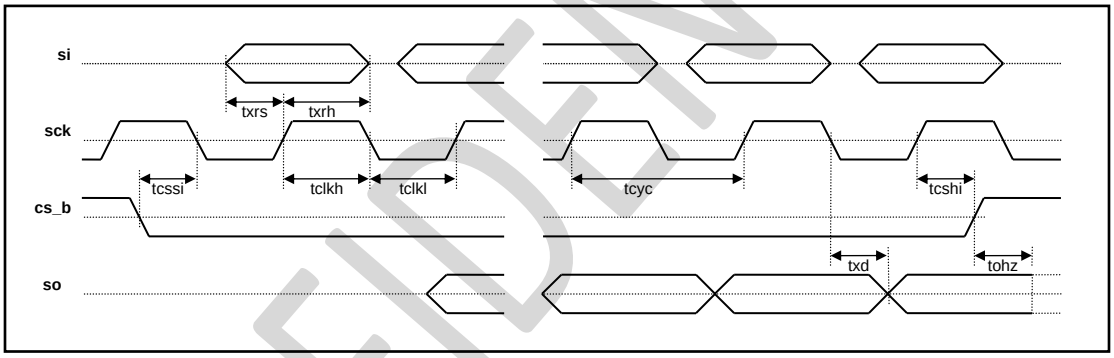


Figure 31 - SPI Slave Interface Timing, LSB First Mode

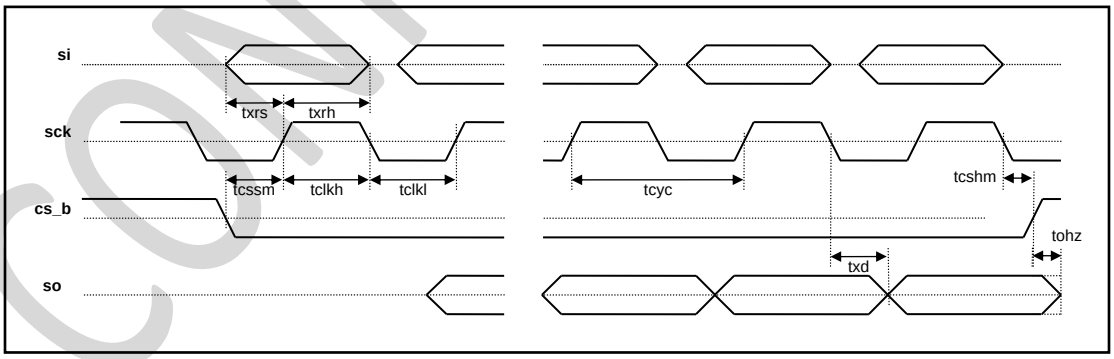


Figure 32 - SPI Slave Interface Timing, MSB First Mode

Table 20 - Electrical Characteristics: I²C Slave Interface Timing

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
SCL clock frequency	f_{SCL}			400	kHz	Note 1
Hold time, START condition	$t_{HD:STA}$	0.6			µs	
Low time, SCL	t_{LOW}	1.3			µs	
High time, SCL	t_{HIGH}	0.6			µs	
Setup time, START condition	$t_{SU:STA}$	0.6			µs	
Data hold time	$t_{HD:DAT}$	0		0.9	µs	Notes 2 and 3
Data setup time	$t_{SU:DAT}$	100			ns	
Rise time	t_R				ns	Note 4
Fall time	t_F	$20 + 0.1C_b$		300	ns	C_b is cap. of one bus line
Setup time, STOP condition	$t_{SU:STO}$	0.6			µs	
Bus free time between STOP/START	t_{BUF}	1.3			µs	
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0		50	ns	
Pin capacitance, SCL, SDA				10	pF	

Note 1: The timing parameters in this table are specifically for 400kbps Fast Mode. Fast Mode devices are downward-compatible with 100kbps Standard Mode I²C bus timing. All parameters in this table are guaranteed by design or characterization. All values referred to V_{IHmin} and V_{ILmax} levels (see Table 7).

Note 2: The device internally provides a hold time of at least 300ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL. Other devices must provide this hold time as well per the I²C specification.

Note 3: The I²C specification indicates that the maximum $t_{HD:DAT}$ spec only has to be met if the device does not stretch the low period (t_{LOW}) of the SCL signal. The device does not stretch the low period of the SCL signal.

Note 4: Determined by choice of pull-up resistor.

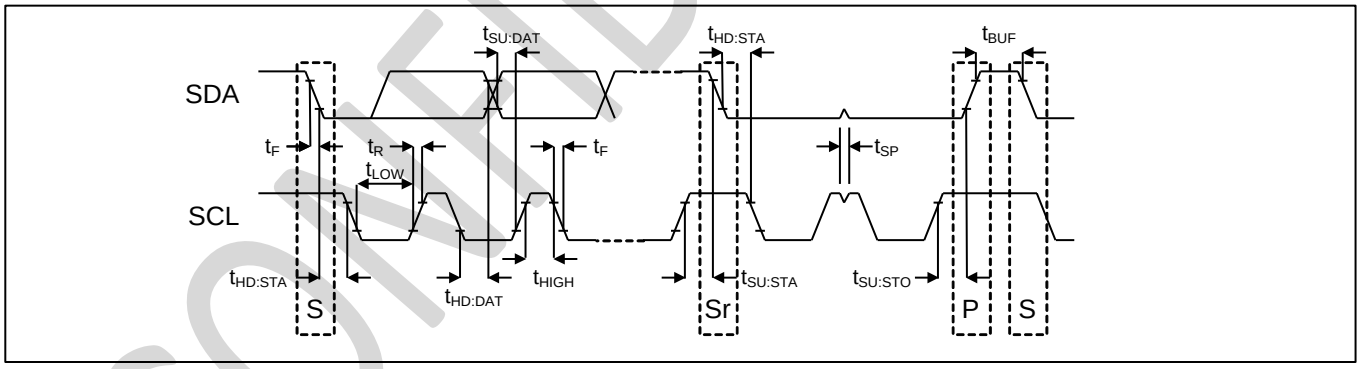


Figure 33 - I²C Slave Interface Timing

11. Performance Characteristics

Table 21 - DPLL Performance Characteristics

Characteristics	Min.	Typ.	Max.	Units	Notes
Pull-in/Hold-in Range	0.1	12	2100	ppm	user programmable
Lock Time (Bandwidth > 10Hz)		1.6	2	sec	unlimited phase slope limit 10us/1s lock selection +/-200ppm pull-in/hold range
Reference Switching MTIE		0.6		ns	bandwidth = 14Hz jitter free input (1ps rms)
Entry into Holdover MTIE		0.6		ns	
Exit from Holdover MTIE		0.6		ns	
Initial Holdover Accuracy (Bandwidth > 10Hz)		2	10	ppb	
Damping Factor	1	5	50		user programmable
Phase gain in the pass band			0.25	dB	damping factor set to 5

Table 22 - Output Clock Jitter Generation – HPOUT Differential, Synth Integer Divider

Characteristics	Test Conditions	Min	Typ	Max	Units
Phase Jitter, 156.25MHz, HP-Synth in FDIV feedback configuration	HP-Synth1, 10kHz to 1MHz, Note 2, 3, 4		0.172		ps RMS
	HP-Synth1, 12kHz to 20MHz, Note 2, 3, 4		0.236		ps RMS
	HP-Synth2, 10kHz to 1MHz, Note 2, 3, 4		0.178		ps RMS
	HP-Synth2, 12kHz to 20MHz, Note 2, 3, 4		0.247		ps RMS
Phase Jitter, 156.25MHz (49.152M XO) HP-Synth in FDIV feedback configuration	10kHz to 1MHz, Note 2a, 3, 4		0.215		ps RMS
	12kHz to 20MHz, Note 2a, 3, 4		0.268		ps RMS
Phase Jitter, 156.25MHz (114.285M XO)	HP-Synth1, 10kHz to 1MHz, Note 2, 3		0.230		ps RMS
	HP-Synth1, 12kHz to 20MHz, Note 2, 3		0.285		ps RMS
	HP-Synth2, 10kHz to 1MHz, Note 2, 3		0.236		ps RMS
	HP-Synth2, 12kHz to 20MHz, Note 2, 3		0.293		ps RMS
Phase Jitter, 156.25MHz (49.152M XO)	10kHz to 1MHz, Note 2a, 3		0.255		ps RMS
	12kHz to 20MHz, Note 2a, 3		0.310		ps RMS

Note 1: Jitter calculated from integrated phase noise from 12kHz to 20MHz.

Note 2: With Vectron VCC1-1537-114M285 XO connected to OSCI pin, 3750MHz VCO frequency, DPLL locked to 19.44MHz REF.

Note 2a: With Vectron VCC1-1545-49M152 XO connected to OSCI pin, XO doubler enabled, 3750MHz VCO frequency, DPLL locked to 19.44MHz REF.

Note 3: With IntDiv=6 and MSDIV=4.

Note 4: HP-Synth configured to have its fractional output divider used as its feedback divider and HP-Synth input doubler enabled. See section 6.5.6 for details and limitations of this configuration.

Table 23 - Typical Output Clock Jitter Generation – HPOUT Differential

Output Frequency	Output Jitter, ps RMS 114.285MHz XO[1]	Output Jitter, ps RMS 114.285MHz XO[2]	Output Jitter, ps RMS 49.152MHz XO[3]	Output Jitter, ps RMS 49.152MHz XO[4]
625MHz	0.188	0.263	0.230	0.282
156.25MHz	0.230	0.285	0.267	0.300
125MHz	0.230	0.310	0.290	0.321
622.08MHz	0.198	0.253	0.273	0.290
625MHz * 66/64	0.196	0.270	0.238	0.291
156.25MHz * 66/64	0.234	0.281	0.271	0.300
614.4MHz	0.198	0.281	0.232	0.302
153.6MHz	0.237	0.303	0.270	0.321

Note 1: HP-Synth locked to Vectron VCC1-1537-114M285, HP-Synth configured to have its fractional output divider used as its feedback divider and HP-Synth input doubler enabled. See section 6.5.6 for details and limitations of this configuration. Numbers shown are HP-Synth1. HP-Synth2 is approximately 10fs higher.

Note 2: HP-Synth locked to Vectron VCC1-1537-114M285.

Note 3: HP-Synth locked to Vectron VCC1-1545-49M152, 114M285, internal doubler enabled. HP-Synth configured to have its fractional output divider used as its feedback divide. See section 6.5.6 for details and limitations of this configuration. Numbers shown are HP-Synth1. HP-Synth2 is approximately 10fs higher.

Note 4: HP-Synth locked to Vectron VCC1-9003-48M000, internal doubler enabled.

Note 5: All signals are differential unless otherwise stated. Jitter is integrated 12kHz to 5MHz for 25MHz output frequency and 12kHz to 20MHz for all other output frequencies.

Table 24 - Output Clock Jitter Generation – HPOUT Differential, Synth Fractional Divider

Characteristics	Test Conditions	Min	Typ	Max	Units
Phase Jitter, 156.25MHz, Integer Divisor	10kHz to 1MHz, Note 1		0.24	0.31	ps RMS
	12kHz to 20MHz, Note 1		0.32	0.42	ps RMS
Phase Jitter, 156.25MHz, Fractional Divisor	10kHz to 1MHz, Note 2		0.25	0.31	ps RMS
	12kHz to 20MHz, Note 2		0.33	0.44	ps RMS
Period Jitter, 100MHz	Note 3		9-20	27	ps pk-pk
Cycle-to-Cycle Jitter, 100MHz	Note 3		8-18	26	ps

Note 1: With Vectron VCC1-1537-114M285 XO connected to OSCI pin, DPLL locked to 19.44MHz REF, 3750MHz VCO frequency, FracDiv=6.0 and MSDIV=2.

Note 2: With Vectron VCC1-1537-114M285 XO connected to OSCI pin, DPLL locked to 19.44MHz REF, 3993.6MHz VCO frequency and MSDIV=2.

Note 3: Measured using Tektronix MSO71604C, Mixed Signal Oscilloscope with DPOJET software. Measured with 3750MHz VCO frequency, 200MHz out of the fractional divider, and 100MHz out of the medium-speed divider. N=10000.

Table 25 - Output Clock Jitter Generation – GPOUT CMOS

Characteristics	Test Conditions	Min	Typ	Max	Units
Phase Jitter, 125MHz	12kHz to 20MHz, Note 1		17.4	31.5	ps RMS
Phase Jitter, 25MHz	12kHz to 5MHz, Note 1		14.5	27.4	ps RMS
Phase Jitter, 125MHz	12kHz to 20MHz, Note 2		54		ps RMS
Phase Jitter, 25MHz	12kHz to 5MHz, Note 2		48		ps RMS

Note 1: GPOUT output drive levels are set to 4x, DPLL locked to 19.44MHz REF, Vectron VCC1-1537-114M285 XO connected to OSCI and MCLKIN_P pins.

Note 2: GPOUT output drive levels are set to 4x, DPLL locked to 19.44MHz REF, Vectron VCC1-1545-49M152 connected to OSCI and MCLKIN_P pins.

12. Package and Thermal Information

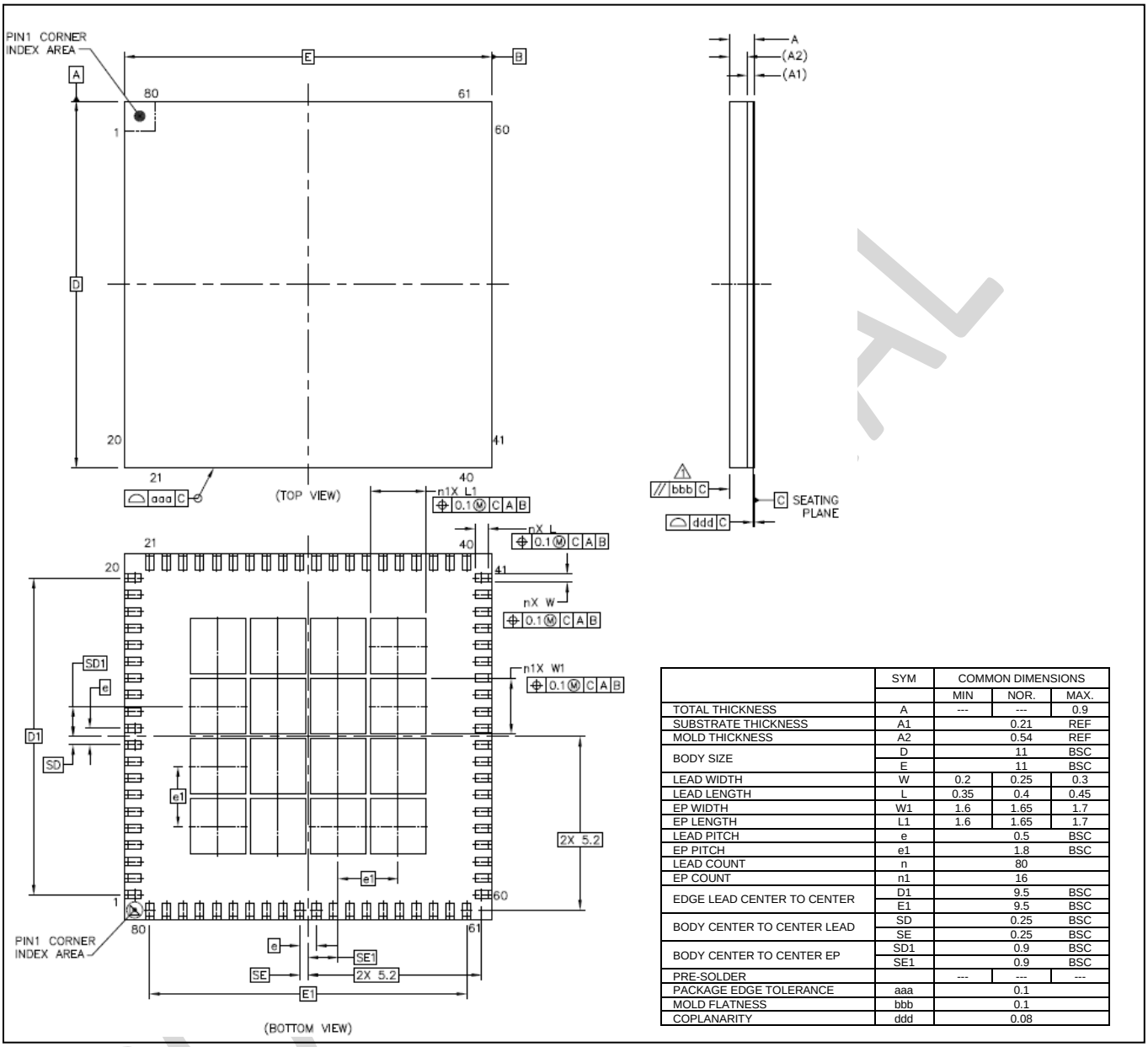
Table 26 - 11x11mm LGA Package Thermal Properties

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Maximum Ambient Temperature	T_A		85	°C
Maximum Junction Temperature	T_{JMAX}		125	°C
Junction to Ambient Thermal Resistance (Note 1)	θ_{JA}	still air	12.92	°C/W
		1m/s airflow	10.95	
		2.5m/s airflow	10.32	
Junction to Board Thermal Resistance	θ_{JB}		3.8	°C/W
Junction to Case Thermal Resistance	θ_{JC}		4.5	°C/W
Junction to Pad Thermal Resistance (Note 2)	θ_{JP}	Still air	1.4	°C/W
Junction to Top-Center Thermal Characterization Parameter	Ψ_{JT}	Still air	1.35	°C/W
	Ψ_{JT}	1m/s airflow	1.41	°C/W
	Ψ_{JT}	2.5m/s airflow	1.47	°C/W

Note 1: Theta-JA (θ_{JA}) is the thermal resistance from junction to ambient when the package is mounted on an 8-layer JEDEC standard test board and dissipating maximum power.

Note 2: Theta-JP (θ_{JP}) is the thermal resistance from junction to the center exposed pad on the bottom of the package.

13. Package Outline Drawing



	SYM	COMMON DIMENSIONS		
		MIN	NOR.	MAX.
TOTAL THICKNESS	A	---	---	0.9
SUBSTRATE THICKNESS	A1		0.21	REF
MOLD THICKNESS	A2		0.54	REF
BODY SIZE	D		11	BSC
	E		11	BSC
LEAD WIDTH	W	0.2	0.25	0.3
LEAD LENGTH	L	0.35	0.4	0.45
EP WIDTH	W1	1.6	1.65	1.7
EP LENGTH	L1	1.6	1.65	1.7
LEAD PITCH	e		0.5	BSC
EP PITCH	e1		1.8	BSC
LEAD COUNT	n		80	
EP COUNT	n1		16	
EDGE LEAD CENTER TO CENTER	D1		9.5	BSC
	E1		9.5	BSC
BODY CENTER TO CENTER LEAD	SD		0.25	BSC
	SE		0.25	BSC
BODY CENTER TO CENTER EP	SD1		0.9	BSC
	SE1		0.9	BSC
PRE-SOLDER		---	---	---
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.08	

14. Acronyms and Abbreviations

APLL	analog phase locked loop
CML	current mode logic
GbE	gigabit Ethernet
HCSL	high-speed current steering logic
HSTL	high-speed transceiver logic
I/O	input/output
LOS	loss of signal
LVDS	low-voltage differential signal
LVPECL	low-voltage positive emitter-coupled logic
PFD	phase/frequency detector
pk-pk	peak-to-peak
PLL	phase locked loop
ppb	parts per billion
ppm	parts per million
PRC	primary reference clock
PRS	primary reference source
RMS	root-mean-square
RO	read-only
R/W	read/write
TCXO	temperature-compensated crystal oscillator
UI	unit interval
UI_{PP} or UI_{P-P}	unit interval, peak to peak
XO	crystal oscillator

15. Data Sheet Revision History

Revision	Description
05-Jul-2017	First general release
19-Sep-2018	In Figure 32 changed tcshm and tohz to be w.r.t. sclk fall edge rather than rising edge. In dpll_df_offset_0 description, added Note 4. In dpll_df_ctrl_0::cmd description clarified the difference between holdover 0xx and 101 decodes. In ref_freq_0P added FFO calculation and added words to define "error". Documented srlsen bit in hp_out_lsctrl_1 to hp_out_lsctrl_7 registers. In pherr_low_freq_ctrl, corrected the avg_time equation. At the end of the Register Map Page 14 table, documented that 0x0730-0x074F are available for customer use. In section 6.3.14 and dpll_df_offset_0 clarified that GP-Synth frequency range is only ±0.4%. In section 6.4.1.1 added Note paragraph about output alignment for NCO mode. Documented gpio_at_startup registers at 0x0019 and 0x001A.
24-Jan-2019	Documented dpll_mon_status_4 and _5, dpll_mon_tl_sticky_4 and _5, dpll_mon_th_sticky_4 and _5, dpll_mon_tl_mask_4 and _5, and dpll_mon_th_mask_4 and _5. In ref_pfm_ctrl::resolution description, documented when 0.005ppm resolution is not available. In section 6.6.3 added a new last paragraph about alignment of outputs internally connected to a synthesizer fractional output divider. In section 6.1.5 added note 3 to indicate that low-frequency input-vs-input phase measurement is not affected by the value of the ref_phase_offset_compensation mailbox register and note 4

Revision	Description
	about delay differences for the three input signal format configurations. In pherr_low_freq_ctrl::avg_time and pherr_meas_ctrl::avg_time descriptions added notes about phase-step tolerance. Documented DPLL4 and DPLL5 bits in dpll_irq_active. In section 6.5.6 third paragraph added a sentence to say that Synth1 cannot be internally connected to DPLL0 when FDIV feedback is enabled for Synth2.
20-Nov-2019	In dpll_psl register description, added guideline for when fast-lock is disabled. In dpll_mon_status_0::ho_ready add a list of conditions where the device clears the bit. In the ref_phase_offset_compensation register description, clarified behavior when a DPLL has hitless switching enabled. Documented in dpll_fp_first_realign that time=1 is invalid. In hp_out_lsctrl_0::neglsd description changed "is set to 0100 or 0111 (two-CMOS mode)" to "is set to a CMOS mode". Documented dpll_fast_lock_ctrl::fcl_en. Added section 7.5.
28-Apr-2020	In gp_out_en::en_1 add note. Deleted hp_stopall_ctrl register description and references. Changed GPSynth minimum VCO frequency from 750MHz to 730MHz. In dpll_fp_lock_thresh corrected LSB from 10ns to 20ns. In section 7.4 and info register, indicated the need to wait 1.1s after power-up or reset before configuring device registers. Annotate register descriptions to indicate these registers are ignored: 0x63C-0x63E for DPLL3-DPLL5. 0x610, 0x614-0x618, 0x639 for DPLL4-DPLL5. 0x21D::ignore_sync for DPLL3. In ref_freq_base description added text that it must be integer divide of 500MHz. In gp_out_width_0, added guidance for aligning GPOUTs with frequency < 250Hz and non-50% duty cycle.
09-Oct-2020	In hp_out_lsdiv_0 documented that LSDIV values should be in the range 4M-25M for 1Hz or 0.5Hz outputs that participate in step-time or phase-step. In ref_pfm_period documented that the field is ignored and the period internally set to 10s for the sync input of a ref-sync pair. Removed all mention of spread spectrum. In Table 1 changed the RST_B pin description to say device registers can be accessed 1.1s after power-up or reset. Updated info::ready description. In custom_config_ver register description, clarified the register is for customer use and ignored by the device. In Table 10 changed V_{OD} max to 0.95V and changed V_{CM} to V_{OD} / 2. Changed dpll_psl description to say the valid range is 400ns/s to 65535ns/s. Documented the fw_ver register.

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