ZL38063 Preliminary Data Sheet
Microphone Array ASR-assist Audio Processor

Description

The ZL38063 is part of Microsemi's Timberwolf audio processor family of products that improves Automatic Speech Recognition (ASR) performance at extended distances with barge-in capability and is optimized for detecting voice commands.

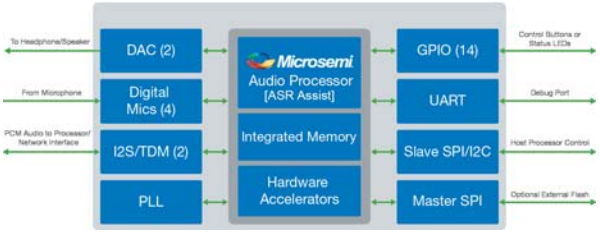
The Microsemi *AcuEdge*™ Technology ZL38063 device is specifically designed for televisions, set-top boxes, and smart speakers, but works equally well in other connected home applications. The device is capable of both voice control and 2-way full duplex audio with voice enhancements such as Acoustic Echo Cancellation (AEC), Noise Reduction (NR) to improve both the intelligibility and subjective quality of voice in harsh acoustic environments.

Microsemi offers additional tools to speed up the product development cycle. The *MiTuner*™ ZLS38508 or ZLS38508LITE GUI software packages allow a user to interactively configure the ZL38063 device. The optional ZLE38470BADA Automatic Tuning Kit provides automatic tuning and easy control for manual fine tuning adjustments.

Applications

- Integrated smart home gateways
- Connected home devices:
  - Set Top Boxes
  - Smart Speakers
  - Digital Assistants

Block Diagram



Ordering Information

- ZL38063LDF1: 64-pin QFN (9×9) package (Tape and Reel)
- ZL38063LDG1: 64-pin QFN (9×9) package (Tray)
- ZL38063UGB2: 56-ball WLCSP (3.1×3.1) package (Tape and Reel)

Note: These packages meet RoHS 2 Directive 2011/65/EU of the European Council to minimize the environmental impact of electrical equipment.

Microsemi *AcuEdge*™ Technology ZL38063 Firmware

The ZL38063 can run different Firmware images that target specific modes of operation. Firmware images can be swapped during normal operation to switch modes dynamically. Microsemi provides firmware images for two basic operational modes:

Two way voice communication

- Supports 2–3 microphone linear arrays for 180° audio pick up
- Supports 3 microphone off-axis or triangular arrays for 360° audio pick up
- Supports device cascading to allow up to a 6 microphones array
- Full Narrowband and Wideband Acoustic Echo Cancellation (AEC) operation
  - Supports long tail AEC (up to 256 ms)
  - Non-Linear AEC provides higher tolerance for speaker distortions
  - Non-Linear processor
- Noise reduction
- Far-field microphone processing

ASR Assist Algorithms

- Supports 2 microphone linear arrays for 180° audio pick up
- Supports 3 microphone off-axis or triangular arrays for 360° audio pick up
- Supports device cascading to allow up to 6 microphones in a circular array for 360° audio pick up
- Support for Barge-in, or incoming trigger 'spotting' in the presence of DAC audio output
- Noise reduction
- Enhanced far-field support for distances up to 16 feet from the microphone

Hardware Features

- DSP with Voice Hardware Accelerators
- SPI or I^2C Slave port for host processor interface
- General purpose UART port for debug
- Master SPI port for serial Flash interface
- Boots from SPI or Flash
  - Flash firmware can be updated from SPI Slave
- 14 General Purpose Input/Output (GPIO) pins (11 with the 56 pin WLCSP)
- 2 low power modes controlled by reset

The *MiTuner*™ Automatic Tuning Kit and ZLS38508 MiTuner GUI

Microsemi's Automatic Tuning Kit option includes:

- Audio Interface Box hardware
- Microphone and Speaker
- ZLS38508 *MiTuner* GUI software
  - Allows tuning of Microsemi's *AcuEdge* Technology Audio Processor

The ZLS38508 software features:

- Auto Tuning and Subjective Tuning support
- Provides visual representations of the audio paths with drop-down menus to program parameters, allowing:
  - Control of the audio routing configuration
  - Programming of key blocks in the transmit (Tx) and receive (Rx) audio paths
  - Setting analog and digital gains
- Configuration parameters allow users to “fine tune” the overall performance

Tools

- ZLK38000 Evaluation Kit
- *MiTuner*™ ZLS38508 and ZLS38508LITE GUI
- *MiTuner*™ ZLE38470BADA Automatic Tuning Kit

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Microphone Array ASR-assist Audio Processor

Microsemi
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Contents

Figures

Tables

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 4.0

The following is a summary of the changes in revision 4 of this document.

- Removed references to non-Microsemi ASR engine
- Minor text corrections
- Headers applied to aid in document navigation

1.2 Revision 3.0

The following is a summary of the changes in revision 3 of this document.

- Migration to new document format; no other changes to technical details or content besides those listed here
- Updated verbiage on front page to better delineate and describe the firmware modes
- Removed references to specific firmware OPNs
- Removed analog microphone reference
- Added current consumption typical values
- Added information regarding master/slave operation for up to 6 microphones
- Removed references to embedded ASR engine. Firmware variants may be available with the embedded ASR engine, but are not available at the time of this publication

2 Overview

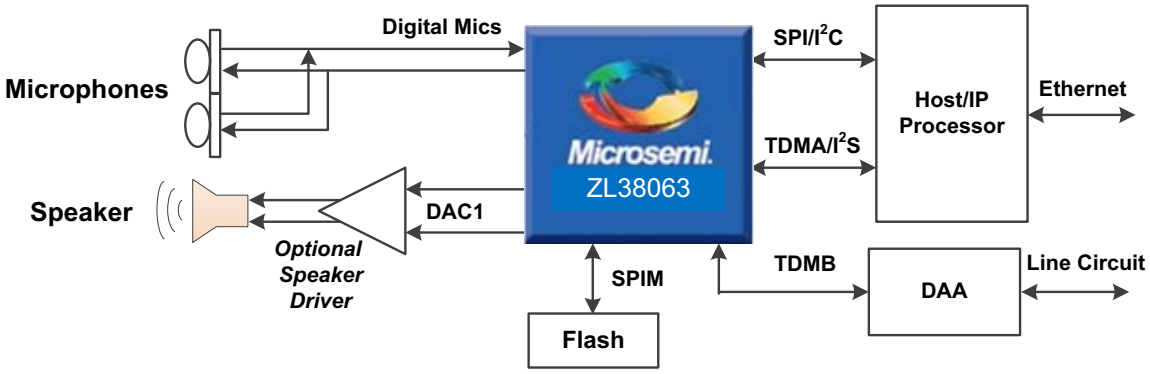
2.1 Introduction

The ZL38063 has two primary modes of operation: Automatic Speech Recognition Assist and Two Way Voice Communications mode.

The ZL38063 integrates Microsemi's patented *AcuEdge™* Technology to improve audio for both two way person to person and person to machine communication by canceling acoustic echo, reducing noise and improving audio pickup at far field distance using various techniques.

Refer to the *Microsemi AcuEdge™ Technology ZLS38063 Firmware Manual* for further details.

Figure 1 • **Set Top Box Application**

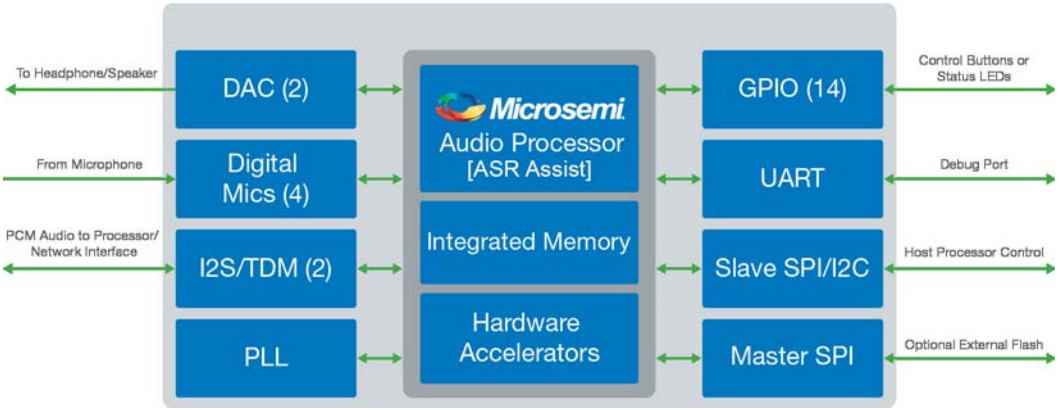


For the Two Way Voice Communications Firmware, the signal processing (AEC, Equalization, Noise Reduction etc.) runs in the Audio Processor Block. Each of the audio inputs (Digital Mics, I^2S/TDM) and outputs (DACs, I^2S/TDM) can be routed amongst themselves or to the Audio Processor via a highly configurable Cross Point Switch.

The main functional blocks of the Two Way Voice Communications Firmware are shown in Figure 2, a description of each block follows.

Refer to the *Microsemi AcuEdge™ Technology ZLS38063 Firmware Manual* for functional blocks of the Automatic Speech Recognition variants.

Figure 2 • **ZL38063 ASR Audio Processor shown with Two Way Voice Communication Firmware**



3 Firmware

The mode of operation in the ZL38063 is selected depending on which Firmware is loaded into the device. The Firmware is initially loaded at power up, either from external serial Flash or from a host controller (see Device Booting and Firmware Swapping, page 22). Real time switching between two Firmware modes can be done during normal operation. There are timing constraints that should be noted for Firmware swapping (see Host Bus Interface Timing Parameters, page 45 for more information).

Refer to the *Microsemi AcuEdge™ Technology ZLS38063 Firmware Manual* for detailed information on the use of the firmware options.

The signal processing (which includes Acoustic Echo Cancellation, Equalization, Noise Reduction, Far-Field Mic) runs in the Audio Processor Block at 16 kHz. Each of the audio inputs (Digital Mics, I^2S/TDM) and outputs (DACs, I^2S/TDM) can be routed amongst themselves or to the Audio Processor via a highly configurable Cross Point Switch.

The ZL38063 device provides the following peripheral interfaces:

- 2 Digital Microphone inputs (supporting up to 4 microphones)
- 2 Time-Division Multiplexing (TDM) buses
  - The ports can be configured for Inter-IC Sound (I^2S) or Pulse-Code Modulation (PCM) operation
  - PCM operation supports PCM and GCI timing, I^2S operation supports I^2S and left justified timing
  - Each port can be a clock master or a slave
  - Each port supports up to four bi-directional streams when configured in PCM mode or two bi-directional streams when configured for I^2S mode at data rates from 128 kb/s to 8 Mb/s
  - Sample rate conversions are automatically done when data is sent/received at different rates than is processed internally. Only integer conversions are allowed.
- SPI – The device provides two Serial Peripheral Interface (SPI) ports
  - The SPI Slave port is recommended as the main communication port with a host processor. The port provides the fastest means to Host Boot and configures the device's firmware and configuration record[1].
  - The Master SPI port is used to load the device's firmware and configuration record from external Flash memory (Auto Boot).
- I^2C - The device provides one Inter-Integrated Circuit (I^2C) port. (Pins are shared with the SPI Slave port)
  - The I^2C port can be used as the main communication port with a host processor, and can be used to Host Boot and configure the device's firmware and configuration record.
- UART – The device provides one Universal Asynchronous Receiver/Transmitter (UART) port
  - The UART port can be used as a debug tool and is used for tuning purposes.
- GPIO – The device provides 14 General Purpose Input/Output (GPIO) ports (full operation with Two Way Communication Firmware, limited operation with ASR Firmware).
  - GPIO ports can be used for interrupt and event reporting, fixed function control, bootstrap options, as well as being used for general purpose I/O for communication and controlling external devices.
  - The 56 pin WLCSP package is limited to 11 GPIOs.

1. The configuration record is a set of register values that are customizable by the application developer to configure and tune the ZL38063 for a particular design. Refer to the Microsemi AcuEdge™ Technology ZLS38063 Firmware Manual for firmware and configuration record information

4 Audio Interfaces

4.1 Digital Microphone Interface

This firmware supports up to four digital microphones using the DMIC_CLK, DMIC_IN1, and DMIC_IN2 interface pins.

The ZL38063 digital microphone clock output (DMIC_CLK) is either 1.024 MHz or 3.072 MHz depending on the selected TDM-A sample rate. Selecting an 8 kHz or 16 kHz TDM-A sample rate corresponds to a 1.024 MHz digital microphone clock and selecting a 48 kHz sample rate corresponds to a 3.072 MHz digital microphone clock. Microphone data is decimated and filtered to operate at the 8 kHz or 16 kHz sampling rate of the Audio Processing block. When there is no TDM-A bus to set the sample rate, the ZL38063 will operate from the crystal (or clock oscillator) and will pass digital audio from the microphones operating at a 48 kHz sampling rate.

The ZL38063 supports both linear and triangular/circular microphone arrays. Two microphone channels are multiplexed on each of the DMIC pins by sending the data for one channel on the rising edge and one channel on the falling edge. This allows for up to four microphones on the two DMIC_IN pins of the ZL38063. Various digital microphone topologies are presented in Figure 3 and Figure 4.

Two ZL38063's may be chained together to support up to six digital microphones in an array. Three microphones are supported on each ZL38063. The master ZL38063 processes the audio streams from both devices.

Figure 3 • **Dual Microphone or Stereo Digital Microphone Interface**

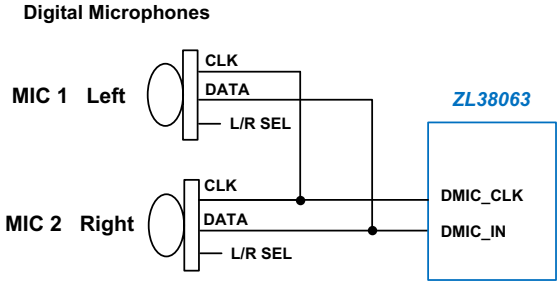
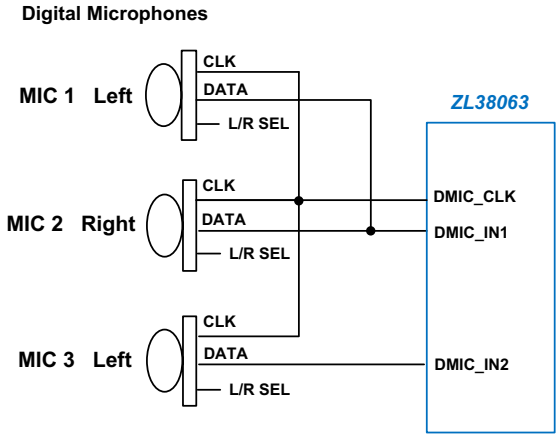


Figure 4 • **Three Digital Microphones**



4.2 DAC Output

The Two Way Voice Communication Mode supports two 16-bit fully differential delta-sigma digital-to-analog converters. The two output DACs can drive 2 outputs either single ended or differentially. Four analog gain settings on each DAC output are provided and can be set to: 1x, 0.5x, 0.333x, or 0.25x.

Note: Only the positive DAC outputs are available with the 56-ball WLCSP package. The 56-ball WLCSP package provides two independent single-ended headphone outputs that can be driven by two independent data streams.

The headphone amplifiers are self-protecting so that a direct short from the output to ground or a direct short across the terminals does not damage the device.

The ZL38063 provides audible pop suppression which reduces pop noise in the headphone earpiece when the device is powered on/off or when the device channel configurations are changed. This is especially important when driving a headphone single-ended through an external capacitor (see Output Driver Configurations, page 54, configuration 3).

The DACs and headphone amplifiers can be powered down if they are not required for a given application. To fully power down the DACs, disable both the positive and negative outputs.

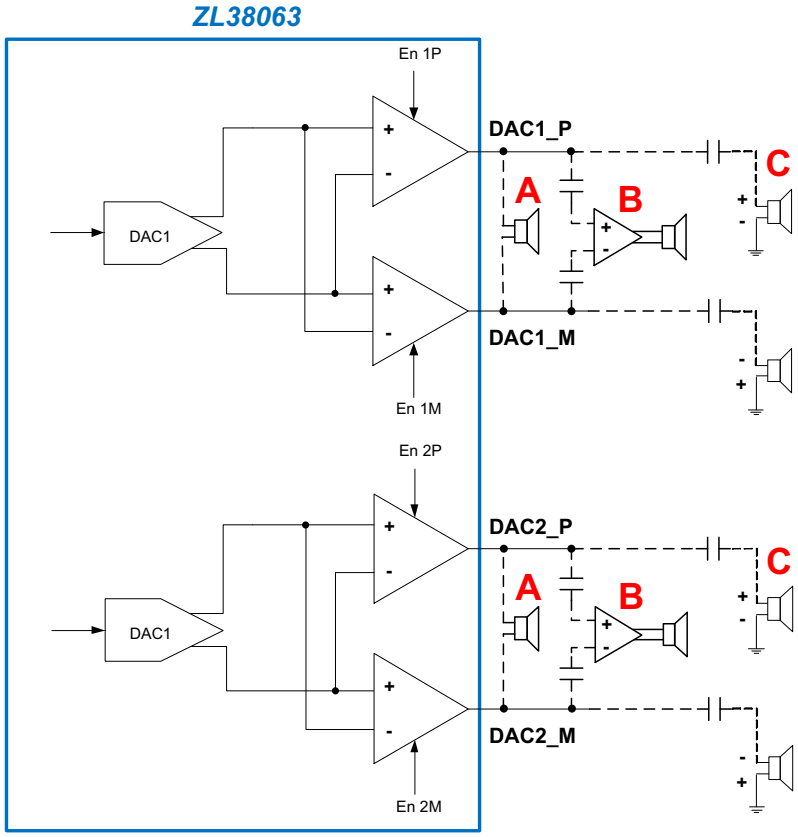
4.2.1 Output Driver Configurations

Figure 5, page 6 shows the different possible output driver configurations for the 64-pin QFN package. When using the 56- ball WLCSP package, only the positive single ended outputs DAC1_P and DAC2_P are provided.

The two output DACs independently drive positive and negative headphone driver amplifiers. The output pins can be independently configured in the following ways:

1. Direct differential drive of a speaker as low as 32 ohms. For this configuration an analog gain of 1x is commonly used. (Differentially driving a 16 ohm speaker is possible, but only with the same amount of power as in the single-ended case. The signal level must be reduced to not exceed ½ scale in this case.)
2. Direct differential drive of a high impedance power amplifier. A Class D amplifier is recommended for this speaker driver. A 1 µF coupling capacitor is generally used with the Class D amplifier. The analog gain setting depends on the gain of the Class D amplifier, analog gain settings of 0.25x or 0.5x are commonly used.
3. Driving either a high impedance or a capacitively coupled speaker as low as 16 ohms single-ended. For this configuration an analog gain of 1x is commonly used. The coupling capacitor value can vary from 10 µf to 100 µf depending on the type of earpiece used and the frequency response desired.

Figure 5 • **Audio Output Configurations**



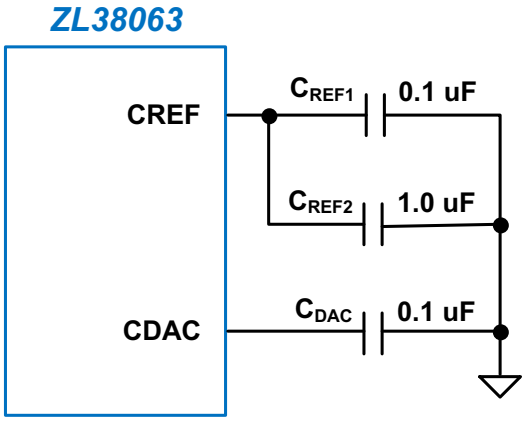
4.3 DAC and Reference Bias Circuits

The common mode bias voltage output signal (CREF) must be decoupled through a 0.1 µF (C_{REF1}) and a 1.0 µF (C_{REF2}) ceramic capacitor to VSS.

The positive DAC reference voltage output (CDAC) must be decoupled through a 0.1 µF (C_{DAC}) ceramic capacitor to VSS as shown in Figure 6 if a DAC is ever to be used. If solely using Alarm, Glass Break and Energy Detector Firmware, this capacitor is not required.

All capacitors can have a 20% tolerance and should have a minimum voltage rating of 6.3 V.

Figure 6 • **ZL38063 Bias Circuit**



5 Digital Interfaces

5.1 TDM Interface

The Two Way Voice Communications Mode supports two generic TDM interfaces, TDM-A and TDM-B. Each interface consists of four signals:

- Data clock (PCLK/I^2S_SCK)
- Data rate sync (FS/I^2S_WS)
- Serial data input (DR/I^2S_SDI)
- Serial data output (DX/I^2S_SDO)

The TDM ports can be configured for Inter-IC Sound (I^2S) or Pulse-Code Modulation (PCM) operation.

Each TDM block is capable of being a master or a slave. Operation of the TDM interfaces are subject to the following limitations.

Table 1 • **Allowable TDM Configurations - Two Way Voice Communications Firmware**

TDM-A Mode	TDM-B Mode	Supported Sample Rates (kHz)	Requirements / Limitations
Master	Master	16, 48	Both TDM-A and TDM-B must be configured for the same data clock and data sync.
Master	Slave-Synchronous	16, 48	The TDM-B sync rate must be the same as the TDM_A sync rate or 48 kHz.
	Slave-Asynchronous[1]	16, 48	
Slave	Master	16, 48	
Slave	Slave-Synchronous[2]	16, 48	
	Slave-Asynchronous[1]	16, 48	

1. When TDM-B is running in 48 kHz Slave-Asynchronous mode, the TDM-B bus is limited to 2-bidirectional audio streams (timeslots).
2. This combination requires that both TDM-A clock and TDM-B clock be physically connected to the same source

While a TDM bus configuration may carry many encoded audio streams, when using Two Way Voice Communication Firmware, the ZL38063 device can only address a maximum of 4 bi-directional audio streams per TDM bus. These four audio streams are referred to as channels #1 through #4, and each of these channels can be independently configured to decode any of the TDM bus's audio streams.

For a given TDM bus, once it is configured for a data sample rate and encoding, all data rates and encoding on that bus will be the same. 16-bit linear data will be sent on consecutive 8-bit timeslots (e.g., if timeslot N is programmed in the timeslot registers, the consecutive timeslot is N+1).

The TDM interface supports bit reversal (LSB first <- -> MSB first) and loopbacks within the TDM interface and from one interface to another (see Cross Point Switch – Two Way Voice Communication Mode, page 11).

The generic TDM interface supports the following mode and timing options.

5.1.1 I^2S Mode

In I^2S mode, the 4-wire TDM port conforms to the I^2S protocol and the port pins become I2S_SCK, I2S_WS, I2S_SDI, and I2S_SDO (refer to Table 10, page 27 for pin definitions). Both TDM buses have I^2S capability.

An I^2S bus supports two bi-directional data streams, left and right channel, by using the send and receive data pins utilizing the common clock and word signals. The send data is transmitted on the I2S_SDO line and the receive data is received on the I2S_SDI line.

The I²S port can be used to connect external analog-to-digital converters or Codecs. The port can operate in master mode where the ZL38063 is the source of the port clocks, or slave mode where the word select and serial clocks are inputs to the ZL38063.

The word select (I2S_WS) defines the I²S data rate and sets the frame period when data is transmitted for the left and right channels. A frame consists of one left and one right audio channel. When using Two Way Voice Communication Firmware, the I²S ports operate as a slave or a master at sample rates as specified in Table 1. Per the I²S standard, the word select is output using a 50% duty cycle.

The serial clock (I2S_SCK) rate sets the number of bits per word select frame period and defines the frequency of I2S_CLK. I²S data is input and output at the serial clock rate. Input data bits are received on I2S_SDI and output data bits are transmitted on I2S_SDO. Data bits are always MSB first. The number of clock and data bits per frame can be programmed as 8, 16, 32, 64, 96, 128, 192, 256, 384, 512, or 1024. Any input data bits that are received after the LSB are ignored.

The I²S port operates in two frame alignment modes (I²S and Left justified) which determine the data start in relation to the word select.

Figure 7 illustrates the I²S mode, which is left channel first with I2S_WS (Left/Right Clock signal) low, followed by the right channel with I2S_WS high. The MSB of the data is clocked out starting on the second falling edge of I2S_SCK following the I2S_WS transition and clocked in starting on the second rising edge of I2S_SCK following the I2S_WS transition. Figure 7 shows I²S operation with 32 bits per frame.

Figure 7 • **I²S Mode**

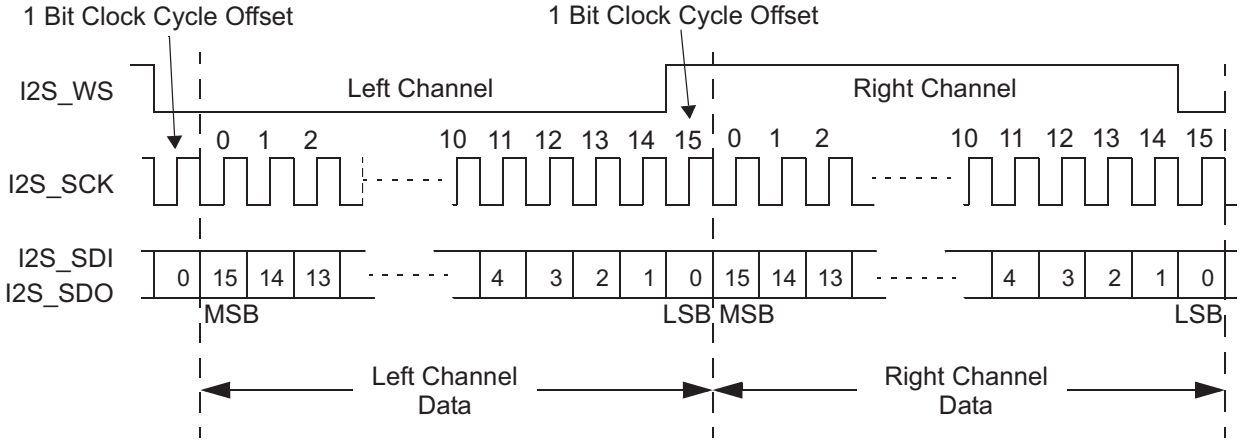
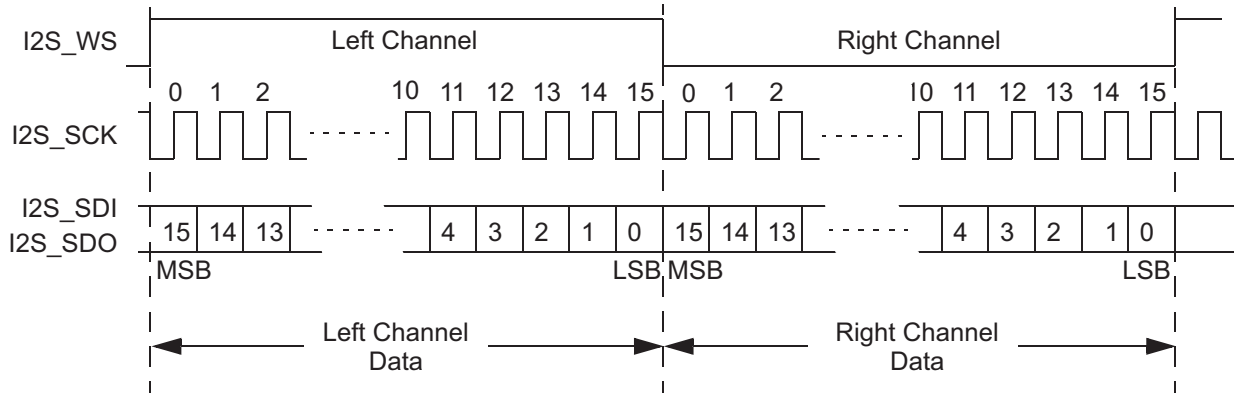


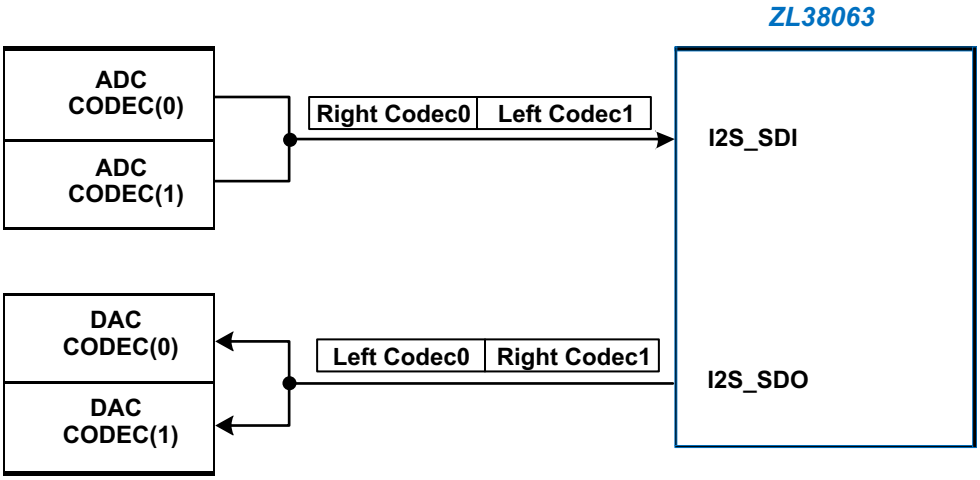
Figure 8 illustrates the left justified mode, which is left channel first associated with I2S_WS (Left/Right Clock signal) high, followed by the right channel associated with I2S_WS low. The MSB of the data is clocked out starting on the falling edge of I2S_SCK associated with the I2S_WS transition, and clocked in starting on the first rising edge of I2S_SCK following the I2S_WS transition.

Figure 8 • **Left Justified Mode**



Each I2S interface can support one dual channel Codec (Figure 9) through the Codec's I2S interface. The four 16- bit channel processing capacity of the DSP is spread across the two input channels from the ADCs of Codec(0) and Codec(1), and the two output channels to the DACs of Codec(0) and Codec(1).

Figure 9 • **Dual Codec Configuration – Two Way Voice Communications Firmware**



Both I2S bus modes can support full bi-directional stereo communication. The device supports I2S loopback.

See the *Microsemi AcuEdge™ Technology ZLS38063 Firmware Manual* for I2S port registers.

5.1.2 PCM Mode

Each of the PCM channels can be assigned an independent timeslot. The timeslots can be any 8-bit timeslot up to the maximum supported by the PCLK being used.

The PCM ports can be configured for Narrowband G.711 A-law/µ-Law or Linear PCM or Wideband G.722 encoding. For a given TDM bus, once it is configured for a data sample rate and encoding, all data rates and encoding on that bus will be the same. 16-bit linear PCM will be sent on consecutive 8-bit timeslots (e.g., if timeslot N is programmed in the timeslot registers, the consecutive timeslot is N+1). The PCM interface can transmit/receive 8-bit compressed or 16-bit linear data with 8 kHz sampling (Narrowband), or 16-bit linear data with 16 kHz sampling (Wideband). Although the firmware allows it, 44.1 and 48 kHz sampling are not commonly used with PCM.

Wideband audio usually means the TDM bus is operating at a 16 kHz FS, but there are two other operating modes that support wideband audio using an 8 kHz FS:

- G.722 supports wideband audio with an 8 kHz FS. This uses a single 8-bit timeslot on the TDM bus.
- "Half-FS Mode" supports wideband audio with an 8 kHz FS signal. In this mode, 16-bit linear audio is received on two timeslot pairs; the first at the specified timeslot (N, N+1) and the second a half-frame later. In total, four 8-bit timeslots are used per frame, timeslots (N, N+1) and ((N + ((bits_per_frame)/16)), (N + 1 + ((bits_per_frame)/16))). The user programs the first timeslot and the second grouping is generated automatically 125/2 µs from the first timeslot.

The PCM voice/data bytes can occupy any of the available timeslots, except for PCM clock rates that have extra clocks in the last timeslot. If there is more than one extra clock in the last timeslot, the timeslot data will be corrupted, do not use the last timeslot for these clock frequencies (e.g., 3.088 MHz etc.).

The PCM block can be configured as a master or a slave and is compatible with the Texas Instruments Inc. McBSP mode timing format.

Figure 10 and Figure 11 illustrate the PCM format with slave timing, FS and PCLK are provided by the host. Slave mode accommodates frame sync pulses with various widths (see GCI and PCM Timing Parameters, page 41).

Figure 12 and Figure 13 illustrate the PCM format with master timing, FS and PCLK are provided by the ZL38063. Master mode outputs a frame sync pulse equal to one PCLK cycle.

Diagrams for PCM transmit on negative edge (xeDX = 0) and PCM transmit on positive edge (xeDX = 1) are shown for both slave and master timing.

Figure 10 • **TDM – PCM Slave Functional Timing Diagram (8-bit, xeDX = 0)**

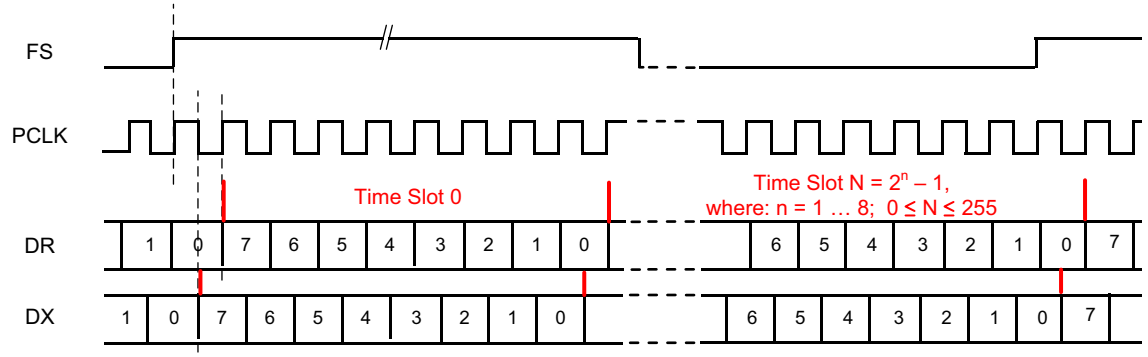


Figure 11 • **TDM – PCM Slave Functional Timing Diagram (8-bit, xeDX = 1)**

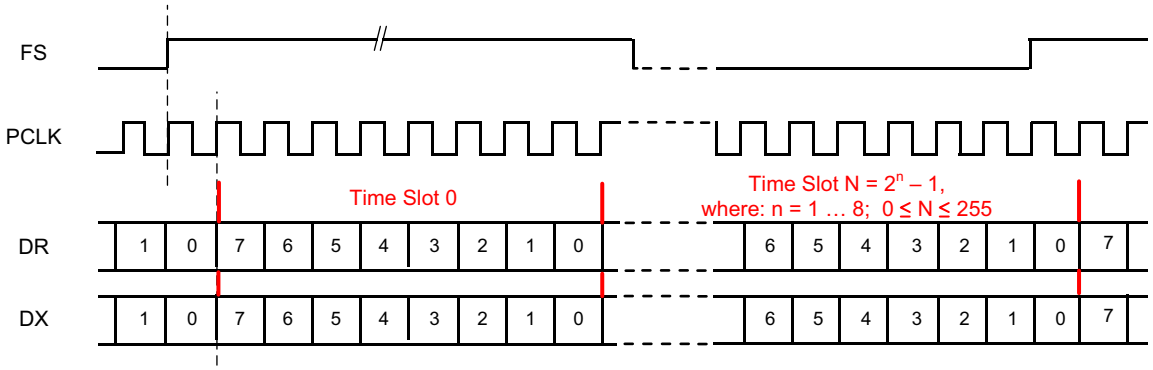


Figure 12 • **TDM – PCM Master Functional Timing Diagram (8-bit, xeDX = 0)**

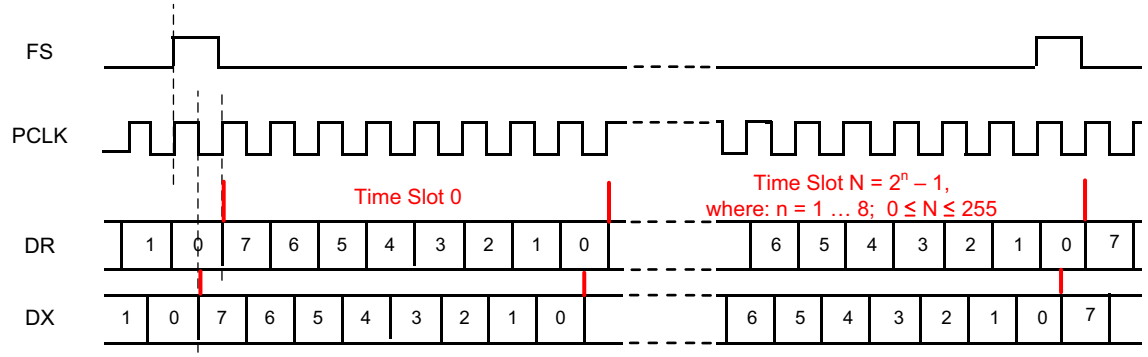
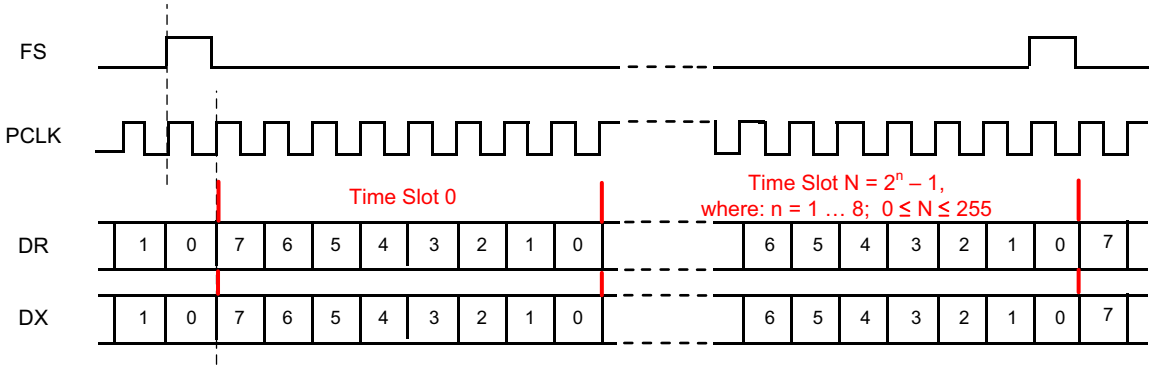


Figure 13 • **TDM – PCM Master Functional Timing Diagram (8-bit, xeDX = 1)**



5.1.3 GCI Mode

The GCI voice/data bytes can occupy any of the available timeslots. The GCI block can be configured as a master or a slave and supports a clock that has the same frequency as the data rate.

Note: Traditional GCI Monitor, Signaling, and Control channel bytes and double data rate are not supported.

Figure 14 illustrates the GCI format with slave timing, FS and PCLK are provided by the host. Slave mode accommodates frame sync pulses with various widths (see GCI and PCM Timing Parameters, page 41).

Figure 15 illustrates the GCI format with master timing, FS and PCLK are provided by the ZL38063. Master mode outputs a frame sync pulse equal to one PCLK cycle.

For both, first data bits are aligned with the rising edge of the frame sync pulse.

Figure 14 • **TDM – GCI Slave Functional Timing Diagram**

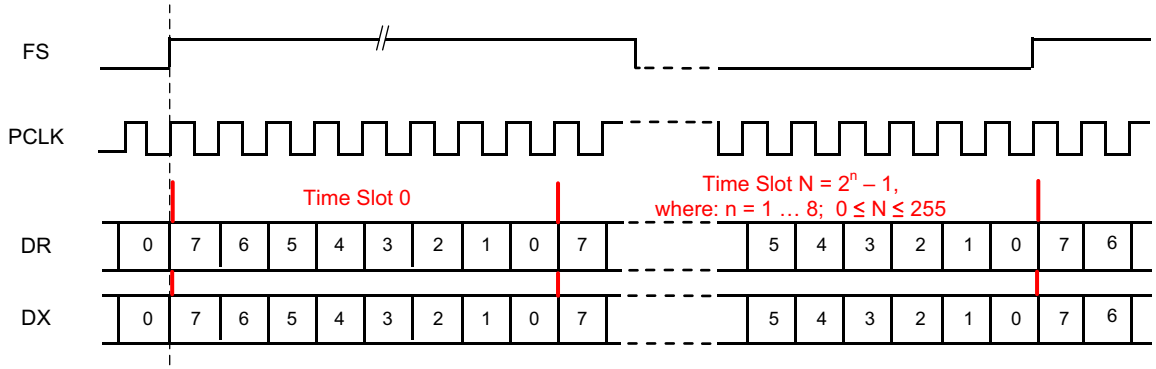
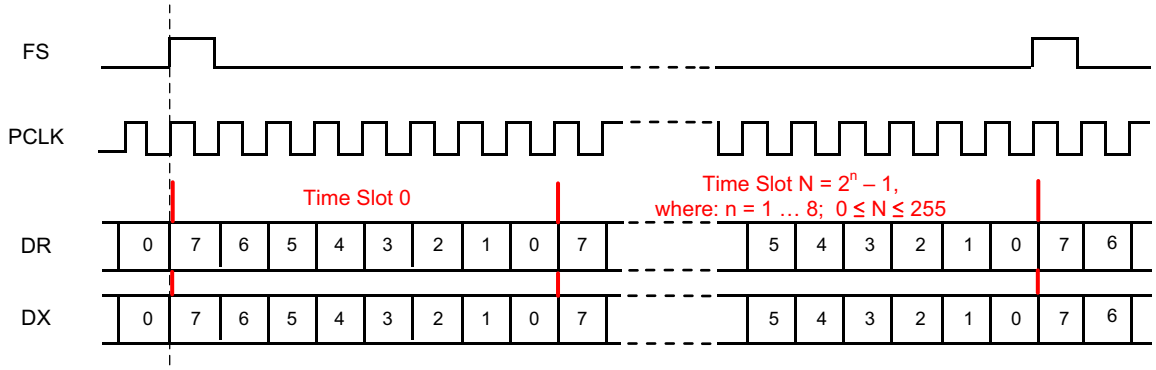


Figure 15 • **TDM – GCI Master Functional Timing Diagram**



5.2 Cross Point Switch – Two Way Voice Communication Mode

The Two Way Voice Communication Mode contains a Cross Point Switch that allows any input port to be routed to any output port as well as routing the input/outputs to/from the audio processor functions. Refer to the *Microsemi AcuEdge™ Technology ZLS38063 Firmware Manual* for Cross Point Switch operation and control.

5.3 Host Bus Interface

The host bus interface (HBI) is the main communication port from a host processor to the ZL38063. It can be configured to be either a SPI Slave or an I^2C Slave port, either of which can be used to program or query the device.

The ZL38063 allows for automatic configuration between SPI and I^2C operation. For the HBI port, if the HCLK toggles for two cycles, the HBI will default to the SPI Slave, otherwise it will remain configured as I^2C (see Table 2, page 12). The HBI comes up listening in both SPI and I^2C modes, but with I^2C inputs

selected. If HCLK is present, it switches the data selection before the first byte is complete so that no bits are lost. Once the port is determined to be SPI, a hardware reset is needed to change back to I^2C.

This port can read and write all of the memory and registers on the ZL38063. The port can also be used to boot the device, refer to Device Booting and Firmware Swapping, page 22.

Table 2 • **HBI Slave Interface Selection**

Description	Condition	Operating Mode	Notes
HBI Slave interface selection.	HCLK toggling	Host SPI bus	
	HDIN tied to VSS	Host I^2C bus. Slave address 45h (7-bit).	1
	HDIN tied to DVDD33	Host I^2C bus. Slave address 52h (7-bit).	

1. By default, the HBI comes up as an I^2C interface. Toggling the HCLK pin will cause the host interface to switch to a SPI interface. If an I^2C interface is desired, HCLK needs to be tied to ground.

5.3.1 SPI Slave

The physical layer is a 4-wire SPI interface. Chip select and clock are both inputs.

The SPI Slave port can support byte, word, or command framing. Write and read diagrams for these framing modes are shown in Figure 16 – Figure 21. The SPI Slave chip select polarity, clock polarity, and sampling phase are fixed.

The ZL38063 command protocol is half duplex, allowing the serial in and serial out to be shorted together for a 3- wire connection. The chip select is active low. The data is output on the falling edge of the clock and sampled on the rising edge of the clock.

The SPI Slave supports access rates up to 25 MHz. The outbound interrupt is always active low.

Figure 16 • **SPI Slave Byte Framing Mode – Write**

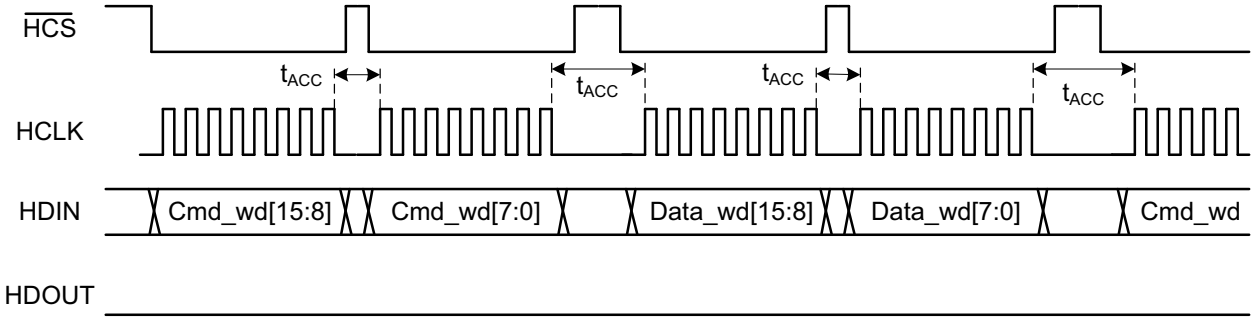


Figure 17 • **SPI Slave Byte Framing Mode – Read**

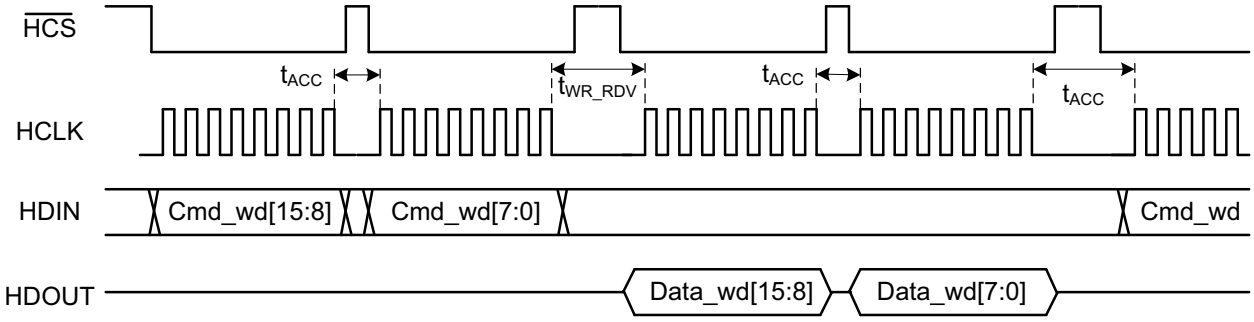


Figure 18 • **SPI Slave Word Framing Mode – Write, Multiple Data Words**

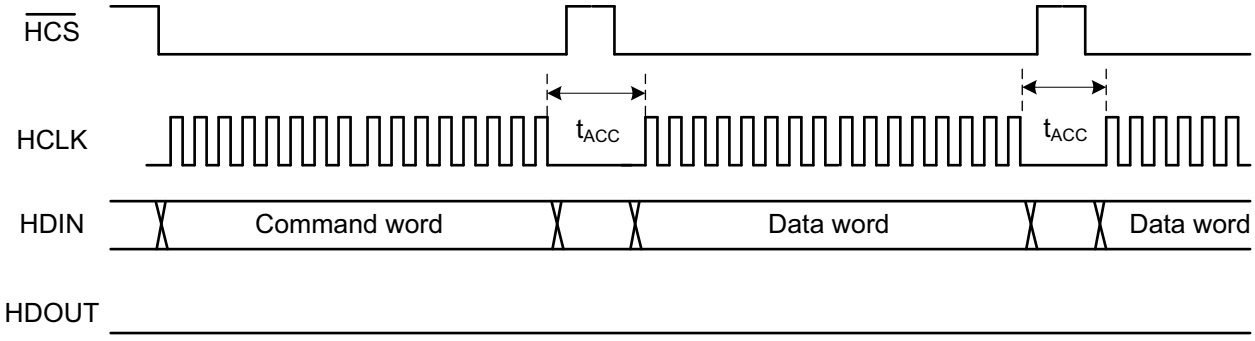


Figure 19 • **SPI Slave Word Framing Mode – Read, Multiple Data Words**

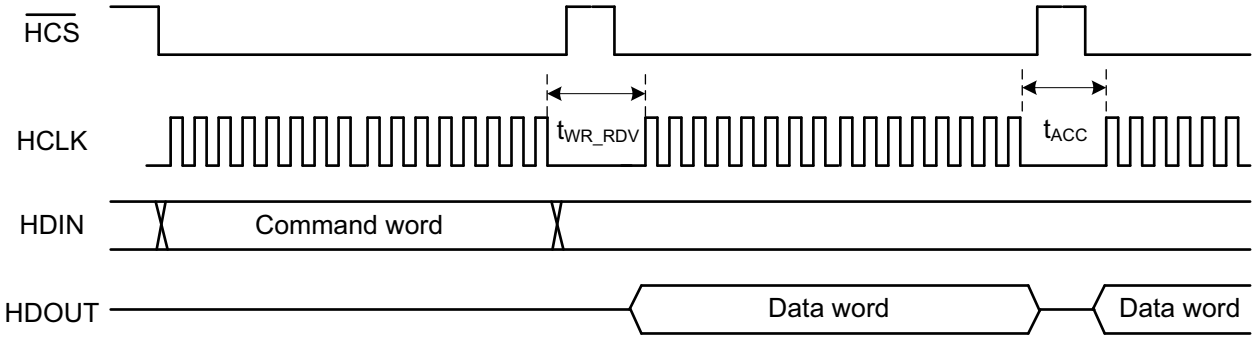


Figure 20 • **SPI Slave Command Framing Mode – Write**

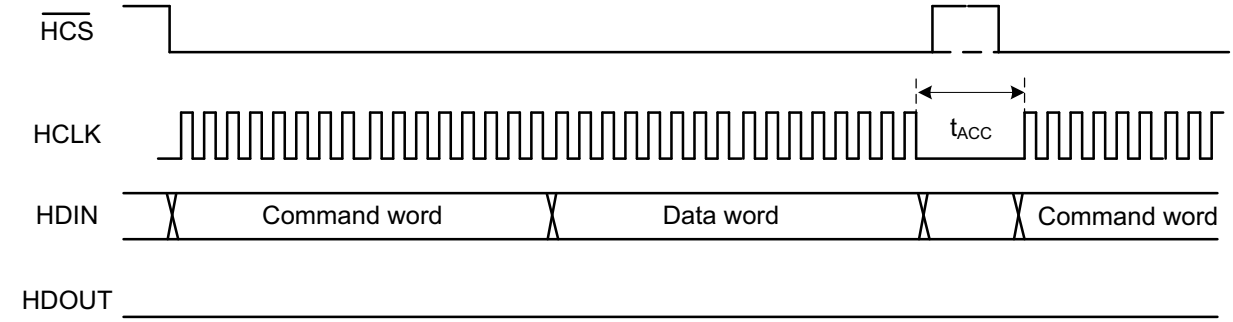
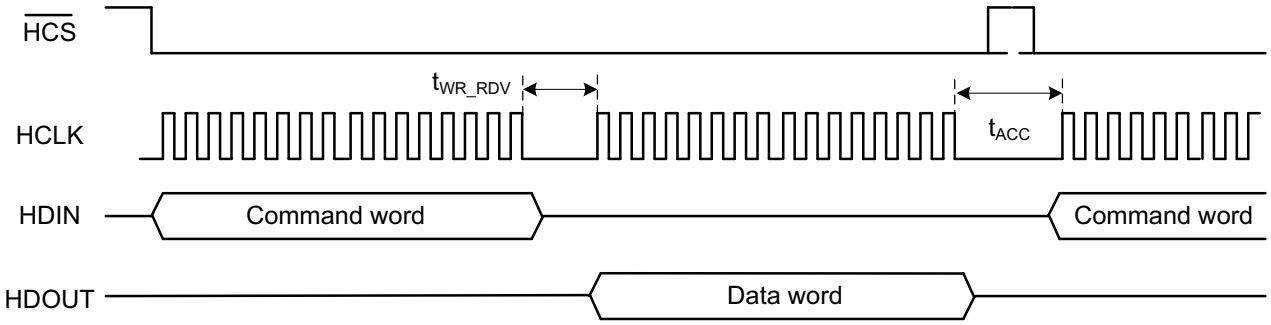


Figure 21 • **SPI Slave Command Framing Mode – Read**



5.3.2 I²C Slave

The I²C bus is similar to the Philips Semiconductor (NXP) 1998 Version 2.0, I²C standard. The ZL38063 I²C bus supports 7-bit addressing and transfer rates up to 400 kHz. External pull-up resistors are required on the I²C serial clock input ($\overline{HCS}$) and the I²C serial data input/output (HDOUT) when operating in this mode (note, the I²C slave pins are 3.3 V pins and are not 5 V tolerant).

The selection of the I^2C slave address is performed at bootup by the strapping of the HDIN and HCLK pins, see Table 2, page 12.

5.3.3 UART

The ZL38063 device incorporates a two-wire UART (Universal Asynchronous Receiver Transmitter) interface with a fixed 115.2K baud transfer rate, 8 data bits, 1 stop and no parity. TX and RX pins allow bi-directional communication with a host. The UART pins must be made accessible on the PCB for debug and tuning purposes.

5.3.4 Host Interrupt Pin

An internal host interrupt controller controls the active low interrupt pin which is part of the host bus interface. Associated with the interrupt controller is an event queue which reports status information about which event caused the interrupts.

Upon sensing the interrupt, the host can read the event queue to determine which event caused the interrupt. Specific events are enabled by the host processor, and are typically not used with a standalone (controllerless) design.

Refer to Events in the *Microsemi AcuEdge™ Technology ZLS38063 Firmware Manual* for Event ID Enumerations.

5.4 Master SPI

Like the HBI SPI Slave, the physical layer of the Master SPI is a 4-wire SPI interface supporting half duplex communication. It supports a chip select which is multiplexed with GPIO_9 for the flash interface and a chip select for a slave ZL38063 which is multiplexed with GPIO_3 (refer to Two ZL38063 Operation, page 17).

The Master SPI is only used by the built in boot ROM to load from an external serial Flash. The ZL38063 can automatically read the Flash data (program code and configuration record) through this interface upon the release of reset (Auto Boot), depending on the value of the bootstrap options.

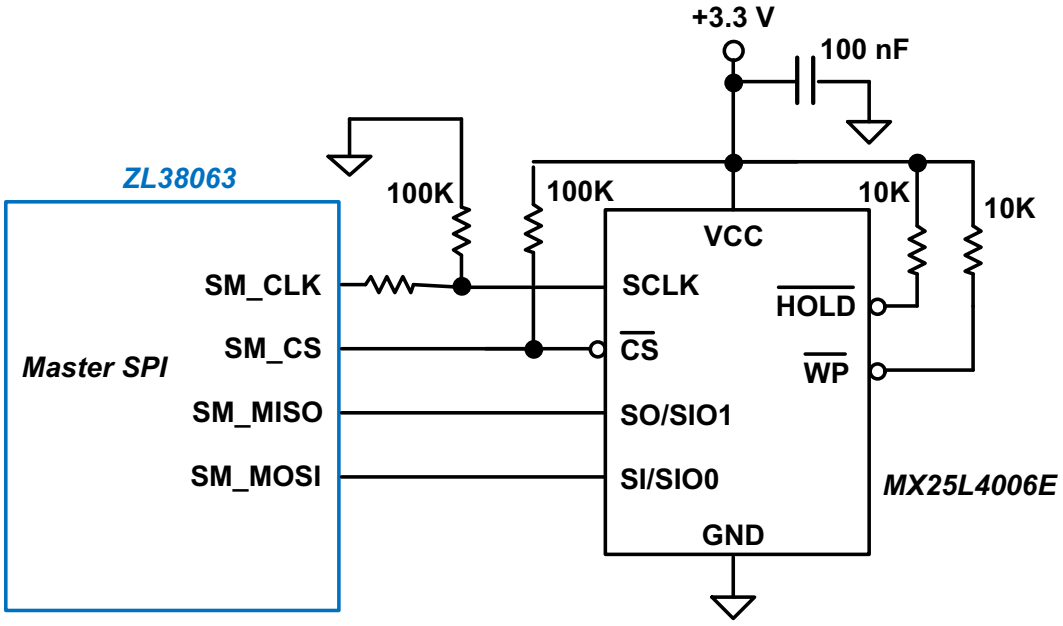
Note: An alternative to Auto Boot is to perform a Host Boot through the HBI port. Refer to Device Booting and Firmware Swapping, page 22.

5.4.1 Flash Interface

After power-up the ZL38063 will run its resident boot code, which establishes the initial setup of the Master SPI port and then downloads the firmware from external Flash memory when configured for auto boot mode. This Flash firmware establishes the resident application and sets the configuration of all the ZL38063 ports.

Figure 22 illustrates the connection of Flash memory to the ZL38063 Master SPI port. Figure 22 and the ZLE38000 demonstration hardware uses the Macronix™ MX25L4006E 4 Mbit CMOS Serial Flash device.

Figure 22 • **Flash Interface Circuit**



5.4.1.1 Flash Selection

The ZL38063 Boot ROM is designed to work with a wide variety of Flash devices. There are numerous Flash devices that the ZL38063 Boot ROM can recognize and program without host intervention other than a command to initialize the Flash. Other unrecognized devices may be utilized if they conform to certain characteristics of known devices and the host informs the ZL38063 Boot ROM of their type and size.

The ZL38063 identifies Flash devices (with a single binary image) with the ZL38063 boot ROM auto sensing the Flash type. The ZL38063 complies with *JEDEC Manufacturer and Device ID Read Methodology for SPI Compatible Serial Interface Memory Devices*. The ZL38063 is compatible with the *Serial Flash Discoverable Parameters JEDEC* standard JESD216B and the *Common Flash Interface* JESD68.01 JEDEC standard. The ZL38063 can identify devices by their JEDEC standard JEP106-K *Standard Manufacturer's Identification Code*.

Select a Flash size that is adequate to store all the firmware images required of the application. The image sizes can be obtained from the specific firmware releases.

A list of Flash devices that are identifiable by the ZL38063 Boot ROM are shown in Table 3. The size of these devices are all 2 Mbit or 4 Mbit, the Boot ROM will also recognize the size of 8 Mbit parts that are Type 1 or Type 2 devices (as defined in Table 4).

Table 3 • **Flash Devices Tested with the ZL38063**

Manufacturer	Part Number	Description
Macronix™	MX25V4006EM1I-13G	4 Mbit Flash.
Winbond™	W25X40CLSNIG-ND	4 Mbit Flash.
	W25X20CLSNIG-ND	2 Mbit Flash.
Micron®	M25P20-VMN6PB	Large 512 Kbit sectors limit the usefulness of this device. Holds only 1 application image.
	M25P40-VMN6PB	4 Mbit Flash. Large 512 Kbit sectors limit the usefulness of this device. Holds only 2 or 3 application images.
Microchip™	SST25VF020B-80-4I	2 Mbit Flash.

Table 3 • **Flash Devices Tested with the ZL38063**

Manufacturer	Part Number	Description
Atmel®	AT25DF041A AT45DB041D	4 Mbit Flash. Must be used in its 256 byte page variant. The default configuration is a 264 byte page. It can be ordered or programmed to use a 256 byte page.
Spansion™	S25FL204K0TMF1010	4 Mbit Flash.
AMIC Technology	A25L020O-F	2 Mbit Flash.

Flash devices whose JEDEC ID or size (usually a size of 16 Mbit or larger) that are not recognized by the ZL38063 Boot ROM can be made to work if they fit the characteristics of one of the four Flash types listed in Table 4. By writing the type (1, 2, 3, or 4) to ZL38063 address 0x118 and the number of sectors to ZL38063 address 0x116 prior to initializing the Flash device, the Boot ROM will treat it as a known device of known size even though the manufacturer ID or size field are not recognized.

Table 4 • **Supported Flash Types**

Characteristic	Type 1	Type 2	Type 3	Type 4
Sector Size	512 Kbit (64 KB)	32 Kbit (4 KB)	32 Kbit (4 KB)	16 Kbit (2 KB)
Read Status Reg Cmd	0x05	0x05	0x05	0xD7
Status Reg	Busy bit = 0x01	Busy bit = 0x01	Busy bit = 0x01	Done bit = 0x80
Data Read Cmd	0x03	0x03	0x03	0x03
Write Enable Cmd	0x06	0x06	0x06	N/A
Page Write Cmd	0x02	0x02	N/A Uses AAI to program word or byte. Uses Write Disable command to terminate AAI.	N/A Uses write from buffer command.
4-Byte Bulk Erase Cmd	N/A	N/A	N/A	0xC794809A
Examples	**Micron®** M25P20-VMN6PB M25P40-VMN6PB	**Winbond™** W25X40CLSNIG-ND W25X20CLSNIG-ND **Macronix™** MX25V4006EM1I-13G **AMIC Technology** A25L020O-F **Spansion™** S25FL204K0TMF1010 **Atmel®** AT25DF041A	**Microchip™** SST25VF020B-80-4I	**Atmel®** AT45DB021D AT45DB041D

5.5 GPIO

Note: GPIO functionality is limited with ASR related functionality. *Refer to the Microsemi AcuEdge™ Technology ZLS38063 Firmware Manual*.

The ZL38063 64-pin QFN package has 14 GPIO (General Purpose Input/Output) pins; the ZL38063 56-ball WLCSP package has 11 GPIO pins.

The GPIO pins can be individually configured as either inputs or outputs, and have associated maskable interrupts reported to the host processor through the interrupt controller and event queue. The GPIO pins are intended for low frequency signaling.

When a GPIO pin is defined as an input, the state of that pin is sampled and latched into the GPIO Read Register. A transition on a GPIO input can cause an interrupt and event to be passed to the host processor.

Certain GPIO pins have special predefined functions associated with the pin. Individual GPIO pins may also be defined as status outputs with associated enable/disable control. See Fixed Function I/O in the *Microsemi AcuEdge™ Technology ZLS38063 Firmware Manual*.

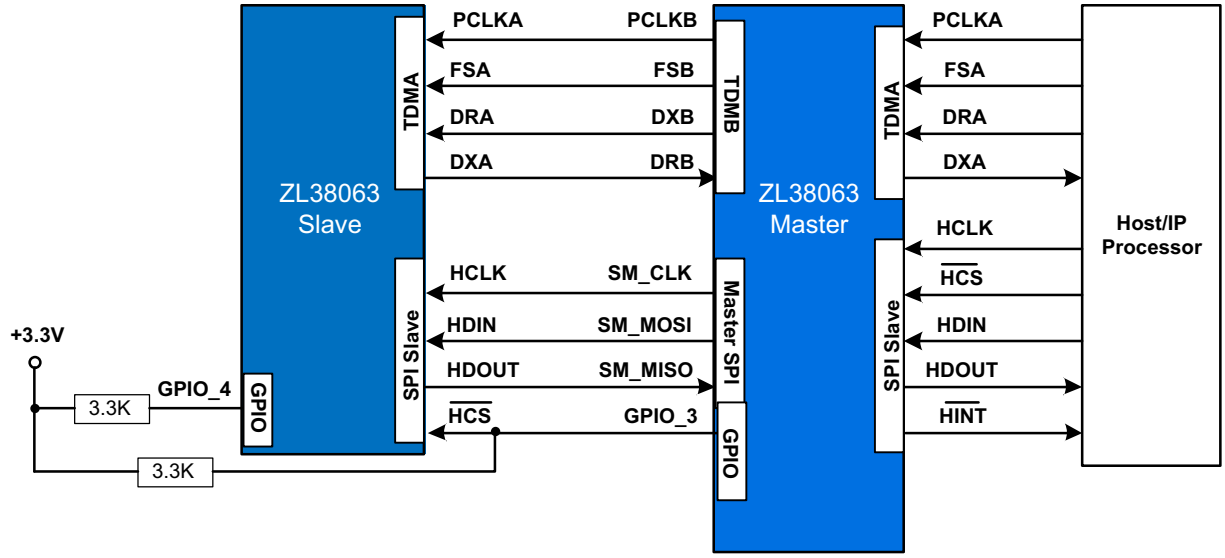
Immediately after any power-on or hardware reset the GPIO pins are defined as inputs and their state is captured in the GPIO Configuration Register. The state of this register is used to determine which options are selected for the device. The GPIO pin status is then redefined as specified in the configuration record that is loaded from the Flash or host.

In addition to the predefined fixed functions and the general functionality of the GPIO pins, the GPIO pins also support the bootstrap functions listed in Table 6, page 22.

5.6 Two ZL38063 Operation

Two ZL38063s can be chained to support up to six digital microphones in an array. The first device (master) manages the communication between the two devices transparently to the host processor. The master device requires a pull up resistor on GPIO_3. This is the chip select signal to the SPI slave port on the slave device. The slave device requires a pull up resistor on GPIO_4. This boot strap option identifies which device is the master and which is the slave. The audio data passes from the slave ZL38063's TDMA port to the master ZL38063's TDMB port. The interconnect between the two ZL38063s is illustrated in Figure 23.

Figure 23 • **ZL38063 Slave and Master Mode Operation**



6 Reset

The device has a hardware reset pin ($\overline{\text{RESET}}$) that places the entire device into a known low power state. The device will perform either a digital or an analog reset depending on the duration of the reset pulse.

- Digital reset – When the reset pin is brought low for a duration of between 100 ns and 1 µs, a digital reset occurs and all device states and registers are reset by this pin.
- Analog reset – When the reset pin is brought low for a duration greater than 10 µs, both a digital and an analog reset will occur. The analog reset will deactivate the internally generated +1.2 V by shutting off the external FET and the internal PLL. Raising the reset pin high will immediately turn back on these supplies (requiring a corresponding PLL startup time, ~3 ms).

For both digital and analog reset cases when reset is released, the device will go though its boot process and the firmware will be reloaded. If the reset had been an analog reset, then the boot process will take longer waiting for the system clocks to power back on.

GPIO sensing will occur with either type of reset.

A 10 KΩ pull-up resistor is required on the $\overline{\text{RESET}}$ pin to DVDD33 if this pin is not continuously driven.

7 Power Supply

7.1 Power Supply Sequencing/Power up

No special power supply sequencing is required. The +3.3 V or +1.2 V power rails can be applied in either order.

Upon power-up, the ZL38063 begins to boot and senses the external resistors on the GPIO to determine the bootstrap settings. After 3 ms, the boot process begins and the ZL38063 takes less than 1 second to become fully operational (for Auto Boot from Flash, including the time it takes to load the firmware).

In order to properly boot, the clocks (and power supplies) to the device must be stable. This requires either the 12.000 MHz crystal or clock oscillator to be active and stable before the ZL38063's reset is released.

7.1.1 Power Supply Considerations

The ZL38063 requires +1.2 V to power its core DSP power supply (DVDD12). To achieve optimum noise and power performance, supply DVDD12 from an external source. Use an LDO regulator like the Microsemi LX8213 to achieve low noise and low overall power consumption. The ZL38063 is designed to minimize power in its active states when DVDD12 is supplied externally.

To further reduce power, the internal PLL can be shut-down as described in Ultra-Low Power Mode, page 21.

7.1.1.1 External +1.2 V Power

Figure 24, page 20 shows DVDD12 powered from an external supply. A Microsemi LX8213 300 mA Low Noise CMOS LDO Regulator is shown.

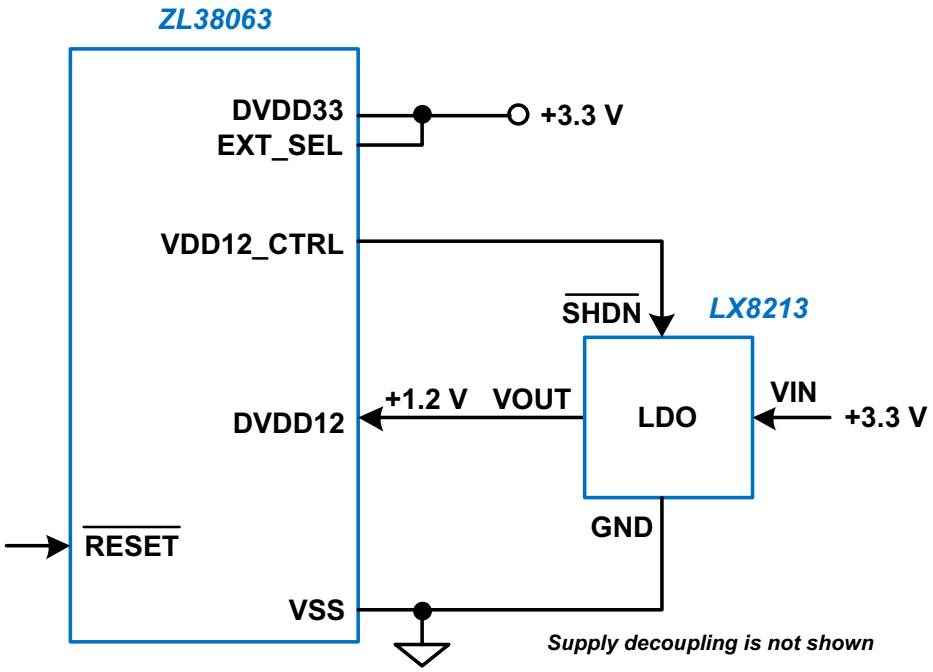
External supply use is selected when the EXT_SEL pin is tied to +3.3 V. The EXT_SEL pin can be pulled high or simply hard-wired to DVDD33.

VDD12_CTRL is a CMOS output which can be used to control the shutdown of the external supply. VDD12_CTRL will provide a steady +3.3 V output (with up to 4 mA of source current) for the external supply to be enabled and 0 V for the supply to be disabled.

For power savings when the ZL38063 does not need to be operational, the external voltage regulator can be turned off by pulling the $\overline{\text{RESET}}$ pin low for longer than 10 µS (Reset mode). This action will force the VDD12_CTRL pin low, shutting off the external LDO and allowing the +1.2 V supply to collapse to 0 V.

If shutdown of the external +1.2 V supply is not desired, simply leave the VDD12_CTRL output pin floating.

Figure 24 • **External +1.2 V Power Supply Configuration**



7.1.1.2 Internal +1.2 V Power

Note: The internal +1.2 V power option is only available with the 64-pin QFN package. The VDD12_CTRL pin is not available on the 56-ball WLCSP package.

Alternatively, the ZL38063 has a built-in voltage regulator that can be used as the DVDD12 source. The internal voltage regulator requires an external N-channel FET device and a parallel 470 ohm resistor. Figure 25, page 21 shows DVDD12 powered from the internal supply. Power dissipation is higher with internal regulator use due to the internal control circuitry and functional blocks being active.

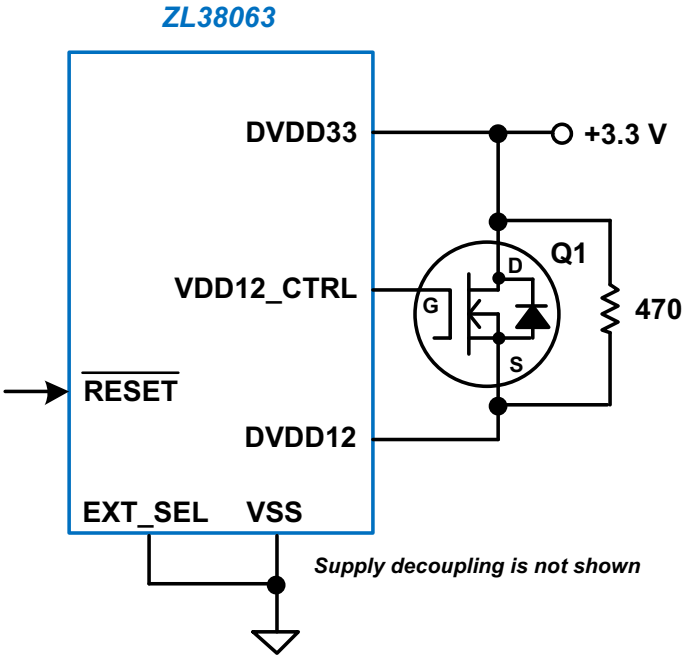
Internal supply use is selected when the EXT_SEL pin is tied to VSS. With the built-in voltage regulator enabled, VDD12_CTRL will drive Q1 and generate +1.2 V at DVDD12. The parallel 470 ohm resistor is required to ensure supply start-up. Q1 can be any of the high power FETs shown in Table 5, page 20, or an equivalent.

Table 5 • **Q1 Component Options**

Manufacturer	Part Number
Vishay®	Si1422DH
International Rectifier	IRLMS2002
Diodes Inc.®	ZXMN2B03E6

For power savings when the ZL38063 does not need to be operational, the internal voltage regulator can be turned off by pulling the RESET pin low for longer than 10 µS (Reset mode). This action will force the VDD12_CTRL pin low, shutting off the FET and allowing the +1.2 V supply to collapse to 0 V.

Figure 25 • **Internal +1.2 V Power Supply Configuration**



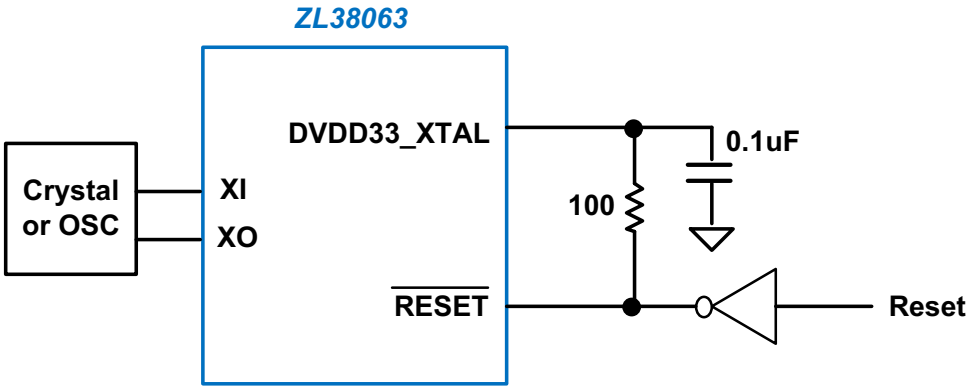
7.1.1.3 Ultra-Low Power Mode

Note: Ultra-low power mode is only available with the 64-pin QFN package. The DVDD33_XTAL pin is not available on the 56-ball WLCSP package.

The ZL38063 can be placed into an Ultra-low power state by turning off the crystal oscillator's internal voltage regulator. The circuit required to perform this is shown in Figure 26, page 21.

The external circuit that drives the ZL38063 $\overline{\text{RESET}}$ pin can also be used to power the DVDD33_XTAL pin. The reset drive circuit (gate) needs to provide at least 10 mA of source current when reset is high. The series 100 ohm resistor provides a time delay to keep crystal power from reacting to short reset pulses. When the reset line goes low for longer than 10 µS, the crystal oscillator's internal regulator will turn off and the ZL38063 will draw Ultra-low power as specified in Device Operating Modes, page 34.

Figure 26 • **Ultra-Low Power Operation Circuit**



8 Device Booting and Firmware Swapping

8.1 Boot Loader

The ZL38063 device contains a built-in boot-loader that gets executed after a hardware reset, when power is initially applied to the part, and during the Firmware Swap process. The Bootloader performs the following actions:

- Reads the GPIO bootstrap information and stores it in the Boot Sense registers
- Determinant on the bootstrap setting, it loads external serial Flash device contents (firmware and configuration record) into Program RAM (Auto Boot), or waits for the host to load Program RAM (Host Boot and Firmware Swap)
- If Auto Boot is selected, the Bootloader then programs the ZL38063 configuration registers to their proper default values, and jumps to Program RAM to execute the firmware

8.2 Bootstrap Modes

Table 6 lists the different boot options that can be selected by using external resistor. GPIOs have internal pull- down resistors, thereby defaulting to a 0 setting. A resistor to DVDD33 is required to select a 1 option. An external pull-up resistor must have a value of 3.3 KΩ. A GPIO with a bootstrap pull-up can be used for other functionality following the power-up boot sense process.

Table 6 • **Bootstrap Modes**

GPIO_2	Operating Mode	Description	Notes
0	Host Boot (default)	Boot source selection	
1	Auto Boot from external Flash		1

1. Apply a 3.3 KΩ resistor from GPIO_2 to DVDD33. Note, when external Flash is selected, GPIO_9 = SM_CS

8.3 Loadable Device Code

In order for the ZL38063 to operate, it must be loaded with code that resides externally. This code can either be Auto Booted from an external Flash memory through the Master SPI, or can be loaded into the ZL38063 by the host processor through the HBI port. An external resistor pull-up or an internal resistor pull-down determines which boot mode will be used (see Table 6).

The external code consists of two logical segments, the firmware code itself and the configuration record. The firmware is a binary image which contains all of the executable code allowing the ZL38063 to perform voice processing and establishes the user command set. The configuration record contains settings for all of the user registers and defines the power-up operation of the device.

The configuration record is set up so that the registers are initialized to their desired values for normal operation.

A GUI development tool (*MiTuner*™ ZLS38508) is provided to create and modify a configuration record and create a bootable Flash image which can then be duplicated for production of the end product. This tool requires access to the UART and to the I^2S port for tuning (refer to AEC Tuning, page 50).

8.3.1 Boot Speed

When performing an Auto Boot from a Flash device the boot sequence lasts <1 second (for a typical firmware image and configuration record of size 400kB, and a SPI clock speed of around 3.2MHz or higher).

When performing a Host Boot through the HBI SPI/I^2C Slave port, the boot time will vary depending on the host's communications speed. SPI can run up to a speed of 25 MHz and has less overhead, allowing it to perform a boot download ~<300 ms; I^2C is limited to a speed of 400 kHz, making a boot download

last ~>5 seconds. If boot speed is important, use the HBI SPI Slave port (or Flash) for booting rather than the I^2C Slave port.

8.4 Bootup Procedure

Valid clocks (crystal or clock oscillator) must be present before the ZL38063 device can exit its reset state. After the reset line is released, the ZL38063's internal voltage regulator will be enabled (if the EXT_SEL pin is strapped low). Once the +1.2 V supply is established, the PLL will be also be enabled. Based on GPIO_0 and GPIO_1 bootstrap settings being 0, the ZL38063 will select the system parameters and the PLL will lock to the crystal or clock oscillator 12.000 MHz operating frequency. An event will be placed in the event queue and the interrupt pin ($\overline{\text{HINT}}$) will be pulled low to signal the host when it's OK to load boot code.

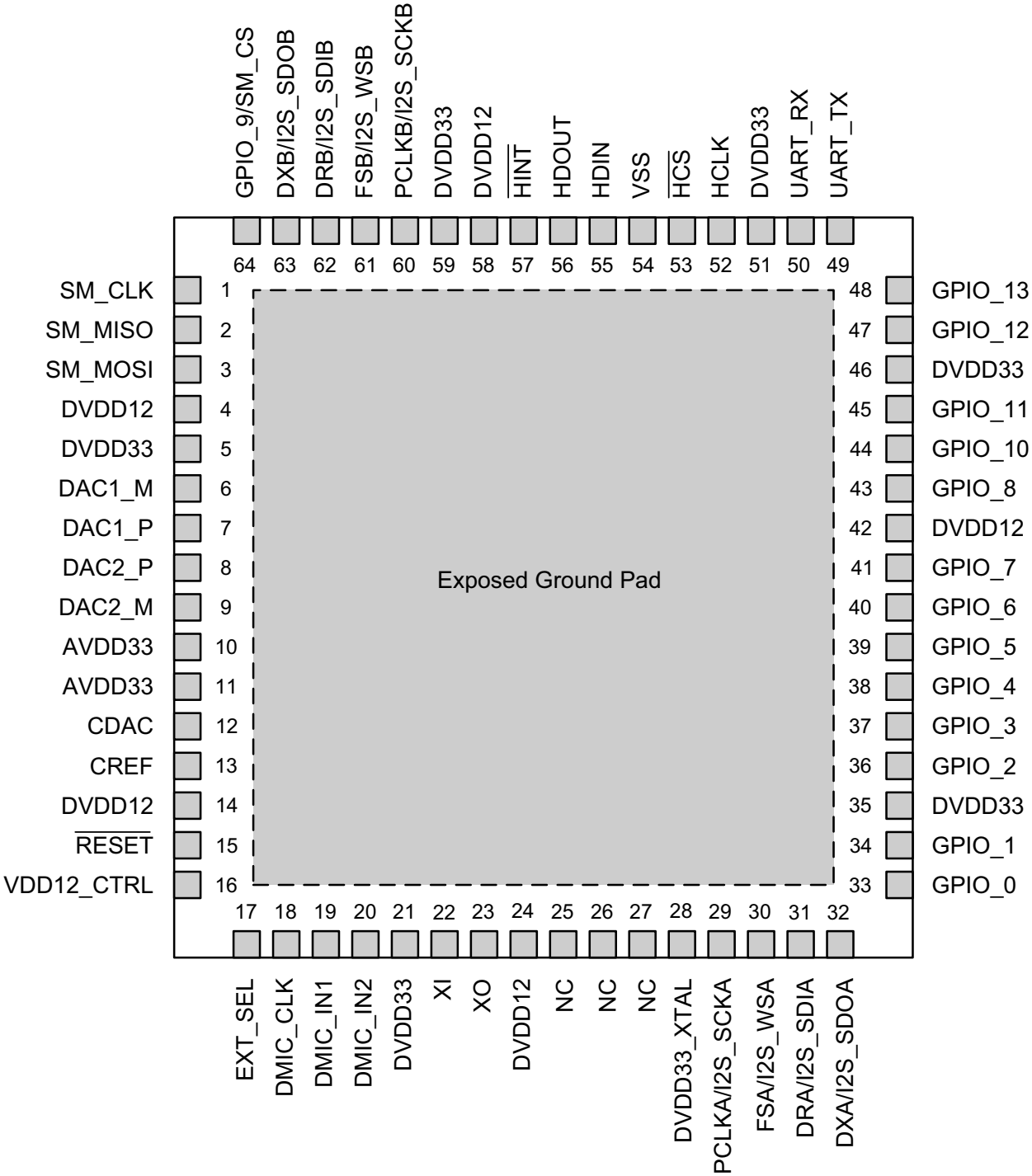
Next, if the GPIO strapping pins indicate that the ZL38063 will Auto Boot, it will begin reading data from the external Flash. Refer to the *Microsemi AcuEdge™ Technology ZLS38063 Firmware Manual* for a listing of the complete Boot Sequence.

If the GPIO strapping pins indicate that the ZL38063 will Host Boot, the SPI or I^2C port that initiates the loading process becomes the boot master. The ZL38063 allows for automatic configuration between SPI and I^2C operation. For the HBI port, if the HCLK toggles for two cycles, the HBI will default to the SPI Slave, otherwise it will remain configured as I^2C.

9 Device Pinouts

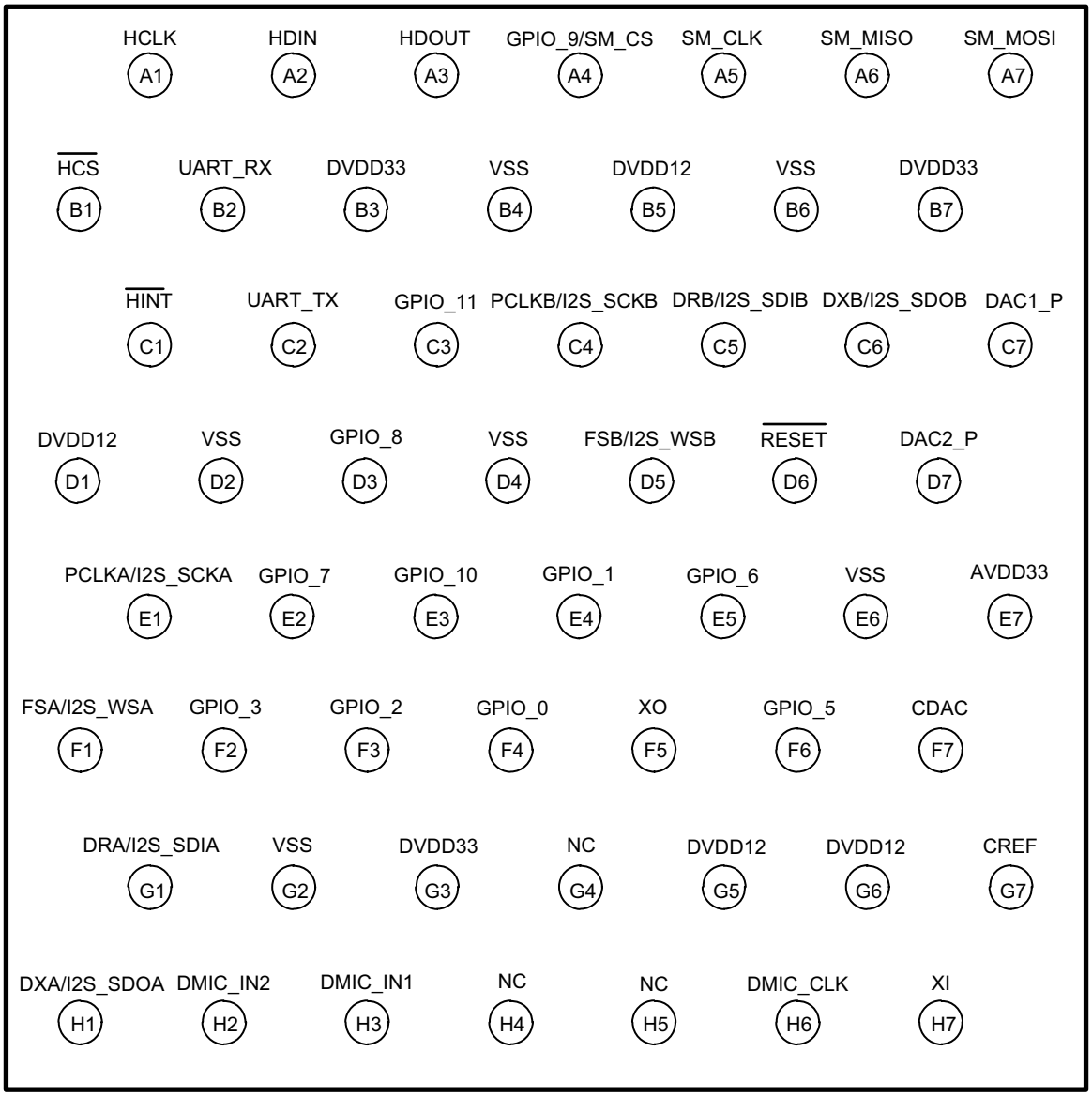
9.1 64-Pin QFN

Figure 27 • **ZL38063 64-Pin QFN – Top View**



9.2 56-Ball WLCSP

Figure 28 • **ZL38063 56-Ball WLCSP – Top View**



10 Pin Descriptions

10.1 Reset Pin

Table 7 • **Reset Pin Description**

QFN Pin #	WLCSP Ball	Name	Type	Description
15	D6	$\overline{\text{RESET}}$	Input	**Reset.** When low the device is in its reset state and all tristate outputs will be in a high impedance state. This input must be high for normal device operation. *A 10 KΩ pull-up resistor is required on this pin to DVDD33 if this pin is not continuously driven.* Refer to Reset, page 18 for an explanation of the various reset states and their timing.

10.2 DAC Pins

Table 8 • **DAC Pin Description**

QFN Pin #	WLCSP Ball	Name	Type	Description
6	–	DAC1_M	Output	**DAC 1 Minus Output.** This is the negative output signal of the differential amplifier of DAC 1. Pin functionality is firmware dependent. *Not available on the WLCSP package.*
7	C7	DAC1_P	Output	**DAC 1 Plus Output.** This is the positive output signal of the differential amplifier of DAC 1. Pin functionality is firmware dependent.
9	–	DAC2_M	Output	**DAC 2 Minus Output.** This is the negative output signal of the differential amplifier of DAC 2. Pin functionality is firmware dependent. *Not available on the WLCSP package.*
8	D7	DAC2_P	Output	**DAC 2 Plus Output.** This is the positive output signal of the differential amplifier of DAC 2. Pin functionality is firmware dependent.
12	F7	CDAC	Output	**DAC Reference.** This pin may require capacitive decoupling. Refer to DAC Output, page 4.
13	G7	CREF	Output	**Common Mode Reference.** This pin requires capacitive decoupling. Refer to DAC Output, page 4.

10.3 Microphone Pins

Table 9 • **Microphone Pin Description**

QFN Pin #	WLCSP Ball	Name	Type	Description
18	H6	DMIC_CLK	Output	**Digital Microphone Clock Output.** Clock output for digital microphones and digital electret microphone pre-amplifier devices.
19, 20	H3, H2	DMIC_IN1,2	Input	**Digital Microphone Input 1/2.** Stereo or mono digital microphone inputs. *Tie to VSS if unused.*

10.4 TDM and I²S Ports Pins

The firmware supports two TDM interfaces, TDM-A and TDM-B. Each TDM block is capable of being a master or a slave. The ports can be configured for Pulse-Code Modulation (PCM) or Inter-IC Sound (I^2S) operation. The ports conform to PCM, GCI, and I^2S timing protocols.

Table 10 • **TDM and I^2S Ports Pin Descriptions**

QFN Pin #	WLCSP Ball	Name	Type	Description
29	E1	PCLKA/ I2S_SCKA	Input/ Output	**PCM Port A Clock (Input/Tristate Output).** PCLKA is equal to the bit rate of signals DRA/DXA. In TDM master mode this clock is an output and in TDM slave mode this clock is an input. **I^2S Port A Serial Clock (Input/Tristate Output).** This is the I^2S port A bit clock. In I^2S master mode this clock is an output and drives the bit clock input of the external slave device's peripheral converters. In I^2S slave mode this clock is an input and is driven from a converter operating in master mode. After power-up, this signal defaults to be an input in I^2S slave mode. *A 100 KW pull-down resistor is required on this pin to VSS. If this pin is unused, tie the pin to VSS.* *When driving PCLKA/I2S_SCKA from a host, one of the following conditions must be satisfied:* *1. Host drives PCLKA low during reset, or* *2. Host tri-states PCLKA during reset (the 100 KW resistor will keep PCLKA low), or* *3. Host drives PCLKA at its normal frequency*
30	F1	FSA/ I2S_WSA	Input/ Output	**CM Port A Frame Sync (Input/Tristate Output).** This is the TDM frame alignment reference. This signal is an input for applications where the PCM bus is frame aligned to an external frame signal (slave mode). In master mode this signal is a frame pulse output. **I^2S Port A Word Select (Left/Right) (Input/Tristate Output).** This is the I^2S port A left or right word select. In I^2S master mode word select is an output which drives the left/right input of the external slave device's peripheral converters. In I^2S slave mode this pin is an input which is driven from a converter operating in master mode. After power-up, this signal defaults to be an input in I^2S slave mode. *Tie this pin to VSS if unused.*

Table 10 • **TDM and I²S Ports Pin Descriptions *(continued)***

QFN Pin #	WLCSP Ball	Name	Type	Description
31	G1	DRA/ I2S_SDIA	Input	**PCM Port A Serial Data Stream Input.** This serial data stream operates at PCLK data rates. **I²S Port A Serial Data Input.** This is the I²S port serial data input. *Tie this pin to VSS if unused.*
32	H1	DXA/ I2S_SDOA	Output	**PCM Port A Serial Data Stream Output.** This serial data stream operates at PCLK data rates. **I²S Port A Serial Data Output.** This is the I²S port serial data output.
60	C4	PCLKB/ I2S_SCKB	Input/ Output	**PCM Port B Clock (Input/Tristate Output).** PCLKB is equal to the bit rate of signals DRB/DXB. In TDM master mode this clock is an output and in TDM slave mode this clock is an input. **I²S Port B Serial Clock (Input/Tristate Output).** This is the I²S port B bit clock. In I²S master mode this clock is an output and drives the bit clock input of the external slave device's peripheral converters. In I²S slave mode this clock is an input and is driven from a converter operating in master mode. After power-up, this signal is an input in I²S slave mode. *Tie this pin to VSS if unused.*
61	D5	FSB/ I2S_WSB	Input/ Output	**PCM Port B Frame Sync (Input/Tristate Output).** This is the TDM frame alignment reference. This signal is an input for applications where the PCM bus is frame aligned to an external frame signal (slave mode). In master mode this signal is a frame pulse output. **I²S Port B Word Select (Left/Right) (Input/Tristate Output).** This is the I²S port B left or right word select. In I²S master mode word select is an output which drives the left/right input of the external slave device's peripheral converters. In I²S slave mode this pin is an input which is driven from a converter operating in master mode. After power-up, this signal defaults to be an input in I²S slave mode. *Tie this pin to VSS if unused.*
62	C5	DRB/ I2S_SDIB	Input	**PCM Port B Serial Data Stream Input.** This serial data stream operates at PCLK data rates. **I²S Port B Serial Data Input.** This is the I²S port serial data input. *Tie this pin to VSS if unused.*
63	C6	DXB/ I2S_SDOB	Output	**PCM Port B Serial Data Stream Output.** This serial data stream operates at PCLK data rates. **I²S Port B Serial Data Output.** This is the I²S port serial data output.

10.5 HBI – SPI Slave Port Pins

This port functions as a peripheral interface for an external controller, and supports access to the internal registers and memory of the device.

Table 11 • **HBI – SPI Slave Port Pin Descriptions**

QFN Pin #	WLCSP Ball	Name	Type	Description
52	A1	HCLK	Input	**HBI SPI Slave Port Clock Input.** Clock input for the SPI Slave port. Maximum frequency = 25 MHz. This input should be tied to VSS in I^2C mode, refer to Table 2, page 12. *Tie this pin to VSS if unused.*
53	B1	$\overline{HCS}$	Input	**HBI SPI Slave Chip Select Input.** This active low chip select signal activates the SPI Slave port. **HBI I^2C Serial Clock Input.** This pin functions as the I2C_SCLK input in I^2C mode. *A pull-up resistor is required on this node for I^2C operation.* *Tie this pin to VSS if unused.*
55	A2	HDIN	Input	**HBI SPI Slave Port Data Input.** Data input signal for the SPI Slave port. This input selects the slave address in I^2C mode, refer to Table 2, page 12. *Tie this pin to VSS if unused.*
56	A3	HDOUT	Input/ Output	**HBI SPI Slave Port Data Output (Tristate Output).** Data output signal for the SPI Slave port. **HBI I^2C Serial Data (Input/Output).** This pin functions as the I2C_SDA I/O in I^2C mode. *A pull-up resistor is required on this node for I^2C operation.*
57	C1	$\overline{HINT}$	Output	**HBI Interrupt Output.** This output can be configured as either CMOS or open drain by the host.

10.6 Master SPI Port Pins

This port functions as the interface to an external Flash device used to optionally Auto Boot and load the device's firmware and configuration record from external Flash memory

Table 12 • **Master SPI Port Pin Descriptions**

QFN Pin #	WLCSP Ball	Name	Type	Description
1	A5	SM_CLK	Output	**Master SPI Port Clock (Tristate Output).** Clock output for the Master SPI port. Maximum frequency = 8 MHz.
2	A6	SM_MISO	Input	**Master SPI Port Data Input.** Data input signal for the Master SPI port.
3	A7	SM_MOSI	Output	**Master SPI Port Data Output (Tristate Output).** Data output signal for the Master SPI port.
64	A4	GPIO_9/ SM_CS	Input/ Output	**Master SPI Port Chip Select (Input Internal Pull-Up/Tristate Output).** Chip select output for the Master SPI port. Shared with GPIO_9, see Table 15, page 30.

10.7 Oscillator Pins

These pins are connected to a 12.000 MHz crystal or clock oscillator which drives the device's internal PLL.

Table 13 • **Oscillator Pin Descriptions**

QFN Pin #	WLCSP Ball	Name	Type	Description
22	H7	XI	Input	**Crystal Oscillator Input.** Refer to External Clock Requirements, page 39.
23	F5	XO	Output	**Crystal Oscillator Output.** Refer to External Clock Requirements, page 39.

10.8 UART Pins

The ZL38063 device incorporates a two-wire UART (Universal Asynchronous Receiver Transmitter) interface with a fixed 115.2K baud transfer rate, 8 data bits, 1 stop and no parity. The UART port can be used as a debug tool and is used for tuning purposes.

Table 14 • **UART Pin Descriptions**

QFN Pin #	WLCSP Ball	Name	Type	Description
50	B2	UART_RX	Input	**UART (Input).** Receive serial data in. This port functions as a peripheral interface for an external controller and supports access to the internal registers and memory of the device.
49	C2	UART_TX	Output	**UART (Tristate Output).** Transmit serial data out. This port functions as a peripheral interface for an external controller and supports access to the internal registers and memory of the device.

10.9 GPIO Pins

GPIO ports can be used for interrupt and event reporting, fixed function control, bootstrap options, as well as being used for general purpose I/O for communication and controlling external devices. Pin functionality is firmware dependent.

Table 15 • **GPIO Pin Descriptions**

QFN Pin #	WLCSP Ball	Name	Type	Description
33, 34	F4, E4	GPIO_[0:1]	Input/ Output	**General Purpose I/O (Input Internal Pull-Down/Tristate Output).** These pins can be configured as an input or output and are intended for low-frequency signaling. They must be pulled low or left floating when coming out of reset.
36	F3	GPIO_2	Input/ Output	**General Purpose I/O (Input Internal Pull-Down/Tristate Output).** These pins can be configured as an input or output and are intended for low-frequency signaling. Refer to Table 6, page 22 for bootstrap functionality.
37, 38, 39, 40, 41, 43	F2, –, F6, E5, E2, D3	GPIO_[3:8]	Input/ Output	**General Purpose I/O (Input Internal Pull-Down/Tristate Output).** These pins can be configured as an input or output and are intended for low-frequency signaling.

Table 15 • **GPIO Pin Descriptions *(continued)***

QFN Pin #	WLCSP Ball	Name	Type	Description
64	A4	GPIO_9/ SM_CS	Input/ Output	**General Purpose I/O (Input Internal Pull-Down/Tristate Output).** This pin can be configured as an input or output and is intended for low-frequency signaling. Alternate functionality with SM_CS, see Table 12, page 29.
44, 45, 47, 48	E3, C3, –, –	GPIO_ [10:13]	Input/ Output	**General Purpose I/O (Input Internal Pull-Down/Tristate Output).** These pins can be configured as an input or output and are intended for low-frequency signaling. *GPIO_12 and GPIO_13 are not available on the WLCSP package.*

10.10 Supply and Ground Pins

Table 16 • **Supply and Ground Pin Descriptions**

QFN Pin #	WLCSP Ball	Name	Type	Description
17	–	EXT_SEL	Input	**VDD +1.2 V Select.** Select external +1.2 V supply. Tie to DVDD33 if the +1.2 V supply is to be provided externally. Tie to VSS (0 V) if the +1.2 V supply is to be generated internally. Refer to Power Supply Considerations, page 19 for more information. *Not available on the WLCSP package.*
16	–	VDD12_CTRL	Output	**VDD +1.2 V Control.** Analog control line for the voltage regulator external FET when EXT_SEL is tied to VSS. When EXT_SEL is tied to DVDD33, the VDD12_CTRL pin becomes a CMOS output which can drive the shutdown input of an external LDO. Refer to 6.1.1, Power Supply Considerations, page 19 for more information. *Not available on the WLCSP package.*
4, 14, 24, 42, 58	B5, D1, G5, G6	DVDD12	Power	**Core Supply.** Connect to a +1.2 V ±5% supply. *Place a 100 nF, 20%, 10 V, ceramic capacitor on each pin decoupled to the VSS plane.* Refer to Power Supply Considerations, page 19 for more information.
5, 21, 35, 46, 51, 59	B3, B7, G3	DVDD33	Power	**Digital Supply.** Connect to a +3.3 V ±5% supply. *Place a 100 nF, 20%, 10 V, ceramic capacitor on each pin decoupled to the VSS plane.*
28	–	DVDD33_ XTAL	Power	**Crystal Digital Supply.** This pin must be connected to a +3.3 V supply source capable of delivering 10 mA. *Not available on the WLCSP package.*
10, 11	E7	AVDD33	Power	**Analog Supply.** Connect to a +3.3 V ±5% supply. *Place a 100 nF, 20%, 10 V, ceramic capacitor on each pin decoupled to the VSS plane.*
54	B4, B6, D2, D4, E6, G2	VSS	Ground	**Ground.** Connect to digital ground plane.

Table 16 • **Supply and Ground Pin Descriptions *(continued)***

QFN Pin #	WLCSP Ball	Name	Type	Description
	–	Exposed Ground Pad	Ground	**Exposed Pad Substrate Connection.** Connect to VSS. This pad is at ground potential and must be soldered to the printed circuit board and connected via multiple vias to a heatsink area on the bottom of the board and to the internal ground plane. *Not available on the WLCSP package.*

10.11 No Connect Pins

Table 17 • **No Connect Pin Description**

QFN Pin #	WLCSP Ball	Name	Type	Description
25, 26, 27	G4, H4, H5	NC		**No Connection.** These pins are to be left unconnected, do not use as a tie point.

11 Electrical Characteristics

11.1 Absolute Maximum Ratings

Stresses above those listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 18 • **Absolute Maximum Ratings**

Supply voltage (DVDD33, AVDD33)	−0.5 to +4.0 V
Core supply voltage (DVDD12)	−0.5 to +1.32 V
Input voltage	−0.5 to +4.0 V
Continuous current at digital outputs	15 mA
Reflow temperature, 10 sec., MSL3, per *JEDEC J-STD-020*	260 °C
Storage temperature	−55 to +125 °C
ESD immunity (Human Body Model)	JESD22 Class 1C compliant

11.2 Thermal Resistance

Table 19 • **Thermal Resistance**

Junction to ambient thermal resistance[1], θ_{JA}	64-pin QFN	°C/W
	56-ball WLCSP	°C/W
Junction to board thermal resistance[1], θ_{JB}	64-pin QFN	°C/W
	56-ball WLCSP	°C/W
Junction to exposed pad thermal resistance[1], θ_{JC}	64-pin QFN	°C/W
Junction to case thermal resistance[1], θ_{JC}	56-ball WLCSP	°C/W
Junction to top characterization parameter, Ψ_{JT}	64-pin QFN	0.1 °C/W
	56-ball WLCSP	°C/W

1. The thermal specifications assume that the device is mounted on an effective thermal conductivity test board (4 layers, 2s2p) per JEDEC JESD51-7 and JESD51-5

11.3 Operating Ranges

Microsemi guarantees the performance of this device over the industrial (−40 °C to 85 °C) temperature range by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with the *Telcordia GR-357-CORE Generic Requirements for Assuring the Reliability of Components Used in Telecommunications Equipment*.

Table 20 • **Operating Ranges**

Parameter	Symbol	Min.	Typ.	Max.	Units
Ambient temperature	T_A	−40		+85	°C

Table 20 • **Operating Ranges *(continued)***

Parameter	Symbol	Min.	Typ.	Max.	Units
Analog supply voltage	V_{AVDD33}	3.135	3.3	3.465	V
Digital supply voltage	V_{AVDD33}				
Crystal Digital supply voltage	V_{DVDD33_XTAL}				
Crystal I/O voltage	V_{XI}		2.5	2.625	V
Core supply voltage	V_{DVDD12}	1.14	1.2	1.26	V

11.4 Device Operating Modes

When the Two Way Voice Communication Firmware or one of the ASR Firmwares is running, the ZL38063 is considered to be in normal operating mode.

Low-power and sleep modes are firmware programmable options. Reset and Ultra-low power modes are hardware modes that can be utilized to minimize power consumption for all firmware variants.

Operating modes are highlighted in the following sections. Refer to the *Microsemi AcuEdge™ Technology ZLS38063 Firmware Manual* for programming and additional information on the firmware operating modes.

11.4.1 Two-Way Audio Operation

- HBI active
- Audio path active, wideband or narrowband operation
- DACs and MICs can be enabled
- Audio Processor always on

Normal mode is recommended for applications that use the internal voltage regulator with analog microphones. Normal mode keeps the Audio Processor always on, thereby minimizing +1.2 V power supply noise that could be injected into sensitive analog microphone circuitry via the board layout.

11.4.2 Low-Power Two-Way Audio Operation

- Low-Power firmware mode
- HBI active
- Audio path active, wideband or narrowband operation
- DACs and MICs can be enabled
- Audio Processor operates in Power Saving Mode

Low-power mode is selected in register 0x206 (System Control Flags) bit 1, or can be selected from the ZLS38508 *MiTuner™* GUI in the AEC Control window (Enable Power Saving Mode). Low-Power mode is not recommended for applications that use the internal voltage regulator with analog microphones.

11.4.3 Automatic Speech Recognition Assist Operation

- HBI active
- One mic active
- DAC's disabled
- Audio processor operates in power saving mode

11.4.4 Sleep

- Sleep firmware mode
- HBI active
- Audio path inactive
- DACs and MICs are powered down
- Audio Processor made inactive, internal clocks are shutdown, requires a wake-up procedure to return to Normal or Low-Power mode

The ZL38063 will respond to no other inputs until it awakens from Sleep mode. To wake from Sleep mode, perform an HBI Wake From Sleep operation, as described in the *Microsemi AcuEdge™*

Technology ZLS38063 Firmware Manual Appendix D. The firmware and configuration records loaded into the device RAM are retained, no re-boot is required.

11.4.5 Reset

- Hardware mode, the ZL38063 goes into this mode when the RESET pin is held low for greater than 10 µS
- HBI inactive
- Audio path inactive
- DACs and MICs are powered down
- Audio Processor powered down via removal of +1.2 V supply

See Reset, page 18 for more information and refer to Power Supply, page 19 for information on +1.2 V removal.

11.4.6 Ultra-Low Power

- Hardware mode, the hardware can be configured to enter this mode when the RESET pin is held low for greater than 10 µS
- HBI inactive
- Audio path inactive
- DACs and MICs are powered down
- Audio Processor powered down via removal of +1.2 V supply
- Crystal or clock oscillator supply made inactive

See Reset, page 18 and Ultra-Low Power Mode, page 21 for more information, refer to Power Supply, page 19 for information on +1.2 V removal.

11.4.7 Current Consumption

Device current consumption can vary with the firmware load. Common values are listed here using an external +1.2 V supply for the core power supply with a 12.000 MHz crystal and a 3.3 KΩ resistor from GPIO_2 to DVDD33 (external Flash selected), unless otherwise noted.

Table 21 • **Current Consumption**

	+3.3 V[1]		+1.2 V[2]			
Operational Mode	**Typ.**	**Max.**	**Typ.**	**Max.**	**Units**	**Notes / Conditions**
Two-Way Audio	12		123		mA	Firmware active, 16KHz sample rate, power-saving off, 1 DAC active[3], 1 or 2 MICs active[4], LEC bypassed, HBI is active.
Low-Power Two-Way Audio	10		78			Firmware active, 16KHz sample rate, power-saving on, 1 DAC active[3], 1 or 2 MICs active[4], LEC bypassed, HBI is active.
ASR Assist	10		95			ASR Firmware active, power-saving on, 1 MIC active, DACs disabled, HBI is active
Sleep	2		3			Firmware inactive (Firmware and configuration record are retained), DACs and MICs are powered down, HBI is active.
Reset	100		0		µA	Device in reset (reset > 10 µS), DVDD12 removed[5].
Ultra-Low Power	3		0			Device in reset (reset > 10 µS), DVDD12 not present, DVDD33_XTAL held low.

1. Table values include all current entering DVDD33, AVDD33, and DVDD33_XTAL pins. Add 1.0 mA to Normal, Low-Power, and Sleep modes if the internal voltage regulator is used (EXT_SEL = VSS).
2. Core supply voltage. Table values include all current entering DVDD12 pins.
3. DAC in differential mode, for 2 DACs active in differential mode, add 3.6 mA to +3.3 V current.
4. DMIC_IN active.
5. DVDD12 is removed if the internal regulator is used for +1.2 V generation or if the VDD12_CTRL pin is used to shutdown an external +1.2 V LDO that provides DVDD12 to the ZL38063.

11.5 DC Specifications

Typical values are for T_A = 25 ºC and nominal supply voltage. Minimum and maximum values are over the industrial −40 ºC to 85 ºC temperature range and supply voltage range as shown in Operating Ranges, page 33, except as noted. A 12.000 MHz clock oscillator is active.

Table 22 • **DC Specifications**

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes / Conditions
Input high voltage	V_{IH}	0.7 × V_{DVDD33}		V_{DVDD33} + 0.3	V	All digital inputs
Input low voltage	V_{IL}	V_{VSS} − 0.3		0.3 × V_{DVDD33}	V	All digital inputs
Input hysteresis voltage	V_{HYS}	0.4			V	
Input leakage (input pins)	I_{IL}			5	µA	0 to +3.3 V
Input leakage (bi-directional pins)	I_{BL}			5	µA	0 to +3.3 V
Weak pull-up current	I_{PU}	38	63	101	µA	Input at 0 V
Weak pull-down current	I_{PD}	19	41	158	µA	Input at +3.3 V
Input pin capacitance	C_I		5		pF	
Output high voltage	V_{OH}	2.4			V	At 12 mA
Output low voltage	V_{OL}			0.4	V	At 12 mA
Output high impedance leakage	I_{OZ}			5	µA	0 to +3.3 V
Pin capacitance (output & input/tristate pins)	C_O		5		pF	
Output rise time	t_{RT}		1.25		ns	10% to 90%, C_{LOAD} = 20 pF
Output fall time	t_{FT}		1.25		ns	90% to 10%, C_{LOAD} = 20 pF

11.6 AC Specifications

For all AC specifications, typical values are for T_A = 25 ºC and nominal supply voltage. Minimum and maximum values are over the industrial −40 ºC to 85 ºC temperature range and supply voltage ranges as shown in Operating Ranges, page 33, except as noted. A 12.000 MHz clock oscillator is active with Two Way Voice Communication Firmware in Normal, Wideband operational mode.

11.6.1 Microphone Interface

Table 23 • **Microphone Interface**

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes / Conditions
Microphone clock output (DMIC_CLK),						
8 kHz, 16 kHz sample rate			1.024		MHz	
48 kHz sample rate			3.072		MHz	
DMIC_CLK, Output high current	I_{OH}		20		mA	$V_{OH} = D_{VDD33} - 0.4$ V
DMIC_CLK, Output low current	I_{OL}		30		mA	$V_{OL} = 0.4$ V
DMIC_CLK, Output rise and fall time	t_R, t_F		5		nS	$C_{LOAD} = 100$ pF

11.6.2 DAC

Measurements taken using PCM mode. THD+N versus output power for speaker drive applications presented in Figure 29, page 38; THD+N versus output voltage for amplifier drive applications presented in Figure 30, page 38.

Table 24 • **DAC**

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes / Conditions
DAC output level:						DAC gain = 1, 1 KΩ load.
Full scale: Differential	V_{DACFS}		4.8		V_{PP}	
Single-ended			2.4			
0 dBm0: Differential			2.8			
Single-ended			1.4			
PCM full scale level (V_{ppd} value)			9		dBm0	DAC gain = 1, 600 Ω load
DAC output power:						1, Single-ended loads driven capacitively to ground
Single-ended, 32 ohm load			20.6	24	mW	
Single-ended, 16 ohm load			37.5	47		
Differential, 32 ohm load			86.0	94		
Frequency response: Sample rate = 48 kS/s	f_R	20		20000	Hz	1, 3 dB cutoff includes external AC coupling, without AC coupling the response is low pass.
Dynamic range: Sample rate = 48 kS/s			92		dBFS	20 Hz – 20 kHz
Total harmonic distortion plus noise	THD + N		−82		dBFS	2, Input = −3 dBFS.
Signal to Noise Ratio	SNR		85		dB	2,1004 Hz, C-message weighted
Allowable capacitive load to ground	C_L			100	pF	1, At each DAC output.
Power supply rejection ratio	PSRR		70		dB	1, 20 Hz - 100 kHz, 100 mVpp supply noise.

Table 24 • **DAC *(continued)***

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes / Conditions
Crosstalk			−85	−70	dB	1, Between DAC outputs.

1. Guaranteed by design, not tested in production.
2. Single-ended or differential output.

Figure 29 • **THD+N Ratio versus Output Power – Driving Low Impedance**

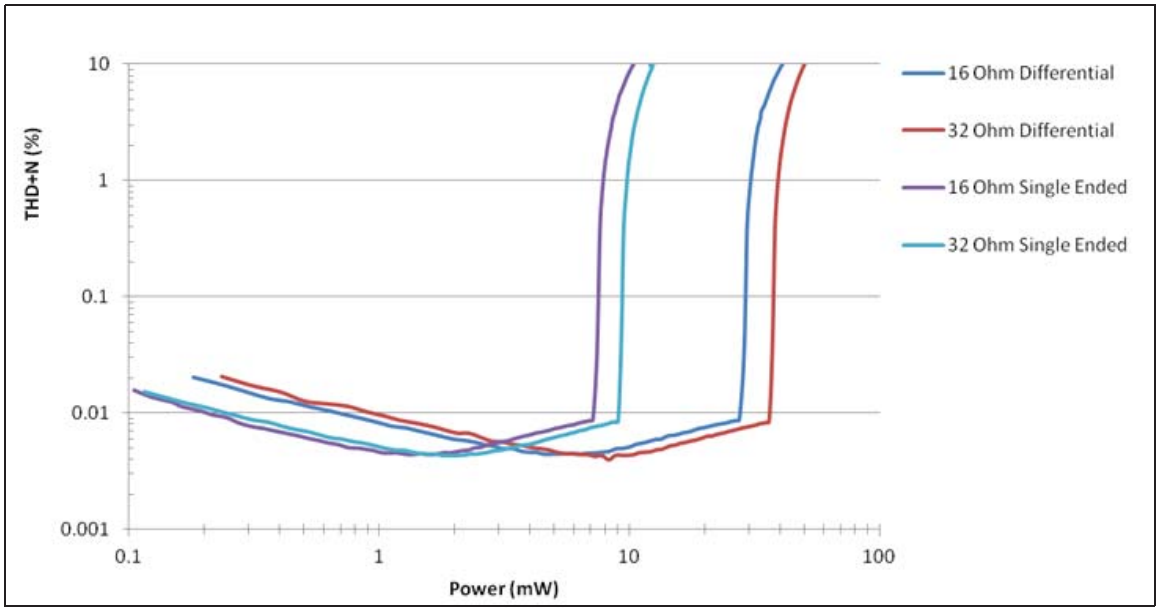
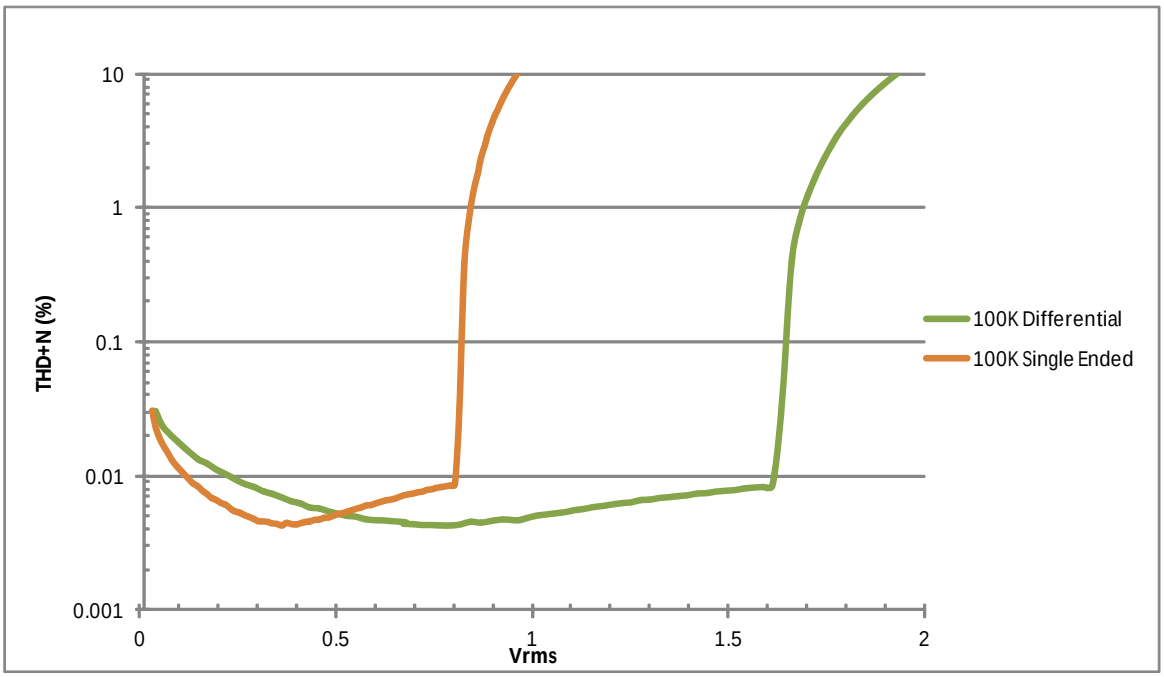


Figure 30 • **THD+N Ratio versus V_{RMS} – Driving High Impedance**



11.7 External Clock Requirements

In all modes of operation the ZL38063 requires an external clock source. The external clock drives the device's internal PLL which is the source for the internal timing signals.

The external clock source can either be:

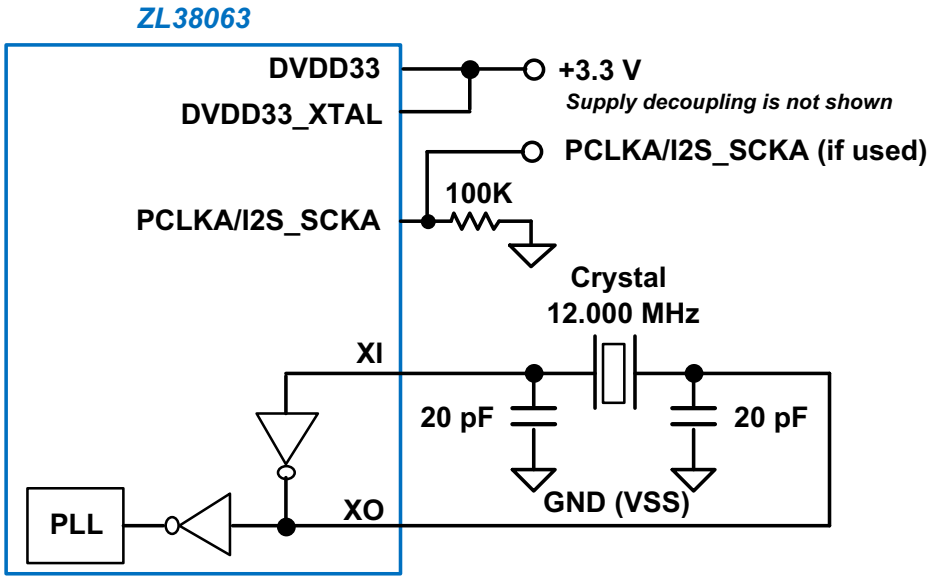
- 12.000 MHz crystal, or
- 12.000 MHz clock oscillator with a 2.5 V output

The following three sections discuss these options.

11.7.1 Crystal Application

The oscillator circuit that is created across pins XI and XO requires an external fundamental mode crystal that has a specified parallel resonance (f_P) at 12.000 MHz.

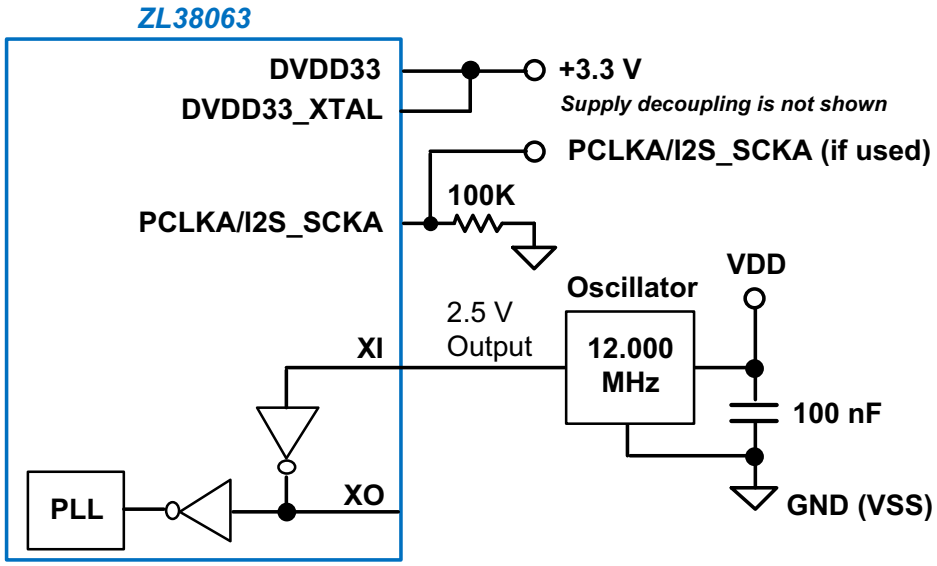
Figure 31 • **Crystal Application Circuit**



11.7.2 Clock Oscillator Application

Figure 32, page 40 illustrates the circuit that is used when the ZL38063 external clock source is a clock oscillator. The oscillator pins are 2.5 V compliant and should not be driven from 3.3 V CMOS without a level shifter or voltage attenuator.

Figure 32 • **Clock Oscillator Application Circuit**



11.7.3 AC Specifications - External Clocking Requirements

These specifications apply to crystal and clock oscillator external clocking.

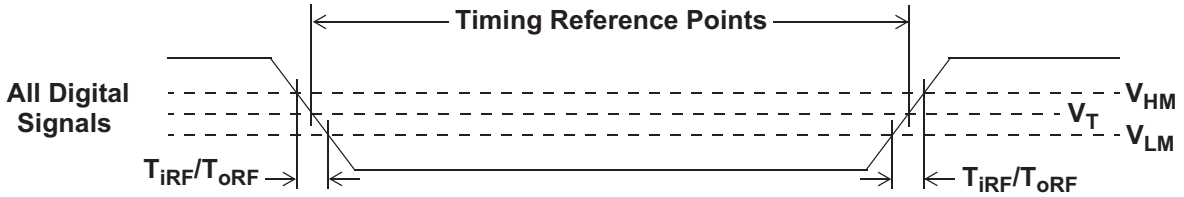
Table 25 • **AC Specifications – External Clocking Requirement**

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes / Conditions
External clocking frequency accuracy	A_{OSC}	−50		50	ppm	Not tested in production.
External clocking duty cycle	DC_{OSC}	40		60	%	
Holdover accuracy				50	ppm	

12 Timing Characteristics

Figure 33 depicts the timing reference points that apply to the timing diagrams shown in this section. For all timing characteristics, typical values are for T_A = 25 °C and nominal supply voltage. Minimum and maximum values are over the industrial −40 °C to 85 °C temperature range and supply voltage ranges as shown in Operating Ranges, page 33, except as noted.

Figure 33 • **Timing Parameter Measurement Digital Voltage Levels**



12.1 TDM Interface Timing Parameters

All TDM timing parameters are with Two Way Voice Communication Firmware running.

12.1.1 GCI and PCM Timing Parameters

Specifications for GCI and PCM timing modes are presented in the following table. The specifications apply to both port A and port B in slave operation.

A timing diagram that applies to GCI timing of the TDM interface is illustrated in Figure 34, page 42.

Timing diagrams that apply to PCM timing of the TDM interface are illustrated in Figure 35, page 43 and Figure 36, page 43.

Table 26 • **GCI and PCM Timing Parameters**

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes / Conditions
PCLK period	t_{PCY}		122	7812.5	nS	1, 2
PCLK High pulse width	t_{PCH}		48			2
PCLK Low pulse width	t_{PCL}		48			2
Fall time of clock	t_{PCF}			8		
Rise time of clock	t_{PCR}			8		
FS delay (output rising or falling)	t_{FSD}		2	15		2
			2	25		3
FS setup time (input)	t_{FSS}		5			4
FS hold time (input)	t_{FSH}		0.5	125000 − $2t_{PCY}$		4
Data output delay	t_{DOD}		2	15		2
			2	25		3
Data output delay to High-Z	t_{DOZ}		0	10		5
Data input setup time	t_{DIS}		5			4
Data input hold time	t_{DIH}		0			4
Allowed PCLK jitter time	t_{PCT}			20		Peak-to-peak
Allowed Frame Sync jitter time	t_{FST}			20		Peak-to-peak

1. PCLK frequency must be within 100 ppm.
2. C_{LOAD} = 40 pF
3. C_{LOAD} = 150 pF
4. Setup times based on 2 ns PCLK rise and fall times; hold times based on 0 ns PCLK rise and fall times.
5. Guaranteed by design, not tested in production.

Figure 34 • **GCI Timing, 8-bit**

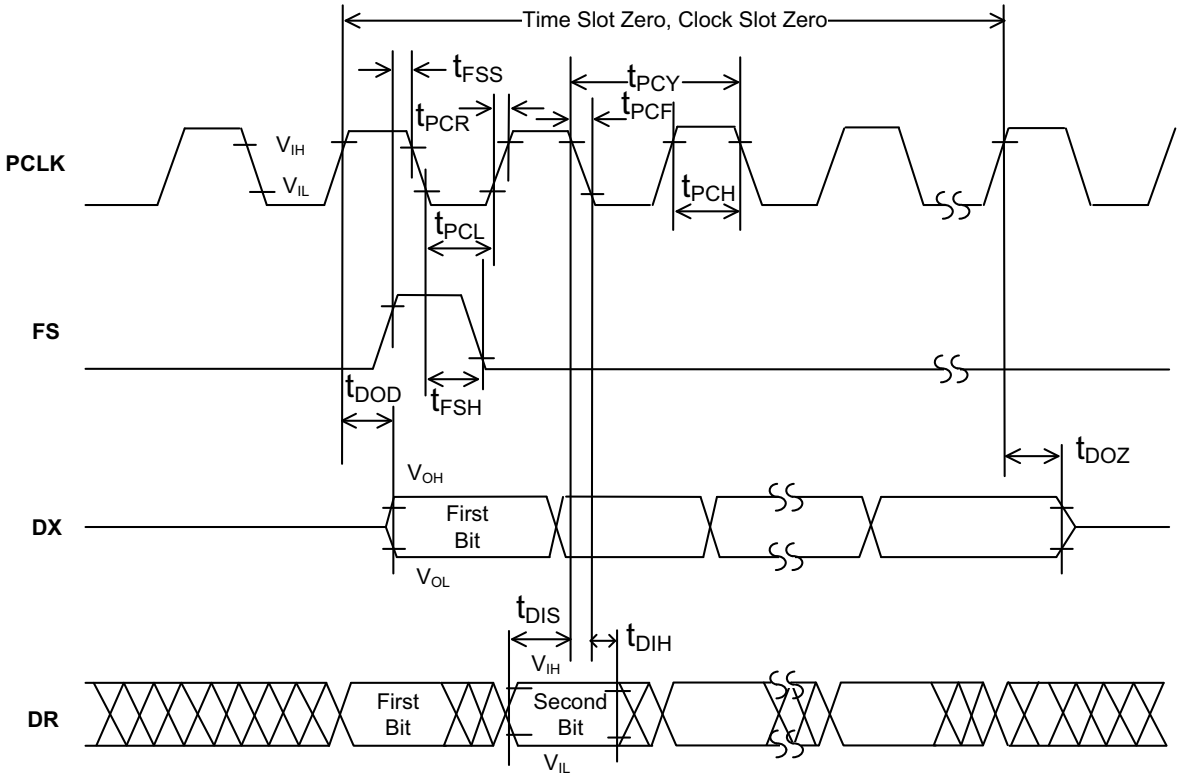


Figure 35 • **PCM Timing, 8-bit with xeDX = 0 (Transmit on Negative PCLK Edge)**

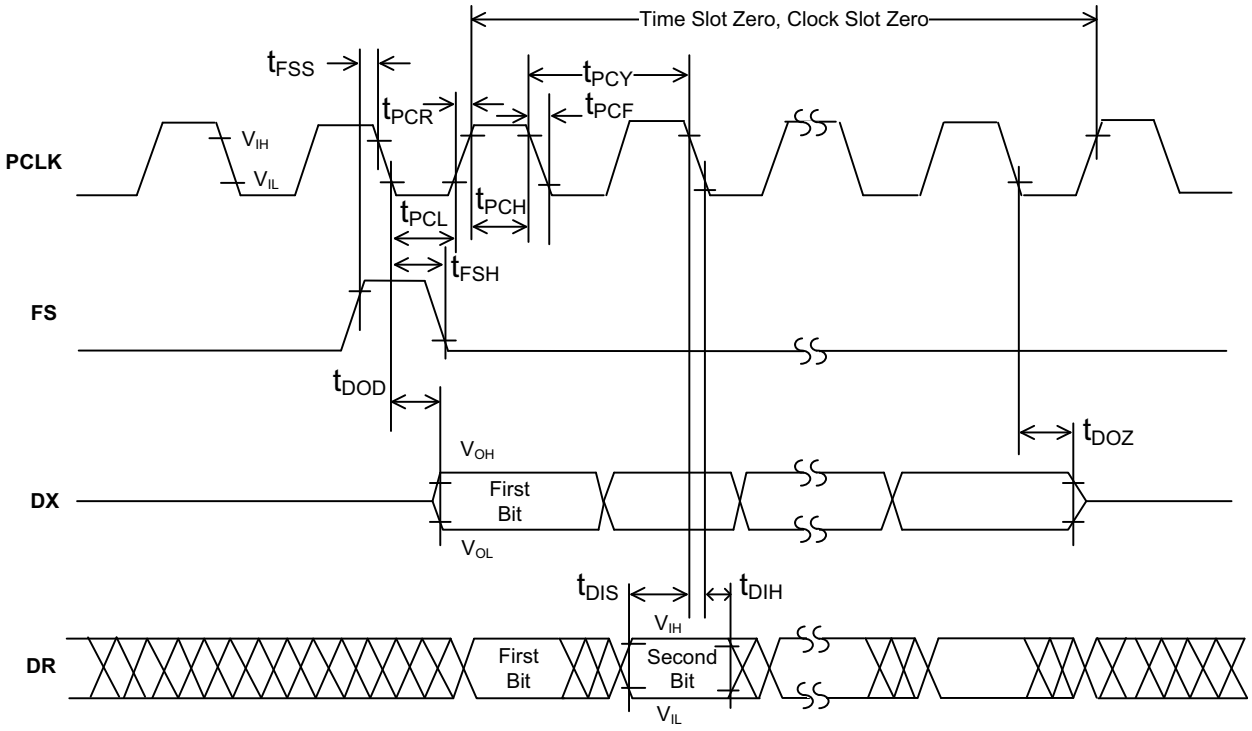
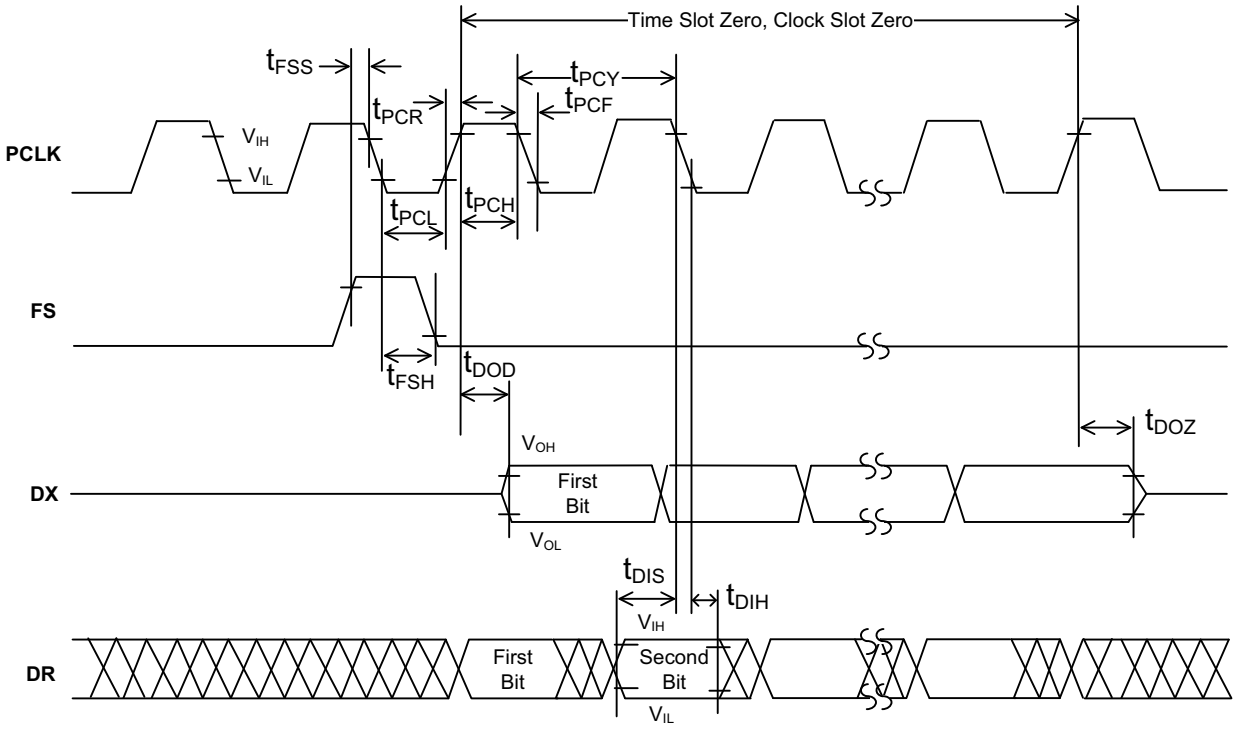


Figure 36 • **PCM Timing, 8-bit with xeDX = 1 (Transmit on Positive PCLK Edge)**



12.1.2 I²S Timing Parameters

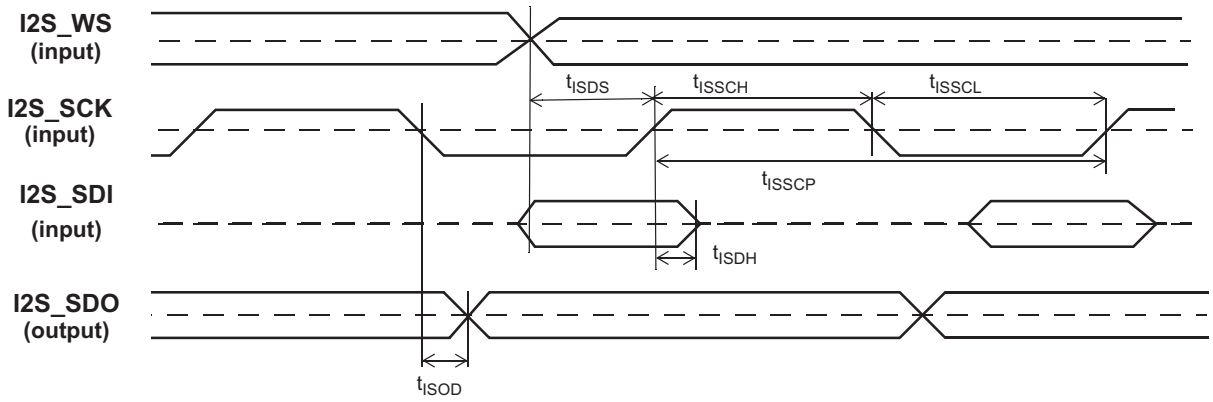
12.1.2.1 I²S Slave

Specifications for I²S Slave timing are presented in the following table. The specifications apply to both port A and port B. A timing diagram for the I²S Slave timing parameters is illustrated in Figure 37, page 44.

Table 27 • **I²S Slave Timing Specifications**

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes / Conditions
I2S_SCK Clock Period						
f_s = 48 kHz	t_{ISSCP}		651.04		ns	
f_s = 8 kHz			3.91		µs	
I2S_SCK Pulse Width High						
f_s = 48 kHz	t_{ISSCH}	292.97		358.07	ns	
f_s = 8 kHz		1.76		2.15	µs	
I2S_SCK Pulse Width Low						
f_s = 48 kHz	t_{ISSCL}	292.97		358.07	ns	
f_s = 8 kHz		1.76		2.15	µs	
I2S_SDI Setup Time	t_{ISDS}	5			ns	
I2S_WS Setup Time	t_{ISDS}	5			ns	
I2S_SDI Hold Time	t_{ISDH}	0			ns	
I2S_WS Hold Time	t_{ISDH}	0.5			ns	
I2S_SCK Falling Edge to I2S_SDO Valid	t_{ISOD}	2		15	ns	C_{LOAD} = 40 pF

Figure 37 • **Slave I²S Timing**



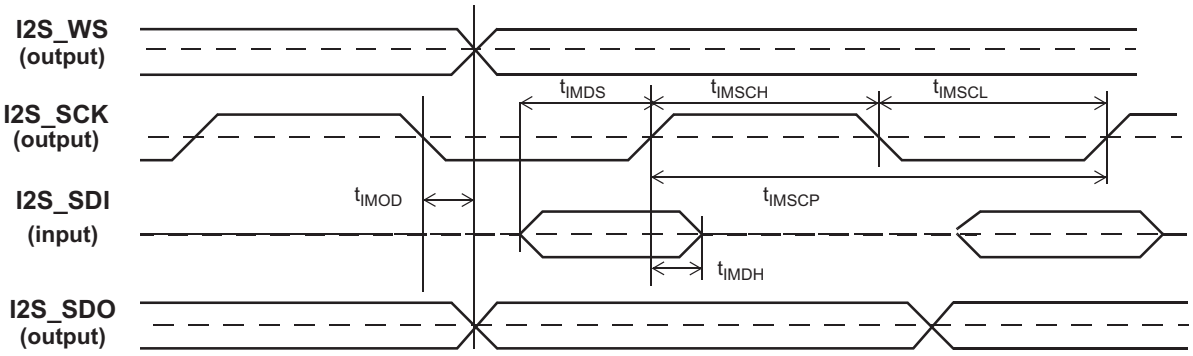
12.1.2.2 I²S Master

Specifications for I²S Master timing are presented in the following table. The specifications apply to both port A and port B. A timing diagram for the I²S Master timing parameters is illustrated in Figure 38.

Table 28 • **I²S Master Timing Specifications**

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes / Conditions
I2S_SCK Clock Period						
f_s = 48 kHz	t_{IMSCP}		651.04		ns	
f_s = 8 kHz			3.91		µs	
I2S_SCK Pulse Width High						
f_s = 48 kHz	t_{IMSCH}	318.0		333.0	ns	
fs = 8 kHz		1.95		1.96	µs	
I2S_SCK Pulse Width Low						
f_s = 48 kHz	t_{IMSCL}	318.0		333.0	ns	
f_s = 8 kHz		1.95		1.96	µs	
I2S_SDI Setup Time	t_{IMDS}	5			ns	
I2S_SDI Hold Time	t_{IMDH}	0			ns	
I2S_SCK Falling Edge to I2S_WS	t_{IMOD}	2		15	ns	C_{LOAD} = 40 pF
I2S_SCK Falling Edge to I2S_SDO Valid	t_{IMOD}	2		15	ns	C_{LOAD} = 40 pF

Figure 38 • **Master I²S Timing**



12.2 Host Bus Interface Timing Parameters

The HBI is the main communication port from the host processor to the ZL38063, this port can read and write all of the memory and registers on the ZL38063. The port can be configured as SPI Slave or I²C Slave.

For fastest command and control operation, use the SPI Slave configuration. The SPI Slave can be operated with HCLK speeds up to 25 MHz; the I²C Slave will operate with HCLK speeds up to 400 kHz.

12.2.1 SPI Slave Port Timing Parameters

The following table describes timing specific to the ZL38063 device. A timing diagram for the SPI Slave timing parameters is illustrated in Figure 39, page 47.

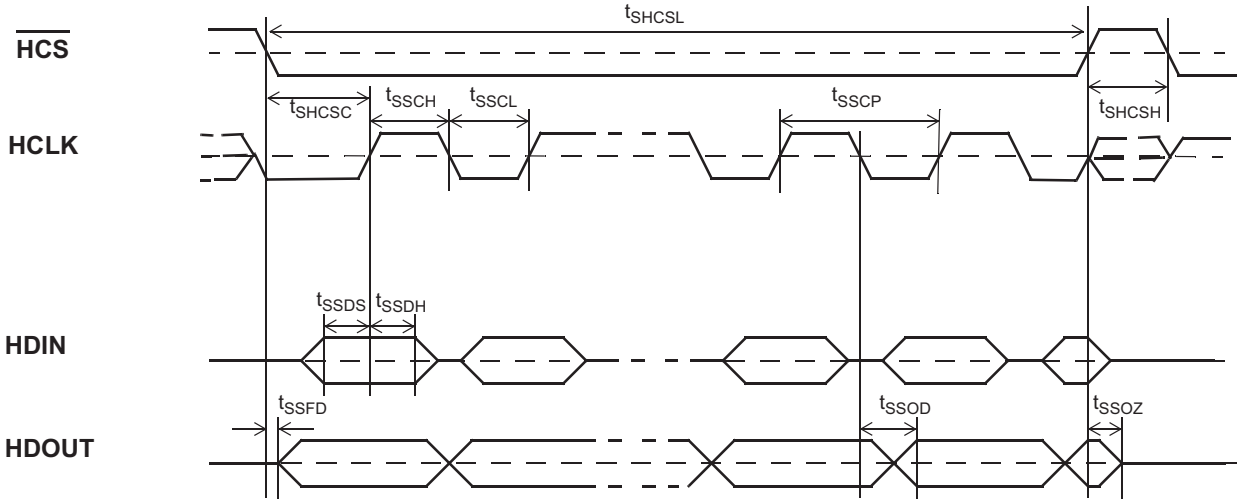
For seamless control operation, both the SPI Slave timing and the system timing need to be considered when operating the SPI Slave at high speeds. System timing includes host set-up and delay times and board delay times.

Table 29 • **SPI Slave Port Timing Parameters**

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes / Conditions
HCLK Clock Period	t_{SSCP}	40			ns	
HCLK Pulse Width High	t_{SSCH}	16	$t_{SSCP}/2$			1
HCLK Pulse Width Low	t_{SSCL}	16	$t_{SSCP}/2$			1
HDIN Setup Time	t_{SSDS}	5				
HDIN Hold Time	t_{SSDH}	0				
$\overline{HCS}$ Asserted to HCLK Rising Edge:						
Write	t_{SHCSC}	5	$t_{SSCP}/2$			
Read if host samples on falling edge		5	$t_{SSCP}/2$			
Read if host samples on rising edge		t_{SSFD} + host HDOUT setup time to HCLK	t_{SSFD} + $t_{SSCP}/2$			
HCLK Driving Edge to HDOUT Valid	t_{SSOD}	2		15		C_{LOAD} = 40 pF
$\overline{HCS}$ Falling Edge to HDOUT Valid	t_{SSFD}	0		15		2, C_{LOAD} = 40 pF
$\overline{HCS}$ De-asserted to HDOUT Tristate	t_{SSOZ}	0		10		5, C_{LOAD} = 40 pF
$\overline{HCS}$ Pulse High	t_{SHCSH}	20	$t_{SSCP}/2$			1, 3
$\overline{HCS}$ Pulse low	t_{SHCSL}					4

1. HCLK may be stopped in the high or low state indefinitely without loss of information. When $\overline{HCS}$ is at low state, every 16 HCLK cycles, the 16-bit received data will be interpreted by the SPI interface logic.
2. The first data bit is enabled on the falling edge of $\overline{HCS}$ or on the falling edge of HCLK, whichever occurs last.
3. The SPI Slave requires 61 ns $\overline{HCS}$ off time just to make the transition of $\overline{HCS}$ synchronized with HCLK clock. In the command framing mode, there is no $\overline{HCS}$ off time between each 16-bit command/data, and $\overline{HCS}$ is held low until the end of command.
4. If $\overline{HCS}$ is not held low for 8 or 16 HCLK cycles exactly, the SPI Slave will reset. During byte or word framing mode, $\overline{HCS}$ is held low for the whole duration of the command. Multiple commands can be transferred with $\overline{HCS}$ low for the whole duration of the multiple commands. The rising edge of the $\overline{HCS}$ indicates the end of the command sequence and resets the SPI Slave.
5. Guaranteed by design, not tested in production.

Figure 39 • **SPI Slave Timing**



12.2.2 I²C Slave Interface Timing Parameters

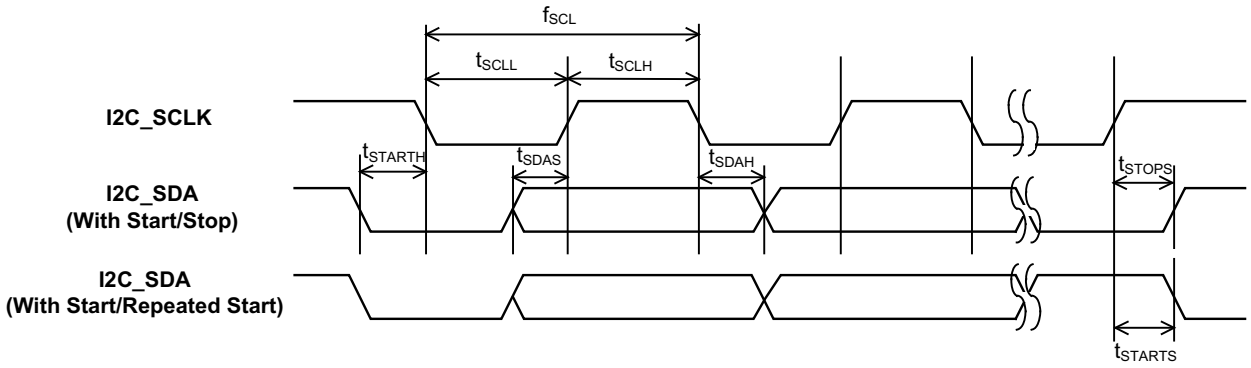
The I²C interface uses the SPI Slave interface pins.

Specifications for I²C interface timing are presented in the following table. A timing diagram for the I²C timing parameters is illustrated in Figure 40, page 48.

Table 30 • **I²S Slave Timing Specifications**

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes / Conditions
SCLK Clock Frequency	f_{SCL}	0		400	kHz	
START Condition Hold Time	t_{STARTH}	0.6			µs	
SDA data setup time	t_{SDAS}	100			ns	
SDA Hold Time Input	t_{SDAH}	100			ns	
SDA Hold Time Output	t_{SDAH}	300			ns	
High period of SCLK	t_{SCLH}	0.6			µs	
Low period of SCLK	t_{SCLL}	1.3			µs	
STOP Condition Setup Time	t_{STOPS}	0.6			µs	
Repeated Start Condition Setup Time	t_{STARTS}	0.6			µs	
Pulse Width Spike Suppression, glitches ignored by input filter	t_{SP}	50			ns	

Figure 40 • **I²C Timing Parameter Definitions**



12.3 UART Timing Parameters

Specifications for UART timing are presented in the following table. Timing diagrams for the UART timing parameters are illustrated in Figure 41 and Figure 42..

Table 31 • **UART Timing Specifications**

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes / Conditions
UART_RX and UART_TX bit width Baud rate = 115.2 kbps	t_{UP}		8.68		µs	
Allowed baud rate deviation 8 bits with no parity				4.86	%	Guaranteed by design, not tested in production.

Figure 41 • **UART_RX Timing**

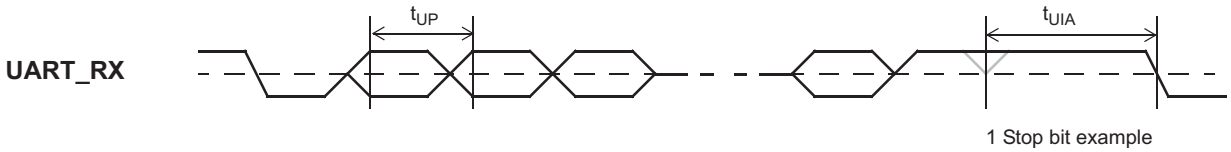
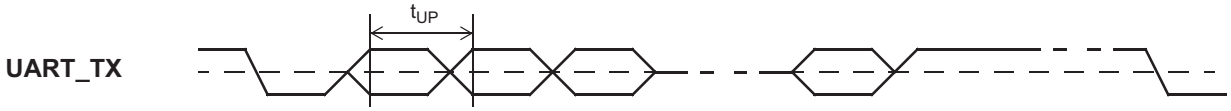


Figure 42 • **UART_TX Timing**



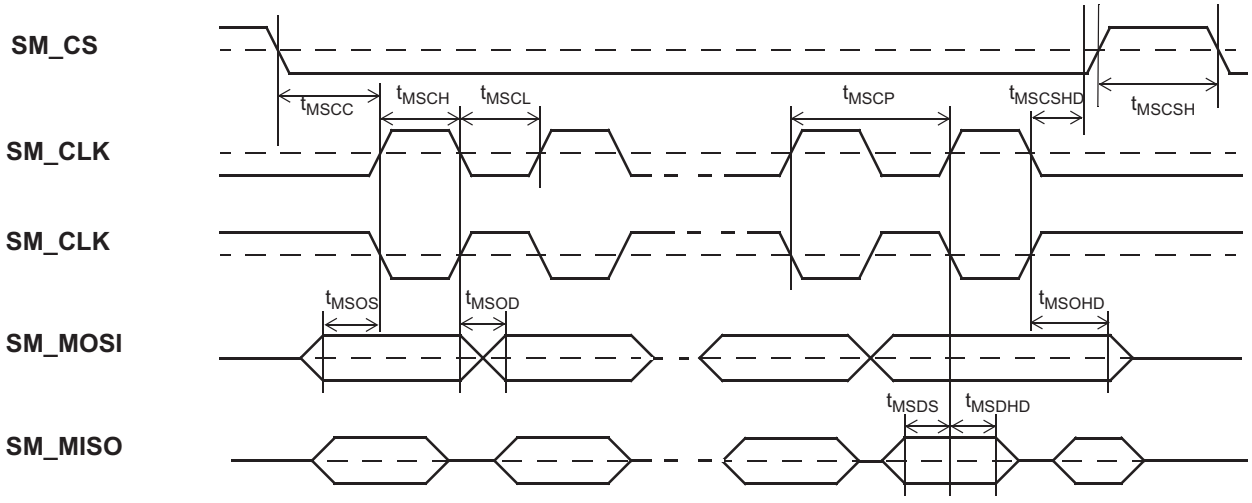
12.4 Master SPI Timing Parameters

Specifications for Master SPI timing are presented in the following table. A timing diagram for the Master SPI timing parameters is illustrated in Figure 43.

Table 32 • **Master SPI Timing Specifications**

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes / Conditions
SM_CLK Clock Period	t_{MSCP}	40		320	ns	Max. 25.0 MHz
SM_CLK Pulse Width High	t_{MSCH}	$(t_{MSCP}/2) - 2$		160		
SM_CLK Pulse Width Low	t_{MSCL}	$(t_{MSCP}/2) - 2$		160		
SM_MISO Setup Time	t_{MSDS}	3				
SM_MISO Hold Time	t_{MSDHD}	0				
SM_CS Asserted to SM_CLK Sampling Edge	t_{MSCC}	$(t_{MSCP}/2) - 4$				
SM_CLK Driving Edge to SM_MOSI Valid	t_{MSOD}	−1		2		C_{LOAD} = 40 pF
SM_MOSI Setup to SM_CLK Sampling Edge	t_{MSOS}	$(t_{MSCP}/2) - 4$				C_{LOAD} = 40 pF
SM_MOSI Hold Time to SM_CLK Sampling Edge	t_{MSOHD}	$(t_{MSCP}/2) - 4$				C_{LOAD} = 40 pF
SM_CS Hold Time after last SM_CLK Sampling Edge	t_{MSCSHD}	$(t_{MSCP}/2) - 4$				
SM_CS Pulse High	t_{MSCSH}	$(t_{MSCP}/2) - 2$				

Figure 43 • **Master SPI Timing**



13 AEC Tuning

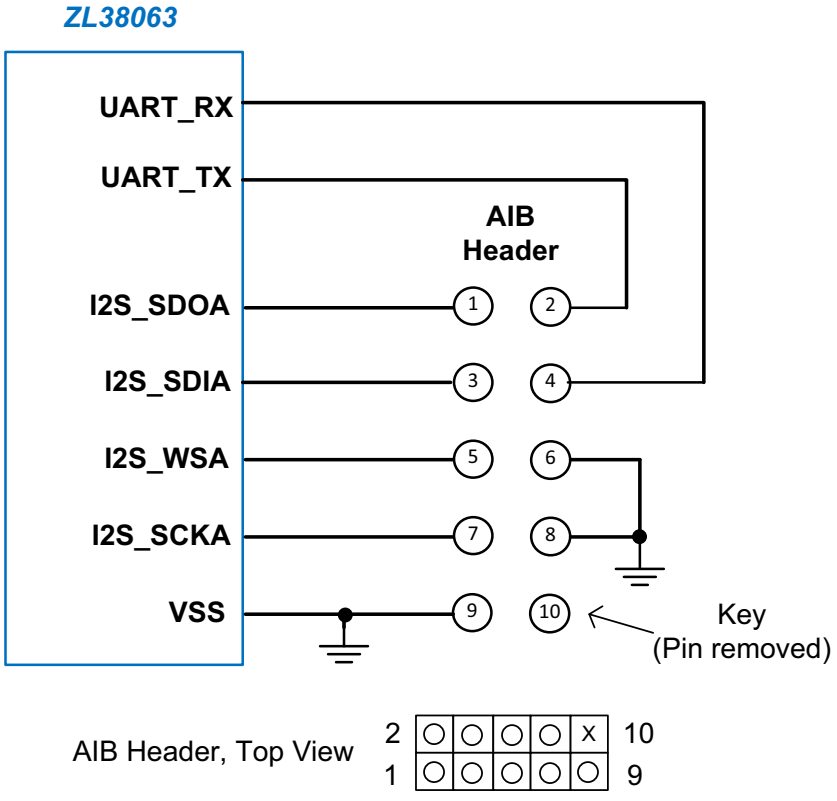
To optimize the acoustic properties of a given system design, the Audio Processor firmware requires gain and level tuning. The mechanical design, including the speaker and microphone quality and placement, will all affect the system's acoustic performance. Microsemi has developed *MiTuner*™ GUI Software (ZLS38508) and the Microsemi Audio Interface Box (AIB) Evaluation Kit (ZLE38470BADA) to automatically optimize the firmware's tunable parameters for a given hardware design, facilitating the system design process and eliminating the need for tedious manual tuning. In order to achieve a high level of acoustic performance for a given enclosure, the MiTuner GUI Software performs both Auto Tuning and Subjective Tuning.

Access to the UART and TDM port of the ZL38063 need to be provided on the system board in order to perform Auto Tuning or Subjective Tuning with the ZLS38508 software. Figure 44 shows the nodes that need to be made available and illustrates an AIB Header that when mounted, will provide a direct connection to the Audio Interface Box cable (no soldering or jumpers required). TDM port A is shown, but port B can be used instead. The header only needs to be populated on the system board(s) that are used for tuning evaluation.

Note: Any connections to a host processor need to be isolated from the UART and I^2S ports during the tuning process. If a host processor is connected to these ports, a resistor should be placed between the host and each ZL38063 port signal, so that the resistor can be removed to isolate the host from the ZL38063 without interfering with the ZL38063's connection to the AIB.

To interface between the header and the AIB, a 10-wire ribbon cable is used. The cable is terminated on both ends with a double row, 5 position, 100 mil (2.54 mm) female socket strip. Pin 10 on each socket is keyed to ensure proper signal connection. On the system board header pin 10 must be removed, or alternatively both pins 9 and 10 can be eliminated to reduce the space needed on the system board. Signal integrity series termination resistors are provided for the interface in the AIB.

Figure 44 • **AIB System Board Connection**



Note: A Samtec TSW-105-07-L-D through-hole terminal strip, or a Samtec TSM-105-01-L-DV surface mount terminal strip, or a suitable equivalent can be used for the AIB Header. The header is a double row, 5 position, 10-pin male 100 mil (2.54 mm) unshrouded terminal strip with 25 mil (0.64 mm) square vertical posts that are 230 mils (5.84 mm) in length.

14 Package Outline Drawings

14.1 Package Drawings

Figure 45 • **64-Pin QFN**

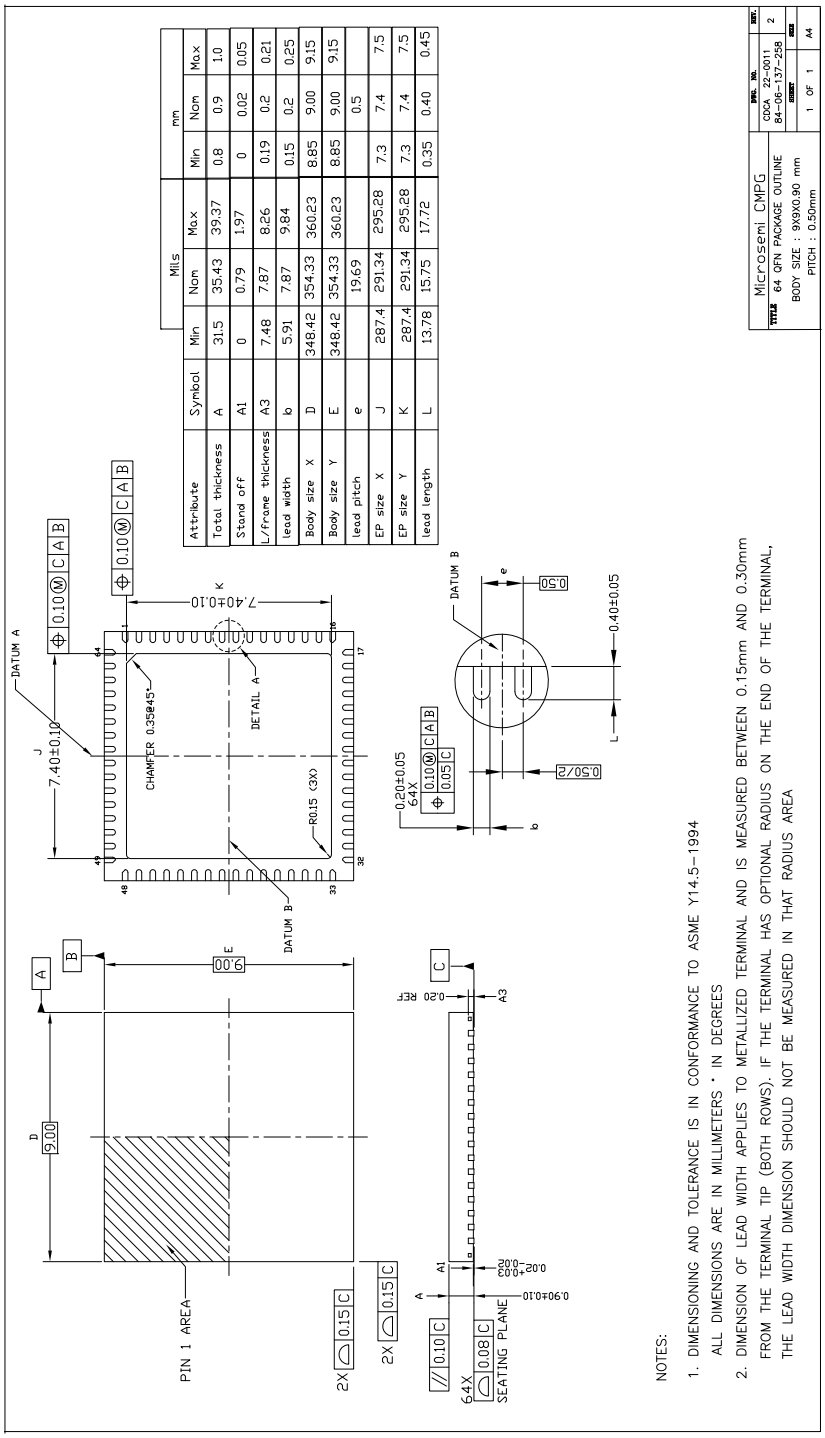
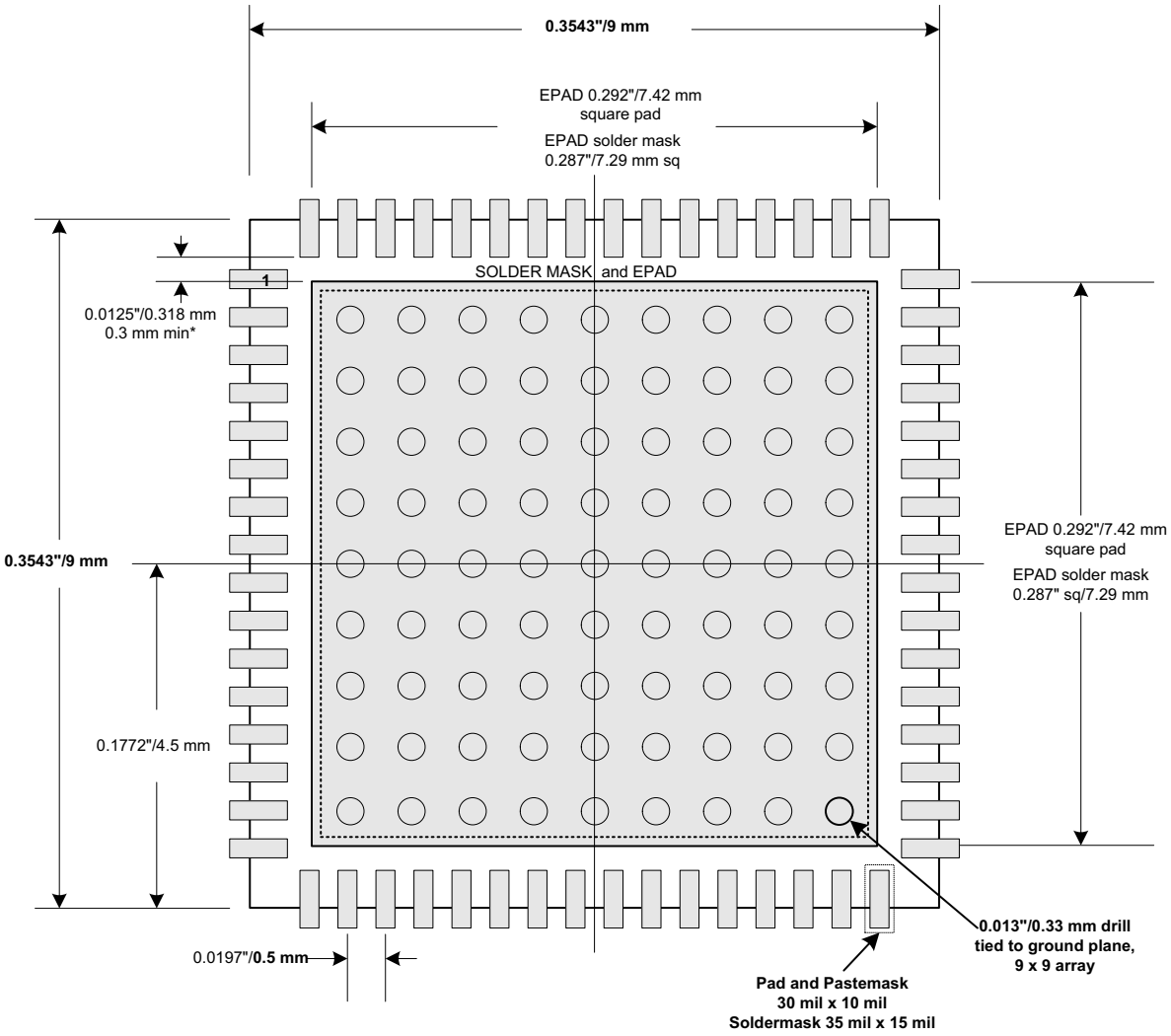


Figure 46 • **Recommended 64-Pin QFN Land Pattern – Top View**

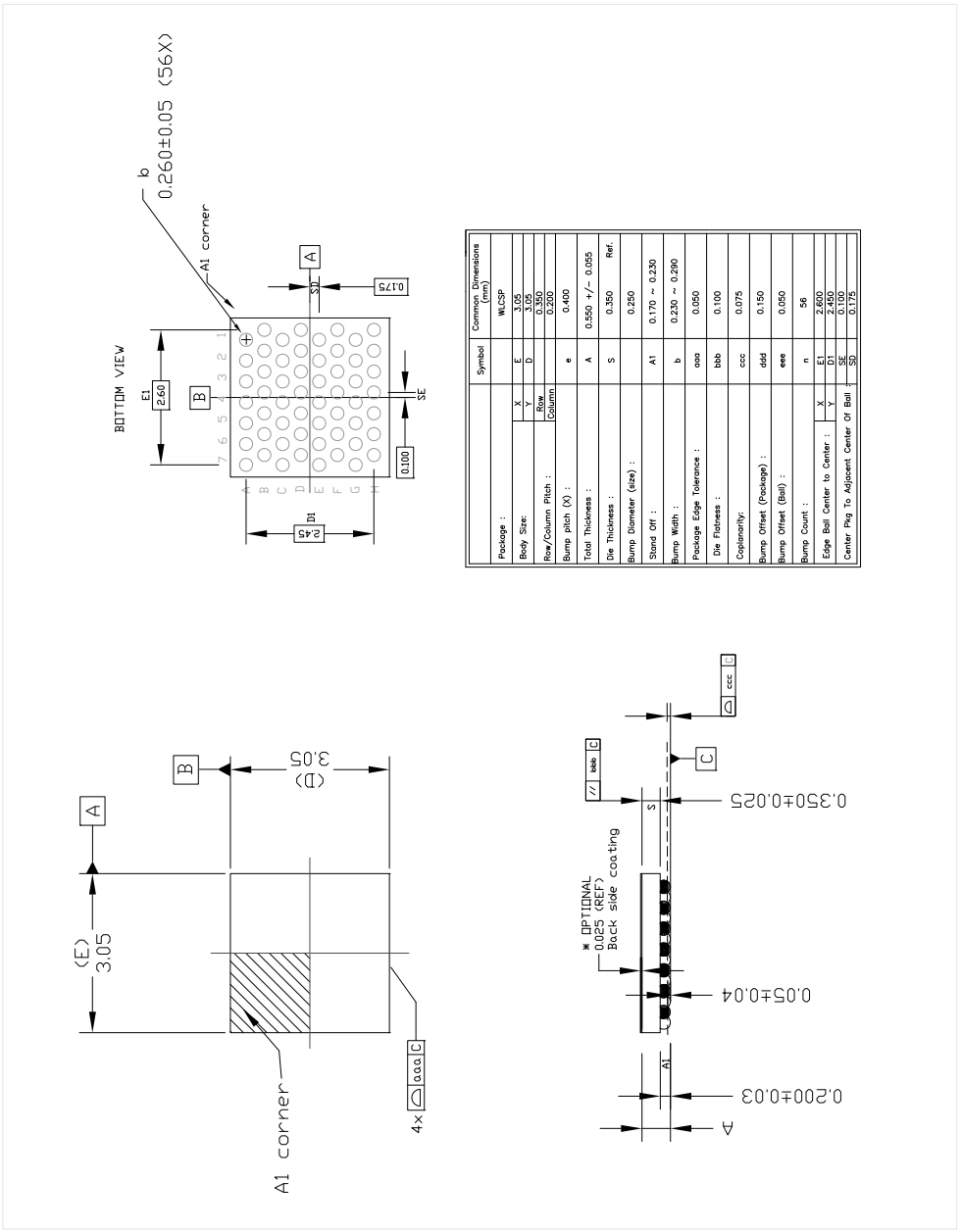


64-QFN
9 mm x 9 mm, 0.5 mm pitch

* Minimum spacing between pins and epad must be 0.3 mm

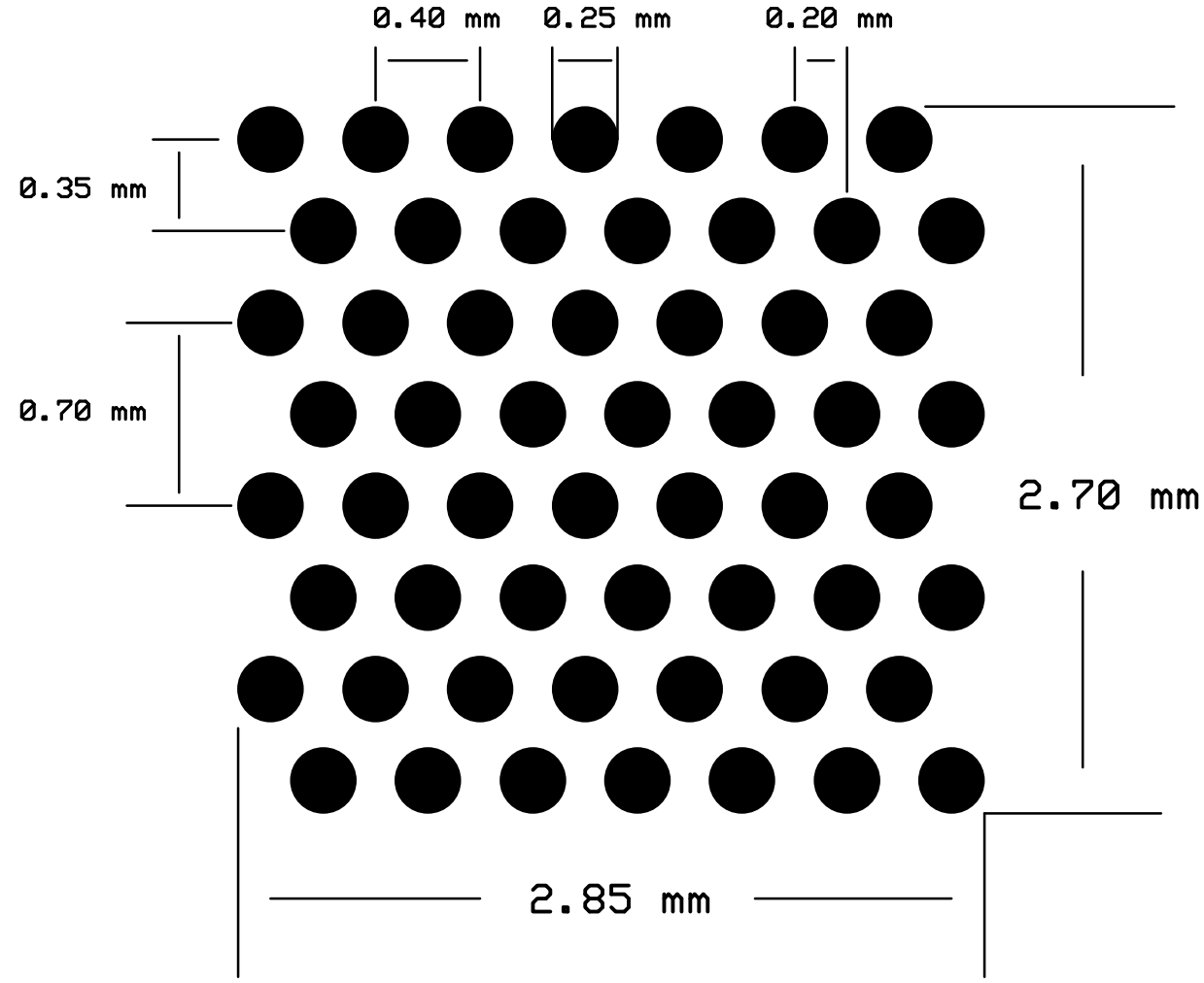
Recommended EPAD configuration uses 0.292"/7.42 mm square pad tied to a ground plane with a 9 x 9 array of 0.013"/0.33 mm vias. This is necessary for good thermal performance.

Figure 47 • **56-Ball WLCSP**



Symbol		Common Dimensions (mm)
Package :		WLCSP
Body Size:	X	E 3.05
	Y	D 3.05
Row/Column Pitch :	Row	0.350
	Column	0.200
Bump pitch (X) :	e	0.400
Total Thickness :	A	0.550 +/- 0.055
Die Thickness :	S	0.350 Ref.
Bump Diameter (size) :		0.250
Stand Off :	A1	0.170 ~ 0.230
Bump Width :	b	0.230 ~ 0.290
Package Edge Tolerance :	aaa	0.050
Die Flatness :	bbb	0.100
Coplanarity:	ccc	0.075
Bump Offset (Package) :	ddd	0.150
Bump Offset (Ball) :	eee	0.050
Bump Count :	n	56
Edge Ball Center to Center :	X E1	2.600
	Y D1	2.450
Center Pkg To Adjacent Center Of Ball :	SE	0.100
	SD	0.175

Figure 48 • **56-Ball WLCSP Staggered Balls Expanded Bottom View**



Ball Diameter -- 0.25 mm

Pitch:

Horizontal -- 0.40 mm

Vertical -- 0.35 mm

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