

## Features

### Inputs/Outputs

- Accepts two differential or single-ended inputs
  - LVPECL, LVDS, CML, HCSL, LVCMOS
- Eight precision LVDS outputs
- Operating frequency up to 750 MHz

### Power

- Option for 2.5 V or 3.3 V power supply
- Current consumption of 113 mA
- On-chip Low Drop Out (LDO) Regulator for superior power supply rejection

### Performance

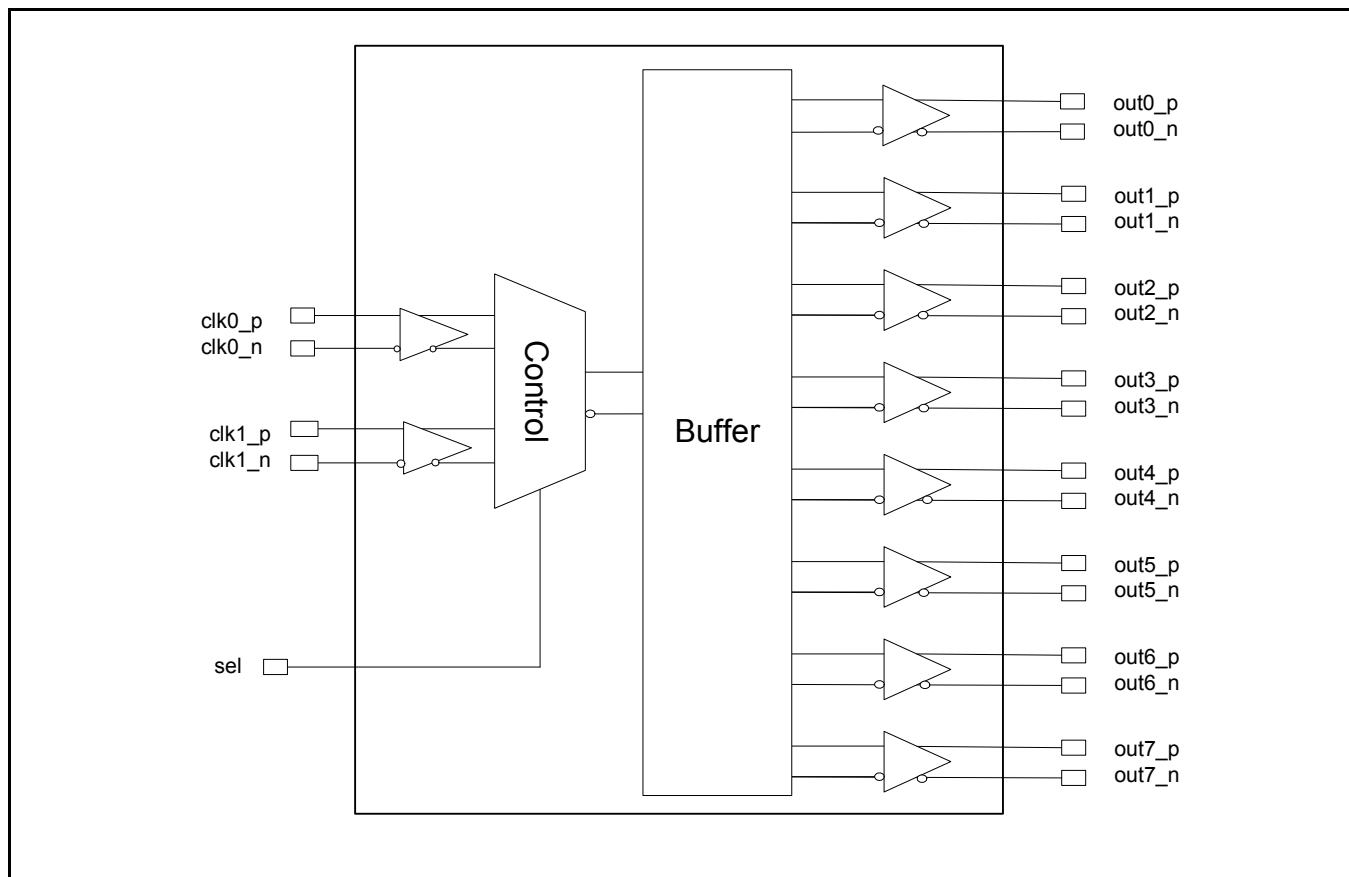
- Ultra low additive jitter of 104 fs RMS

### Ordering Information

|                        |            |               |
|------------------------|------------|---------------|
| ZL40226LDG1            | 32 Pin QFN | Trays         |
| ZL40226LDF1            | 32 Pin QFN | Tape and Reel |
| Matte Tin              |            |               |
| Package size: 5 x 5 mm |            |               |
| <b>-40°C to +85°C</b>  |            |               |

## Applications

- General purpose clock distribution
- Low jitter clock trees
- Logic translation
- Clock and data signal restoration
- Redundant clock distribution
- Wired communications: OTN, SONET/SDH, GE, 10 GE, FC and 10G FC
- Wireless communications
- High performance micro-processor clock distribution



**Figure 1 - Functional Block Diagram**

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## Table of Contents

|   |           |
|---|-----------|
| <b>Features</b> .....                                 | <b>1</b>  |
| Inputs/Outputs .....                                  | 1         |
| Power .....   | 1         |
| Performance .....                                     | 1         |
| <b>Applications</b> .....                             | <b>1</b>  |
| <b>1.0 Package Description</b> .....                  | <b>4</b>  |
| <b>2.0 Pin Description</b> .....                      | <b>5</b>  |
| <b>3.0 Functional Description</b> .....               | <b>6</b>  |
| 3.1 Clock Input Selection .....                       | 6         |
| 3.2 Clock Input Termination .....                     | 6         |
| 3.3 Clock Outputs .....                               | 11        |
| 3.4 Device Additive Jitter .....                      | 14        |
| 3.5 Power Supply .....                                | 15        |
| 3.5.1 Sensitivity to power supply noise .....         | 15        |
| 3.5.2 Power supply filtering .....                    | 15        |
| 3.5.3 PCB layout considerations .....                 | 15        |
| <b>4.0 AC and DC Electrical Characteristics</b> ..... | <b>16</b> |
| <b>5.0 Performance Characterization</b> .....         | <b>18</b> |
| <b>6.0 Typical Behavior</b> .....                     | <b>19</b> |
| <b>7.0 Package Characteristics</b> .....              | <b>20</b> |
| <b>8.0 Mechanical Drawing</b> .....                   | <b>21</b> |

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## List of Figures

|   |    |
|---|----|
| Figure 1 - Functional Block Diagram . . . . .                                     | 1  |
| Figure 2 - Pin Connections . . . . .  | 4  |
| Figure 3 - LVPECL Input DC Coupled Thevenin Equivalent . . . . .                  | 6  |
| Figure 4 - LVPECL Input DC Coupled Parallel Termination . . . . .                 | 7  |
| Figure 5 - LVPECL Input AC Coupled Termination . . . . .                          | 7  |
| Figure 6 - LVDS Input DC Coupled . . . . .  | 8  |
| Figure 7 - LVDS Input AC Coupled . . . . .  | 8  |
| Figure 8 - CML Input AC Coupled . . . . .   | 9  |
| Figure 9 - HCSL Input AC Coupled . . . . .  | 9  |
| Figure 10 - CMOS Input DC Coupled Referenced to VDD/2 . . . . .                   | 10 |
| Figure 11 - CMOS Input DC Coupled Referenced to Ground . . . . .                  | 10 |
| Figure 12 - Simplified LVDS Output Driver . . . . .                               | 11 |
| Figure 13 - LVDS DC Coupled Termination (Internal Receiver Termination) . . . . . | 11 |
| Figure 14 - LVDS DC Coupled Termination (External Receiver Termination) . . . . . | 12 |
| Figure 15 - LVDS AC Coupled Termination . . . . .                                 | 12 |
| Figure 16 - LVDS AC Output Termination for CML Inputs . . . . .                   | 13 |
| Figure 17 - Additive Jitter . . . . .   | 14 |
| Figure 18 - Decoupling Connections for Power Pins . . . . .                       | 15 |
| Figure 19 - Differential Voltage Parameter . . . . .                              | 17 |
| Figure 20 - Input To Output Timing . . . . .                                      | 17 |

### 1.0 Package Description

The device is packaged in a 32 pin QFN

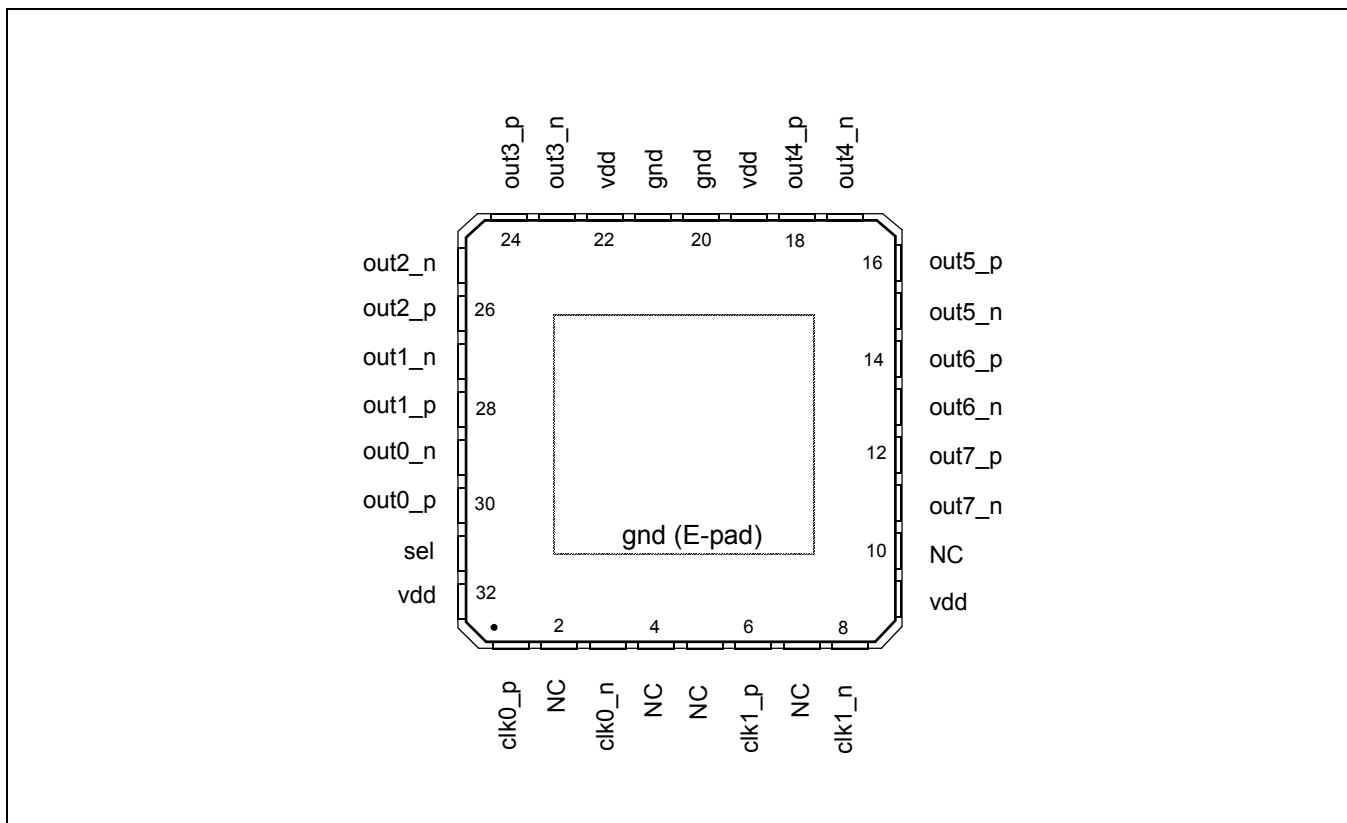


Figure 2 - Pin Connections

## 2.0 Pin Description

| Pin #   | Name   | Description   |
|---|--|---|
| 1,3,<br>6, 8  | clk0_p, clk0_n,<br>clk1_p, clk1_n  | <b>Differential Input (Analog Input).</b> Differential (or singled ended) input signals. For all input signal configuration see Section 3.2, "Clock Input Termination". |
| 30, 29,<br>28, 27,<br>26, 25,<br>24, 23,<br>18, 17,<br>16, 15,<br>14, 13,<br>12, 11 | out0_p, out0_n<br>out1_p, out1_n<br>out2_p, out2_n<br>out3_p, out3_n<br>out4_p, out4_n<br>out5_p, out5_n<br>out6_p, out6_n<br>out7_p, out7_n | <b>Differential Output (Analog Output).</b> Differential outputs.   |
| 9, 19,<br>22, 32  | vdd  | <b>Positive Supply Voltage.</b> 2.5V <sub>DC</sub> or 3.3 V <sub>DC</sub> nominal.  |
| 20, 21  | gnd  | <b>Ground.</b> 0 V.   |
| 31  | sel  | <b>Input Select (Input).</b> Selects the reference input that is buffered;<br>0: clk0<br>1: clk1<br>This pin is internally pulled down to GND.                          |
| 2, 4,<br>5, 7, 10   | NC   | <b>No Connection.</b> Leave unconnected.  |

### 3.0 Functional Description

The ZL40226 is an LVDS clock fanout buffer with eight identical output clock drivers capable of operating at frequencies up to 750MHz.

The two Inputs to the ZL40226 are externally terminated to allow use of precision termination components and to allow full flexibility of input termination. The ZL40226 can accept DC or AC coupled LVPECL, LVDS, CML or HCSL input signals; single ended input signals can also be accepted. A pin compatible device with internal termination is also available.

The ZL40226 is designed to fan out low-jitter reference clocks for wired or optical communications applications while adding minimal jitter to the clock signal. An internal linear power supply regulator and bulk capacitors minimize additive jitter due to power supply noise. The device operates from 2.5V $\pm$ 5% or 3.3V $\pm$ 5% supply. Its operation is guaranteed over the industrial temperature range -40°C to +85°C.

The device block diagram is shown in Figure 1; its operation is described in the following sections.

#### 3.1 Clock Input Selection

The select line chooses which input clock is routed to the outputs.

| Sel | Active Input |
|-----|--------------|
| 0   | clk0         |
| 1   | clk1         |

Table 1 - Input Selection

#### 3.2 Clock Input Termination

The ZL40226 is adaptable to support different types of differential and single-ended input signals depending on the passive components used in the input termination. The application diagrams in the following figures allow the ZL40226 to accept LVPECL, LVDS, CML, HCSL and single-ended inputs.

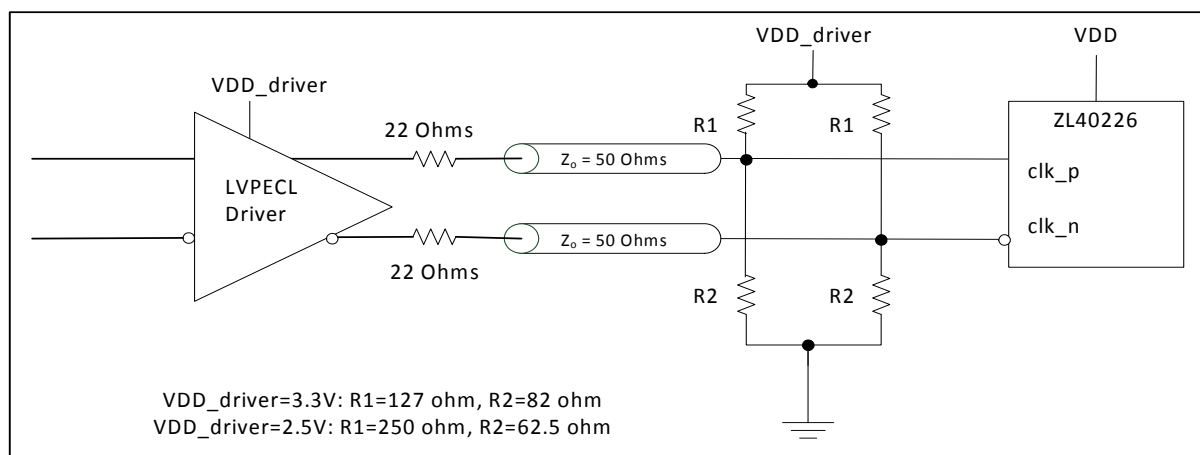


Figure 3 - LVPECL Input DC Coupled Thevenin Equivalent

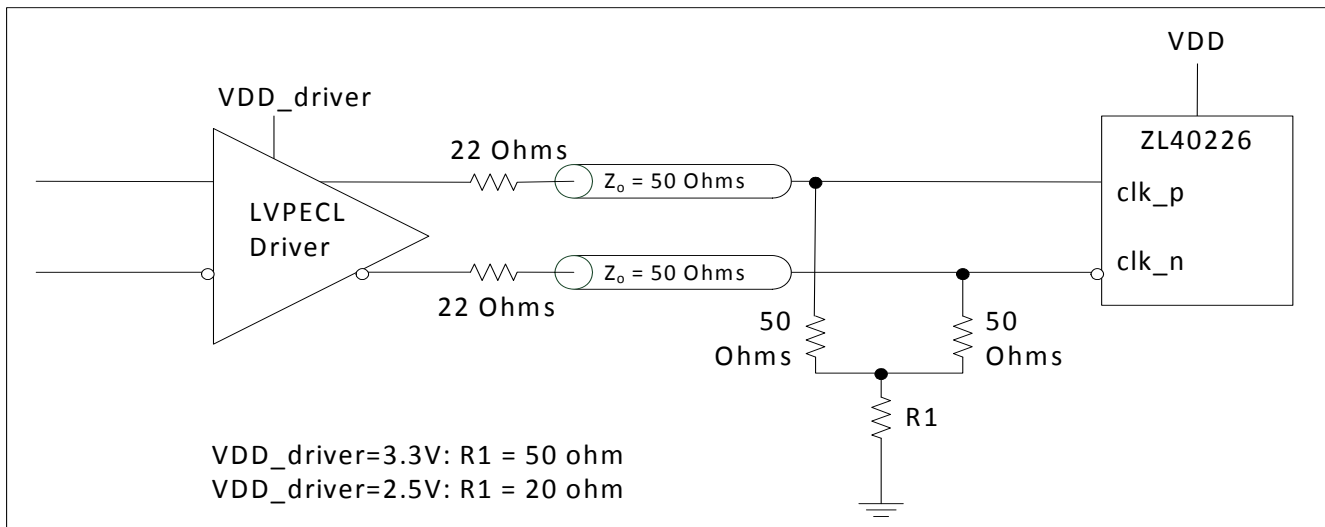


Figure 4 - LVPECL Input DC Coupled Parallel Termination

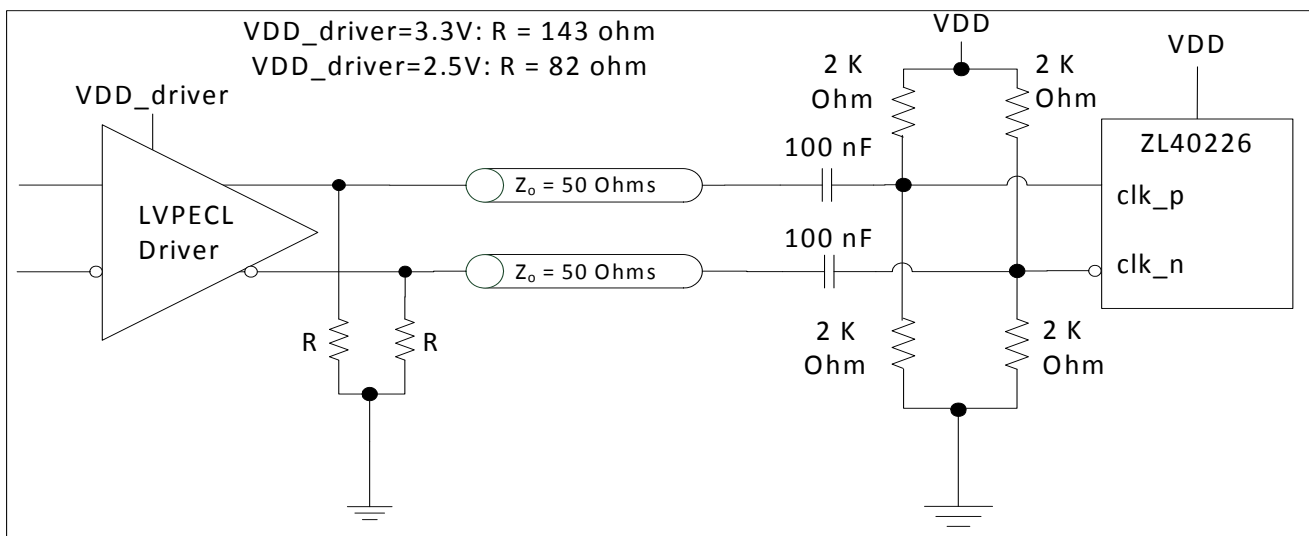


Figure 5 - LVPECL Input AC Coupled Termination

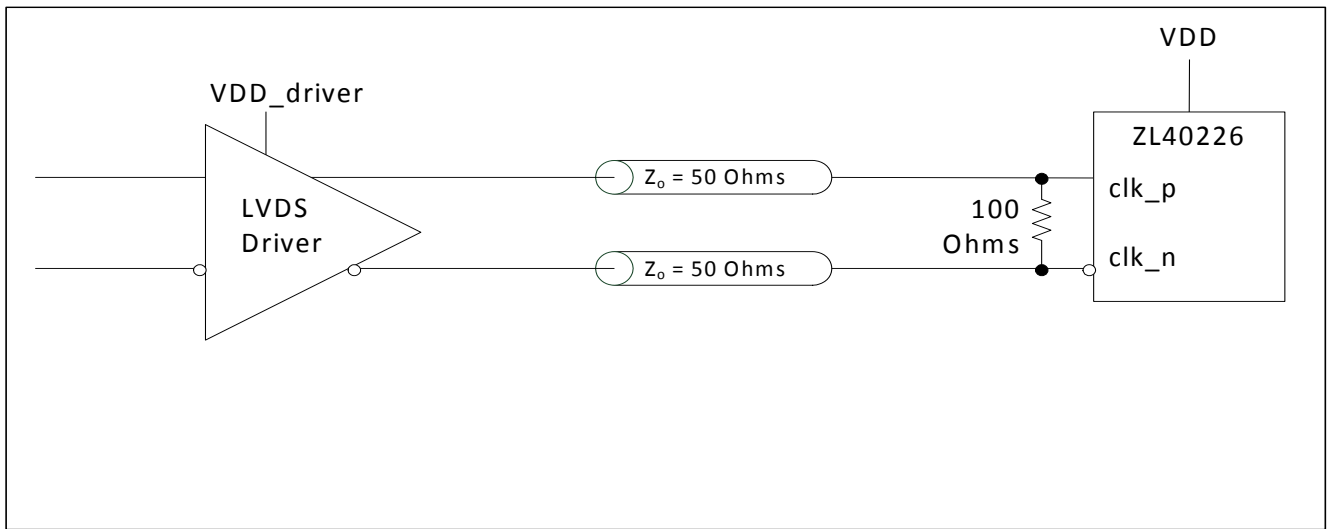


Figure 6 - LVDS Input DC Coupled

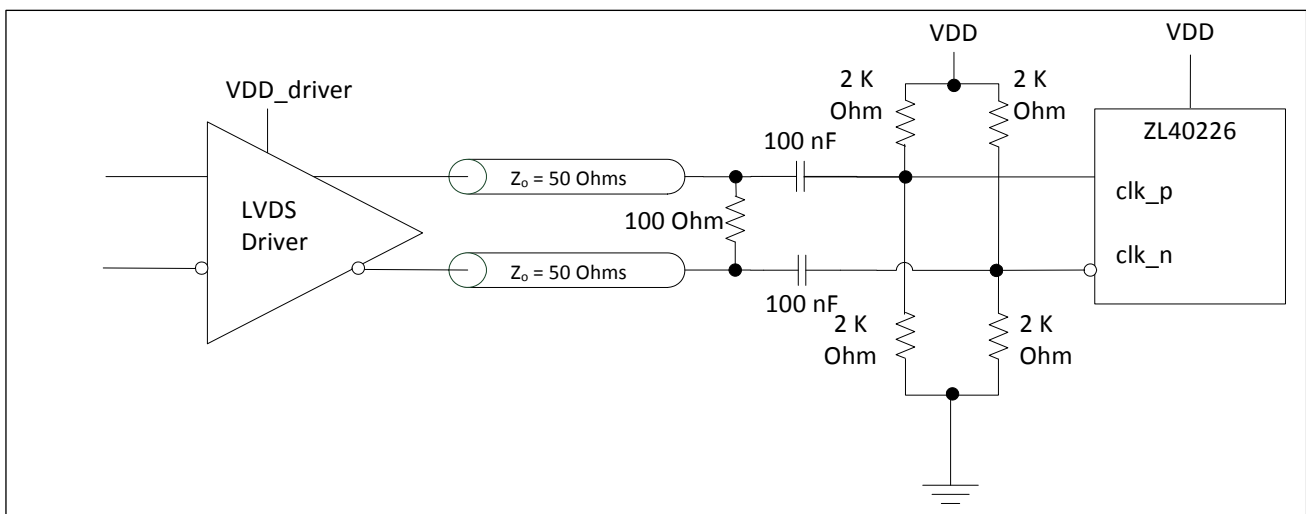


Figure 7 - LVDS Input AC Coupled



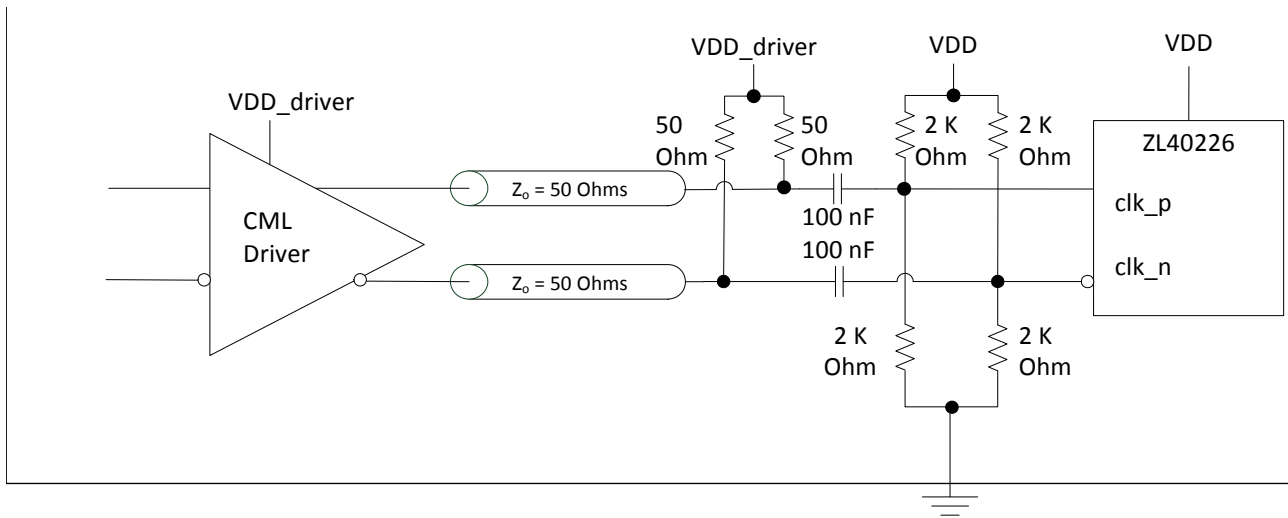


Figure 8 - CML Input AC Coupled

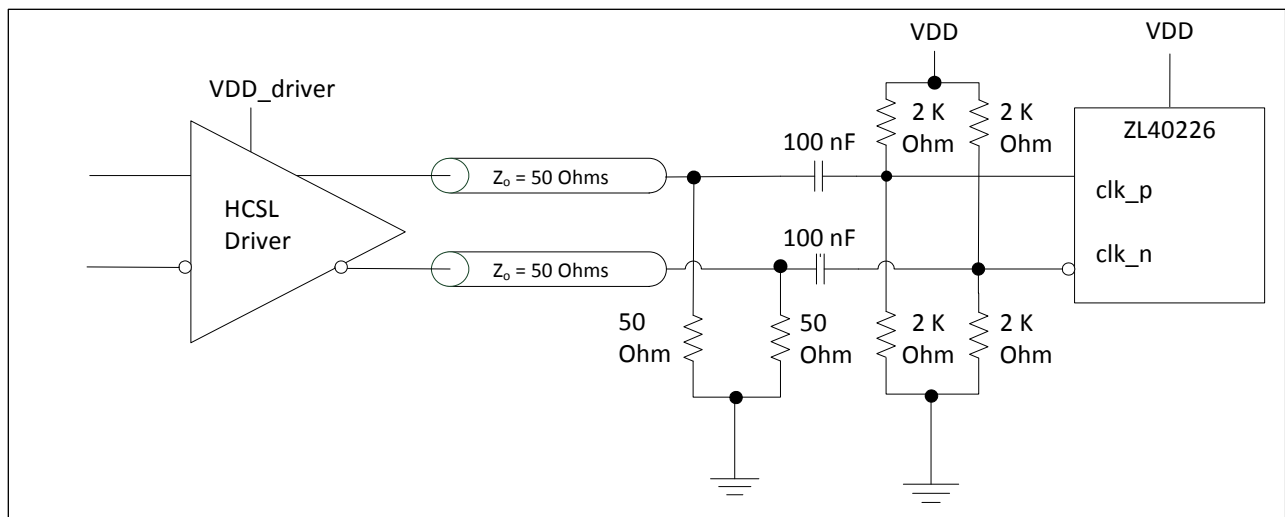
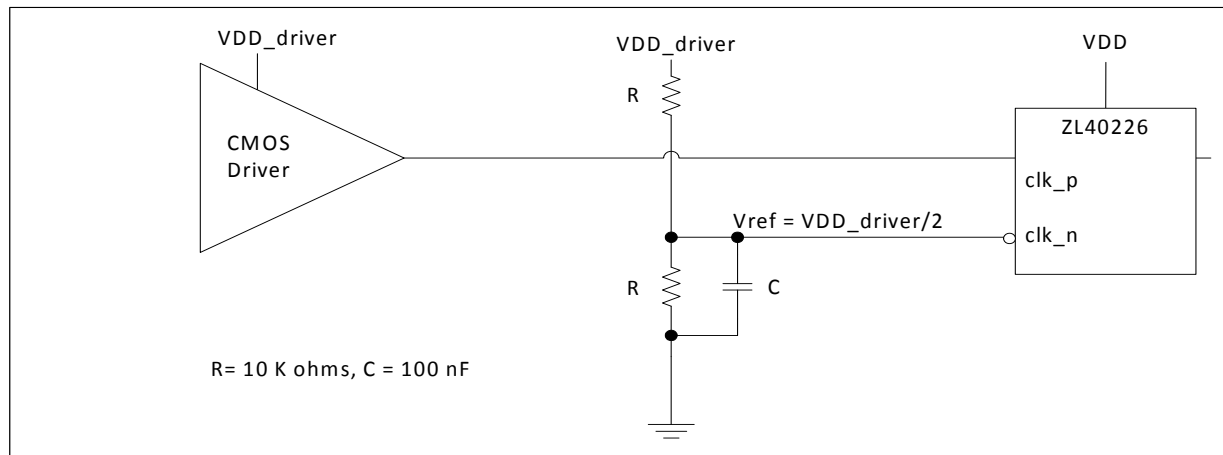
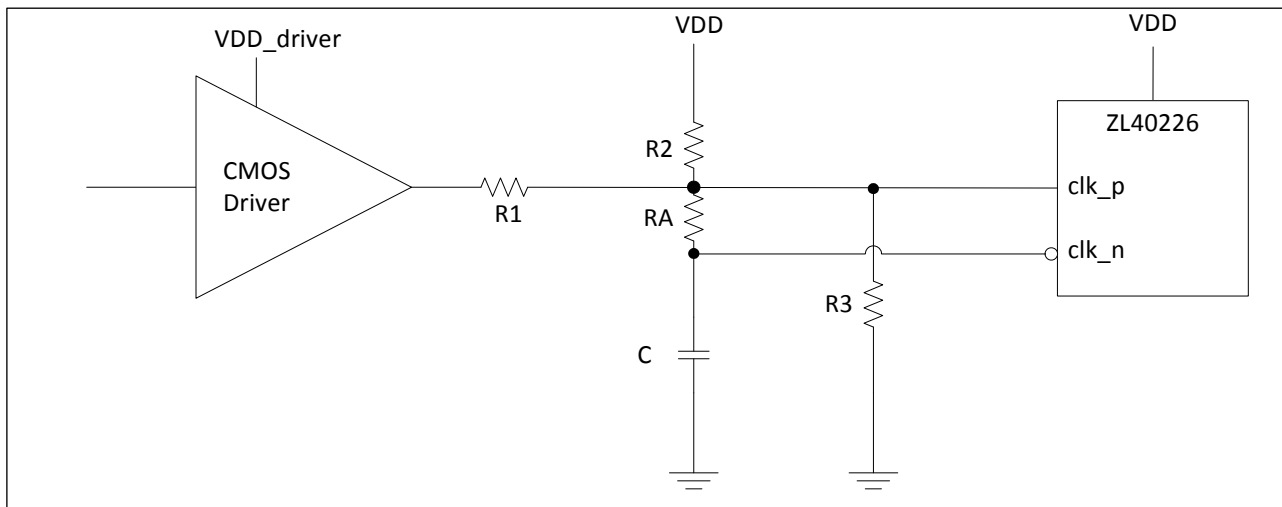


Figure 9 - HCSL Input AC Coupled



**Figure 10 - CMOS Input DC Coupled Referenced to VDD/2**



**Figure 11 - CMOS Input DC Coupled Referenced to Ground**

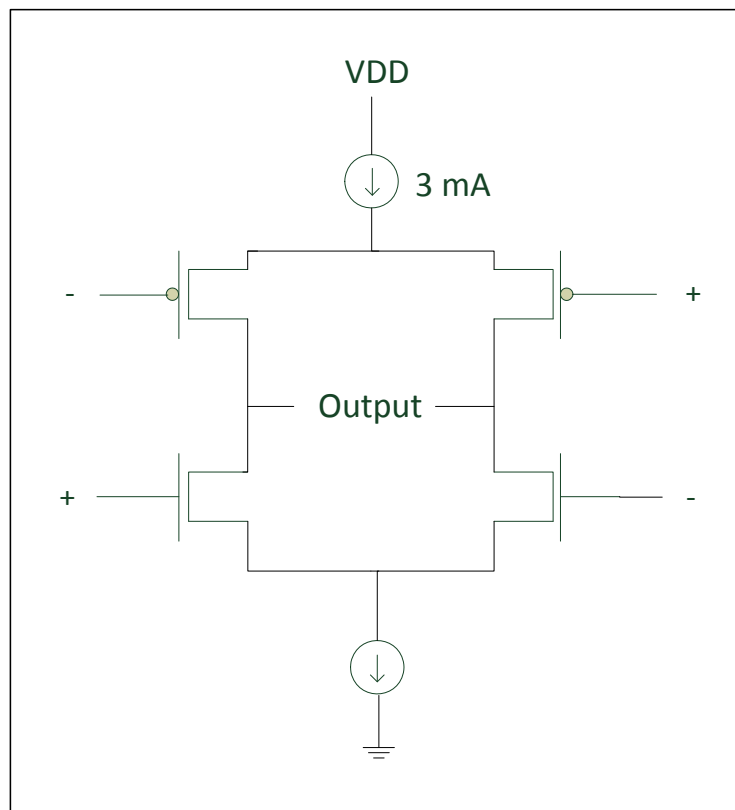
| VDD_driver | R1 (kΩ) | R2 (kΩ) | R3 (kΩ) | RA (kΩ) | C (pF) |
|------------|---------|---------|---------|---------|--------|
| 1.5        | 1.25    | 3.075   | open    | 10      | 10     |
| 1.8        | 1       | 3.8     | open    | 10      | 10     |
| 2.5        | 0.33    | 4.2     | open    | 10      | 10     |
| 3.3        | 0.75    | open    | 4.2     | 10      | 10     |

**Table 2 - Component Values for Single Ended Input Reference to Ground**

\* For frequencies below 100 MHz, increase C to avoid signal integrity issues.

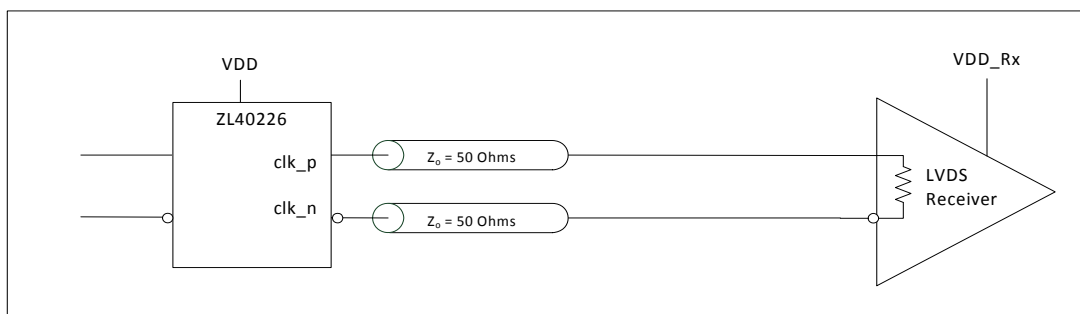
### 3.3 Clock Outputs

LVDS has lower signal swing than LVPECL which results in a low power consumption. A simplified diagram for the LVDS output stage is shown in Figure 12.

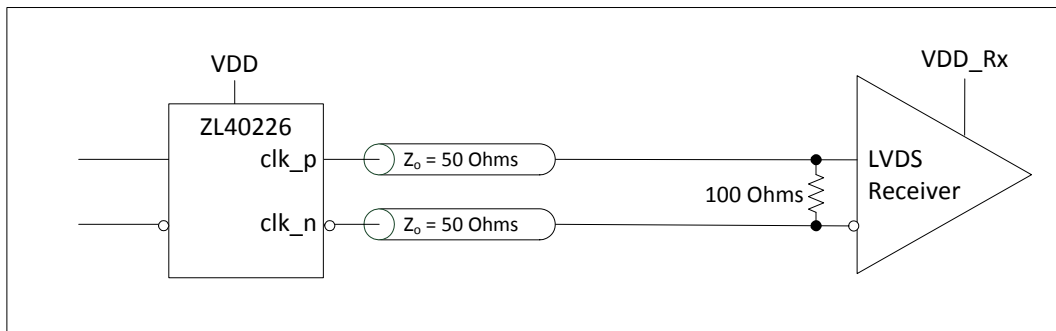


**Figure 12 - Simplified LVDS Output Driver**

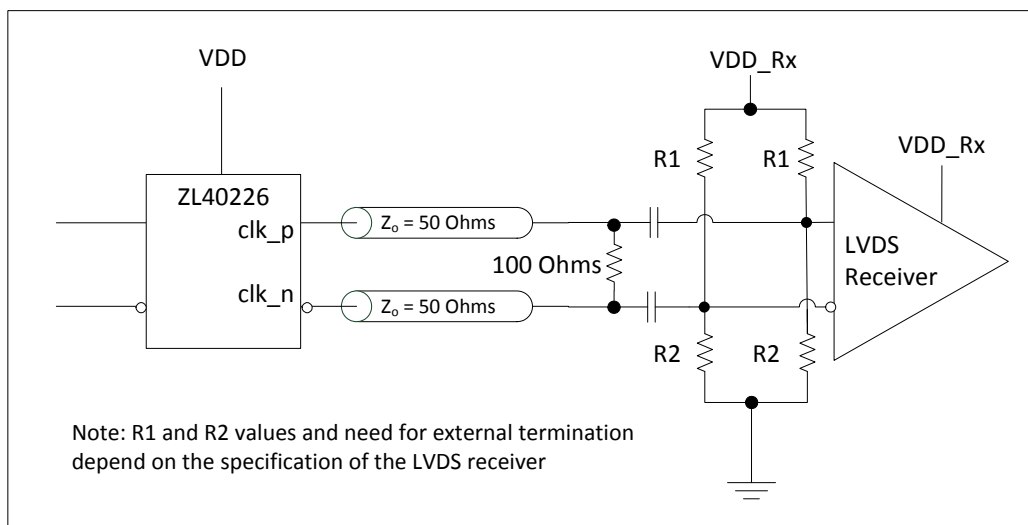
The methods to terminate the ZL40226 drivers are shown in the following figures.



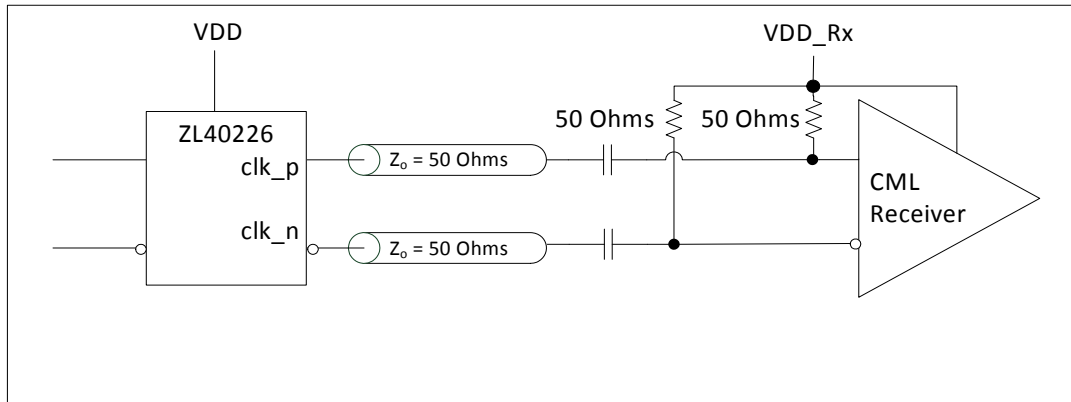
**Figure 13 - LVDS DC Coupled Termination (Internal Receiver Termination)**



**Figure 14 - LVDS DC Coupled Termination (External Receiver Termination)**



**Figure 15 - LVDS AC Coupled Termination**



**Figure 16 - LVDS AC Output Termination for CML Inputs**

### 3.4 Device Additive Jitter

The ZL40226 clock fanout buffer is not intended to filter clock jitter. The jitter performance of this type of device is characterized by its additive jitter. Additive jitter is the jitter the device would add to a hypothetical jitter-free clock as it passes through the device. The additive jitter of the ZL40226 is random and as such it is not correlated to the jitter of the input clock signal.

The square of the resultant random RMS jitter at the output of the ZL40226 is equal to the sum of the squares of the various random RMS jitter sources including: input clock jitter; additive jitter of the buffer; and additive jitter due to power supply noise. There may be additional deterministic jitter sources, but they are not shown in Figure 17.

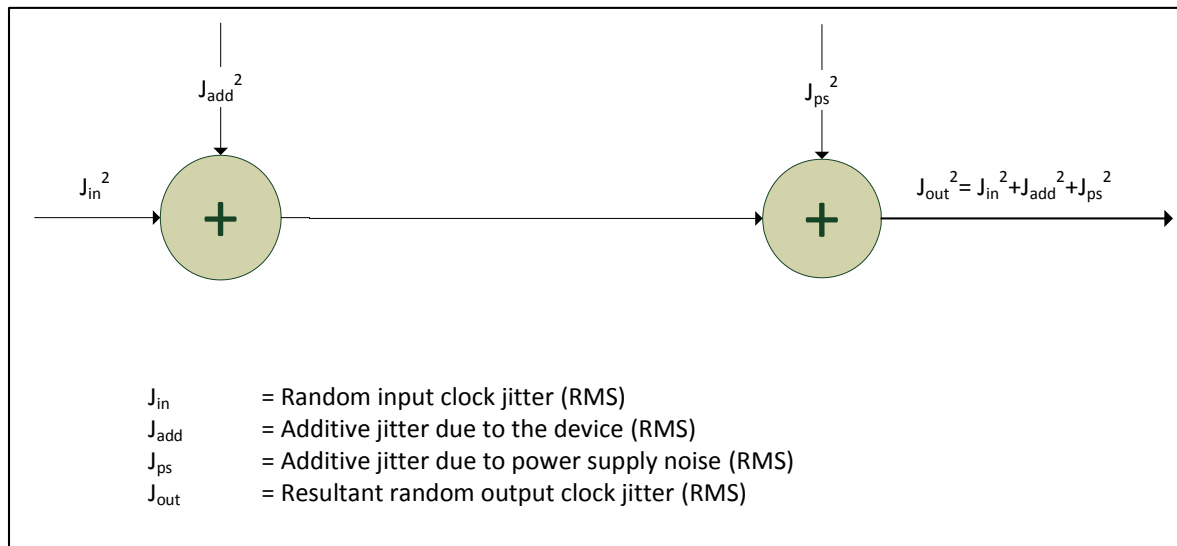


Figure 17 - Additive Jitter

### 3.5 Power Supply

This device operates with either a 2.5V supply or 3.3V supply.

#### 3.5.1 Sensitivity to power supply noise

Power supply noise from sources such as switching power supplies and high-power digital components such as FPGAs can induce additive jitter on clock buffer outputs. The ZL40226 is equipped with a low drop out (LDO) linear power regulator and on-chip bulk capacitors to minimize additive jitter due to power supply noise. The on-chip measures in combination with the simple recommended power supply filtering and PCB layout minimize additive jitter from power supply noise.

#### 3.5.2 Power supply filtering

For optimal jitter performance, the ZL40226 should be isolated from the power planes connected to its power supply pins as shown in Figure 18.

- 10  $\mu\text{F}$  capacitors should be size 0603 or size 0805 X5R or X7R ceramic, 6.3 V minimum rating
- 0.1  $\mu\text{F}$  capacitors should be size 0402 X5R ceramic, 6.3 V minimum rating
- Capacitors should be placed next to the connected device power pins

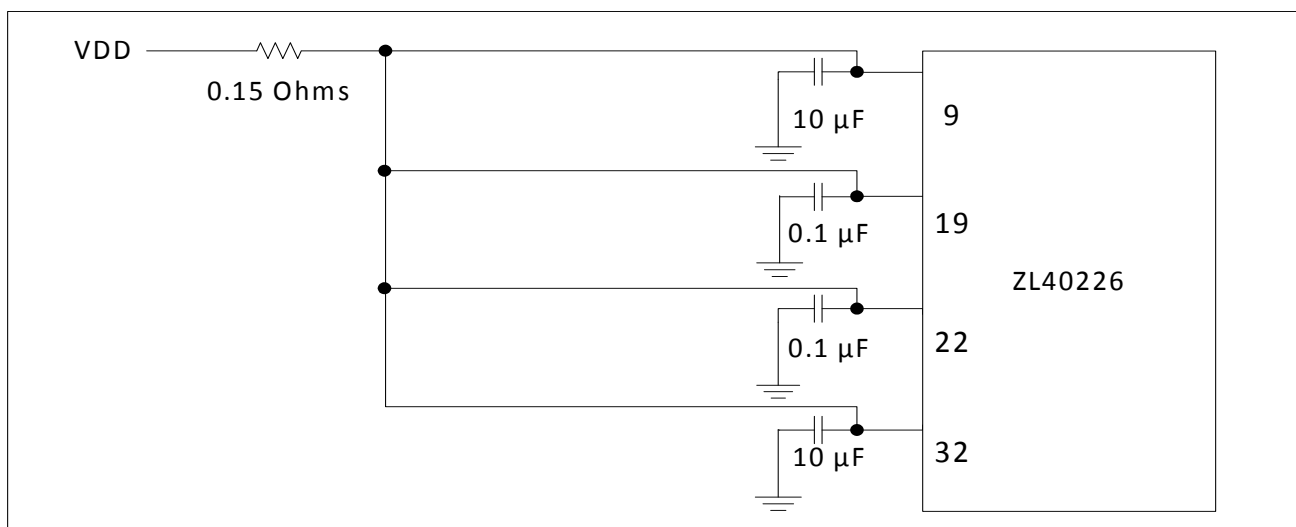


Figure 18 - Decoupling Connections for Power Pins

#### 3.5.3 PCB layout considerations

The power supply filtering shown in Figure 18 can be implemented either as a plane island, or as a routed power topology with the same performance.

## 4.0 AC and DC Electrical Characteristics

### Absolute Maximum Ratings\*

|   | Parameter                  | Sym.        | Min. | Max.     | Units |
|---|----------------------------|-------------|------|----------|-------|
| 1 | Supply voltage             | $V_{DD\_R}$ | -0.5 | 4.6      | V     |
| 2 | Voltage on any digital pin | $V_{PIN}$   | -0.5 | $V_{DD}$ | V     |
| 3 | Soldering temperature      | T           |      | 260      | °C    |
| 4 | Storage temperature        | $T_{ST}$    | -55  | 125      | °C    |
| 5 | Junction temperature       | $T_j$       |      | 125      | °C    |
| 6 | Voltage on input pin       | $V_{input}$ |      | $V_{DD}$ | V     |
| 7 | Input capacitance each pin | $C_p$       |      | 500      | fF    |

\* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

\* Voltages are with respect to ground (GND) unless otherwise stated

### Recommended Operating Conditions\*

|   | Characteristics           | Sym.       | Min.  | Typ. | Max.  | Units |
|---|---------------------------|------------|-------|------|-------|-------|
| 1 | Supply voltage 2.5 V mode | $V_{DD25}$ | 2.375 | 2.5  | 2.625 | V     |
| 2 | Supply voltage 3.3 V mode | $V_{DD33}$ | 3.135 | 3.3  | 3.465 | V     |
| 3 | Operating temperature     | $T_A$      | -40   | 25   | 85    | °C    |

\* Voltages are with respect to ground (GND) unless otherwise stated

### DC Electrical Characteristics - Current Consumption

|   | Characteristics   | Sym.           | Min. | Typ. | Max. | Units | Notes |
|---|---|----------------|------|------|------|-------|-------|
| 1 | Supply current LVDS drivers - loaded (all outputs are active) | $I_{dd\_load}$ |      | 113  |      | mA    |       |

### DC Electrical Characteristics - Inputs and outputs - for 2.5/3.3 V supply

|   | Characteristics                          | Sym.      | Min.               | Typ. | Max.               | Units | Notes                 |
|---|--|-----------|--------------------|------|--------------------|-------|-----------------------|
| 1 | CMOS control logic high-level input      | $V_{CIH}$ | $0.7 \cdot V_{DD}$ |      |                    | V     |                       |
| 2 | CMOS control logic low-level input       | $V_{CIL}$ |                    |      | $0.3 \cdot V_{DD}$ | V     |                       |
| 3 | CMOS control logic Input leakage current | $I_{IL}$  |                    | 1    |                    | μA    | $V_I = V_{DD}$ or 0 V |
| 4 | Differential input voltage difference    | $V_{ID}$  | 0.25               |      | 1                  | V     |                       |
| 5 | Differential common mode voltage         | $V_{CM}$  | 1.1                |      | 1.6                | V     | for 2.5 V             |
| 6 | Differential common mode voltage         | $V_{CM}$  | 1.1                |      | 2.0                | V     | for 3.3 V             |
| 7 | LVDS output differential voltage*        | $V_{OD}$  | 0.25               | 0.30 | 0.40               | V     |                       |
| 8 | LVDS output common mode                  | $V_{CM}$  | 1.1                | 1.25 | 1.375              | V     |                       |

\* The VOD parameter was measured from 125 MHz to 750 MHz.





Figure 19 - Differential Voltage Parameter

AC Electrical Characteristics\* - Inputs and Outputs (see Figure 20) - for 2.5/3.3 V supply.

|   | Characteristics                         | Sym.                                | Min. | Typ. | Max. | Units   | Notes |
|---|---|-------------------------------------|------|------|------|---------|-------|
| 1 | Maximum Operating Frequency             | 1/t <sub>p</sub>                    |      |      | 750  | MHz     |       |
| 2 | Input to output clock propagation delay | t <sub>pd</sub>                     | 0    | 1    | 2    | ns      |       |
| 3 | Output to output skew                   | t <sub>out2out</sub>                |      | 80   | 150  | ps      |       |
| 4 | Part to part output skew                | t <sub>part2part</sub>              |      | 120  | 300  | ps      |       |
| 5 | Output clock Duty Cycle degradation     | t <sub>PWH</sub> / t <sub>PWL</sub> | -5   | 0    | 5    | Percent |       |
| 6 | LVDS Output slew rate                   | r <sub>sl</sub>                     | 0.55 |      |      | V/ns    |       |
| 7 | Reference transition time               | t <sub>switch</sub>                 |      | 0.5  | 1    | us      |       |

\* Supply voltage and operating temperature are as per Recommended Operating Conditions

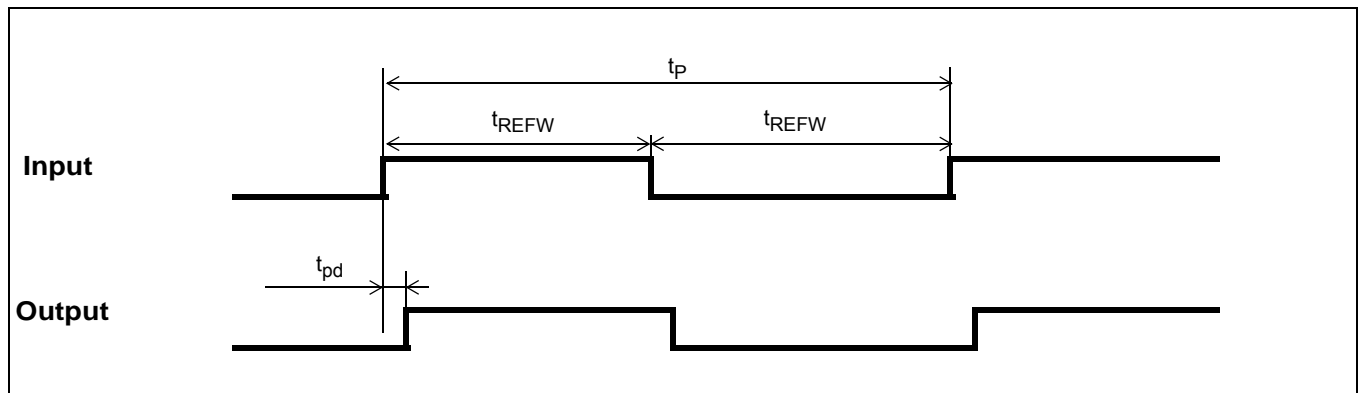


Figure 20 - Input To Output Timing

## 5.0 Performance Characterization

### Additive Jitter at 2.5 V\*

|   | Output Frequency (MHz) | Jitter Measurement Filter | Typical RMS (fs) | Notes |
|---|------------------------|---------------------------|------------------|-------|
| 1 | 125                    | 12 kHz - 20 MHz           | 148              |       |
| 2 | 212.5                  | 12 kHz - 20 MHz           | 138              |       |
| 3 | 311.04                 | 12 kHz - 20 MHz           | 121              |       |
| 4 | 425                    | 12 kHz - 20 MHz           | 115              |       |
| 5 | 500                    | 12 kHz - 20 MHz           | 107              |       |
| 6 | 622.08                 | 12 kHz - 20 MHz           | 107              |       |
| 7 | 750                    | 12 kHz - 20 MHz           | 105              |       |

\*The values in this table were taken with an approximate slew rate of 0.8 V/ns.

### Additive Jitter at 3.3 V\*

|   | Output Frequency (MHz) | Jitter Measurement Filter | Typical RMS (fs) | Notes |
|---|------------------------|---------------------------|------------------|-------|
| 1 | 125                    | 12 kHz - 20 MHz           | 150              |       |
| 2 | 212.5                  | 12 kHz - 20 MHz           | 138              |       |
| 3 | 311.04                 | 12 kHz - 20 MHz           | 120              |       |
| 4 | 425                    | 12 kHz - 20 MHz           | 115              |       |
| 5 | 500                    | 12 kHz - 20 MHz           | 107              |       |
| 6 | 622.08                 | 12 kHz - 20 MHz           | 106              |       |
| 7 | 750                    | 12 kHz - 20 MHz           | 104              |       |

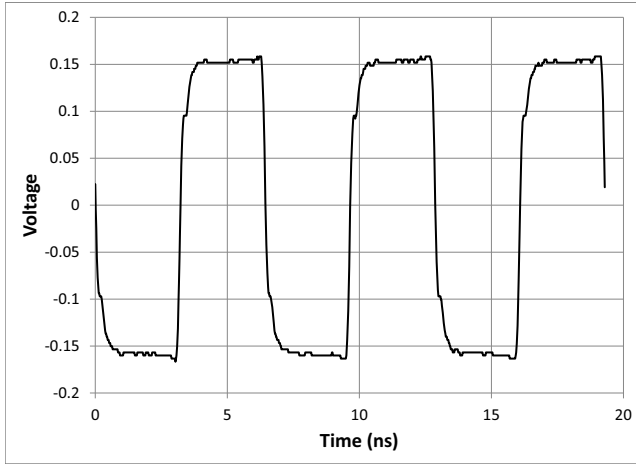
\*The values in this table were taken with an approximate slew rate of 0.8 V/ns.

### Additive jitter from a power supply tone\*

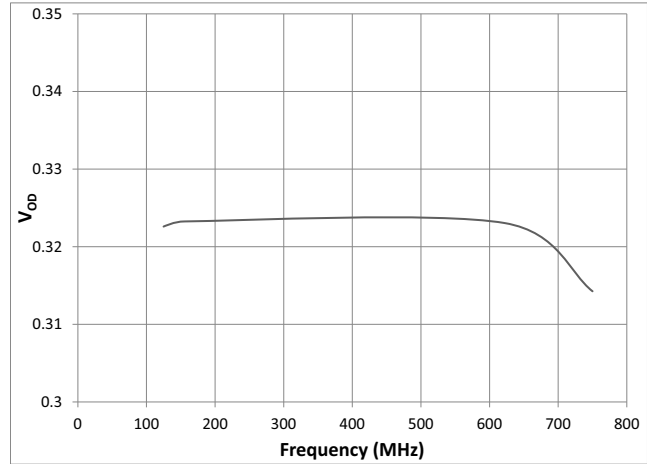
| Carrier frequency | Parameter        | Typical | Units  | Notes |
|-------------------|------------------|---------|--------|-------|
| 125               | 25 mV at 100 kHz | 24      | fs RMS |       |
| 750               | 25 mV at 100 kHz | 23      | fs RMS |       |

\* The values in this table are the additive periodic jitter caused by an interfering tone typically caused by a switching power supply. For this test, measurements were taken over the full temperature and voltage range for  $V_{DD} = 3.3$  V. The magnitude of the interfering tone is measured at the DUT.

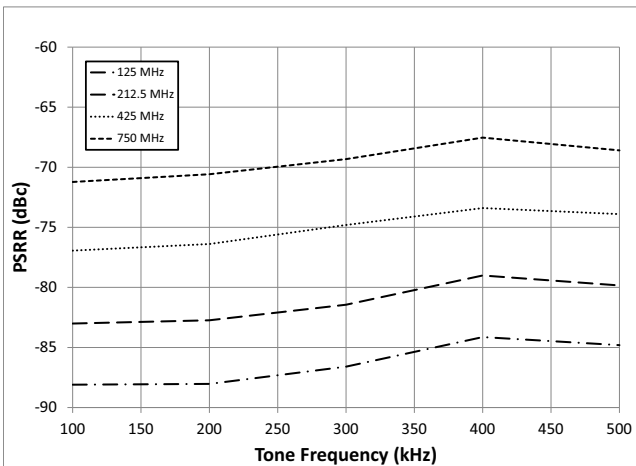
## 6.0 Typical Behavior



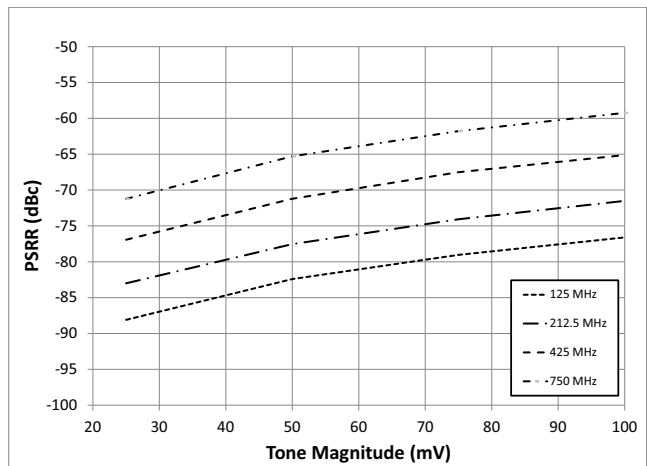
Typical Waveform at 155.52 MHz



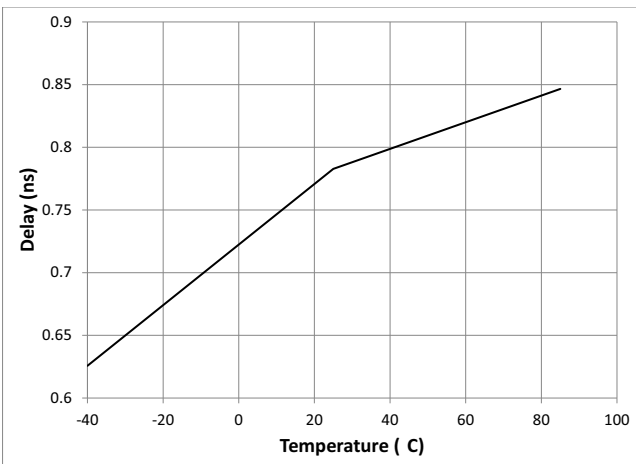
V<sub>OD</sub> vs Frequency



Power Supply Tone Frequency versus PSRR



Power Supply Tone Magnitude versus PSRR



Propagation Delay versus Temperature

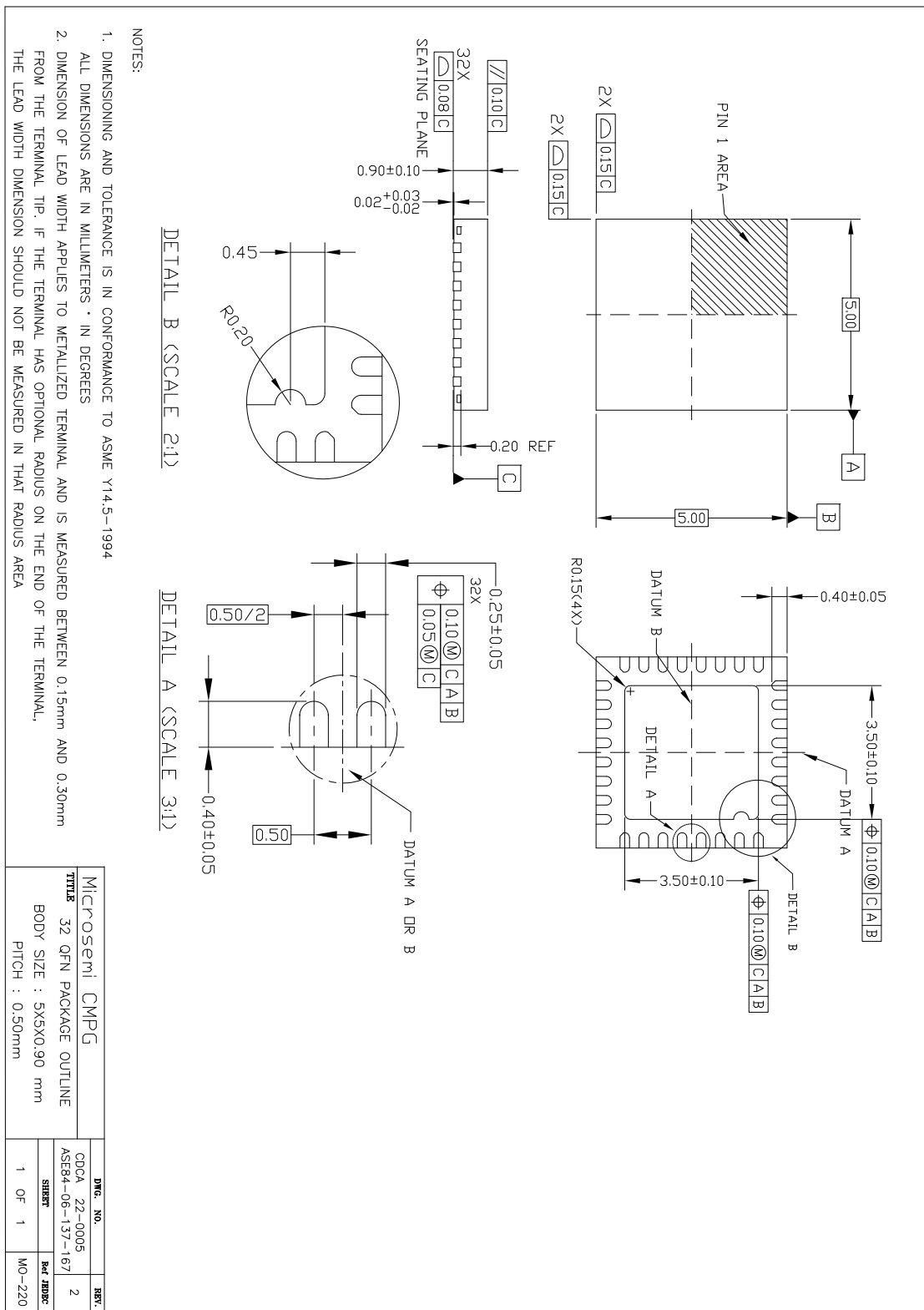
Note: This is for a single device. For more details, see the characterization section.

## 7.0 Package Characteristics

### Thermal Data

| Parameter                              | Symbol        | Test Condition | Value | Unit                        |
|--|---------------|----------------|-------|-----------------------------|
| Junction to Ambient Thermal Resistance | $\Theta_{JA}$ | Still Air      | 37.4  | $^{\circ}\text{C}/\text{W}$ |
|  |               | 1 m/s          | 33.1  |                             |
|  |               | 2 m/s          | 31.5  |                             |
| Junction to Case Thermal Resistance    | $\Theta_{JC}$ |                | 24.4  | $^{\circ}\text{C}/\text{W}$ |
| Junction to Board Thermal Resistance   | $\Theta_{JB}$ |                | 19.5  | $^{\circ}\text{C}/\text{W}$ |
| Maximum Junction Temperature*          | $T_{jmax}$    |                | 125   | $^{\circ}\text{C}$          |
| Maximum Ambient Temperature            | $T_A$         |                | 85    | $^{\circ}\text{C}$          |

### 8.0 Mechanical Drawing





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