

Features

- **Next Generation ZL880 VoicePort Family with Enhanced Features and Performance**
 - Low BOM cost shared power supplies
 - Optional low BOM cost shared protection circuitry
 - Same API interface as the VE880 Series
- **Complete BORSCHT Functions for Two FXS Channels in a Single 64-Pin 9x9 QFN Package**
- **Choice of Low cost, Energy Efficient Switching Regulator Architectures**
 - Patent-pending Shared Buck-Boost Automatic Battery Switching (BBABS)
 - Shared Tracking Battery (STB)
- **Integrated Power Management**
 - STB switching regulator tracks line voltage minimizing active power dissipation
 - Low Power Idle Mode
 - Integrated real-time power monitoring tool
- **Ringing**
 - 50 V_{RMS} open circuit with 5 REN load (BBABS)
 - 60 V_{RMS} open circuit with 3 REN load (STB)
 - Adaptive ringing for power management
- **Worldwide Programmability**
 - Narrowband or Wideband mode
 - Input impedance, balance impedance, gain
 - DC feed voltage and current limit
 - Ringing frequency, voltage and current limit
 - G.711 μ -law, A-law, or 16-bit linear coding
 - Call progress tone and Caller ID generation
 - Sample coefficients for more than 50 countries
- **Pin-Selectable PCM/MPI or ZSI Interfaces**
 - MPI Mode with support for SPI Mode 3 and no inter byte chip select off time
 - ZSI Mode for a smaller number of interface signals to the host and less expensive isolation
- **VoicePath™ SDK and VP-API-II Software Available to Implement FXS Functions**
- **VeriVoice™ Software Suites Available for Manufacturing and Subscriber Loop Testing**
 - Utilizes integrated test tool box

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Ordering Information

Device OPN ⁽¹⁾	Device Type	Package	Packing
ZL88801LDF1	100V-Tracker	64-pin QFN (9x9)	Tape & Reel
ZL88801LDG1	100V-Tracker	64-pin QFN (9x9)	Tray

1. The Green package meets RoHS Directive 2002/95/EC of the European Council to minimize the environmental impact of electrical equipment.

Applications

- **DSL Residential Gateways and Integrated Access Devices (IADs)**
- **PON Single Family Units (SFUs)**

Description

The Microsemi® ZL88801 Dual Channel Shared Battery Wideband VoicePort Device provides complete BORSCHT functions for two telephone line FXS ports. This device is a part of the new ZL880 Series featuring enhanced functionality, lower BOM cost, and greater power efficiency. The ZL880 Series maintains software compatibility with the industry leading VE880 Series.

The ZL88801 uses energy efficient shared power supply topologies for reduced BOM cost. The ZL88801 can be configured for patent-pending inverting Buck-Boost Automatic Battery Switching or Shared Tracking Battery operation.

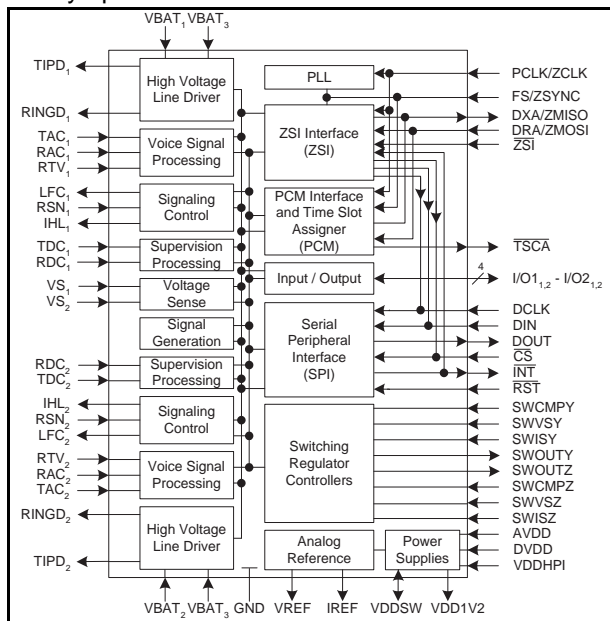


Figure 1 - ZL88801 Device Block Diagram

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1.0 Solution Overview

The *ZL880 VoicePort Series* represents Microsemi's next generation solution for cable eMTAs, fiber PON SFUs, Integrated Access Devices, DSL Gateways, and other telephony products for worldwide markets. The *ZL880 VoicePort Series* consists of a *ZL88701/702 Tracking Battery*, *ZL88601/602 Auto Battery Switching (ABS)*, or *ZL88801 Shared Battery* device, *VoicePath API-II (VP-API-II) Software*, and *Profiles Data Structures*. To support the *ZL880 VoicePort Series*, Microsemi offers a comprehensive *VoicePath Software Development Kit (SDK)* and hardware reference designs.

The ZL88801 Shared Battery device implements a universal telephone line interface by performing all necessary voice telephony functions from driving a high voltage subscriber telephone line to DSP codec functions for two lines. All AC, DC, and signaling parameters are fully programmable via a pin-selectable PCM and SPI or reduced pin-count ZSI interface.

The ZL88801 features integrated switching controllers that drive external components to generate the high voltages necessary for efficiently powering and ringing analog telephones. The high performance architecture permits high efficiency in all operating states and corresponding low power consumption. The switching regulator circuit can be configured for Shared Inverting Buck-Boost Automatic Battery Switching (BBABS) or Shared Tracking Battery (STB) operation. Both circuits support ringing voltages up to $85-V_{PK}$. BBABS operation supports large ringing loads and requires a minimal number of external components. STB operation features low power consumption and maximum power efficiency in all states. The lower battery voltages used in STB operation also allow for use of a low cost shared protection option.

Additionally, the ZL88801 has self-test and line test support to allow the system to resolve faults to the line or line circuit.

The *VoicePath API-II (VP-API-II)* software initializes each FXS port coefficient data containing application or country-specific AC and DC parameters, ringing and other signaling characteristics, and configures the switcher. *VP-API-II* resides on the customer's VoIP processor or SoC and provides high-level control over the telephony functions. *VP-API-II* offers a seamless migration between products utilizing its common software architecture and interfaces with the Microsemi *VeriVoice Professional Test Suite Software*.

A Microsoft® Windows® GUI (Graphical User Interface) application, *VoicePath Profile Wizard (VP Profile Wizard)*, allows the user to select the operating parameters of the FXS channels and to automatically generate the sets of data structures, called *Profiles*, that are required by the *VP-API-II* for integration with the VoIP host software.

[Figure 2](#) shows a high-level solution diagram with a *ZL880* device, *VP-API-II* and *Profiles*.

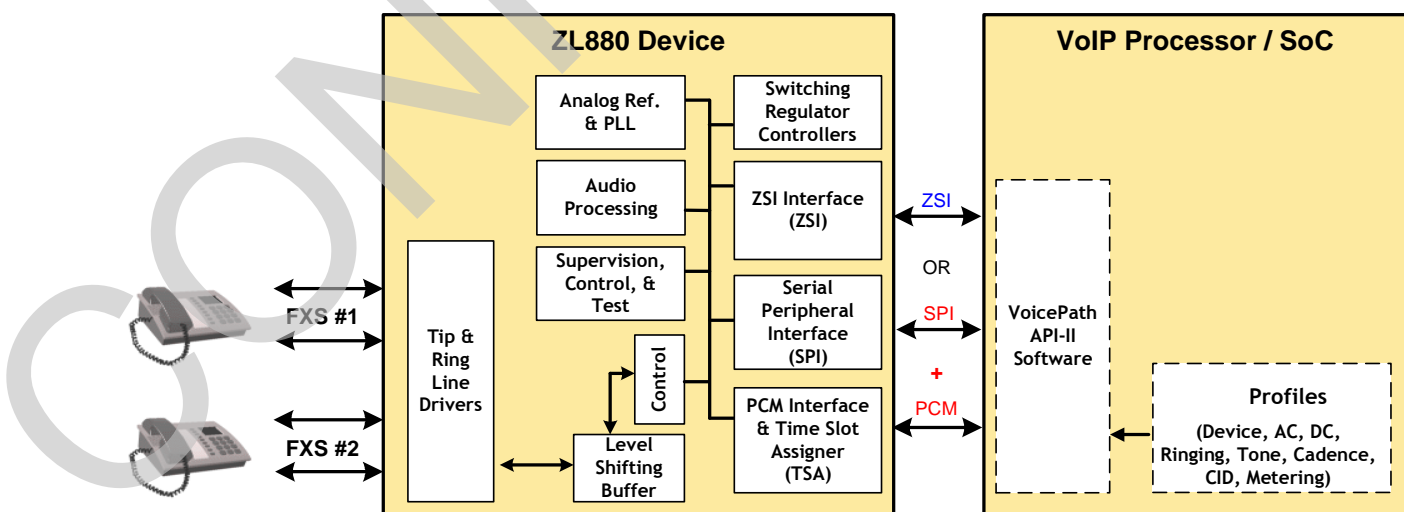


Figure 2 - ZL880 Dual Channel VoicePort Solution Diagram

2.0 ZL88801 Device Overview and Block Diagram

2.1 VE880 Series Features

The ZL88801 device supports the following standard FXS features, which are common with the *VE880 Series*:

- Performs all Battery feed, Ringing, Signaling, Coding, Hybrid and Test (BORSCHT) functions
- Single chip solution provides high voltage line driving, digital signal processing, and high voltage power generation for two lines
- Wideband 7 kHz and Narrowband 3.4 kHz codec modes
- Exceeds *Telcordia® GR-909-CORE* transmission requirements
- Single hardware design meets worldwide requirements through software programming of:
 - Ringing waveform, frequency and amplitude
 - DC loop-feed characteristics and current limit
 - Loop-supervision detection thresholds
 - Off-hook debounce circuit
 - Ground-key and ring-trip filters
 - Two-wire AC impedance
 - Transhybrid balance impedance
 - Transmit and receive gains
 - Transmit and receive equalization
 - Digital I/O pins
 - A-law/ μ -law and linear coding selection
 - Switching power supply
- Supports both loop-start and ground-start signaling
- On-hook transmission
- Power/service denial mode
- Smooth polarity reversal
- Supports wink function
- Metering generation with envelope shaping
 - Programmable frequency and duration
- Internal Test Termination
- Compatible with inexpensive protection networks
- Self-contained ringing generation and control
 - Programmable ringing cadencing
 - Internal battery-backed balanced sinusoidal or trapezoidal ringing
 - Integrated ring-trip filter and software enabled manual or automatic ring-trip mode
- Flexible tone generation
 - Call progress tone generation
 - DTMF tone generation
 - Universal Caller ID generation (FSK and DTMF signaling)
 - Howler tone generation with *VP-API-II*
- Integrated switching regulator controller
 - Can generate the battery voltages for each line
 - Good efficiency in all states
 - Low idle-power per line
 - Line-feed characteristics independent of battery voltage
- Monitors two-wire interface voltages and currents for subscriber line diagnostics implemented by *VeriVoice Professional Test Suite Software*
- Supported by *VeriVoice Manufacturing Test Package*
- Can monitor and/or drive Tip and Ring independently
- Built-in voice-path test modes
- Integrated self-test features
- 100% compatible with *VoicePath SDK* and *VP-API-II*
- Small physical size in 9x9 mm 64-pin QFN

2.2 New and Enhanced Features

In addition to the standard *VE880 Series* FXS features, the ZL88801 features the following enhancements and new capabilities for greater power efficiency and lower system cost:

- New *ZL880 Series* family with a core operating at 1.2 V_{DC}
 - Internal 1.2 V_{DC} regulator
- Very low BOM cost:
 - Single power supply for two channels
 - Optional single low cost fixed voltage protector for two channels (STB operation)
 - Smaller value/size/cost switcher output capacitors
 - Smaller and less expensive capacitors at the SLIC VBAT pins
 - Smaller and less expensive C_{TAC} and C_{RAC} capacitors
- Low-Power Idle Mode (LPIM)
 - Voltage-based off-hook detection
- Supervision ADC for advanced testing, improved calibration and adaptive power management
 - Can monitor up to 5 signals in multiplexed mode, such as VTIP, VRING, IM, IL, and VBAT
 - Two pins for sensing external voltages ranging from -180 V to +60 V
- Improved DC leakage measurements
 - Facilitated by increasing the value of the DC sense resistors to 1.0 MΩ
- Adaptive ringing algorithm adjusts ringing amplitude to meet preset power limit
- Simultaneous ground key / DC fault detection
- Over current monitoring and blanking
 - New programmable options and thresholds
- Improved hook and ground key detection with hysteresis and calibrated thresholds
- Enhanced SPI Interface
 - Eliminates the need for \overline{CS} off requirement between data bytes
 - Up to 3 times higher effective bandwidth
 - Support for SPI Modes 0 and 3
- ZSI Interface option requires fewer serial interface signals to the host
 - Only 4 ZSI signals required compared to 9 for PCM and SPI
 - Less expensive system isolation cost
- Programmable PCM and SPI or ZSI interface voltage
 - Supports communication with host processors at 1.8 V, 2.5 V or 3.3 V
- Upgraded command set
 - Per-channel Wideband sampling mode
 - On-chip timer functions
 - Tone generators add frequency modulation capability for compliance with *BT*, *NTT*, and *Austel* special Howler tone requirements
 - Upgraded ring-trip algorithm
- Comprehensive device calibration capabilities
 - Shorter calibration time
 - No need to generate voltages to the Tip/Ring interface
 - Longitudinal operating point calibration
 - Programmable loop current dependent overhead

2.3 Device Block Diagram

Figure 3 shows the major functional blocks of the ZL88801 device.

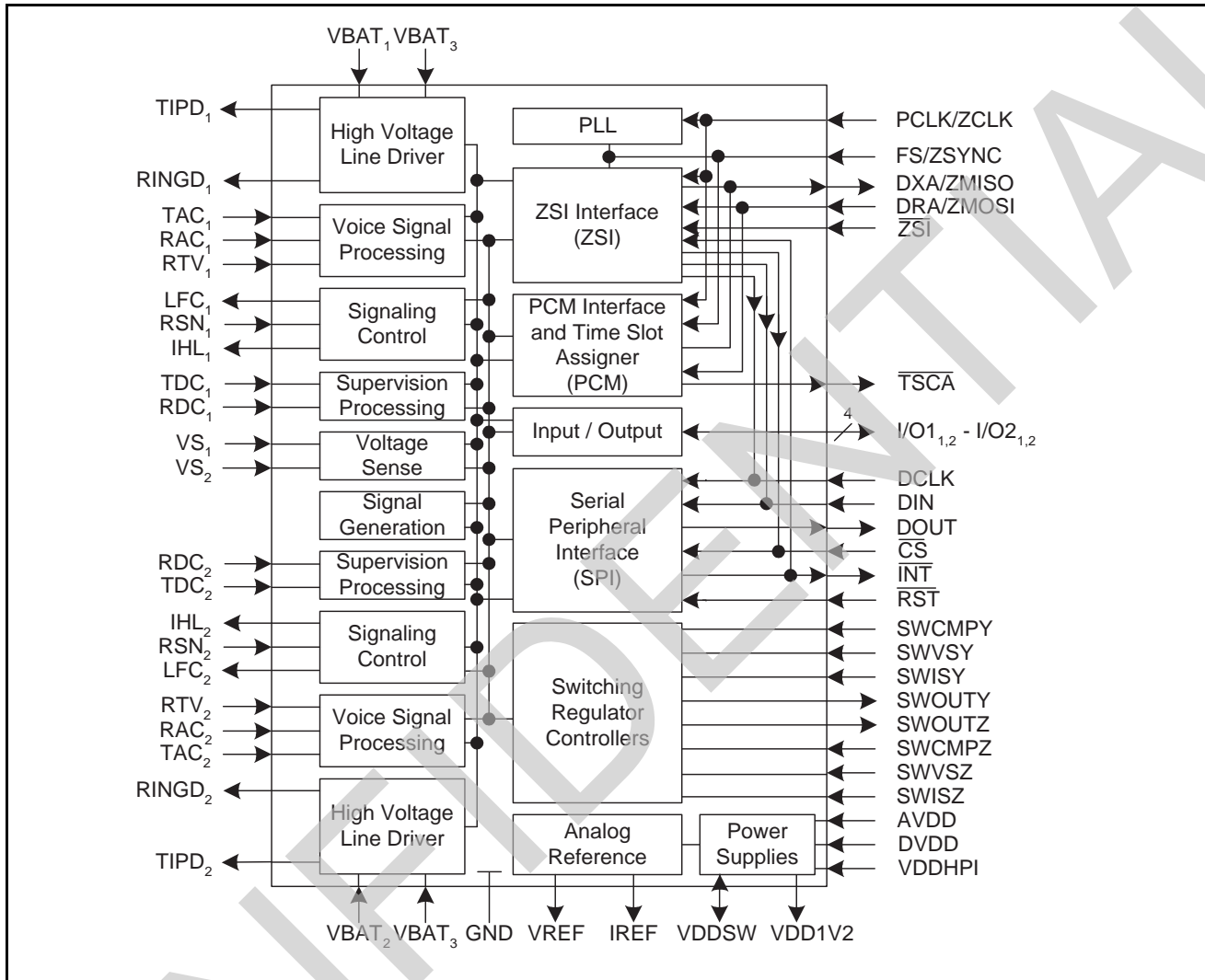


Figure 3 - ZL88801 Device Block Diagram

3.0 Functional Description

3.1 Host Port Interface

The ZL88801 device features a flexible host port interface which is hardware-selectable for communicating with VoIP processors and SoCs using standard PCM and SPI or the reduced pin-count ZSI interfaces.

The host port interface voltage level (VDDHPI) can be set for 1.8 V, 2.5 V, or 3.3 V for maximum system-level compatibility. The host port interface supports the standard telecommunications clock rates of 1.024 MHz, 1.536 MHz, 2.048 MHz, 3.072 MHz, 4.096 MHz, 6.144 MHz, and 8.192 MHz with a Frame Sync (FS) of 8 kHz.

The host port supports two modes of operation: 1) PCM and SPI and 2) ZSI, selected by the $\overline{\text{ZSI}}$ pin.

3.1.1 PCM Interface and Time Slot Assigner

The PCM Interface and Time Slot Assigner (PCM block) is a synchronized serial mode of communication between the system and the ZL88801 device. In PCM mode, voice data can be transmitted/received on a serial PCM highway. This highway uses Frame Sync (FS) and PCLK as reference. The host port interface operates in this mode if the $\overline{\text{ZSI}}$ pin is pulled high.

Data is transmitted out of the DXA pin and received on the DRA pin. The ZL88801 device transmits/receives single 8-bit time slot (A-law/ μ -law) compressed voice data or two contiguous time slot 16-bit two's complement linear voice data. The PCLK is a data clock supplied to the device that determines the rate at which the data is shifted in/out of the PCM ports. The FS pulse identifies the beginning of a transmit/receive frame and all time slots are referenced to it. For the ZL88801 device, the frequency of the FS signal is 8 kHz. In Wideband mode, two evenly spaced sets of time slots are exchanged in each frame. The PCLK frequency can be a number of fixed frequencies as defined by the *VP-API-II*. Please refer to [Figure 46. "Profile Wizard - Device Profile Configuration" on page 74](#) for an example setting of the Transmit and Receive Clock Slots, PCM Transmit Edge, and PCLK Frequency.

The *VP-API-II* allows the time slots to be offset to eliminate any clock skew in the system. The Transmit Clock Slot and Receive Clock Slot fields are each three bits wide to offset the time slot assignment by 0 to 7 PCLK periods. The Transmit and Receive Clock Slot is a global command that is applied at the device level. Thus, for each channel, two time slots must be assigned: one for transmitting voice data and the other for receiving voice data. [Figure 4](#) shows the PCM highway time slot structure.

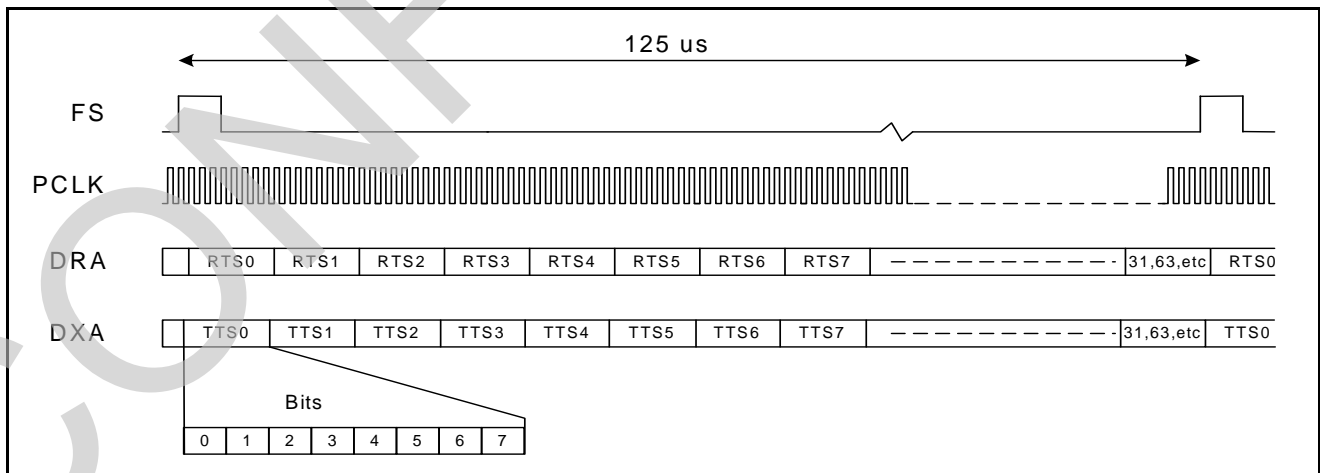


Figure 4 - PCM Highway Structure

3.1.1.1 Transmit PCM Interface

The Transmit PCM interface receives an 8-bit compressed code (A-law/ μ -law) or a 16-bit two's complement linear code from the voice signal processor (compressor). The transmit PCM interface logic ([Figure 5 on page 13](#)) controls the transmission of the data onto the PCM highway through the output port selection circuitry and the time and clock slot control block. The data can be transmitted on either edge of the PCLK, as selected in the *Device Profile*.

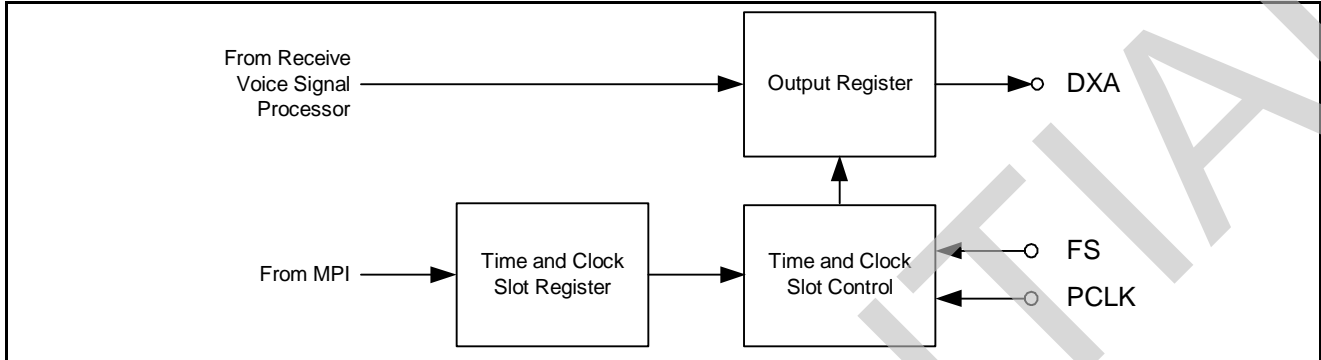


Figure 5 - Transmit PCM Interface

The *VP-API-II* allows the time slot of the selected channel to be programmed. The Transmit Time Slot Register is 7 bits wide and allows up to 128 8-bit time slots in each frame, depending on the value of the PCLK frequency, the encoding scheme, and whether Narrowband or Wideband modes are selected. Refer to [Table 1](#) below for the maximum number of available channels. Please note that linear mode requires two back-to-back time slots to transmit one voice channel. The data is transmitted in bytes with the most significant bit first. Wideband mode requires twice the number of transmit time slots as Narrowband linear mode.

Audio Mode	Encoding	1.024 MHz	2.048 MHz	4.096 MHz	8.192 MHz
Narrowband (8 kHz sampling)	8-bit compressed A-law/ μ -law	16	32	64	128
	16-bit linear	8	16	32	64
Wideband (16 kHz sampling)	16-bit linear	4	8	16	32

Table 1 - Maximum Number of Transmit or Receive Channels

3.1.1.2 Receive PCM Interface

The receive PCM interface logic (see [Figure 6](#)) controls the reception of data bytes from the PCM highway. 8-bit compressed (A-law/ μ -law) or 16-bit two's complement linear data is formatted and passed to the voice signal processor (expander).

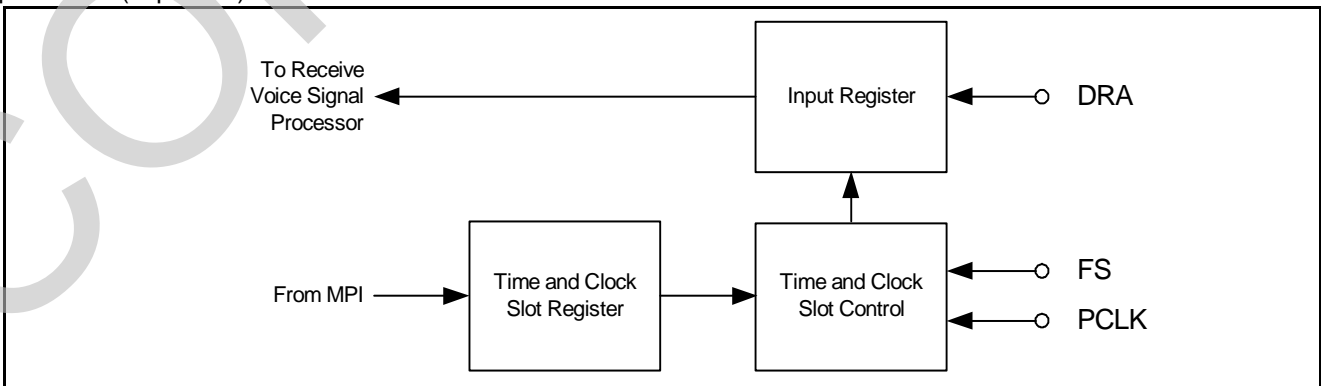


Figure 6 - Receive PCM Interface

The VP-API-II allows the time slot of the selected channel to be programmed. The Receive Time Slot Register is 7 bits wide and allows up to 128 8-bit time slots in each frame. Refer to [Table 1](#) for the maximum number of available channels. Please note that linear mode requires two back-to-back time slots to receive one voice channel. The data is transmitted in bytes with the most significant bit first. Wideband mode requires twice the numbers of receive time slots as Narrowband linear mode. Please refer to [“VP-API-II Functions for Speech Coding” on page 20](#) for more details about setting the codec mode and transmit and receive time slots. [Figure 7](#) illustrates data flow on the PCM highway with data transmitted on the negative PCLK edge.

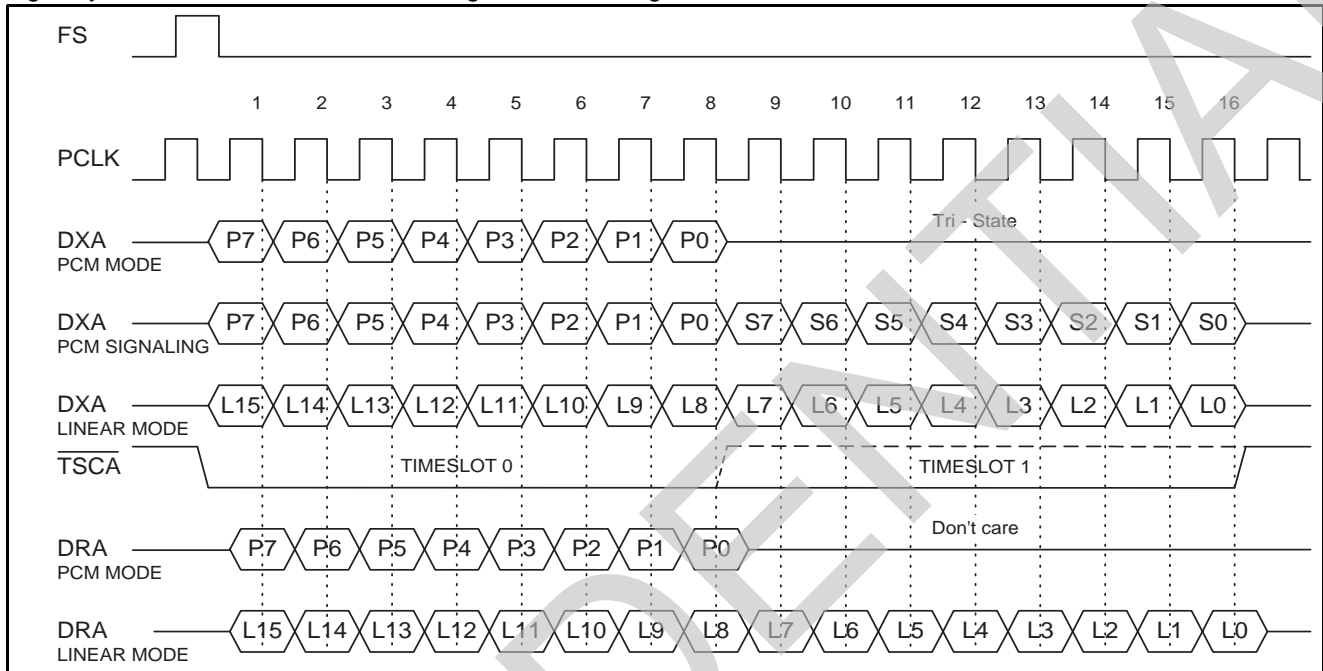


Figure 7 - PCM Data Flow Transmit and Receive Data (Transmit Data on Negative PCLK Edge)

3.1.2 Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) block communicates with external VoIP processors over a flexible half-duplex synchronous serial interface. This port is always a slave to the host processor's SPI port which provides clocking, chip select and initiates transactions.

3.1.2.1 SPI Signals

The SPI port physically consists of a serial data input (DIN) serial data output (DOUT), a data clock (DCLK), and a chip select (CS).

Signal Name	Type	Description
DCLK	Input	Serial Clock
$\overline{\text{CS}}$	Input	Chip or Slave Select, active low
DOUT	Output	Master Input Slave Output
DIN	Input	Master Output Slave Input

Table 1 - SPI Interface Signals

3.1.2.2 Interrupt Signal

An optional interrupt signal ($\overline{\text{INT}}$) is available to alert the host processor that the device has status information. It is recommended that the INT signal be tied to an interrupt-generating pin on the host processor. If the interrupt signal is not used, the host processor will need to regularly poll the device.

3.1.2.3 SPI Connection Diagram

Figure 8 below shows a the standard 4-Wire SPI connection to the host processor. The optional $\overline{\text{INT}}$ signal is also shown here.

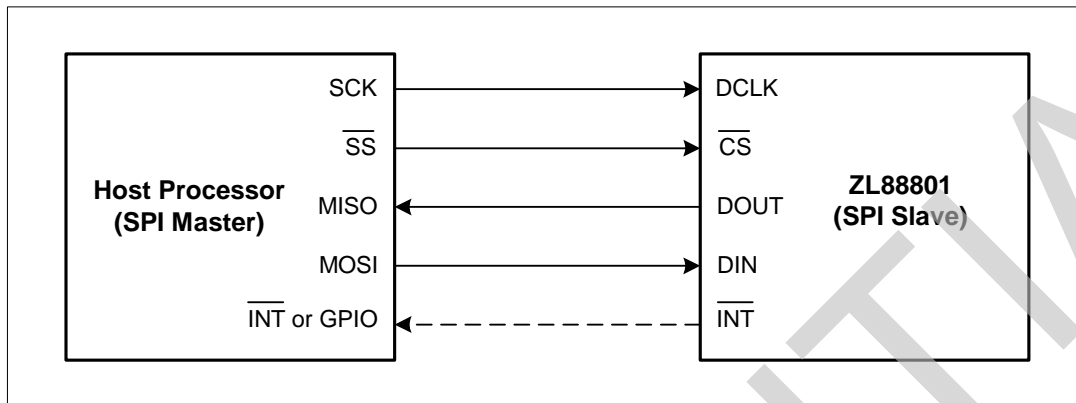


Figure 8 - 4-Wire SPI Connection to Host Processor

The ZL88801 device also supports 2- and 3-wire variants of the SPI interface in case of limitations on the host's serial port. Contact *Microsemi CMPG Customer Applications* for more information.

3.1.2.4 Chip Select Settings

Three chip select settings are supported:

1. Low for each Byte or Word: $\overline{\text{CS}}$ goes inactive between bytes or words. This mode is compatible with the legacy MPI mode.
2. Command Framing: $\overline{\text{CS}}$ goes inactive on some command boundaries. Commands cannot be aborted in this mode. All required bytes are expected even if $\overline{\text{CS}}$ is de-asserted in the middle.
3. $\overline{\text{CS}}$ Hard-Wired Low: This can be used when the ZL88801 device is the only slave on the SPI bus, but additional measures are required to acquire synchronization if it is ever lost.

Whenever $\overline{\text{CS}}$ goes inactive the bit state machine is reset. Also, if $\overline{\text{CS}}$ has not been active for *exactly* a multiple of 8 bit times, any byte which was partially received when $\overline{\text{CS}}$ goes inactive is ignored.

3.1.2.5 DCLK Polarity and Phase Settings

The SPI standards include four modes, defined by the polarity of DCLK and the phase relationship between data and DCLK. The clock polarity (CPOL) is determined by the idle state of DCLK. If the idle state is low, CPOL is 0. If the idle state is high, CPOL is 1. The clock phase (CPHA) is determined by which edge that data is valid. If the data is valid on the first edge of DCLK, CPHA is 0. If the data is valid on the second edge of DCLK, CPHA is 1.

The ZL88801 device supports SPI Modes 0 (CPOL = 0 and CPHA = 0) and 3 (CPOL = 1 and CPHA = 1) and contains a logic block to automatically conform to the selected Mode. SPI Modes 1 (CPOL = 0 and CPHA = 1) and 2 (CPOL = 1 and CPHA = 0) are not supported.

Since the host processor is the master, it must place DCLK in the proper idle state before $\overline{\text{CS}}$ is asserted.

3.1.2.6 Length of Data Transactions

The SPI port on the ZL88801 device supports 8-bit (byte-wide) transactions. 16-bit transactions are not supported.

3.1.2.7 SPI Interface Timing

Figure 9 below shows a typical timing interface diagram for SPI Mode 3.

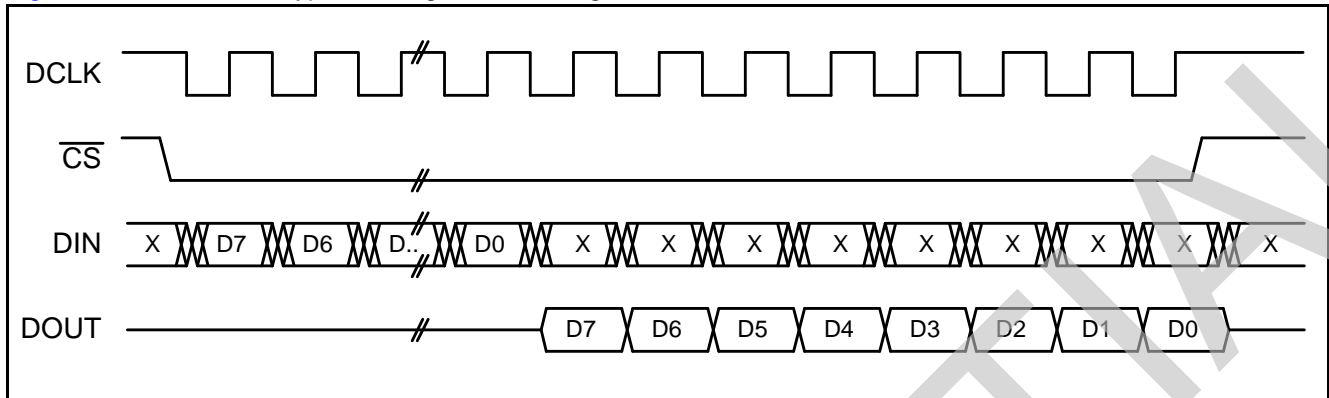


Figure 9 - SPI Mode 3 Interface Timing

3.1.2.8 MPI Interface

The Microprocessor Interface (MPI) is essentially a 4-Wire SPI Mode 3, with \overline{CS} low for each byte and 8-bit data transactions. This interface has been historically used on numerous Microsemi *VoicePort* devices such as the *VE880 Series*. With the MPI interface, 8-bit commands can be followed with additional bytes of input data, or can be followed by the ZL88801 device sending out bytes of data. All data input and output is MSB (D7) first and LSB (D0) last. All data bytes are read or written one at a time, with \overline{CS} going high for at least a minimum off period before the next byte is read or written. Only a single channel should be enabled during read commands.

All commands that require additional input data to the device must have the input data as the next N words written into the device (for example, framed by the next N transitions of \overline{CS}). All unused bits must be programmed to 0 to ensure compatibility with future parts. All commands that are followed by output data will cause the device to output data for the next N transitions of \overline{CS} going low. The ZL88801 device will not accept any commands until all the data has been shifted in or out. The output values of unused bits are not specified.

Figure 10 shows an example MPI mode interface timing, with DOUT changing on the negative edge of DCLK. DIN is sampled on the rising edge of DCLK.

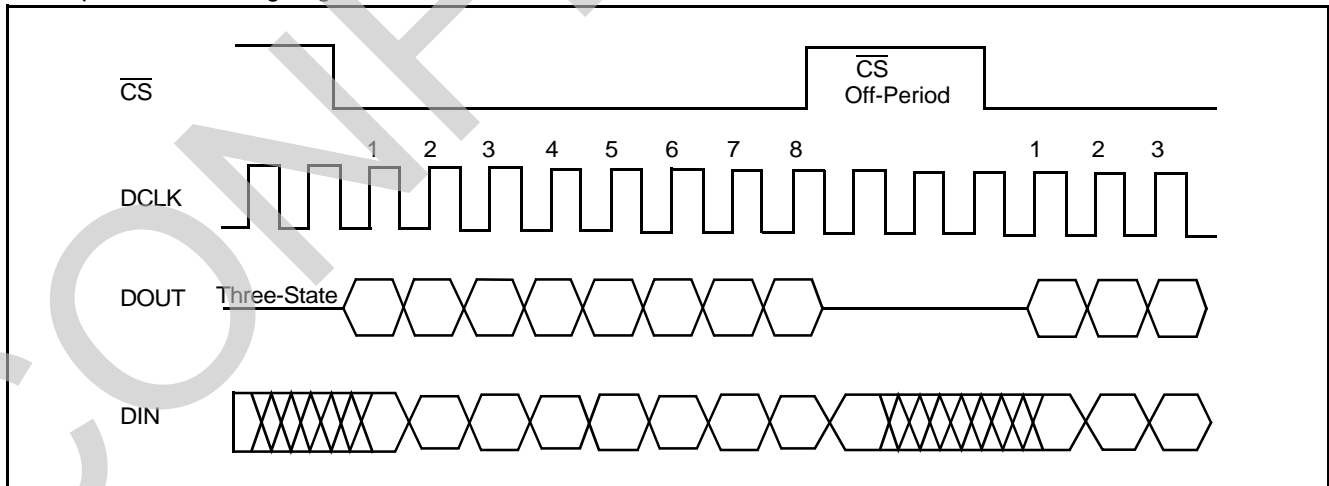


Figure 10 - MPI Interface Timing

An MPI cycle is defined by transitions of \overline{CS} and DCLK. If the \overline{CS} lines are held in the high state between accesses, the DCLK may run continuously with no change to the internal control data. Using this method, the same DCLK can be run to a number of ZL88801 devices and the individual \overline{CS} lines will select the appropriate device to access. Between command sequences, DCLK can stay in a static state indefinitely with no loss of internal control

information regardless of any transitions on the \overline{CS} lines. Between bytes of a multi byte read or write command sequence, DCLK can also stay in a static high state indefinitely. If the host controller has a single bidirectional serial data pin, the DOUT pin of the ZL88801 device can be connected to its DIN pin.

If a low period of \overline{CS} contains less than 8 positive DCLK transitions, it is ignored. If it contains 8 or more positive transitions, the first 8 transitions will be interpreted as the first byte and the next 8 transitions will be treated as the second byte, etc. This allows the chip select input to be tied low permanently if desired.

3.1.3 ZSI Serial Mode

An alternative host interface supported by the ZL88801 device is a 4-wire interface called ZSI (see [Figure 11](#).) It is active when the \overline{ZSI} pin is tied to ground. Note that the ZSI interface must also be supported by the host processor or by a PCM/SPI to ZSI bus translator device such as the Le88004.

This interface supports separate PCM and control channels based on the level of the ZCLK. For receive signals (ZSYNC, ZMOSI) PCM data is valid when ZCLK is high and control data is valid when ZCLK is low. For the transmit ZMISO, PCM data is valid when ZCLK is low and control data valid when ZCLK is high. The control data is framed byte by byte in a similar way to the separate MPI interface on other VoicePort family products. Chip select status is carried on the ZSYNC signal and requires a chip select off time of at least one clock period. Interrupt status is communicated on the ZMISO control channel whenever the previous ZSYNC CS status is low. This is achieved by XORing the DXA data with the active high INT status.

The ZCLK rate can be 1.024 MHz, 1.536 MHz, 2.048 MHz, 3.072 MHz, 4.096 MHz, 6.144 MHz, or 8.192 MHz. The ZL88801 must be programmed to match the applied ZCLK frequency using the control channel. Both PCM and control data are transferred at the same ZCLK rate over the ZSI.

3.1.3.1 ZSI Timing

[Figure 11](#) shows the protocol for multiplexing the PCM and control signals onto the ZSI.

Note that chip select must be de-asserted at least one clock between bytes or a reset will be generated after 16 clocks.

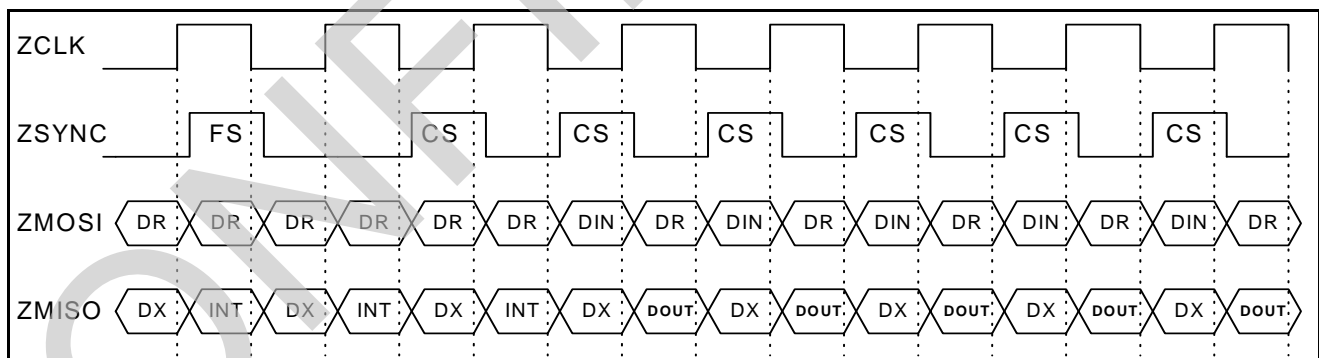


Figure 11 - ZSI Timing Protocol

3.2 Input / Output Block

The ZL88801 device features two dedicated and two optional general purpose input / output (I/O) pins. I/O₁ and I/O₂ can be configured by the user as inputs, outputs, or as high-current LED or relay drivers. I/O₂₁ and I/O₂₂ may be configured as general purpose digital inputs or outputs or as voltage sense pins (VS1 and VS2). When configured as inputs, I/O₂₁ and I/O₂₂ are capable of generating interrupts.

3.3 Voltage Sense

The voltage sense block allows the measurement of analog voltages at the pins VS1 and VS2, when they are configured as analog inputs. This makes it possible to monitor VSW and VBAT in real time and make switcher optimizations based on their levels and to measure power consumption. An external 1.0-MΩ, 1% resistor needs to be connected between each of these pins and the voltages to be measured.

3.4 Voice Signal Processor

This block, shown in [Figure 12](#), performs digital signal processing for the transmission and reception of voice. It includes G.711 compression/decompression, impedance matching, filtering, gain scaling, DTMF generation and general-purpose tone generators for each channel. Additionally Caller ID (FSK and DTMF) and metering generation are provided.

This block performs the codec and filter functions associated with the four-wire section of the subscriber line circuitry in a digital switch. These functions involve converting an analog voice signal into digital PCM samples and converting digital PCM samples back into an analog signal. During conversion, digital filters are used to band-limit the voice signals.

The user-programmable filters perform the following functions:

- Sets the receive and transmit gain
- Performs the transhybrid balancing function
- Permits adjustment of the two-wire termination impedance
- Provides frequency attenuation adjustment (equalization) of the receive and transmit paths

Country- and standards-specific *Profiles* are available from Microsemi with pre-computed digital filter coefficients. The PCM codes can be either 16-bit linear two's-complement or 8-bit GR companded A-law or μ-law.

The ZL88801 device is architected in such a way as to reduce the real time demands on the host processor. An integrated cadencer/sequencer controls ringing and call progress tone generation. This feature can also generate timed interrupts and substantially reduces the user's need to implement time critical functions.

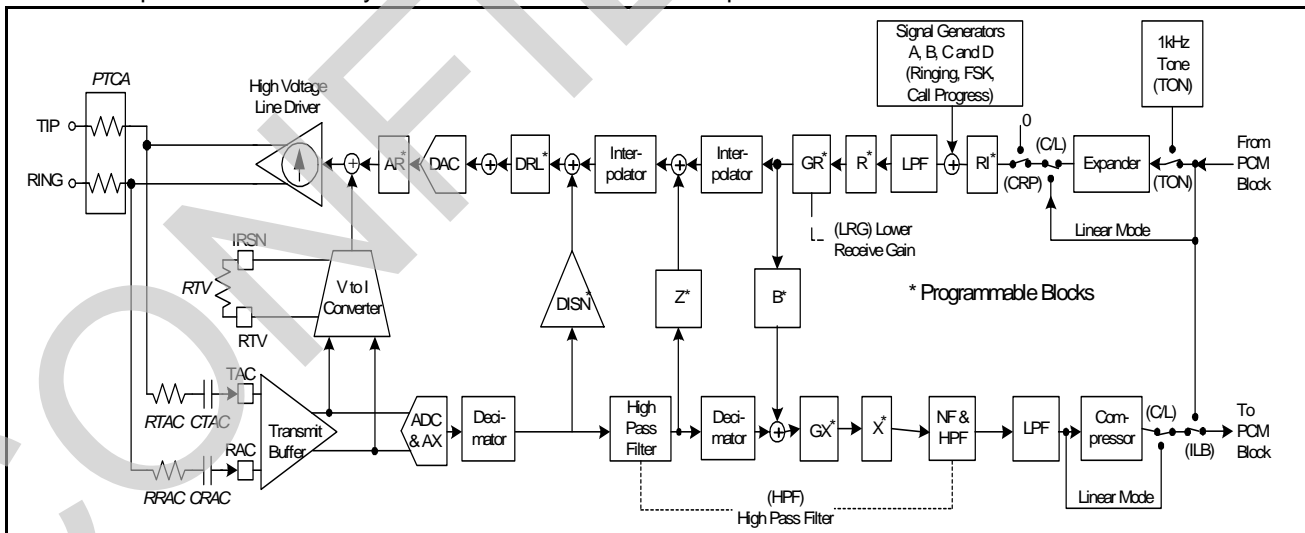


Figure 12 - Voice Signal Processing Block Diagram

3.4.1 Impedance Synthesis

The analog impedance synthesis loop is comprised of the SLIC block, the AC sense path components, the transmit amplifier, and a voltage to current converter. An external resistor, R_{TV} , synthesizes the nominal impedance in the

analog domain. Additional refinement of the impedance is done in the DSP via the Digital Impedance Scaling Network (DISN) and Z-blocks.

The DISN path is comprised of the voice A/D and its first stage of decimation, a DISN, and the voice DAC. The 8-bit DISN synthesizes a portion of the AC impedance which appears in parallel with R_{TV} and is used to modify the impedance set by the external analog network.

The Z Filter is a programmable digital filter providing an additional path and programming flexibility over the DISN in modifying the transfer function of the synthesis loop. Together R_{TV} , DISN, and the Z Filter enable the user to synthesize virtually all required telephony device input impedances.

3.4.2 Frequency Response Correction and Equalization

The voice signal processor contains programmable filters in the receive (R) and transmit (X) directions that may be programmed for line equalization and to correct any attenuation distortion caused by the Z Filter.

3.4.3 Transhybrid Balancing

The voice signal processor's programmable B Filter is used to adjust transhybrid balance. The filter has a single pole Infinite Impulse Response (IIR) section and an eight-tap Finite Impulse Response (FIR) section, both operating at 16 kHz.

3.4.4 Gain Adjustment

The transmit path of the FXS has two programmable gain blocks. Gain block AX is an analog gain of 0 dB or 6.02 dB (unity gain or gain of 2.0), located immediately before the A/D converter. GX is a digital gain block that is programmable from 0 dB to +12 dB, with a worst-case step size of 0.1 dB for gain settings below +10 dB, and a worst-case step size of 0.3 dB for gain settings above +10 dB. The filters provide a net gain in the range of 0 dB to 18 dB. The receive voice path has three programmable gain blocks. GR is a digital loss block that is programmable from 0 dB to 12 dB, with a worst-case step size of 0.1 dB. DRL is a digital loss block of 0 dB or 6.02 dB. AR is an analog gain of 0 dB or 6.02 dB (unity gain or gain of 2) or a loss of 6.02 dB (gain of 0.5), located immediately after the D/A converter. This provides an attenuation in the range of 0 dB to 18 dB.

The gain adjustment block can also be accessed by a *VP-API-II* function directly, without using an *AC FXS Profile*.

Function Name	Description
VpSetRelGain()	Adjusts transmit and/or receive gain up to +/-6 dB. Relative gain of 1 (0 dB) defined as initial value programmed by <i>AC FXS Profile</i> . Note that the supplied <i>AC FXS Profiles</i> have initial gains of -6 dB receive and 0 dB transmit
VpSetOption()	VP_OPTION_ID_ABS_GAIN -- Programs absolute gain

Table 2 - VP-API-II Functions for Gain Adjustment

3.4.5 Transmit Signal Processing

In the transmit path (A/D) of the FXS, the AC Tip - Ring analog input signal is sensed by the TAC and RAC pins, buffered, amplified by the analog AX gain and sampled by the A/D converter, filtered, companded (for A-law or μ -law), and made available to the PCM blocks. If linear format is selected, the 16-bit data will be transmitted in two consecutive time slots starting at the programmed time slot. The B, X, and GX digital filter blocks are user-programmable digital filter sections. The first high-pass filter is for DC rejection, and the second high pass and notch filters reject low frequencies such as 50 Hz or 60 Hz.

3.4.6 Receive Signal Processing

In the receive path (D/A) of the FXS port, the digital signal is expanded (for A-law or μ -law), filtered, interpolated, converted to analog, and driven onto TIP and RING by the SLIC block. The AR, DRL, DISN, Z, R, and GR blocks are user-programmable filter sections.

3.4.7 Speech Coding

The A/D and D/A conversion follows either the A-law or the μ -law standard as defined in *ITU-T Recommendation G.711*. Alternate bit inversion is performed as part of the A-law coding. Linear code is an option on both the transmit and receive sides of the device. Two successive time slots are required for linear code operation. The linear code is a 16-bit two's-complement number which appears sign bit first on the PCM highway.

3.4.8 Wideband Operation

Each channel on the ZL88801 device can be set to operate in either Narrowband or Wideband mode under *VP-API-II* software control. In the Wideband mode, the nominal voice bandwidth is expanded and starts at 50 Hz or 200 Hz (depending on whether or not a high-pass and 50/60 Hz notch filter is enabled) to 7000 Hz to provide better voice quality. The *AC FXS Profiles* must be programmed with wideband coefficients. In the Wideband mode, the increased data rate is processed by accessing a second set of timeslots equally spaced in the frame.

Function Name	Description
VpSetOption()	VP_OPTION_ID_TIMESLOT -- Programs transmit and receive timeslot. VP_OPTION_ID_CODECS -- Programs speech coding mode.
VpGetOption()	VP_OPTION_ID_TIMESLOT -- Retrieves current values of transmit and receive timeslot. VP_OPTION_ID_CODECS -- Retrieves current speech coding mode.

Table 3 - VP-API-II Functions for Speech Coding

3.5 Signal Generation

Up to four programmable digital signal generators are available for the FXS channel. These signal generators can be programmed for multi-tone generation, amplitude and frequency modulation, and or the generation of complex sine, triangular or trapezoidal signals.

3.5.1 Multi-Tone Generation

In this configuration, up to four tone generators are summed into the output path, as shown in [Figure 13](#). The Bias generator produces a DC bias that can be used to provide DC offset during ringing or DC test signals during diagnostics. This generator is automatically enabled when entering the VP_LINE_RINGING state.

Function Name	Description
VpSetLineTone()	Provides simultaneous generation of up to four tones. Note that with Tone Cadencing, tones can be enabled/disabled individually to provide Special Indication Tone (SIT).
VpSetLineStyle()	VP_LINE_RINGING and VP_LINE_RINGING_POLREV -- Uses Signal Generator A (and B for trapezoidal type ringing) with user selected frequency, offset, amplitude, and type.
VpSendSignal()	VP_SENDSIG_DTMF_DIGIT -- Generates a DTMF digit on the line.
VpInitCid()	Sending Caller ID (FSK and DTMF message data supported) on an FXS line. Providing Type 2 CID Alerting tone.
VpSendCid()	
VpContinueCid()	

Table 4 - VP-API-II Functions Using Signal Generators

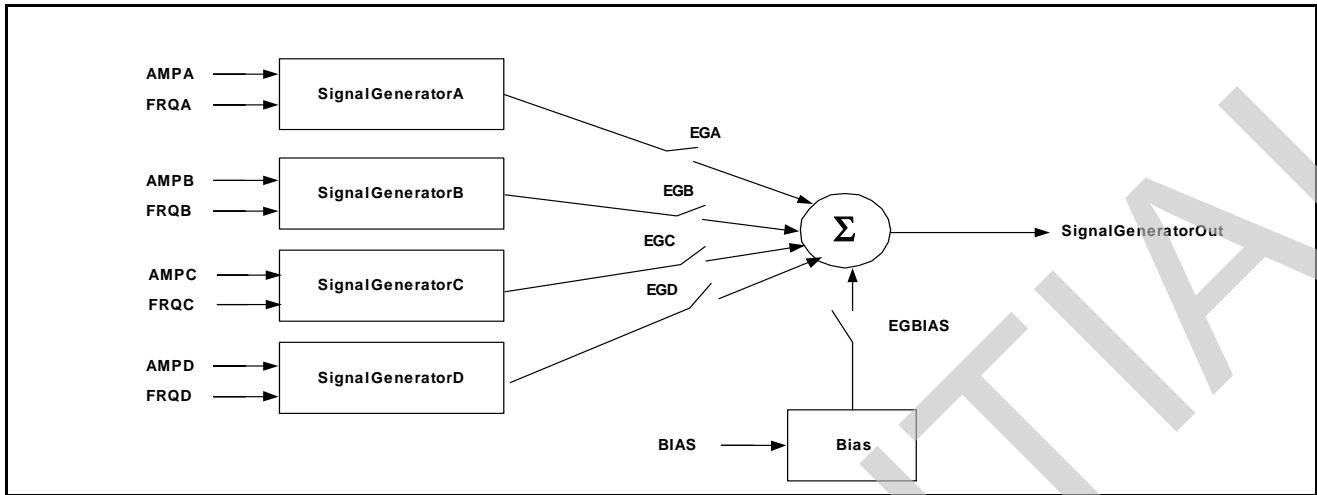


Figure 13 - Multi-Tone Generation

Signal Generator A is also used by the Microsemi *VeriVoice* test suites to produce slow ramps. This allows a complex sequence of diagnostic test voltages to be generated in a controlled manner without generating unwanted transients on the line.

Each generator has independent frequency and amplitude parameters. The frequency accuracy is basically the same as the crystal accuracy of the system.

The EGA/B/C/D bits are controlled by the *VP-API-II* Cadencing engine.

3.5.2 Frequency and Amplitude Modulation

The signal generators can also be used to generate frequency- and/or amplitude-modulated tones in conformance with worldwide Howler (receiver off-hook) and call progress tone requirements. Frequency modulation is performed in a dedicated hardware block, while amplitude modulation is performed in software by *VP-API-II*.

To generate frequency-modulated tones, Signal Generator A is configured as a modulator, while Signal Generator D is configured as a carrier. The output of Signal Generator A is the frequency input to Signal Generator D. Note that Signal Generator A needs a positive DC bias so that its output is always positive. Caller ID generation is not available while frequency modulation is taking place. [Figure 14](#) shows the configuration for modulation. Note that Signal Generators B and C are available to be summed to the frequency-modulated signal, if necessary.

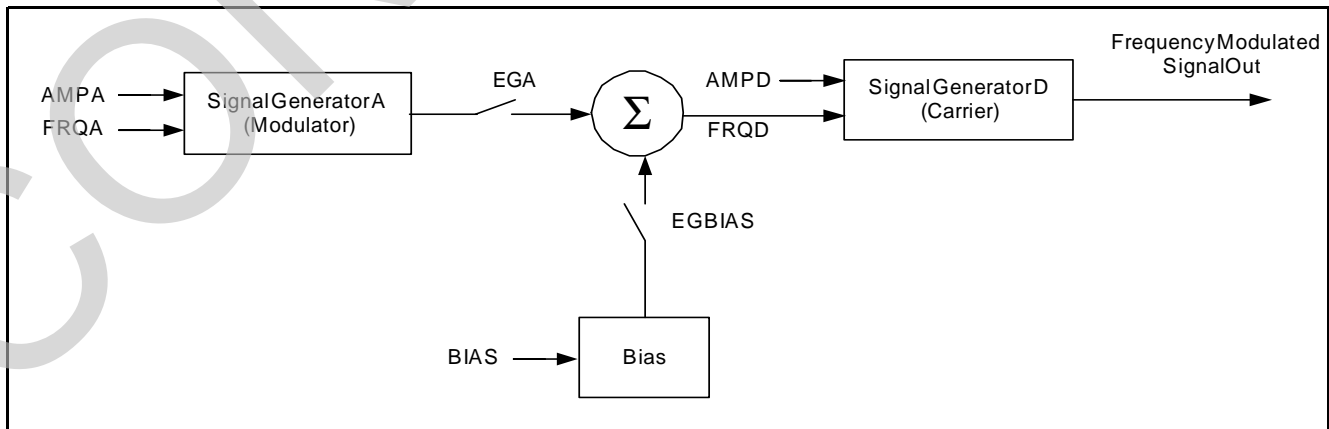


Figure 14 - Frequency Tone Modulation

Frequency and amplitude modulation allow the ZL88801 device to meet exacting Howler tone requirements such as those specified in *BTNR 1080 Version 15* and *Draft 960-G, NTT Edition 5* and *Austel AUS002:2001*.

[Table 5](#) lists the *VP-API-II* functions that are used for Howler tone generation.

Function Name	Description
VpSetLineState()	VP_LINE_HOWLER -- Places the device in a high gain state for Howler tone generation.
VpSetLineTone()	Provides simultaneous generation of up to four tones. Note that with Tone Cadencing, tones can be enabled/disabled individually or modulated in order to generate Howler tones.

Table 5 - VP-API-II Functions for Howler Tone Generation

3.5.3 Triangular and Trapezoidal Signal Generation

The signal generators can also be used to generate trapezoidal waveforms for ringing. [Figure 15](#) shows a configuration that is typically used to generate trapezoidal waveforms. Triangular waveforms can also be generated.

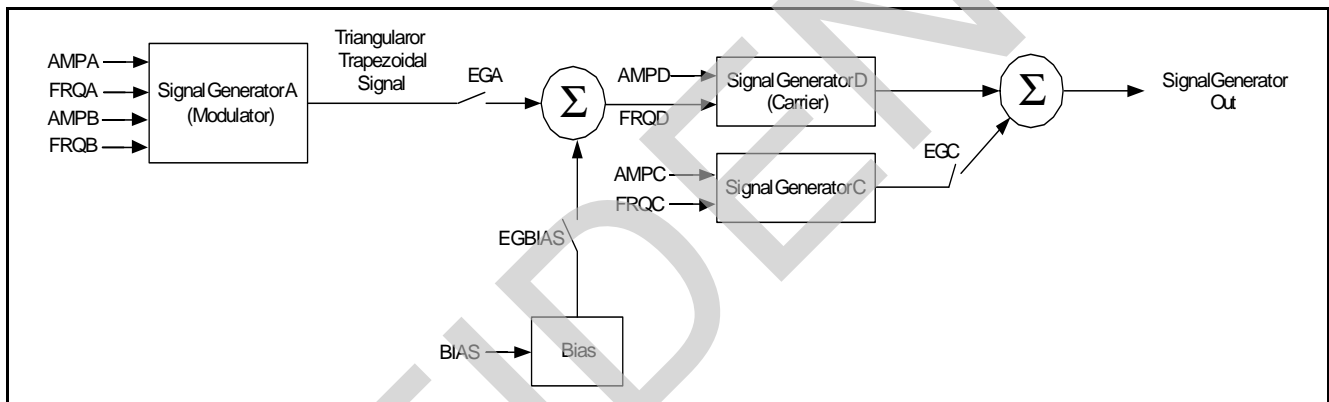


Figure 15 - Trapezoidal Signal Generation

3.6 Low Power DC Feed

The ZL88801 device supports *Low Power Idle Mode (LPIM)*, which reduces the system power consumption during idle (On-Hook) state. *LPIM* provides a weak DC feed capable of at least 5 mA to the line and reacts to a change in the line voltage to create an off-hook indication when a telephone goes off-hook.

3.7 Normal DC Feed

DC feed is active in normal idle, talk and ringing states and the programmed characteristics appear between Tip and Ring. *VAS* is chosen to ensure that sufficient headroom is available for the amplifiers when On-Hook to support On-Hook transmission with the programmed open circuit (VOC) voltage. Values programmed in device for *VAS*, *VOC*, and *ILA* are determined during *VpCallLine()* to ensure circuit performance. Please refer to [Figure 16, "Active State I / V Characteristic" on page 23](#) for the Active state I/V characteristic feed curve for *Rfeed* = 200 Ω.

The *DC Profile* produces a DC feed curve at Tip and Ring when the fuse resistors are inside the feedback loop formed by the *RTDC* and *RRDC* feedback network. Note that the value of the combined Tip and Ring feed resistors *Rfeed* is programmable to 0, 50, 100, or 200 Ω to correspond to the choice of PTCs or fuse resistors that are used. Refer to [Figure 47, "Profile Wizard - DC Profile Configuration Example" on page 76](#) for more details.

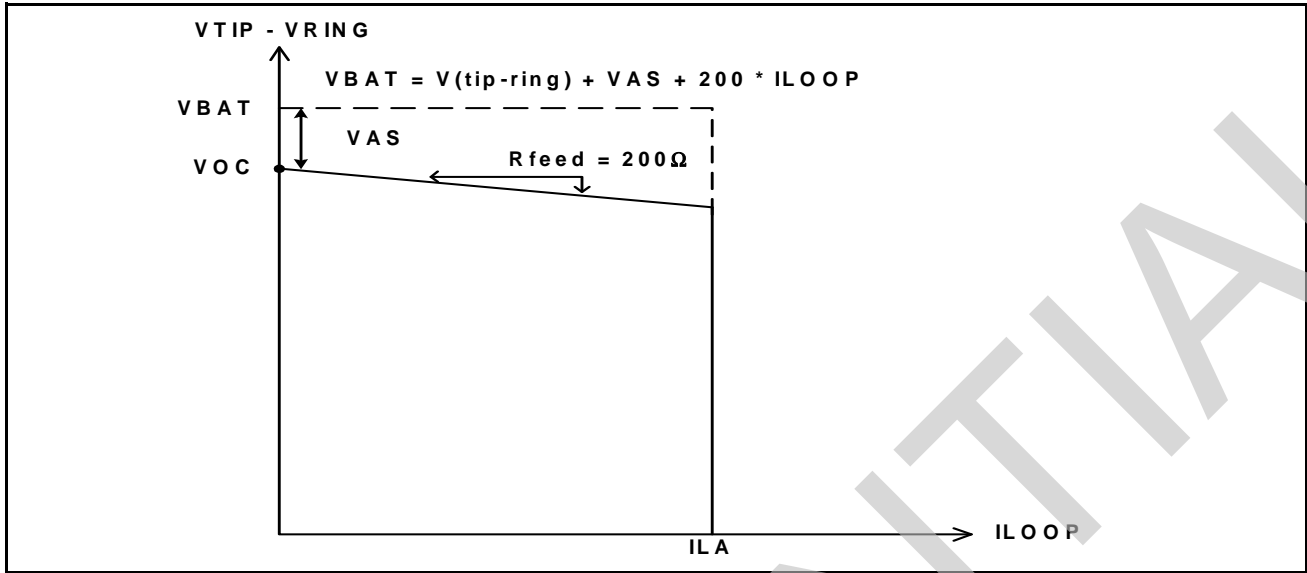


Figure 16 - Active State I / V Characteristic

3.8 Test Feed

The Tip Open test state presents the DC feed characteristic shown in [Figure 16](#) between the Ring lead and ground.

3.9 Ringing

The ZL88801 device supports balanced ringing with fixed supplies.

3.9.1 Balanced Ringing

Internal balanced ringing drives the subscriber line with balanced ringing voltage waveforms (see [Figure 17](#)). In the balanced ringing mode, the ringing signal is driven differentially, thus maximizing the ringing signal swing. In this mode, the SLIC appears to the subscriber line as a voltage source with an output impedance of 200 Ω. The maximum ringing signal possible in the balanced mode is 85-V_{PK}, corresponding to the maximum AC + DC voltages.

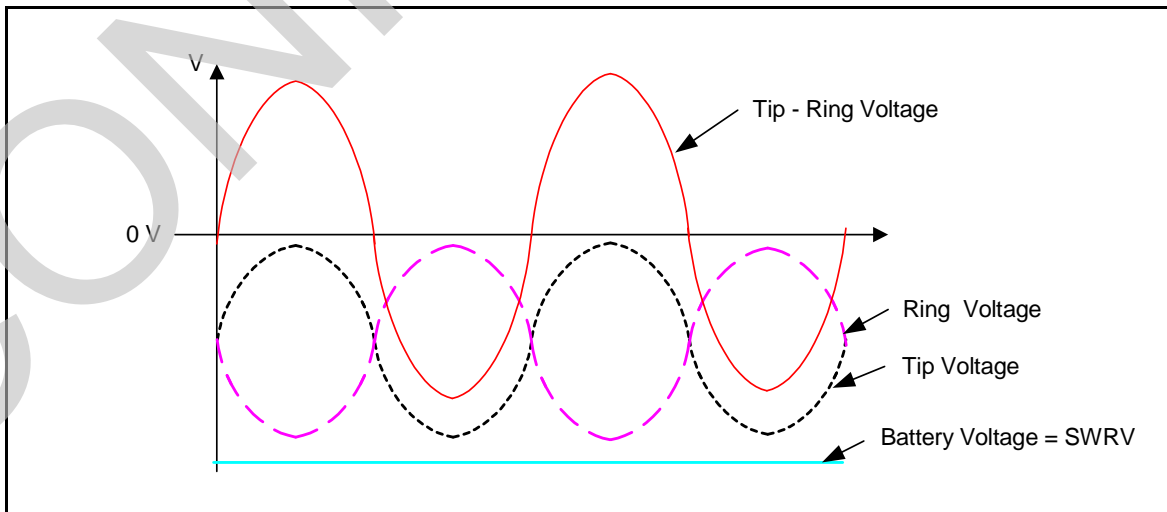


Figure 17 - Balanced Ringing with Fixed Supply

3.9.2 Adaptive Ringing Amplitude

The ZL88801 device supports adaptive ringing amplitude. Adaptive ringing amplitude limits the maximum power that is generated during ringing at or below a specified level.

3.9.3 Switch Hook Detection

The FXS supervision circuits of the ZL88801 device provide debounced off-hook indications to an external processor via the host port interface. The supervision circuit compares a scaled version of the Tip-Ring current to a programmed off-hook threshold, TSH. The output of the comparator is debounced by a programmable debounce timer, DSH. A debounced *Off-Hook* indication generates an interrupt to the host processor.

3.9.4 Ring Trip Detection

Ring trip is the process of sensing a subscriber's off-hook event during ringing. This is accomplished by sensing the rise in loop current which occurs when a phone goes Off-Hook. The ZL88801 device can detect ring trip when the ringing signal is purely AC and/or when the ringing signal has a DC bias on it. To do so, the ring trip algorithm is automatically altered internally by the ZL88801 device based on the user-programmed parameters.

The ring trip detector uses the Tip-Ring current as an input. This current is rectified so that AC + DC ring trip can be detected. The output of the rectified signal is compared to a programmable ring trip threshold and the output is digitally debounced. The output is blanked upon ring entry to avoid false ring trips.

The ring trip detection circuit provides debounced ring trip indications to an external processor via the host port interface. The ring trip circuit compares a scaled version of the Tip-Ring current to a programmed Ring Trip Threshold (RTTH). The output of the comparator is processed by the ring trip algorithm on a cycle by cycle basis to provide immunity to false ring trips. In addition, spending more than 50% of the time in ringing current limit will generate a trip indication. A positive ring trip occurs if a trip indication is present for one (optional) or two (default) complete ring cycles, and an interrupt can be raised to the host processor. For AC-only ringing, the signal is half-wave rectified.

The Ring Trip Threshold (RTTH), integration method (positive half-wave for AC only or full-wave for AC+DC), the number of cycles (1 or 2), and Ringing Current Limit (ILR) are programmed in the *Ringing Profile*. Microsemi provides a number of example *Ringing Profiles* for most common ringing requirements incorporating the ringing signal parameters and corresponding ring trip settings.

The following equations can be used to select new ring trip settings when using different ringing waveforms and different loads. They allow the ratio of the open circuit ringing voltage to the ringing threshold current to vary by +/-20%, which is conservative.

Name	Description
AMPA	Amplitude of signal generator A which is used for ringing
FREQA	Frequency of signal generator A which is used for ringing
BIAS	DC bias for ringing
RTDCAC	Ringing trip based on AC only or Battery Backed (DC) Ringing
RTTH	Ringing trip threshold in 0.5 mA steps from 0 to 63.5 mA
ILR	Ringing current limit programmed in 2 mA steps. ILR = 18 to 112 mA
HOOK	Interrupt in signalling register indicating a ring trip occurred

Table 6 - Ring Trip Parameters

For AC only ringing, RTDCAC is 1 and the ringing current is half-wave rectified and averaged over a ringing cycle. If this result exceeds the RTTH threshold for two successive cycles, the HOOK bit will be set. This method limits the supported loop length x depending on the minimum must not trip ringing impedance (R_{mnt} in Ohms) and allowing for errors in the applied ringing voltage and trip level. The maximum loop resistance is given by:

$$R_{LOOP(max)} = 0.67 \times R_{mnt} - R_{phone} - 66\Omega$$

RLOOP (max) excludes the DC resistance of the phone (Rphone, typically 430 Ω in the U.S.), and the fuse resistance if DC line sensing is behind the fuse resistors.

For a sinusoidal ringing waveform of VRING (RMS) volts, and Rmnt impedance, the following ring trip settings should be used:

$$RTTH = \frac{0.54 \times VRING}{R_{mnt} + 200\Omega}$$

$$ILR = \frac{1.4 \times VRING}{R_{mnt} + 200\Omega}$$

In general for short loop applications, it is recommended to use AC ring trip even in the presence of a DC bias that could allow a DC based ring trip, and the above equations still apply. Note that the ringing source impedance is nominally 200 Ω.

3.10 Subscriber Line Testing

The ZL88801 device provides the ability for the user to perform the *Telcordia GR-909-CORE / TIA-1063* diagnostic testing for the voice ports. In Test mode, a variety of input signals can be read from the voice ADC converter. These signals include the switching regulator voltage and the line DC and AC voltages.

3.10.1 VeriVoice Professional Test Suite Software for the ZL880

VeriVoice Professional Test Suite Software is an advanced test suite featuring the following tests:

- Line Voltage: Checks for hazardous and foreign AC and DC voltages.
- Receiver Off-Hook: Checks for longitudinal fault, off-hook resistive fault and receiver off-hook.
- Regular REN: Tests the impedance of the line and returns a fail if the Ringer Equivalence Number (REN) is too low or high.
- Electronic REN: Provides REN Tip to Ring, Tip to ground and Ring to ground based on capacitance
- Resistive Fault: Measures three-element resistance.
- GR-909-CORE / TIA-1063: Performs all of the *GR-909-CORE* outward tests in the correct sequence.
- Capacitance: Measures three element capacitance
- Master Socket: Detects master socket terminations
- Cross Connect: Detects cross connected FXS
- Loopback: Enables receive-to-transmit signal loopback using two different methods
- Read Loop Conditions: Measures voltages between Tip and Ring, Tip to ground, Ring to ground, and VBAT to ground. Also measures metallic and longitudinal line currents in supported states.
- Read Battery Conditions: Reads the battery voltages connected to the line circuit.
- DC Voltage Self-Test: Verifies that the line circuit has the ability to drive the voltage ranges required for the normal operation of the line circuit.
- DC Feed Self-Test: Measures the voltage and current across a known internal test termination using the *DC Profile* that has been programmed.
- Ringing Self-Test: Verifies ring signal generation, drive capability, and ring trip.
- On/Off-Hook Self Test: Creates on-hook and off-hook conditions on the line using the internal test termination and verifies that they are properly reported.

3.11 Manufacturing Testing

The ZL88801 is supported by the *VeriVoice Manufacturing Test Package (VVMT)*, a platform-independent 'C' source code module which facilitates factory testing and calibration of assembled boards with this and other Microsemi voice products.

3.12 Metering

The ZL88801 device is capable of $0.5 V_{RMS}$ metering into a 200Ω metering load at either 12 kHz or 16 kHz. Smooth metering application and abrupt metering application are supported. A typical metering sequence is shown below in [Figure 18](#).

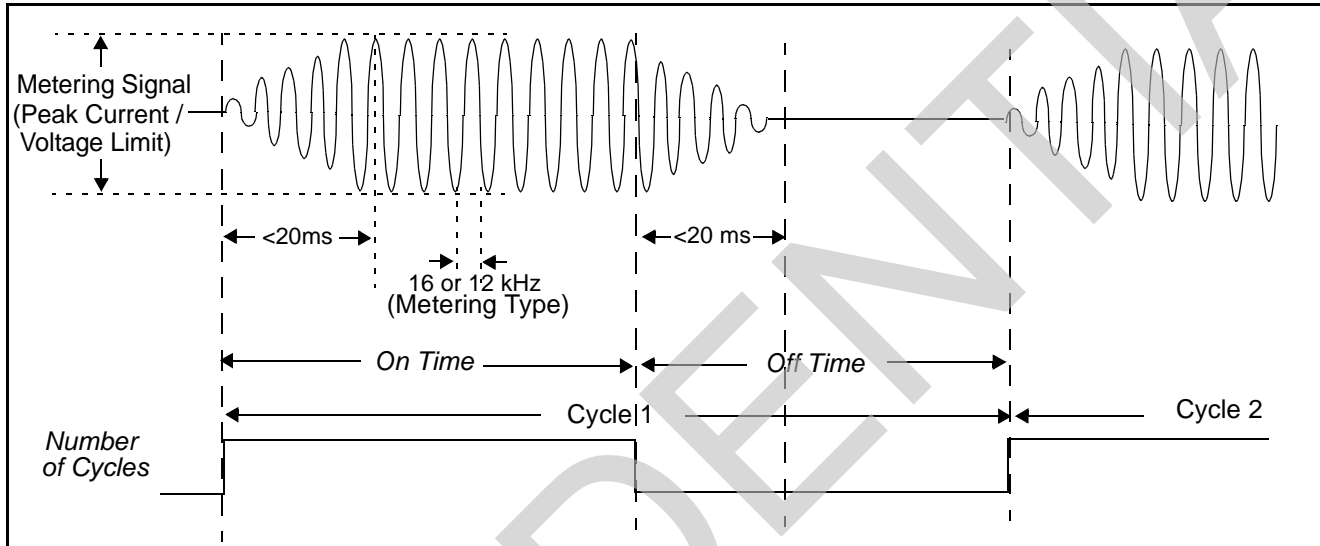


Figure 18 - Metering Pulse Definitions

The metering on time, off-time, and number of cycles are programmed in the *VP-API-II* function `VpStartMeter()`. This off-loads much of the timing from the host processor. Note that a ramp up / ramp down period of up to 20 ms is possible. The metering type (12 or 16 kHz), peak current and voltage limit are set in the *Metering Profile* and are used by the *VP-API-II* function `VpInitMeter()`. Note that in a normal configuration, some of the metering current flows into the CTD and CRD capacitors, so that the current sourced into an external load will be less than that programmed peak current parameter even when the metering voltage limit is not reached. The metering voltage that reaches the load is also dependent on the total fuse resistance and the minimum load resistance, which is typically 200Ω .

3.13 Switching Regulator Controller

The switching regulator controller and the external power train circuitry provide a flexible switching regulator that automatically produces the negative supply voltage required to drive each line. The switching regulator has three modes of operation: Low, Medium, and High, which roughly correspond with On-Hook, Off-Hook, and Ringing states. These modes of operation provide for increased efficiency over a wide load range. Switching regulator parameters are set in the *Device Profile*.

The ZL88801 controller supports the following switching regulator types.

3.13.1 Shared Inverting Buck-Boost Automatic Battery Switching (BBABS)

The recommended BBABS switching regulator circuit is shown in [Figure 40 on page 59](#). The regulator shown is an inductor based inverting buck-boost configuration with output voltage doubler. The circuit adds the applied VSW voltage to the doubled battery voltage. The BBABS switching regulator circuit has been crafted to use low cost, low voltage components while maintaining high performance and high efficiency. The switching regulator circuit is

capable of simultaneous ringing of both lines without clipping. The control switching frequency for BBABS is 24 kHz for Low Power mode and 128 kHz for Medium and High Power modes.

Switcher Y has been configured to generate one fixed supply voltage, low battery voltage VBATL. The VBATL value is programmable. The VBATL supply is regulated but the switching circuit provides good VBATH regulation when VBATL is loaded. VBATH is obtained by the formula:

$$VBATH = -(VSW + (2 * |VBATL|) - 2 V).$$

VBATL can be programmed to a low value for supervision and active states and can be programmed to a high value to perform ringing. With a VSW of +12 V, a VBATL setting of -25 V produces a VBATH of -60 V, these voltages are adequate for line supervision and active off-hook operation. VBATL can be increased to -35 V to produce a VBATH of -80 V and open circuit ringing of 50 V_{RMS}; or VBATL can be increased to -40 V to produce a VBATH of -90 V and open circuit ringing of 60 V_{RMS}. For the short period of time that one channel is ringing, the adjacent channel will consume more power due to the elevated battery voltages, but overall performance in that channel will not be affected. VBATH is applied to the VBAT₃ device pin and VBATL is applied to the VBAT₁ and VBAT₂ device pins.

The LFC pins support a soft start for the switching regulator controllers by filtering the internally generated switcher output reference using an external capacitor. LFC₁ is associated with Switcher Y, and LFC₂ is associated with Switcher Z. The pole is set with a nominal 4 kΩ internal resistance, allowing a 0.1 μF capacitor to provide a 10 ms ramp time. It is also possible to control the power-up of the switching regulators by appropriate use of the switcher power modes, eliminating the need for external capacitors. If the switcher controller is not being used, the corresponding LFC pin can be left open.

3.13.2 Shared Tracking Battery (STB)

The recommended STB switching regulator circuit is shown in [Figure 42 on page 63](#). The STB switching circuit produces a single battery voltage that is shared by both channels. STB supports one line ringing a 3 REN ringing load up to 85-V_{PK} while the other line is off-hook. Just before entering the ringing state the power supply ramps up to a pre-programmed voltage that is sufficient to support the programmed ringing waveform. The control switching frequency for STB is 96 kHz for Low, Medium, and High Power modes.

The variable output tracking switching regulator is used to generate the VBAT supply voltage based on line usage. VBAT is dynamically determined by the line that requires the most negative voltage. An offset voltage (set by the VAS DC feed parameter) is added to the measured Tip-Ring voltage when on hook and the resulting signal controls the output of the switching regulator. When loop current is drawn in the Active or Ringing states, an additional offset defined as Rfeed * Iloop is added, to ensure overhead is maintained with up to 160 Ohms of total fuse resistance present in the DC feed loop. This architecture enables the switching regulator output voltage to generate the required voltage to feed the line whether in the on-hook, off-hook or ringing states. The ZL88801 controller detects over current events and terminates the output pulse as necessary on a cycle by cycle basis.

The output of the STB circuit splits into three separate battery voltages, VBAT₁, VBAT₂, and VBAT₃. VBAT₁ provides the battery supply for channel 1, VBAT₂ for channel 2, and VBAT₃ serves as a SLIC bias.

3.14 Tip/Ring Protection

To minimize BOM cost, Tip/Ring protection on the ZL88801 can be configured to utilize the Microsemi shared fixed voltage protector scheme. This protection scheme is compatible with the STB supply implementation. This protection scheme is illustrated in [Figure 41 on page 61](#). As shown, the PTC, diode bridge, and fixed voltage protector circuitry will protect against lightning, power line induction, power cross, and AC or DC fault conditions.

If preferred, individual line battery referenced overvoltage SLIC protection (as shown in the [“BBABS Line Interface Circuit” on page 57](#)) can be used with the ZL88801.

Please refer to the *ZL880 Protection Schemes Application Note, Document ID# 146139* for additional details on protection options.

4.0 Electrical Specifications

4.1 Absolute Maximum Ratings

Stresses above those listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Ambient temperature, under Bias BBABS operation STB operation	-40°C < T _A < +85°C -40°C < T _A < +70°C
Ambient relative humidity (non condensing)	5 to 95%
VBAT ₁ , VBAT ₂ voltage with respect to GND	-115 V _{DC} to +0.5 V _{DC}
AVDD, DVDD, VDDHPI voltages with respect to GND	-0.4 V _{DC} to +4.0 V _{DC}
AVDD voltage with respect to DVDD	-0.4 V _{DC} to +0.4 V _{DC}
I/O ₁ , I/O ₂ current sink to GND ⁽¹⁾	70 mA
TIPD _i or RINGD _i voltage with respect to GND (continuous)	VBAT _i - 1 V _{DC} to + 1.0 V _{DC}
TIPD _i or RINGD _i voltage with respect to GND (10 ms, F = 0.1Hz)	VBAT _i - 5 V _{DC} to + 5.0 V _{DC}
TIPD _i or RINGD _i voltage with respect to GND (1 μs, F = 0.1Hz)	VBAT _i - 10 V _{DC} to + 10 V _{DC}
TIPD _i or RINGD _i voltage with respect to GND (250 ns, F = 0.1Hz)	VBAT _i - 15 V _{DC} to + 15 V _{DC}
TIPD _i or RINGD _i current (continuous)	±150 mA
TIPD _i or RINGD _i current (1 μs)	±400 mA
Latch up immunity (any pin)	±100 mA
Maximum device power dissipation, continuous ⁽²⁾ P _D	2.1 W
Junction to ambient thermal resistance ⁽²⁾ θ _{JA}	26°C/W
Junction to board thermal resistance ⁽²⁾ θ _{JB}	7°C/W
Junction to case bottom (exposed pad) thermal resistance ⁽²⁾ θ _{JC (BOTTOM)}	3.6°C/W
Junction-to-top characterization parameter ⁽²⁾ ψ _{JT}	0.8°C/W
Reflow temperature, 10 sec., MSL3, per JEDEC J-STD-020	260°C
ESD immunity (Human Body Model)	JESD22 Class 1C compliant

Notes:

1. When configured as outputs (for LED or relay drive control)
2. See ["Thermal Performance"](#)

4.2 Thermal Performance

The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout. Specified performance requires that the exposed thermal pad be soldered to an equally sized exposed copper surface, which, in turn, conducts heat through multiple vias to a copper plane. Thermal performance depends on the number of PCB layers and the size of the copper area.

The thermal specifications in [“Absolute Maximum Ratings”](#) assume that the device is mounted on a highly effective thermal conductivity test board (4 layers, 2s2p) per *JEDEC JESD51-7* and *JESD51-5*, and featuring the recommended 10x10 array of thermal vias shown in [Figure 55 on page 84](#). The ZL88801 can be mounted on a 2 layer board and operate satisfactorily to the target temperature range as specified in [“Recommended Operating Conditions”](#).

4.3 Operating Ranges

Microsemi guarantees the performance of this device over the specified temperature range by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with the *Telcordia GR-357-CORE Generic Requirements for Assuring the Reliability of Components Used in Telecommunications Equipment*.

4.3.1 Recommended Operating Conditions

Ambient temperature BBABS operation STB operation	-40°C < T _A < +85°C 0°C < T _A < +45°C
Ambient relative humidity	15% to 85%
GND	0 V _{DC}
AVDD with respect to GND	+3.3 V _{DC} ± 5%
DVDD with respect to AVDD	±50 mV _{DC}
VDDHPI with respect to GND	+1.71 V _{DC} to DVDD
VDDSW with respect to GND	+3.3 V _{DC} ± 5%
BBABS operation VBAT ₃ with respect to GND VBAT _{1/2} with respect to GND	VBAT ₃ = -(VSW + (2 * VBAT ₁) - 2V) -40 V _{DC} to -25 V _{DC}
STB operation VBAT _i with respect to GND, in Disconnect or Shutdown states VBAT _i with respect to GND, in other states	-105 V _{DC} to +0.4 V _{DC} -105 V _{DC} to -12 V _{DC}
Digital pins, except I/O _{1i} , I/O _{2i}	GND to VDDHPI
I/O _{1i} , I/O _{2i}	GND to DVDD
Analog pins	GND - 0.3 V _{DC} to AVDD + 0.3 V _{DC}

5.0 Electrical Characteristics

5.1 Test Conditions

Unless otherwise noted, test conditions are:

- Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltages. Minimum and maximum values are over the temperature and supply voltage ranges shown in ["Recommended Operating Conditions" on page 29](#), except where noted
- Default (unity) gain in X, R, DRL, AX and AR blocks; default coefficients in DISN, Z and B filters
- Battery voltage for BBABS operation:
 - Active and Idle states: $V_{BAT3} = -60\text{ V}$ and $V_{BAT1/2} = -25\text{ V}$
 - Ringing state: $V_{BAT3} = -80\text{ V}$ and $V_{BAT1/2} = -35\text{ V}$
- DC feed programmed and calibrated to:
 - BBABS operation: $ILA = 25\text{ mA}$, $VOC = 48.0\text{ V}$, $b_{sov} = 2.92\text{ V}$, and $b_{shv} = 5\text{ V}$
 - STB operation: $ILA = 25\text{ mA}$, $VOC = 48.0\text{ V}$, and $VAS = 8.76\text{ V}$
- AC and DC load resistance $R_L = 600\ \Omega$
- Fuse resistors for device tests are $R_F = 14\ \Omega$
- $0\text{ dBm}_0 = 0\text{ dBm}$ ($600\ \Omega$) = 0.775 V_{RMS} . Digital gains GX0 and GR0 to achieve 0 dB relative levels are $GX0 = +6.797\text{ dB}$ (7A20h) A-law or linear and $GX0 = +6.737\text{ dB}$ (2A20h) μ -law to set A/D transmit gain to 0dB $GR0 = -1.793\text{ dB}$ (6AA0h) A-law or linear and $GR0 = -1.720\text{ dB}$ (3AA0h) μ -law to set D/A receive gain to 0dB
- BBABS ringing tests use the following conditions:
 - C1 programmed ringing 70.7 V_{PK} (50 V_{RMS}), 0 V_{DC} offset and 3 REN ($2333\ \Omega + 24\text{-}\mu\text{F}$) load
 - C2 programmed ringing 70.7 V_{PK} (50 V_{RMS}), 0 V_{DC} offset and 5 REN ($1386\ \Omega + 40\text{-}\mu\text{F}$) load
- STB ringing tests use the following conditions:
 - C3 programmed ringing 85 V_{PK} (60 V_{RMS}), 0 V_{DC} offset and 1 REN ($7000\ \Omega + 8\text{-}\mu\text{F}$) load
 - C4 programmed ringing 85 V_{PK} (60 V_{RMS}), 0 V_{DC} offset and 3 REN ($2333\ \Omega + 24\text{-}\mu\text{F}$) load

5.2 Supply Currents and Power Dissipation

5.2.1 BBABS Operation

External Switcher circuit as shown in [Figure 40 on page 59](#) with input voltage $V_{SW} = 12\text{ V}_{DC}$.

Operational State	Condition	$I_{DD}\text{ mA}$	$I_{VSW}\text{ mA}$	$I_{VBAT3}\text{ mA}$	$I_{VBAT1/2}\text{ mA}$	Device Power mW	System Power mW	Power	Notes
		(Note 2)	(Note 3)	Typ	Typ	Typ	Typ		
Shutdown	Ch1/Ch2	1.5	0	0	0	5	5	Per Channel	
Disconnect	Ch1/Ch2	5.5	0.7	0.1	0	25	26		
Low Power Idle Mode (LPIM)	Ch1/Ch2	9.5	1.6	0.3	0	47	51		
Idle	On-Hook	14.5	5.3	0.8	0	99	112		
Active (normal or reverse polarity)	OHT	23	11.9	1.9	0	190	219		
	Off-Hook, $300\ \Omega$	24	73.3	0.9	26	520	959		
LPIM/Ringing	Ch1 LPIM, Ch2 Ringing C1	33.5	275	31.3	0	1140	3406	Both Channels	1.
	Ch1 LPIM, Ch2 Ringing C2	33.5	184	21	0	839	2319		
Active/Ringing	Ch1 Off-Hook, Ch2 Ringing C1	48	360	32	26	1793	4483	Both Channels	1.
	Ch1 Off-Hook, Ch2 Ringing C2	48	275	21.6	26	1523	3463		

1. *Not Tested in Production. Parameter is guaranteed by characterization or correlation to other tests.*
2. I_{DD} supply current is the sum of I_{AVDD} and I_{DVDD} for the device divided by 2.
3. I_{VSW} is not tested in production.

5.2.2 STB Operation

External Switcher circuit as shown in [Figure 42 on page 63](#) with input voltage $V_{SW} = 12 V_{DC}$. Supply currents and power consumption are per channel of the device based on both channels in the same state. When channels are in different states, the values shown are total supply current and device power consumption divided by 2. Device or package power does not include power delivered to the load.

Operational State	Condition	I_{DD} mA (Note 2)	I_{VSW} mA (Note 3)	I_{VBAT} mA	Device Power mW	Note
		Typ	Typ	Typ	Typ	
Shutdown	Disconnect, switcher off	1.5	0	0	5	
Low Power Idle Mode (LPIM)	$V_{BAT} = -48 V$	9.5	2.5	0.2	39	
1 line Active (normal or reverse polarity), 1 line LPIM	Off-Hook, 300 Ω	16.5	95	13.6	620	1.
Active (normal or reverse polarity)	Off-Hook, 300 Ω	23	85	54	470	1.
1 line Ringing, 1 line LPIM	C3	17	66	5.5	300	1.
	C4	17	150	12.5	476	
1 line Ringing, 1 line Active (normal or reverse polarity)	C3, Off-Hook, 300 Ω	24	220	19	1260	1.
	C4, Off-Hook, 300 Ω	24	310	26	1570	

Notes:

1. *Not Tested in Production. Parameter is guaranteed by characterization or correlation to other tests.*
2. I_{DD} supply current is the sum of I_{AVDD} and I_{DVDD} for the device divided by 2.
3. I_{VSW} is not tested in production.

5.3 DC Characteristics

Symbol	Parameter Descriptions	Min	Typ	Max	Unit	Note
V_{IL}	Digital input low voltage			0.8	V	
V_{IH}	Digital input high voltage	2.0				
I_{IL}	Digital input leakage current	-7		+7	μ A	
I_{AIL}	Analog input leakage current	-1		+1		
V_{HYS}	Digital input hysteresis	0.16	0.25	0.34	V	1.
V_{OL}	Digital output low voltage			0.8	V	2.
	I/O ₁ , I/O ₂ ($I_{OL} = 50$ mA)			0.4		
	I/O ₂ , I/O ₂ ($I_{OL} = 4$ mA)			0.8		
	I/O ₂ , I/O ₂ ($I_{OL} = 8$ mA)			0.4		
	TSCA ($I_{OL} = 14$ mA)			0.4		
	Other digital outputs ($I_{OL} = 2$ mA)			0.4		
V_{OH}	Digital output high voltage					
	I/O ₂ , I/O ₂ ($I_{OH} = 4$ mA)	$V_{DVDD} - 0.4$ V				
	I/O ₂ , I/O ₂ ($I_{OH} = 8$ mA)	$V_{DVDD} - 0.8$ V				
	Other digital outputs ($I_{OH} = 400$ μ A)	2.4				
I_{OL}	Digital output leakage current (Hi-Z state) $0 < V < DVDD$	-7		+7	μ A	
V_{REF}	VREF output open circuit voltage ($I_{VREF} = \pm 100$ μ A)	1.43	1.5	1.57	V	
C_{IREF}	IREF pin maximum load capacitance			20	pF	1.
C_I	Digital input capacitance			4		
C_O	Digital output capacitance			4		
PSRR ₁	AVDD, DVDD power supply rejection ratio (1.02 kHz, 100 mV _{RMS} , either path, GX = GR = 0 dB)	32	38		dB	
PSRR ₂	VBAT _i power supply rejection ratio (1.02 kHz, 100 mV _{RMS} , either path, GX = GR = 0 dB)	40				1.

Notes:

1. This parameter is guaranteed by characterization or correlation to other tests. Not tested in production.
2. I/O₁, and I/O₂ outputs are resistive for less than a 0.8 V drop. Total DC current must not exceed absolute maximum ratings.

5.4 DC Feed and Signaling – All States Except Low Power Idle Mode

Description	Test Conditions	Min	Typ	Max	Unit	Note
ILA programmable range, Active state BBABS operation STB operation		18 18		30 25	mA	1.
I_L , Loop-current accuracy, Active state	I_L in constant-current region after ILA calibration	-10		+10	%	
I_{RINGD} , RINGD leakage, Ring Open state	VBAT = -100 V $R_L = 0$ to GND or VBAT			1000	μA	1.
I_{TIPD} , TIPD leakage, Tip Open state	VBAT = -100 V $R_L = 0$ to GND or VBAT			1000		
TIPD, RINGD leakage, Disconnect state	VBAT = -100 V $R_L = 0$ to GND or VBAT			10		
I_{RINGD} , RINGD current accuracy, Tip Open state	RINGD to ground	-10		+10	%	1.
V_{TIPD} , ground-start signaling	TIPD to -48 V = 7 kΩ, RINGD to ground = 100 Ω	-7.5	-5		V	
TDC, RDC input offset current		1.35	1.5	1.65	μA	1., 2.
Ground key accuracy	After calibration	-1 mA – 15%		+1 mA + 15%		
Switch hook accuracy	After calibration	-20		+20	%	
Open circuit voltage, $V_{TIPD} - V_{RINGD}$	VOC = 48 V, after VOC calibration	-7		+7		
V_{RINGD} , open circuit	VOC = 48 V, after VOC calibration	-56.5		-49.0	V	

Notes:

1. This parameter is guaranteed by characterization or correlation to other tests. Not tested in production.
2. Analog input pad leakage can add to this value - see specification under [“DC Characteristics” on page 32](#).

5.5 DC Feed and Signaling – Low Power Idle Mode State

Description	Test Conditions	Min	Typ	Max	Unit	Note
$V_{TIPD} - V_{RINGD}$ voltage	VBAT=-52 V, $I_{LOAD} = 3$ mA	44			V	1.
	$R_{LOAD}=3.5$ KΩ	23	28	33		
	VBAT=-52 V, $R_{LOAD} =$ open	44	48	51		
I_{TIPD} current limit	TIPD sourcing current	9	31	70	mA	1.
I_{RINGD} current limit	RINGD sinking current, $R_{LOAD} = 600$ Ω	7.1	8.0	9.3		
Off-hook current settling time	$R_{LOAD} = 200$ Ω		90	800	μs	1.
DC feed resistance	$I_{LOAD} <$ current limit		200		Ω	
	$I_{LOAD} >$ current limit		230K			

Note:

1. This parameter is guaranteed by characterization or correlation to other tests. Typical values not tested in production.

5.6 Metering

Description	Test Conditions	Min	Typ	Max	Unit	Note
Level accuracy	0.5 V _{RMS} , 12 or 16 kHz, 200 or 3000 Ω AC load	-5		+10	%	1.
Frequency accuracy	12 or 16 kHz	-0.1		+0.1	%	

Note:

1. This parameter is guaranteed by characterization or correlation to other tests. Typical values not tested in production.

5.7 Ringing

Description	Test Conditions	Min	Typ	Max	Unit	Note
Ringing Voltage Accuracy	52.5 V _{PK} into a 3 REN load	-7		+7	%	1.
Normal Polarity Ringing DC offset, V _{TIPD} - V _{RINGD}	R _L = open circuit, programmed rInging = 0 V _{PK}	-5	0	+2	V	2.,3.
Harmonic distortion	52.5 V _{PK} into a 3 REN load		3	5	%	
Ringing current limit accuracy	R _L = 600 Ω	-10		10		
Ringing source impedance			200		Ω	2.
DC ring trip accuracy	EGBIAS = 1	-15		+15	%	2.,4.
AC ring trip accuracy	EGBIAS = 0	-15		+15		
Ring trip delay	Periods of ringing	1		3	cycles	

Notes:

1. This production test is performed without calibration. After calibration, typical accuracy is within +/-4 %.
2. This parameter is guaranteed by characterization or correlation to other tests. Not tested in production.
3. After calibration.
4. If the ringing current in the loop is near the current limit more than 50% of the time, a ring trip will occur regardless of the average current.

5.8 Switching Regulator Controller

The following specifications apply to switching regulator controllers Y and Z.

Description	Test Conditions	Min	Typ	Max	Unit	Note
SWISx shutdown threshold	Referenced to GND	85	100	115	mV	1.
SWISx hysteresis			25			
SWISx input bias current		-10		10	μA	
SWISx shutdown delay	V _{SWISx} > 115 mV	12		88	ns	1., 2.
SWCMPx output current		-200		200	μA	1.
SWCMPx operating range		0.4		2.6	V	
SWVSx to SWCMPx gain		0.4		40	V/nA	
SWVSx to SWCMPx bandwidth		100			kHz	
SWVSx input offset current	R _{VSx} = 1.0 MΩ	1.3	1.5	1.7	μA	
LFC output impedance			12		kΩ	
SWxV output voltage accuracy	Calibrated -95 V fixed ringing voltage	-100		-90	V	3.

Notes:

1. This parameter is guaranteed by characterization or correlation to other tests. Not tested in production.
2. Time from SWISx exceeding threshold to SWOUTx voltage passing through DVDD/2.
3. Accuracy following battery calibration depends on the battery voltage sense accuracy (+/-4 %) plus the calibration resolution of +/- 0.625 V

5.9 Voice ADC Signal Sense Accuracy

Description	Code	Full Scale	Useful Range	Min	Typ	Max	Unit	Note
Metallic AC coupled voltage (Tip/Ring voice)	00h	-3.44 to +3.44	-3.44 to +3.44	-4%		+4%	V	1., 2.
Voice DAC analog loopback	0Ah	-2.0 to +2.0	-1.0 to +1.0	-12%		+12%		

Notes:

- All specifications assume calibration.
- The % limits are defined as the % of programmed threshold value or the % of the actual voltage or current on Tip / Ring. The offset and percentage errors are independent and combine as RMS errors.

5.10 Supervision ADC Signal Sense Accuracy

Description	Code	Full Scale	Useful Range	Min	Typ	Max	Unit	Note
Sense at SWVSY	01h	-240 to +240	-180 to 0	-0.5 V – 4 %		+0.5 V + 4 %	V	1., 2., 3., 6.
Sense at SWVSZ	02h		-180 to 0	-0.5 V – 4 %		+0.5 V + 4 %		
Sense at VS1, VS2	03h		-180 to +60	-0.5 V – 4 %		+0.5 V + 4 %		
Tip voltage to ground	04h		-225 to +225	-2.0 V – 4 %		+1.0 V + 4 %		
Ring voltage to ground	05h		-2.0 V – 4 %		+1.0 V + 4 %			
Metallic DC line voltage (Tip to Ring)	06h		-160 to +160	-0.5 V – 5 %		+0.5 V + 5 %		
Longitudinal DC line voltage (Tip to ground + Ring to ground)	0Ah		-1.0 V – 5 %		+1.0 V + 5 %			
Metallic loop current, IM (Tip to Ring) in Normal Mode	07h	-59.5 to +59.5 ⁽⁴⁾	-51 to +51 ⁽⁴⁾	-1.0 mA – 5 %		+1.0 mA + 5%	mA	1., 2., 6.
Longitudinal loop current, IL (total) in Normal Mode	08h	-59.5 to +59.5	-42 to +42	-1.0 mA – 5 %		+1.0 mA + 5%		
Ring current, IB (IM+IL)	0Eh			-2.0 mA – 5 %		+2.0 mA + 5%		
Tip current, IA (IM-IL)	0Fh			-2.0 mA – 5 %		+2.0 mA + 5%		
Metallic loop current (IM) in Low Gain Mode	08h	-297.5 to +297.5	-100 to +100	-5.0 μ A – 5 %		+5.0 μ A + 5%	μ A	
Longitudinal loop current per wire (IL) in Low Gain Mode	07h		-250 to +250	-5.0 μ A – 5 %		+5.0 μ A + 5%		
Tip voltage to Longitudinal current ratio				-6.5		+6.5	%	1., 5., 6., 7.
Ring voltage to Longitudinal current ratio	N/A	N/A	N/A	-6.5		+6.5		
Metallic voltage to Metallic current ratio				-6.5		+6.5		
Temperature sense	0Dh	-50 to +150	-50 to +150	-15		+15	$^{\circ}$ C	1., 6.

Notes:

- All specifications assume calibration.
- The % limits are defined as the % of programmed threshold value or the % of the actual voltage or current. The offset and percentage errors are independent and combine as RMS errors.
- This is measured in production by calibrating offset voltage and applying -26 V for voltage to ground and 20 V Metallic. Accurately measuring smaller voltage requires care in offset calibration.
- The Metallic loop current scale and range during ringing are -119 mA to +119 mA.
- These are ratios of voltage to current measurements in Low Gain state performed during production testing.
- Full scale is defined as a digital output code of ± 32768 .

7. Not tested in production.

5.11 Transmission Characteristics – Narrowband Codec Mode

Description	Test Conditions	Min	Typ	Max	Unit	Note
TAC - RAC overload level	Active state, GX = AX = 0 dB	3.4			V _{PK}	1., 2.
Transmit level, A/D	0 dBm, GX = GX0, 1014 Hz		0		dBm0	
Receive level, D/A	0 dBm0, GR = GR0, 1014 Hz		0		dBm	
Gain accuracy, D/A or A/D	0 dBm0, 1014 Hz, off-hook	-0.35		+0.35	dB	
Gain accuracy, D/A or A/D	0 dBm0, 1014 Hz, on-hook	-0.5		+0.5		
Idle channel noise V _{TIPD} - V _{RINGD} DXA, digital out	DRA, digital input = 0, A-law, 0 dBr DRA, digital input = 0, μ-law, 0 dBr V _{TIPD} - V _{RINGD} = 0 V _{AC} , A-law, 0 dBr V _{TIPD} - V _{RINGD} = 0 V _{AC} , μ-law, 0 dBr			-74 16 -65 19	dBm0p dBrnC0 dBm0p dBrnC0	5.
Two-wire return loss	200 to 3400 Hz	26	30		dB	
Longitudinal to metallic balance TIPD - RINGD or DXA	200 to 3400 Hz	50				7.
DRA to longitudinal signal generation	300 to 3400 Hz	42				7.
Longitudinal current capability, per wire TIPD or RINGD	Active state	8.5			mA _{RMS}	1.
Longitudinal impedance at TIPD or RINGD	0 to 100 Hz, LI = 0		100		Ω/pin	
Crosstalk between channels TX or RX to TX RX or TX to RX	0 dBm0, 1014Hz, Average 0 dBm0, 1014Hz, Average			-76 -78	dBm0	
Attenuation distortion	300 to 3000 Hz	-0.125		+0.125	dB	1., 3.
Single frequency distortion	A-law or μ-law, off-hook			-46		4.
Second harmonic distortion, D/A	GR = 0 dB, linear mode, off-hook			-55		
End-to-end absolute group delay	B = Z = 0; X = R = 1, C/L = 0			678	μs	1., 6.
PESQ-LQ voice quality score	Linear, A-law, or μ-law		4.30			1.

Notes:

1. This parameter is guaranteed by characterization or correlation to other tests. Not tested in production.
2. Overload level is defined when THD = 1%.
3. See [Figure 19](#) and [Figure 20 on page 37](#).
4. 0 dBm0 input signal, 300 to 3400 Hz measurement at any other frequency, 300 Hz to 3400 Hz.
5. No single frequency component in the range above 3800 Hz may exceed a level of -55 dBm0.
6. The End-to-End Group Delay is the absolute group delay of the echo path with the B filter turned off.
7. This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.

5.12 Attenuation Distortion – Narrowband Codec Mode

The signal attenuation in either path is nominally independent of the frequency. The deviations from nominal attenuation will stay within the limits shown in [Figure 19](#) and [Figure 20](#). The reference frequency is 1014 Hz and the signal level is -10 dBm0.

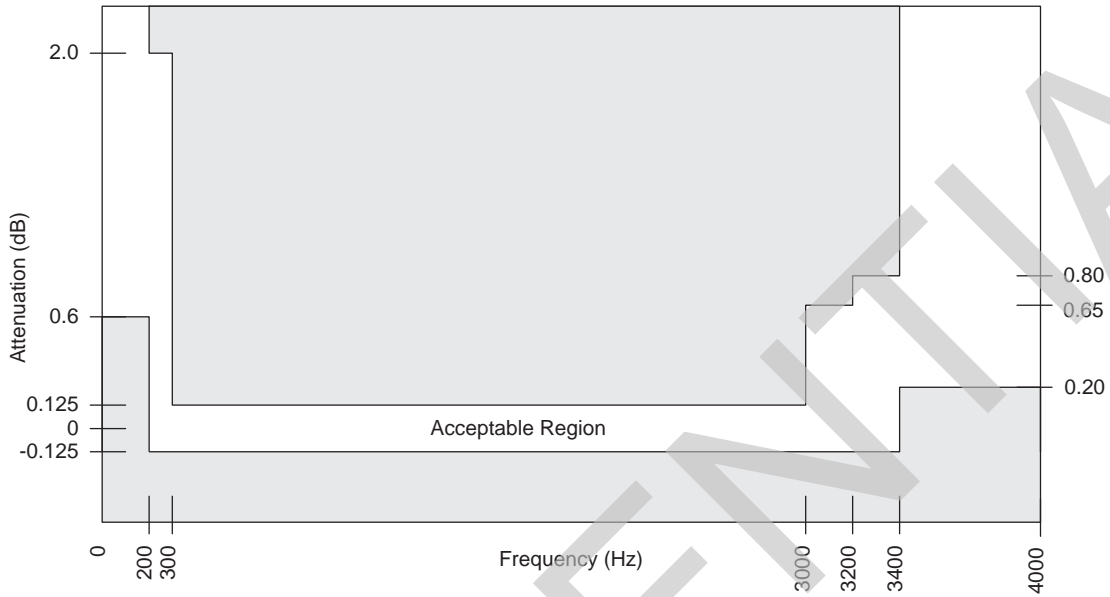


Figure 19 - Transmit (A to D) Path Attenuation vs. Frequency

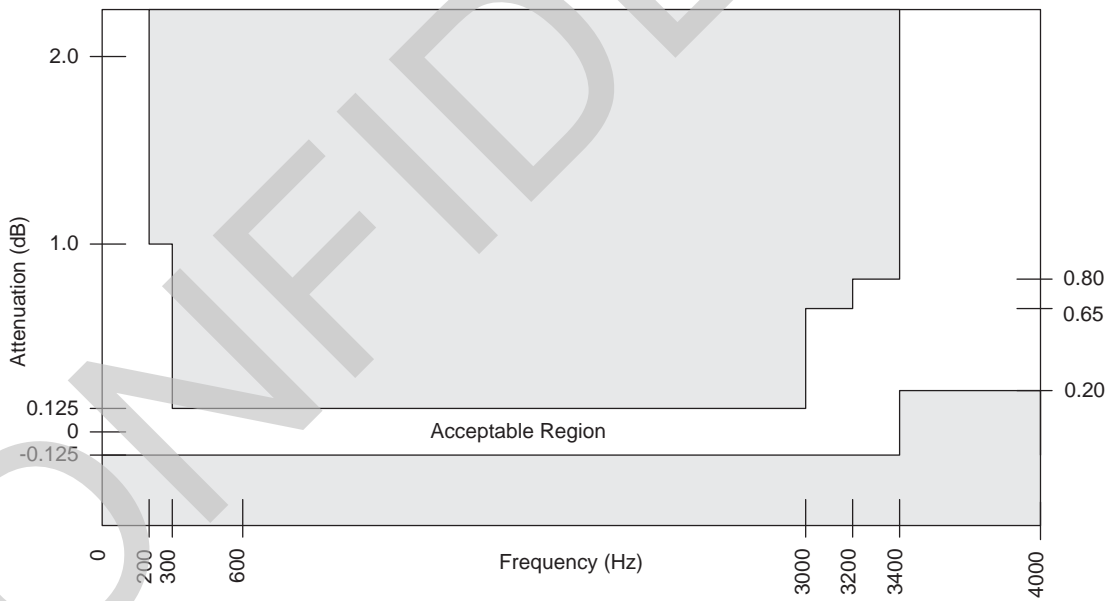


Figure 20 - Receive (D to A) Path Attenuation vs. Frequency

5.13 Discrimination Against Out-of-Band Input Signals – Narrowband Codec Mode

When an out-of-band sine wave signal of frequency f , and level A is applied to the analog input, there may be frequency components below 4 kHz at the digital output which are caused by the out-of-band signal. These components are at least the specified dB level below the level of a signal at the same output originating from a 1014-Hz sine wave signal with a level of A dBm0 also applied to the analog input. The minimum specifications are shown in [Table 7](#). The attenuation of the waveform below amplitude A , between 3400 Hz and 4600 Hz, is given by the formula:

$$\text{Attenuation} = \left[14 - 14 \sin\left(\frac{\pi(4000 - f)}{1200}\right) \right] \text{ dB}$$

Frequency of Out-of-Band Signal	Amplitude of Out-of-Band Signal	Level below A
16.6 Hz < f < 45 Hz	-25 dBm0 < $A \leq 0$ dBm0	18 dB
45 Hz < f < 65 Hz	-25 dBm0 < $A \leq 0$ dBm0	25 dB
65 Hz < f < 100 Hz	-25 dBm0 < $A \leq 0$ dBm0	10 dB
3400 Hz < f < 4600 Hz	-25 dBm0 < $A \leq 0$ dBm0	see Figure 21
4600 Hz < f < 100 kHz	-25 dBm0 < $A \leq 0$ dBm0	32 dB

Table 7 - Out of Band Discrimination, Narrowband Codec Mode

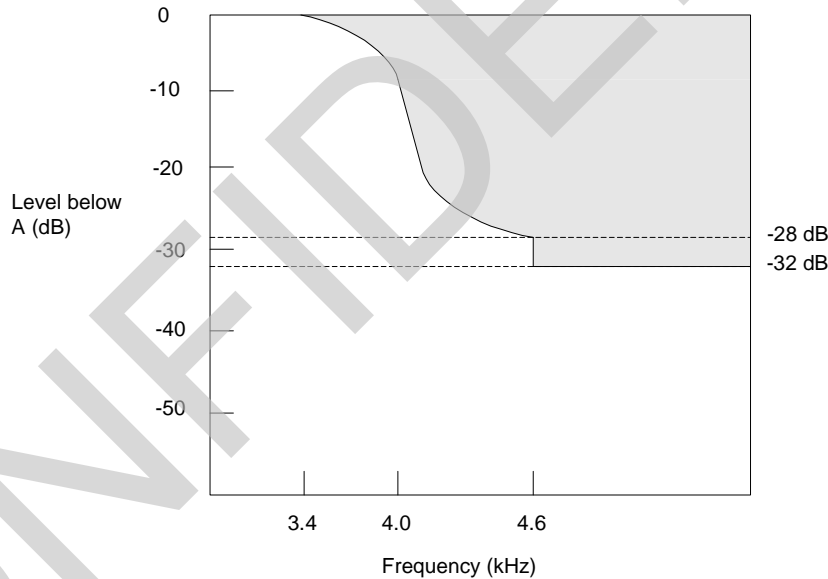


Figure 21 - Discrimination Against Out-of-Band Signals

5.14 Discrimination Against 12- and 16-kHz Metering Signals – Narrowband Codec Mode

If the ZL88801 device is used in a metering application where 12- or 16-kHz tone bursts are injected onto the telephone line toward the subscriber, a portion of these tones may also appear at the transmit input. These out-of-band signals may cause frequency components to appear below 4 kHz at the digital output. For a 12-kHz or 16-kHz tone, the frequency components below 4 kHz are reduced from the input by at least 70 dB. The sum of the peak metering and signal voltages must be within the TAC – RAC pin overload level.

5.15 Spurious Out-of-Band Signals at the Analog Output – Narrowband Codec Mode

With PCM idle code being applied to the digital input and either a quiet 600 Ω termination or an open being applied to Tip and Ring, any single frequency tone between 0 and 16kHz measured at the analog output shall be less than -50 dBm0. With PCM code words representing a sine wave signal in the range of 300 Hz to 3400 Hz at a level of 0 dBm0 applied to the digital input, the level of the spurious Out-of-Band signals at the analog output is less than the limits shown below.

Frequency	Level
4.6 kHz to 40 kHz	-32 dBm0
40 kHz to 240 kHz	-46 dBm0
240 kHz to 1 MHz	-36 dBm0

With code words representing any sine wave signal in the range 3.4 kHz to 4.0 kHz at a level of 0 dBm0 applied to the digital input, the level of the signals at the analog output are below the limits in [Figure 22](#). The amplitude of the spurious out-of-band signals between 3400 Hz and 4600 Hz is given by the formula:

$$\text{Level} = \left[-14 - 14 \sin\left(\frac{\pi(f - 4000)}{1200}\right) \right] \text{ dBm0}$$

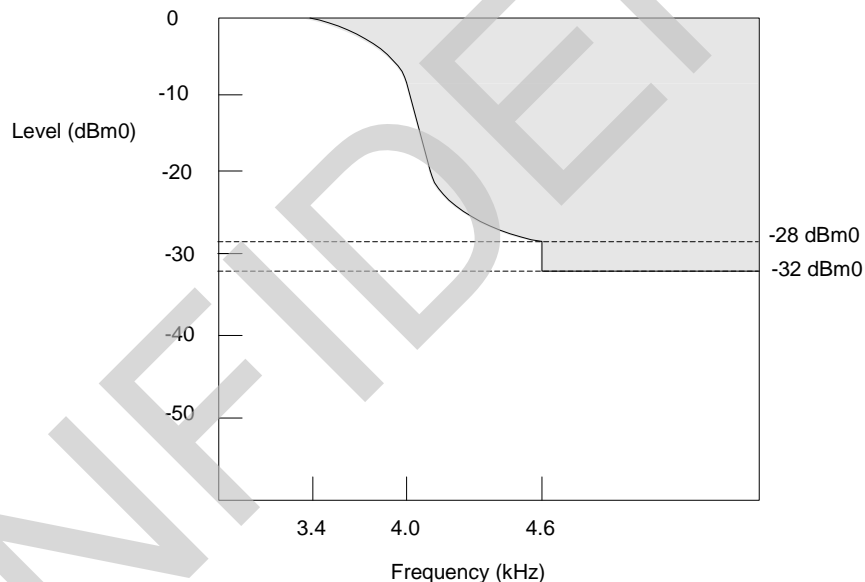


Figure 22 - Spurious Out-of-Band Signals

5.16 Overload Compression – Narrowband Codec Mode

[Figure 23 on page 40](#) shows the acceptable region of operation for input signal levels above the reference input power (0 dBm0). The conditions for this figure are:

1. $+1.2 \text{ dB} < GX \leq +12 \text{ dB}$
2. $-12 \text{ dB} \leq GR < -1.2 \text{ dB}$
3. Digital voice output of one VoicePort channel connected to digital voice input of a second VoicePort channel.
4. Measurement analog-to-analog

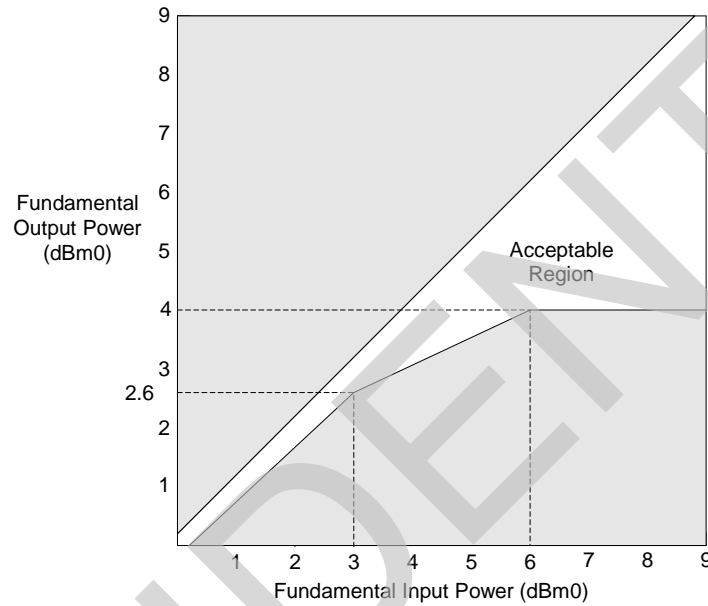


Figure 23 - Analog-to-Analog Overload Compression

5.17 Gain Linearity – Narrowband Codec Mode

The gain deviation relative to the gain at -10 dBm0 is within the limits shown in [Figure 24](#) (A-law) and [Figure 25](#) (μ -law) for either transmission path when the input is a sine wave signal of 1014 Hz.

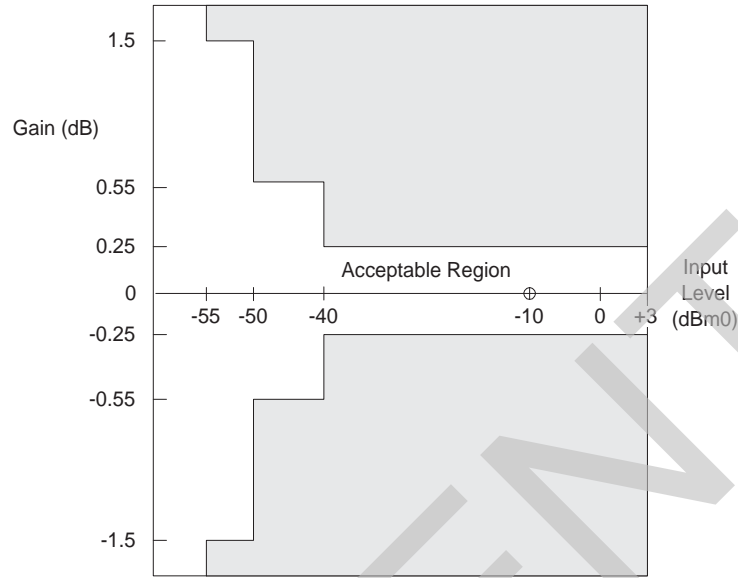


Figure 24 - A-law Gain Linearity with Tone Input (Both Paths)

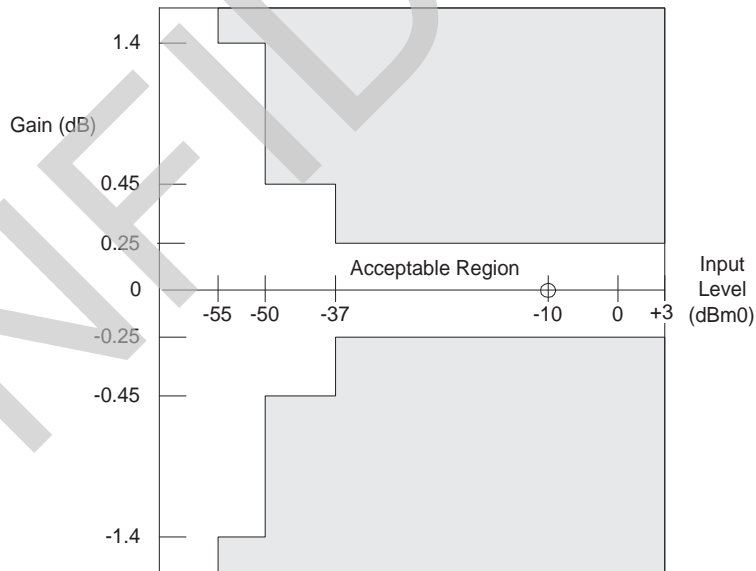


Figure 25 - μ -law Gain Linearity with Tone Input (Both Paths)

5.18 Total Distortion Including Quantizing Distortion – Narrowband Codec Mode

The signal to total distortion ratio will exceed the limits shown in [Figure 26](#) for either path when the input signal is a sine wave with a frequency of 1014 Hz, using psophometric weighting for A-law and C-message weighting for μ -law.

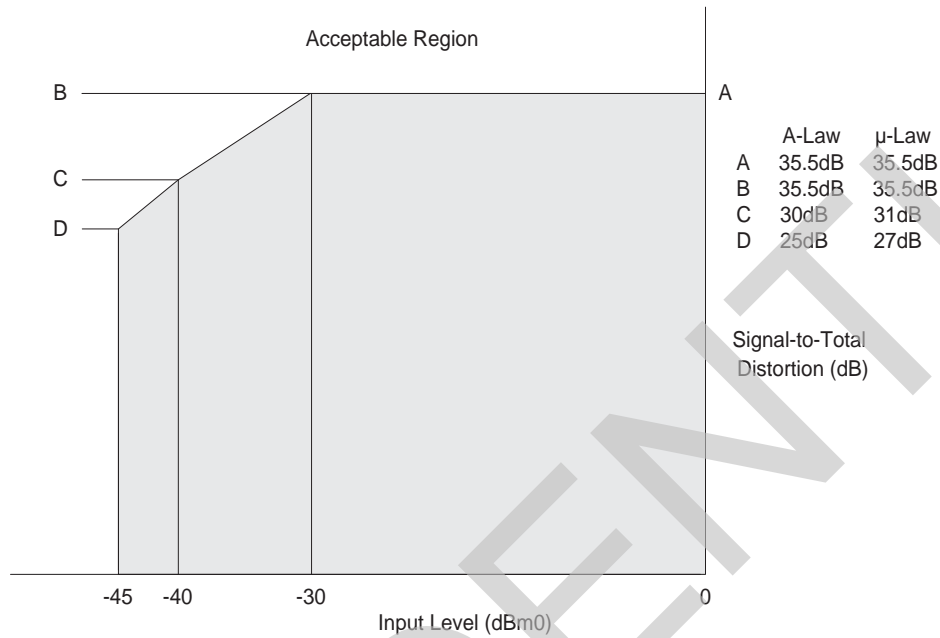


Figure 26 - Total Distortion with Tone Input (Both Paths)

5.19 Group Delay Distortion – Narrowband Codec Mode

For either transmission path, the group delay distortion is within the limits shown in [Figure 27](#). The minimum value of the group delay is taken as the reference. The signal level should be 0 dBm0.

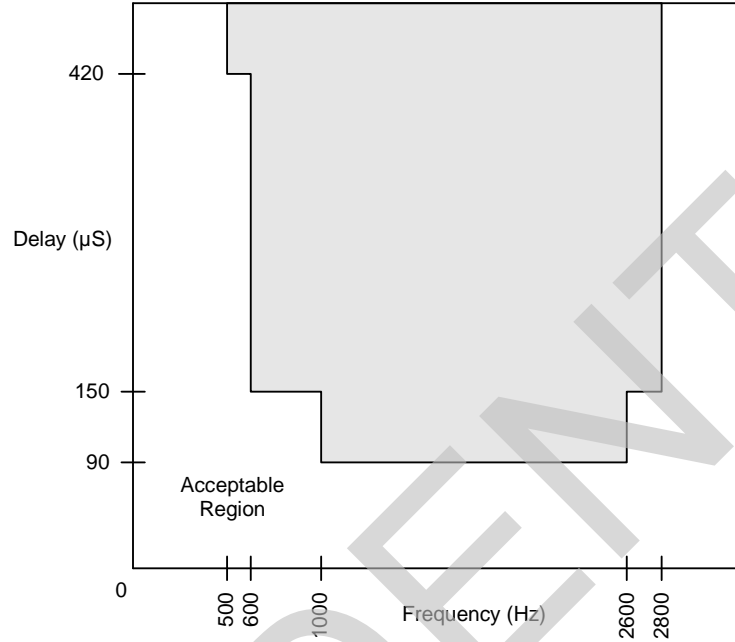


Figure 27 - Group Delay Distortion

5.20 Transmission Characteristics – Wideband Codec Mode

Description	Test Conditions	Min	Typ	Max	Unit	Note
TAC - RAC overload level	Active state GX = AX = 0 dB	3.4			V _{PK}	1., 2.
Transmit level, A/D	0 dBm, GX = GX0, 1014 Hz		0		dBm0	
Receive level, D/A	0 dBm0, GR = GR0, 1014 Hz		0		dBm	
Gain accuracy, D/A or A/D	0 dBm0, 1014 Hz, Off-hook	-0.5		+0.5	dB	
Gain accuracy, D/A or A/D	0 dBm0, 1014 Hz, On-hook	-0.5		+0.5		1.
Attenuation distortion	100 Hz to 6.0 kHz	-0.25		+0.25		3.
Single frequency distortion	0 dBm0, Linear Mode, 50 Hz to 7.0 kHz, off-hook			-50		4.
Signal to noise + distortion	0 dBm0, Linear Mode, 50 Hz to 7.0 kHz	50				4.
Second harmonic distortion, D/A	GR = 0 dB, off-hook			-55		
Idle channel noise, V _{TIPD} - V _{RINGD} DXA, digital out	DRA, digital input = 0, linear, 0 dB V _{TIPD} - V _{RINGD} = 0 V _{AC} , linear, 0 dB			-67 -67	dBm0p dBm0p	1., 5.
End-to-end absolute group delay	B = Z = 0; X = R = 1, C/L = 0			340	μs	1., 6.
Two-wire return loss	50 to 7000 Hz	20	26		dB	1.
Longitudinal to metallic balance TIPD - RINGD or DXA	50 to 7000 Hz	48			dB	7.
DRA to longitudinal signal generation	300 to 7000 Hz	40				1.
Longitudinal current capability, per wire TIPD or RINGD	Active state	8.5			mA _{RMS}	1.
Longitudinal impedance at TIPD or RINGD	0 to 100 Hz, LI = 0		100		Ω/pin	1.
PESQ-LQ voice quality score	Linear		4.30			1.

Notes:

1. This parameter is guaranteed by characterization or correlation to other tests. Not tested in production.
2. Overload level is defined when THD = 1%.
3. See [Figure 28. "Transmit \(A to D\) Path Attenuation vs. Frequency - \(with High-Pass Filter Enabled\)" on page 45](#) and [Figure 29. "Receive \(D to A\) Path Attenuation vs. Frequency" on page 45](#).
4. 0 dBm0 input signal, 50 to 7000 Hz measurement at any other frequency, 50 to 7000 Hz.
5. No single frequency component in the range above 7600 Hz may exceed a level of -55 dBm0.
6. The End-to-End Group Delay is the absolute group delay of the echo path with the B filter turned off.
7. This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.

5.21 Attenuation Distortion – Wideband Codec Mode

The signal attenuation in either path is nominally independent of the frequency. The deviations from nominal attenuation will stay within the limits shown in [Figure 28](#) and [Figure 29](#). The reference frequency is 1014 Hz and the signal level is -10 dBm0.

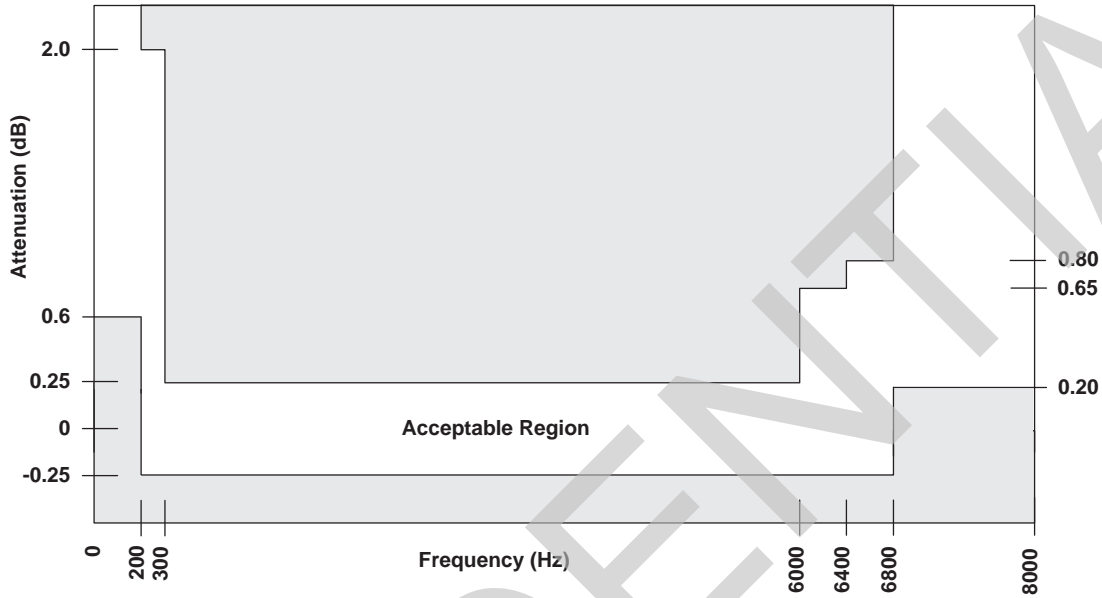


Figure 28 - Transmit (A to D) Path Attenuation vs. Frequency - (with High-Pass Filter Enabled)

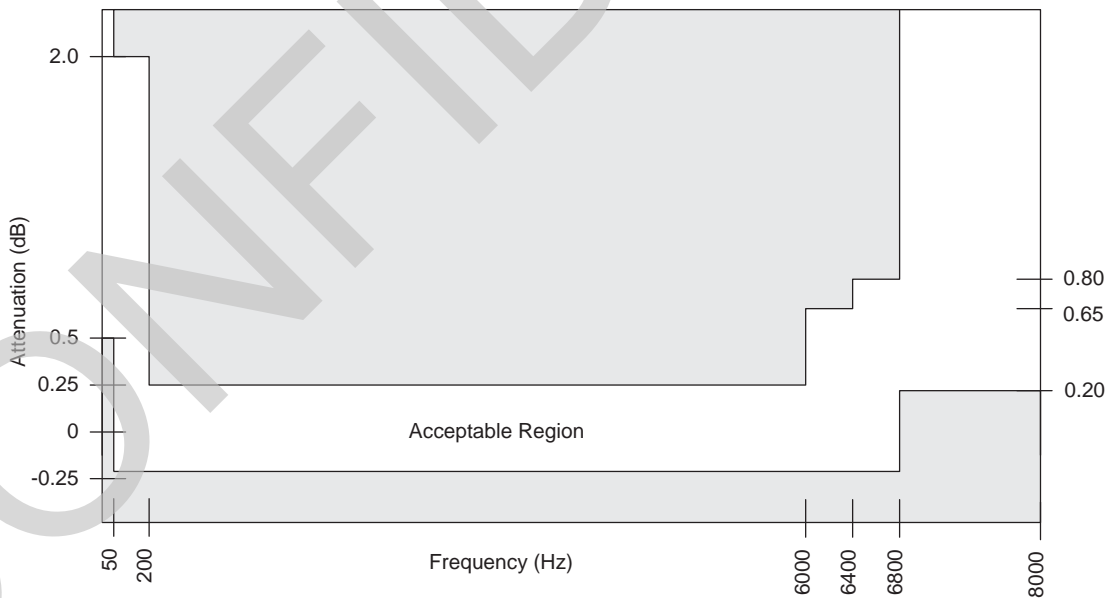


Figure 29 - Receive (D to A) Path Attenuation vs. Frequency

5.22 Group Delay Distortion – Wideband Codec Mode

For either transmission path, the group delay distortion is within the limits shown in [Figure 30](#). The minimum value of the group delay is taken as the reference. The signal level should be 0 dBm0.

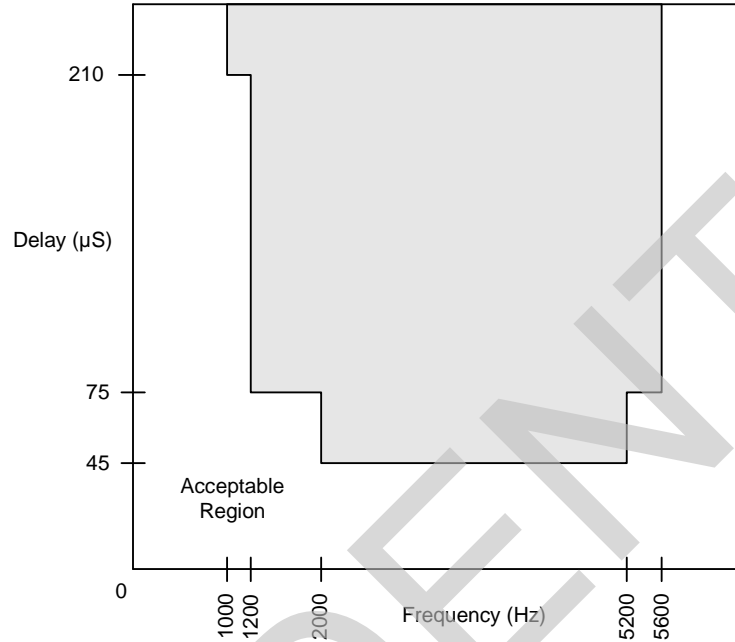


Figure 30 - Group Delay Distortion

6.0 Switching Characteristics and Waveforms

The following are the switching characteristics over operating range, unless otherwise noted. Minimum and maximum values are valid for all digital outputs with a 115 pF load.

6.1 PCM and SPI Mode

The PCM and SPI mode is used to communicate audio and control information to the host processor. It is enabled when the $\overline{\text{ZSI}}$ pin is tied to DVDD. Unless otherwise specified, the SPI timing values are valid for $V_{\text{DDHPI}} = 1.8 V_{\text{DC}}$, $2.5 V_{\text{DC}}$, or $3.3 V_{\text{DC}}$.

6.1.1 SPI Interface

No.	Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
1	t_{DCY}	Data clock period	122			ns	
2	t_{DCH}	Data clock high pulse width	48				
3	t_{DCL}	Data clock low pulse width	48				
4	t_{DCR}	Rise time of clock			8		
5	t_{DCF}	Fall time of clock			8		
6	t_{ICSS}	Chip select setup time, Input mode	5				
7	t_{ICSH}	Chip select hold time, Input mode	0				
8	t_{ICSL}	Chip select pulse width, Input mode		$8t_{\text{DCY}}$			
9	t_{ICSO}	Chip select off time, Input mode	0				1.
10	t_{IDS}	Input data setup time	5				
11	t_{IDH}	Input data hold time	0				
12	t_{OLH}	I/O1, I/O2 output latch valid			2500		
13	t_{OCSS}	Chip select setup time, Output mode	5				
14	t_{OCSH}	Chip select hold time, Output mode	0				
15	t_{OCSL}	Chip select pulse width, Output mode		$8t_{\text{DCY}}$			
16	t_{OCSSO}	Chip select off time, Output mode	0				1.
17	t_{ODD}	Output data turn on delay			16		2., 3.
18	t_{ODH}	Output data hold time	2				4.
19	t_{ODOF}	Output data turn off delay	0		10		
20	t_{ODC}	Output data valid			16		2.
–	t_{RST}	Reset pulse width	5			μs	

Notes:

1. VE880 Series devices required a minimum 2.5 μs chip select off-time when reading or writing over the SPI (MPI) interface. The delay is not required by devices belonging to the new ZL880 Series.
2. Values shown for $V_{\text{DDHPI}} = 3.3 \text{ V}$. Maximum t_{ODD} and t_{ODC} is 25 ns at 1.8 V and 18 ns at 2.5 V.
3. The first data bit is enabled on the falling edge of $\overline{\text{CS}}$ or the falling edge of DCLK , whichever occurs last.
4. This parameter is guaranteed by characterization or correlation to other tests. It is not tested in production.

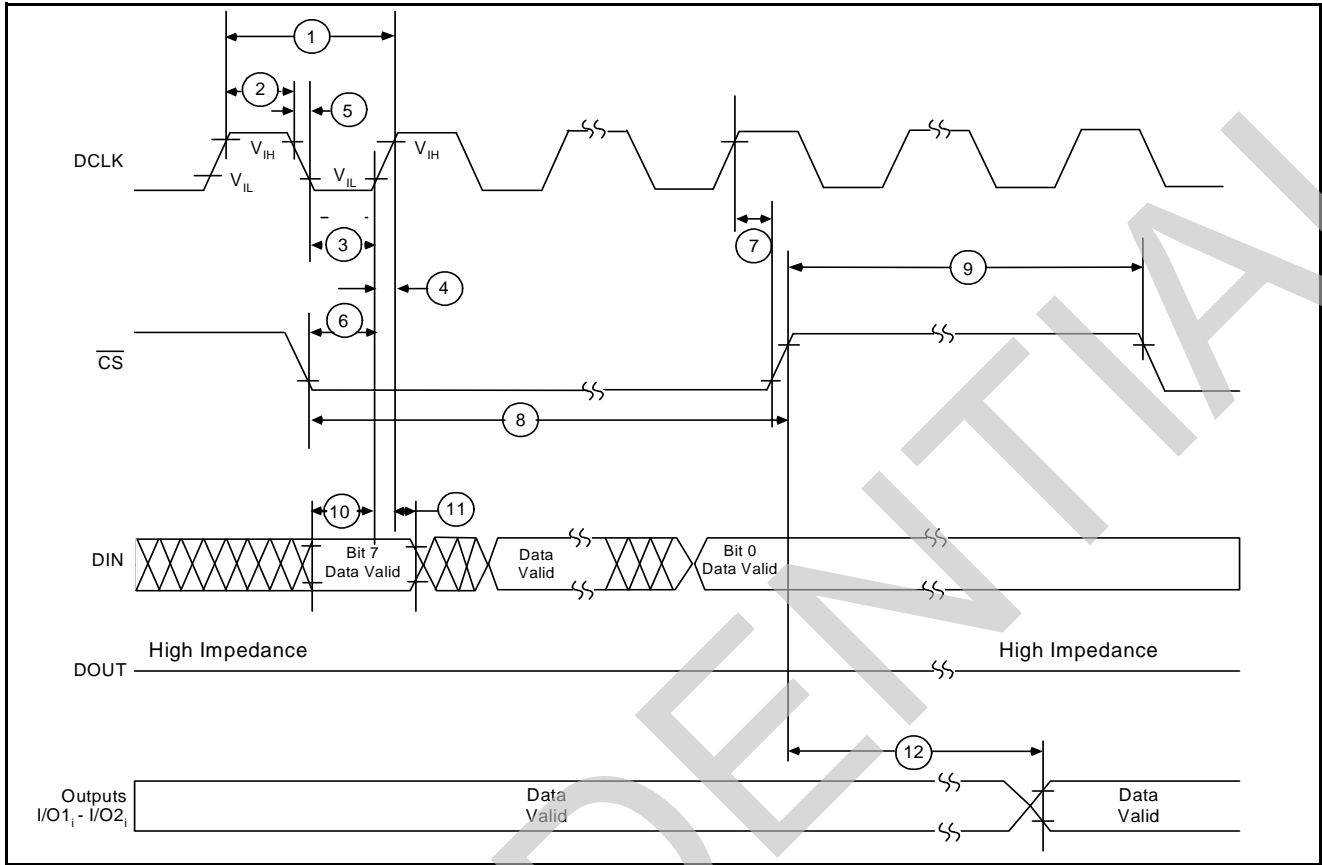


Figure 31 - SPI Interface (Input Mode)

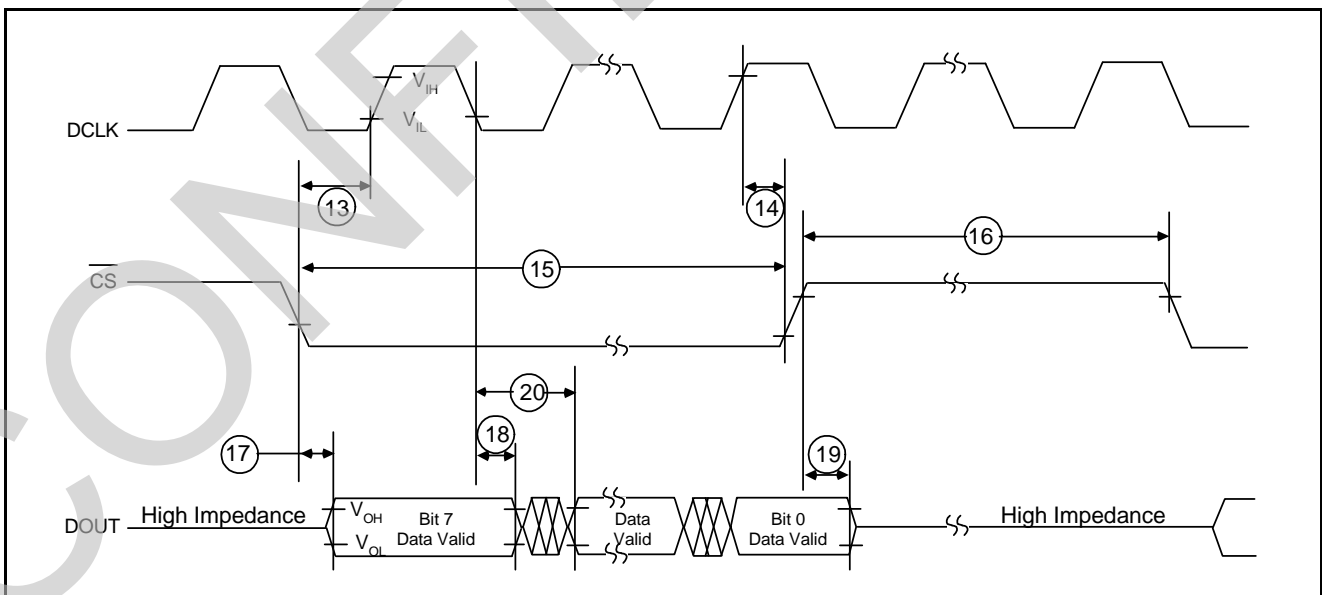


Figure 32 - SPI Interface (Output Mode)

6.1.2 PCM Interface

PCLK shall not exceed 8.192 MHz. Pull-up resistor to DVDD of 240 Ω is attached to \overline{TSCA} . Unless otherwise specified, the PCM timing values are valid for VDDHPI = 1.8 V_{DC}, 2.5 V_{DC}, or 3.3 V_{DC}. See [Figure 33 on page 50](#) through [Figure 35 on page 51](#) for the PCM interface timing diagrams.

No.	Symbol	Parameter	Min.	Typ	Max	Unit	Note
21	t _{PCY}	PCM Clock (PCLK) period	122		977	ns	1.
22	t _{PCH}	PCLK high pulse width	48				
23	t _{PCL}	PCLK low pulse width	48				
24	t _{PCR}	PCLK rise time			8		
25	t _{PCF}	PCLK fall time			8		
26	t _{FSS}	FS setup time	5		t _{PCY} -30		
27	t _{FSH}	FS hold time	0				2.
-	t _{FST}	Allowed PCLK or FS jitter time	-25		25		1.
28	t _{TSD}	Delay to \overline{TSCA} valid	2		16		3., 4.
29	t _{TSO}	Delay to \overline{TSCA} off	0				4., 5.
30	t _{DXD}	PCM data output delay			16		3.
31	t _{DXH}	PCM data output hold time	2				
32	t _{DXZ}	PCM data output delay to high Z	0		10		
33	t _{DRS}	PCM data input setup time	5				
34	t _{DRH}	PCM data input hold time	0				2.
-	t _{FSL}	FS low pulse width	1.5 t _{PCY}				6.

Notes:

1. The PCLK frequency must be an integer multiple of the Frame Sync (FS) frequency. Frame Sync is expected to be an accurate 8 kHz pulse train. The actual PCLK rate depends on the CSEL bit setting in the Chip Configuration register. The minimum frequency is 1.024 MHz and the maximum frequency is 8.192 MHz. If PCLK has jitter, care must be taken to ensure that all setup, hold, and pulse width requirements are met.
2. Values shown for VDDHPI = 3.3 V. Minimum t_{FSH} and t_{DRH} is 0.3 ns at 1.8 V and 0.2 ns at 2.5 V.
3. Values shown for VDDHPI = 3.3 V. Maximum t_{TSD} and t_{DXD} is 25 ns at 1.8 V and 18 ns at 2.5 V.
4. \overline{TSCA} is delayed from FS by a typical value of N • t_{PCY}, where N is the value stored in the time / calculus register.
5. t_{TSO} is defined as the time at which the output achieves the Open Circuit state.
6. Applies only when FS is active low.

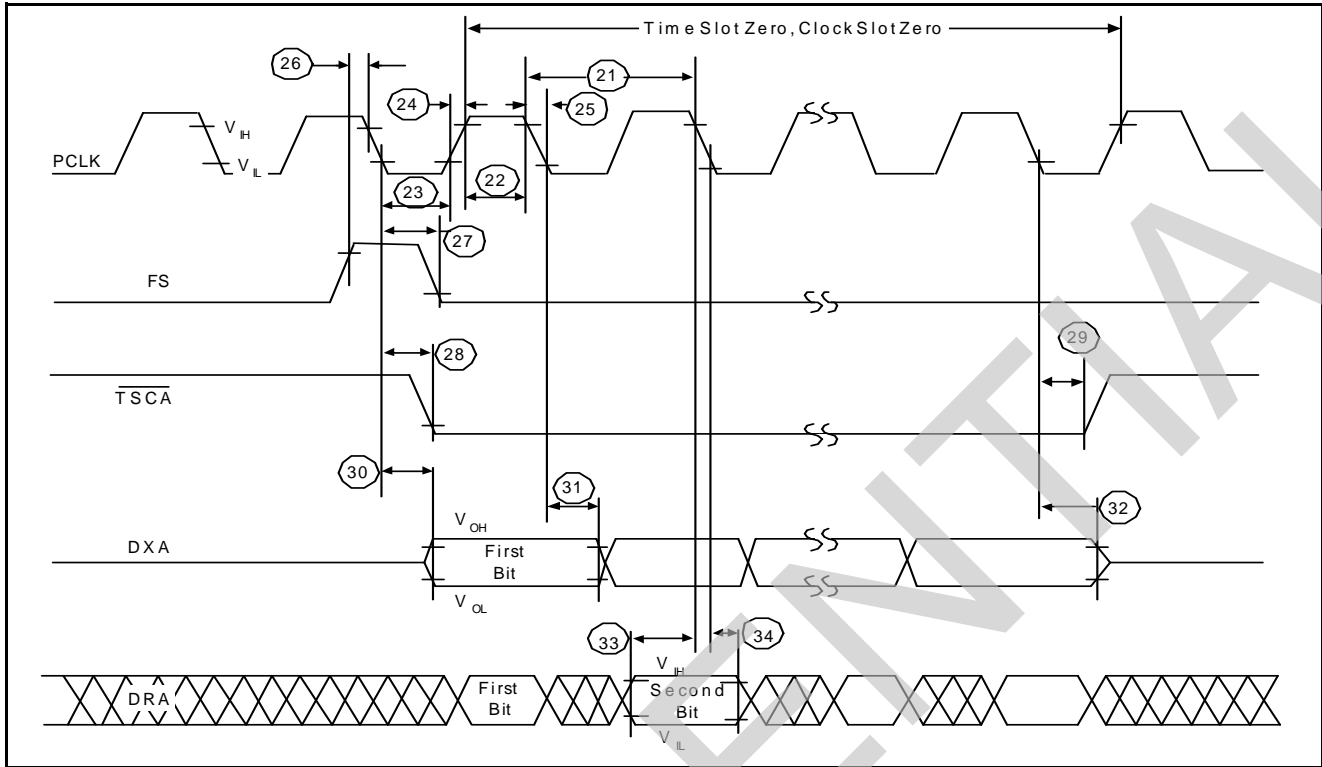


Figure 33 - PCM Highway Timing for XE = 0 (Transmit on Negative PCLK Edge)

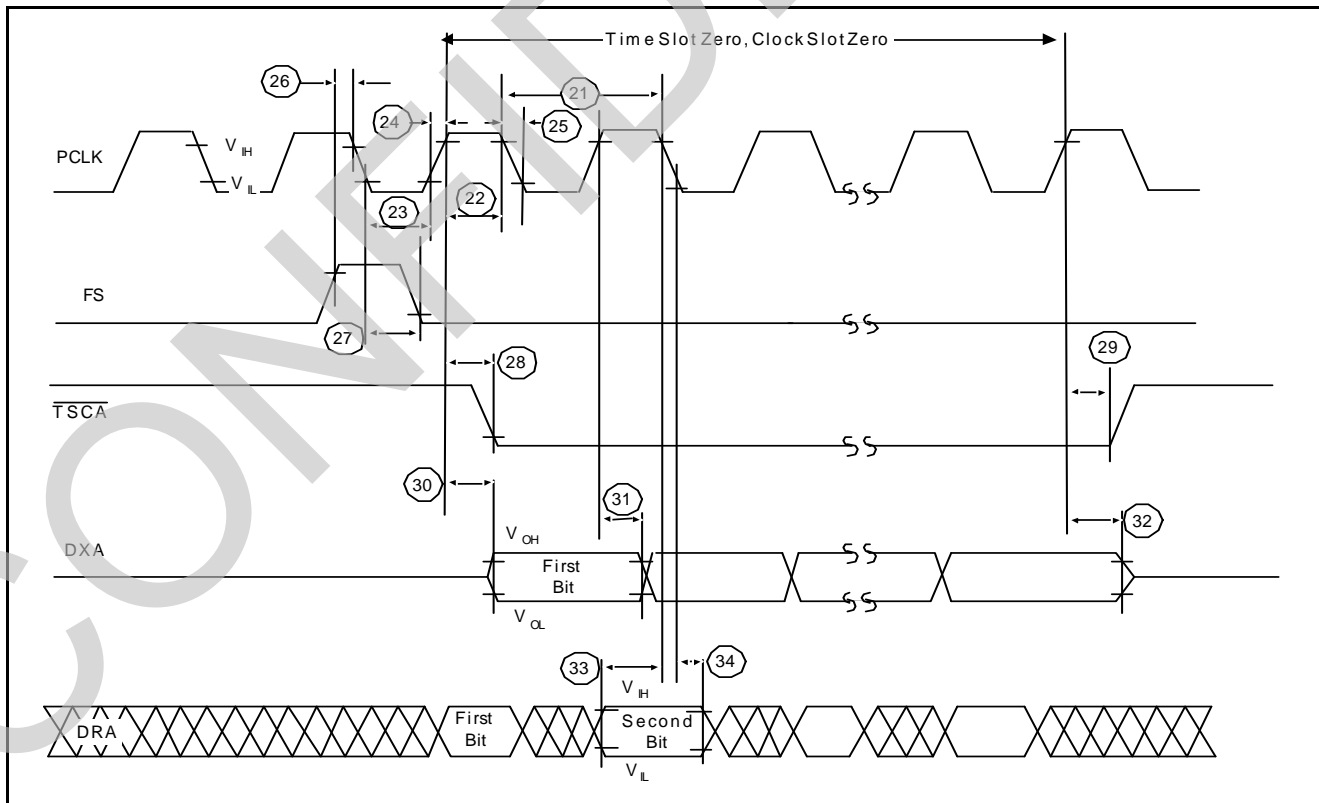


Figure 34 - PCM Highway Timing for XE = 1 (Transmit on Positive PCLK Edge)

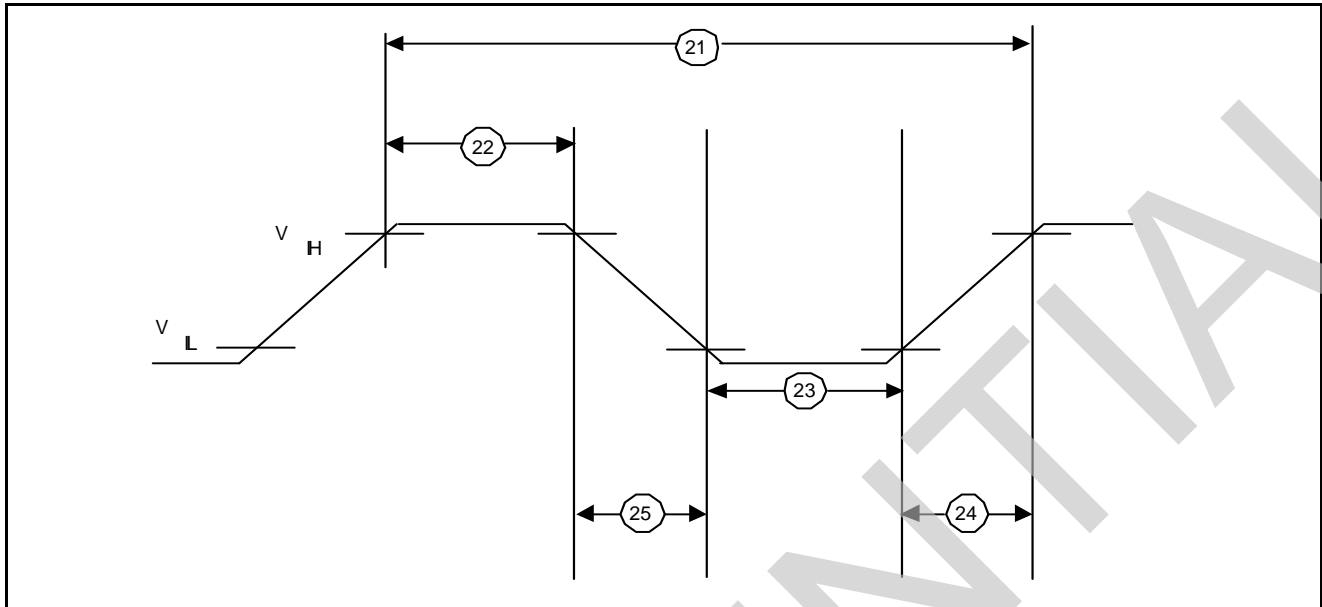


Figure 35 - PCM Clock Timing

6.2 ZSI Interface

The ZSI multiplexed serial interface is enabled when the $\overline{\text{ZSI}}$ pin is tied low. Note that ZCLK shall not exceed 8.192 MHz. All input setup and hold, and output delay and hold times are relative to either edge of ZCLK. Unless otherwise specified, the ZSI timing values are valid for $V_{DDHPI} = 1.8 V_{DC}$, $2.5 V_{DC}$, or $3.3 V_{DC}$. See [Figure 36](#) for the ZSI interface timing diagram.

No.	Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
1	t_{ZCY}	ZSI Clock (ZCLK) period	122		977	ns	1.
2	t_{ZCH}	ZCLK high pulse width	48				
3	t_{ZCL}	ZCLK low pulse width	48				
4	t_{ZCF}	ZCLK fall time			8		
5	t_{ZCR}	ZCLK rise time			8		
6	t_{ZSS}	ZSYNC setup time	5				2.
	t_{SIS}	ZMOSI slave input setup time	5				
7	t_{ZSH}	ZSYNC hold time	0				2., 3.
	t_{SIH}	ZMOSI slave input hold time	0				
8	t_{ZSOD}	ZMISO slave output delay	0		16	2., 4.	
9	t_{ZST}	Allowed ZCLK or ZSYNCFS jitter time	-25		25	2.	

Notes:

- The ZCLK frequency must be an integer multiple of the ZSYNC frequency. ZSYNC is expected to be an accurate 8-kHz pulse train. The minimum frequency is 1.024 MHz and the maximum frequency is 8.192 MHz. If ZCLK has jitter, care must be taken to ensure that all setup, hold, and pulse width requirements are met.
- ZSYNC, ZMOSI, and ZMISO contain dual data rate signals which are sampled or driven on both edges of the ZCLK clock.
- Values shown for $V_{DDHPI} = 3.3 V$. Minimum t_{ZSH} and t_{SIH} is 0.3 ns at 1.8 V and 0.2 ns at 2.5 V.
- Value shown for $V_{DDHPI} = 3.3 V$. Maximum t_{ZSOD} is 25 ns at 1.8 V and 18 ns at 2.5 V.

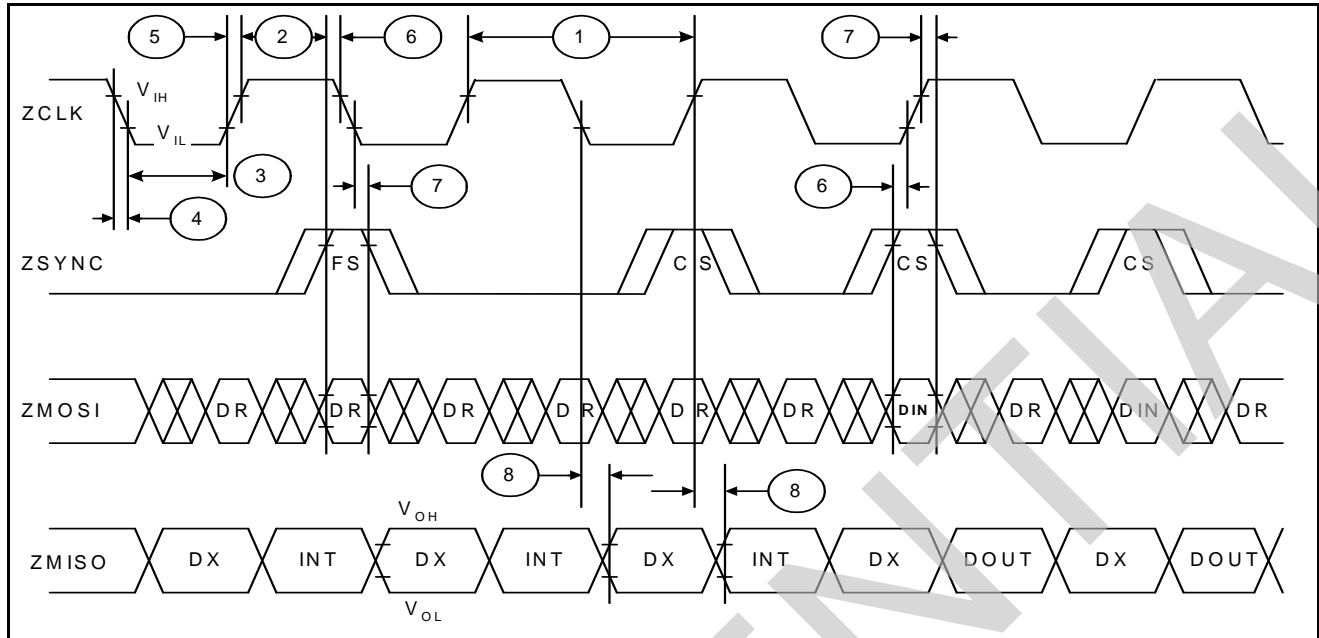


Figure 36 - ZSI Interface Timing Protocol

6.3 Switcher Output Timing

(See Figure 37 on page 53 for the SWOUTY, SWOUTZ timing diagram)

No.	Symbol	Parameter	Min	Typ	Max	Unit	Notes
1	Tfall	Output fall time		15		ns	1.
2	Trise	Output rise time		30			
3LP	TPeriod	Period for Low Power mode		41.667		μs	2., 5.
4LP	Tmax	Max on-time for Low Power mode		1.017			
3MP	TPeriod	Period for Medium Power mode		2.604			
4MP	Tmax	Max on-time for Medium Power mode		1.017			
3HP	TPeriod	Period for High Power mode		1.953		μs	4., 5.
4HP	Tmax	Max on-time for High Power mode		1.017			
-	Duty Cycle LP	Duty cycle Low Power mode	0	2.5		%	2., 5.
-	Duty Cycle MP	Duty cycle Medium Power mode	0	30.4			
-	Duty Cycle HP	Duty cycle High Power mode	0	52.0			
5	Y to Z offset	Delay from SWOUTZ to SWOUTY on		1.302		μs	4., 5.
-		SWISY leading edge blanking period		120		ns	6.

Notes:

1. Measured with a 1.5 nF load between SWOUTx and ground.
2. Register E6/E7h Write/Read Switching Regulator Control is loaded with Low Power mode 01h.
3. Register E6/E7h Write/Read Switching Regulator Control is loaded with Medium Power mode 02h.
4. Register E6/E7h Write/Read Switching Regulator Control is loaded with High Power mode 03h.
5. Timing values assume SWFS[1:0] = 00b in E4/E5h Write/Read Switching Regulator Parameters. Stated periods and on times scale inversely with frequency selected.
6. This is a programmable setting with the default value shown here. The value should be programmed to 0x01 (81 ns). This is automatically done by Profile Wizard.

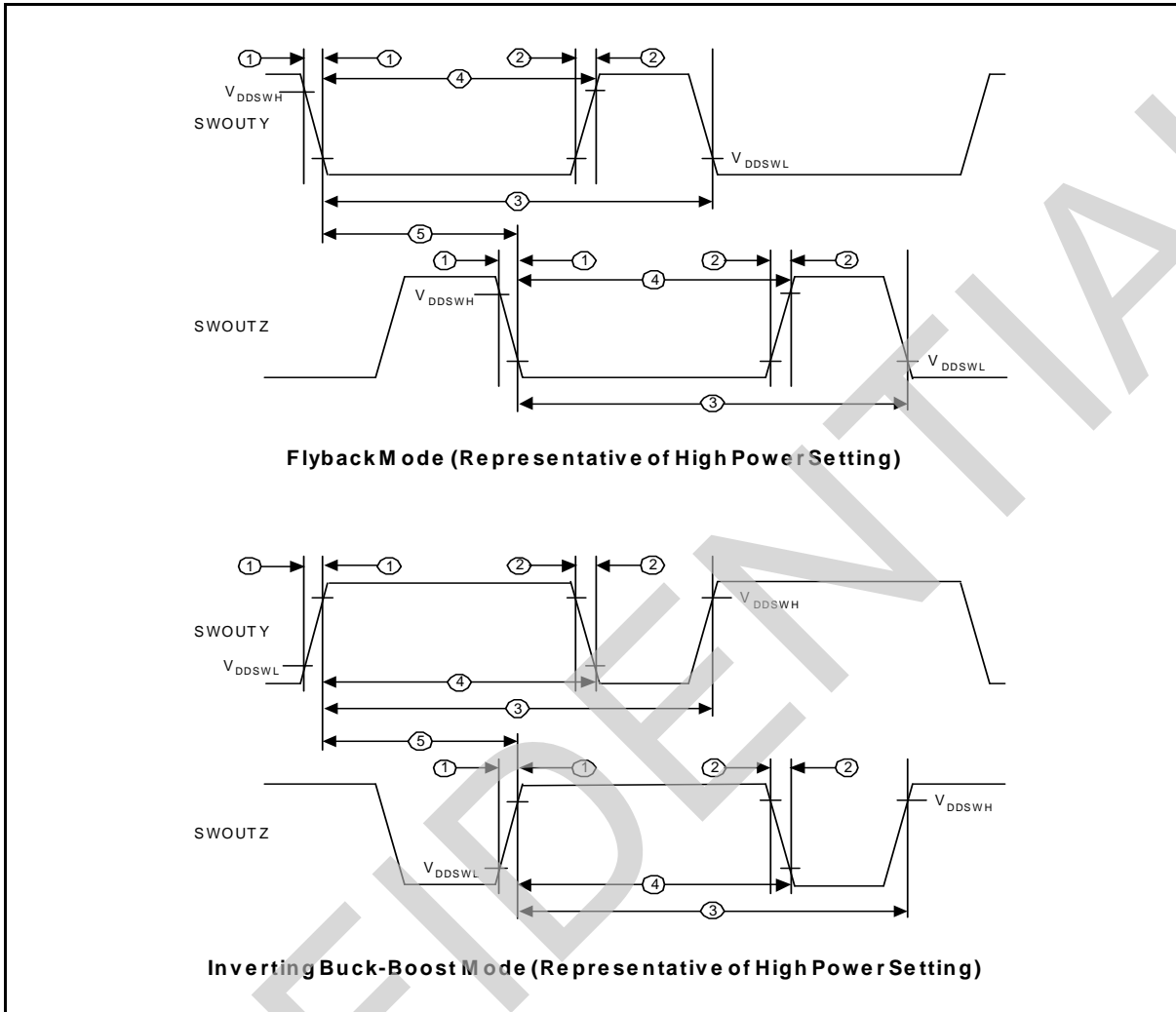


Figure 37 - Switcher Output Waveform SWOUTY, SWOUTZ

7.0 Device Pinout

The pins of the ZL88801 device are listed and described in this section. Note that there are no ground pins. All ground connections inside this device are made through the exposed pad.

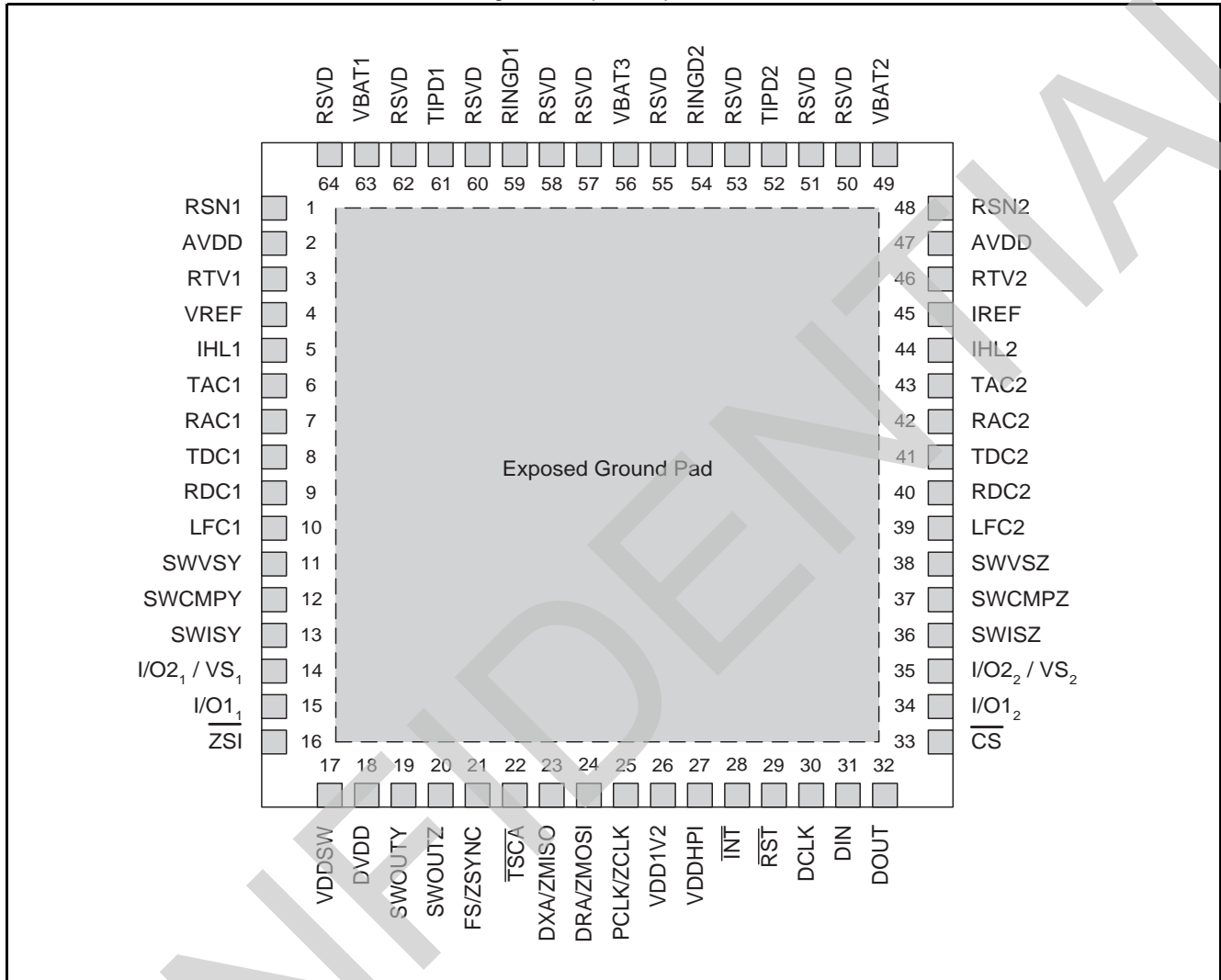


Figure 38 - ZL88801 Device Pinout (QFN-64) – Top View

Name	Type	Description
AVDD/DVDD	Power	3.3 V Analog and digital power supply inputs. AVDD and DVDD are provided to allow for noise isolation and proper power supply decoupling techniques. For best performance, all of the VDD power supply pins should be connected together at the power supply or power connection to the printed circuit board.
$\overline{\text{CS}}$	Input	In the PCM and SPI mode, the Chip Select input (active low) enables the device so that control data can be written to or read from the part. This pin features a weak (1.0 M Ω) internal pull-up to VDDHPI.
DCLK	Input	Data Clock. In the PCM and SPI mode, the Data Clock input shifts data into and out of the microprocessor interface of the device. The maximum clock rate is 8.192 MHz. This pin features a weak (1.0 M Ω) internal pull-up to VDDHPI.
DIN	Input	Data Input. In the PCM and SPI mode, control data is serially written into the device via the DIN pin, most significant bit first. The Data Clock determines the data rate. This pin features a weak (1.0 M Ω) internal pull-up to VDDHPI.
DOUT	Output	Data Output. In the PCM and SPI mode, control data is serially written out of the device via the DOUT pin, most significant bit first. The Data Clock determines the data rate. DOUT is high impedance except when data is being transmitted, which allows DIN and DOUT to be directly tied together in systems which use a single line for data input and output. This pin features a weak (1.0 M Ω) internal pull-up to VDDHPI.
DRA/ZMOSI	Input	PCM or ZSI Data Input. PCM voice (in PCM and SPI mode) or multiplexed PCM voice and control data (in ZSI mode) is written serially into the device through this pin, most significant bit first. PCLK/ZCLK determines the data rate.
DXA/ZMISO	Output	PCM or ZSI Data Output. PCM (in PCM and SPI mode) or multiplexed PCM voice and control data (in ZSI mode) is written serially out of the device through this pin, most significant bit first. PCLK/ZCLK determines the data rate.
FS/ZSYNC	Input	Interface synchronization signal for PCM voice (in PCM and SPI mode) or for multiplexed PCM voice and control channels (in ZSI mode).
IHL ₁ , IHL ₂	Output	High Level Current Drive Filter.
$\overline{\text{INT}}$	Output	Interrupt. $\overline{\text{INT}}$ is an active low output signal, which is programmable as either 3 V CMOS compatible or open drain (with external 4.7 K Ω pull-up resistor to VDDHPI required). This pin features a weak (1.0 M Ω) internal pull-up to VDDHPI.
I/O ₁ , I/O ₂	I/O	General Purpose Input/ Output 1 on Channels 1 and 2, respectively. Each of these two I/O's is capable of driving a 150 mW, 3 V relay (external catch diode required) or an LED, sinking up to 70 mA. Note, digital I/O pins may glitch low during AVDD power up.
I/O ₂ / VS1	I/O or Input	General Purpose Input/ Output 2 on Channel 1 or Voltage Sense 1. When configured as a voltage sense input, connect a 1.0 M Ω 1% resistor between this pin and the voltage to be monitored. The maximum working voltage rating of the resistor must be higher than the monitored voltage. Note, digital I/O pins may glitch low during AVDD power up.
I/O ₂ / VS2	I/O or Input	General Purpose Input/ Output 2 on Channel 2 or Voltage Sense 2. When configured as a voltage sense input, connect a 1.0 M Ω 1% resistor between this pin and the voltage to be monitored. The maximum working voltage rating of the resistor must be higher than the monitored voltage. Note, digital I/O pins may glitch low during AVDD power up.
IREF	Input	Current Reference. An external resistor R _{REF} connected between this pin and analog ground generates an accurate current reference used by the analog circuits on the chip.
LFC ₁ , LFC ₂	Output	Connection for longitudinal filter capacitor.
PCLK/ZCLK	Input	PCM or ZSI Data Clock 1.024 to 8.192 MHz. This is the clock for the PCM (in PCM and SPI mode) or ZSI (in ZSI mode) interfaces.
RAC ₁ , RAC ₂	Input	Ring lead AC sense. A series R + C network is connected from this pin to the Ring lead.
RDC ₁ , RDC ₂	Input	Ring lead DC Sense. A resistor is connected from this pin to the Ring lead. The connection can be to either side of the protection resistor.
RINGD ₁ , RINGD ₂	Output	RING-lead (B) output to the two-wire line.

RSN ₁ , RSN ₂	Input	High voltage line drive receive current summing node for each channel.
$\overline{\text{RST}}$	Input	Device Hardware Reset. A logic Low signal at this pin resets the device to its default state.
RSVD	Open	Reserved. Make no connection to this pin.
RTV ₁ , RTV ₂	Output	Drive output for two-wire AC impedance scaling resistor.
SWCMPY, SWCMPZ	Output	Compensation connection for switching regulator controller.
SWISY, SWISZ	Input	Current sense input for switching regulator controller.
SWOUTY, SWOUTZ	Output	Pulse output for drive to switching regulator circuit.
SWVSY, SWVSZ	Input	Voltage sense for switching regulator controller.
TAC ₁ , TAC ₂	Input	Tip lead AC Sense. A series R + C network is connected from this pin to the Tip lead.
TDC ₁ , TDC ₂	Input	Tip lead DC Sense. A resistor is connected from this pin to the Tip lead. The connection can be to either side of the protection resistor.
TIPD ₁ , TIPD ₂	Output	TIP-lead (A) output to two-wire line.
$\overline{\text{TSCA}}$	Output	Time Slot Control. The Time Slot Control output is open-drain (requiring an external 240 Ω pull-up resistor to VDDHPI, if used) and is normally inactive (high impedance). In the PCM and SPI mode, TSCA is active (low) when PCM data is transmitted on the DXA pin. This signal is not used in the ZSI mode and may be left floating.
VBAT ₁ , VBAT ₂	Supply	For BBABS operation: Low Negative Battery Supply, channel 1 and channel 2. Used for off-hook states. For STB operation: Negative Battery Supply, provides power for the high voltage line driver in all states.
VBAT ₃	Supply	For BBABS operation: High Negative Battery Supply. Used for on-hook, on-hook transmission (OHT), and ringing states. For STB operation: Negative Battery Supply, provides power for the high voltage line driver in all states.
VDD1V2	Output	Internally generated 1.2 V supply. Connect a 0.1 μF ceramic decoupling capacitor between this pin and ground.
VDDHPI	Power	Digital power supply input for SPI and PCM/ZSI pins. Place a 0.1 μF ceramic decoupling capacitor between this pin and ground.
VDDSW	Power	This supply powers circuitry used with the external switcher, tie directly to DVDD. Place a 0.1 μF ceramic decoupling capacitor between this pin and ground. For any other use or connection to this pin, contact Microsemi Customer Applications. To avoid stressing this pin, ensure that VDDSW is never hard tied to ground at any time, including during power up and power down cycles.
VREF	Output	Analog Voltage Reference. The VREF output has an external 10 μF ceramic capacitor connected to ground, filtering noise present on the internal voltage reference.
$\overline{\text{ZSI}}$	Input	ZSI Mode Select. Connect to ground for ZSI mode or to DVDD for PCM and SPI mode.
Exposed Ground Pad (EPAD/GND)	Power	Thermal Pad and Circuit Ground. Connect to a ground plane on the printed circuit board for thermal conduction and electrical connection to ground return. This is the only ground connection on the device.

8.0 Application Information

8.1 BBABS Line Interface Circuit

Figure 39 shows a typical line interface circuit for the ZL88801 when the switching regulator circuit is configured for buck-boost automatic battery switching. Decoupling, filtering, reference generation components and per channel protection are shown.

The parts list for this circuit is shown in “BBABS Line Interface Circuit Bill of Materials” on page 58. The BBABS switching regulator circuit is detailed in Figure 40. Consult Microsemi for the most recent reference design.

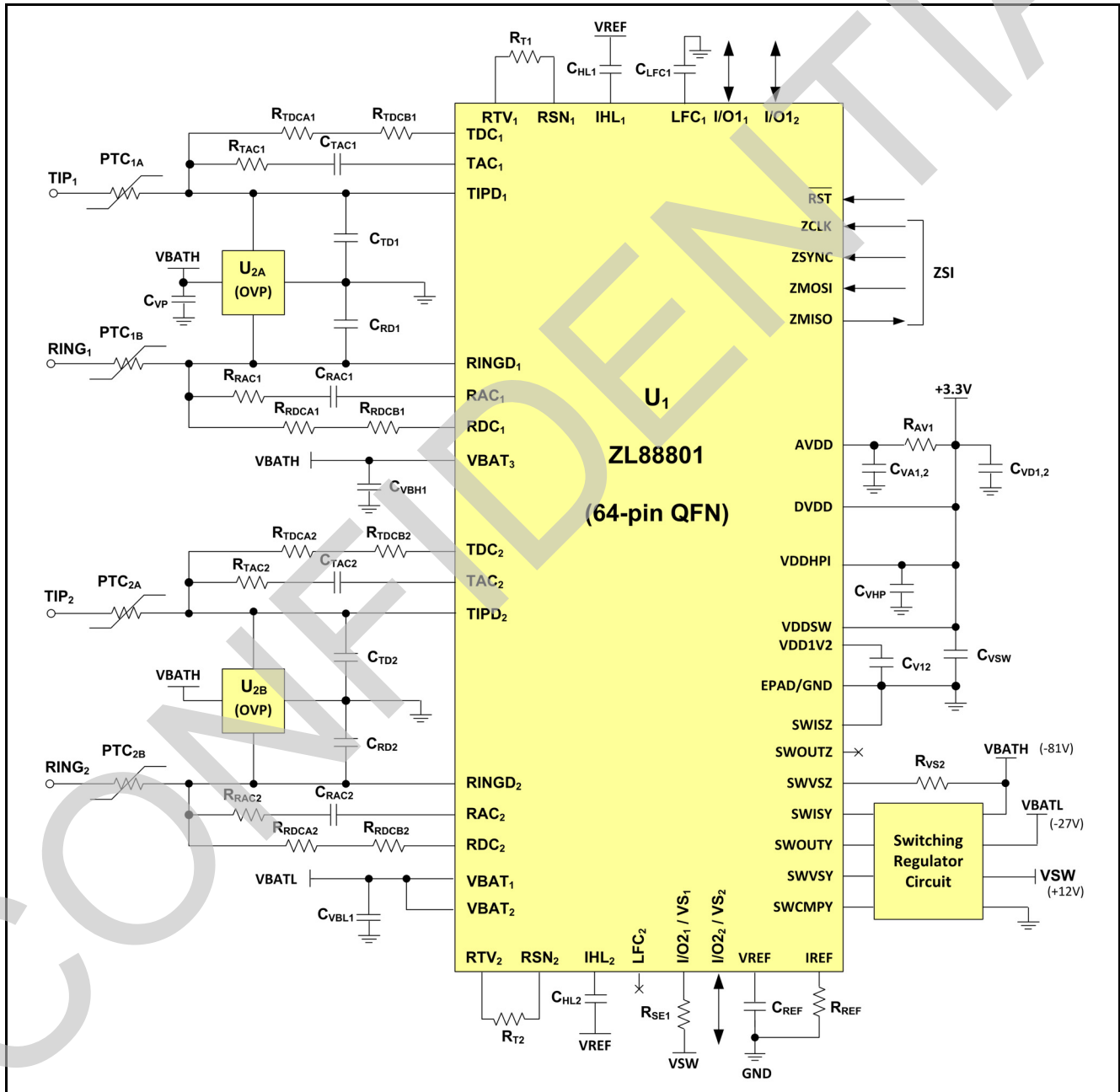


Figure 39 - ZL88801 BBABS Line Interface Circuit

8.2 BBABS Line Interface Circuit Bill of Materials

Qty.	Item	Type	Value	Tol.	Rating	Size	Note
4	C _{H1} 1, C _{H1} 2, C _{VA1} , C _{VD1}	Ceramic Capacitor	4.7 μ F, X5R	20%	6.3 V	0603	
3	C _{LFC1} , C _{V12} , C _{VA2}	Ceramic Capacitor	0.1 μ F, X7R	10%	16 V	0402	
8	C _{RAC1} , C _{RAC2} , C _{RD1} , C _{RD2} , C _{TAC1} , C _{TAC2} , C _{TD1} , C _{TD2}	Ceramic Capacitor	0.022 μ F, X7R	10%	100 V	0603 or 0805	1.
1	C _{REF}	Ceramic Capacitor	10 μ F, X5R	10%	6.3 V	0805	
1	C _{VBH1}	Ceramic Capacitor	0.01 μ F, X7R	20%	250 V	0805	
1	C _{VBL1}	Ceramic Capacitor	0.01 μ F, X7R	10%	50 V	0603	
2	C _{VD2} , C _{VHP}	Ceramic Capacitor	0.01 μ F, X7R	10%	16 V	0402	
1	C _{VP}	Ceramic Capacitor	0.1 μ F, X7R	10%	100 V	0805	1.
1	C _{VSW}	Ceramic Capacitor	0.047 μ F, X7R	10%	16 V	0402	
2	P _{TC1} , P _{TC2}	Dual Matched PTC Thermistors	7 Ω , 0.13 A Hold	20%	250 V _{RMS} / 3A		2., 3.
1	R _{AV1}	Resistor	1.0 Ω	5%	1/10 W	0603	
1	R _{RAC1} , R _{RAC2} , R _{TAC1} , R _{TAC2}	Resistor	10 K Ω	1%	150 V	0805	
8	R _{RDCA1} , R _{RDCA2} , R _{RDCB1} , R _{RDCB2} , R _{TDCA1} , R _{TDCA2} , R _{TDCB1} , R _{TDCB2}	Resistor	499 K Ω	1%	200 V	1206	
1	R _{REF}	High-Precision Thin Film Resistor	75.0 K Ω	0.5%, 25ppm	1/16 W	0402	4.
1	R _{SE1}	Resistor	1.0 M Ω	1%	50 V	0402	5.
1	R _{T1} , R _{T2}	Resistor	47.5 K Ω	1%	1/16 W	0402	
1	R _{VS2}	Resistor	1.00 M Ω	1%	150 V	0805	
1	U ₁	IC, Dual Channel Shared Battery Wideband VoicePort	Microsemi ZL88801		-100 V/-120 V	QFN-64	
1	U ₂	IC, Programmable Dual Channel SLIC Protector	Bourns TISP61089Q or TISP6NTP2C, STMicro LCDP1521S		-150 V/30 A	SOIC-8	2.

Notes:

- For designs with $\geq 70 V_{PK}$ maximum ringing, the rating of these capacitors should be increased to 200 V or 250 V.
- Protection components depend on the target application. The components on the BOM are believed to be suitable for ITU-T Recommendation K.21 (Basic Level) and Telcordia GR-1089-CORE Intra-Building compliance. Please check with Microsemi CMPG Customer Applications for component selection for other safety or EMC standards.
- Recommended dual PTCs include Bourns CMF-SDP07 or MF-SD013/250.
- The tolerance and stability of this resistor are critical as they affect calibration and measurement accuracy. Microsemi recommends using resistors with 0.5% tolerance and 25 ppm/ $^{\circ}$ C temperature coefficient for most applications. Examples include Susumu RR0510P-753-D, Panasonic ERA-2AED753X, and Yageo RT0402DRD0775KL. For high-performance applications, 0.1% 25 ppm/ $^{\circ}$ C resistors such as Panasonic ERA-2AEB753X or Yageo RT0402BRD0775KL are recommended.
- Populate only to sense the voltages shown on the schematic. Always make sure that these resistors are selected so that their maximum working DC voltage rating is more than the desired sensed voltage.

8.3 BBABS Switching Regulator Circuit

The BBABS switching regulator circuit uses an inverting buck-boost inductor based architecture with voltage doubler that regulates off of the low battery supply. Consult Microsemi for the most recent reference design.

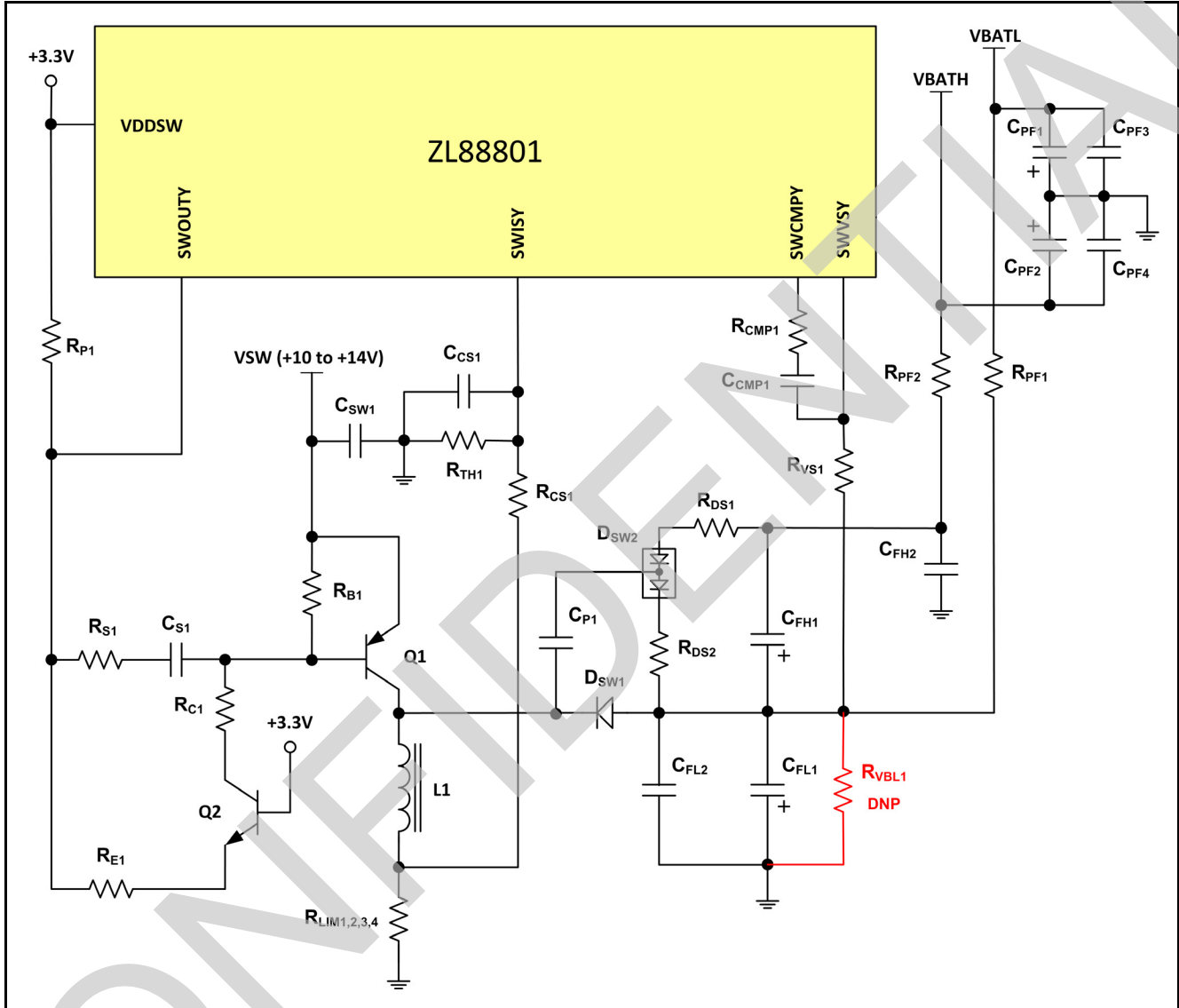


Figure 40 - BBABS Switching Regulator Circuit

8.4 BBABS Switching Regulator Circuit Bill of Materials

Qty.	Item	Type	Value	Tol.	Rating	Size	Notes
1	C _{CMP1}	Ceramic Capacitor	0.0022 μ F, X7R	10%	16 V	0402	
1	C _{CS1}	Ceramic Capacitor	220 pF, X7R	10%	25 V	0402	
2	C _{FH1} , C _{FL1}	Electrolytic Capacitor	22 μ F	20%	63 V		
2	C _{FH2} , C _{PF4}	Ceramic Capacitor	0.1 μ F, X7R	10%	100 V	0805	
2	C _{FL2} , C _{PF3}	Ceramic Capacitor	0.1 μ F, X7R	10%	50 V	0603	
1	C _{P1}	Ceramic Capacitor	0.22 μ F, X7R	10%	100 V	0805	
1	C _{PF1}	Electrolytic Capacitor	2.2 μ F	20%	50 V		
1	C _{PF2}	Electrolytic Capacitor	1.0 μ F	20%	100 V		
1	C _{S1}	Ceramic Capacitor	0.1 μ F, X7R	10%	25 V	0603	
1	C _{SW1}	Electrolytic Capacitor	220 μ F, Low ESR	20%	25 V		
1	D _{SW1}	Ultrafast Diode	ES1B		100 V, 1.0 A		
1	D _{SW2}	Dual Diode	BAV23S		200 V, 0.2 A	SOT23	1.
1	L1	Power Inductor	47 μ H	20%	1.5 A		
1	Q ₁	Transistor	PNP, Low V _{ce} , ZXTP2013G Diodes Inc.® or equivalent		100 V	SOT223	
1	Q ₂	Transistor	NPN, MMBT3904 Diodes Inc.® or equivalent			SOT23	
1	R _{B1}	Resistor	1 K Ω	5%	1/16 W	0402	
2	R _{C1} , R _{E1}	Resistor	75 Ω	5%	1/10 W	0603	
1	R _{CMP1}	Resistor	1.0 M Ω	1%	1/16 W	0402	
1	R _{CS1}	Resistor	3.01 K Ω	1%	1/16 W	0402	
2	R _{DS1} , R _{PF2}	Resistor	10 Ω	5%	1/4 W	1206	
2	R _{DS2} , R _{PF1}	Resistor	5.1 Ω	5%	1/4 W	1206	
4	R _{LIM1} , R _{LIM2} , R _{LIM3} , R _{LIM4}	Resistor	1.0 Ω	5%	1/16 W	0402	
1	R _{P1}	Resistor	10 K Ω	5%	1/16 W	0402	
1	R _{S1}	Resistor	0 Ω	5%	1/16 W	0402	
1	R _{TH1}	Resistor	1 K Ω	1%	1/16 W	0402	
1	R _{VBL1}	Resistor	51 K Ω	5%	1/10 W	0603	Do not populate
1	R _{VS1}	Resistor	1.0 M Ω	1%	1/8 W	0805	

Notes:

1. Repetitive peak forward surge current rating of 600 mA.

8.5 STB Line Interface Circuit

Figure 41 shows a typical line interface circuit for the ZL88801 with shared protection. The device is configured for operation in the PCM and SPI mode. Decoupling, filtering, and reference generation components are shown. The switching regulator circuit is detailed in Figure 42. Consult Microsemi for the most recent reference design.

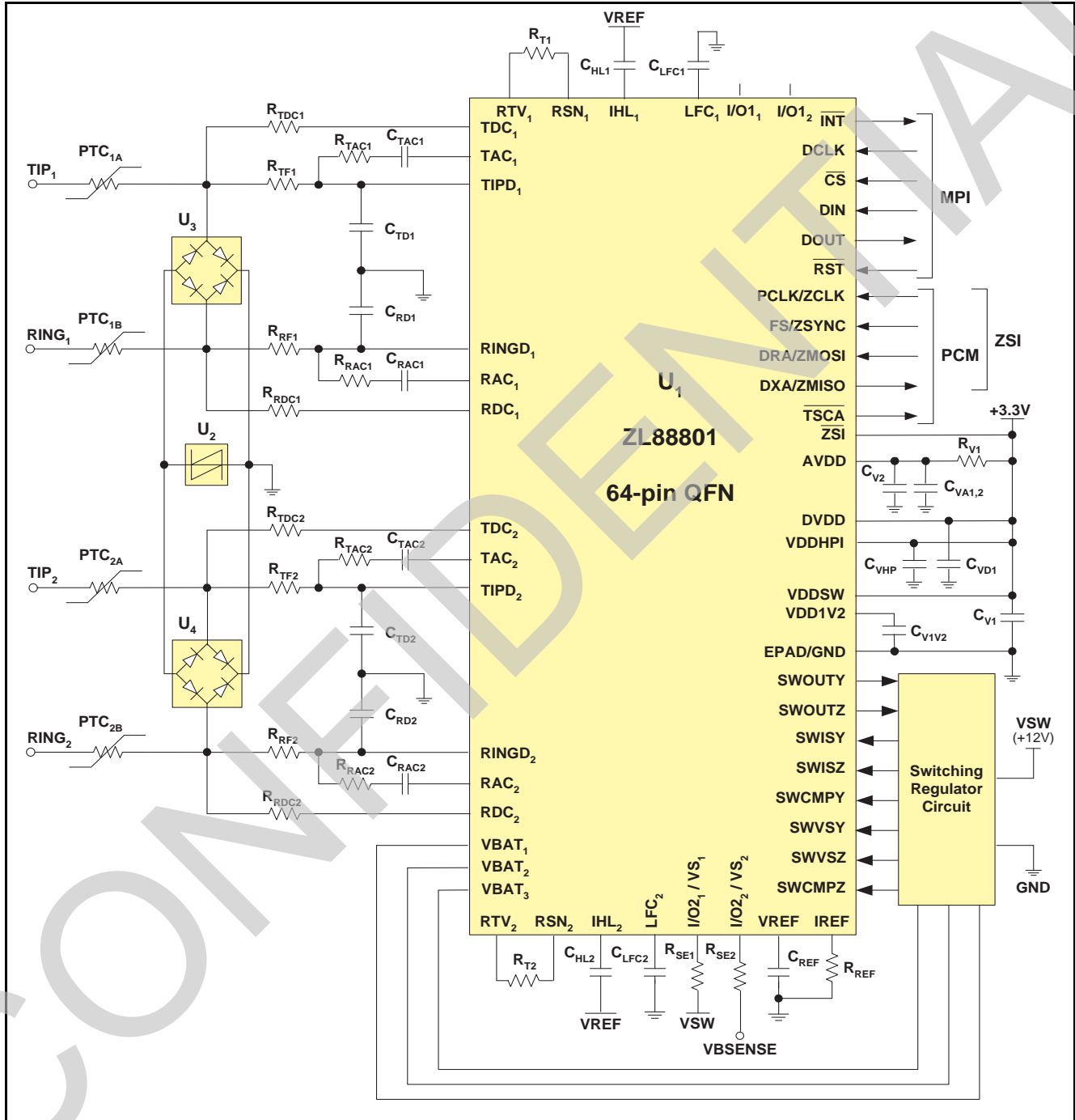


Figure 41 - ZL88801 STB Line Interface Circuit

8.6 STB Line Interface Circuit Bill of Materials

Qty.	Item	Type	Value	Tol.	Rating	Size	Notes
6	C _{H1} 1, C _{H1} 2, C _{LFC} 1, C _{LFC} 2, C _{V1} , C _{V2}	Ceramic Capacitor	4.7 μ F, X5R	20%	6.3 V	0603	
8	C _{RAC} 1, C _{RAC} 2, C _{RD} 1, C _{RD} 2, C _{TAC} 1, C _{TAC} 2, C _{TD} 1, C _{TD} 2	Ceramic Capacitor	0.022 μ F, X7R	10%	100 V	0603 or 0805	
1	C _{REF}	Ceramic Capacitor	10 μ F, X5R	10%	6.3 V	0805	
3	C _{V1V2} , C _{V1} 1, C _{V1} 2	Ceramic Capacitor	0.1 μ F, X7R	10%	10 V	0402	
2	C _{VD} 1, C _{VHP}	Ceramic Capacitor	0.01 μ F, X7R	10%	16 V	0402	
2	PTC ₁ , PTC ₂	Dual PTC Thermistors	25 Ω , 0.13 A Hold	20%	250 V _{RMS} / 3A		1.
4	R _{RAC} 1, R _{RAC} 2, R _{TAC} 1, R _{TAC} 2	Resistor	10 K Ω	1%	150 V	0603	
4	R _{RDC} 1, R _{RDC} 2, R _{TDC} 1, R _{TDC} 2	Resistor	1.0 M Ω	1%	200 V	1206	
1	R _{REF}	Resistor	75.0 K Ω	0.5%	1/16 W	0402	
4	R _{RF} 1, R _{RF} 2, R _{TF} 1, R _{TF} 2	Resistor	20 Ω	1%	1/4 W	1206	
1	R _{SE} 1	Resistor	1.0 M Ω	1%	1/10 W	0603	2.
1	R _{SE} 2	Resistor	1.0 M Ω	1%	1/8 W	0805	2.
2	R _{T1} , R _{T2}	Resistor	47.5 K Ω	1%	1/16 W	0402	
1	R _{V1}	Resistor	1 Ω	5%	1/16 W	0402	
1	U ₁	IC, Dual Channel Shared Battery Wideband VoicePort	Microsemi ZL88801			QFN-64	
1	U ₂	Bidirectional Thyristor Overvoltage Protector	Bourns® TISP4115M3 or equivalent			DO- 214AC	1.
2	U ₃ , U ₄	Fast Recovery Bridge Rectifier	Vishay® RMB2S or equivalent			TO- 269AA	1.

Notes:

1. Protection components depend on the target application.
2. Populate only to sense the voltages shown on the schematic. Always make sure that these resistors are selected so that their maximum working DC voltage rating is more than the desired sensed voltage.

8.7 STB Switching Regulator Circuit

The STB switching regulator circuit uses an inverting buck-boost architecture that automatically produces the negative supply voltage (VBAT) that powers both channels. VBAT is dynamically determined by the channel that requires the most negative voltage. Consult Microsemi for the most recent reference design.

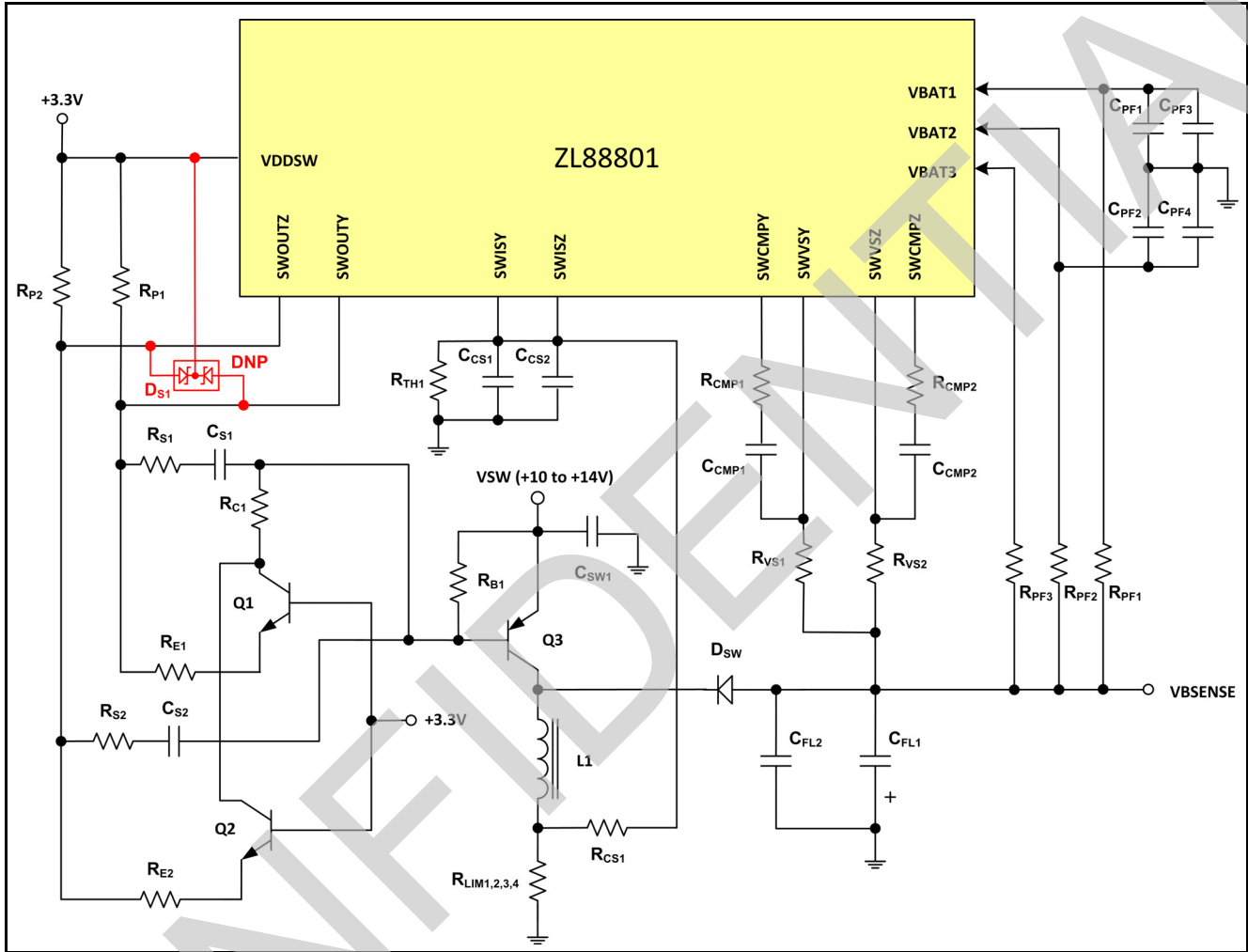


Figure 42 - STB Switching Regulator Circuit

8.8 STB Switching Regulator Circuit Bill of Materials

Qty.	Item	Type	Value	Tol.	Rating	Size	Notes
2	C _{CMP1} , C _{CMP2}	Ceramic Capacitor	0.0022 μ F, X7R or COG	10%	16 V	0402	
2	C _{CS1} , C _{CS2}	Ceramic Capacitor	100 pF, X7R or COG	10%	16 V	0402	
1	C _{FL1}	Electrolytic Capacitor	4.7 μ F, Low ESR	20%	100 V		
3	C _{FL2} , C _{PF3} , C _{PF4}	Ceramic Capacitor	0.1 μ F, X7R	10%	100 V	0805	
2	C _{PF1} , C _{PF2}	Electrolytic Capacitor	1.0 μ F	20%	100 V		
2	C _{S1} , C _{S2}	Ceramic Capacitor	0.047 μ F, X7R	10%	25 V	0603	
1	C _{SW1}	Ceramic Capacitor	10 μ F, X5R	20%	25 V	1206	
1	D _{S1}	Schottky Diodes	BAT54CTA		30 V, 0.2 A	SOT23	Optional
1	D _{SW}	Ultrafast Diode	ES1C		150 V, 1.0 A		
1	L1	Power Inductor	33 μ H	20%	2.9 A		
2	Q ₁ , Q ₂	Transistor	MMBT3904 Diodes Inc.® or equivalent		40 V, 0.2 A	SOT23	
1	Q ₃	Transistor	ZXTP2014G Diodes Inc.® or equivalent		140 V, 4.0 A	SOT223	
1	R _{B1}	Resistor	1 K Ω	5%	1/16 W	0402	
1	R _{C1}	Resistor	75 Ω	5%	1/8 W	0805	
2	R _{CMP1} , R _{CMP2}	Resistor	1.0 M Ω	1%	1/16 W	0402	
1	R _{CS1}	Resistor	5.11 K Ω	1%	1/16 W	0402	
2	R _{E1} , R _{E2}	Resistor	33 Ω	5%	1/10 W	0603	
4	R _{LIM1} , R _{LIM2} , R _{LIM3} , R _{LIM4}	Resistor	1 Ω	5%	1/10 W	0603	
2	R _{P1} , R _{P2}	Resistor	10 K Ω	5%	1/16 W	0402	
2	R _{PF1} , R _{PF2}	Resistor	47 Ω	5%	1/4 W	1206	
1	R _{PF3}	Resistor	10 Ω	5%	1/4 W	1206	
2	R _{S1} , R _{S2}	Resistor	5.1 Ω	5%	1/16 W	0402	
1	R _{TH1}	Resistor	750 Ω	1%	1/16 W	0402	
2	R _{VS1} , R _{VS2}	Resistor	1.0 M Ω	1%	1/8 W	0805	

9.0 Programming the ZL88801

The ZL88801 device is programmed through the *VoicePath Application Program Interface II (VP-API-II)*. This API hides the complexity of the device and its internal registers and provides a much simpler interface to the software engineer. The *VoicePath Software Development Kit (SDK)* accelerates the development cycle and reduces the development time. It also allows the user to build on proven software that is currently used to control over 100 million subscriber lines worldwide.

9.1 Programmable Features

The features directly supported by *VP-API-II* are dependent upon the underlying device capabilities. The following features are supported by the *VP-API-II* for the ZL88801:

- AC and DC coefficient programming
- Ringing parameter (amplitude, frequency, bias, type) and power management
- Tone generation (frequency, amplitude, and modulation)
- Programmable tone and ringing cadence
- Universal Caller ID generation (Types 1 and 2) with FSK and DTMF signaling
- Loop start signaling, including dial pulse detection
- Ground start signaling
- Seamless integration of the Microsemi *VeriVoice Professional Test Suite Software for Telcordia® GR-909-CORE* metallic loop testing
- Four modes of interrupt support

9.2 VoicePath SDK Overview

The *VoicePath Software Development Kit (SDK)* is a software package provided to simplify development using Microsemi voice products. It consists of:

1. *VoicePath API-II* or *VoicePath API-II Lite* – C source libraries to abstract the Microsemi ZL880, VE790, VE880, and VE890 devices from the application code. The *VP-API-II* contains the full software and requires a Software License Agreement (SLA). The *VP-API-II Lite* is a subset of the full *VP-API-II* and allows for basic functionality for initialization and state / event handling. It does not include tone or ringing cadencing or Caller ID generation. The *VP-API-II Lite* does not require an SLA and is suitable for use in open-source applications. This data sheet and associated feature descriptions and specifications require *VP-API-II* version 2.20.1 or later be used.
2. *VoicePath Profile Wizard* – A Windows GUI application that aids in the organization and creation of *Profiles* used in the *VP-API-II* into a single project file.
3. Example Hardware Abstraction Layer (HAL) and System Services functions required by *VP-API-II*.
4. Example applications using *VP-API-II* functions. Provided to help the programmer verify correct implementation of the HAL, System Services, and *VP-API-II* function use.
5. Microsemi *Telephony Applications Platform (ZTAP)* – This optional hardware platform is used to demonstrate the capabilities of devices or chip sets in the ZL880, VE880 and VE890 families.
6. *ZTAP Support Package* – This software package contains system files for the ZTAP board and Microsoft Windows USB drivers for communicating with it.
7. *Microsemi Voice Toolkit* – A collection of menu-driven applications to be used in conjunction with the ZTAP for demonstration and testing. It includes *VP-Script*, a TCL/TK-based scripting environment, and *Mini-PBX*, a call control and routing application.

9.3 VoicePath API-II Software Overview

9.3.1 Introduction

The Microsemi *VoicePath Application Programming Interface II (VP-API-II)* is a C source code module that provides a standard software interface for controlling, testing, and passing digitized voice through a set of subscriber lines using the Microsemi family of voice termination devices. This section describes a few of the device and line control capabilities using the *VP-API-II* interface. For a complete list, refer to *ZL880 VP-API-II Reference Guide*. *VP-API-II* uses the layered architecture shown below. The portion of the diagram in white is Microsemi-provided code, while the gray portions are customer-provided.

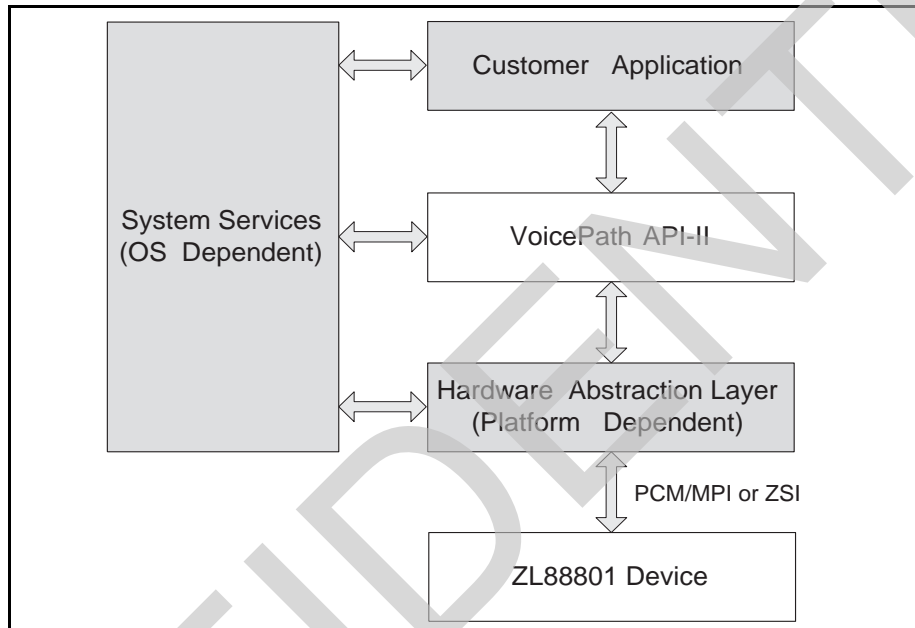


Figure 43 - VP-API-II Software Architecture

9.3.2 Customer Application

This block represents the user's line management module that performs tasks such as initializing the system, configuring lines, changing the line states in response to line events and other inputs, switching digitized voice traffic, etc. Microsemi provides example implementations of this layer as part of the *VoicePath SDK*.

9.3.3 VoicePath API-II

The *VoicePath API-II* is the core component of the Microsemi *VoicePath SDK*. This software module runs on the host microprocessor that controls one or more Microsemi voice telephony devices. This code is provided by Microsemi and should not require modification by the application developer.

9.3.4 Hardware Abstraction Layer

The Hardware Abstraction Layer (HAL) provides access to Microsemi voice telephony devices through the SPI or the multiplexed ZSI interfaces, depending on the selected device and mode. The HAL software is platform-dependent and must be implemented by the *VP-API-II* user. Microsemi provides example HAL source code with the *VoicePath SDK*.

9.3.5 System Services Layer

The System Services layer provides critical section, timing and interrupt control functions. These functions are system-dependent and must be implemented specifically for each platform on which the *VP-API-II* is used. Microsemi provides example System Services code for use with the Microsemi *ZTAP*. The following functions are included in the System Services layer.

Function Name	Description
VpSysEnterCritical()	A semaphore operation to provide protected access to device or shared memory. Required only in multi-threaded architectures.
VpSysExitCritical()	A semaphore operation to release protected access to device or shared memory. Required only in multi-threaded architectures.
VpSysWait()	Delay operator used to suspend program/thread execution. Delay parameter passed in 125 μ s steps.
VpSysDebugPrintf()	Print mechanism used by <i>VP-API-II</i> debug features.
VpSysTestInt()	Interrupt function for Efficient Poll Mode. Required for backward compatibility with <i>VE880</i> code.

Table 8 - VP-API-II Functions for System Services

9.4 System Configuration Functions

Two main functions in *VP-API-II* are required in all applications are listed below:

Function Name	Description
VpMakeDeviceObject()	Configures a specific device (chip select) to a device context. Provides <i>VP-API-II</i> with device specific type (<i>deviceType</i>).
VpMakeLineObject()	Configures a specific line (channel) to a line and device context. Provides <i>VP-API-II</i> with line specific type (<i>termType</i>).

Table 9 - VP-API-II Functions for System Configuration

When using the ZL88801 device, the following settings must be used:

- The value for *deviceType* in *VpMakeDeviceObject()* must be: `VP_DEV_887_SERIES`
- The value for *termType* in *VpMakeLineObject()* must be:
 - `VP_TERM_FXS_GENERIC` when *channelId* = 0 and Normal Standby operation is desired
 - `VP_TERM_FXS_LOW_PWR` when *channelId* = 0 and Low Power Standby operation is desired.

Please refer to *ZL880 VP-API-II Reference Guide* for additional details.

9.5 Initialization

The *VP-API-II* functions that perform initialization are listed below. Please refer to [10.0, "VP-API-II Profiles" on page 71](#) for the use of these functions with each associated *Profile*.

Function Name	Description
VpInitDevice()	Resets and initializes device with parameters defined in the specified <i>Profiles</i> .
VpInitLine()	Resets and initializes line with parameters defined in the specified <i>Profiles</i> .
VpInitRing()	User function to provide Ringing Cadence. Also allows use selection of <i>Caller ID Profile</i> associated with ringing.

9.6 Line State Control

The Signaling Control blocks process the Line State information to perform related control functions such as DC feed, ringing generation, and line test for each channel.

Fifteen system states are possible for the operation of the FXS channel on the ZL88801: `VP_LINE_DISABLED`, `VP_LINE_DISCONNECT`, `VP_LINE_STANDBY`, `VP_LINE_TIP_OPEN`, `VP_LINE_OHT`, `VP_LINE_ACTIVE`, `VP_LINE_TALK`, `VP_LINE_RINGING`, `VP_LINE_HOWLER`, and corresponding reverse polarity of each state.

Function Name	Description
<code>VpSetLineState()</code>	Sets line to state specified. After <code>VpInitDevice()</code> or <code>VpInitLine()</code> , the default line state is <code>VP_LINE_DISCONNECT</code> .

Table 10 - VP-API-II Functions for Line State Control

9.6.1 VP_LINE_DISABLED

`VP_LINE_DISABLED` is the power up and hardware reset state of the device. The System State register is in *Shutdown*, the voice channel is deactivated and the switching regulator is off. No transmission or signaling is possible. This state can also be entered due to certain fault conditions such as battery overvoltage or clock fault.

9.6.2 VP_LINE_DISCONNECT

In the `VP_LINE_DISCONNECT` state, the SLIC block outputs are shut off providing a high impedance to the line. This state can be used for denial of service. The switching regulator is active and outputs the programmed SWFV floor voltage. The voice channel is normally deactivated, but can be activated and used with the converter configuration command to monitor the voltages on Tip or Ring for line diagnostics.

9.6.3 VP_LINE_STANDBY

The `VP_LINE_STANDBY` state is used when On-Hook. This state behaves differently based on the FXS line termination type selected according to [“System Configuration Functions” on page 67](#).

If the termination type `VP_TERM_FXS_GENERIC` is selected, the DC feed is active, and hook supervision functions are enabled. The loop feed polarity is controlled by the *VP-API-II*. The high voltage switching regulator only generates the voltage needed to support the DC line voltage defined by the DC feed curve shown in [Figure 16, “Active State I / V Characteristic” on page 23](#). The DC feed drives Tip and Ring to the programmed VOC. Voice transmission is disabled to save power.

If the termination type `VP_TERM_FXS_LOW_PWR` is selected, a special *Low Power Idle Mode (LPIM)* state is supported to reduce on-hook power consumption to about 45 mW per channel, while still being able to detect off-hook transitions. In this mode, the DC feed is not active and a voltage is presented to the Ring lead. The line voltage is monitored so that any transitions to off-hook state can be detected. Voice transmission is disabled in this state.

9.6.4 VP_LINE_OHT

In the `VP_LINE_OHT` states, the DC feed is activated and voice transmission is enabled. `VP_LINE_OHT` allows the transmission of Caller ID information. Hook supervision functions are operating. The switching regulator only generates the negative high voltage needed to support the DC line voltage defined by the DC feed curve. In this way, power consumption is minimized.

9.6.5 VP_LINE_ACTIVE, VP_LINE_TALK

In the VP_LINE_ACTIVE and VP_LINE_TALK states, the DC feed is activated. The PCM highway is enabled in VP_LINE_TALK and disabled in VP_LINE_ACTIVE. Both states allow the transmission of Caller ID information for Type 2 Caller ID. Hook supervision functions are operating. The switching regulator only generates the negative high voltage needed to support the DC line voltage defined by the DC feed curve. In this way, power consumption is minimized.

9.6.6 VP_LINE_TIP_OPEN

In the VP_LINE_TIP_OPEN state, the device provides a high impedance on the Tip lead and drives the Ring lead to the programmed VOC voltage. The loop supervision detector monitors the ground key current. When this current is larger than the programmed threshold, the VP-API-II reports a ground start event. This state can also be used to determine Ring to ground leakage and Ring to ground capacitance in combination with the appropriate converter configuration.

9.6.7 VP_LINE_RINGING

In the VP_LINE_RINGING state, the voice DAC is used to apply the ringing signal generated from Signal Generator A and the Bias generator to the SLIC block. Internal feedback maintains a low (200 Ω) system output impedance during ringing. The current limit is increased in the *Ringing* state and is programmable via the parameter, ILR. In order to minimize line transients, entry and exit from the VP_LINE_RINGING states are intelligently managed by the ZL88801. When ringing is requested by the user, the corresponding signal generators are started but not applied to the subscriber line until the ringing voltage is equal to the on-hook Tip-Ring voltage. This algorithm, known as *Ring Entry*, assures that there is a smooth line transition when entering the VP_LINE_RINGING state. *Ring Entry* is guaranteed to occur within one period of the programmed ringing frequency. *Ring Exit* is an analogous procedure whereby the ringing signal is not immediately removed from the line after a ring trip or new state request. The ringing signal will persist until its voltage is equal to the required line voltage. Ring Entry and Ring Exit are configured using the VP-API-II option VP_OPTION_ID_RING_CNTRL.

While in the VP_LINE_RINGING state, the integrated switching regulator may be programmed to behave in one of two ways: tracking or fixed. Note that these three topologies require different external switching power supply components. See [“Device Profile” on page 74](#) and [“Ringing Profile” on page 77](#) for information on setting the switcher topology.

9.6.8 VP_LINE_HOWLER

In the VP_LINE_HOWLER state, the transmit (A to D) voice path and impedance generation are disabled. Gain is increased by 11.5 dB compared to a 0 dB D/A setting.

9.7 Line Status Monitoring

Line status is monitored by the VP-API-II using the functions listed in [Table 11](#).

Function Name	Description
VpGetEvent ()	Typically used to implement event driven method to monitor line status. Provides event queue such that a single event reported for each instance function is called (when an event is active).
VpGetLineStatus ()	Typically used to implement polling method to monitor line status.
	• VP_INPUT_HOOK -- Hook Status timing per Dial Pulse Detection.
	• VP_INPUT_RAW_HOOK -- Real time hook status. Changes during Dial Pulse
	• VP_INPUT_GKEY -- Real time ground key status.

Table 11 - VP-API-II Functions for Line Status Monitoring

9.8 Input / Output Control

The ZL88801 device features four general purpose I/O pins that can be configured by the user as inputs, outputs, or relay drivers. All I/O pins are configured and accessed through the *VP-API-II* using the functions listed in [Table 12](#)

Function Name	Description
VpSetOption()	<p>VP_DEVICE_OPTION_ID_DEVICE_IO - Used to configure pins individually as input, output, or as a voltage sense pin. Parameter <code>directionPins_31_0</code> used to set pin as input (0) or output (1). Bit in <code>directionPins_31_0</code> corresponding to I/O is (I/O₁ = 0x1, I/O₂ = 0x2, I/O₁= 0x4, and IO₂ = 0x8). Other bits in <code>directionPins_31_0</code> are ignored.</p> <p>Configuring output type done by setting corresponding bit location in <code>outputTypePins_31_0</code> with VP_OUTPUT_DRIVEN_PIN (driven).</p> <p>Note that when writing a '1' to a driven pin results in voltage being present on the corresponding I/O pin.</p>
VpGetOption()	<p>VP_DEVICE_OPTION_ID_DEVICE_IO - Retrieves current I/O pin configuration. When calling <code>VpGetOption()</code>, an event (Response Category, Event ID VP_LINE_EVID_RD_OPTION) is generated and must be processed by the host application. Host application then calls <code>VpGetResults()</code> with pointer to structure of type <code>VpOptionDeviceIoType</code> that is filled in by <i>VP-API-II</i> with current I/O configuration data.</p>
VpDeviceIoAccess()	<p>Parameter <code>accessMask_31_0</code> provides bit field access to the I/O pins as (I/O₁ = 0x1, I/O₂ = 0x2, I/O₁= 0x4, and IO₂ = 0x8). Access is by 'OR' combination, so <code>accessMask_31_0 = 0x0F</code> provides access to all lines simultaneously.</p> <p>The <code>accessType</code> parameter indicates read (VP_DEVICE_IO_READ) or write (VP_DEVICE_IO_WRITE) operation.</p> <p>For write operation, <code>deviceIOData_31_0</code> is used to set lines to '0' or '1'. Bit mask is same as <code>accessMask_31_0</code> (I/O₁ is set to value in <code>deviceIOData_31_0</code> location 0x1, I/O₂ in <code>deviceIOData_31_0</code> location 0x2, and so on).</p> <p>All other parameters (<code>accessMask_63_32</code> and <code>deviceIOData_63_32</code>) are ignored for the ZL88801)</p>

Table 12 - VP-API-II Functions for Configuring and Accessing I/O Lines

10.0 VP-API-II Profiles

Profiles are structures that contain design data to meet specific system requirements. Many *VP-API-II* functions take *Profiles* as one or more arguments. There are several types of *Profiles*. Each defines a different set of parameters for a service aspect of the device. [Table 13](#) provides a summary of all the *Profiles* that are used by the *VP-API-II* with the ZL88801 device. *Profiles* are created using *VP Profile Wizard*.

Profile Name	Description
Device	The <i>Device Profile</i> provides default start-up values for device-specific configuration options that are normally set at initialization and never changed. These options include the Pulse Code Modulation (PCM) bus clock frequency and configuration information, interrupt mode, voltage monitoring mode, dial pulse correction, device mode register, and switching regulator configuration. The <i>ZL880 Device Profile</i> is not compatible with the version used in the <i>VE880</i> due to the added features.
AC FXS	Used for programming the transmission characteristics of the system, the <i>AC FXS Profile</i> holds the programmable gain and filter coefficient data. Over 70 country-specific <i>AC FXS Profiles</i> are provided and the user can select the one or ones that are required for his or her application. The <i>ZL880 AC FXS Profile</i> is compatible with the <i>VE880 AC Profile</i> .
DC	The <i>DC Profile</i> holds the DC feed and loop supervision parameters. The <i>ZL880 DC Profile</i> is not compatible with the <i>VE880 DC Profile</i> due to the added features.
Ringing	The <i>Ringing Profile</i> contains the necessary commands and data to set up the ring generator of an FXS channel. Different <i>Profiles</i> can be used to vary the ringing characteristics of a line. Options available in the <i>Ringing Profile</i> include ringing waveform, frequency, amplitude, DC offset, ring trip method, maximum peak power, and ring cadence control. The <i>ZL880 Ringing Profile</i> is not compatible with the <i>VE880 Ringing Profile</i> due to the added features.
Tone	The <i>Tone Profile</i> defines the various call progress tones that might be used in the FXS channel. The tones include dial tone, busy, ring-back, re-order, and howler. This <i>Profile</i> is compatible with the one used with the <i>VE880</i> family.
Ringing Cadence	The <i>Ringing Cadence Profile</i> defines the cadence that is associated with ringing. This <i>Profile</i> is compatible with the one used with the <i>VE880</i> family.
Tone Cadence	The <i>Tone Cadence Profile</i> defines the various call progress cadences that might be used in a system. The cadences include stutter dial, busy, ring-back, and reorder. This <i>Profile</i> is compatible with the one used with the <i>VE880</i> family.
Caller ID	The <i>Caller ID Profile</i> defines the on- and off-hook signal generation for services such as Caller ID and message waiting indication. This <i>Profile</i> abstracts the physical and data link layers of the protocol. FSK and DTMF signaling are supported. This <i>Profile</i> is compatible with the one used with the <i>VE880</i> family.
Metering	The <i>Metering Profile</i> sets the frequency (12- or 16-kHz), transition type, peak current, and echo voltage limits. This <i>Profile</i> is not compatible with the one used with the <i>VE880</i> family due to added parameters.

Table 13 - VP-API-II Profile Types

10.1 Profile Wizard Project Definition

The *Profile Wizard* application allows the user to define the requirements of the telephone line characteristics, switching and signaling with an intuitive user interface. After selecting the requirements, the user can generate the corresponding *Profiles* (.c and .h files) which the *VP-API-II* software uses to initialize and control the ZL88801 device. Microsemi provides many example *Profiles* based on known country or standard requirements.

After launching *Profile Wizard*, it presents the user with the option of creating a new project based on a Microsemi telephony device family or evaluation board or to open an existing project.

[Figure 44](#) shows a typical screen shot for getting started and creating a new project.

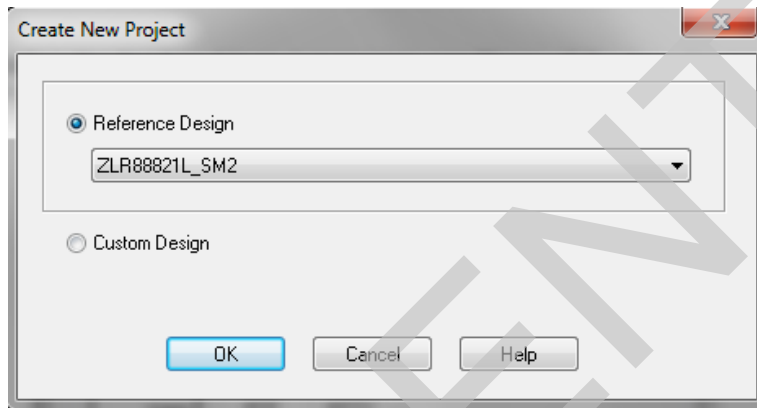


Figure 44 - Profile Wizard Screen - Creating a New Project

10.2 Profile Wizard Main Menu

Figure 45 shows a screen shot of the main menu of *Profile Wizard* with a sample ZL88801 project loaded.

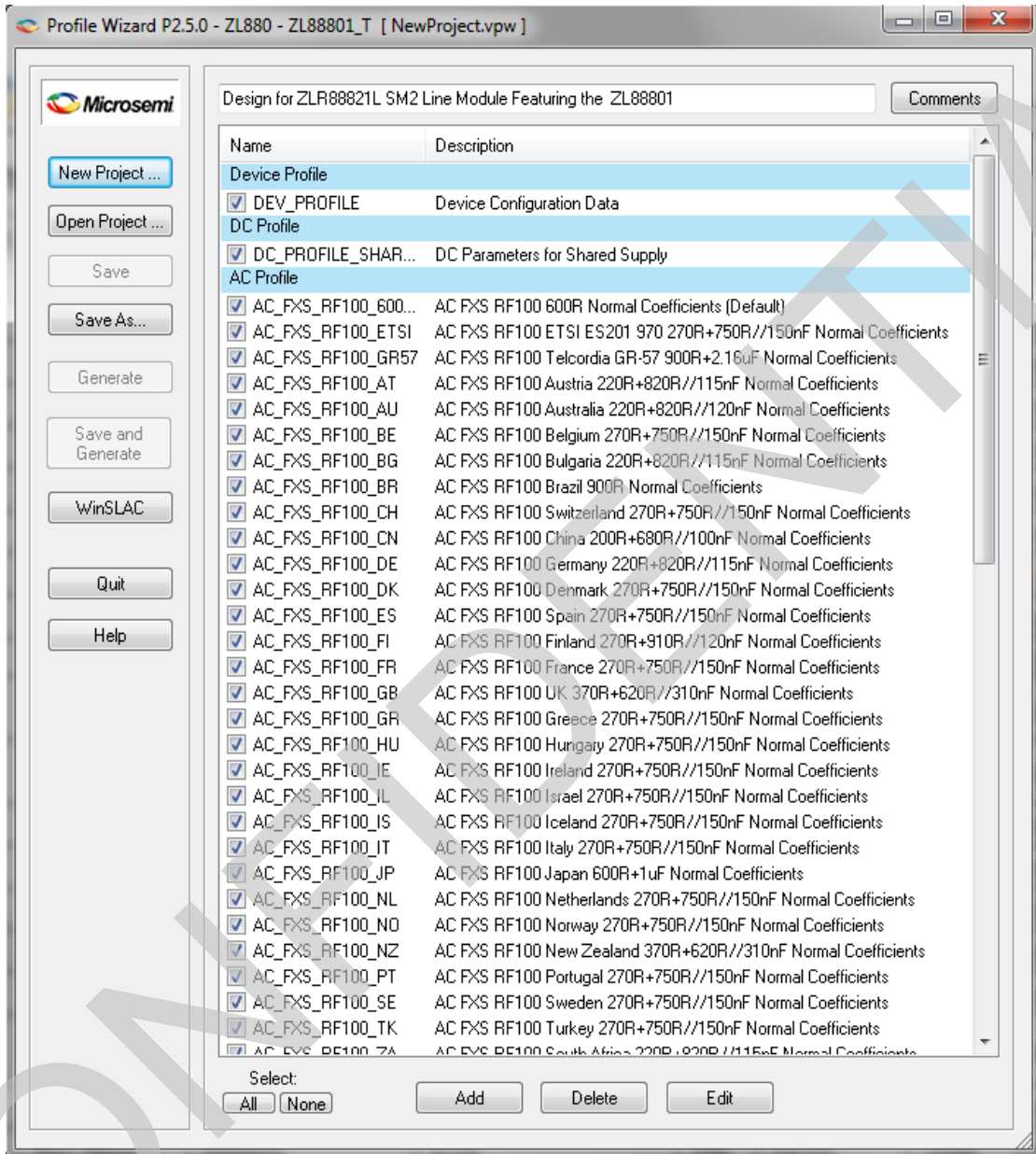


Figure 45 - Profile Wizard - Main Menu

10.3 Device Profile

10.3.1 Overview

The *Device Profile* configures device or circuit level parameters for the entire device. This *Profile* is required to enable reliable host communication with the device, to configure the switching regulator, and to define *VP-API-II* driver parameters. An example *Device Profile* configuration for the *ZL88801* using *VP Profile Wizard* is shown in [Figure 46](#).

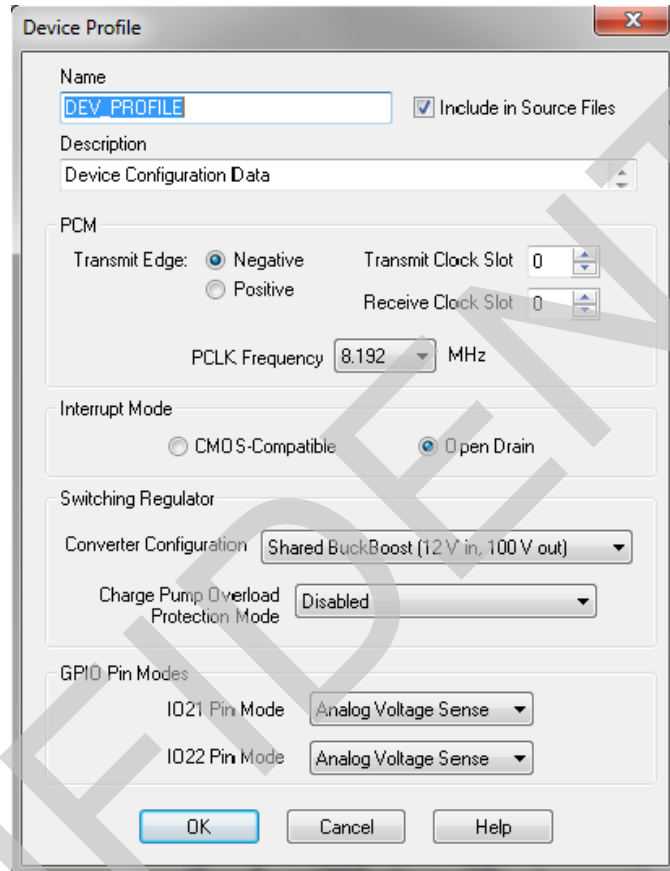


Figure 46 - Profile Wizard - Device Profile Configuration

[Table 14](#) lists the *VP-API-II* functions which use values that are defined in the *Device Profile*.

Function Name	Description
VpInitDevice()	Resets and initializes device with parameters defined in <i>Device Profile</i> and optionally configures all lines on the device with AC, DC, and Ringing parameters.
VpCalLine()	This function may need to be called under some circumstances following the above function. Refer to the <i>ZL880 VP-API-II Reference Guide</i> for more details.

Table 14 - VP-API-II Functions For Device Configuration

10.4 AC FXS Profiles

AC FXS Profiles are used to define the input impedance, receive and transmit frequency response, hybrid balance, and initial gain values. Microsemi provides AC FXS Profile examples for over 70 countries including the following:

Input Impedance	Network Balance Impedance	Countries
150 Ω + (510 Ω // 47 nF)	150 Ω + (510 Ω // 47 nF)	Russia
200 Ω + (680 Ω // 100 nF)	200 Ω + (680 Ω // 100 nF)	China
220 Ω + (820 Ω // 115 nF)	220 Ω + (820 Ω // 115 nF)	Bulgaria, Germany, and South Africa
220 Ω + (820 Ω // 120 nF)	220 Ω + (820 Ω // 120 nF)	Australia
270 Ω + (750 Ω // 150 nF)	270 Ω + (750 Ω // 150 nF)	Belgium, Croatia, Denmark, Egypt, Estonia, France, Greece, Hungary, Iceland, Ireland, Israel, Italy, Ivory Coast, Netherlands, Nigeria, Norway, Portugal, Romania, Spain, Sweden, Switzerland, and Turkey
270 Ω + (910 Ω // 120 nF)	270 Ω + (1200 Ω // 120 nF)	Finland
370 Ω + (620 Ω // 310 nF)	370 Ω + (620 Ω // 310 nF)	New Zealand
300 Ω + (1000 Ω // 220 nF)	370 Ω + (620 Ω // 310 nF)	United Kingdom
600 Ω	600 Ω	USA, Argentina, Armenia, Belarus, Canada, Chile, Colombia, Czech Republic, Ecuador, El Salvador, Georgia, Hong Kong, India, Indonesia, Jordan, Korea, Kuwait, Malaysia, Mexico, Pakistan, Paraguay, Peru, Philippines, Poland, Qatar, Saudi Arabia, Singapore, South Korea, Taiwan, Thailand, Ukraine, UAE, Uruguay, and Venezuela.
600 Ω + 1.0 μF	600 Ω + 1.0 μF	Japan and PBX
900 Ω	900 Ω	Brazil
900 Ω + 2.16 μF	800 Ω // (0.05 μF + 100 Ω)	Telcordia GR-57-CORE Non-Loaded Loop

Table 15 - Supported AC Source Impedances
Notes:

1. [Table 15](#) provides suggested AC source impedances for the listed countries and are believed to be accurate as of the date of publication of this document. However, standards can and do change from time to time or new ones may be introduced. Some countries may support more than one standard AC source impedance. Customers are responsible for using the appropriate AC FXS Profiles for their applications.
2. VP Profile Wizard makes it easy to add additional countries as long as they are based on the supported impedances.
3. The standard files provided with VP Profile Wizard are for FXS interfaces with two 7-ohm PTC's in series with Tip and Ring. Please contact Microsemi CMPG Customer Applications if alternate series resistor or PTC resistance values are planned.
4. Narrowband and Wideband versions of these Profiles are available.

[Table 16](#) below lists the VP-API-II functions which use values that are defined in the AC FXS Profile.

Function Name	Description
VpInitDevice()	Resets and initializes device with parameters defined in Device Profile and optionally configures all lines on the device with AC, DC, and Ringing parameters.
VpInitLine()	Resets and initializes line with AC, DC, and Ringing parameters.
VpConfigLine()	Configures line with AC, DC, and Ringing parameters. Similar to VpInitLine() but line is not reset. Values not provided in function call result in line retaining previously set parameters.
VpCalLine()	This function may need to be called under some circumstances following the functions listed above. Refer to the ZL880 VP-API-II Reference Guide for more details.

Table 16 - VP-API-II Functions Using AC FXS Profile

10.5 DC Profile

DC Profiles are used to define the feed and loop supervision conditions of the line. An example DC Profile for the ZL88801 device using VP Profile Wizard is shown in Figure 47.

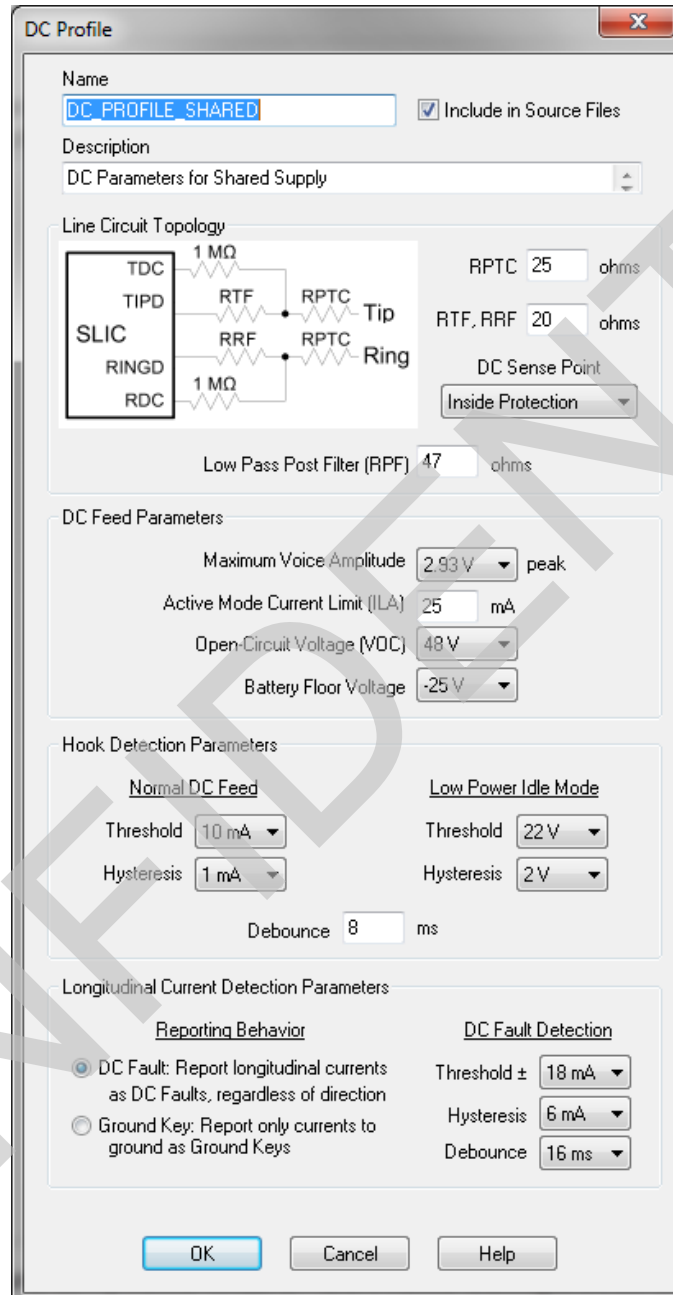


Figure 47 - Profile Wizard - DC Profile Configuration Example

[Table 17](#) lists the *VP-API-II* functions which use values that are defined in the *DC Profile*.

Function Name	Description
VpInitDevice()	Resets and initializes device with parameters defined in <i>Device Profile</i> and optionally configures all lines on the device with AC, DC, and Ringing parameters.
VpInitLine()	Resets and initializes line with AC, DC, and Ringing parameters.
VpConfigLine()	Configures line with AC, DC, and Ringing parameters. Similar to VpInitLine() but line is not reset. Values not provided in function call result in line retaining previously set parameters.
VpCalLine()	This function may need to be called under some circumstances following the functions listed above. Refer to the <i>ZL880 VP-API-II Reference Guide</i> for more details.

Table 17 - VP-API-II Functions For DC Feed and Hook Detection Configuration

10.6 Ringing Profile

The *Ringing Profile* is used to define the type of ringing, ringing frequency, amplitude, offset, ring trip threshold, and ringing current limit. The *Ringing Profile* for the ZL88801 using *VP Profile Wizard* is shown in [Figure 48](#).

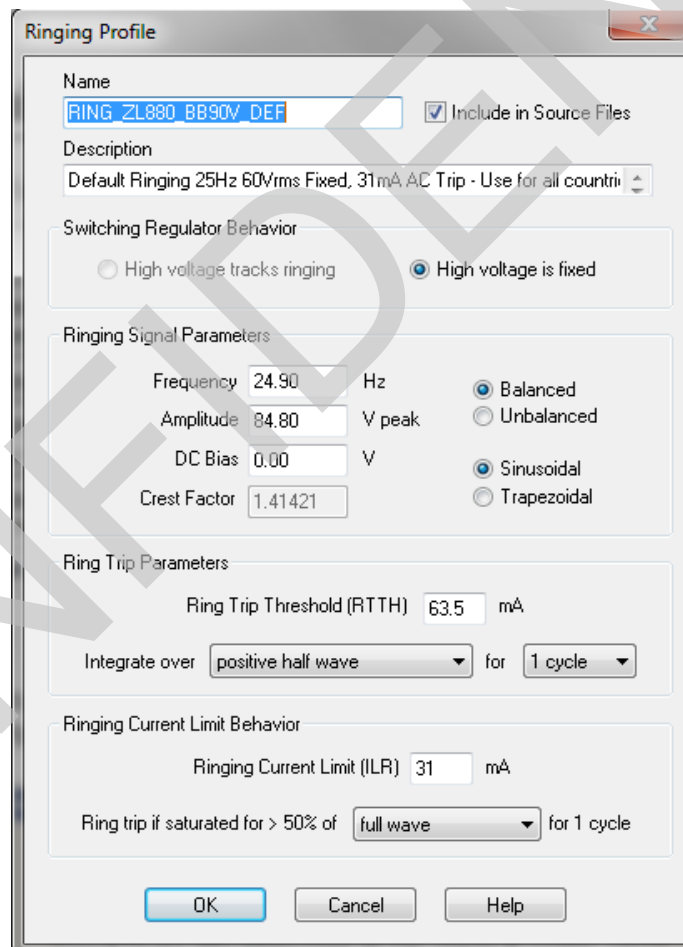


Figure 48 - Profile Wizard - Ringing Profile Configuration Example

[Table 18](#) lists the *VP-API-II* functions which use values that are defined in the *Ringing Profile.Tone Profile*

Function Name	Description
VpInitDevice ()	Resets and initializes device with parameters defined in <i>Device Profile</i> and optionally configures all lines on the device with AC, DC, and Ringing parameters.
VpInitLine ()	Resets and initializes line with AC, DC, and Ringing parameters.
VpConfigLine ()	Configures line with AC, DC, and Ringing parameters. Similar to VpInitLine () but line is not reset. Values not provided in function call result in line retaining previously set parameters.
VpCalLine ()	This function may need to be called under some circumstances following the functions listed above. Refer to the <i>ZL880 VP-API-II Reference Guide</i> for more details.

Table 18 - VP-API-II Functions For Ringing and Ring Trip Definition

10.7 Tone Profile

Tone Profiles provide the capability to program up to four simultaneous tones on the line. An example Tone Profile is shown in [Figure 49](#).

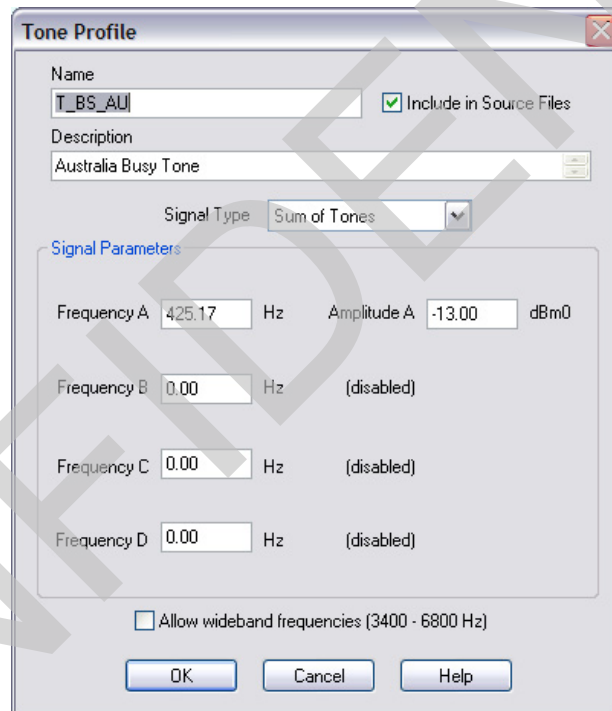


Figure 49 - Profile Wizard - Tone Profile Configuration

[Table 19](#) lists the *VP-API-II* function which uses values that are defined in the *Tone Profile*.

Function Name	Description
VpSetLineTone ()	Starts a tone on the line. The tone can be cadenced or “always on”.

Table 19 - VP-API-II Function Using Tone Profile

10.8 Tone Cadence Profile

VP-API-II Tone Cadencing is a highly flexible set of operators the user selects to implement any country-specific ringing or tone cadence requirements including Special Information Tones (SIT) and howler tones. [Figure 50](#) shows how to define cadences for call progress tones with VP Profile Wizard.

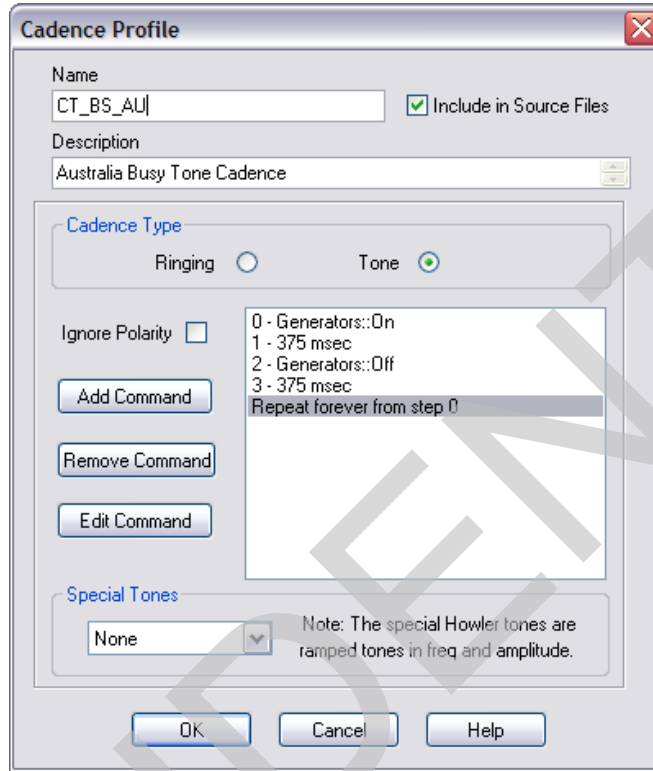


Figure 50 - Profile Wizard - Tone Cadence Profile Example

The VP-API-II Cadencer supports the following operations:

1. Time -- Delays (in a non-blocking fashion) program execution.
2. Generator Control -- Enable/Disable selection on a per-generator basis.
3. Branch -- Forces the cadencing to return to a previous step with "repeat" for *n* number of times. If *n* == 0, repeat forever.
4. Line State -- Sets line to specific VP-API-II Line State.

[Table 20](#) lists the VP-API-II function which uses values that are defined in the Tone Cadence Profile.

Function Name	Description
VpSetLineTone ()	Provides tone cadencing for up to four tones. Also supports country-specific howler tone cadencing (AUS, UK, NTT) with ramp frequency and amplitude.

Table 20 - VP-API-II Function For Tone Cadencing

10.9 Ringing Cadence Profile

VP-API-II ringing cadencing is a flexible set of operators the user selects to implement any country-specific ringing cadence. [Figure 51](#) shows how to define cadences for ringing generation with *VP Profile Wizard*. Note that events that are associated with Type 1 (on-hook) Caller ID ringing are included by this Profile.

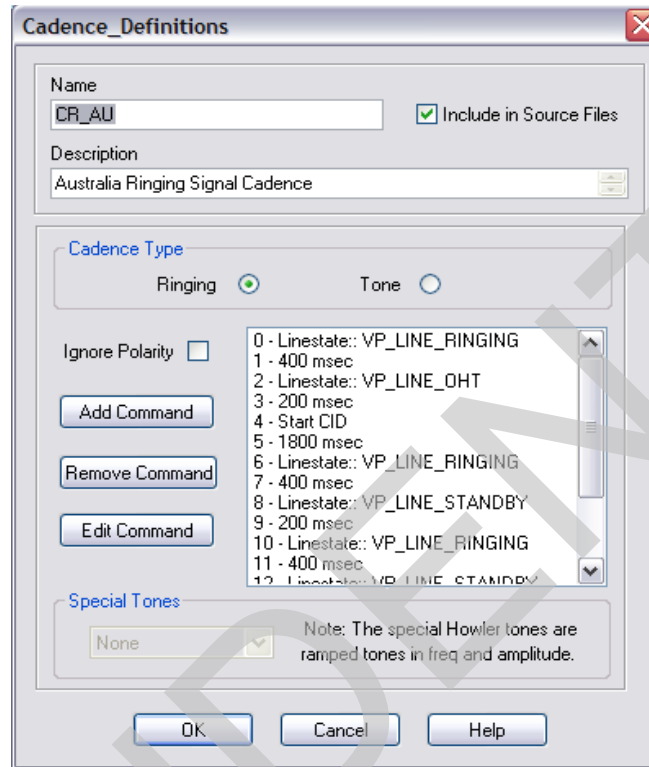


Figure 51 - Profile Wizard - Ringing Cadence Profile Example

The VP-API-II Cadencer supports the following operations:

1. Time -- Delays (in a non-blocking fashion) program execution.
2. Generator Control -- Enable/Disable selection on a per-generator basis.
3. Branch -- Forces the cadencing to return to a previous step with "repeat" for *n* number of times. If *n* == 0, repeat forever.
4. Line State -- Sets line to specific VP-API-II line state.
5. Send CID -- Starts Caller ID (CID) on the line while continuing to run cadence. Used for Type 1 Caller ID when CID occurs after first regular ringing cycle in order to achieve a precise delay between the first and second rings.
6. Wait On Caller ID -- Starts Caller ID on the line and suspends currently running cadence. Used for Type 1 Caller ID when CID occurs prior to the first regular ringing cycle.

[Table 21](#) lists the VP-API-II functions which use values that are defined in the *Ringing Cadence Profile*.

Function Name	Description
VpSetLineState()	VP_LINE_RINGING and VP_LINE_RINGING_POLREV for Ringing Cadence.
VpInitRing()	User function to provide Ringing Cadence. Also allows use selection of <i>Caller ID Profile</i> associated with ringing.

Table 21 - VP-API-II Functions For Ringing Cadencing

10.10 Caller ID Profile

The Caller ID block uses Generators C and D to generate phase-continuous 1200 baud FSK tones for on- or off-hook information such as Calling Line ID (or Caller ID) and Visual Message Waiting Indication (VMWI). The duration of each (bit) tone is fixed at 0.833 ms (1200 baud).

Bell 202 tone frequencies are used in the North American and some international markets, and the *ITU-T Recommendation V.23* tone frequencies are used in most of Europe and other international markets. The signal generator amplitude may need to be adjusted depending on the programmed loss plan. Data transmission levels are normally specified as -13.5 dBm +/-1.5 dB.

Exact preamble and mark sequences are generated by adjusting the framing mode and sending the appropriate number of characters. The *VP-API-II* abstracts this into a simple driver level interface. *VP Profile Wizard* enables the user to select the Caller ID parameters and build them into the *Caller ID Profile*, which generates the necessary coefficients and instructions for the *VP-API-II*. Note that the signal level in the example below is -7.5 dBm0, which corresponds to a transmitted signal of -13.5 dBm0 to the line due to the 6 dB D/A loss in the default *AC Profile*.

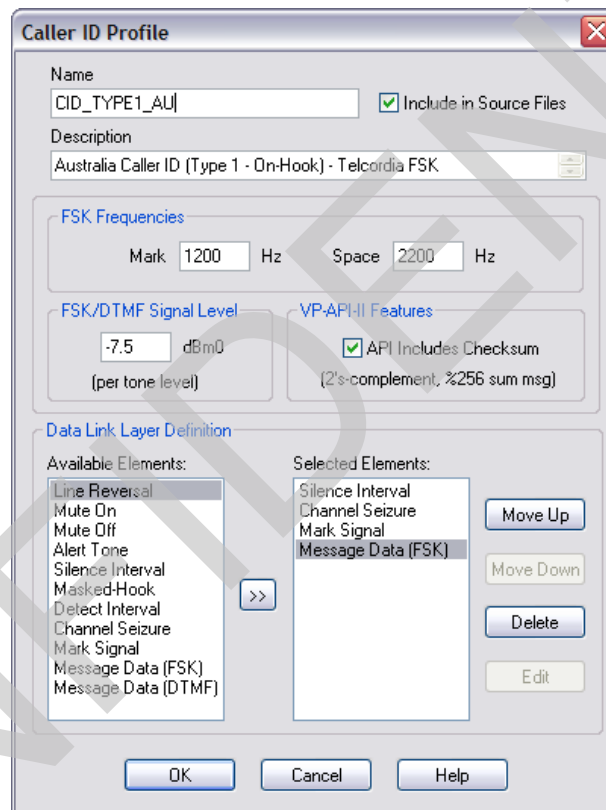


Figure 52 - Profile Wizard - Type 1 Caller ID Profile Example

[Table 22](#) lists the *VP-API-II* functions which use values that are defined in the *Caller ID Profile*.

Function Name	Description
VpInitRing()	User function to provide <i>Caller ID Profile</i> associated with ringing.
VpSendCid()	Configures and starts Caller ID immediately. Used for Type 2 Caller ID.
VpInitCid()	Input for Caller ID Message Data up to 32 bytes.
VpContinueCid()	Input for Caller ID Message Data up to 16 bytes. Called after VpInitCid() or VpSendCid() when event VP_LINE_EVID_CID_DATA is generated.

Table 22 - VP-API-II Functions For Caller ID

10.11 Metering Profile

The *Metering Profile* allows the user to define the pulse metering frequency (12 or 16 kHz), peak current, and voltage limit. [Figure 53](#) shows an example screen shot of the *Metering Profile* definition in *VP Profile Wizard*.

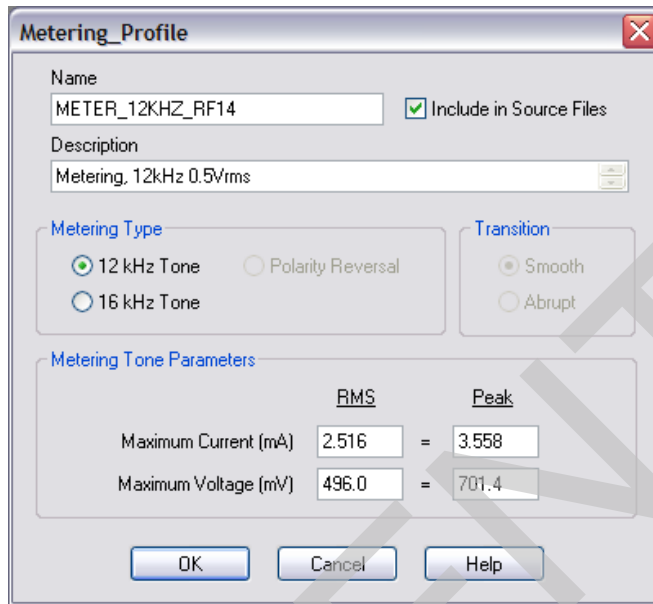


Figure 53 - Profile Wizard - Metering Profile Example

[Table 23](#) lists the *VP-API-II* functions which use values that are defined in the *Metering Profile*.

Function Name	Description
VpInitMeter()	Configures the metering signal generator of an individual line.
VpStartMeter()	Starts metering pulses.

Table 23 - VP-API-II Functions for Metering

11.0 Package Outline

The package outline and recommended land pattern of the ZL88801 Dual Channel Shared Battery Wideband VoicePort device are described in this section.

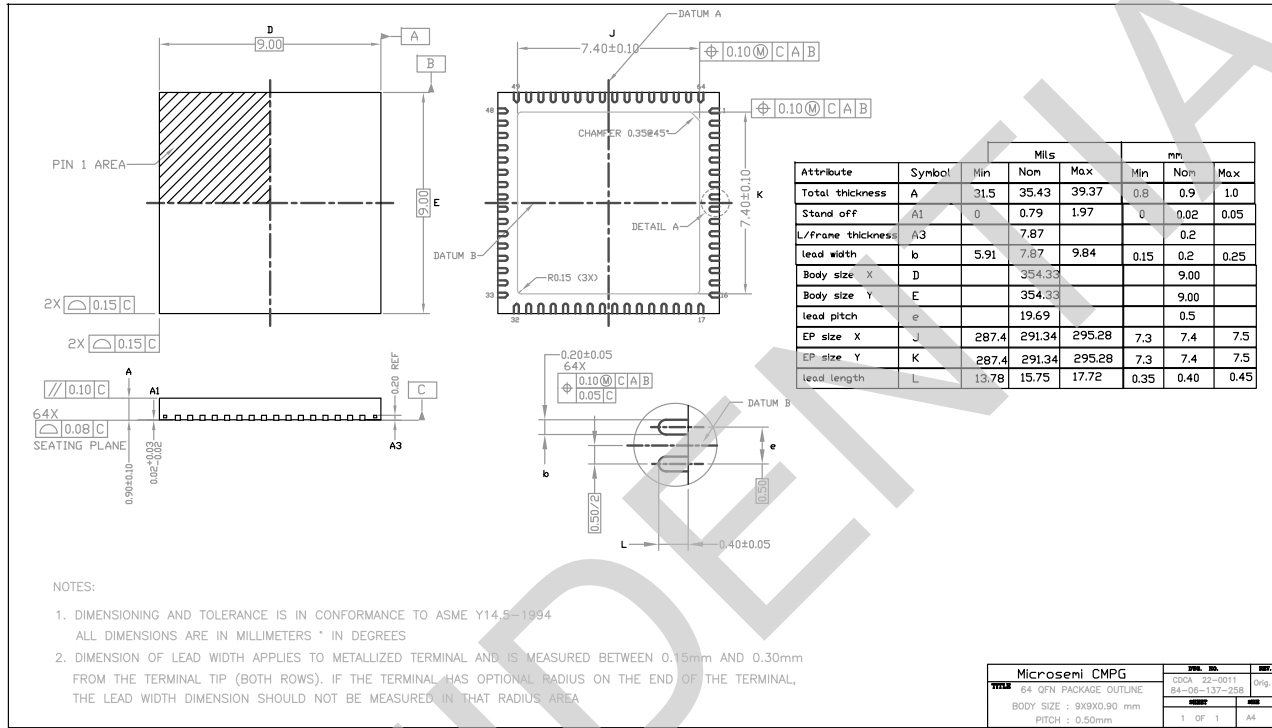


Figure 54 - ZL88801 (QFN-64) Package Drawing

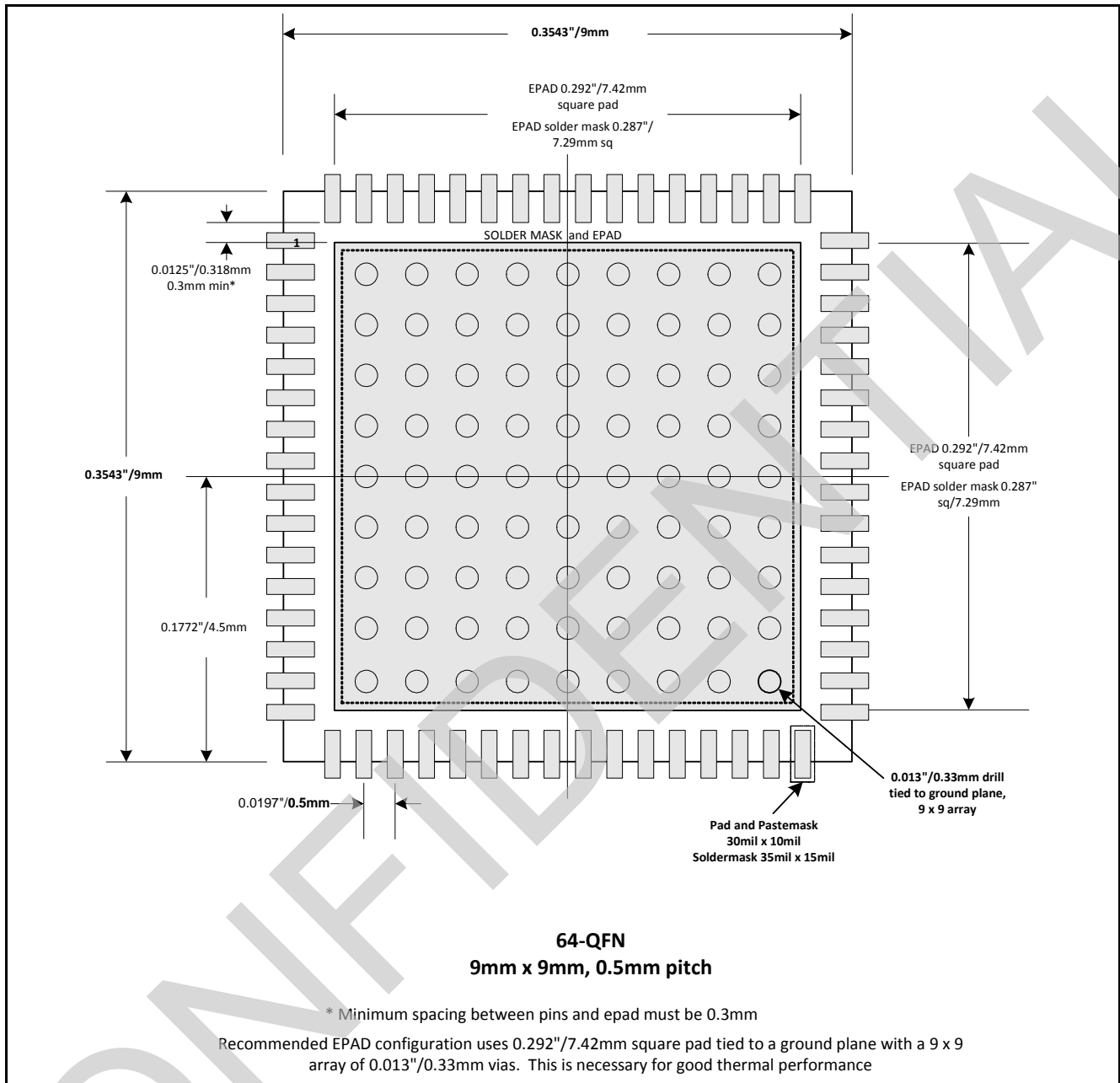


Figure 55 - Recommended Land Pattern (QFN-64) – Top View

12.0 Related Collateral

12.1 Documentation

- **ZL880 VP-API-II Reference Guide** – Document ID#: 143271
- **VeriVoice Line Test API (LT-API) User's Guide** – Document ID#: 081470
- **VeriVoice Manufacturing Test Package Reference Guide** – Document ID#: 141005
- **ZL880 Protection Schemes Application Note** – Document ID#: 146139
- **ZLR88821L Line Module Reference Design User Guide** – Document ID#: 146342
- **ZLR88822L Line Module Reference Design User Guide** – Document ID#: 147606
- **ZLR88842L Line Module Reference Design User Guide** – Document ID#: Reference 147606

12.2 Development Hardware

- **SM2 Evaluation Module - OPN: ZLR88821L**
 - The *ZLR88821L Evaluation Module* features one *ZL88801 Dual Channel VoicePort* device and one STB switching supply capable of generating up to 85- V_{PK} ringing and 3 REN drive capability. This module plugs into the *SM2* receptacle on the *ZTAP* platform.
- **SM2 Evaluation Module - OPN: ZLR88822L**
 - The *ZLR88822L Evaluation Module* features one *ZL88801 Dual Channel VoicePort* device and one BBABS switching supply capable of generating up to 70.7- V_{PK} ringing and 5 REN drive capability. This module plugs into the *SM2* receptacle on the *ZTAP* platform.
- **Broadcom Evaluation Module - OPN: ZLR88842L**
 - The *ZLR88821L Evaluation Module* features one *ZL88801 Dual Channel VoicePort* device and one *Ve8901 FXO Chipset*. The *Evaluation Module* features one BBABS switching supply capable of generating up to 70.7- V_{PK} ringing and 5 REN drive capability. This module plugs into the into the *Broadcom® ADSL2+/VDSL2 Reference Platforms*.

12.3 Development Software

- **VoicePath API-II - OPN: Le71SK0002**
 - The *VP-API-II* is a set of C source used by the host application to interface to the *ZL880 Series* and other Microsemi voice products. A signed Software License Agreement (SLA) is required.
- **VoicePath API-II Lite - OPN: Le71SDKAPIL**
 - The *VP-API-II Lite* is identical to *VP-API-II*, with reduced functionality. *VP-API-II Lite* does not support tone or ringing cadencing, Caller ID, or Metering. This software is available without an SLA.
- **VoicePath Profile Wizard - OPN: Le71SDKPRO**
 - The *VP Profile Wizard* is a *Microsoft Windows* GUI application that aids in the organization and creation of country *Profiles* used in the *VP-API-II* into a single project file.

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