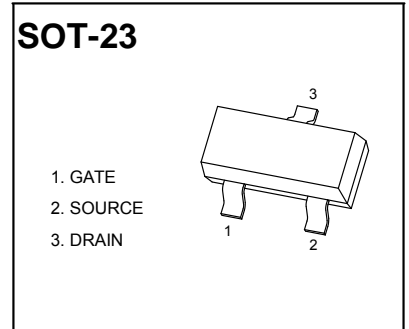


**SOT-23 Plastic-Encapsulate MOSFETS**
**-12V P-Channel MOSFET**

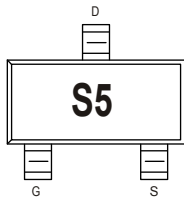
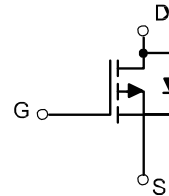
$V_{(BR)DSS}$	$R_{DS(on)Typ}$	$I_D Max$
-12V	37mΩ@ -4.5V	-4.2A
	40mΩ@ -3.3V	


**Features**

Trench FET Power MOSFET

**APPLICATION**

- Load Switch for Portable Devices
- DC/DC Converter

**MARKING**

**Equivalent circuit**

**PACKAGE SPECIFICATIONS**

Package	Reel Size	Reel DIA. (mm)	Q'TY/Reel (pcs)	Box Size (mm)	QTY/Box (pcs)	Carton Size (mm)	Q'TY/Carton (pcs)
SOT-23	7'	330	3000	203×203×195	45000	438×438×220	180000

**Maximum Ratings and Thermal Characteristics (TA = 25°C unless otherwise noted)**

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	$V_{DS}$	-20	V	
Gate-Source Voltage	$V_{GS}$	±10		
Continuous Drain Current	$I_D$	$T_A = 25^\circ C$	-4.2	A
		$T_A = 70^\circ C$	-2.8	
Pulsed Drain Current <sup>1)</sup>	$I_{DM}$	-16.8	A	
Maximum Power Dissipation <sup>2)</sup>	$P_D$	$T_A = 25^\circ C$	1.25	W
		$T_A = 70^\circ C$	1.0	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-50 to 150	°C	
Junction-to-Ambient Thermal Resistance (PCB mounted) <sup>2)</sup>	$R_{thJA}$	100	°C/W	

**Notes**

- <sup>1)</sup> Pulse width limited by maximum junction temperature.  
<sup>2)</sup> Surface Mounted on FR4 Board,  $t \leq 5$  sec.

The above data are for reference only.



**MOSFET ELECTRICAL CHARACTERISTICS**

$T_a=25\text{ }^\circ\text{C}$  unless otherwise specified

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Static</b>						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-20			V
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-0.4	-0.6	-1	
Gate-source leakage	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 10V$			$\pm 100$	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = -20V, V_{GS} = 0V$			-1	$\mu A$
Drain-source on-state resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = -4.5V, I_D = -4A$		37	48	m $\Omega$
		$V_{GS} = -3.3V, I_D = -3.0A$		40	55	
		$V_{GS} = -2.5V, I_D = -2.0A$		45	60	
Forward transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = -5V, I_D = -2.8A$	6.5			S
<b>Dynamic<sup>b</sup></b>						
Input capacitance	$C_{iss}$	$V_{DS} = -10V, V_{GS} = 0V, f = 1MHz$		760		pF
Output capacitance	$C_{oss}$			94		
Reverse transfer capacitance	$C_{rss}$			76		
Total gate charge	$Q_g$	$V_{DS} = -10V, V_{GS} = -4.5V, I_D = -3A$		7.8		nC
Gate-source charge	$Q_{gs}$	$V_{DS} = -10V, V_{GS} = -4.5V, I_D = -3A$		0.9		
Gate-drain charge	$Q_{gd}$			1.8		
Turn-on delay time	$t_{d(on)}$	$V_{DD} = -10V, R_L = 1.2\Omega,$ $I_D = -2A,$ $V_{GEN} = -4.5V, R_g = 3.3\Omega$		5.5		ns
Rise time	$t_r$			3.9		
Turn-off delay time	$t_{d(off)}$			11.3		
Fall time	$t_f$			36		
<b>Drain-source body diode characteristics</b>						
Continuous source-drain diode current	$I_S$	$T_C = 25^\circ C$			-2.0	A
Body diode voltage	$V_{SD}$	$I_S = -4A$		-0.87	-1.2	V

a) Pulse test: pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$

b) Guaranteed by design, not subject to production testing

Typical Characteristics

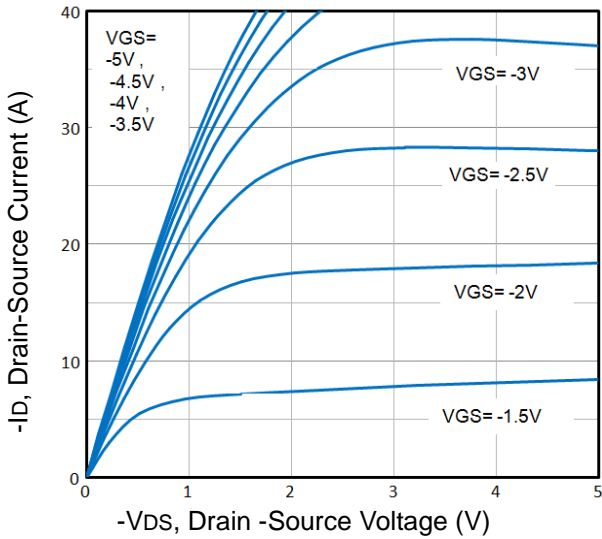


Fig1. Typical Output Characteristics

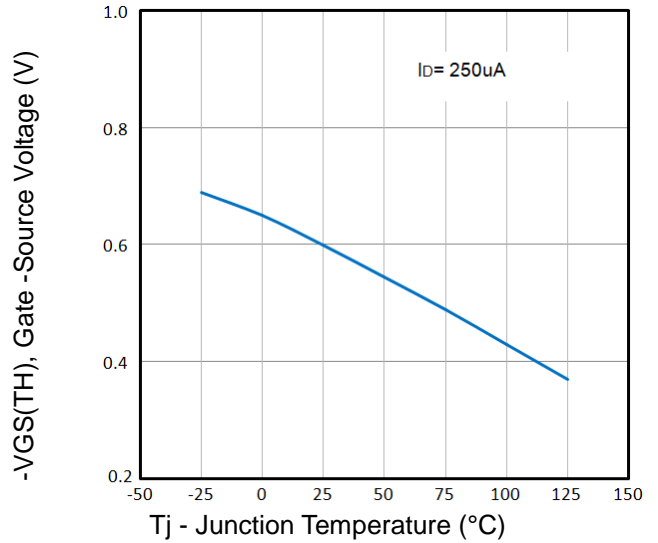


Fig2. Normalized Threshold Voltage Vs. Temperature

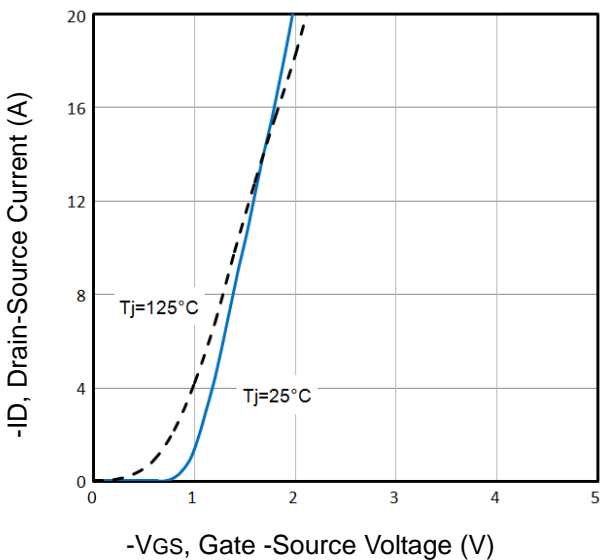


Fig3. Typical Transfer Characteristics

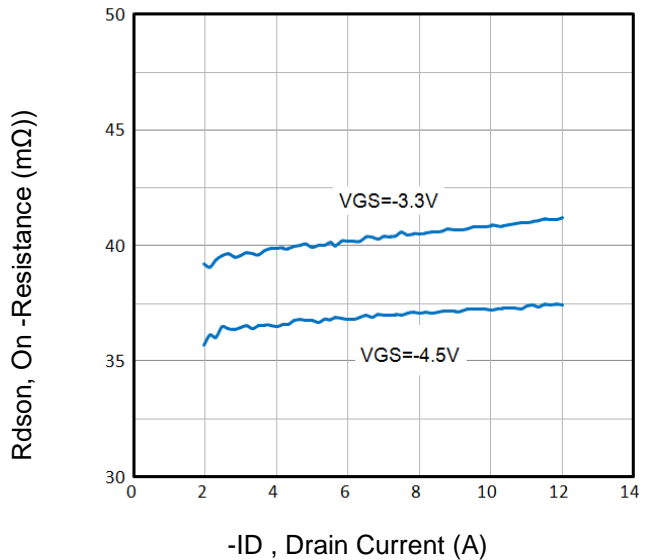


Fig4. On-Resistance vs. Drain Current and Gate Voltage

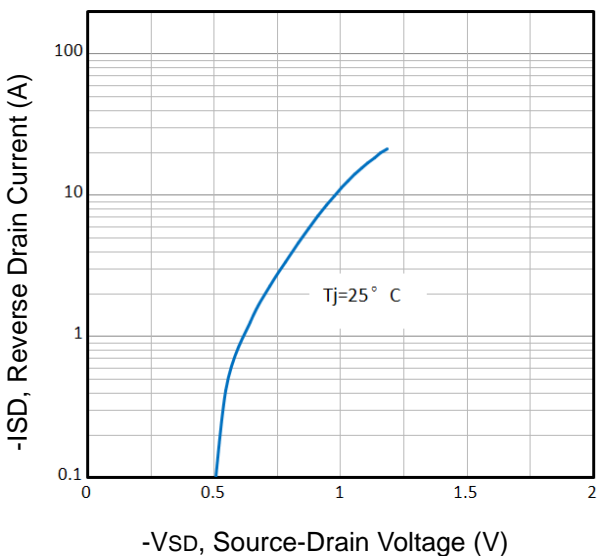


Fig5. Typical Source-Drain Diode Forward Voltage

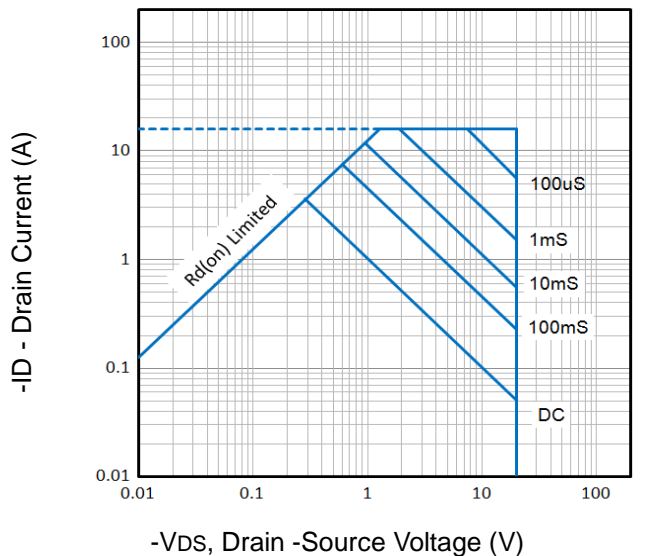


Fig6. Maximum Safe Operating Area

Typical Characteristics

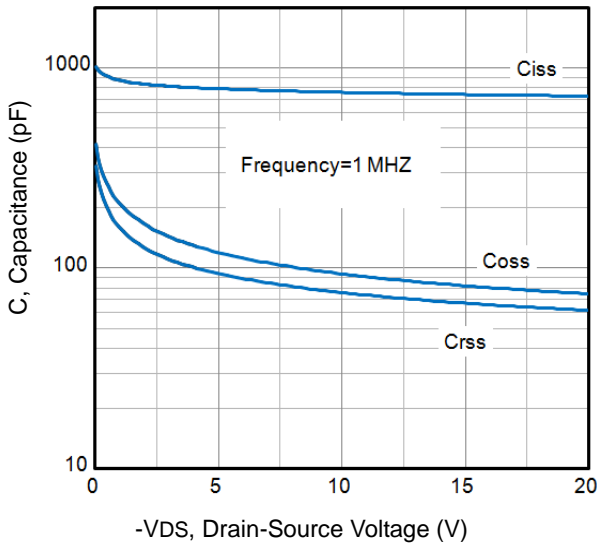


Fig7. Typical Capacitance Vs. Drain-Source Voltage

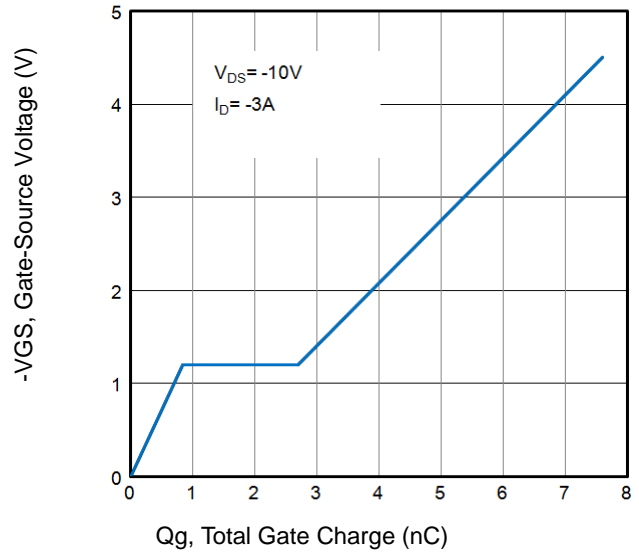


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

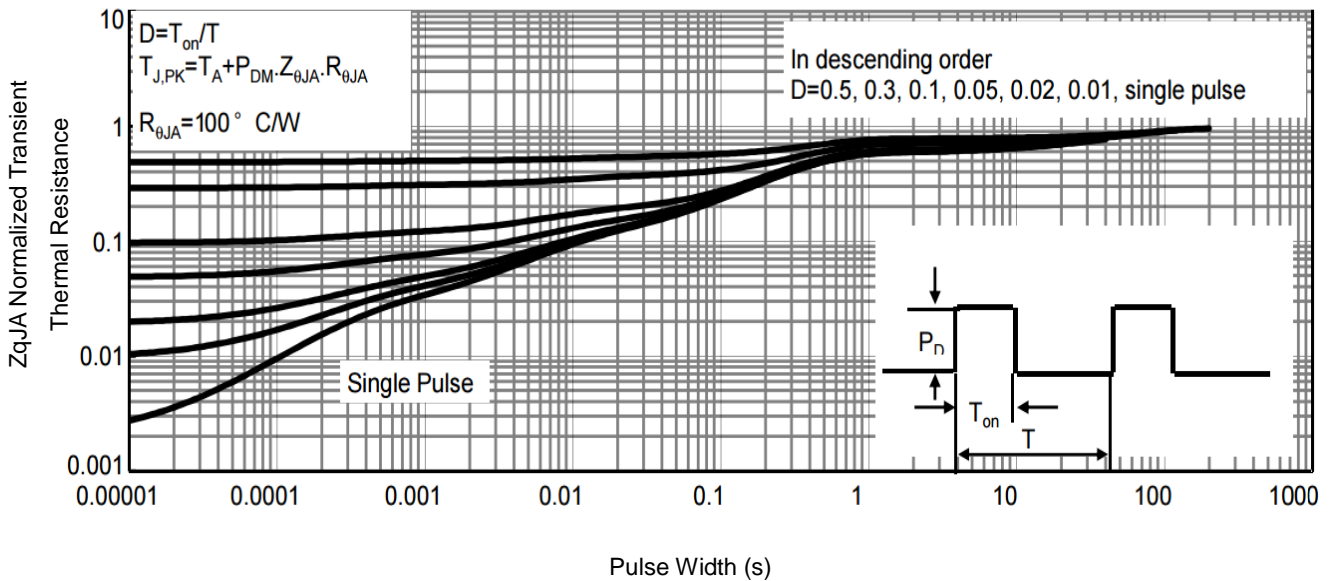


Fig9. Normalized Maximum Transient Thermal Impedance

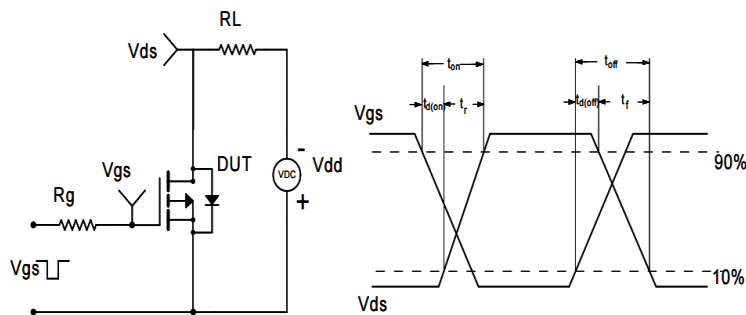
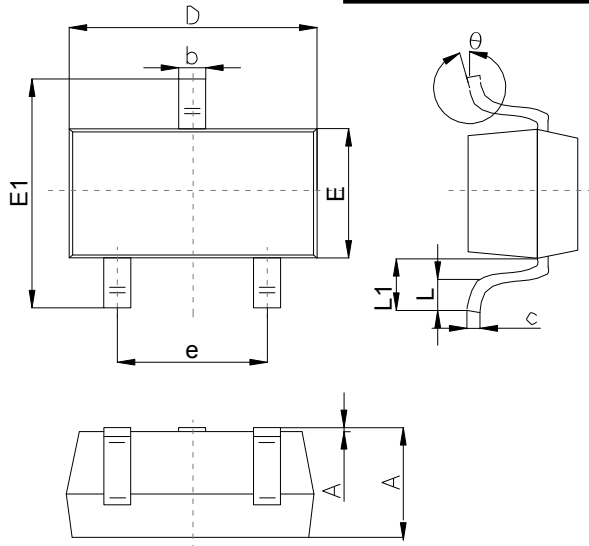


Fig10. Switching Time Test Circuit and waveforms

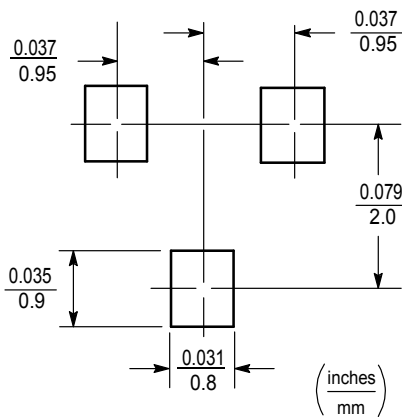
**Outlitne Drawing**

**SOT-23 Package Outline Dimensions**



Symbol	Dimensions In Millimeters		
	Min	Typ	Max
A	1.00		1.40
A1			0.10
b	0.35		0.50
c	0.10		0.20
D	2.70	2.90	3.10
E	1.40		1.60
E1	2.4		2.80
e		1.90	
L	0.10		0.30
L1	0.4		
θ	0°		10°

**Suggested Pad Layout**



Note:  
 1. Controlling dimension:in/millimeters. 2.General tolerance: ±0.05mm.  
 3.The pad layout is for reference purposes only.

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