



# Embedded LPDDR2 SDRAM

**EDB8164B4PR, EDB8164B4PK, EDB8164B4PT, EDDBA164B2PR**

## Features

- Ultra-low-voltage core and I/O power supplies
- Frequency range
  - 533 MHz (data rate: 1066 Mb/s/pin)
- 4n prefetch DDR architecture
- 8 internal banks for concurrent operation
- Multiplexed, double data rate, command/address inputs; commands entered on each CK\_t/CK\_c edge
- Bidirectional/differential data strobe per byte of data (DQS\_t/DQS\_c)
- Programmable READ and WRITE latencies (RL/WL)
- Burst length: 4, 8, and 16
- Per-bank refresh for concurrent operation
- Auto temperature-compensated self refresh (ATCSR) by built-in temperature sensor
- Partial-array self refresh (PASR)
- Deep power-down mode (DPD)
- Selectable output drive strength (DS)
- Clock-stop capability
- Lead-free (RoHS-compliant) and halogen-free packaging

**Table 1: Key Timing Parameters**

Speed Grade	Clock Rate (MHz)	Data Rate (Mb/s/pin)	RL	WL
1D	533	1066	8	4

## Options

- Density/Page Size
  - 8Gb/2-CS – dual die 81
  - 16Gb/4-CS – quad die A1
- Organization
  - x64 64
- V<sub>DD1</sub>/V<sub>DD2</sub>/V<sub>DDQ</sub>: 1.8V/1.2V/1.2V B
- Revision
  - Dual die 2
  - Quad die 4
- FBGA “green” package
  - 12mm x 12mm x 0.8mm, 216-ball PoP FBGA package, dual die PR
  - 12mm x 12mm x 0.8mm, 216-ball PoP FBGA package, dual die PT
  - 12mm x 12mm x 1.0mm, 216-ball PoP FBGA package, quad die PR
  - 14mm x 14mm x 0.7mm, 220-ball PoP FBGA package, dual die PK
- Timing – cycle time
  - 1.875ns @ RL = 8 -1D
- Special options
  - Non-Automotive blank
- Operating temperature range
  - From –30°C to +85°C blank
  - From –40°C to +85°C IT
  - From –40°C to +105°C AT

## Marking

**Table 2: S4 Configuration Addressing**

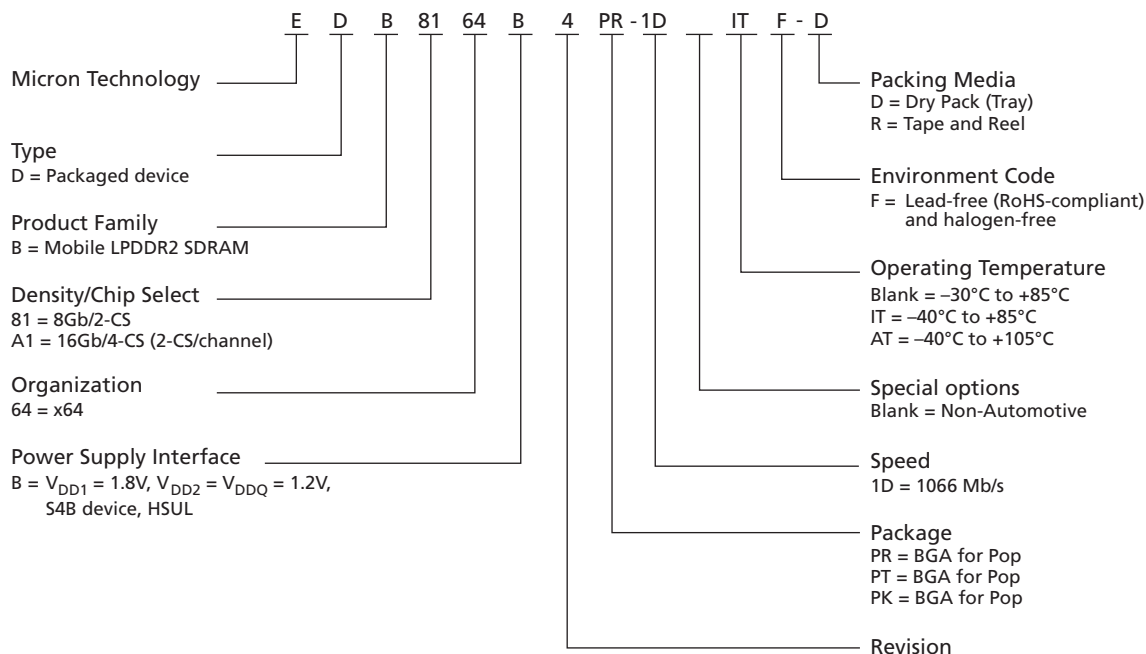
Architecture	128 Meg x 64	256 Meg x 64
Die configuration	16 Meg x 32 x 8 banks x 2 channel	32 Meg x 32 x 8 banks x 2 channel
Row addressing	16K A[13:0]	16K A[13:0]
Column addressing	1K A[9:0]	1K A[9:0]
Number of die	2	4
Die per rank	1	2
Ranks per channel	1	2

Note: 1. A channel is a complete LPDRAM interface, including command/address and data pins.



# 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Features

**Figure 1: LPDDR2 Part Numbering**



## FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at [www.micron.com/decoder](http://www.micron.com/decoder).

**Table 3: Package Codes and Descriptions**

Package Code	Ball Count	# Ranks	# Channels	Size (mm)	Die per Package	Solder Ball Composition
PR	216	1	2	12mm x 12mm x 0.80mm, 0.40 pitch	DDP	SAC302
PT	216	1	2	12mm x 12mm x 0.80mm, 0.40 pitch	DDP	SAC302
PR	216	2	2	12mm x 12mm x 1.00mm, 0.40 pitch	QDP	SAC302
PK	220	1	2	14mm x 14mm x 0.70mm, 0.50 pitch	DDP	SAC302

- Notes: 1. DDP = dual-die package, QDP = quad-die package  
 2. Solder ball material: SAC302 (96.8% Sn, 3% Ag, 0.2% Cu).



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## LPDDR2 Array Configuration

The 4Gb Mobile Low-Power DDR2 SDRAM (LPDDR2) is a high-speed CMOS, dynamic random-access memory containing 4,294,967,296-bits. The device is internally configured as an eight-bank DRAM. Each of the x16's 536,870,912-bit banks is organized as 16,384 rows by 2048 columns by 16 bits. Each of the x32's 536,870,912-bit banks is organized as 16,384 rows by 1024 columns by 32 bits.

## General Notes

Throughout the data sheet, figures and text refer to DQs as "DQ." DQ should be interpreted as any or all DQ collectively, unless specifically stated otherwise.

"DQS" and "CK" should be interpreted as DQS\_t, DQS\_c and CK\_t, CK\_c respectively, unless specifically stated otherwise. "BA" includes all BA pins used for a given density.

Complete functionality may be described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any specific requirement takes precedence over a general statement.

Any functionality not specifically stated herein is considered undefined, illegal, is not supported, and will result in unknown operation.



## I<sub>DD</sub> Specifications

**Table 4: I<sub>DD</sub> Specifications – Dual Die, Dual Channel**
 $V_{DD2}, V_{DDQ} = 1.14\text{--}1.30\text{V}; V_{DD1} = 1.70\text{--}1.95\text{V}; T_C = -40^\circ\text{C to } +105^\circ\text{C}$ 

Symbol	Supply	Speed		Unit	Parameter/Condition
		1066	800		
I <sub>DD01</sub>	V <sub>DD1</sub>	16	16	mA	All devices in operating one bank active-pre-charge Conditions for operating devices are: t <sub>CK</sub> = t <sub>CK</sub> (avg) MIN; t <sub>RC</sub> = t <sub>RC</sub> (MIN); CKE is HIGH; CS <sub>n</sub> is HIGH between valid commands; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I <sub>DD02</sub>	V <sub>DD2</sub> , V <sub>DDQ</sub>	100	90		
I <sub>DD0,in</sub>	V <sub>DD2</sub> , V <sub>DDQ</sub>	1.2	1.2		
I <sub>DD2P1</sub>	V <sub>DD1</sub>	0.8	0.8	mA	All devices in idle power-down standby current t <sub>CK</sub> = t <sub>CK</sub> (avg) MIN; CKE is LOW; CS <sub>n</sub> is HIGH; All banks are idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I <sub>DD2P2</sub>	V <sub>DD2</sub> , V <sub>DDQ</sub>	1.8	1.8		
I <sub>DD2P,in</sub>	V <sub>DD2</sub> , V <sub>DDQ</sub>	0.2	0.2		
I <sub>DD2PS1</sub>	V <sub>DD1</sub>	0.8	0.8	mA	All devices in idle power-down standby current with clock stop CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is LOW; CS <sub>n</sub> is HIGH; All banks are idle; CA bus inputs are STABLE; Data bus inputs are STABLE
I <sub>DD2PS2</sub>	V <sub>DD2</sub> , V <sub>DDQ</sub>	1.8	1.8		
I <sub>DD2PS,in</sub>	V <sub>DD2</sub> , V <sub>DDQ</sub>	0.2	0.2		
I <sub>DD2N1</sub>	V <sub>DD1</sub>	1.2	1.2	mA	All devices in idle non power-down standby current. t <sub>CK</sub> = t <sub>CK</sub> (avg) MIN; CKE is HIGH; CS <sub>n</sub> is HIGH; All banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I <sub>DD2N2</sub>	V <sub>DD2</sub> , V <sub>DDQ</sub>	26	22		
I <sub>DD2N,in</sub>	V <sub>DD2</sub> , V <sub>DDQ</sub>	1.2	1.2		
I <sub>DD2NS1</sub>	V <sub>DD1</sub>	1.2	1.2	mA	All devices in idle non power-down standby current with clock stop CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is HIGH; CS <sub>n</sub> is HIGH; All banks are idle; CA bus inputs are STABLE; Data bus inputs are STABLE
I <sub>DD2NS2</sub>	V <sub>DD2</sub> , V <sub>DDQ</sub>	12	12		
I <sub>DD2NS,in</sub>	V <sub>DD2</sub> , V <sub>DDQ</sub>	1.2	1.2		
I <sub>DD3P1</sub>	V <sub>DD1</sub>	1.6	1.2	mA	All devices in active power-down standby current t <sub>CK</sub> = t <sub>CK</sub> (avg) MIN; CKE is LOW; CS <sub>n</sub> is HIGH; One bank is active; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I <sub>DD3P2</sub>	V <sub>DD2</sub> , V <sub>DDQ</sub>	10	10		
I <sub>DD3P,in</sub>	V <sub>DD2</sub> , V <sub>DDQ</sub>	0.2	0.2		



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM I<sub>DD</sub> Specifications

**Table 4: I<sub>DD</sub> Specifications – Dual Die, Dual Channel (Continued)**
 $V_{DD2}, V_{DDQ} = 1.14\text{--}1.30\text{V}; V_{DD1} = 1.70\text{--}1.95\text{V}; T_C = -40^\circ\text{C to } +105^\circ\text{C}$ 

Symbol	Supply	Speed		Unit	Parameter/Condition
		1066	800		
I <sub>DD3PS1</sub>	V <sub>DD1</sub>	1.6	1.6	mA	All devices in active power-down standby current with clock stop CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is LOW; CS <sub>n</sub> is HIGH; One bank is active; CA bus inputs are STABLE; Data bus inputs are STABLE
I <sub>DD3PS2</sub>	V <sub>DD2</sub> , V <sub>DDQ</sub>	10	10		
I <sub>DD3PS,in</sub>	V <sub>DD2</sub> , V <sub>DDQ</sub>	0.2	0.2		
I <sub>DD3N1</sub>	V <sub>DD1</sub>	2.4	2.4	mA	All devices in active non power-down standby current t <sup>CK</sup> = t <sup>CK</sup> (avg) MIN; CKE is HIGH; CS <sub>n</sub> is HIGH; One bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I <sub>DD3N2</sub>	V <sub>DD2</sub> , V <sub>DDQ</sub>	44	34		
I <sub>DD3N,in</sub>	V <sub>DD2</sub> , V <sub>DDQ</sub>	2.0	1.2		
I <sub>DD3NS1</sub>	V <sub>DD1</sub>	2.4	2.4	mA	All devices in active non power-down standby current with clock stop CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is HIGH; CS <sub>n</sub> is HIGH; One bank is active; CA bus inputs are STABLE; Data bus inputs are STABLE
I <sub>DD3NS2</sub>	V <sub>DD2</sub> , V <sub>DDQ</sub>	24	24		
I <sub>DD3NS,in</sub>	V <sub>DD2</sub> , V <sub>DDQ</sub>	1.2	1.2		
I <sub>DD4R1</sub>	V <sub>DD1</sub>	4.0	4.0	mA	All devices in operating burst read t <sup>CK</sup> = t <sup>CK</sup> (avg) MIN; CS <sub>n</sub> is HIGH between valid commands; One bank is active; BL = 4; RL = RL (MIN); CA bus inputs are SWITCHING; 50% data change occurs at each burst transfer
I <sub>DD4R2</sub>	V <sub>DD2</sub> , V <sub>DDQ</sub>	320	260		
I <sub>DD4W1</sub>	V <sub>DD1</sub>	4.0	4.0	mA	All devices in operating burst write t <sup>CK</sup> = t <sup>CK</sup> (avg) MIN; CS <sub>n</sub> is HIGH between valid commands; One bank is active; BL = 4; WL = WL (MIN); CA bus inputs are SWITCHING; 50% data change occurs at each burst transfer
I <sub>DD4W2</sub>	V <sub>DD2</sub> , V <sub>DDQ</sub>	300	240		
I <sub>DD4W,in</sub>	V <sub>DD2</sub> , V <sub>DDQ</sub>	2.0	2.0		
I <sub>DD51</sub>	V <sub>DD1</sub>	40	40	mA	All devices in all bank auto-refresh t <sup>CK</sup> = t <sup>CK</sup> (avg) MIN; CKE is HIGH between valid commands; t <sup>RC</sup> = t <sup>RFCab</sup> (MIN); Burst refresh; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I <sub>DD52</sub>	V <sub>DD2</sub> , V <sub>DDQ</sub>	240	240		
I <sub>DD5,in</sub>	V <sub>DD2</sub> , V <sub>DDQ</sub>	1.2	1.2		
I <sub>DD5AB1</sub>	V <sub>DD1</sub>	4.0	4.0	mA	All devices in all bank auto-refresh t <sup>CK</sup> = t <sup>CK</sup> (avg) MIN; CKE is HIGH between valid commands; t <sup>RC</sup> = t <sup>REFI</sup> ; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I <sub>DD5AB2</sub>	V <sub>DD2</sub> , V <sub>DDQ</sub>	32	30		
I <sub>DD5AB,in</sub>	V <sub>DD2</sub> , V <sub>DDQ</sub>	1.2	1.2		



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM I<sub>DD</sub> Specifications

**Table 4: I<sub>DD</sub> Specifications – Dual Die, Dual Channel (Continued)**
 $V_{DD2}, V_{DDQ} = 1.14\text{--}1.30\text{V}; V_{DD1} = 1.70\text{--}1.95\text{V}; T_C = -40^\circ\text{C to } +105^\circ\text{C}$ 

Symbol	Supply	Speed		Unit	Parameter/Condition
		1066	800		
I <sub>DD5PB1</sub>	V <sub>DD1</sub>	4.0	4.0	mA	All devices in per bank auto-refresh t <sub>CK</sub> = t <sub>CK(avg)</sub> MIN; CKE is HIGH between valid commands; t <sub>RC</sub> = t <sub>REFIpb</sub> ; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I <sub>DD5PB2</sub>	V <sub>DD2</sub> , V <sub>DDQ</sub>	32	30		
I <sub>DD5PB,in</sub>	V <sub>DD2</sub> , V <sub>DDQ</sub>	1.2	1.2		
I <sub>DD81</sub>	V <sub>DD1</sub>	32	32	μA	All devices in deep power-down CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
I <sub>DD82</sub>	V <sub>DD2</sub> , V <sub>DDQ</sub>	12	12		
I <sub>DD8,in</sub>	V <sub>DD2</sub> , V <sub>DDQ</sub>	24	24		

- Notes:
1. Published I<sub>DD</sub> values are the maximum of the distribution of the arithmetic mean.
  2. I<sub>DD</sub> current specifications are tested after the device is properly initialized.
  3. V<sub>DD2</sub> and V<sub>DDQ</sub> are connected internally in the package.

**Table 5: I<sub>DD6</sub> Full-Array Self Refresh Current at 45°C**
 $V_{DD2}, V_{DDQ} = 1.14\text{--}1.30\text{V}; V_{DD1} = 1.70\text{--}1.95\text{V}$ 

PASR	Supply	Value	Unit	Parameters/Conditions
Full array	V <sub>DD1</sub>	400	μA	All devices in self refresh CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
	V <sub>DD2</sub>	1600		
	V <sub>DDQ</sub>	20		
1/2 array	V <sub>DD1</sub>	320		
	V <sub>DD2</sub>	1000		
	V <sub>DDQ</sub>	20		
1/4 array	V <sub>DD1</sub>	260		
	V <sub>DD2</sub>	600		
	V <sub>DDQ</sub>	20		
1/8 array	V <sub>DD1</sub>	240		
	V <sub>DD2</sub>	400		
	V <sub>DDQ</sub>	20		

- Note: 1. I<sub>DD6</sub> 45°C is the typical of the distribution of the arithmetic mean.


**Table 6: I<sub>DD6</sub> Partial-Array Self Refresh Current at 85°C**
 $V_{DD2}, V_{DDQ} = 1.14\text{--}1.30\text{V}; V_{DD1} = 1.70\text{--}1.95\text{V}$ 

PASR	Supply	Value	Unit	Parameters/Conditions
Full array	V <sub>DD1</sub>	1800	μA	All devices in self refresh CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
	V <sub>DD2</sub>	6400		
	V <sub>DDQ</sub>	24		
1/2 array	V <sub>DD1</sub>	1300		
	V <sub>DD2</sub>	4400		
	V <sub>DDQ</sub>	24		
1/4 array	V <sub>DD1</sub>	1100		
	V <sub>DD2</sub>	3400		
	V <sub>DDQ</sub>	24		
1/8 array	V <sub>DD1</sub>	1000		
	V <sub>DD2</sub>	2800		
	V <sub>DDQ</sub>	24		

Note: 1. I<sub>DD6</sub> 85°C is the maximum of the distribution of the arithmetic mean.

**Table 7: I<sub>DD6</sub> Partial-Array Self Refresh Current at 105°C**
 $V_{DD2}, V_{DDQ} = 1.14\text{--}1.30\text{V}; V_{DD1} = 1.70\text{--}1.95\text{V}$ 

PASR	Supply	Value	Unit	Parameters/Conditions
Full array	V <sub>DD1</sub>	TBD	μA	All devices in self refresh CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
	V <sub>DD2</sub>	TBD		
	V <sub>DDQ</sub>	TBD		
1/2 array	V <sub>DD1</sub>	TBD		
	V <sub>DD2</sub>	TBD		
	V <sub>DDQ</sub>	TBD		
1/4 array	V <sub>DD1</sub>	TBD		
	V <sub>DD2</sub>	TBD		
	V <sub>DDQ</sub>	TBD		
1/8 array	V <sub>DD1</sub>	TBD		
	V <sub>DD2</sub>	TBD		
	V <sub>DDQ</sub>	TBD		

Note: 1. I<sub>DD6</sub> 105°C is the typical of the distribution of the arithmetic mean.



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM I<sub>DD</sub> Specifications

**Table 8: I<sub>DD</sub> Specifications – Quad Die, Dual Channel**
 $V_{DD2}, V_{DDQ} = 1.14\text{--}1.30\text{V}; V_{DD1} = 1.70\text{--}1.95\text{V}; T_C = -40^\circ\text{C to } +105^\circ\text{C}$ 

Symbol	Supply	Speed		Unit	Parameter/Condition
		1066	800		
I <sub>DD01</sub>	V <sub>DD1</sub>	TBD	TBD	mA	All devices in operating one bank active-pre-charge Conditions for operating devices are: t <sub>CK</sub> = t <sub>CK</sub> (avg) MIN; t <sub>RC</sub> = t <sub>RC</sub> (MIN); CKE is HIGH; CS <sub>n</sub> is HIGH between valid commands; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I <sub>DD02</sub>	V <sub>DD2</sub>	TBD	TBD		
I <sub>DD0,in</sub>	V <sub>DDQ</sub>	TBD	TBD		
I <sub>DD2P1</sub>	V <sub>DD1</sub>	TBD	TBD	mA	All devices in idle power-down standby current t <sub>CK</sub> = t <sub>CK</sub> (avg) MIN; CKE is LOW; CS <sub>n</sub> is HIGH; All banks are idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I <sub>DD2P2</sub>	V <sub>DD2</sub>	TBD	TBD		
I <sub>DD2P,in</sub>	V <sub>DDQ</sub>	TBD	TBD		
I <sub>DD2PS1</sub>	V <sub>DD1</sub>	TBD	TBD	mA	All devices in idle power-down standby current with clock stop CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is LOW; CS <sub>n</sub> is HIGH; All banks are idle; CA bus inputs are STABLE; Data bus inputs are STABLE
I <sub>DD2PS2</sub>	V <sub>DD2</sub>	TBD	TBD		
I <sub>DD2PS,in</sub>	V <sub>DDQ</sub>	TBD	TBD		
I <sub>DD2N1</sub>	V <sub>DD1</sub>	TBD	TBD	mA	All devices in idle non power-down standby current. t <sub>CK</sub> = t <sub>CK</sub> (avg) MIN; CKE is HIGH; CS <sub>n</sub> is HIGH; All banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I <sub>DD2N2</sub>	V <sub>DD2</sub>	TBD	TBD		
I <sub>DD2N,in</sub>	V <sub>DDQ</sub>	TBD	TBD		
I <sub>DD2NS1</sub>	V <sub>DD1</sub>	TBD	TBD	mA	All devices in idle non power-down standby current with clock stop CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is HIGH; CS <sub>n</sub> is HIGH; All banks are idle; CA bus inputs are STABLE; Data bus inputs are STABLE
I <sub>DD2NS2</sub>	V <sub>DD2</sub>	TBD	TBD		
I <sub>DD2NS,in</sub>	V <sub>DDQ</sub>	TBD	TBD		
I <sub>DD3P1</sub>	V <sub>DD1</sub>	TBD	TBD	mA	All devices in active power-down standby current t <sub>CK</sub> = t <sub>CK</sub> (avg) MIN; CKE is LOW; CS <sub>n</sub> is HIGH; One bank is active; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I <sub>DD3P2</sub>	V <sub>DD2</sub>	TBD	TBD		
I <sub>DD3P,in</sub>	V <sub>DDQ</sub>	TBD	TBD		
I <sub>DD3PS1</sub>	V <sub>DD1</sub>	TBD	TBD	mA	All devices in active power-down standby current with clock stop CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is LOW; CS <sub>n</sub> is HIGH; One bank is active; CA bus inputs are STABLE; Data bus inputs are STABLE
I <sub>DD3PS2</sub>	V <sub>DD2</sub>	TBD	TBD		
I <sub>DD3PS,in</sub>	V <sub>DDQ</sub>	TBD	TBD		



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM I<sub>DD</sub> Specifications

**Table 8: I<sub>DD</sub> Specifications – Quad Die, Dual Channel (Continued)**
 $V_{DD2}, V_{DDQ} = 1.14\text{--}1.30\text{V}; V_{DD1} = 1.70\text{--}1.95\text{V}; T_C = -40^\circ\text{C to } +105^\circ\text{C}$ 

Symbol	Supply	Speed		Unit	Parameter/Condition
		1066	800		
I <sub>DD3N1</sub>	V <sub>DD1</sub>	TBD	TBD	mA	All devices in active non power-down standby current t <sub>CK</sub> = t <sub>CK</sub> (avg) MIN; CKE is HIGH; CS <sub>n</sub> is HIGH; One bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I <sub>DD3N2</sub>	V <sub>DD2</sub>	TBD	TBD		
I <sub>DD3N,in</sub>	V <sub>DDQ</sub>	TBD	TBD		
I <sub>DD3NS1</sub>	V <sub>DD1</sub>	TBD	TBD	mA	All devices in active non power-down standby current with clock stop CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is HIGH; CS <sub>n</sub> is HIGH; One bank is active; CA bus inputs are STABLE; Data bus inputs are STABLE
I <sub>DD3NS2</sub>	V <sub>DD2</sub>	TBD	TBD		
I <sub>DD3NS,in</sub>	V <sub>DDQ</sub>	TBD	TBD		
I <sub>DD4R1</sub>	V <sub>DD1</sub>	TBD	TBD	mA	All devices in operating burst read t <sub>CK</sub> = t <sub>CK</sub> (avg) MIN; CS <sub>n</sub> is HIGH between valid commands; One bank is active; BL = 4; RL = RL (MIN); CA bus inputs are SWITCHING; 50% data change occurs at each burst transfer
I <sub>DD4R2</sub>	V <sub>DD2</sub>	TBD	TBD		
I <sub>DD4W1</sub>	V <sub>DD1</sub>	TBD	TBD	mA	All devices in operating burst write t <sub>CK</sub> = t <sub>CK</sub> (avg) MIN; CS <sub>n</sub> is HIGH between valid commands; One bank is active; BL = 4; WL = WL (MIN); CA bus inputs are SWITCHING; 50% data change occurs at each burst transfer
I <sub>DD4W2</sub>	V <sub>DD2</sub>	TBD	TBD		
I <sub>DD4W,in</sub>	V <sub>DDQ</sub>	TBD	TBD		
I <sub>DD51</sub>	V <sub>DD1</sub>	TBD	TBD	mA	All devices in all bank auto-refresh t <sub>CK</sub> = t <sub>CK</sub> (avg) MIN; CKE is HIGH between valid commands; t <sub>RC</sub> = t <sub>RC</sub> ab (MIN); Burst refresh; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I <sub>DD52</sub>	V <sub>DD2</sub>	TBD	TBD		
I <sub>DD5,in</sub>	V <sub>DDQ</sub>	TBD	TBD		
I <sub>DD5AB1</sub>	V <sub>DD1</sub>	TBD	TBD	mA	All devices in all bank auto-refresh t <sub>CK</sub> = t <sub>CK</sub> (avg) MIN; CKE is HIGH between valid commands; t <sub>RC</sub> = t <sub>REFI</sub> ; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I <sub>DD5AB2</sub>	V <sub>DD2</sub>	TBD	TBD		
I <sub>DD5AB,in</sub>	V <sub>DDQ</sub>	TBD	TBD		
I <sub>DD5PB1</sub>	V <sub>DD1</sub>	TBD	TBD	mA	All devices in per bank auto-refresh t <sub>CK</sub> = t <sub>CK</sub> (avg) MIN; CKE is HIGH between valid commands; t <sub>RC</sub> = t <sub>REFI</sub> pb; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I <sub>DD5PB2</sub>	V <sub>DD2</sub>	TBD	TBD		
I <sub>DD5PB,in</sub>	V <sub>DDQ</sub>	TBD	TBD		





## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM I<sub>DD</sub> Specifications

**Table 8: I<sub>DD</sub> Specifications – Quad Die, Dual Channel (Continued)**
 $V_{DD2}, V_{DDQ} = 1.14\text{--}1.30\text{V}; V_{DD1} = 1.70\text{--}1.95\text{V}; T_C = -40^\circ\text{C to } +105^\circ\text{C}$ 

Symbol	Supply	Speed		Unit	Parameter/Condition
		1066	800		
I <sub>DD81</sub>	V <sub>DD1</sub>	TBD	TBD	μA	All devices in deep power-down CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
I <sub>DD82</sub>	V <sub>DD2</sub>	TBD	TBD		
I <sub>DD8,in</sub>	V <sub>DDQ</sub>	TBD	TBD		

- Notes: 1. Published I<sub>DD</sub> values are the maximum of the distribution of the arithmetic mean.  
2. I<sub>DD</sub> current specifications are tested after the device is properly initialized.

**Table 9: I<sub>DD6</sub> Full-Array Self Refresh Current at 45°C**
 $V_{DD2}, V_{DDQ} = 1.14\text{--}1.30\text{V}; V_{DD1} = 1.70\text{--}1.95\text{V}$ 

PASR	Supply	Value	Unit	Parameters/Conditions
Full array	V <sub>DD1</sub>	TBD	μA	All devices in self refresh CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
	V <sub>DD2</sub>	TBD		
	V <sub>DDQ</sub>	TBD		
1/2 array	V <sub>DD1</sub>	TBD		
	V <sub>DD2</sub>	TBD		
	V <sub>DDQ</sub>	TBD		
1/4 array	V <sub>DD1</sub>	TBD		
	V <sub>DD2</sub>	TBD		
	V <sub>DDQ</sub>	TBD		
1/8 array	V <sub>DD1</sub>	TBD		
	V <sub>DD2</sub>	TBD		
	V <sub>DDQ</sub>	TBD		

- Note: 1. I<sub>DD6</sub> 45°C is the typical of the distribution of the arithmetic mean.


**Table 10: I<sub>DD6</sub> Partial-Array Self Refresh Current at 85°C**
 $V_{DD2}, V_{DDQ} = 1.14\text{--}1.30\text{V}; V_{DD1} = 1.70\text{--}1.95\text{V}$ 

PASR	Supply	Value	Unit	Parameters/Conditions
Full array	V <sub>DD1</sub>	TBD	μA	All devices in self refresh CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
	V <sub>DD2</sub>	TBD		
	V <sub>DDQ</sub>	TBD		
1/2 array	V <sub>DD1</sub>	TBD		
	V <sub>DD2</sub>	TBD		
	V <sub>DDQ</sub>	TBD		
1/4 array	V <sub>DD1</sub>	TBD		
	V <sub>DD2</sub>	TBD		
	V <sub>DDQ</sub>	TBD		
1/8 array	V <sub>DD1</sub>	TBD		
	V <sub>DD2</sub>	TBD		
	V <sub>DDQ</sub>	TBD		

Note: 1. I<sub>DD6</sub> 85°C is the maximum of the distribution of the arithmetic mean.

**Table 11: I<sub>DD6</sub> Partial-Array Self Refresh Current at 105°C**
 $V_{DD2}, V_{DDQ} = 1.14\text{--}1.30\text{V}; V_{DD1} = 1.70\text{--}1.95\text{V}$ 

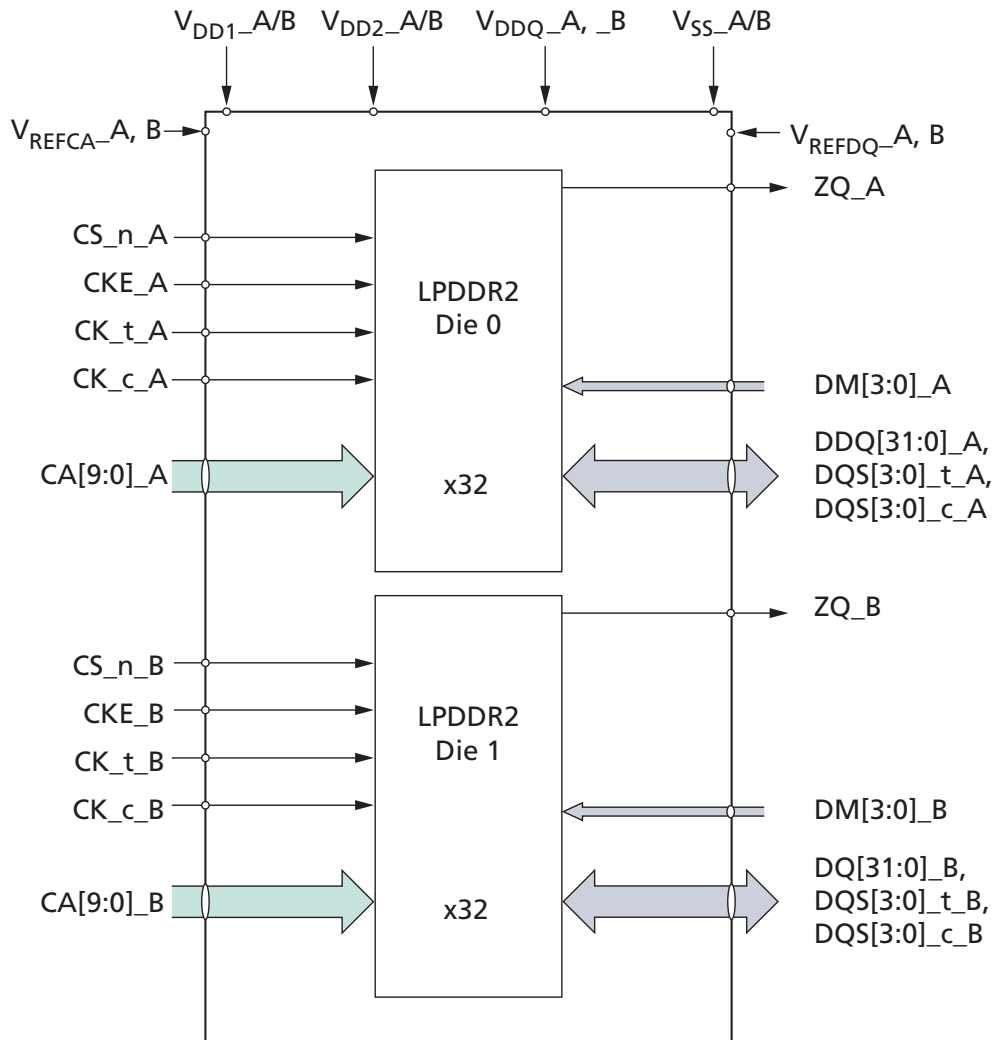
PASR	Supply	Value	Unit	Parameters/Conditions
Full array	V <sub>DD1</sub>	TBD	μA	All devices in self refresh CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
	V <sub>DD2</sub>	TBD		
	V <sub>DDQ</sub>	TBD		
1/2 array	V <sub>DD1</sub>	TBD		
	V <sub>DD2</sub>	TBD		
	V <sub>DDQ</sub>	TBD		
1/4 array	V <sub>DD1</sub>	TBD		
	V <sub>DD2</sub>	TBD		
	V <sub>DDQ</sub>	TBD		
1/8 array	V <sub>DD1</sub>	TBD		
	V <sub>DD2</sub>	TBD		
	V <sub>DDQ</sub>	TBD		

Note: 1. I<sub>DD6</sub> 105°C is the typical of the distribution of the arithmetic mean.



## Package Block Diagrams

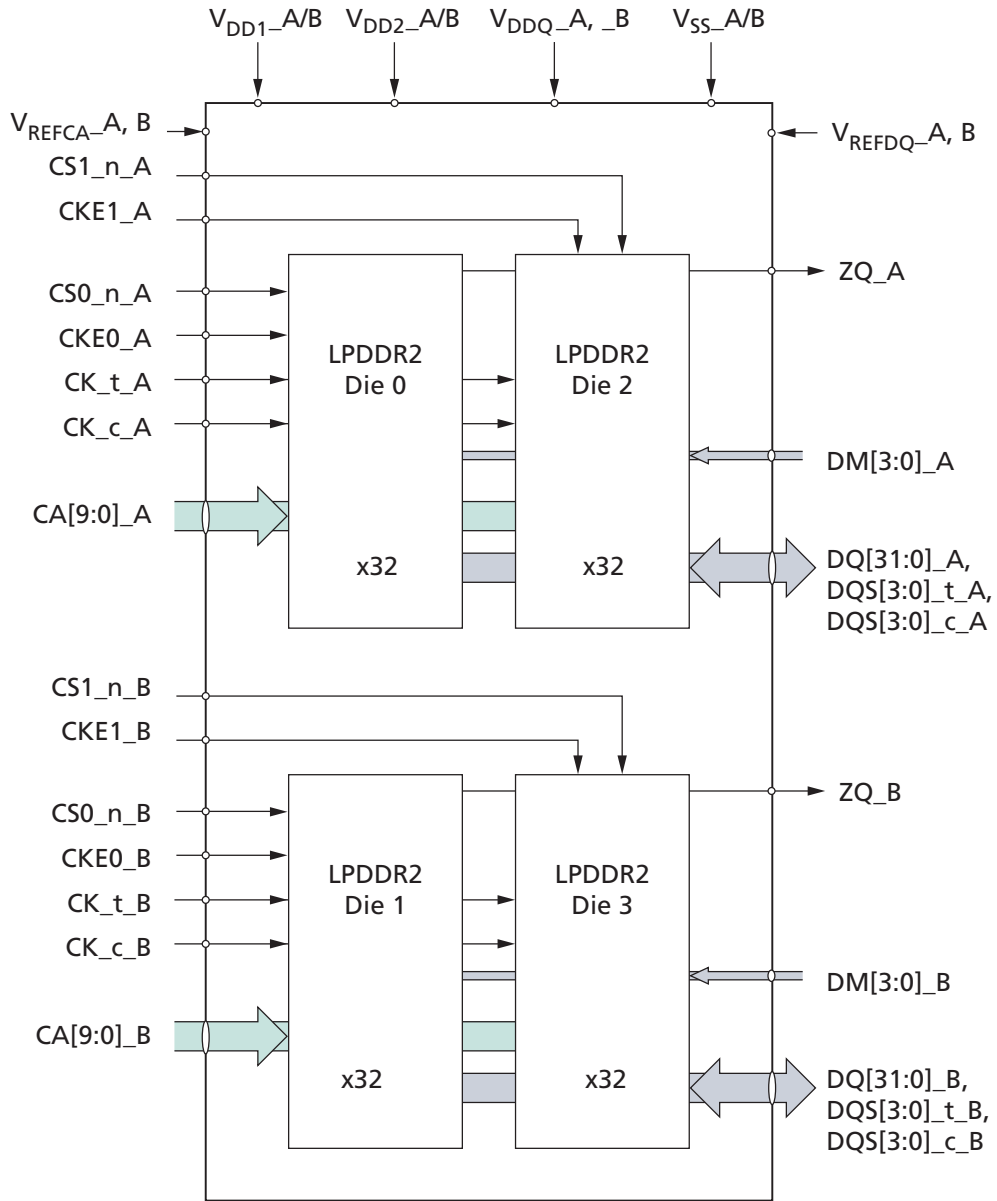
Figure 2: Dual Die Single Rank, Single Channel Package Block Diagram





## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Package Block Diagrams

**Figure 3: Quad Die Dual Rank, Dual Channel Package Block Diagram**

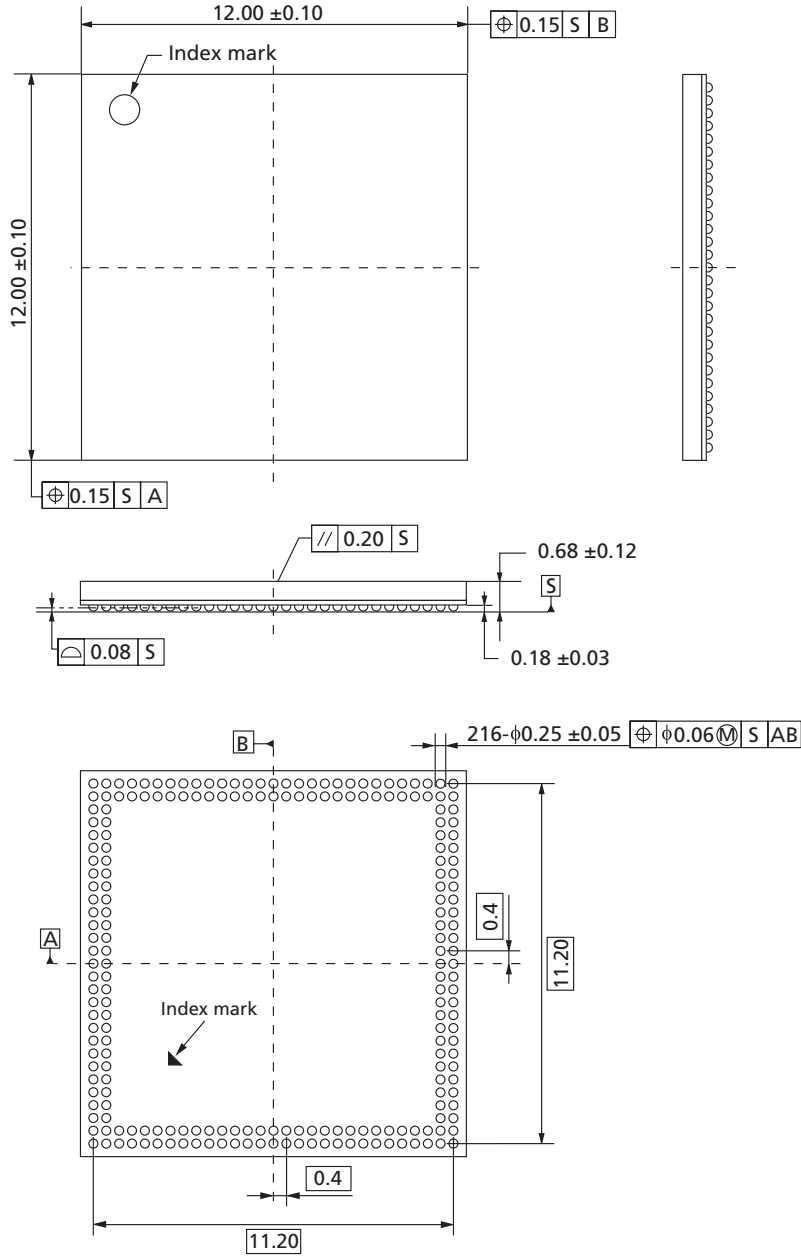




**216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Package Dimensions**

**Package Dimensions**

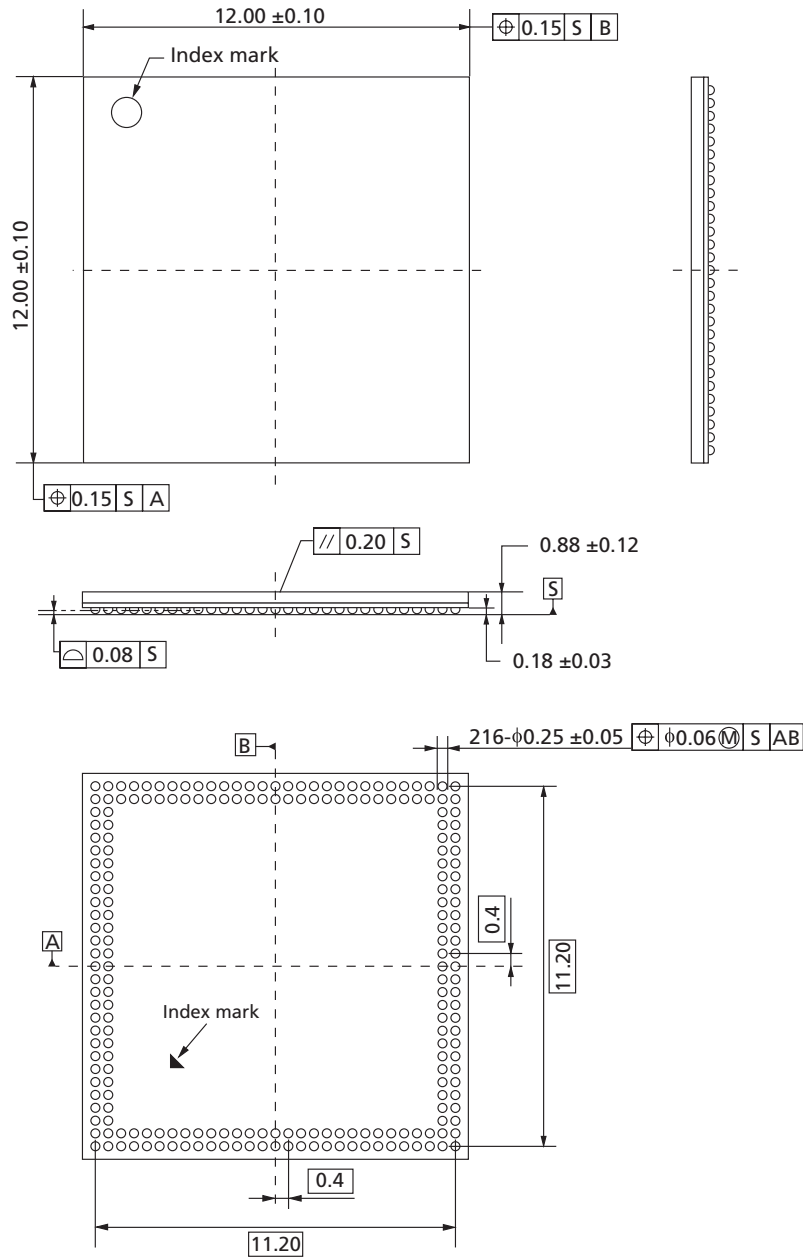
**Figure 4: 216-Ball FBGA (12mm x 12mm x 0.8mm) – EDB8164B4PR, EDB8164B4PT**



Note: 1. All dimensions are in millimeters.

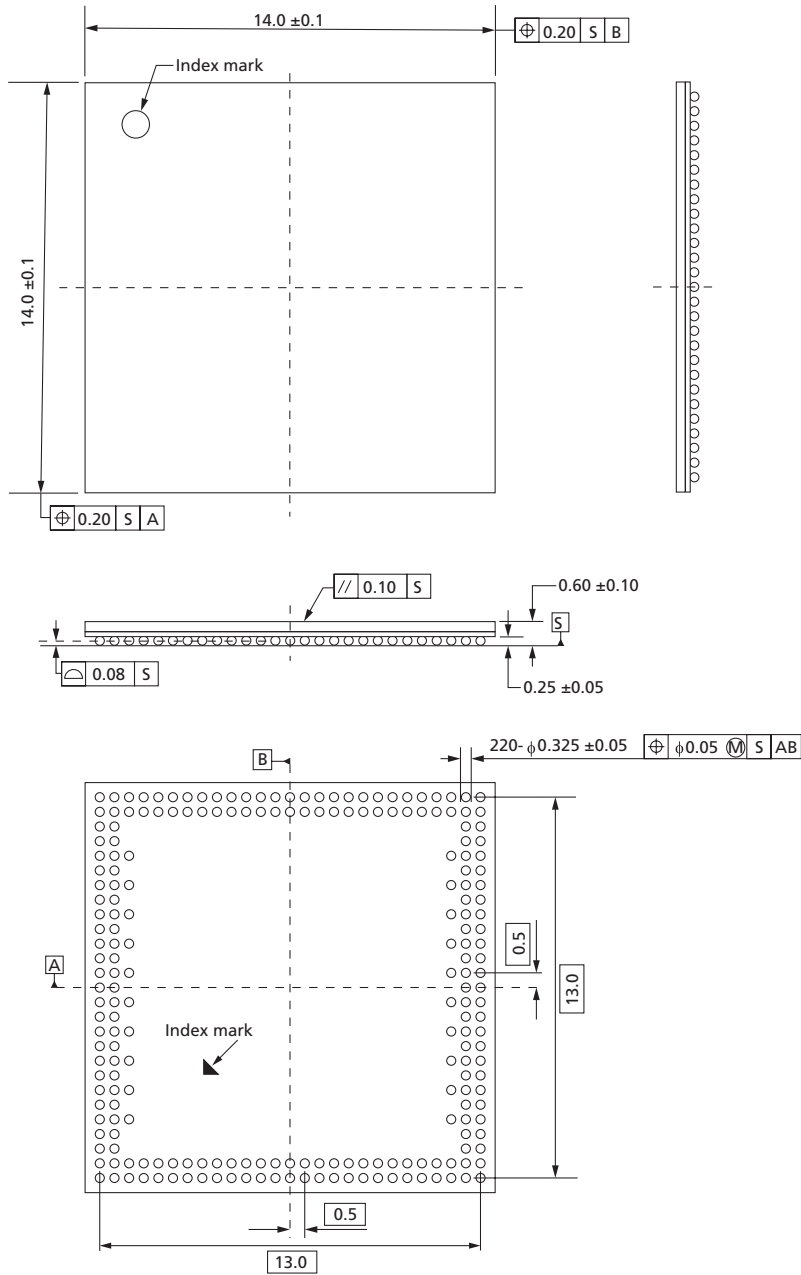
## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Package Dimensions

Figure 5: 216-Ball FBGA (12mm x 12mm x 1.0mm) – EDBA164B4PR



Note: 1. All dimensions are in millimeters.

**Figure 6: 220-Ball FBGA (14mm x 14mm x 0.7mm) – EDB8164B4PK**



Note: 1. All dimensions are in millimeters.

# Ball Assignments

Figure 7: 216-Ball Dual-Channel FBGA – 2 x 4Gb Die

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
A	NC	V <sub>SS</sub>	V <sub>DD2</sub>	DQ30_A	DQ29_A	V <sub>SS</sub>	DQ26_A	DQ25_A	V <sub>SS</sub>	DQS3_c_A	V <sub>SS</sub>	DQ14_A	DQ13_A	V <sub>SS</sub>	V <sub>DD1</sub>	V <sub>DD2</sub>	DQ11_A	DQ10_A	DQ9_A	DQS1_t_A	DM1_A	V <sub>DD0</sub>	DQS0_t_A	DQ7_A	DQ6_A
B	V <sub>SS</sub>	NC	DQ31_A	V <sub>DD0</sub>	DQ28_A	DQ27_A	V <sub>DD0</sub>	DQ24_A	V <sub>DD0</sub>	DQS3_t_A	DM3_A	DQ15_A	V <sub>DD0</sub>	V <sub>SS</sub>	V <sub>REFDQ_A</sub>	V <sub>DD2</sub>	DQ12_A	V <sub>DD0</sub>	DQ8_A	DQS1_c_A	V <sub>SS</sub>	DM0_A	DQS0_c_A	V <sub>SS</sub>	V <sub>DD0</sub>
C	V <sub>DD1</sub>	DQ16_B																							
D	DQ17_B	V <sub>DD0</sub>																							
E	DQ18_B	DQ19_B																							
F	V <sub>SS</sub>	DQ20_B																							
G	DQ21_B	V <sub>DD0</sub>																							
H	DQ22_B	DQ23_B																							
J	V <sub>SS</sub>	V <sub>DD0</sub>																							
K	DQS2_c_B	DQS2_t_B																							
L	DM2_B	DQ0_B																							
M	DQ1_B	V <sub>SS</sub>																							
N	DQ2_B	V <sub>DD1</sub>																							
P	V <sub>SS</sub>	V <sub>SS</sub>																							
R	V <sub>DD1</sub>	V <sub>REFDQ_B</sub>																							
T	V <sub>DD2</sub>	V <sub>DD2</sub>																							
U	V <sub>DD0</sub>	DQ3_B																							
V	DQ4_B	V <sub>SS</sub>																							
W	DQ6_B	DQ5_B																							
Y	V <sub>DD0</sub>	DQ7_B																							
AA	DQS0_t_B	DQS0_c_B																							
AB	DM0_B	V <sub>SS</sub>																							
AC	V <sub>DD0</sub>	DM1_B																							
AD	DQS1_c_B	DQS1_t_B																							
AE	DQ8_B	V <sub>SS</sub>																							
AF	DQ9_B	V <sub>DD0</sub>																							
AG	DQ10_B	DQ11_B																							
AH	V <sub>SS</sub>	V <sub>DD1</sub>	V <sub>DD2</sub>	DQ13_B	V <sub>SS</sub>	DQ15_B	DM3_B	DQS3_t_B	V <sub>DD0</sub>	DQ26_B	DQ27_B	V <sub>DD0</sub>	DQ30_B	V <sub>SS</sub>	V <sub>DD2</sub>	V <sub>REFCA_A</sub>	CA9_A	V <sub>SS</sub>	CA7_A	CA6_A	CK_c_A	NC	CKE_A	CS_n_A	CA3_A
AJ	NC	V <sub>SS</sub>	DQ12_B	V <sub>DD0</sub>	DQ14_B	V <sub>DD0</sub>	V <sub>SS</sub>	DQS3_c_B	DQ24_B	DQ25_B	V <sub>SS</sub>	DQ28_B	DQ29_B	DQ31_B	V <sub>DD1</sub>	V <sub>SS</sub>	ZQ_A	CA8_A	NC	CA5_A	CK_t_A	V <sub>SS</sub>	NC	NC	CA4_A

Top View (ball down)

Channel a (A) Channel b (B)



# Ball Assignments

**Figure 8: 220-Ball Dual-Channel FBGA – 2 x 4Gb Die**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A	NC	V <sub>SS</sub>	V <sub>DD2</sub>	V <sub>SS</sub>	DQ29_B	DQ28_B	V <sub>SS</sub>	DQ25_B	DQ24_B	DQS3_c_B	DM3_B	DQ15_B	V <sub>SS</sub>	DQ13_B	DQ11_B	V <sub>SS</sub>	DQ9_B	DQS1_c_B	DM1_B	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD2</sub>	DQS0_c_B	DQ0_B
B	V <sub>DD1</sub>	NC	V <sub>DDQ</sub>	DQ31_B	DQ30_B	V <sub>DDQ</sub>	DQ27_B	DQ26_B	V <sub>DDQ</sub>	DQS3_t_B	V <sub>SS</sub>	V <sub>DDQ</sub>	DQ14_B	DQ12_B	V <sub>DDQ</sub>	DQ10_B	DQ8_B	DQS1_t_B	V <sub>DDQ</sub>	V <sub>REFDQ_B</sub>	V <sub>DD1</sub>	DM0_B	DQS0_t_B	V <sub>DD1</sub>
C	DQ16_A	DQ17_A																						
D	DQ18_A	V <sub>DDQ</sub>																						
E	V <sub>SS</sub>	DQ20_A	DQ19_A																					
F	DQ21_A	V <sub>DDQ</sub>																						
G	V <sub>SS</sub>	DQ22_A	DQ23_A																					
H	DQS2_t_A	DQS2_c_A																						
J	V <sub>SS</sub>	DM2_A	DQ0_A																					
K	DQ1_A	V <sub>DDQ</sub>																						
L	V <sub>SS</sub>	DQ2_A	DQ3_A																					
M	DQ4_A	V <sub>DDQ</sub>																						
N	V <sub>SS</sub>	DQ5_A	DQ6_A																					
P	DQ7_A	V <sub>DDQ</sub>																						
R	V <sub>SS</sub>	DQS0_c_A	DQS0_t_A																					
T	DM0_A	V <sub>DDQ</sub>																						
U	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>REFDQ_A</sub>																					
V	V <sub>DD2</sub>	V <sub>DD1</sub>																						
W	V <sub>SS</sub>	V <sub>DD2</sub>	DM1_A																					
Y	DQS1_c_A	DQS1_t_A																						
AA	V <sub>SS</sub>	DQ9_A	DQ10_A																					
AB	DQ8_A	V <sub>DDQ</sub>																						
AC	V <sub>SS</sub>	DQ11_A	DQ12_A																					
AD	DQ13_A	DQ14_A																						
AE	V <sub>SS</sub>	DQ15_A																						
AF	V <sub>SS</sub>	V <sub>DDQ</sub>	DM3_A	DQS3_t_A	DQS3_c_A	DQ25_A	DQ27_A	V <sub>DDQ</sub>	DQ29_A	DQ31_A	V <sub>DD2</sub>	V <sub>DD1</sub>	NC	CA9_B	CA7_B	V <sub>DD2</sub>	V <sub>REFCA_B</sub>	NC	CK_t_B	NC	CS0_n_B	CA4_B	NC	CA2_B
AG	NC	V <sub>DD2</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	DQ24_A	DQ26_A	V <sub>SS</sub>	DQ28_A	DQ30_A	V <sub>SS</sub>	V <sub>SS</sub>	ZQ_B	V <sub>SS</sub>	CA8_B	CA6_B	CA5_B	V <sub>SS</sub>	V <sub>SS</sub>	CK_c_B	CKE0_B	NC	V <sub>SS</sub>	CA3_B	CA1_B
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24

Top View (ball down)

Channel a (A)
  Channel b (B)

# Ball Assignments

**Figure 9: 216-Ball Dual-Channel FBGA – 4 x 4Gb Die**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
A	NC	V <sub>SS</sub>	V <sub>DD2</sub>	DQ30_A	DQ29_A	V <sub>SS</sub>	DQ26_A	DQ25_A	V <sub>SS</sub>	DQS3_c_A	V <sub>SS</sub>	DQ14_A	DQ13_A	V <sub>SS</sub>	V <sub>DD1</sub>	V <sub>DD2</sub>	DQ11_A	DQ10_A	DQ9_A	DQS1_L_A	DM1_A	V <sub>DD0</sub>	DQS0_L_A	DQ7_A	DQ6_A
B	V <sub>SS</sub>	NC	DQ31_A	V <sub>DD0</sub>	DQ28_A	DQ27_A	V <sub>DD0</sub>	DQ24_A	V <sub>DD0</sub>	DQS3_L_A	DM3_A	DQ15_A	V <sub>DD0</sub>	V <sub>SS</sub>	V <sub>REFDQ_A</sub>	V <sub>DD2</sub>	DQ12_A	V <sub>DD0</sub>	DQ8_A	DQS1_c_A	V <sub>SS</sub>	DM0_A	DQS0_c_A	V <sub>SS</sub>	V <sub>DD0</sub>
C	V <sub>DD1</sub>	DQ16_B																							
D	DQ17_B	V <sub>DD0</sub>																							
E	DQ18_B	DQ19_B																							
F	V <sub>SS</sub>	DQ20_B																							
G	DQ21_B	V <sub>DD0</sub>																							
H	DQ22_B	DQ23_B																							
J	V <sub>SS</sub>	V <sub>DD0</sub>																							
K	DQS2_c_B	DQS2_L_B																							
L	DM2_B	DQ0_B																							
M	DQ1_B	V <sub>SS</sub>																							
N	DQ2_B	V <sub>DD1</sub>																							
P	V <sub>SS</sub>	V <sub>SS</sub>																							
R	V <sub>DD1</sub>	V <sub>REFDQ_B</sub>																							
T	V <sub>DD2</sub>	V <sub>DD2</sub>																							
U	V <sub>DD0</sub>	DQ3_B																							
V	DQ4_B	V <sub>SS</sub>																							
W	DQ6_B	DQ5_B																							
Y	V <sub>DD0</sub>	DQ7_B																							
AA	DQS0_L_B	DQS0_c_B																							
AB	DM0_B	V <sub>SS</sub>																							
AC	V <sub>DD0</sub>	DM1_B																							
AD	DQS1_c_B	DQS1_L_B																							
AE	DQ8_B	V <sub>SS</sub>																							
AF	DQ9_B	V <sub>DD0</sub>																							
AG	DQ10_B	DQ11_B																							
AH	V <sub>SS</sub>	V <sub>DD1</sub>	V <sub>DD2</sub>	DQ13_B	V <sub>SS</sub>	DQ15_B	DM3_B	DQS3_L_B	V <sub>DD0</sub>	DQ26_B	DQ27_B	V <sub>DD0</sub>	DQ30_B	V <sub>SS</sub>	V <sub>DD2</sub>	V <sub>REFCA_A</sub>	CA9_A	V <sub>SS</sub>	CA7_A	CA6_A	CK_c_A	NC	CKE0_A	CS0_n_A	CA3_A
AJ	NC	V <sub>SS</sub>	DQ12_B	V <sub>DD0</sub>	DQ14_B	V <sub>DD0</sub>	V <sub>SS</sub>	DQS3_c_B	DQ24_B	DQ25_B	V <sub>SS</sub>	DQ28_B	DQ29_B	DQ31_B	V <sub>DD1</sub>	V <sub>SS</sub>	ZQ_A	CA8_A	NC	CA5_A	CK_L_A	V <sub>SS</sub>	CKE1_A	CS1_n_A	CA4_A

Top View (ball down)

Channel a (A) Channel b (B)



## Ball Descriptions

The ball/pad description table below is a comprehensive list of signals for the device family. All signals listed may not be supported on this device. See Ball Assignments for information specific to this device.

**Table 12: Ball/Pad Descriptions**

Symbol	Type	Description
CA[9:0]_A, CA[9:0]_B	Input	<b>Command/address inputs:</b> Provide the command and address inputs according to the command truth table. A separate CA[9:0] is provided for each channel (A and B).
CK_t_A, CK_t_B CK_c_A, CK_c_B	Input	<b>Clock:</b> Differential clock inputs. All CA inputs are sampled on both rising and falling edges of CK. CS and CKE inputs are sampled at the rising edge of CK. AC timings are referenced to clock. A separate CK_t/CK_c is provided for each channel (A and B).
CKE[1:0]_A, CKE[1:0]_B	Input	<b>Clock enable:</b> CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is considered part of the command code. CKE is sampled on the rising edge of CK. A separate CKE is provided for each channel (A and B).
CS[1:0]_n_A, CS[1:0]_n_B	Input	<b>Chip select:</b> Considered part of the command code and is sampled on the rising edge of CK. A separate CS_n is provided for each channel (A and B).
DM[3:0]_A, DM[3:0]_B	Input	<b>Input data mask:</b> Input mask signal for write data. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. DM[3:0] is DM for each of the four data bytes, respectively. A separate DM[3:0] is provided for each channel (A and B).
DQ[31:0]_A, DQ[31:0]_B	I/O	<b>Data input/output:</b> Bidirectional data bus. A separate DQ[11:0] is provided for each channel (A and B).
DQS[3:0]_t_A, DQS[3:0]_t_B, DQS[3:0]_c_A, DQS[3:0]_c_B	I/O	<b>Data strobe:</b> Bidirectional (used for read and write data) and complementary (DQS_t and DQS_c). It is edge-aligned output with read data and centered input with write data. DQS[3:0]_t/DQS[3:0]_c is DQS for each of the four data bytes, respectively. A separate DQS[3:0]_t and DQS[3:0]_c is provided for each channel (A and B).
V <sub>DDQ</sub> _A, V <sub>DDQ</sub> _B	Supply	<b>DQ power supply:</b> Isolated on the die for improved noise immunity.
V <sub>SSQ</sub> _A/B	Supply	<b>DQ ground:</b> Isolated on the die for improved noise immunity.
V <sub>DD1</sub> _A/B	Supply	<b>Core power:</b> Supply 1.
V <sub>DD2</sub> _A/B	Supply	<b>Core power:</b> Supply 2.
V <sub>SS</sub> _A/B	Supply	<b>Common ground.</b>
V <sub>REFCA</sub> _A, V <sub>REFCA</sub> _B V <sub>REFDQ</sub> _A, V <sub>REFDQ</sub> _B	Supply	<b>Reference voltage:</b> V <sub>REFCA</sub> is reference for command/address input buffers, V <sub>REFDQ</sub> is reference for DQ input buffers. A separate V <sub>REFCA</sub> and V <sub>REFDQ</sub> provided for each channel (A and B).
ZQ_A, ZQ_B	Reference	<b>External reference ball for output drive calibration:</b> This ball is tied to an external 240Ω resistor (RZQ), which is tied to V <sub>SSQ</sub> . A separate ZQ is provided for each channel (A and B).
NU	–	<b>Not usable:</b> Do not connect.
NC	–	<b>No connect:</b> Not internally connected.
(NC)	–	<b>No connect:</b> Balls indicated as (NC) are no connects; however, they could be connected together internally.



## Functional Description

Mobile LPDDR2 is a high-speed SDRAM internally configured as a 4- or 8-bank memory device. The device uses a double data rate architecture on the command/address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus is used to transmit command, address, and bank information. Each command uses one clock cycle, during which command information is transferred on both the rising and falling edges of the clock.

The LPDDR2-S4 device uses a double data rate architecture on the DQ pins to achieve high-speed operation. The double data rate architecture is essentially a  $4n$  prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR2-S4 effectively consists of a single  $4n$ -bit-wide, one-clock-cycle data transfer at the internal SDRAM core and four corresponding  $n$ -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

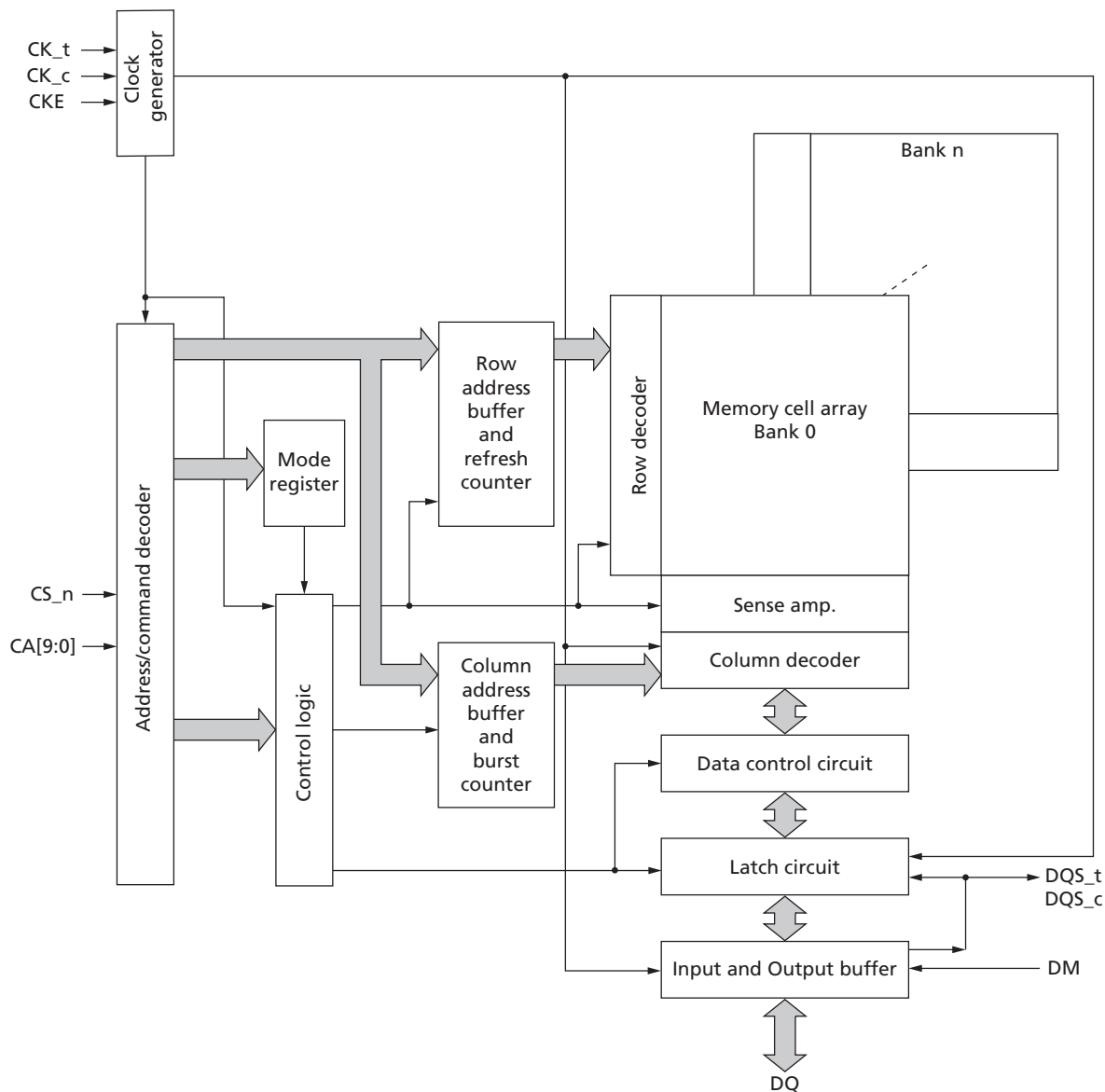
Read and write access is burst oriented; access starts at a selected location and continues for a programmed number of locations in a programmed sequence.

Access begins with the registration of an ACTIVATE command followed by a READ or WRITE command. Registered address and BA bits that coincide with the ACTIVATE command are used to select the row and bank to be accessed. Registered address bits that coincide with the READ or WRITE command are used to select the bank and the starting column location for the burst access.



# 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Simplified State Diagram

Figure 10: Functional Block Diagram



Note: 1. 512Mb is a 4-bank only.

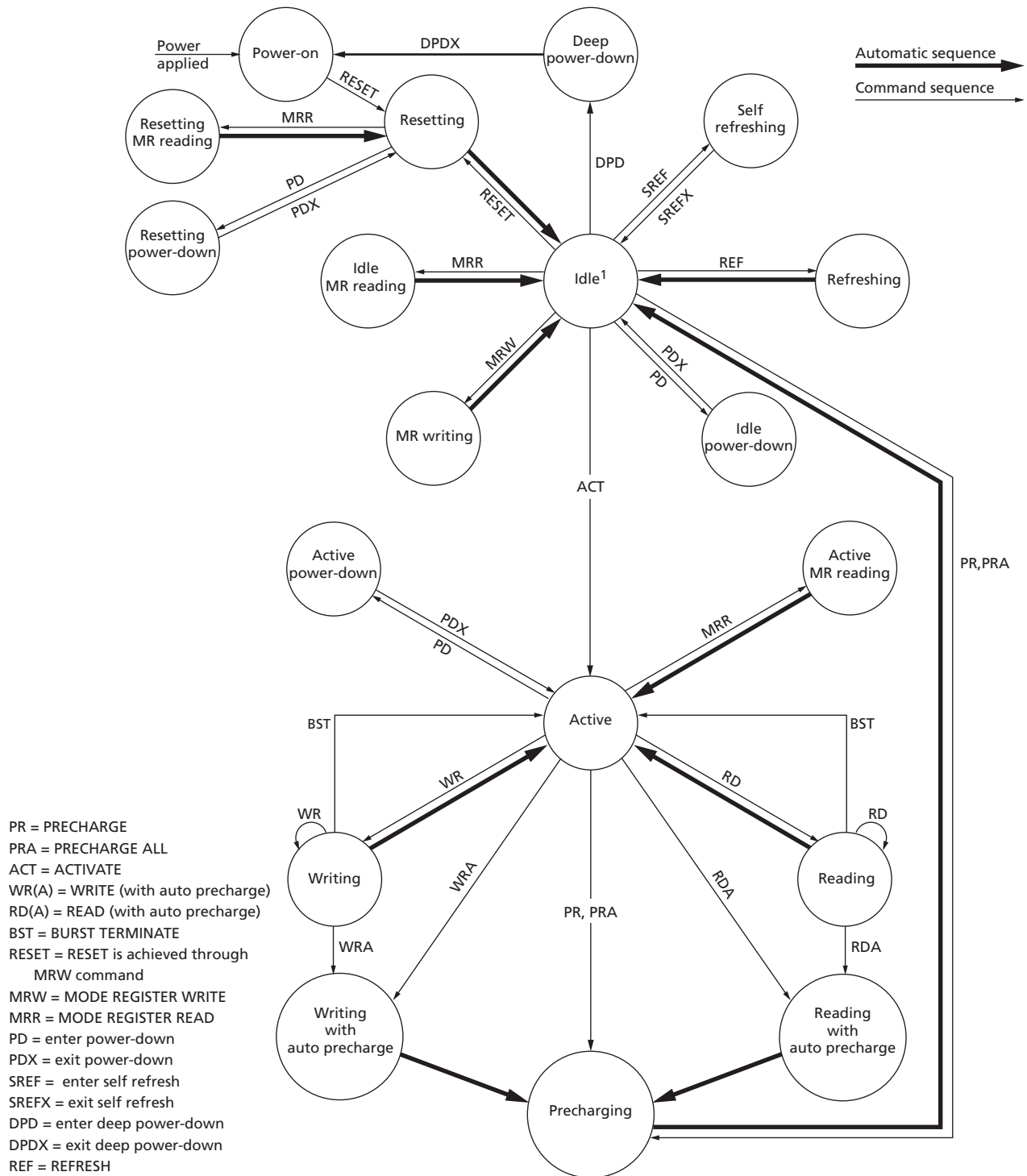
## Simplified State Diagram

The state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specification. The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the banks.



# 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Simplified State Diagram

Figure 11: Simplified State Diagram



Note: 1. All banks are precharged in the idle state.



## Power-Up and Initialization

The device must be powered up and initialized in a predefined manner. Power-up and initialization by means other than those specified will result in undefined operation.

### Voltage Ramp and Device Initialization

The following sequence must be used to power up the device. Unless specified otherwise, this procedure is mandatory (see the Voltage Ramp and Initialization Sequence figure). Power-up and initialization by means other than those specified will result in undefined operation.

#### 1. Voltage Ramp Beginning

While applying power (after  $T_a$ ), CKE must be held LOW ( $\leq 0.2 \times V_{DD2}$ ), and all other inputs must be between  $V_{ILmin}$  and  $V_{IHmax}$ . The device outputs remain at High-Z while CKE is held LOW.

On or before the completion of the voltage ramp ( $T_b$ ), CKE must be held LOW. DQ, DM, DQS\_t, and DQS\_c voltage levels must be between  $V_{SSQ}$  and  $V_{DDQ}$  during voltage ramp to avoid latchup. CK\_t, CK\_c, CS\_n, and CA input levels must be between  $V_{SS}$  and  $V_{DD2}$  during voltage ramp to avoid latchup.

The following conditions apply for voltage ramp:

- $T_a$  is the point when any power supply first reaches 300mV.
- Noted conditions apply between  $T_a$  and power-down (controlled or uncontrolled).
- $T_b$  is the point at which all supply and reference voltages are within their defined operating ranges.
- Power ramp duration  $t_{INIT0}$  ( $T_b - T_a$ ) must not exceed 20ms.
- For supply and reference voltage operating conditions, see the Recommended DC Operating Conditions table.
- The voltage difference between any of  $V_{SS}$ , and  $V_{SSQ}$  pins must not exceed 100mV.

#### 2. Voltage Ramp Completion

After  $T_a$  is reached:

- $V_{DD1}$  must be greater than  $V_{DD2} - 200mV$
- $V_{DD1}$  and  $V_{DD2}$  must be greater than  $V_{DDQ} - 200mV$
- $V_{REF}$  must always be less than all other supply voltages

Beginning at  $T_b$ , CKE must remain LOW for at least  $t_{INIT1} = 100ns$ , after which CKE can be asserted HIGH. The clock must be stable at least  $t_{INIT2} = 5 \times t_{CK}$  prior to the first CKE LOW-to-HIGH transition ( $T_c$ ). CKE, CS\_n, and CA inputs must observe setup and hold requirements ( $t_{IS}$ ,  $t_{IH}$ ) with respect to the first rising clock edge (and to subsequent falling and rising edges).

If any MRRs are issued, the clock period must be within the range defined for  $t_{CKb}$  (18ns to 100ns). MRWs can be issued at normal clock frequencies as long as all AC timings are met. Some AC parameters (for example,  $t_{DQSCK}$ ) could have relaxed timings (such as  $t_{DQSCKb}$ ) before the system is appropriately configured. While keeping CKE HIGH, NOP commands must be issued for at least  $t_{INIT3} = 200\mu s$  ( $T_d$ ).



### 3. RESET Command

After  $t_{\text{INIT3}}$  is satisfied, the MRW RESET command must be issued ( $T_d$ ). An optional PRECHARGE ALL command can be issued prior to the MRW RESET command. Wait at least  $t_{\text{INIT4}}$  while keeping CKE asserted and issuing NOP commands.

### 4. MRRs and Device Auto Initialization (DAI) Polling

After  $t_{\text{INIT4}}$  is satisfied ( $T_e$ ), only MRR commands and power-down entry/exit commands are supported. After  $T_e$ , CKE can go LOW in alignment with power-down entry and exit specifications (see Power-Down).

The MRR command can be used to poll the DAI bit, which indicates when device auto initialization is complete; otherwise, the controller must wait a minimum of  $t_{\text{INIT5}}$  or until the DAI bit is set before proceeding.

Because the memory output buffers are not properly configured by  $T_e$ , some AC parameters must use relaxed timing specifications before the system is appropriately configured.

After the memory device sets the DAI bit (MR0, DAI) to zero, indicating DAI complete, the device is in the idle state ( $T_f$ ). DAI status can be determined by issuing the MRR command to MR0.

The device sets the DAI bit no later than  $t_{\text{INIT5}}$  after the RESET command. The controller must wait at least  $t_{\text{INIT5}}$  or until the DAI bit is set before proceeding.

### 5. ZQ Calibration

After  $t_{\text{INIT5}}$  ( $T_f$ ), the MRW initialization calibration (ZQ calibration) command can be issued to the memory (MR10).

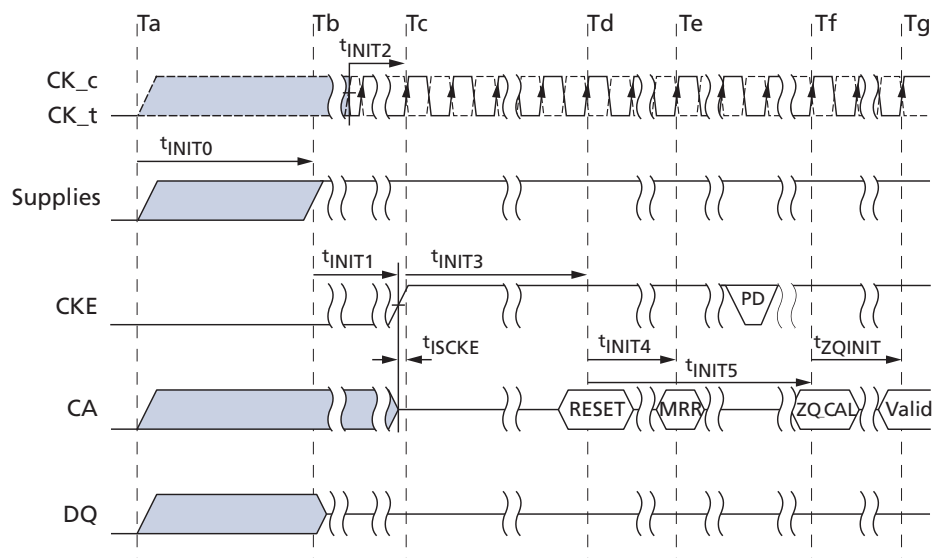
This command is used to calibrate output impedance over process, voltage, and temperature. In systems where more than one Mobile LPDDR2 device exists on the same bus, the controller must not overlap MRW ZQ calibration commands. The device is ready for normal operation after  $t_{\text{ZQINIT}}$ .

### 6. Normal Operation

After ( $T_g$ ), the MRW command must be used to properly configure the memory, including, for example, output buffer drive strength, latencies, and so on. Specifically, MR1, MR2, and MR3 must be set to configure the memory for the target frequency and memory configuration.

After the initialization sequence is complete, the device is ready for any valid command. After  $T_g$ , the clock frequency can be changed using the procedure described in Input Clock Frequency Changes and Stop Events.




**Figure 12: Voltage Ramp and Initialization Sequence**


Note: 1. High-Z on the CA bus indicates valid NOP.

**Table 13: Initialization Timing Parameters**

Parameter	Value		Unit	Comment
	Min	Max		
$t_{INIT0}$	–	20	ms	Maximum voltage ramp time
$t_{INIT1}$	100	–	ns	Minimum CKE LOW time after completion of voltage ramp
$t_{INIT2}$	5	–	$t_{CK}$	Minimum stable clock before first CKE HIGH
$t_{INIT3}$	200	–	$\mu$ s	Minimum idle time after first CKE assertion
$t_{INIT4}$	1	–	$\mu$ s	Minimum idle time after RESET command
$t_{INIT5}$	–	10	$\mu$ s	Maximum duration of device auto initialization
$t_{ZQINIT}$	1	–	$\mu$ s	ZQ initial calibration (S4 devices only)
$t_{CKb}$	18	100	ns	Clock cycle time during boot

Note: 1. The  $t_{INIT0}$  maximum specification is not a tested limit and should be used as a general guideline. For voltage ramp times exceeding  $t_{INIT0}$  MAX, contact the factory.

### Initialization After RESET (Without Voltage Ramp)

If the RESET command is issued before or after the power-up initialization sequence, the reinitialization procedure must begin at Td.

### Power-Off Sequence

While powering off, CKE must be held LOW ( $\leq 0.2 \times V_{DD2}$ ); all other inputs must be between  $V_{ILmin}$  and  $V_{IHmax}$ . The device outputs remain at High-Z while CKE is held LOW.



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Mode Register Definition

DQ, DM, DQS\_t, and DQS\_c voltage levels must be between  $V_{SSQ}$  and  $V_{DDQ}$  during the power-off sequence to avoid latchup. CK\_t, CK\_c, CS\_n, and CA input levels must be between  $V_{SS}$  and  $V_{DD2}$  during the power-off sequence to avoid latchup.

Tx is the point where any power supply drops below the minimum value specified in the Recommended DC Operating Conditions table.

Tz is the point where all power supplies are below 300mV. After Tz, the device is powered off.

### Required Power Supply Conditions Between Tx and Tz:

- $V_{DD1}$  must be greater than  $V_{DD2} - 200\text{mV}$
- $V_{DD1}$  must be greater than  $V_{DDQ} - 200\text{mV}$
- $V_{REF}$  must always be less than all other supply voltages

The voltage difference between  $V_{SS}$  and  $V_{SSQ}$  must not exceed 100mV.

For supply and reference voltage operating conditions, see Recommended DC Operating Conditions table.

## Uncontrolled Power-Off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

- At Tx, when the power supply drops below the minimum values specified in the Recommended DC Operating Conditions table, all power supplies must be turned off and all power-supply current capacity must be at zero, except for any static charge remaining in the system.
- After Tz, the point at which all power supplies first reach 300mV, the device must power off. The time between Tx and Tz must not exceed  $t_{POFF}$ . During this period, the relative voltage between power supplies is uncontrolled.  $V_{DD1}$  and  $V_{DD2}$  must decrease with a slope lower than  $0.5\text{ V}/\mu\text{s}$  between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

**Table 14: Power-Off Timing**

Parameter	Symbol	Min	Max	Unit
Maximum power-off ramp time	$t_{POFF}$	–	2	sec

## Mode Register Definition

The LPDDR2 device contains a set of mode registers used for programming device operating parameters, reading device information and status, and for initiating special operations such as DQ calibration, ZQ calibration, and device reset.

## Mode Register Assignments and Definitions

The MRR command is used to read from a register. The MRW command is used to write to a register. An “R” in the access column of the mode register assignment table indicates read-only; a “W” indicates write-only; “R/W” indicates read or write capable or enabled.



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Mode Register Definition

**Table 15: Mode Register Assignments**

Notes 1–5 apply to all parameters and conditions

MR#	MA[7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
0	00h	Device info	R	RFU			RZQI	RFU	DI	DAI		go to MR0
1	01h	Device feature 1	W	nWR (for AP)			WC	BT	BL			go to MR1
2	02h	Device feature 2	W	RFU			RL and WL				go to MR2	
3	03h	I/O config-1	W	RFU			DS				go to MR3	
4	04h	SDRAM refresh rate	R	TUF	RFU			Refresh rate			go to MR4	
5	05h	Basic config-1	R	LPDDR2 Manufacturer ID								go to MR5
6	06h	Basic config-2	R	Revision ID1								go to MR6
7	07h	Basic config-3	R	Revision ID2								go to MR7
8	08h	Basic config-4	R	I/O width	Density			Type			go to MR8	
9	09h	Test mode	W	Vendor-specific test mode								go to MR9
10	0Ah	I/O calibration	W	Calibration code								go to MR10
11–15	0Bh ~ 0Fh	Reserved	–	RFU								go to MR11
16	10h	PASR_Bank	W	Bank mask								go to MR16
17	11h	PASR_Seg	W	Segment mask								go to MR17
18–31	12h–1Fh	Reserved	–	RFU								go to MR18
32	20h	DQ calibration pattern A	R	See Data Calibration Pattern Description table								go to MR32
33–39	21h–27h	Do not use										go to MR33
40	28h	DQ calibration pattern B	R	See Data Calibration Pattern Description table								go to MR40
41–47	29h–2Fh	Do not use										go to MR41
48–62	30h–3Eh	Reserved	–	RFU								go to MR48
63	3Fh	RESET	W	X								go to MR63
64–126	40h–7Eh	Reserved	–	RFU								go to MR64
127	7Fh	Do not use										go to MR127
128–190	80h–BEh	Reserved for vendor use		RVU								go to MR128
191	BFh	Do not use										go to MR191
192–254	C0h–FEh	Reserved for vendor use		RVU								go to MR192
255	FFh	Do not use										go to MR255

- Notes:
1. RFU bits must be set to 0 during MRW.
  2. RFU bits must be read as 0 during MRR.
  3. For READs to a write-only or RFU register, DQS will be toggled and undefined data is returned.
  4. RFU mode registers must not be written.
  5. WRITEs to read-only registers must have no impact on the functionality of the device.



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Mode Register Definition

**Table 16: MR0 Device Information (MA[7:0] = 00h)**

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
	RFU		RZQI		RFU	DI	DAI

**Table 17: MR0 Op-Code Bit Definitions**

Notes 1–4 apply to all parameters and conditions

Register Information	Tag	Type	OP	Definition
Device auto initialization status	DAI	Read-only	OP0	0b: DAI complete
				1b: DAI in progress
Device information	DI	Read-only	OP1	0b:DDR2 Mobile RAM (S4 SDRAM)
Built-in self test for RZQ information	RZQI	Read-only	OP[4:3]	01b: ZQ pin might be connected to V <sub>DD2</sub> or left floating
				10b: ZQ pin might be shorted to ground
				11b: ZQ pin self test complete; no error condition detected(ZQ-pin may not connect to VDD or float nor short to GND)

- Notes:
1. If RZQI is supported, it will be set upon completion of the MRW ZQ initialization calibration.
  2. If ZQ is connected to V<sub>DD2</sub> to set default calibration, OP[4:3] must be set to 01. If ZQ is not connected to V<sub>DD2</sub>, either OP[4:3] = 01 or OP[4:3] = 10 could indicate a ZQ-pin assembly error. It is recommended that the assembly error be corrected.
  3. In the case of a possible assembly error (either OP[4:3] = 01 or OP[4:3] = 10, as defined above), the device will default to factory trim settings for R<sub>ON</sub>(output impedance) and will ignore ZQ calibration commands. In either case, the system might not function as intended.
  4. If a ZQ self test returns a value of 11b, this indicates that the device has detected a resistor connection to the ZQ pin. Note that this result cannot be used to validate the ZQ resistor value, nor does it indicate that the ZQ resistor tolerance meets the specified limits (240 ohms ±1%).

**Table 18: MR1 Device Feature 1 (MA[7:0] = 01h)**

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
	nWR (for AP)		WC	BT		BL	

**Table 19: MR1 Op-Code Bit Definitions**

Feature	Type	OP	Definition	Notes
BL = burst length	Write-only	OP[2:0]	010b: BL4 (default)	1
			011b: BL8	
			100b: BL16	
			All others: Reserved	



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Mode Register Definition

**Table 19: MR1 Op-Code Bit Definitions (Continued)**

Feature	Type	OP	Definition	Notes
BT = burst type	Write-only	OP3	0b: Sequential (default)	
			1b: Interleaved	
WC = wrap control	Write-only	OP4	0b: Wrap (default)	
			1b: No wrap (allowed for BL4 only)	
nWR = number of <sup>t</sup> WR clock cycles	Write-only	OP[7:5]	001b: nWR = 3 (default)	2
			010b: nWR = 4	
			011b: nWR = 5	
			100b: nWR = 6	
			101b: nWR = 7	
			110b: nWR = 8	
			All others: Reserved	

- Notes:
1. BL16, interleaved is not an official combination to be supported.
  2. The programmed value in nWR register is the number of clock cycles that determines when to start internal precharge operation for a WRITE burst with AP enabled. It is determined by RU (<sup>t</sup>WR/<sup>t</sup>CK).

**Table 20: Burst Sequence by Burst Length (BL), Burst Type (BT), and Wrap Control (WC)**

Notes 1–5 apply to all parameters and conditions

BL	BT	C3	C2	C1	C0	WC	Burst Cycle Number and Burst Address Sequence																	
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		
4	Any	X	X	0b	0b	Wrap	0	1	2	3														
		X	X	1b	0b		2	3	0	1														
	Any	X	X	X	0b	No wrap	y	y+1	y+2	y+3														
8	Seq	X	0b	0b	0b	Wrap	0	1	2	3	4	5	6	7										
		X	0b	1b	0b		2	3	4	5	6	7	0	1										
		X	1b	0b	0b		4	5	6	7	0	1	2	3										
		X	1b	1b	0b		6	7	0	1	2	3	4	5										
	Int	X	0b	0b	0b		0	1	2	3	4	5	6	7										
		X	0b	1b	0b		2	3	0	1	6	7	4	5										
		X	1b	0b	0b		4	5	6	7	0	1	2	3										
		X	1b	1b	0b		6	7	4	5	2	3	0	1										
	Any	X	X	X	0b		No wrap	Illegal (not supported)																



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Mode Register Definition

**Table 20: Burst Sequence by Burst Length (BL), Burst Type (BT), and Wrap Control (WC) (Continued)**

Notes 1–5 apply to all parameters and conditions

BL	BT	C3	C2	C1	C0	WC	Burst Cycle Number and Burst Address Sequence															
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
16	Seq	0b	0b	0b	0b	Wrap	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		0b	0b	1b	0b		2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1
		0b	1b	0b	0b		4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
		0b	1b	1b	0b		6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5
		1b	0b	0b	0b		8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
		1b	0b	1b	0b		A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9
		1b	1b	0b	0b		C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B
		1b	1b	1b	0b		E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D
	Int	X	X	X	0b	Illegal (not supported)																
Any	X	X	X	0b	No wrap	Illegal (not supported)																

- Notes:
1. C0 input is not present on CA bus. It is implied zero.
  2. For BL = 4, the burst address represents C[1:0].
  3. For BL = 8, the burst address represents C[2:0].
  4. For BL = 16, the burst address represents C[3:0].
  5. For no-wrap, BL4, the burst must not cross the page boundary or the sub-page boundary. The variable y can start at any address with C0 equal to 0, but must not start at any address shown in the following table.

**Table 21: No-Wrap Restrictions**

Width	64Mb	128Mb/256Mb	512Mb/1Gb/2Gb	4Gb/8Gb
Cannot cross full-page boundary				
x16	FE, FF, 00, 01	1FE, 1FF, 000, 001	3FE, 3FF, 000, 001	7FE, 7FF, 000, 001
x32	7E, 7F, 00, 01	FE, FF, 00, 01	1FE, 1FF, 000, 001	3FE, 3FF, 000, 001
Cannot cross sub-page boundary				
x16	7E, 7F, 80, 81	0FE, 0FF, 100, 101	1FE, 1FF, 200, 201	3FE, 3FF, 400, 401
x32	None	None	None	None

Note: 1. No-wrap BL = 4 data orders shown are prohibited.

**Table 22: MR2 Device Feature 2 (MA[7:0] = 02h)**

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				RL and WL			



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Mode Register Definition

**Table 23: MR2 Op-Code Bit Definitions**

Feature	Type	OP	Definition
RL and WL	Write-only	OP[3:0]	0001b: RL3/WL1 (default)
			0010b: RL4/WL2
			0011b: RL5/WL2
			0100b: RL6/WL3
			0101b: RL7/WL4
			0110b: RL8/WL4
			All others: Reserved

**Table 24: MR3 I/O Configuration 1 (MA[7:0] = 03h)**

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				DS			

**Table 25: MR3 Op-Code Bit Definitions**

Feature	Type	OP	Definition
DS	Write-only	OP[3:0]	0000b: Reserved
			0001b: 34.3 ohm typical
			0010b: 40 ohm typical (default)
			0011b: 48 ohm typical
			0100b: 60 ohm typical
			0101b: Reserved
			0110b: 80 ohm typical
			0111b: 120 ohm typical
			All others: Reserved

**Table 26: MR4 Device Temperature (MA[7:0] = 04h)**

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	RFU				SDRAM refresh rate		



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Mode Register Definition

**Table 27: MR4 Op-Code Bit Definitions**

Notes 1–8 apply to all parameters and conditions

Feature	Type	OP	Definition
SDRAM refresh rate	Read-only	OP[2:0]	000b: SDRAM low temperature operating limit exceeded
			001b: $4 \times t_{REFI}$ , $4 \times t_{REFIpb}$ , $4 \times t_{REFW}$
			010b: $2 \times t_{REFI}$ , $2 \times t_{REFIpb}$ , $2 \times t_{REFW}$
			011b: $1 \times t_{REFI}$ , $1 \times t_{REFIpb}$ , $1 \times t_{REFW}$ ( $\leq 85^\circ\text{C}$ )
			100b: Reserved
			101b: $0.25 \times t_{REFI}$ , $0.25 \times t_{REFIpb}$ , $0.25 \times t_{REFW}$ , do not derate SDRAM AC timing
			110b: $0.25 \times t_{REFI}$ , $0.25 \times t_{REFIpb}$ , $0.25 \times t_{REFW}$ , derate SDRAM AC timing
			111b: SDRAM high temperature operating limit exceeded
Temperature update flag (TUF)	Read-only	OP7	0b: OP[2:0] value has not changed since last read of MR4
			1b: OP[2:0] value has changed since last read of MR4

- Notes:
1. A MODE REGISTER READ from MR4 will reset OP7 to 0.
  2. OP7 is reset to 0 at power-up.
  3. If OP2 = 1, the device temperature is greater than 85°C.
  4. OP7 is set to 1 if OP[2:0] has changed at any time since the last MR4 read.
  5. The device might not operate properly when OP[2:0] = 000b or 111b.
  6. For specified operating temperature range and maximum operating temperature, refer to the Operating Temperature Range table.
  7. LPDDR2 devices must be derated by adding 1.875ns to the following core timing parameters:  $t_{RCD}$ ,  $t_{RC}$ ,  $t_{RAS}$ ,  $t_{RP}$ , and  $t_{RRD}$ . The  $t_{DQSCK}$  parameter must be derated as specified in AC Timing. Prevailing clock frequency specifications and related setup and hold timings remain unchanged.
  8. The recommended frequency for reading MR4 is provided in Temperature Sensor.

**Table 28: MR5 Basic Configuration 1 (MA[7:0] = 05h)**

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
LPDDR2 Manufacturer ID							

**Table 29: MR5 Op-Code Bit Definitions**

Feature	Type	OP	Definition
Manufacturer ID	Read-only	OP[7:0]	00000011b
			All others: Reserved





## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Mode Register Definition

**Table 30: MR6 Basic Configuration 2 (MA[7:0] = 06h)**

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID1 (Die Revision)							

Note: 1. MR6 is vendor-specific.

**Table 31: MR6 Op-Code Bit Definitions**

Feature	Type	OP	Definition
Revision ID1 (Die Revision)	Read-only	OP[7:0]	0000 0000b: Version A 0000 0001b: Version B 0000 0010b: Version C 0000 0010b: Version D(512Mb only) 0000 0011b: Version D

**Table 32: MR7 Basic Configuration 3 (MA[7:0] = 07h)**

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID2 (RFU)							

**Table 33: MR7 Op-Code Bit Definitions**

Feature	Type	OP	Definition
Revision ID2 (RFU)	Read-only	OP[7:0]	0000 0000b: Default Value

Note: 1. MR7 is vendor-specific.

**Table 34: MR8 Basic Configuration 4 (MA[7:0] = 08h)**

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

**Table 35: MR8 Op-Code Bit Definitions**

Feature	Type	OP	Definition
Type	Read-only	OP[1:0]	00b: S4 SDRAM
			01b: S2 SDRAM
			10b: Reserved
			11b: Reserved



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Mode Register Definition

**Table 35: MR8 Op-Code Bit Definitions (Continued)**

Feature	Type	OP	Definition
Density	Read-only	OP[5:2]	0000b: 64Mb
			0001b: 128Mb
			0010b: 256Mb
			0011b: 512Mb
			0100b: 1Gb
			0101b: 2Gb
			0110b: 4Gb
			0111b: 8Gb
			1000b: 16Gb
			1001b: 32Gb
			All others: Reserved
I/O width	Read-only	OP[7:6]	00b: x32
			01b: x16
			10b: x8
			11b: not used

**Table 36: MR9 Test Mode (MA[7:0] = 09h)**

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Vendor-specific test mode							

**Table 37: MR10 Calibration (MA[7:0] = 0Ah)**

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
S4	Calibration code							

**Table 38: MR10 Op-Code Bit Definitions**

Notes 1–6 apply to all parameters and conditions

Feature	Type	OP	Definition
Calibration code	Write-only	OP[7:0]	0xFF: Calibration command after initialization
			0xAB: Long calibration
			0x56: Short calibration
			0xC3: ZQRESET
			All others: Reserved

- Notes:
1. Host processor must not write MR10 with reserved values.
  2. The device ignores calibration commands when a reserved value is written into MR10.
  3. See AC timing table for the calibration latency.



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Mode Register Definition

4. If ZQ is connected to  $V_{SS}$  through  $R_{ZQ}$ , either the ZQ calibration function (see MODE REGISTER WRITE command) or default calibration (through the ZQRESET command) is supported. If ZQ is connected to  $V_{DD2}$ , the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection must not change after power is supplied to the device.
5. LPDDR2 devices that do not support calibration shall ignore the ZQ Calibration command.
6. Optionally, the MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection.

**Table 39: MR[11:15] Reserved (MA[7:0] = 0Bh-0Fh)**

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Reserved							

**Table 40: MR16 PASR Bank Mask (MA[7:0] = 010h)**

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Bank mask (4-bank or 8-bank)							

**Table 41: MR16 Op-Code Bit Definitions**

Feature	Type	OP	Definition
Bank[7:0] mask	Write-only	OP[7:0]	0b: refresh enable to the bank = unmasked (default)
			1b: refresh blocked = masked

Note: 1. For 4-bank devices, only OP[3:0] are used.

**Table 42: MR16 Bank and OP corresponding table**

Feature	Type	OP	4-Bank Mask		8-Bank Mask	
			Bank #	Bank Address	Bank #	Bank Address
Bank[7:0] mask	Write-only	0	Bank 0	000b	Bank 0	000b
		1	Bank 1	001b	Bank 1	001b
		2	Bank 2	010b	Bank 2	010b
		3	Bank 3	011b	Bank 3	011b
		4	-	-	Bank 4	100b
		5	-	-	Bank 5	101b
		6	-	-	Bank 6	110b
		7	-	-	Bank 7	111b

Note: 1. Each bank can be masked independently by setting each OP value.



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Mode Register Definition

**Table 43: MR17 PASR Segment Mask (MA[7:0] = 011h)**

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Segment mask							

Note: 1. This table applies for 1Gb to 8Gb devices only.

**Table 44: MR17 PASR Segment Mask Definitions (1Gb - 8Gb only)**

Feature	Type	OP	Definition
Segment[7:0] mask	Write-only	OP[7:0]	0b: refresh enable to the segment: = unmasked (default)
			1b: refresh blocked: = masked

**Table 45: MR17 PASR Row Address Ranges in Masked Segments**

Segment	OP	Segment Mask	1Gb	2Gb, 4Gb	8Gb
			R[12:10]	R[13:11]	R[14:12]
0	0	XXXXXXX1		000b	
1	1	XXXXXX1X		001b	
2	2	XXXXX1XX		010b	
3	3	XXXX1XXX		011b	
4	4	XXX1XXXX		100b	
5	5	XX1XXXXX		101b	
6	6	X1XXXXXX		110b	
7	7	1XXXXXXX		111b	

Note: 1. X is "Don't Care" for the designated segment.

**Table 46: Reserved Mode Registers**

Mode Register	MA	Address	Restriction	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR[18:19]	MA[7:0]	12h–13h	RFU	Reserved							
MR[20:31]		14h–1Fh	NVM <sup>1</sup>								
MR[33:39]		21h–27h	DNU <sup>1</sup>								
MR[41:47]		29h–2Fh									
MR[48:62]		30h–3Eh	RFU								
MR[64:126]		40h–7Eh	RFU								
MR127		7Fh	DNU								
MR[128:190]		80h–BEh	RVU <sup>1</sup>								
MR191		BFh	DNU								
MR[192:254]		C0h–FEh	RVU								
MR255		FFh	DNU								

Note: 1. NVM = nonvolatile memory use only; DNU = Do not use; RVU = Reserved for vendor use.

**Table 47: MR32 DQ Calibration Pattern A (MA[7:0] = 20H)**

MR32 Reads
Reads to MR32 return DQ Calibration Pattern A

**Table 48: MR40 DQ Calibration Pattern B (MA[7:0] = 28H)**

MR40 Reads
Reads to MR40 return DQ Calibration Pattern B

**Table 49: MR63 RESET (MA[7:0] = 3Fh) – MRW Only**

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
X							

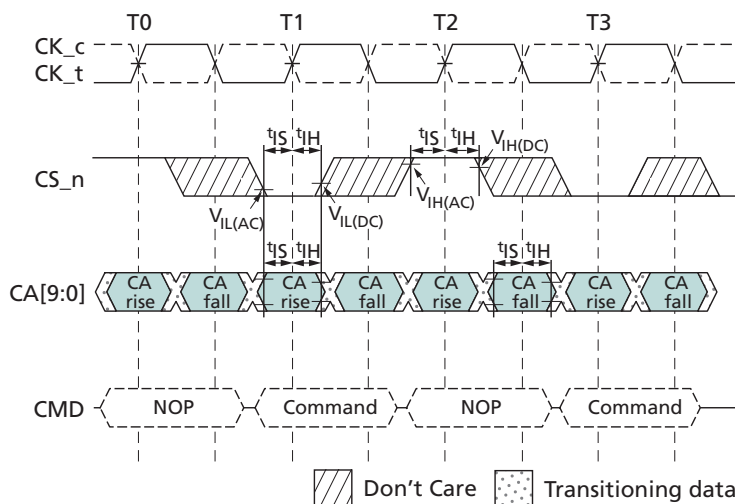
Note: 1. For additional information on MRW RESET see MODE REGISTER WRITE Command.

## Commands and Timing

The setup and hold timings shown in the figures below apply for all commands.

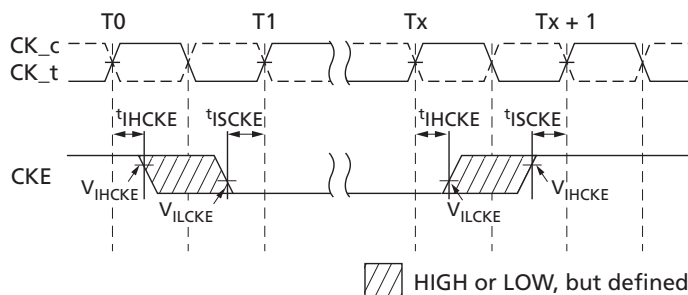


Figure 13: Command and Input Setup and Hold



Note: 1. Setup and hold conditions also apply to the CKE pin. For timing diagrams related to the CKE pin, see the Power-Down section.

Figure 14: CKE Input Setup and Hold



Notes: 1. After CKE is registered LOW, the CKE signal level is maintained below  $V_{ILCKE}$  for  $t_{CKE}$  specification (LOW pulse width).  
2. After CKE is registered HIGH, the CKE signal level is maintained below  $V_{IHCKE}$  for  $t_{CKE}$  specification (HIGH pulse width).

## ACTIVATE Command

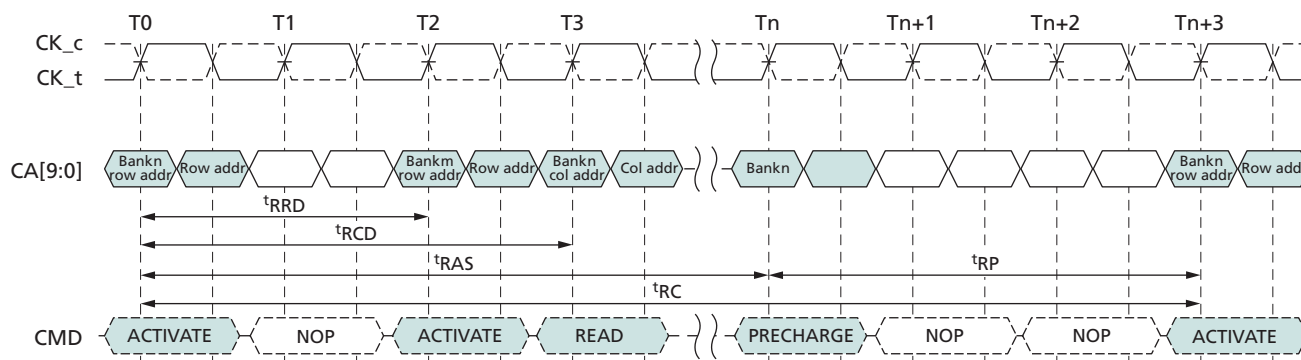
The ACTIVATE command is issued by holding CS<sub>n</sub> LOW, CA0 LOW, and CA1 HIGH at the rising edge of the clock. The bank addresses BA[2:0] are used to select the desired bank. Row addresses are used to determine which row to activate in the selected bank. The ACTIVATE command must be applied before any READ or WRITE operation can be executed. The device can accept a READ or WRITE command at  $t_{RCD}$  after the ACTIVATE command is issued. After a bank has been activated, it must be precharged before another ACTIVATE command can be applied to the same bank. The bank active and precharge times are defined as  $t_{RAS}$  and  $t_{RP}$ , respectively. The minimum time interval between successive ACTIVATE commands to the same bank is determined by the RAS



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM ACTIVATE Command

cycle time of the device ( $t_{RC}$ ). The minimum time interval between ACTIVATE commands to different banks is  $t_{RRD}$ .

**Figure 15: ACTIVATE Command**



- Notes:
1.  $t_{RCD} = 3$ ,  $t_{RP} = 3$ ,  $t_{RRD} = 2$ .
  2. A PRECHARGE ALL command uses  $t_{RPab}$  timing, and a single-bank PRECHARGE command uses  $t_{RPpb}$  timing. In this figure,  $t_{RP}$  is used to denote either an all-bank PRECHARGE or a single-bank PRECHARGE.

### 8-Bank Device Operation

Two rules regarding 8-bank device operation must be observed: One rule restricts the number of sequential ACTIVATE commands that can be issued; the second rule provides additional RAS precharge time for a PRECHARGE ALL command.

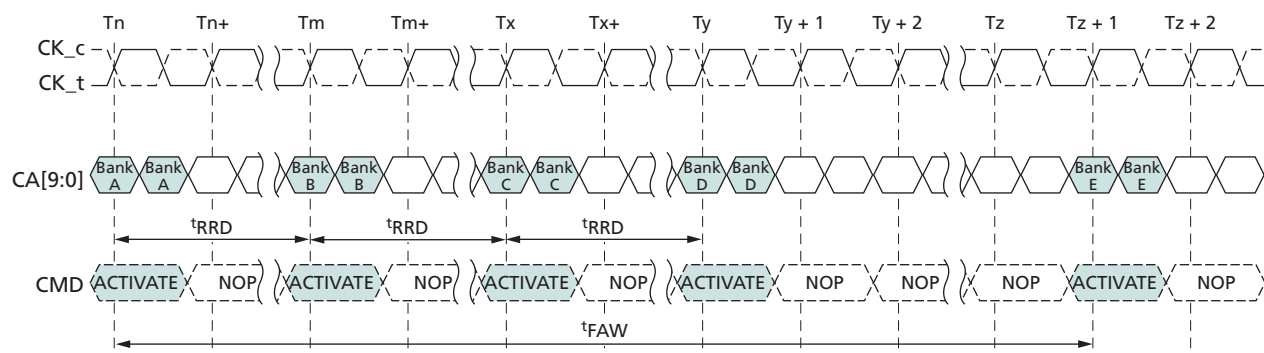
**The 8-Bank Device Sequential Bank Activation Restriction:** No more than four banks can be activated (or refreshed, in the case of REFpb) in a rolling  $t_{FAW}$  window. To convert to clocks, divide  $t_{FAW}[ns]$  by  $t_{CK}[ns]$ , and round up to the next integer value. For example, if  $RU(t_{FAW}/t_{CK})$  is 10 clocks, and an ACTIVATE command is issued in clock  $n$ , no more than three further ACTIVATE commands can be issued at or between clock  $n + 1$  and  $n + 9$ . REFpb also counts as bank activation for purposes of  $t_{FAW}$ .

**The 8-Bank Device PRECHARGE ALL Provision:**  $t_{RP}$  for a PRECHARGE ALL command must equal  $t_{RPab}$ , which is greater than  $t_{RPpb}$ .



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Read and Write Access Modes

Figure 16:  $t_{FAW}$  Timing (8-Bank Devices)



Note: 1. Exclusively for 8-bank devices.

## Read and Write Access Modes

After a bank is activated, a READ or WRITE command can be issued with CS<sub>n</sub> LOW, CA0 HIGH, and CA1 LOW at the rising edge of the clock. CA2 must also be defined at this time to determine whether the access cycle is a READ operation (CA2 HIGH) or a WRITE operation (CA2 LOW). A single READ or WRITE command initiates a burst READ or burst WRITE operation on successive clock cycles.

A new burst access must not interrupt the previous 4-bit burst operation when BL = 4. When BL = 8 or BL = 16, a READ can be interrupted by a READ and a WRITE can be interrupted by a WRITE, provided that the interrupt occurs on a 4-bit boundary and that  $t_{CCD}$  is met.

## Burst READ Command

The burst READ command is initiated with CS# LOW, CA0 HIGH, CA1 LOW, and CA2 HIGH at the rising edge of the clock. The command address bus inputs, CA5<sub>r</sub>–CA6<sub>r</sub> and CA1<sub>f</sub>–CA9<sub>f</sub>, determine the starting column address for the burst. The read latency (RL) is defined from the rising edge of the clock on which the READ command is issued to the rising edge of the clock from which the  $t_{DQSCK}$  delay is measured. The first valid data is available  $RL \times t_{CK} + t_{DQSCK} + t_{DQSQ}$  after the rising edge of the clock when the READ command is issued. The data strobe output is driven LOW  $t_{RPRE}$  before the first valid rising strobe edge. The first bit of the burst is synchronized with the first rising edge of the data strobe. Each subsequent data-out appears on each DQ pin, edge-aligned with the data strobe. The RL is programmed in the mode registers.

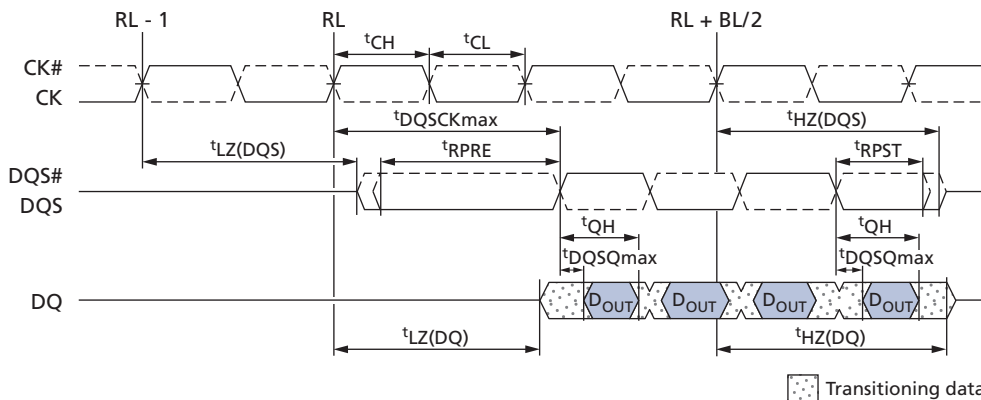
Pin input timings for the data strobe are measured relative to the crosspoint of DQS and its complement, DQS#.





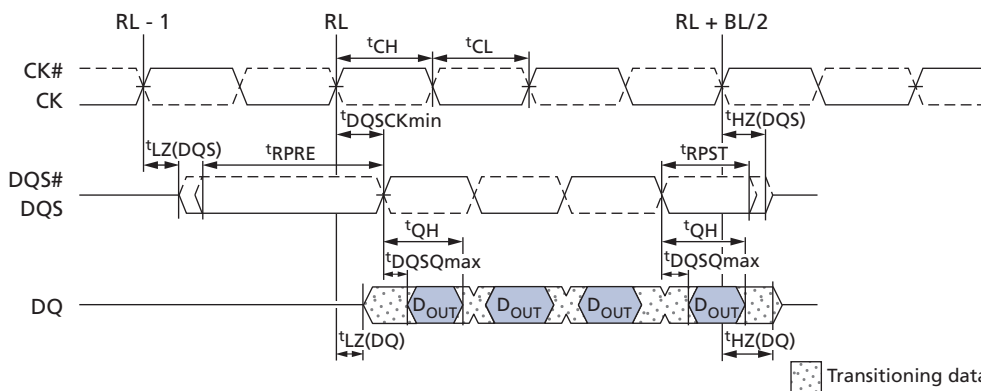
## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Burst READ Command

**Figure 17: READ Output Timing –  $t_{DQSK} (MAX)$**



- Notes: 1.  $t_{DQSK}$  can span multiple clock periods.  
2. An effective burst length of 4 is shown.

**Figure 18: READ Output Timing –  $t_{DQSK} (MIN)$**

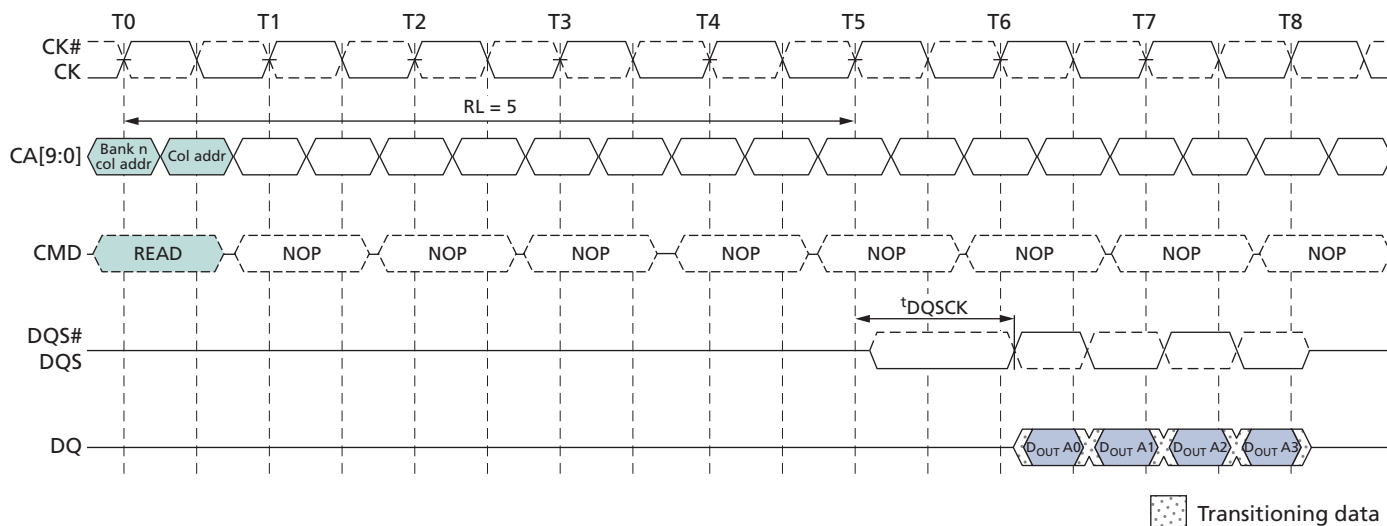


- Note: 1. An effective burst length of 4 is shown.

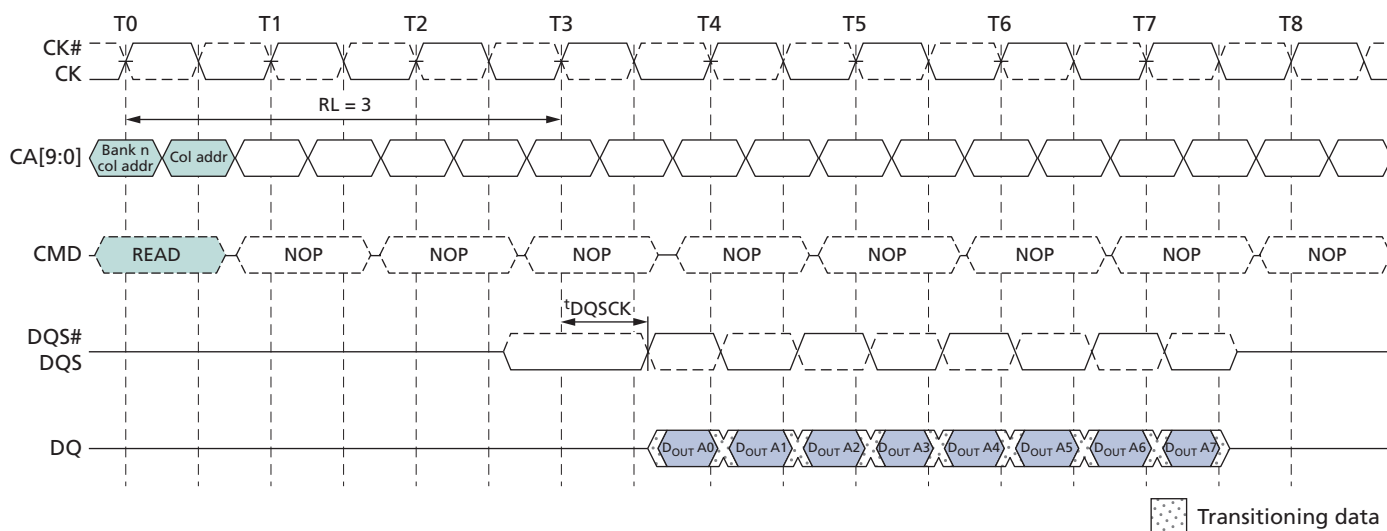


## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Burst READ Command

**Figure 19: Burst READ – RL = 5, BL = 4,  $t_{DQSCK} > t_{CK}$**



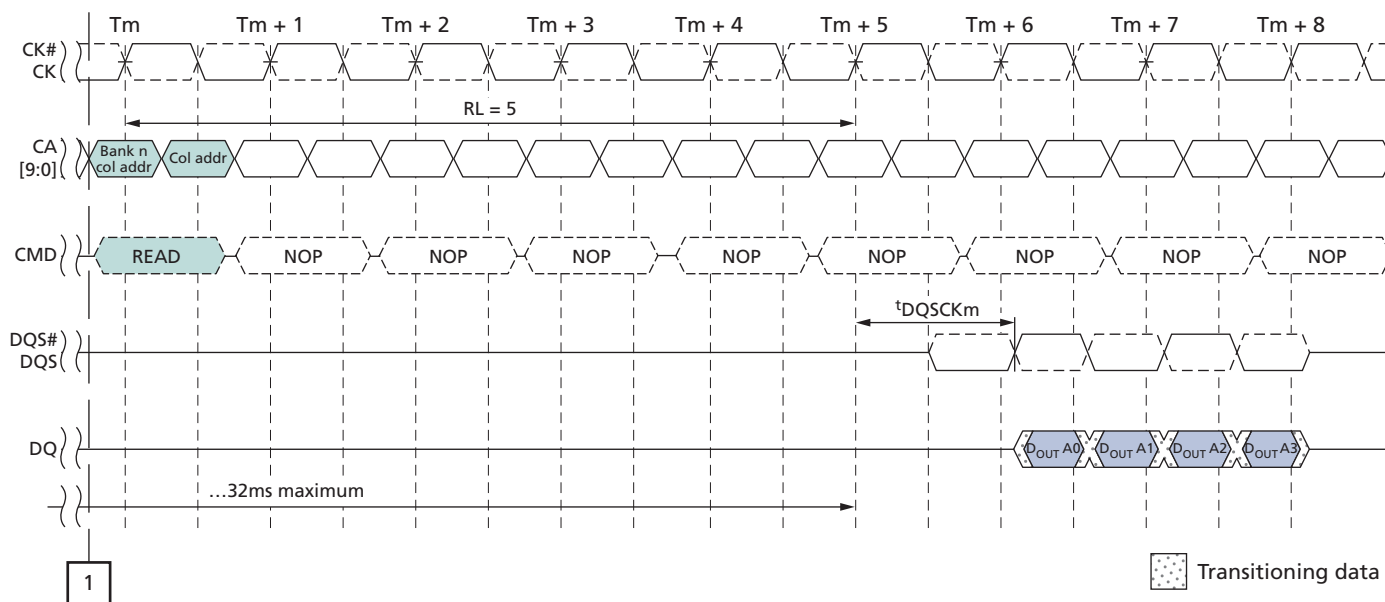
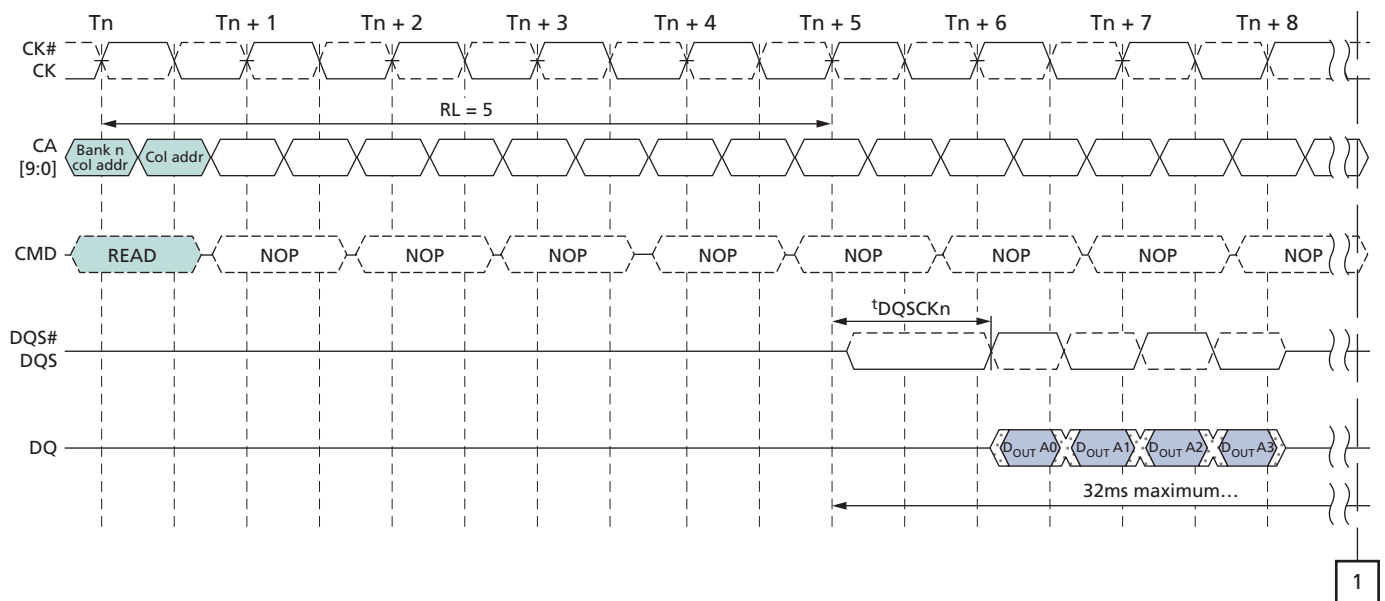
**Figure 20: Burst READ – RL = 3, BL = 8,  $t_{DQSCK} < t_{CK}$**





# 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Burst READ Command

Figure 21:  $t_{DQSKDL}$  Timing

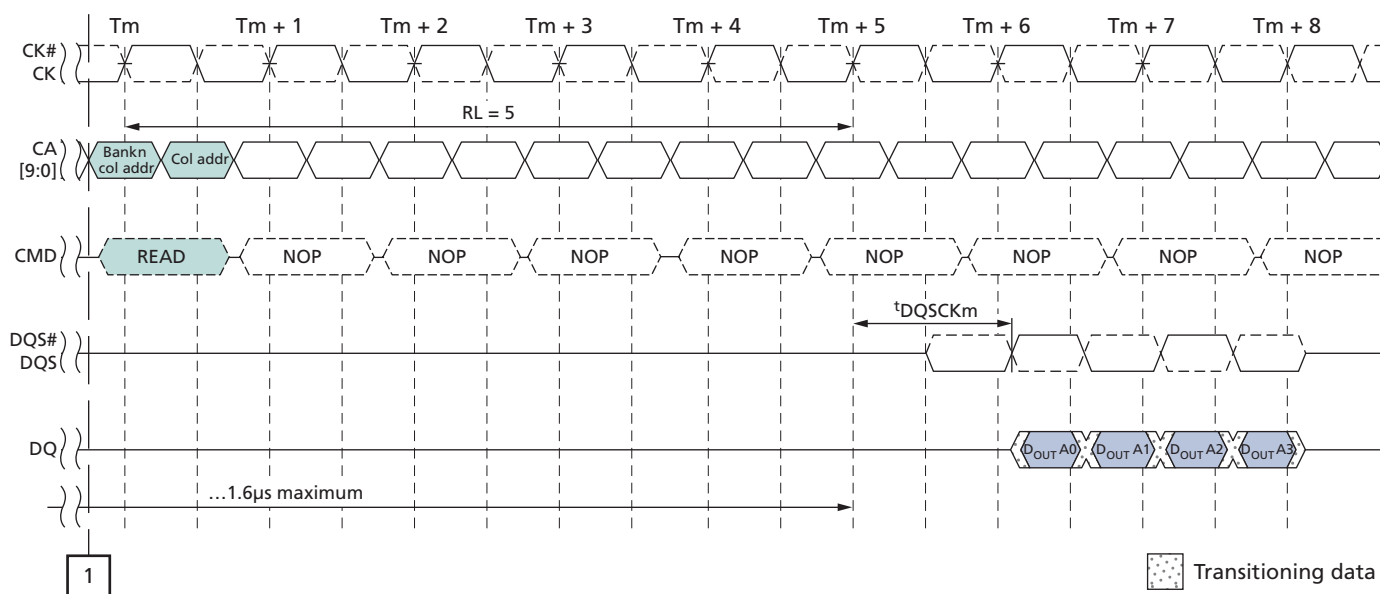
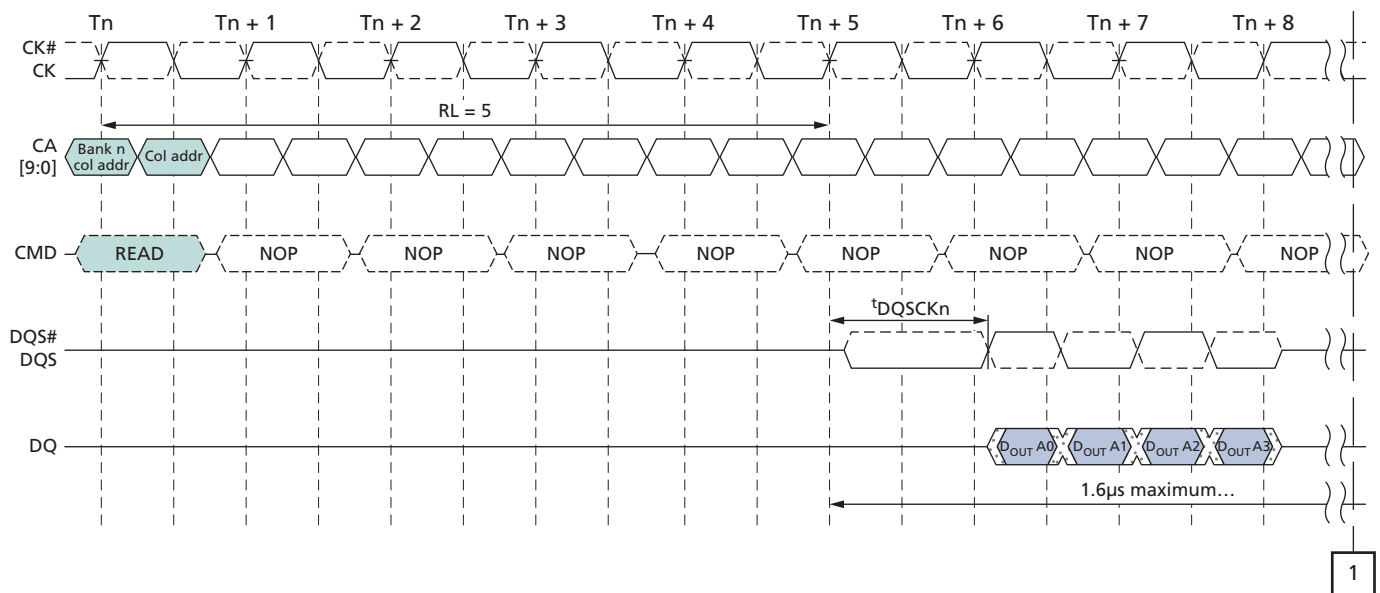


- Notes:
1.  $t_{DQSKDL} = (t_{DQSKn} - t_{DQSKm})$ .
  2.  $t_{DQSKDL} (MAX)$  is defined as the maximum of ABS ( $t_{DQSKn} - t_{DQSKm}$ ) for any ( $t_{DQSKn}$ ,  $t_{DQSKm}$ ) pair within any 32ms rolling window.



# 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Burst READ Command

Figure 22:  $t_{DQSKDM}$  Timing

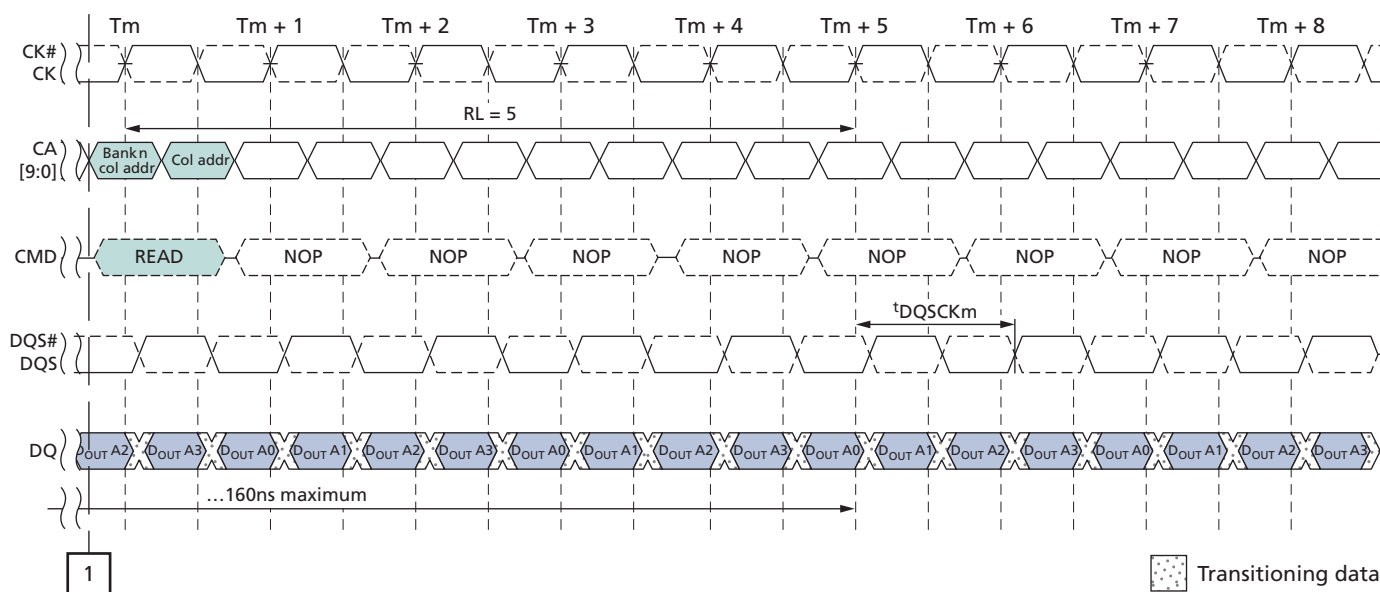
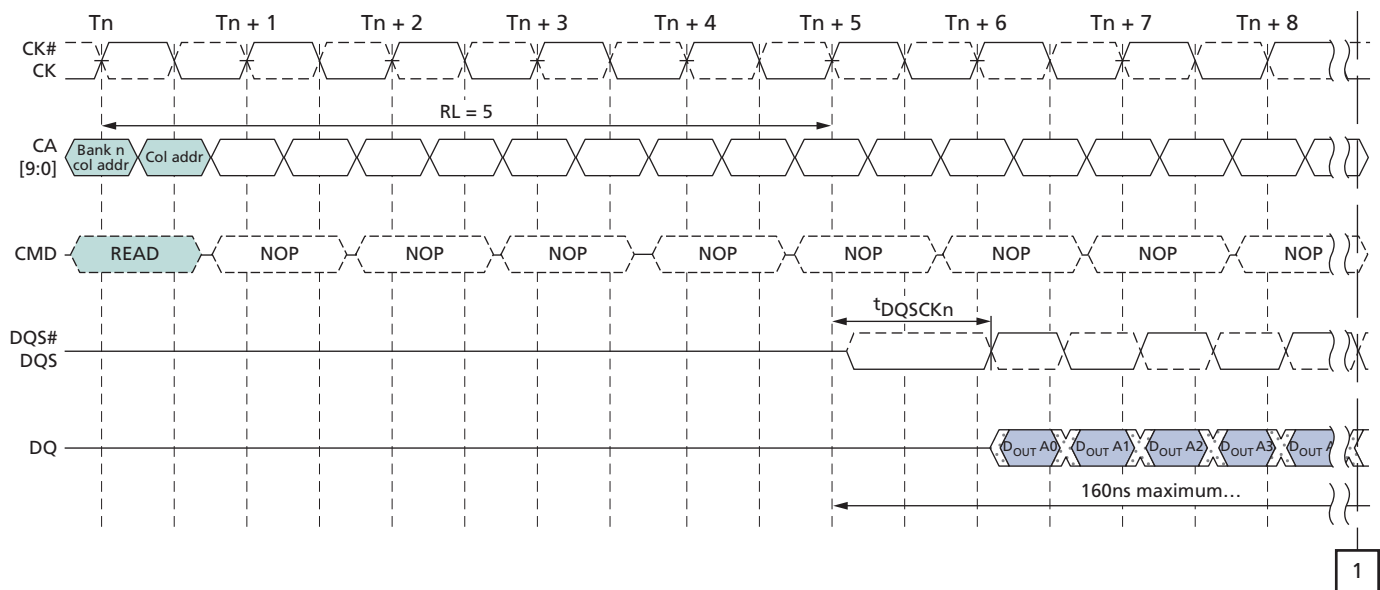


- Notes:
1.  $t_{DQSKDM} = (t_{DQSKn} - t_{DQSKm})$ .
  2.  $t_{DQSKDM} (MAX)$  is defined as the maximum of ABS ( $t_{DQSKn} - t_{DQSKm}$ ) for any ( $t_{DQSKn}, t_{DQSKm}$ ) pair within any  $1.6\mu s$  rolling window.



# 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Burst READ Command

Figure 23:  $t_{DQCKDS}$  Timing

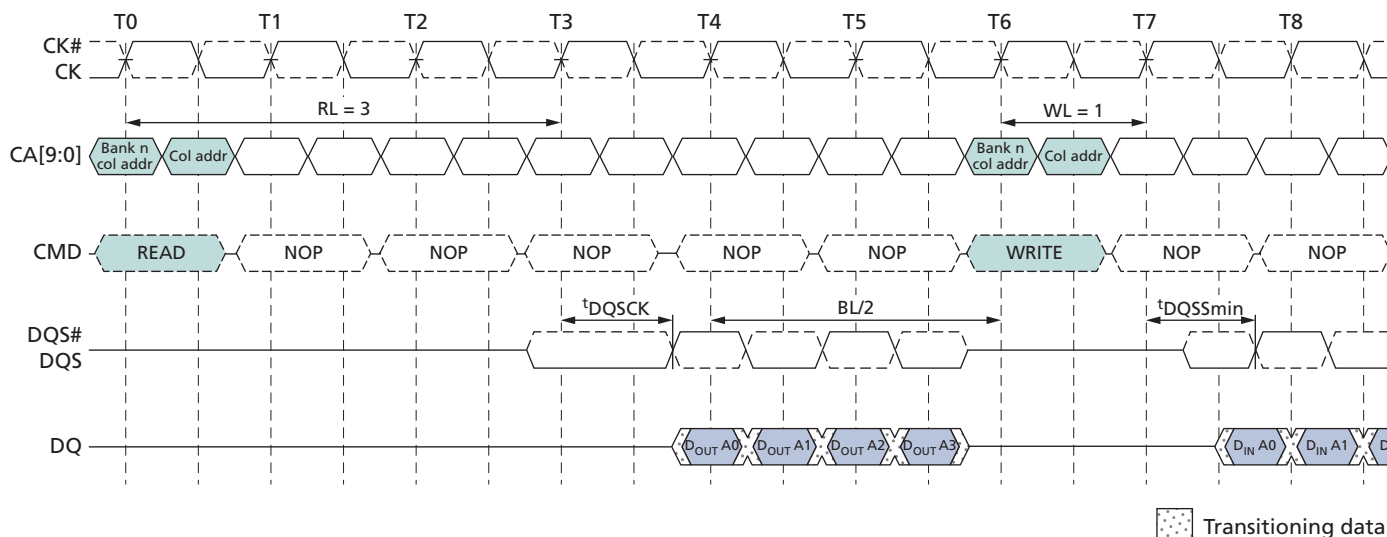


- Notes:
1.  $t_{DQCKDS} = (t_{DQCKn} - t_{DQCKm})$ .
  2.  $t_{DQCKDS} (MAX)$  is defined as the maximum of ABS ( $t_{DQCKn} - t_{DQCKm}$ ) for any ( $t_{DQCKn}$ ,  $t_{DQCKm}$ ) pair for READs within a consecutive burst, within any 160ns rolling window.



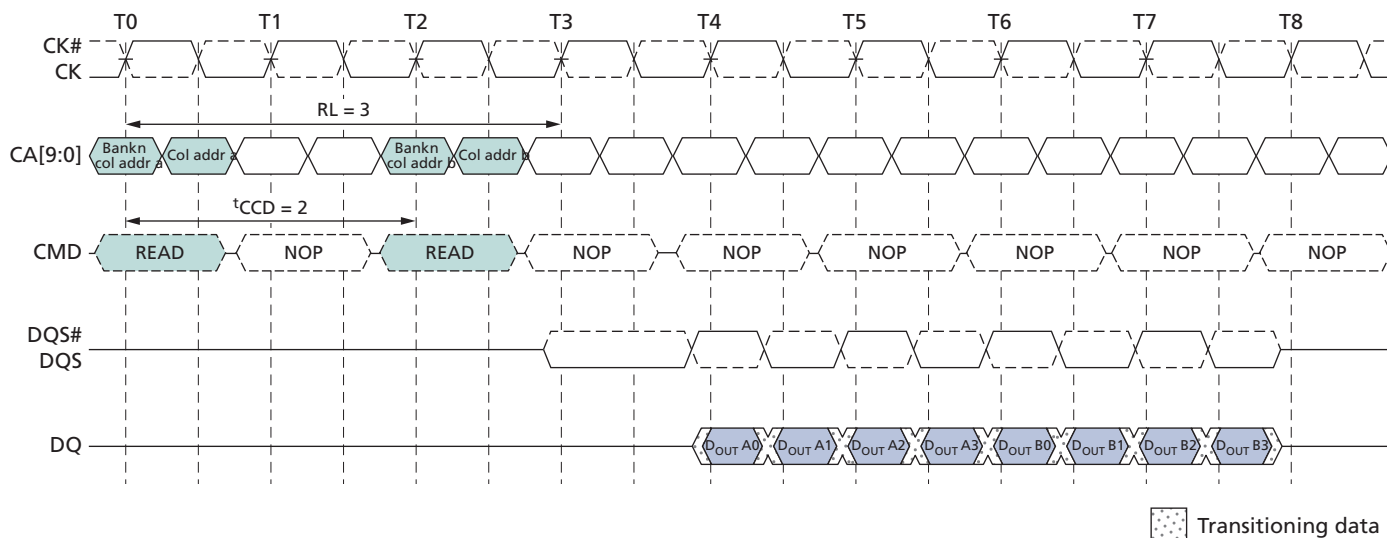
## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Burst READ Command

**Figure 24: Burst READ Followed by Burst WRITE – RL = 3, WL = 1, BL = 4**



The minimum time from the burst READ command to the burst WRITE command is defined by the read latency (RL) and the burst length (BL). Minimum READ-to-WRITE latency is  $RL + RU(t_{DQSCk}(MAX)/t_{CK}) + BL/2 + 1 - WL$  clock cycles. Note that if a READ burst is truncated with a burst TERMINATE (BST) command, the effective burst length of the truncated READ burst should be used for BL when calculating the minimum READ-to-WRITE delay.

**Figure 25: Seamless Burst READ – RL = 3, BL = 4, t<sub>CCD</sub> = 2**



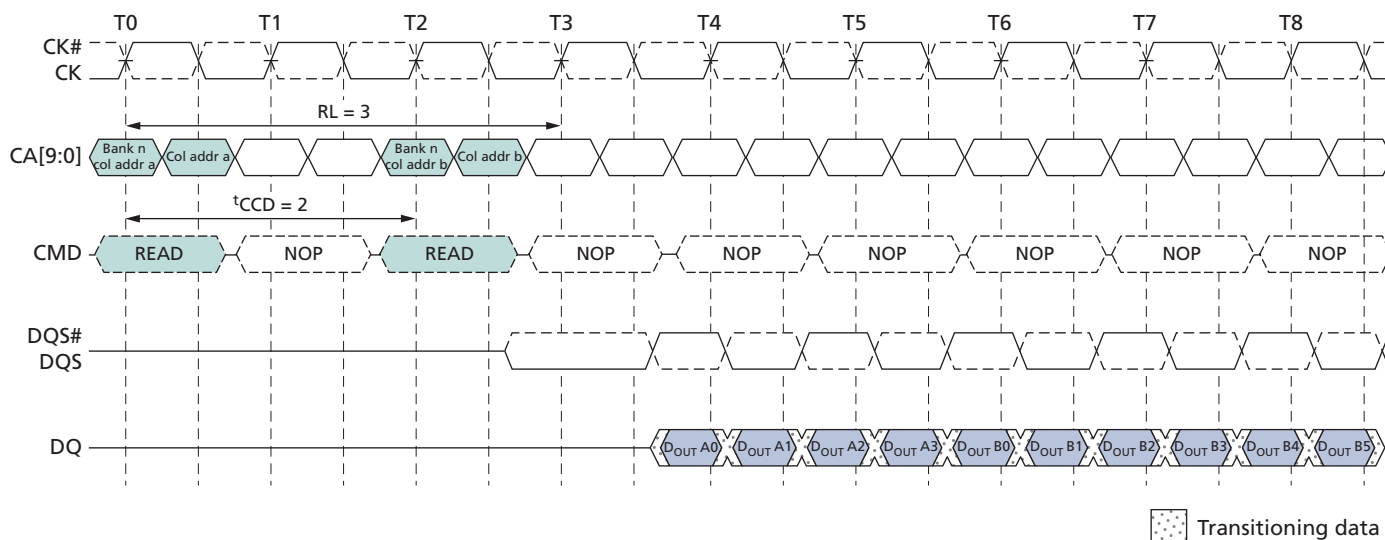
A seamless burst READ operation is supported by enabling a READ command at every other clock cycle for BL = 4 operation, every fourth clock cycle for BL = 8 operation, and every eighth clock cycle for BL = 16 operation. This operation is supported as long as the banks are activated, whether the accesses read the same or different banks.



### READs Interrupted by a READ

A burst READ can be interrupted by another READ with a 4-bit burst boundary, provided that  $t_{CCD}$  is met.

**Figure 26: READ Burst Interrupt Example – RL = 3, BL = 8,  $t_{CCD} = 2$**



Note: 1. READs can only be interrupted by other READs or the BST command.

### Burst WRITE Command

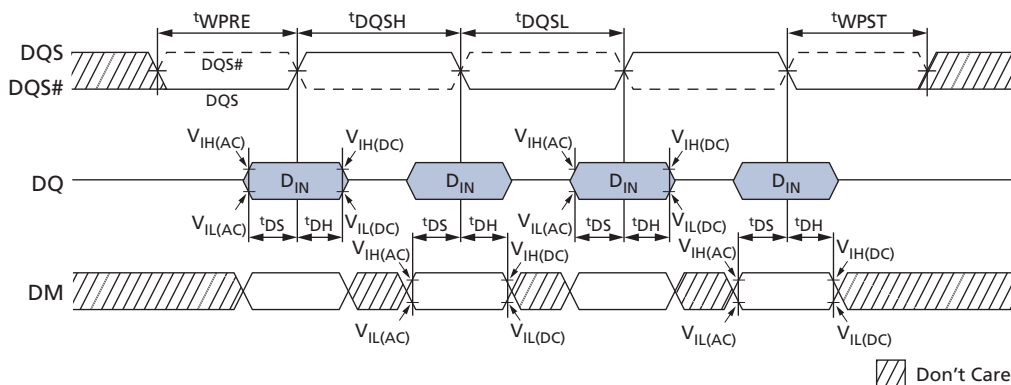
The burst WRITE command is initiated with CS# LOW, CA0 HIGH, CA1 LOW, and CA2 LOW at the rising edge of the clock. The command address bus inputs, CA5r–CA6r and CA1f–CA9f, determine the starting column address for the burst. Write latency (WL) is defined from the rising edge of the clock on which the WRITE command is issued to the rising edge of the clock from which the  $t_{DQSS}$  delay is measured. The first valid data must be driven  $WL \times t_{CK} + t_{DQSS}$  from the rising edge of the clock from which the WRITE command is issued. The data strobe signal (DQS) must be driven LOW  $t_{WPRE}$  prior to data input. The burst cycle data bits must be applied to the DQ pins  $t_{DS}$  prior to the associated edge of the DQS and held valid until  $t_{DH}$  after that edge. Burst data is sampled on successive edges of the DQS until the 4-, 8-, or 16-bit burst length is completed. After a burst WRITE operation,  $t_{WR}$  must be satisfied before a PRECHARGE command to the same bank can be issued.

Pin input timings are measured relative to the crosspoint of DQS and its complement, DQS#.

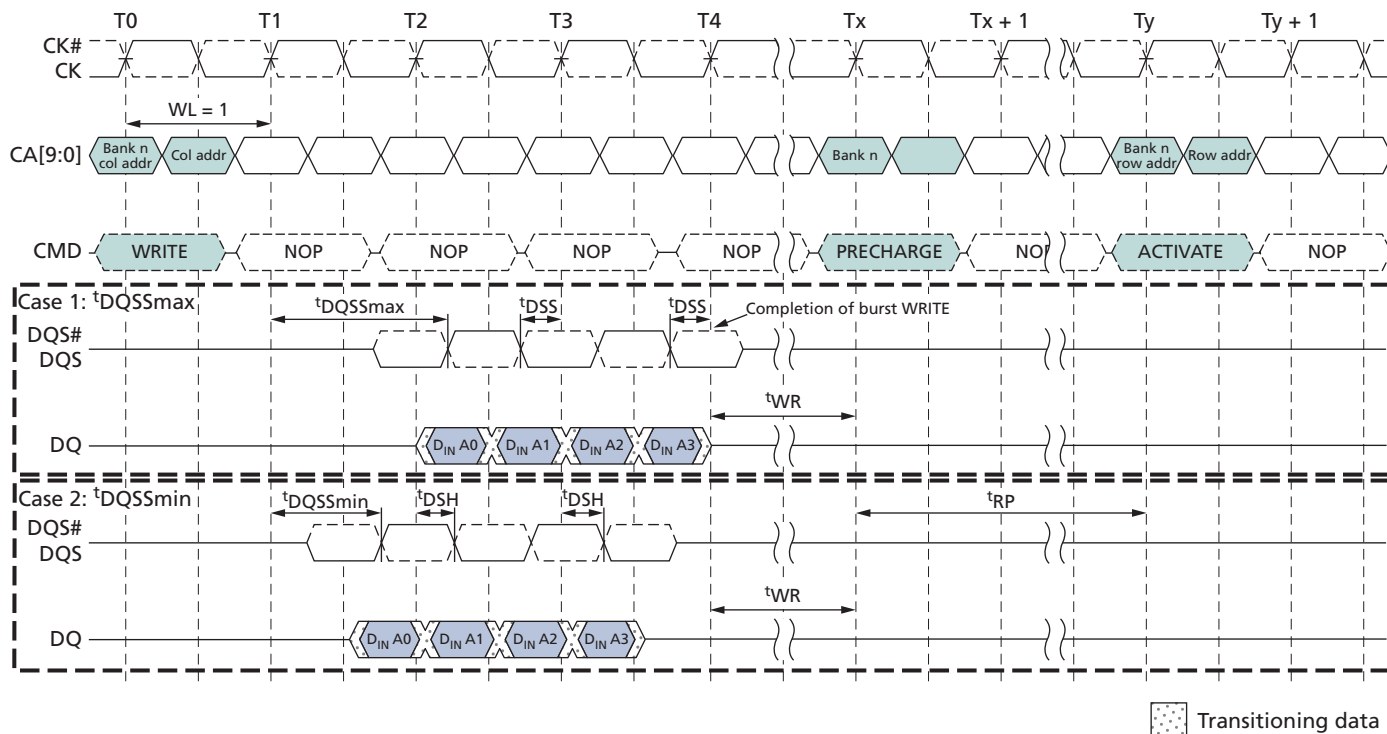


## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Burst WRITE Command

**Figure 27: Data Input (WRITE) Timing**



**Figure 28: Burst WRITE – WL = 1, BL = 4**

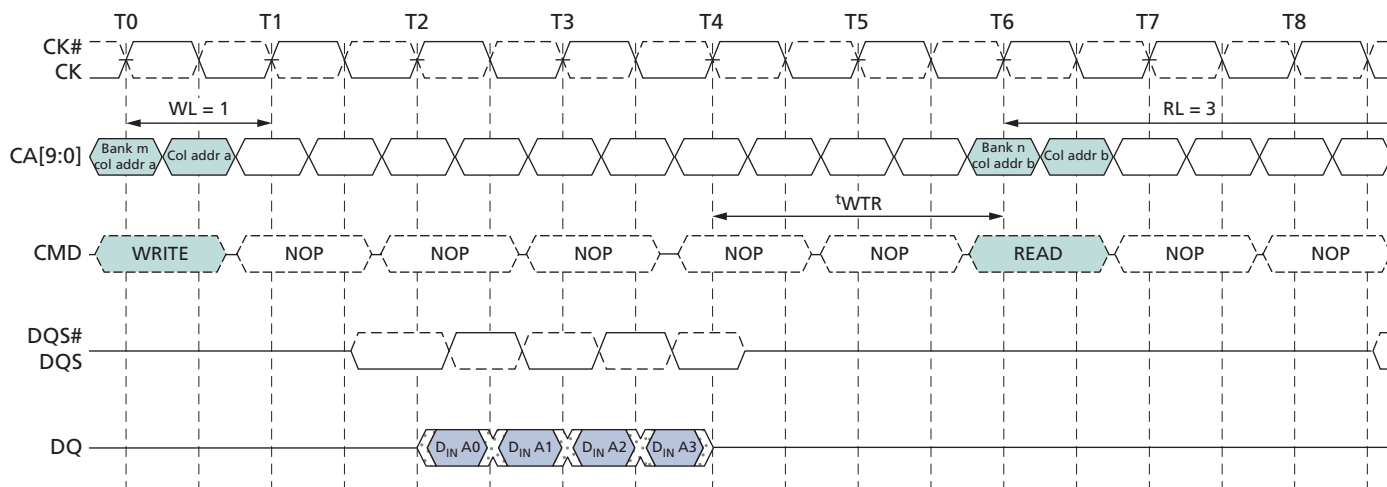






## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Burst WRITE Command

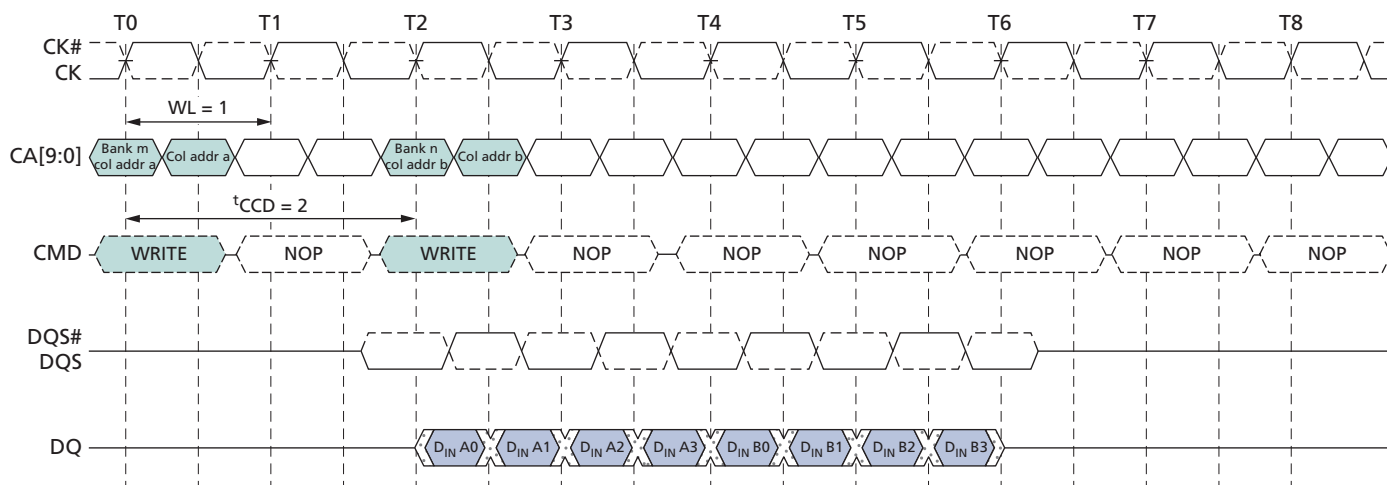
**Figure 29: Burst WRITE Followed by Burst READ – RL = 3, WL = 1, BL = 4**



Transitioning data

- Notes:
1. The minimum number of clock cycles from the burst WRITE command to the burst READ command for any bank is  $[WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})]$ .
  2.  $t_{WTR}$  starts at the rising edge of the clock after the last valid input data.
  3. If a WRITE burst is truncated with a BST command, the effective burst length of the truncated WRITE burst should be used as BL to calculate the minimum WRITE-to-READ delay.

**Figure 30: Seamless Burst WRITE – WL = 1, BL = 4,  $t_{CCD} = 2$**



Transitioning data

- Note:
1. The seamless burst WRITE operation is supported by enabling a WRITE command every other clock for BL = 4 operation, every four clocks for BL = 8 operation, or every eight clocks for BL = 16 operation. This operation is supported for any activated bank.



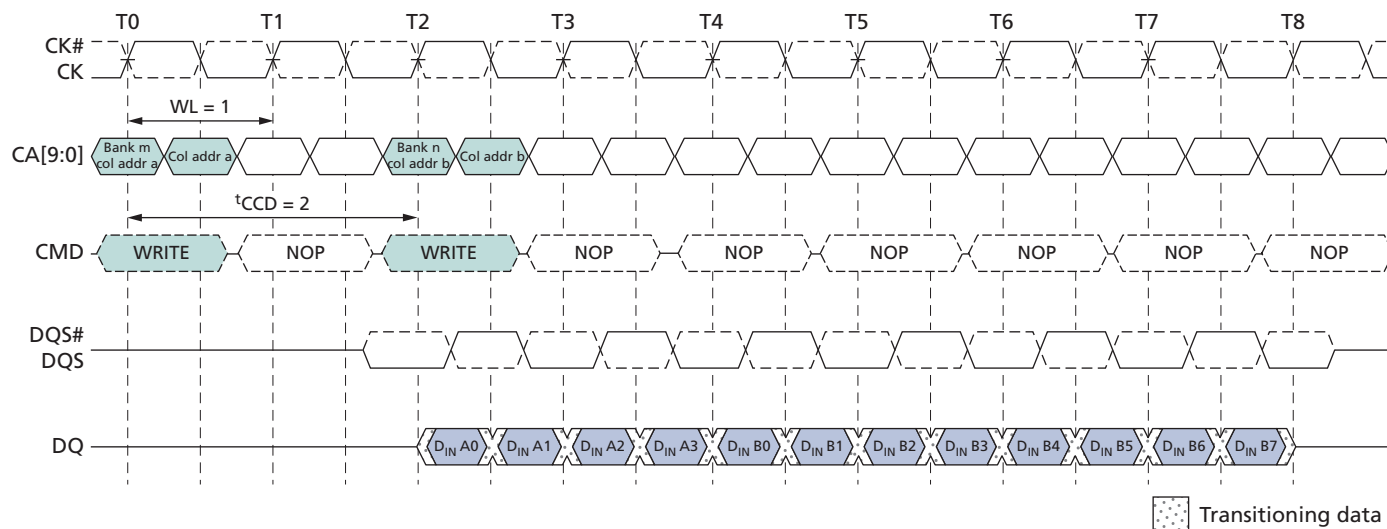
## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM BURST TERMINATE Command

### WRITES Interrupted by a WRITE

A burst WRITE can only be interrupted by another WRITE with a 4-bit burst boundary, provided that  $t_{CCD}$  (MIN) is met.

A WRITE burst interrupt can occur on even clock cycles after the initial WRITE command, provided that  $t_{CCD}$  (MIN) is met.

**Figure 31: WRITE Burst Interrupt Timing – WL = 1, BL = 8,  $t_{CCD} = 2$**



- Notes:
1. WRITES can only be interrupted by other WRITES or the BST command.
  2. The effective burst length of the first WRITE equals two times the number of clock cycles between the first WRITE and the interrupting WRITE.

### BURST TERMINATE Command

The BURST TERMINATE (BST) command is initiated with CS\_n LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 LOW at the rising edge of the clock. A BST command can be issued only to terminate an active READ or WRITE burst. Therefore, a BST command can be issued only up to and including  $BL/2 - 1$  clock cycles after a READ or WRITE command. The effective burst length of a READ or WRITE command truncated by a BST command is as follows:

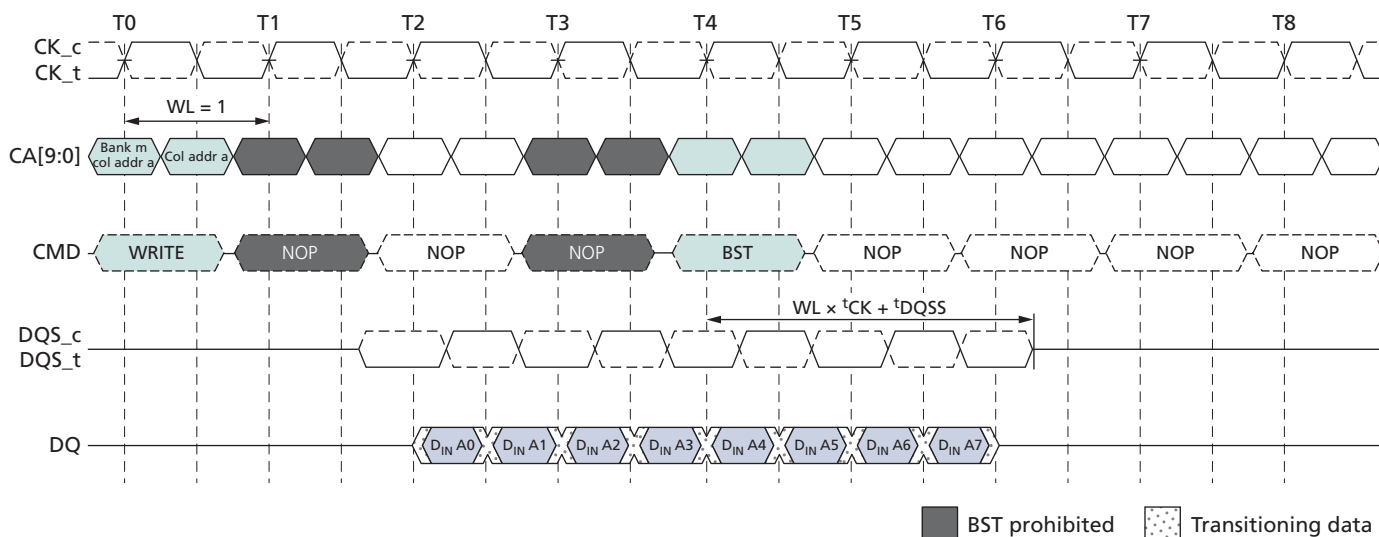
- Effective burst length =  $2 \times$  (number of clock cycles from the READ or WRITE command to the BST command).
- If a READ or WRITE burst is truncated with a BST command, the effective burst length of the truncated burst should be used for BL when calculating the minimum READ-to-WRITE or WRITE-to-READ delay.
- The BST command only affects the most recent READ or WRITE command. The BST command truncates an ongoing READ burst  $RL \times t_{CK} + t_{DQSCK} + t_{DQSQ}$  after the rising edge of the clock where the BST command is issued. The BST command truncates an ongoing WRITE burst  $WL \times t_{CK} + t_{DQSS}$  after the rising edge of the clock where the BST command is issued.



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM BURST TERMINATE Command

- The 4-bit prefetch architecture enables BST command assertion on even clock cycles following a WRITE or READ command. The effective burst length of a READ or WRITE command truncated by a BST command is thus an integer multiple of four.

**Figure 32: Burst WRITE Truncated by BST – WL = 1, BL = 16**

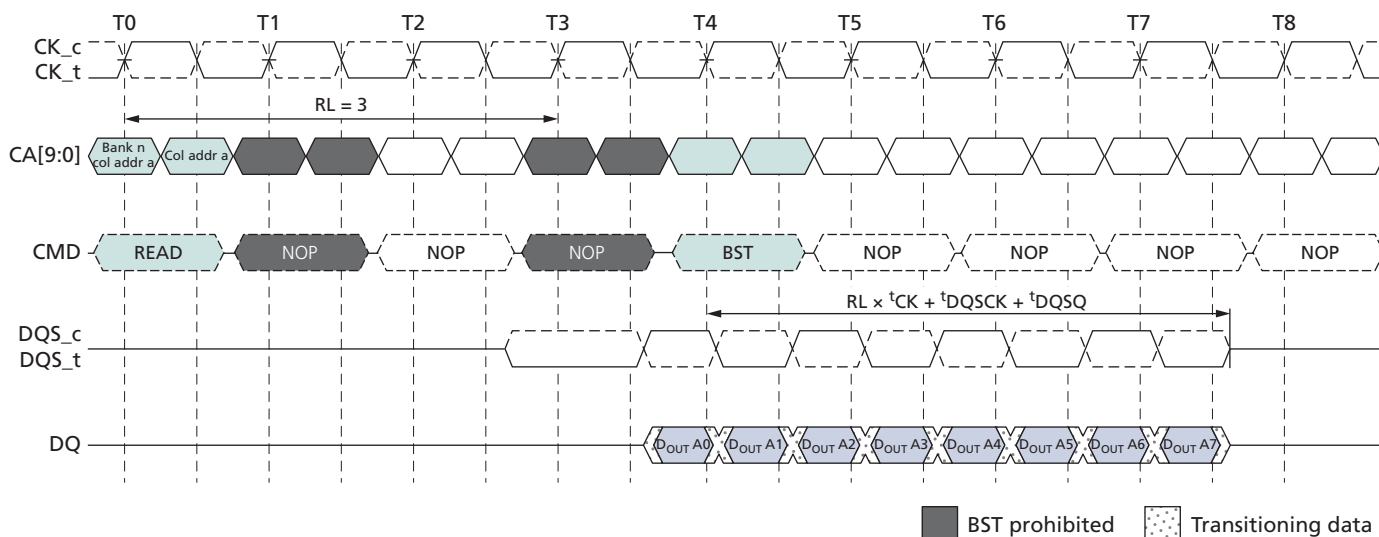


- Notes:
- The BST command truncates an ongoing WRITE burst  $WL \times t_{CK} + t_{DQSS}$  after the rising edge of the clock where the BST command is issued.
  - BST can only be issued an even number of clock cycles after the WRITE command.
  - Additional BST commands are not supported after T4 and must not be issued until after the next READ or WRITE command.



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Write Data Mask

**Figure 33: Burst READ Truncated by BST – RL = 3, BL = 16**

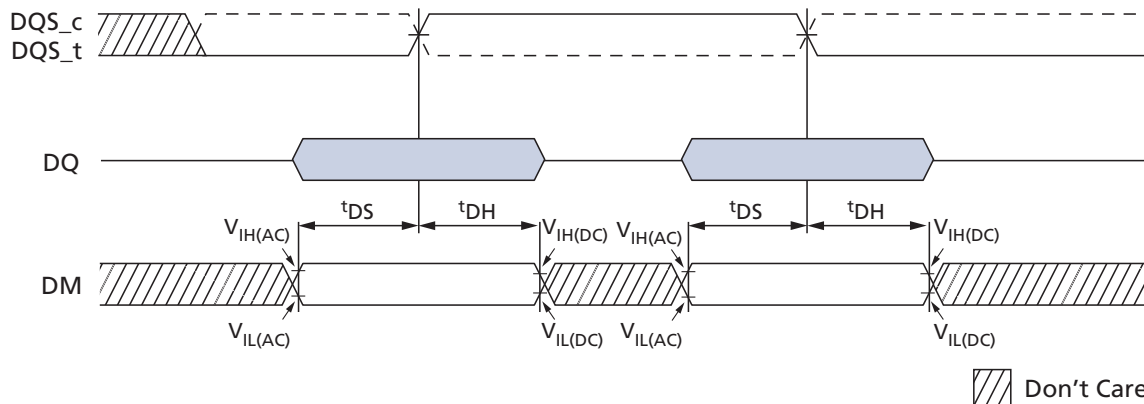


- Notes:
1. The BST command truncates an ongoing READ burst ( $RL \times t_{CK} + t_{DQSK} + t_{DQSQ}$ ) after the rising edge of the clock where the BST command is issued.
  2. BST can only be issued an even number of clock cycles after the READ command.
  3. Additional BST commands are not supported after T4 and must not be issued until after the next READ or WRITE command.

## Write Data Mask

On the LPDDR2 device, one write data mask (DM) pin for each data byte (DQ) is supported, consistent with the implementation on LPDDR SDRAM. Each DM can mask its respective DQ for any given cycle of the burst. Data mask timings match data bit timing, but are inputs only. Internal data mask loading is identical to data bit loading to ensure matched system timing.

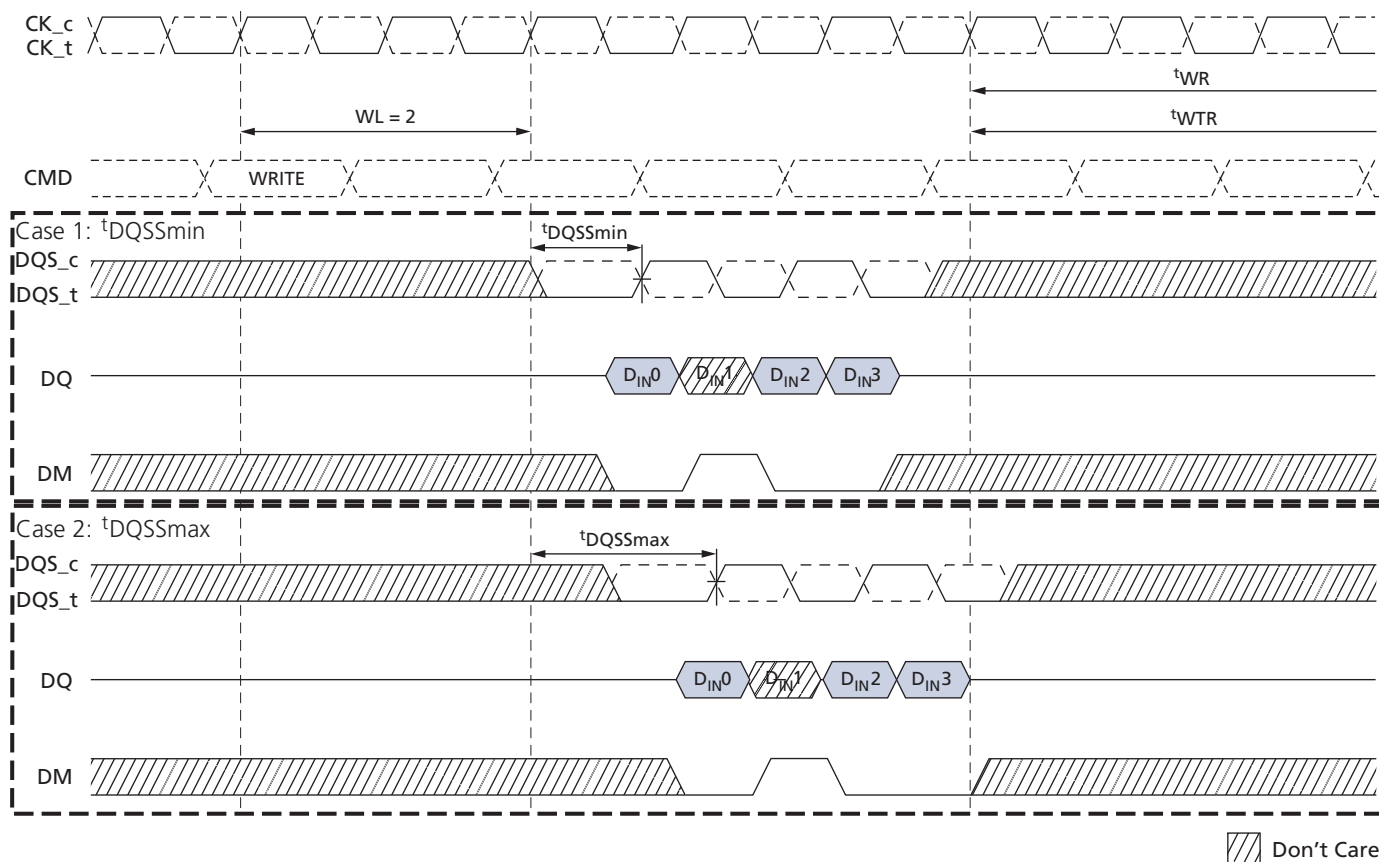
**Figure 34: Data Mask Timing**





## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM PRECHARGE Command

Figure 35: Write Data Mask – Second Data Bit Masked



Note: 1. For the data mask function, WL = 2, BL = 4 is shown; the second data bit is masked.

## PRECHARGE Command

The PRECHARGE command is used to precharge or close a bank that has been activated. The PRECHARGE command is initiated with CS<sub>n</sub> LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The PRECHARGE command can be used to precharge each bank independently or all banks simultaneously. For a 4-bank device, the AB flag and bank address bits BA0 and BA1 are used to determine which bank(s) to precharge. For an 8-bank device, the AB flag and the bank address bits BA0, BA1, and BA2 are used to determine which bank(s) to precharge. The precharged bank(s) will be available for subsequent row access  $t_{RPab}$  after an all bank PRECHARGE command is issued, or  $t_{RPpb}$  after a single-bank PRECHARGE command is issued.

To ensure that an 8-bank device can meet the instantaneous current demand required to operate, the row precharge time ( $t_{RP}$ ) for an all bank PRECHARGE in an 8-bank device ( $t_{RPab}$ ) will be longer than the row precharge time for a single-bank PRECHARGE ( $t_{RPpb}$ ). For a 4-bank device,  $t_{RPab}$  is equal to  $t_{RPpb}$ .

ACTIVATE to PRECHARGE timing is shown in ACTIVATE Command.



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM PRECHARGE Command

**Table 50: Bank Selection for PRECHARGE by Address Bits**

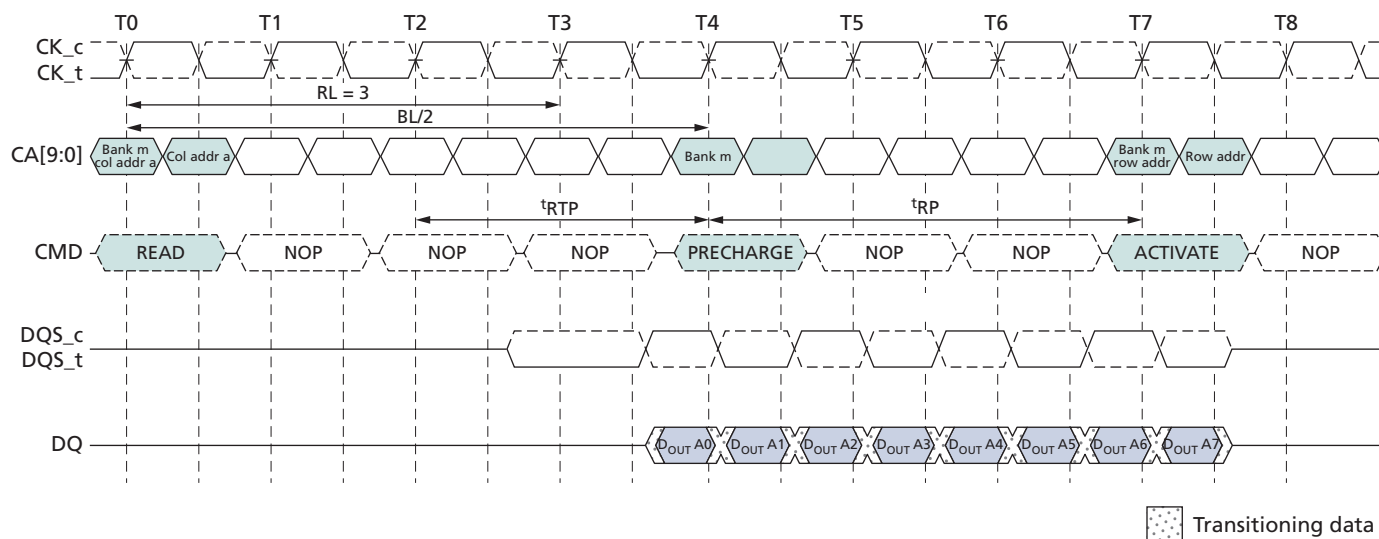
AB (CA4r)	BA2 (CA9r)	BA1 (CA8r)	BA0 (CA7r)	Precharged Bank(s) 4-Bank Device	Precharged Bank(s) 8-Bank Device
0	0	0	0	Bank 0 only	Bank 0 only
0	0	0	1	Bank 1 only	Bank 1 only
0	0	1	0	Bank 2 only	Bank 2 only
0	0	1	1	Bank 3 only	Bank 3 only
0	1	0	0	Bank 0 only	Bank 4 only
0	1	0	1	Bank 1 only	Bank 5 only
0	1	1	0	Bank 2 only	Bank 6 only
0	1	1	1	Bank 3 only	Bank 7 only
1	Don't Care	Don't Care	Don't Care	All banks	All banks

### READ Burst Followed by PRECHARGE

For the earliest possible precharge, the PRECHARGE command can be issued BL/2 clock cycles after a READ command. A new bank ACTIVATE command can be issued to the same bank after the row precharge time ( $t_{RP}$ ) has elapsed. A PRECHARGE command cannot be issued until after  $t_{RAS}$  is satisfied.

The minimum READ-to-PRECHARGE time ( $t_{RTP}$ ) must also satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefetch of a READ command.  $t_{RTP}$  begins BL/2 - 2 clock cycles after the READ command.

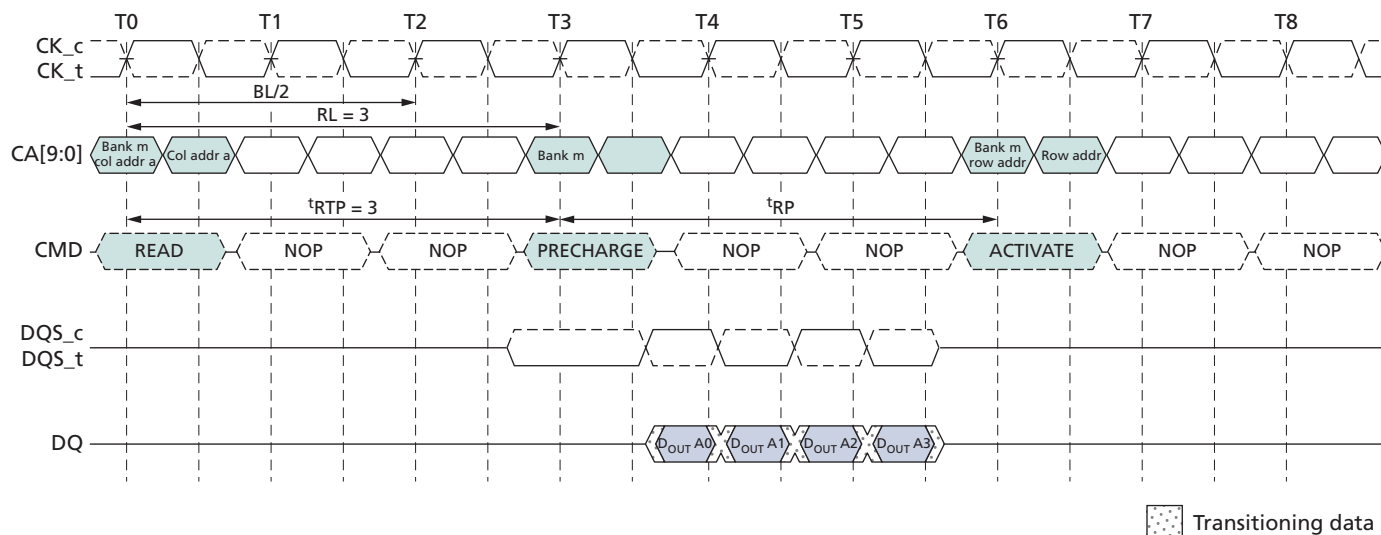
If the burst is truncated by a BST command, the effective BL value is used to calculate when  $t_{RTP}$  begins.

**Figure 36: READ Burst Followed by PRECHARGE – RL = 3, BL = 8,  $RU(t_{RTP(MIN)}/t_{CK}) = 2$** 




## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM PRECHARGE Command

**Figure 37: READ Burst Followed by PRECHARGE – RL = 3, BL = 4,  $RU(t_{RTP}(\text{MIN})/t_{CK}) = 3$**



### WRITE Burst Followed by PRECHARGE

For WRITE cycles, a WRITE recovery time ( $t_{WR}$ ) must be provided before a PRECHARGE command can be issued.  $t_{WR}$  delay is referenced from the completion of the burst WRITE. The PRECHARGE command must not be issued prior to the  $t_{WR}$  delay. For WRITE-to-PRECHARGE timings, see the PRECHARGE and Auto Precharge Clarification table.

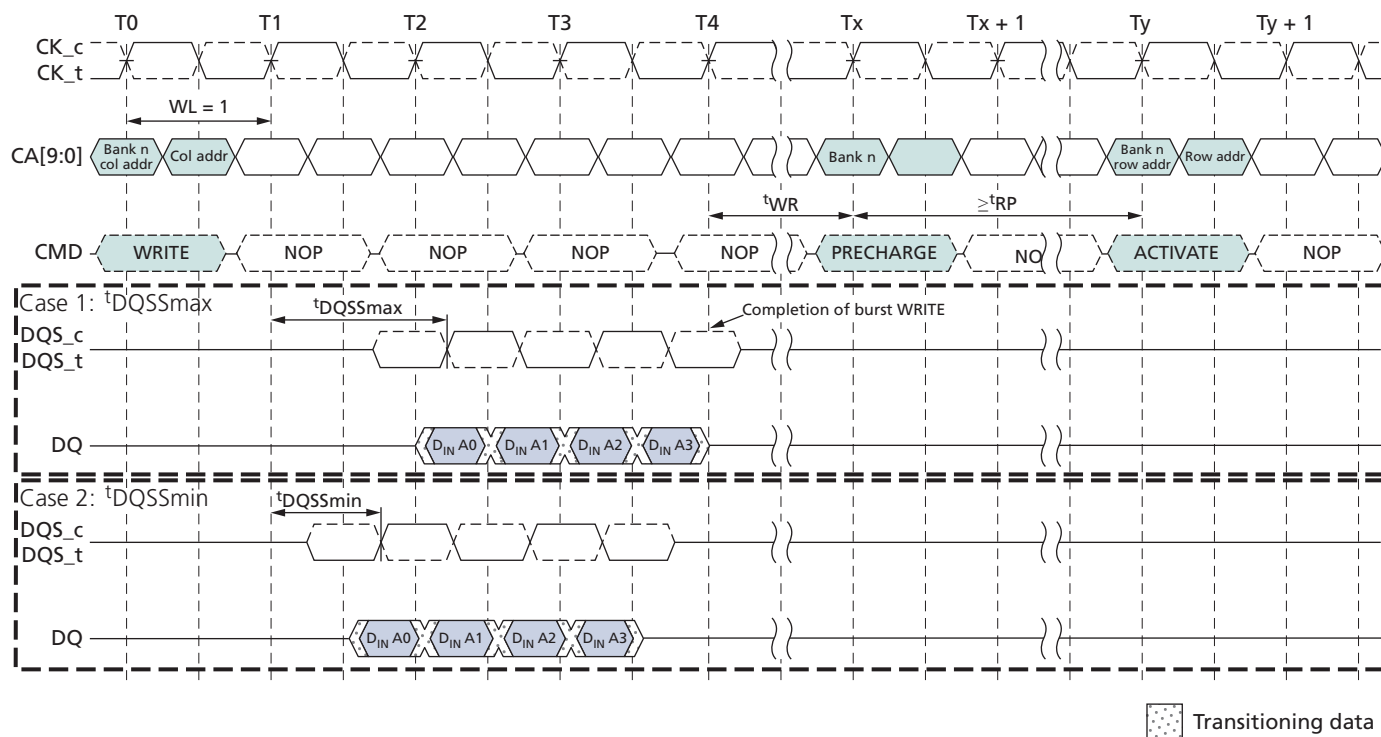
These devices write data to the array in prefetch quadruples (prefetch = 4). An internal WRITE operation can only begin after a prefetch group has been completely latched.

The minimum WRITE-to-PRECHARGE time for commands to the same bank is  $WL + BL/2 + 1 + RU(t_{WR}/t_{CK})$  clock cycles. For untruncated bursts, BL is the value set in the mode register. For truncated bursts, BL is the effective burst length.



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM PRECHARGE Command

**Figure 38: WRITE Burst Followed by PRECHARGE – WL = 1, BL = 4**



### Auto Precharge operation

Before a new row can be opened in an active bank, the active bank must be precharged using either the PRECHARGE command or the auto precharge function. When a READ or WRITE command is issued to the device, the auto precharge bit (AP) can be set to enable the active bank to automatically begin precharge at the earliest possible moment during the burst READ or WRITE cycle.

If AP is LOW when the READ or WRITE command is issued, then normal READ or WRITE burst operation is executed and the bank remains active at the completion of the burst.

If AP is HIGH when the READ or WRITE command is issued, the auto precharge function is engaged. This feature enables the PRECHARGE operation to be partially or completely hidden during burst READ cycles (dependent upon READ or WRITE latency), thus improving system performance for random data access.

### READ Burst with Auto Precharge

If AP (CA0f) is HIGH when a READ command is issued, the READ with auto precharge function is engaged.

This device starts an auto precharge on the rising edge of the clock BL/2 or BL/2 - 2 + RU ( $t_{RTP}/t_{CK}$ ) clock cycles later than the READ with auto precharge command, whichever is greater. For auto precharge calculations, see the PRECHARGE and Auto Precharge Clarification table.



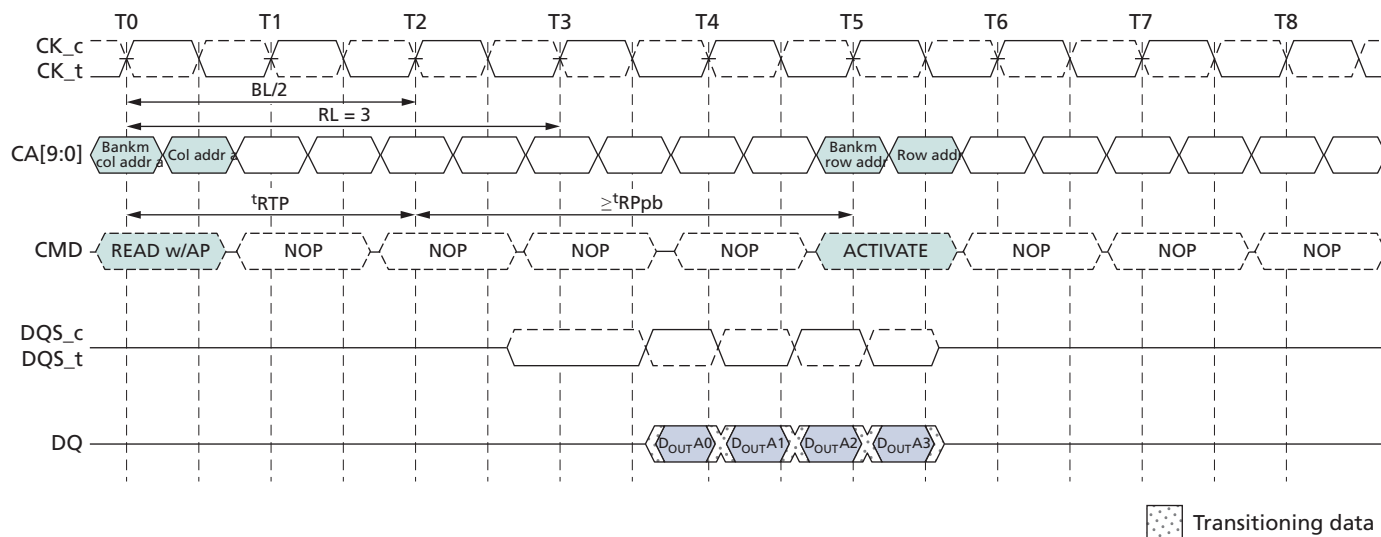


## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM PRECHARGE Command

Following an auto precharge operation, an ACTIVATE command can be issued to the same bank if the following two conditions are satisfied simultaneously:

- The RAS precharge time ( $t_{RP}$ ) has been satisfied from the clock at which the auto precharge begins.
- The RAS cycle time ( $t_{RC}$ ) from the previous bank activation has been satisfied.

**Figure 39: READ Burst with Auto Precharge – RL = 3, BL = 4,  $RU(t_{RTP(MIN)}/t_{CK}) = 2$**



### WRITE Burst with Auto Precharge

If AP (CA0f) is HIGH when a WRITE command is issued, the WRITE with auto precharge function is engaged. The device starts an auto precharge at the clock rising edge  $t_{WR}$  cycles after the completion of the burst WRITE.

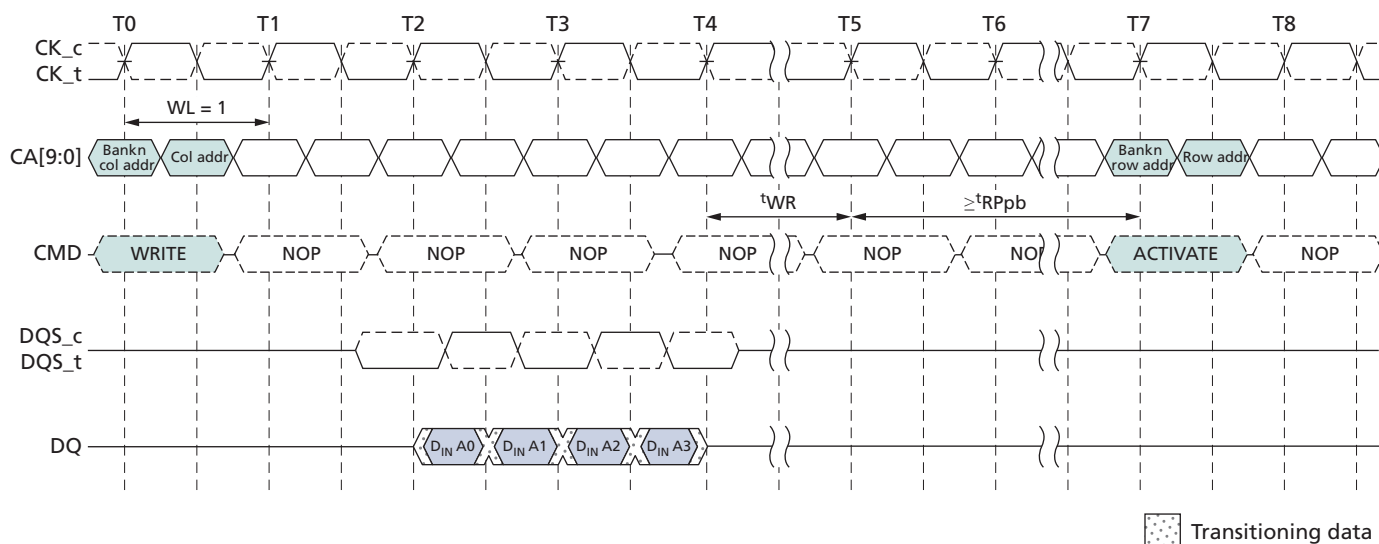
Following a WRITE with auto precharge, an ACTIVATE command can be issued to the same bank if the following two conditions are met:

- The RAS precharge time ( $t_{RP}$ ) has been satisfied from the clock at which the auto precharge begins.
- The RAS cycle time ( $t_{RC}$ ) from the previous bank activation has been satisfied.



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM PRECHARGE Command

**Figure 40: WRITE Burst with Auto Precharge – WL = 1, BL = 4**



**Table 51: PRECHARGE and Auto Precharge Clarification**

From Command	To Command	Minimum Delay Between Commands	Unit	Notes
READ	PRECHARGE to same bank as READ	$BL/2 + \text{MAX}(2, RU(t_{RTP}/t_{CK})) - 2$	CLK	1
	PRECHARGE ALL	$BL/2 + \text{MAX}(2, RU(t_{RTP}/t_{CK})) - 2$	CLK	1
BST	PRECHARGE to same bank as READ	1	CLK	1
	PRECHARGE ALL	1	CLK	1
READ w/AP	PRECHARGE to same bank as READ w/AP	$BL/2 + \text{MAX}(2, RU(t_{RTP}/t_{CK})) - 2$	CLK	1, 2
	PRECHARGE ALL	$BL/2 + \text{MAX}(2, RU(t_{RTP}/t_{CK})) - 2$	CLK	1
	ACTIVATE to same bank as READ w/AP	$BL/2 + \text{MAX}(2, RU(t_{RTP}/t_{CK})) - 2 + RU(t_{RPpb}/t_{CK})$	CLK	1
	WRITE or WRITE w/AP (same bank)	Illegal	CLK	3
	WRITE or WRITE w/AP (different bank)	$RL + BL/2 + RU(t_{DQSKmax}/t_{CK}) - WL + 1$	CLK	3
	READ or READ w/AP (same bank)	Illegal	CLK	3
	READ or READ w/AP (different bank)	$BL/2$	CLK	3
WRITE	PRECHARGE to same bank as WRITE	$WL + BL/2 + RU(t_{WR}/t_{CK}) + 1$	CLK	1
	PRECHARGE ALL	$WL + BL/2 + RU(t_{WR}/t_{CK}) + 1$	CLK	1
BST	PRECHARGE to same bank as WRITE	$WL + RU(t_{WR}/t_{CK}) + 1$	CLK	1
	PRECHARGE ALL	$WL + RU(t_{WR}/t_{CK}) + 1$	CLK	1


**Table 51: PRECHARGE and Auto Precharge Clarification (Continued)**

From Command	To Command	Minimum Delay Between Commands	Unit	Notes
WRITE w/AP	PRECHARGE to same bank as WRITE w/AP	$WL + BL/2 + RU(t^{WR}/t^{CK}) + 1$	CLK	1, 2
	PRECHARGE ALL	$WL + BL/2 + RU(t^{WR}/t^{CK}) + 1$	CLK	1
	ACTIVATE to same bank as WRITE w/AP	$WL + BL/2 + RU(t^{WR}/t^{CK}) + 1 + RU(t^{RPpb}/t^{CK})$	CLK	1
	WRITE or WRITE w/AP (same bank)	Illegal	CLK	3
	WRITE or WRITE w/AP (different bank)	BL/2	CLK	3
	READ or READ w/AP (same bank)	Illegal	CLK	3
	READ or READ w/AP (different bank)	$WL + BL/2 + RU(t^{WTR}/t^{CK}) + 1$	CLK	3
PRECHARGE	PRECHARGE to same bank as PRECHARGE	1	CLK	1
	PRECHARGE ALL	1	CLK	1
PRECHARGE ALL	PRECHARGE	1	CLK	1
	PRECHARGE ALL	1	CLK	1

- Notes:
- For a given bank, the PRECHARGE period should be counted from the latest PRECHARGE command—either a one-bank PRECHARGE or PRECHARGE ALL—issued to that bank. The PRECHARGE period is satisfied after  $t^{RP}$ , depending on the latest PRECHARGE command issued to that bank.
  - Any command issued during the specified minimum delay time is illegal.
  - After READ with auto precharge, seamless READ operations to different banks are supported. After WRITE with auto precharge, seamless WRITE operations to different banks are supported. READ with auto precharge and WRITE with auto precharge must not be interrupted or truncated.

## REFRESH Command

The REFRESH command is initiated with CS<sub>n</sub> LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. A per-bank REFRESH command is initiated with CA3 LOW at the rising edge of the clock. The all-bank REFRESH command is initiated with CA3 HIGH at the rising edge of the clock. A per-bank REFRESH is only supported in devices with eight banks.

A per-bank REFRESH command (REFpb) performs a per-bank REFRESH operation to the bank scheduled by the bank counter in the memory device. The bank sequence for per-bank REFRESH is fixed to be a sequential round-robin: 0-1-2-3-4-5-6-7-0-1-.... The bank count is synchronized between the controller and the SDRAM by resetting the bank count to zero. Synchronization can occur upon issuing a RESET command or at every exit from self refresh.

A bank must be idle before it can be refreshed. The controller must track the bank being refreshed by the per-bank REFRESH command.

The REFpb command must not be issued to the device until the following conditions have been met:

- $t^{RCab}$  has been satisfied after the prior REFab command
- $t^{RCpb}$  has been satisfied after the prior REFpb command
- $t^{RP}$  has been satisfied after the prior PRECHARGE command to that bank



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$t^{\text{RRD}}$  has been satisfied after the prior ACTIVATE command (when applicable, for example after activating a row in a different bank than the one affected by the REFpb command)

The target bank is inaccessible during per-bank REFRESH cycle time ( $t^{\text{RFCpb}}$ ); however, other banks within the device are accessible and can be addressed during the cycle. During the REFpb operation, any of the banks other than the one being refreshed can be maintained in an active state or accessed by a READ or WRITE command.

When the per-bank REFRESH cycle has completed, the affected bank will be in the idle state.

After issuing REFpb, the following conditions must be met:

- $t^{\text{RFCpb}}$  must be satisfied before issuing a REFab command
- $t^{\text{RFCpb}}$  must be satisfied before issuing an ACTIVATE command to the same bank
- $t^{\text{RRD}}$  must be satisfied before issuing an ACTIVATE command to a different bank
- $t^{\text{RFCpb}}$  must be satisfied before issuing another REFpb command

An all-bank REFRESH command (REFab) issues a REFRESH command to all banks. All banks must be idle when REFab is issued (for instance, by issuing a PRECHARGE ALL command prior to issuing an all-bank REFRESH command). REFab also synchronizes the bank count between the controller and the SDRAM to zero. The REFab command must not be issued to the device until the following conditions have been met:

- $t^{\text{RFCab}}$  has been satisfied following the prior REFab command
- $t^{\text{RFCpb}}$  has been satisfied following the prior REFpb command
- $t^{\text{RP}}$  has been satisfied following the prior PRECHARGE commands

After an all-bank REFRESH cycle has completed, all banks will be idle. After issuing REFab:

- $t^{\text{RFCab}}$  latency must be satisfied before issuing an ACTIVATE command
- $t^{\text{RFCab}}$  latency must be satisfied before issuing a REFab or REFpb command

**Table 52: REFRESH Command Scheduling Separation Requirements**

Symbol	Minimum Delay From	To	Notes
$t^{\text{RFCab}}$	REFab	REFab	
		ACTIVATE command to any bank	
		REFpb	
$t^{\text{RFCpb}}$	REFpb	REFab	
		ACTIVATE command to same bank as REFpb	
		REFpb	


**Table 52: REFRESH Command Scheduling Separation Requirements (Continued)**

Symbol	Minimum Delay From	To	Notes
$t_{RRD}$	REFpb	ACTIVATE command to a different bank than REFpb	
	ACTIVATE	REFpb affecting an idle bank (different bank than activate)	1
		ACTIVATE command to a different bank than the prior ACTIVATE command	

Note: 1. A bank must be in the idle state before it is refreshed, so REFab is prohibited following an ACTIVATE command. REFpb is supported only if it affects a bank that is in the idle state.

## REFRESH Requirements

### 1. Minimum Number of REFRESH Commands

Mobile LPDDR2 requires a minimum number, R, of REFRESH (REFab) commands within any rolling refresh window ( $t_{REFW} = 32 \text{ ms @ MR4}[2:0] = 011$  or  $T_C \leq 85^\circ\text{C}$ ). For actual values per density and the resulting average refresh interval ( $t_{REFI}$ ), see Refresh Requirements.

For  $t_{REFW}$  and  $t_{REFI}$  refresh multipliers at different MR4 settings, see the MR4 Device Temperature (MA[7:0] = 04h) table.

For devices supporting per-bank REFRESH, a REFab command can be replaced by a full cycle of eight REFpb commands.

### 2. Burst REFRESH Limitation

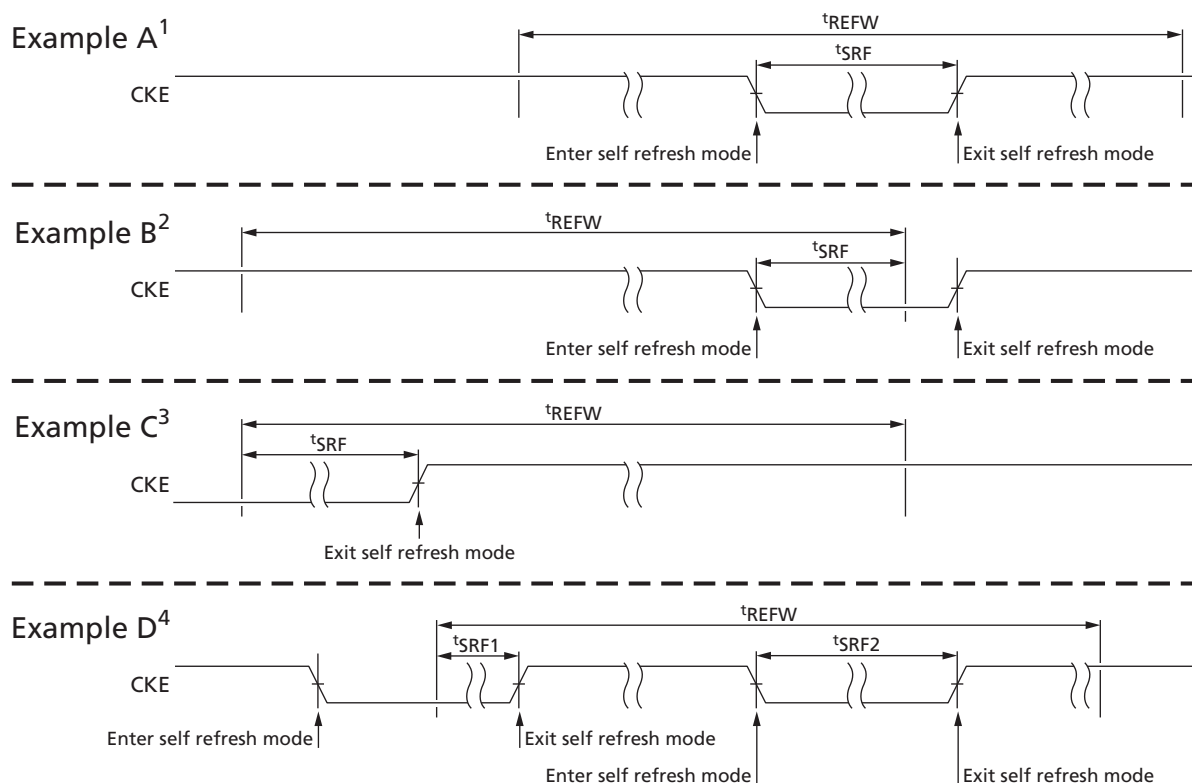
To limit current consumption, a maximum of eight REFab commands can be issued in any rolling  $t_{REFBW}$  ( $t_{REFBW} = 4 \times 8 \times t_{RFCab}$ ). This condition does not apply if REFpb commands are used.

### 3. REFRESH Requirements and Self Refresh

If any time within a refresh window is spent in self refresh mode, the number of required REFRESH commands in that window is reduced to the following:

$$R' = R - RU \left( \frac{t_{SRF}}{t_{REFI}} \right) = R - RU \left( R \times \frac{t_{SRF}}{t_{REFW}} \right)$$

Where RU represents the round-up function

**Figure 41:  $t_{SRF}$  Definition**


- Notes:
1. Time in self refresh mode is fully enclosed in the refresh window ( $t_{REFW}$ ).
  2. At self refresh entry.
  3. At self refresh exit.
  4. Several intervals in self refresh during one  $t_{REFW}$  interval. In this example,  $t_{SRF} = t_{SRF1} + t_{SRF2}$ .

The mobile LPDDR2 device provides significant flexibility in scheduling a REFRESH command as long as the required boundary conditions are met (see the  $t_{SRF}$  Definition figure).

In the most straightforward implementations, a REFRESH command should be scheduled every  $t_{REFI}$ . In this case, self refresh can be entered at any time.

Users may choose to deviate from this regular refresh pattern, for instance, to enable a period in which no refresh is required. As an example, using a 1Gb LPDDR2 device, the user can choose to issue a refresh burst of 4096 REFRESH commands at the maximum supported rate (limited by  $t_{REFBW}$ ), followed by an extended period without issuing any REFRESH commands, until the refresh window is complete. The maximum supported time without REFRESH commands is calculated as follows:  $t_{REFW} - (R/8) \times t_{REFBW} = t_{REFW} - R \times 4 \times t_{RfCab}$ .

For example, a 1Gb device at  $T_C \leq 85^\circ\text{C}$  can be operated without a refresh for up to 32ms -  $4096 \times 4 \times 130\text{ns} \approx 30\text{ms}$ .

Both the regular and the burst/pause patterns can satisfy refresh requirements if they are repeated in every 32ms window. It is critical to satisfy the refresh requirement in



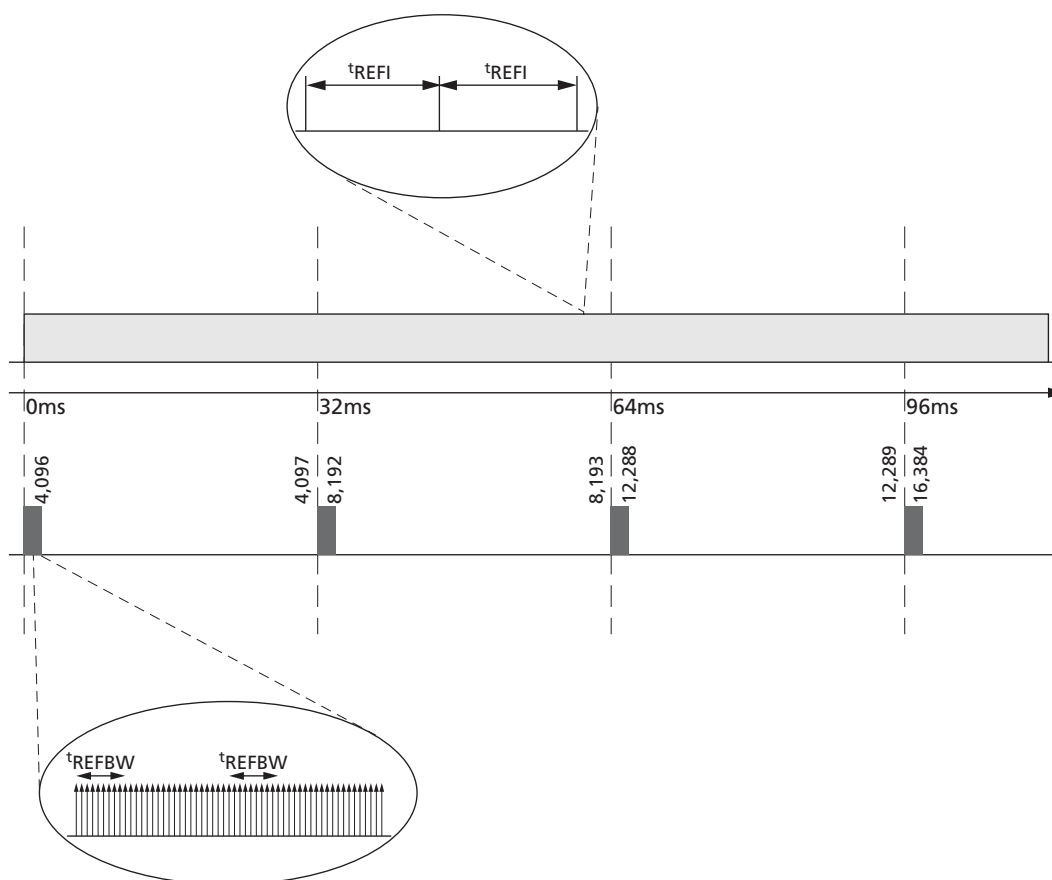
## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM REFRESH Command

*every* rolling refresh window during refresh pattern transitions. The supported transition from a burst pattern to a regular distributed pattern is shown in the Supported Transition from Repetitive REFRESH Burst figure. If this transition occurs immediately after the burst refresh phase, all rolling  $t_{REFW}$  intervals will meet the minimum required number of REFRESH commands.

A nonsupported transition is shown below. In this example, the regular refresh pattern starts after the completion of the pause phase of the burst/pause refresh pattern. For several rolling  $t_{REFW}$  intervals, the minimum number of REFRESH commands is not satisfied.

Understanding this pattern transition is extremely important, even when only one pattern is employed. In self refresh mode, a regular distributed refresh pattern must be assumed. Micron recommends entering self refresh mode immediately following the burst phase of a burst/pause refresh pattern; upon exiting self refresh, begin with the burst phase (see the Recommended Self Refresh Entry and Exit figure).

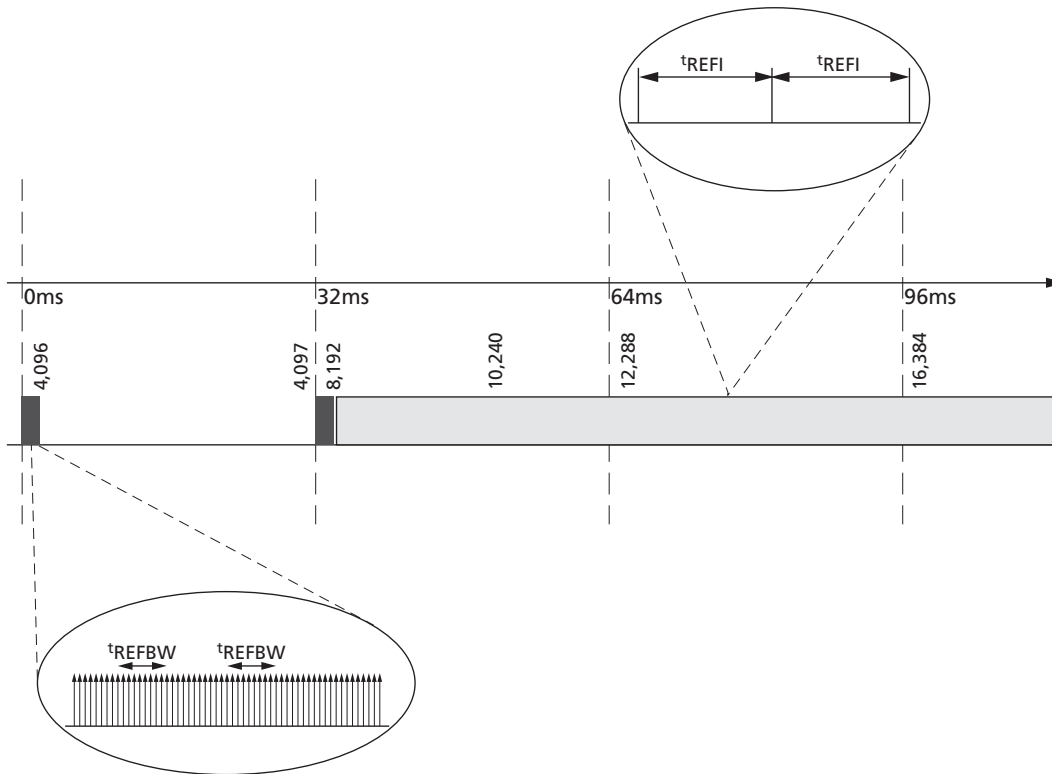
Figure 42: Regular Distributed Refresh Pattern



- Notes:
1. Compared to repetitive burst REFRESH with subsequent REFRESH pause.
  2. As an example, in a 1Gb LPDDR2 device at  $T_C \leq 85^\circ\text{C}$ , the distributed refresh pattern has one REFRESH command per 7.8 $\mu\text{s}$ ; the burst refresh pattern has one REFRESH command per 0.52 $\mu\text{s}$ , followed by  $\approx 30\text{ms}$  without any REFRESH command.

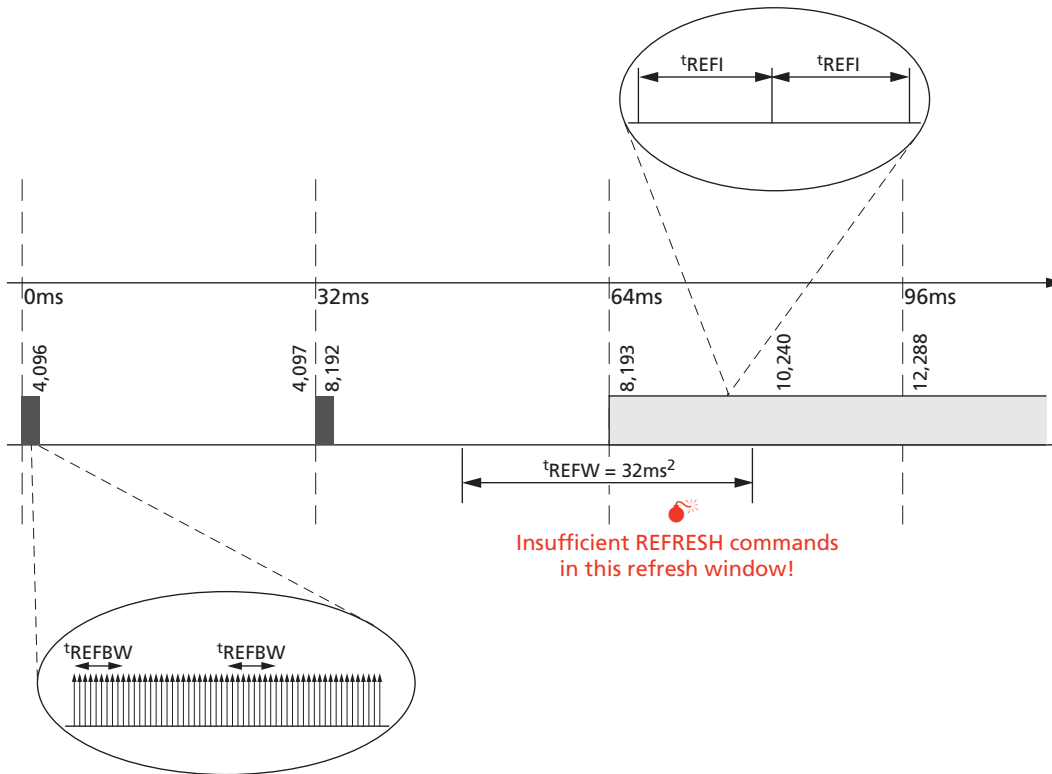


Figure 43: Supported Transition from Repetitive REFRESH Burst



- Notes:
1. Shown with subsequent REFRESH pause to regular distributed refresh pattern.
  2. As an example, in a 1Gb LPDDR2 device at  $T_C \leq 85^\circ\text{C}$ , the distributed refresh pattern has one REFRESH command per  $7.8\mu\text{s}$ ; the burst refresh pattern has one REFRESH command per  $0.52\mu\text{s}$ , followed by  $\approx 30\text{ms}$  without any REFRESH command.

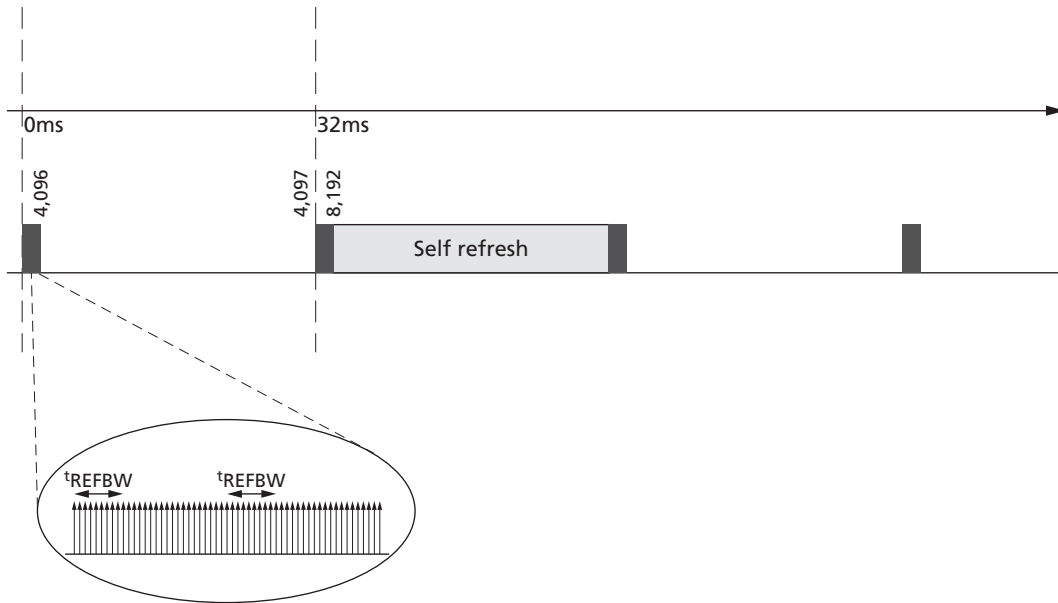
Figure 44: Nonsupported Transition from Repetitive REFRESH Burst



- Notes:
1. Shown with subsequent REFRESH pause to regular distributed refresh pattern.
  2. There are only  $\approx 2048$  REFRESH commands in the indicated  $t_{REFW}$  window. This does not provide the required minimum number of REFRESH commands (R).



Figure 45: Recommended Self Refresh Entry and Exit

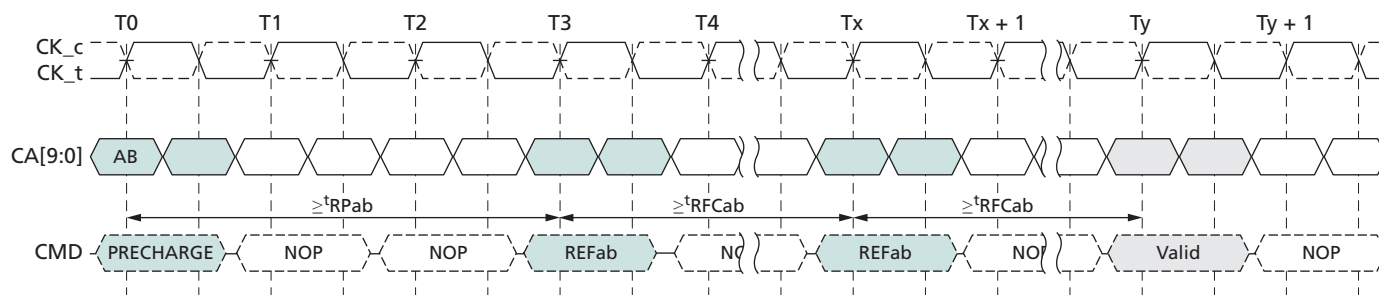


Note: 1. In conjunction with a burst/pause refresh pattern.

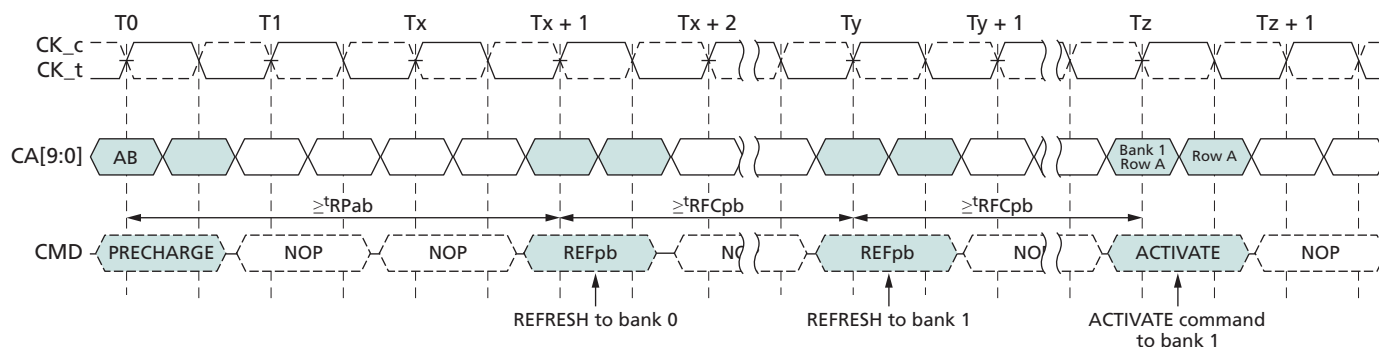


## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM SELF REFRESH Operation

**Figure 46: All-Bank REFRESH Operation**



**Figure 47: Per-Bank REFRESH Operation**



- Notes:
1. Prior to T0, the REFpb bank counter points to bank 0.
  2. Operations to banks other than the bank being refreshed are supported during the  $t_{RFCpb}$  period.

## SELF REFRESH Operation

The SELF REFRESH command can be used to retain data in the array, even if the rest of the system is powered down. When in the self refresh mode, the device retains data without external clocking. The device has a built-in timer to accommodate the SELF REFRESH operation.

The SELF REFRESH command is executed by taking CKE LOW, CS\_n LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. CKE must be HIGH during the previous clock cycle. A NOP command must be driven in the clock cycle following the POWER-DOWN command. Once the command is registered, CKE must be held LOW to keep the device in self-refresh mode.

The mobile LPDDR2 device can operate in self refresh mode in both the standard and extended temperature ranges. The device also manages self refresh power consumption when the operating temperature changes, resulting in the lowest possible power consumption across the operating temperature range (See IDD Specifications for details).

After the device has entered self refresh mode, all external signals other than CKE are “Don’t Care.” For proper self refresh operation, power supply pins ( $V_{DD1}$ ,  $V_{DD2}$ , and  $V_{DDQ}$ ) must be at valid levels.  $V_{DDQ}$  can be turned off during self refresh. If  $V_{DDQ}$  is turned off,  $V_{REFDQ}$  must also be turned off. Prior to exiting self refresh, both  $V_{DDQ}$  and



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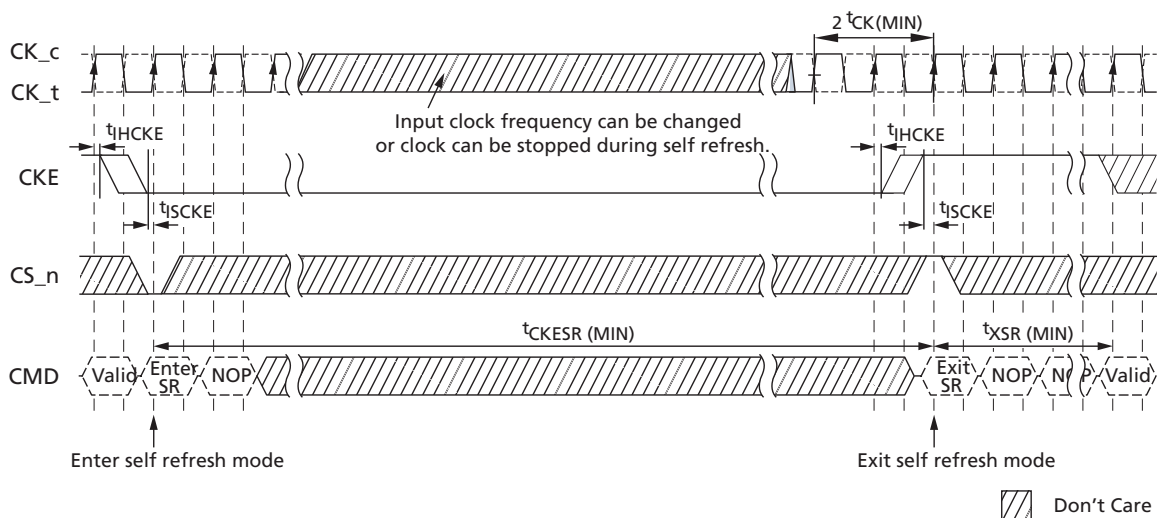
$V_{REFDQ}$  must be within their respective minimum/maximum operating ranges (see the Single-Ended AC and DC Input Levels for DQ and DM table).  $V_{REFDQ}$  can be at any level between 0 and  $V_{DDQ}$ ;  $V_{REFCA}$  can be at any level between 0 and  $V_{DD2}$  during self refresh.

Before exiting self refresh,  $V_{REFDQ}$  and  $V_{REFCA}$  must be within specified limits (See AC and DC Logic Input Measurement Levels for Single-Ended Signals for details). After entering self refresh mode, the device initiates at least one all-bank REFRESH command internally during  $t_{CKESR}$ . The clock is internally disabled during SELF REFRESH operation to save power. The device must remain in self refresh mode for at least  $t_{CKESR}$ . The user can change the external clock frequency or halt the external clock one clock after self refresh entry is registered; however, the clock must be restarted and stable before the device can exit SELF REFRESH operation.

Exiting self refresh requires a series of commands. First, the clock must be stable prior to CKE returning HIGH. After the self refresh exit is registered, a minimum delay, at least equal to the self refresh exit interval ( $t_{XSR}$ ), must be satisfied before a valid command can be issued to the device. This provides completion time for any internal refresh in progress. For proper operation, CKE must remain HIGH throughout  $t_{XSR}$ . NOP commands must be registered on each rising clock edge during  $t_{XSR}$ .

Using self refresh mode introduces the possibility that an internally timed refresh event could be missed when CKE is driven HIGH for exit from self refresh mode. Upon exiting self refresh, at least one REFRESH command (one all-bank command or eight per-bank commands) must be issued before issuing a subsequent SELF REFRESH command.

**Figure 48: SELF REFRESH Operation**



- Notes:
1. Input clock frequency can be changed or stopped during self refresh, provided that upon exiting self-refresh, a minimum of two cycles of stable clocks are provided, and the clock frequency is between the minimum and maximum frequencies for the particular speed grade.
  2. The device must be in the all banks idle state prior to entering self refresh mode.
  3.  $t_{XSR}$  begins at the rising edge of the clock after CKE is driven HIGH.
  4. A valid command can be issued only after  $t_{XSR}$  is satisfied. NOPs must be issued during  $t_{XSR}$ .



## Partial-Array Self Refresh – Bank Masking

Any device of densities of 64Mb–512Mb is comprised of four banks; a device of 1Gb density or higher is comprised of eight banks. Each bank can be configured independently whether or not a SELF REFRESH operation will occur in that bank. One 8-bit mode register (accessible via the MRW command) is assigned to program the bank-masking status of each bank up to eight banks. For bank masking bit assignments, see the MR16 PASR Bank Mask (MA[7:0] = 010h) and MR16 Op-Code Bit Definitions tables.

The mask bit to the bank enables or disables a refresh operation of the entire memory space within the bank. If a bank is masked using the bank mask register, a REFRESH operation to the entire bank is blocked and bank data retention is not guaranteed in self refresh mode. To enable a REFRESH operation to a bank, the corresponding bank mask bit must be programmed as “unmasked.” When a bank mask bit is unmasked, the array space being refreshed within that bank is determined by the programmed status of the segment mask bits.

## Partial-Array Self Refresh – Segment Masking

Programming segment mask bits is similar to programming bank mask bits. For a density of 1Gb or higher, eight segments are used for masking (see the MR17 PASR Segment Mask (MA[7:0] = 011h) and MR17 PASR Segment Mask Definitions tables). A mode register is used for programming segment mask bits up to eight bits. For a density of less than 1Gb, segment masking is not supported.

When the mask bit to an address range (represented as a segment) is programmed as “masked,” a REFRESH operation to that segment is blocked. Conversely, when a segment mask bit to an address range is unmasked, refresh to that segment is enabled.

A segment masking scheme can be used in place of or in combination with a bank masking scheme. Each segment mask bit setting is applied across all banks. For segment masking bit assignments, see the tables noted above.

**Table 53: Bank and Segment Masking Example**

	Segment Mask (MR17)	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5	Bank 6	Bank 7
<b>Bank Mask (MR16)</b>		<b>0</b>	<b>1</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>1</b>
Segment 0	0	–	M	–	–	–	–	–	M
Segment 1	0	–	M	–	–	–	–	–	M
Segment 2	1	M	M	M	M	M	M	M	M
Segment 3	0	–	M	–	–	–	–	–	M
Segment 4	0	–	M	–	–	–	–	–	M
Segment 5	0	–	M	–	–	–	–	–	M
Segment 6	0	–	M	–	–	–	–	–	M
Segment 7	1	M	M	M	M	M	M	M	M

Note: 1. This table provides values for an 8-bank device with REFRESH operations masked to banks 1 and 7, and segments 2 and 7.

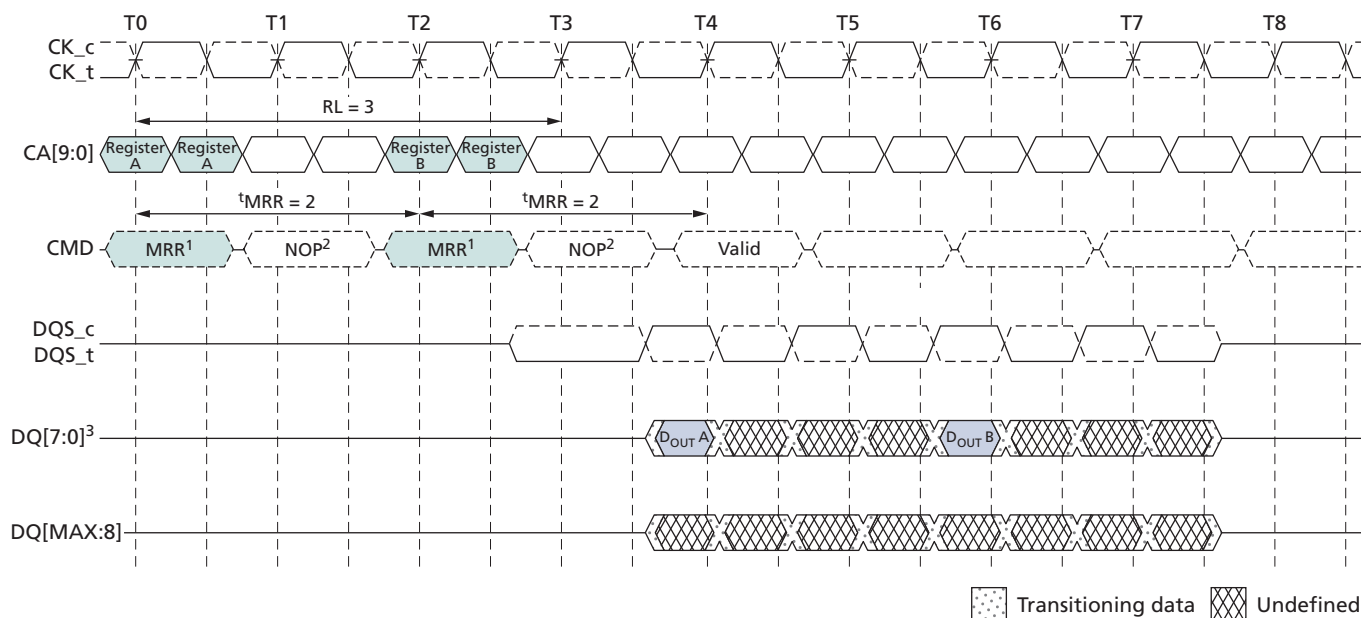


## MODE REGISTER READ

The MODE REGISTER READ (MRR) command is used to read configuration and status data from SDRAM mode registers. The MRR command is initiated with CS<sub>n</sub> LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The mode register is selected by CA1f–CA0f and CA9r–CA4r. The mode register contents are available on the first data beat of DQ[7:0] after  $RL \times ^tCK + ^tDQSCK + ^tDQSQ$  and following the rising edge of the clock where MRR is issued. Subsequent data beats contain valid but undefined content, except in the case of the DQ calibration function, where subsequent data beats contain valid content as described in the Data Calibration Pattern Description table. All DQS<sub>t</sub>, DQS<sub>c</sub> are toggled for the duration of the mode register READ burst.

The MRR command has a burst length of four. MRR operation (consisting of the MRR command and the corresponding data traffic) must not be interrupted. The MRR command period ( $^tMRR$ ) is two clock cycles. The MRR command issued to reserved and write-only registers should return valid but undefined content on all data beats, and DQS<sub>t</sub>, DQS<sub>c</sub> should be toggled.

**Figure 49: MRR Timing – RL = 3,  $^tMRR = 2$**



- Notes:
1. MRRs to DQ calibration registers MR32 and MR40 are described in the Data Calibration Pattern Description table.
  2. Only the NOP command is supported during  $^tMRR$ .
  3. Mode register data is valid only on DQ[7:0] on the first beat. Subsequent beats contain valid but undefined data. DQ[MAX:8] contain valid but undefined data for the duration of the MRR burst.
  4. Minimum MRR to write latency is  $RL + RU(^tDQSCK_{max}/^tCK) + 4/2 + 1 - WL$  clock cycles.
  5. Minimum MRR to MRW latency is  $RL + RU(^tDQSCK_{max}/^tCK) + 4/2 + 1$  clock cycles.

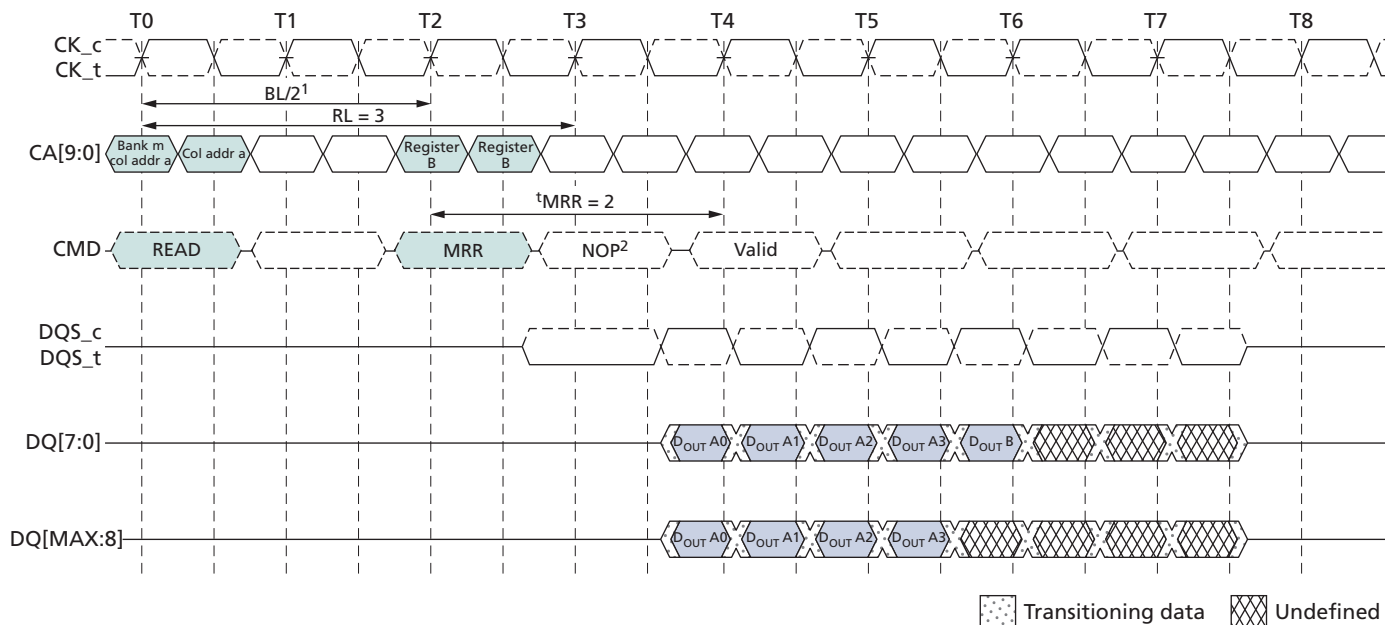
READ bursts and WRITE bursts cannot be truncated by MRR. Following a READ command, the MRR command must not be issued before BL/2 clock cycles have completed.



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM MODE REGISTER READ

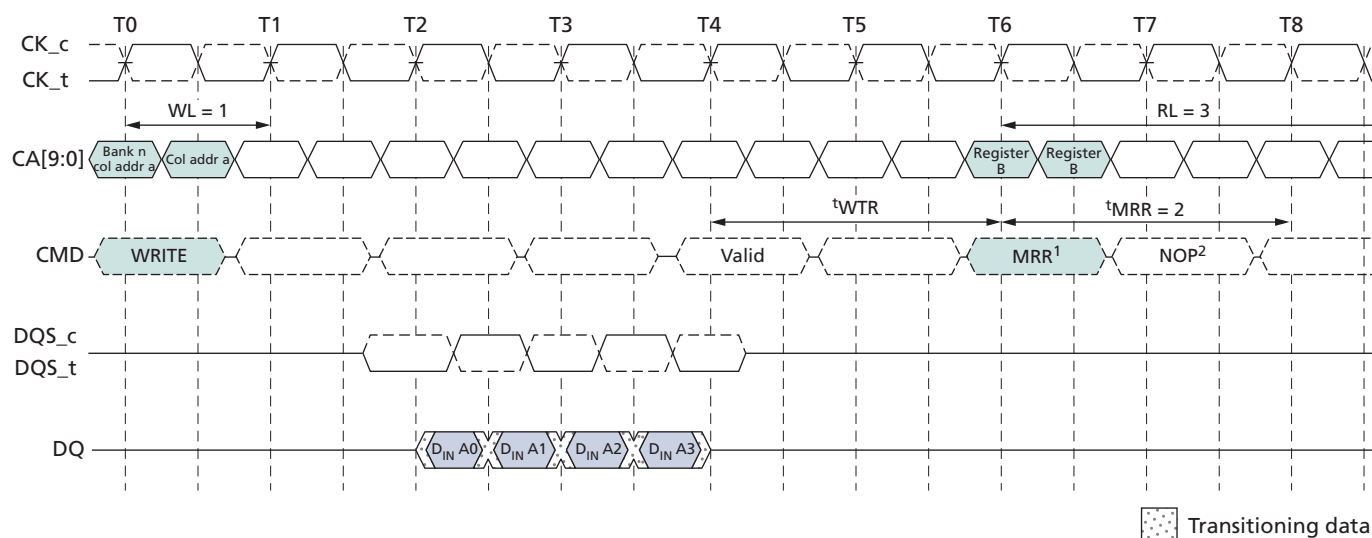
Following a WRITE command, the MRR command must not be issued before  $WL + 1 + BL/2 + RU$  ( $t_{WTR}/t_{CK}$ ) clock cycles have completed. If a READ or WRITE burst is truncated with a BST command, the effective burst length of the truncated burst should be used for the BL value.

**Figure 50: READ to MRR Timing – RL = 3,  $t_{MRR} = 2$**



- Notes:
1. The minimum number of clock cycles from the burst READ command to the MRR command is BL/2.
  2. Only the NOP command is supported during t<sub>MRR</sub>.




**Figure 51: Burst WRITE Followed by MRR – RL = 3, WL = 1, BL = 4**


- Notes:
1. The minimum number of clock cycles from the burst WRITE command to the MRR command is  $[WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})]$ .
  2. Only the NOP command is supported during  $t_{MRR}$ .

## Temperature Sensor

The mobile LPDDR2 device features a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate, determine whether AC timing derating is required in the extended temperature range, and/or monitor the operating temperature. Either the temperature sensor or the device operating temperature can be used to determine whether operating temperature requirements are being met (see Operating Temperature Range table).

Temperature sensor data can be read from MR4 using the mode register read protocol. Upon exiting self-refresh or power-down, the device temperature status bits will be no older than  $t_{TSI}$ .

When using the temperature sensor, the actual device case temperature may be higher than the operating temperature specification that applies for the standard or extended temperature ranges (see table noted above). For example,  $T_{CASE}$  could be above 85°C when MR4[2:0] equals 011b.

To ensure proper operation using the temperature sensor, applications must accommodate the parameters in the temperature sensor definitions table.


**Table 54: Temperature Sensor Definitions and Operating Conditions**

Parameter	Description	Symbol	Min/Max	Value	Unit
System temperature gradient	Maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2°C	TempGradient	MAX	System-dependent	°C/s
MR4 READ interval	Time period between MR4 READs from the system	ReadInterval	MAX	System-dependent	ms
Temperature sensor interval	Maximum delay between internal updates of MR4	<sup>t</sup> TSI	MAX	32	ms
System response delay	Maximum response time from an MR4 READ to the system response	SysRespDelay	MAX	System-dependent	ms
Device temperature margin	Margin above maximum temperature to support controller response	TempMargin	MAX	2	°C

The mobile LPDDR2 device accommodates the temperature margin between the point at which the device temperature enters the extended temperature range and the point at which the controller reconfigures the system accordingly. To determine the required MR4 polling frequency, the system must use the maximum TempGradient and the maximum response time of the system according to the following equation:

$$\text{TempGradient} \times (\text{ReadInterval} + {}^t\text{TSI} + \text{SysRespDelay}) \leq 2^\circ\text{C}$$

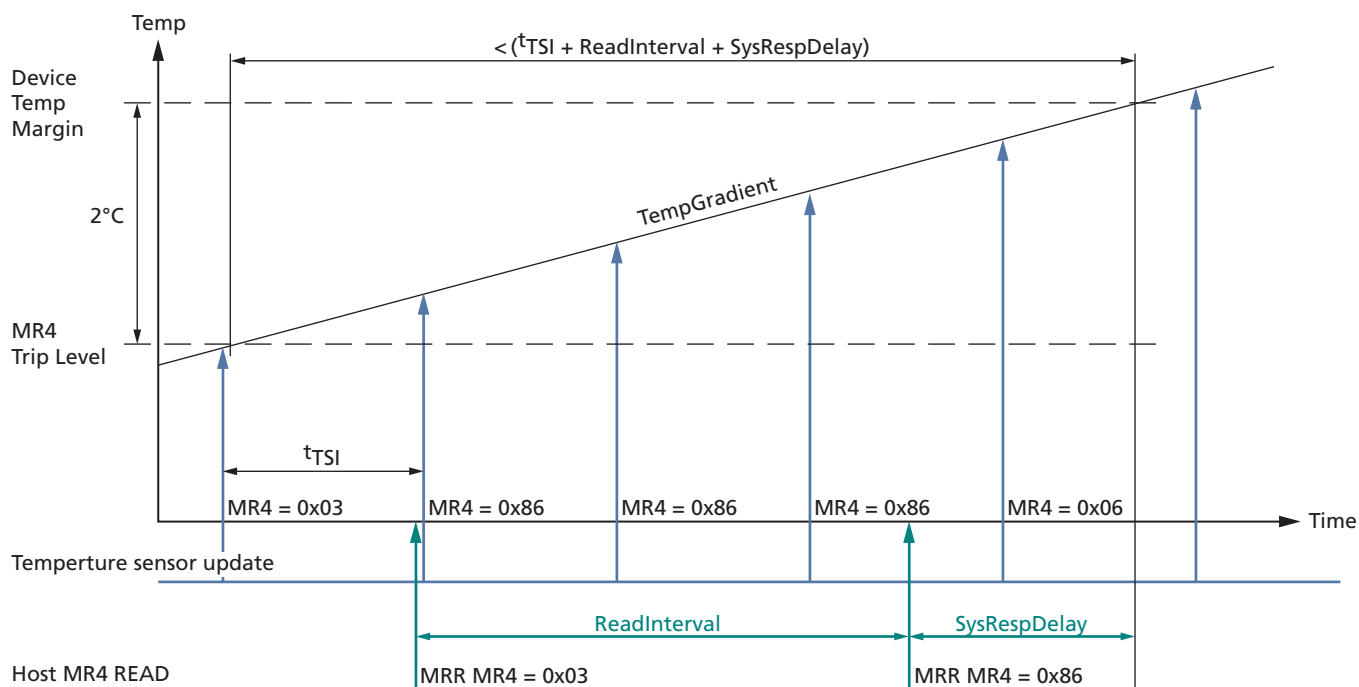
For example, if TempGradient is 10°C/s and the SysRespDelay is 1ms:

$$\frac{10^\circ\text{C}}{\text{s}} \times (\text{ReadInterval} + 32\text{ms} + 1\text{ms}) \leq 2^\circ\text{C}$$

In this case, ReadInterval must not exceed 167ms.



Figure 52: Temperature Sensor Timing



## DQ Calibration

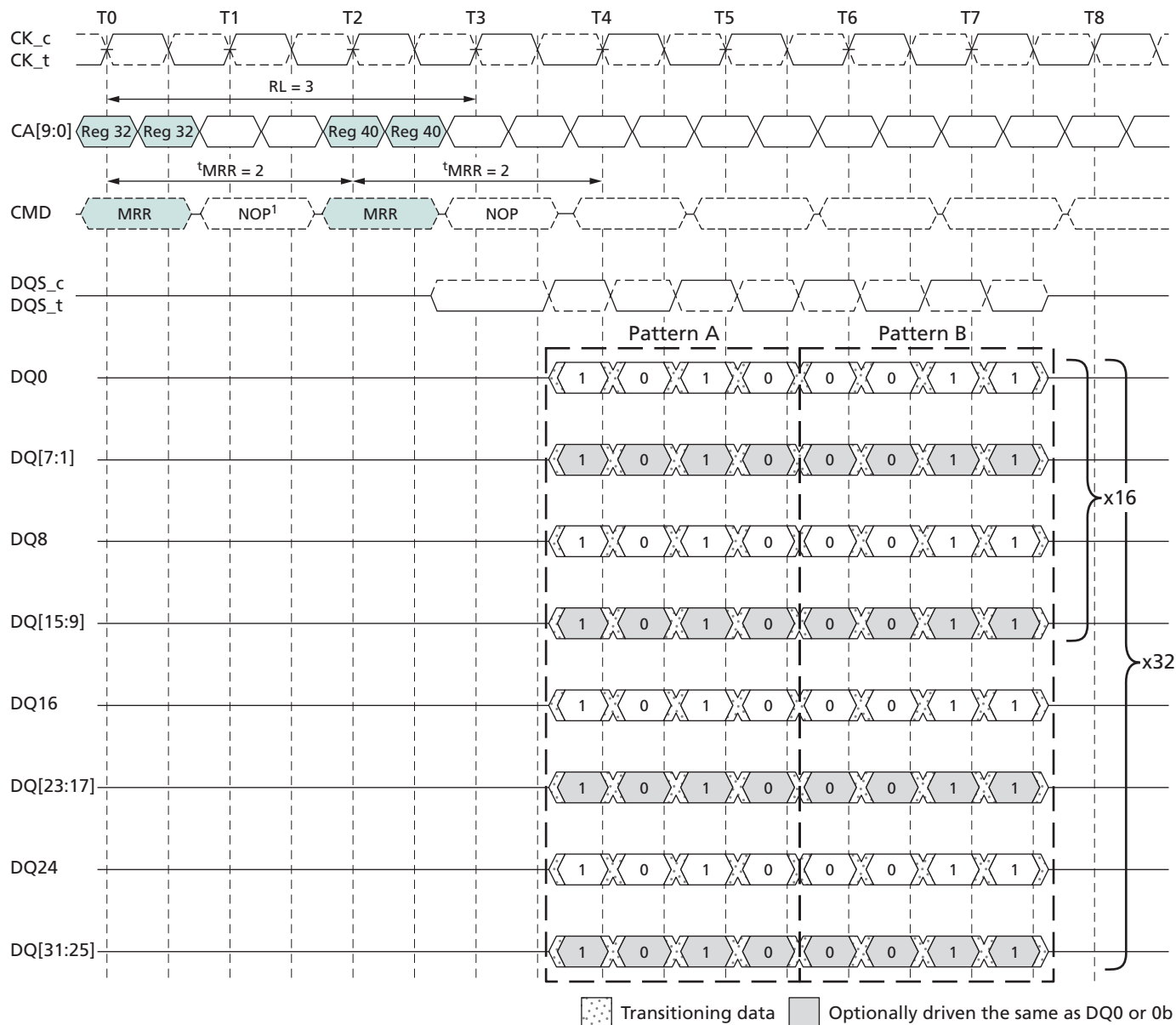
The mobile LPDDR2 device features a DQ calibration function that outputs one of two predefined system timing calibration patterns. For a x16 device, pattern A (MRR to MRR32), and pattern B (MRR to MRR40), will return the specified pattern on DQ0 and DQ8; a x32 device returns the specified pattern on DQ0, DQ8, DQ16, and DQ24.

For a x16 device, DQ[7:1] and DQ[15:9] drive the same information as DQ0 during the MRR burst. For a x32 device, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] drive the same information as DQ0 during the MRR burst. MRR DQ calibration commands can occur only in the idle state.



# 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM MODE REGISTER READ

**Figure 53: MR32 and MR40 DQ Calibration Timing – RL = 3,  $t^{MRR} = 2$**



- Notes:
1. The MRR command has a burst length of four.
  2. The MRR operation must not be interrupted.
  3. A MRR to MR32 and MR40 drives valid data on DQ[0] during the entire burst. For a x16 device, DQ[8] drives the same information as DQ[0] during the burst. For a x32 device, DQ[8], DQ[16], and DQ[24] drive the same information as DQ[0] during the burst.
  4. For a x16 device, DQ[7:1] and DQ[15:9] may optionally drive the same information as DQ[0], or they may drive 0b during the burst. For a x32 device, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] may optionally drive the same information as DQ[0], or they may drive 0b during the burst.
  5. The MODE REGISTER command period is  $t^{MRR}$ . No command (other than NOP) is allowed during this period.



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM MODE REGISTER WRITE Command

**Table 55: Data Calibration Pattern Description**

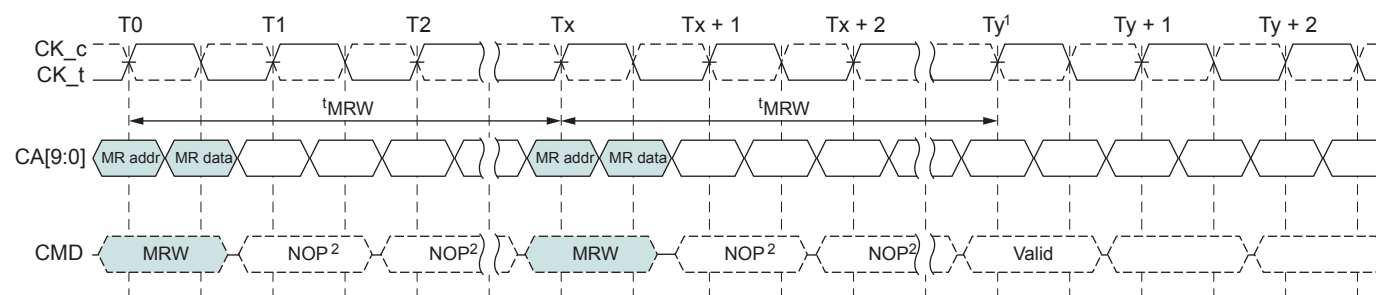
Pattern	MR#	Bit Time 0	Bit Time 1	Bit Time 2	Bit Time 3	Description
Pattern A	MR32	1	0	1	0	Reads to MR32 return DQ calibration pattern A
Pattern B	MR40	0	0	1	1	Reads to MR40 return DQ calibration pattern B

### MODE REGISTER WRITE Command

The MODE REGISTER WRITE (MRW) command is used to write configuration data to the mode registers. The MRW command is initiated with CS<sub>n</sub> LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 LOW at the rising edge of the clock. The mode register is selected by CA1f–CA0f, CA9r–CA4r. The data to be written to the mode register is contained in CA9f–CA2f. The MRW command period is defined by  $t_{MRW}$ . A MRW command to read-only registers has no impact on the functionality of the device.

MRW can be issued only when all banks are in the idle precharge state. One method of ensuring that the banks are in this state is to issue a PRECHARGE ALL command.

**Figure 54: MODE REGISTER WRITE Timing – RL = 3,  $t_{MRW} = 5$**



- Notes: 1. At time  $T_y$ , the device is in the idle state.  
2. Only the NOP command is supported during  $t_{MRW}$ .

**Table 56: Truth Table for MRR and MRW**

Current State	Command	Intermediate State	Next State
All banks idle	MRR	Reading mode register, all banks idle	All banks idle
	MRW	Writing mode register, all banks idle	All banks idle
	MRW (RESET)	Resetting, device auto initialization	All banks idle
Bank(s) active	MRR	Reading mode register, bank(s) active	Bank(s) active
	MRW	Not allowed	Not allowed
	MRW (RESET)	Not allowed	Not allowed

### MRW RESET Command

The MRW RESET command brings the device to the device auto initialization (resetting) state in the power-on initialization sequence (see step 2. of the RESET Command



under Voltage Ramp and Initialization Sequence). The MRW RESET command can be issued from the idle state. This command resets all mode registers to their default values. Only the NOP command is supported during  $t_{INIT4}$ . After MRW RESET, boot timings must be observed until the device initialization sequence is complete and the device is in the idle state. Array data is undefined after the MRW RESET command has completed. For MRW RESET timing, see Voltage Ramp and Initialization Sequence.

## MRW ZQ Calibration Commands

The MRW command is used to initiate a ZQ calibration command that calibrates output driver impedance across process, temperature, and voltage. LPDDR2-S4 devices support ZQ calibration. To achieve tighter tolerances, proper ZQ calibration must be performed.

There are four ZQ calibration commands and related timings:  $t_{ZQINIT}$ ,  $t_{ZQRESET}$ ,  $t_{ZQCL}$ , and  $t_{ZQCS}$ .  $t_{ZQINIT}$  is used for initialization calibration;  $t_{ZQRESET}$  is used for resetting ZQ to the default output impedance;  $t_{ZQCL}$  is used for long calibration(s); and  $t_{ZQCS}$  is used for short calibration(s). See the MR10 Calibration (MA[7:0] = 0Ah) table for ZQ calibration command code definitions.

ZQINIT must be performed for LPDDR2 devices. ZQINIT provides an output impedance accuracy of  $\pm 15\%$ . After initialization, the ZQ calibration long (ZQCL) can be used to recalibrate the system to an output impedance accuracy of  $\pm 15\%$ . A ZQ calibration short (ZQCS) can be used periodically to compensate for temperature and voltage drift in the system.

ZQRESET resets the output impedance calibration to a default accuracy of  $\pm 30\%$  across process, voltage, and temperature. This command is used to ensure output impedance accuracy to  $\pm 30\%$  when ZQCS and ZQCL commands are not used.

One ZQCS command can effectively correct at least 1.5% (ZQ correction) of output impedance errors within  $t_{ZQCS}$  for all speed bins if maximum sensitivities are met as specified in Output Driver Sensitivity Definition and Output Driver Temperature and Voltage Sensitivity. The appropriate interval between ZQCS commands can be determined using these tables and system-specific parameters.

Mobile LPDDR2 devices are subject to temperature drift rate ( $T_{driftrate}$ ) and voltage drift rate ( $V_{driftrate}$ ) in various applications. To accommodate drift rates and calculate the necessary interval between ZQCS commands, apply the following formula:

$$\frac{ZQ_{correction}}{(T_{sens} \times T_{driftrate}) + (V_{sens} \times V_{driftrate})}$$

Where  $T_{sens} = \text{MAX}(dR_{ONdT})$  and  $V_{sens} = \text{MAX}(dR_{ONdV})$  define temperature and voltage sensitivities.

For example, if  $T_{sens} = 0.75\%/^{\circ}\text{C}$ ,  $V_{sens} = 0.20\%/mV$ ,  $T_{driftrate} = 1^{\circ}\text{C}/\text{sec}$ , and  $V_{driftrate} = 15\text{ mV}/\text{sec}$ , then the interval between ZQCS commands is calculated as:

$$\frac{1.5}{(0.75 \times 1) + (0.20 \times 15)} = 0.4s$$

A ZQ calibration command can only be issued when the device is in the idle state with all banks precharged.

No other activities can be performed on the data bus during calibration periods

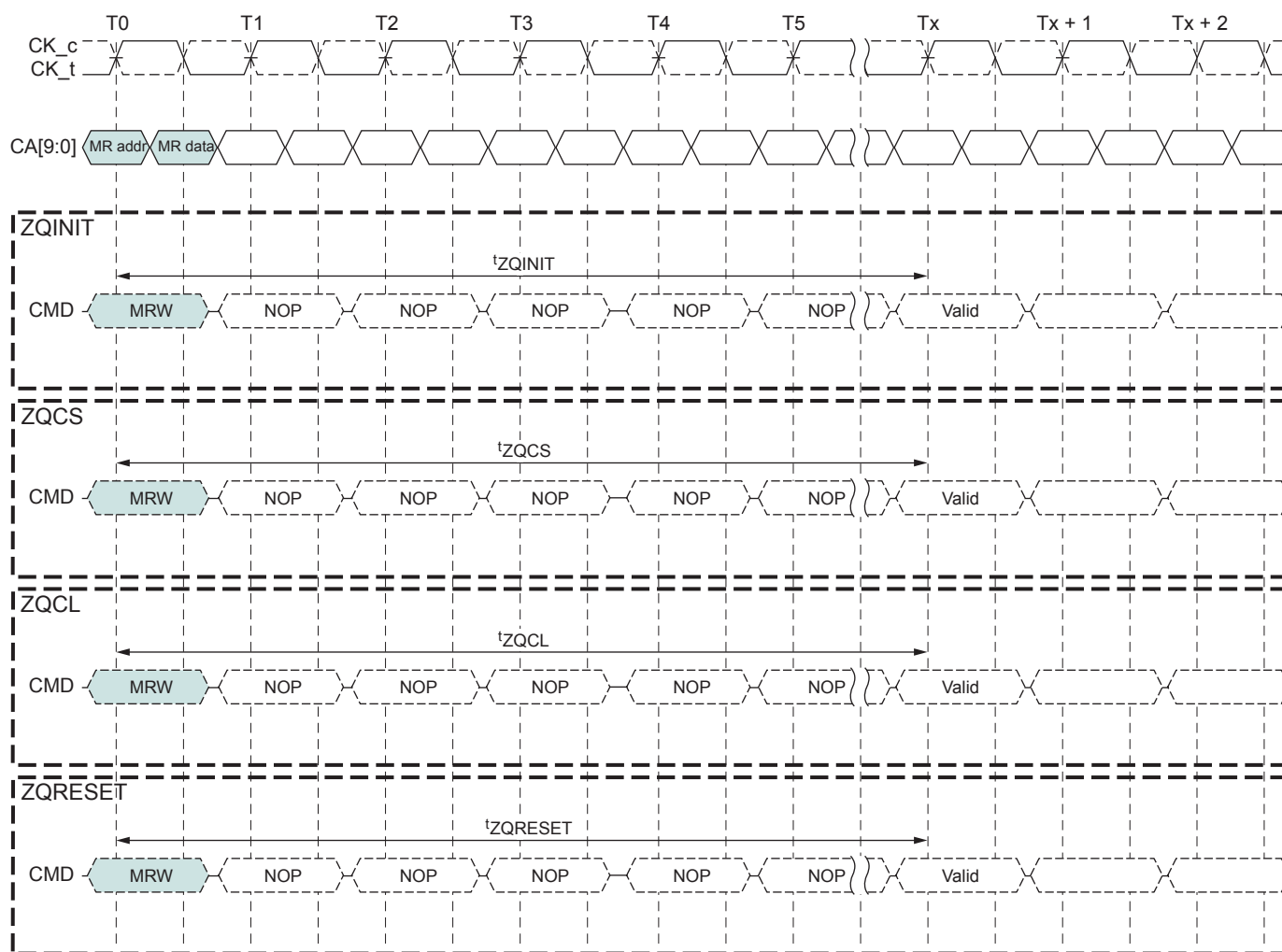


## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM MODE REGISTER WRITE Command

( $t_{ZQINIT}$ ,  $t_{ZQCL}$ , or  $t_{ZQCS}$ ). The quiet time on the data bus helps to calibrate output impedance accurately. There is no required quiet time after the ZQRESET command. If multiple devices share a single ZQ resistor, only one device can be calibrating at any given time. After calibration is complete, the ZQ ball circuitry is disabled to reduce power consumption.

In systems sharing a ZQ resistor between devices, the controller must prevent  $t_{ZQINIT}$ ,  $t_{ZQCS}$ , and  $t_{ZQCL}$  overlap between the devices. ZQRESET overlap is acceptable. If the ZQ resistor is absent from the system, ZQ must be connected to  $V_{DD2}$ . In this situation, the device must ignore ZQ calibration commands and the device will use the default calibration settings.

Figure 55: ZQ Timings



- Notes: 1. Only the NOP command is supported during ZQ calibrations
- $t_{ZQINIT}$ : ZQ calibration initialization period
  - $t_{ZQCS}$ : ZQ calibration short period
  - $t_{ZQCL}$ : ZQ calibration long period
  - $t_{ZQRESET}$ : ZQ calibration reset period



2. CKE must be registered HIGH continuously during the calibration period.
3. All devices connected to the DQ bus should be High-Z during the calibration process.

## ZQ External Resistor Value, Tolerance, and Capacitive Loading

To use the ZQ calibration function, a 240 ohm ( $\pm 1\%$  tolerance) external resistor must be connected between the ZQ pin and ground. A single resistor can be used for each device or one resistor can be shared between multiple devices if the ZQ calibration timings for each device do not overlap. The total capacitive loading on the ZQ pin must be limited (see the Input/Output Capacitance table).

## Power-Down

Power-down is entered synchronously when CKE is registered LOW and CS<sub>n</sub> is HIGH at the rising edge of clock. A NOP command must be driven in the clock cycle following power-down entry. CKE must not go LOW while MRR, MRW, READ, or WRITE operations are in progress. CKE can go LOW while any other operation such as ACTIVATE, PRECHARGE, auto precharge, or REFRESH are in progress, but the power-down I<sub>DD</sub> specification will not be applied until such operations are complete.

If power-down occurs when all banks are idle, this mode is referred to as idle power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down.

Entering power-down deactivates the input and output buffers, excluding CK<sub>t</sub>, CK<sub>c</sub>, and CKE. In power-down mode, CKE must be held LOW; all other input signals are "Don't Care." CKE LOW must be maintained until <sup>t</sup>CKE is satisfied. V<sub>REFCA</sub> must be maintained at a valid level during power-down.

V<sub>DDQ</sub> can be turned off during power-down. If V<sub>DDQ</sub> is turned off, V<sub>REFDQ</sub> must also be turned off. Prior to exiting power-down, both V<sub>DDQ</sub> and V<sub>REFDQ</sub> must be within their respective minimum/maximum operating ranges (see AC and DC Operating Conditions).

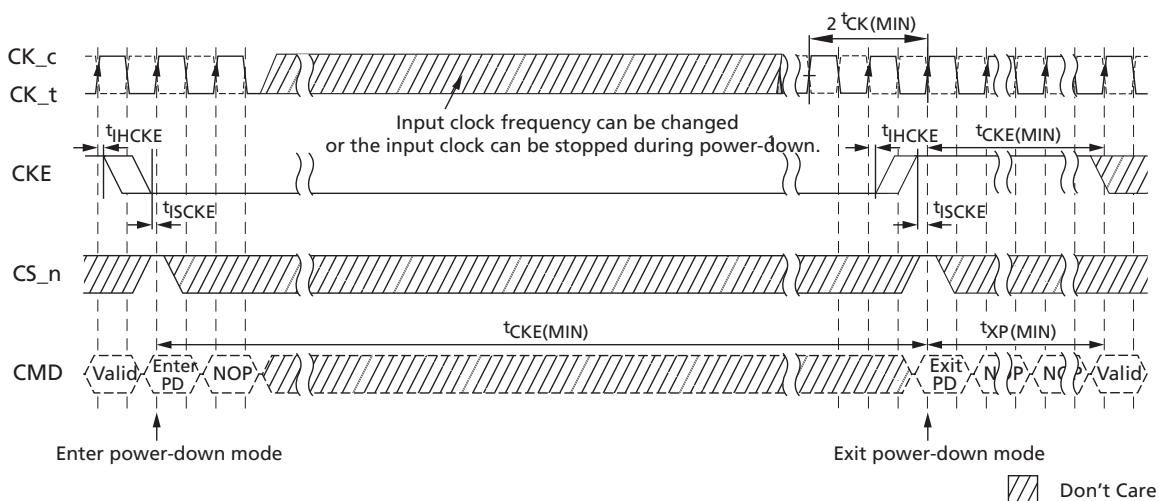
No refresh operations are performed in power-down mode. The maximum duration in power-down mode is limited only by the refresh requirements outlined in REFRESH Command.

The power-down state is exited when CKE is registered HIGH. The controller must drive CS<sub>n</sub> HIGH in conjunction with CKE HIGH when exiting the power-down state. CKE HIGH must be maintained until <sup>t</sup>CKE is satisfied. A valid, executable command can be applied with power-down exit latency <sup>t</sup>XP after CKE goes HIGH. Power-down exit latency is defined in the AC Timing section.





Figure 56: Power-Down Entry and Exit Timing



Note: 1. Input clock frequency can be changed or the input clock stopped during power-down, provided that the clock frequency is between the minimum and maximum specified frequencies for the speed grade in use, and that prior to power-down exit, a minimum of two stable clocks complete.

Figure 57: CKE Intensive Environment

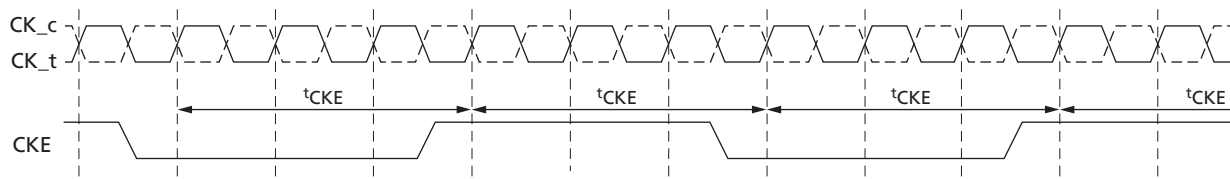
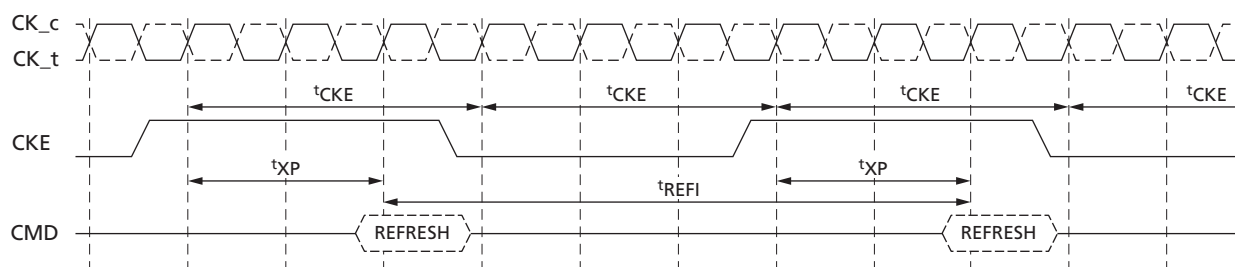


Figure 58: REFRESH-to-REFRESH Timing in CKE Intensive Environments

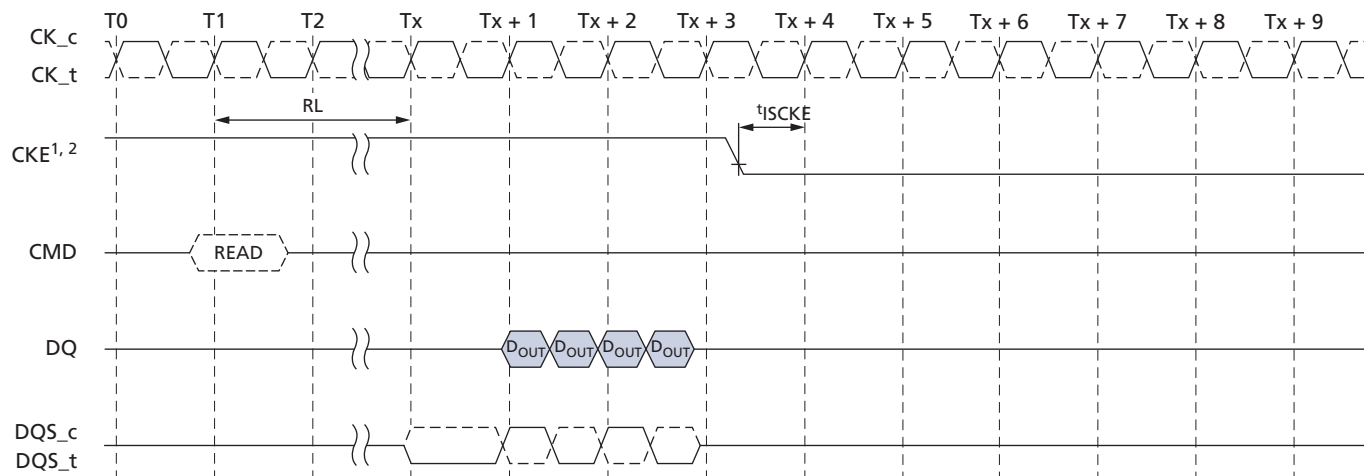


Note: 1. The pattern shown can repeat over an extended period of time. With this pattern, all AC and DC timing and voltage specifications with temperature and voltage drift are ensured.

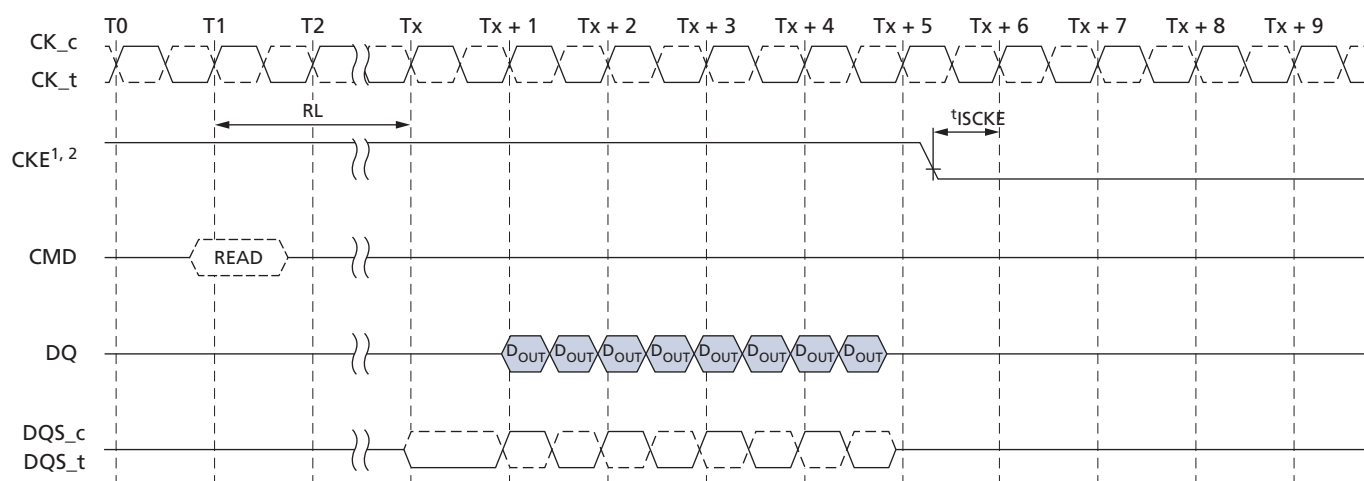


Figure 59: READ to Power-Down Entry

BL = 4



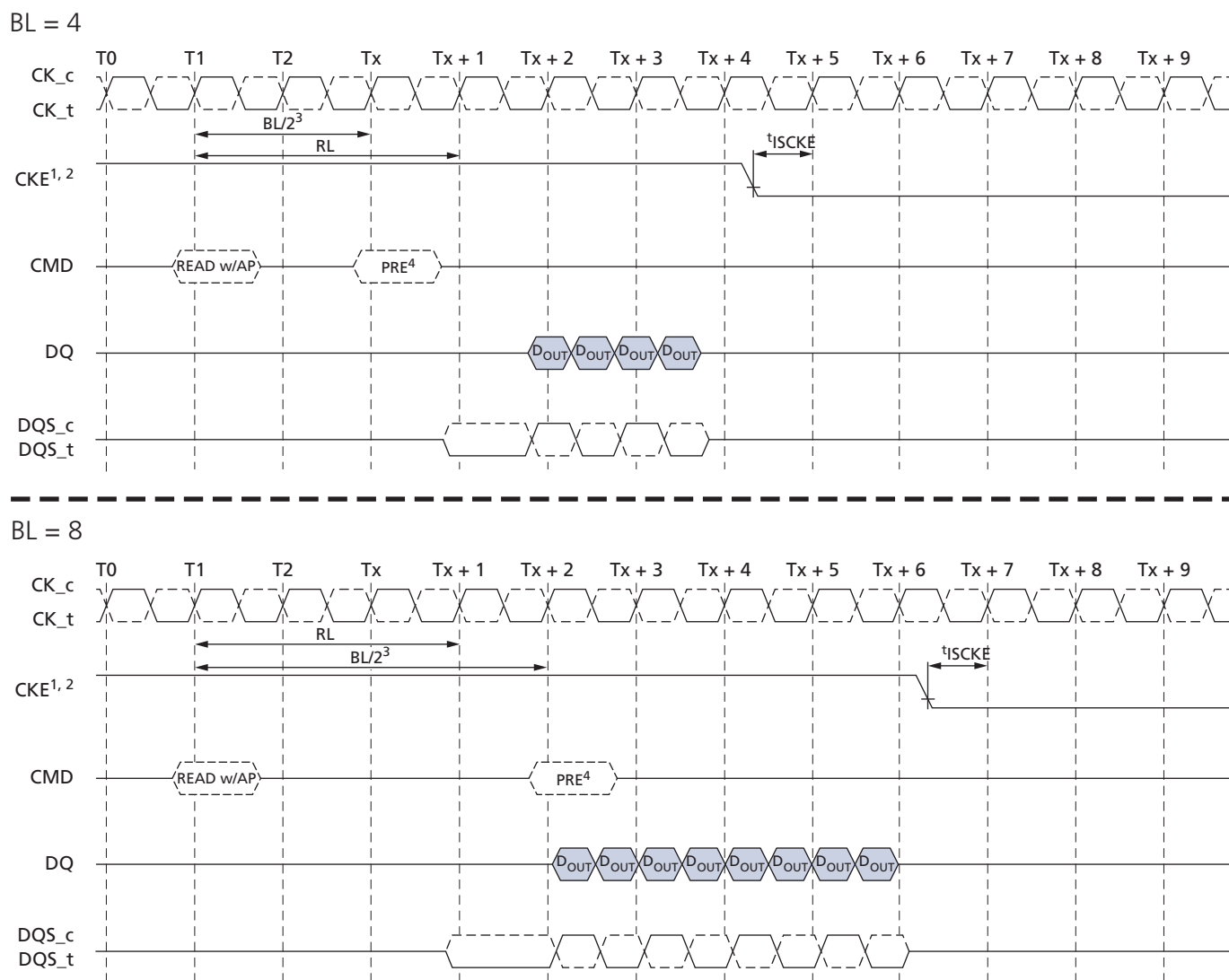
BL = 8



- Notes:
1. CKE must be held HIGH until the end of the burst operation.
  2. CKE can be registered LOW at  $(RL + RU(t_{DQSCK}(MAX)/t_{CK}) + BL/2 + 1)$  clock cycles after the clock on which the READ command is registered.



Figure 60: READ with Auto Precharge to Power-Down Entry

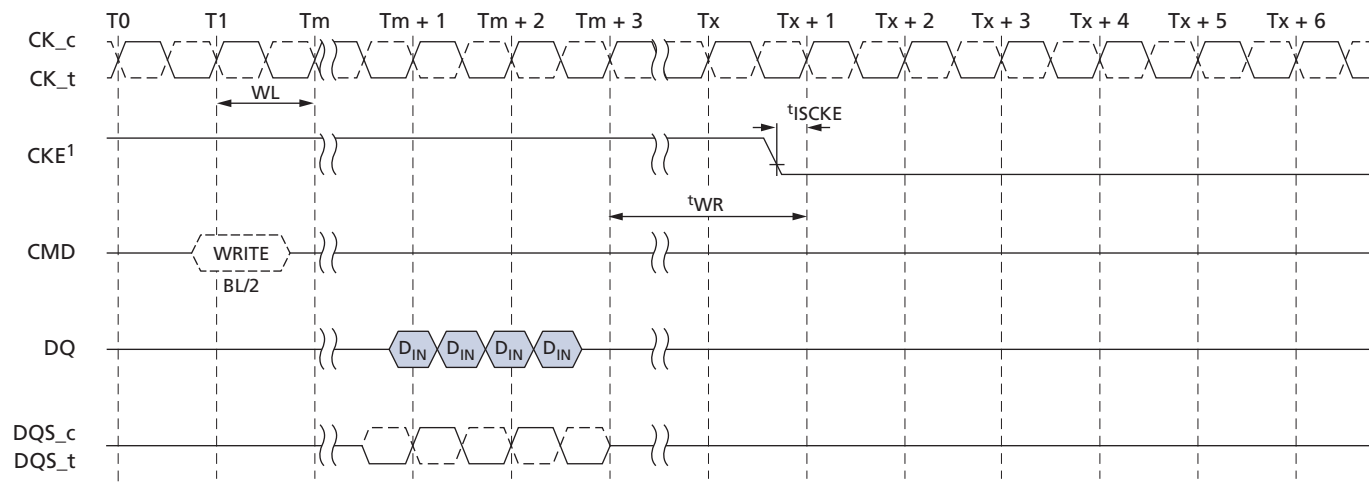


- Notes:
1. CKE must be held HIGH until the end of the burst operation.
  2. CKE can be registered LOW at  $(RL + RU(t_{DQSCK}/t_{CK}) + BL/2 + 1)$  clock cycles after the clock on which the READ command is registered.
  3. BL/2 with  $t_{RTP} = 7.5\text{ns}$  and  $t_{RAS}(\text{MIN})$  is satisfied.
  4. Start internal PRECHARGE.

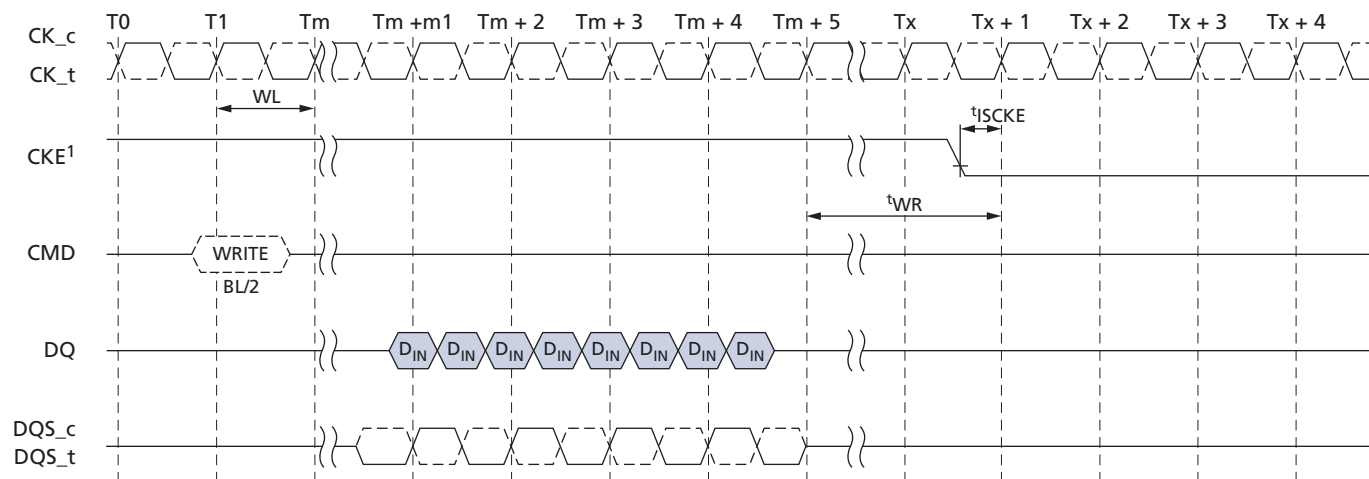


Figure 61: WRITE to Power-Down Entry

BL = 4



BL = 8

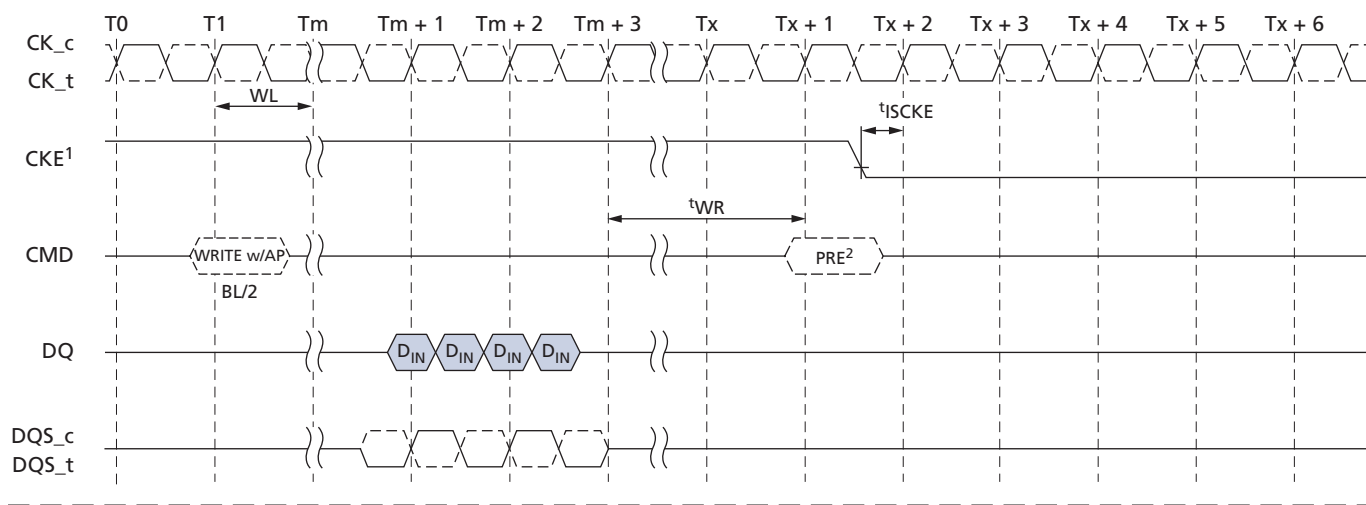


Note: 1. CKE can be registered LOW at  $(WL + 1 + BL/2 + RU(t_{WR}/t_{CK}))$  clock cycles after the clock on which the WRITE command is registered.

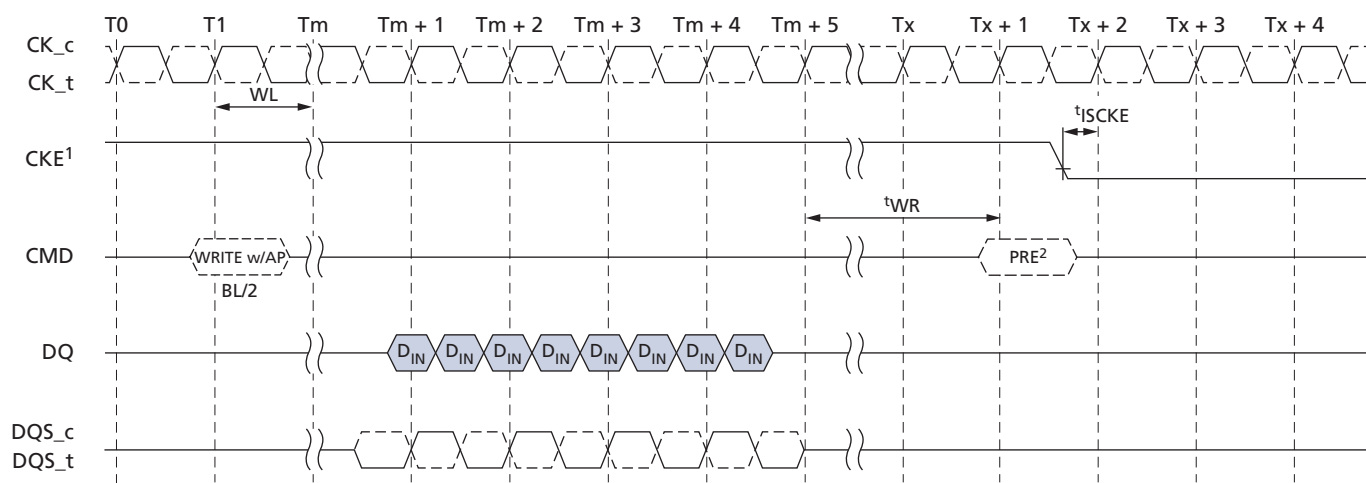


Figure 62: WRITE with Auto Precharge to Power-Down Entry

BL = 4



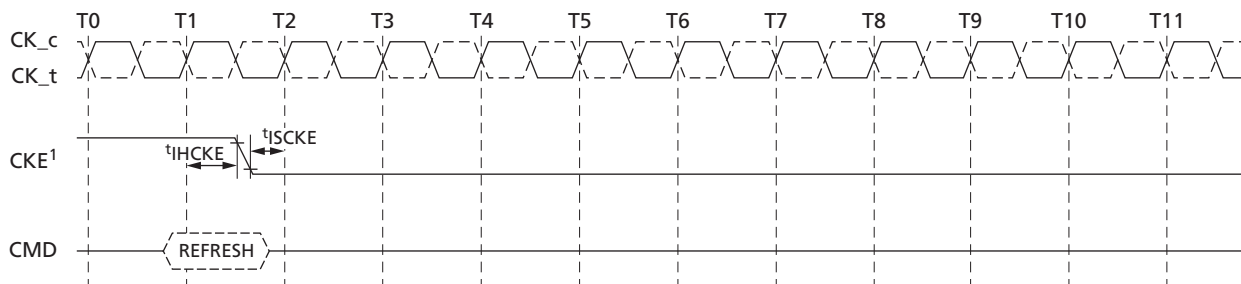
BL = 8



- Notes:
1. CKE can be registered LOW at  $(WL + 1 + BL/2 + RU(t_{WR}/t_{CK} + 1))$  clock cycles after the WRITE command is registered.
  2. Start internal PRECHARGE.

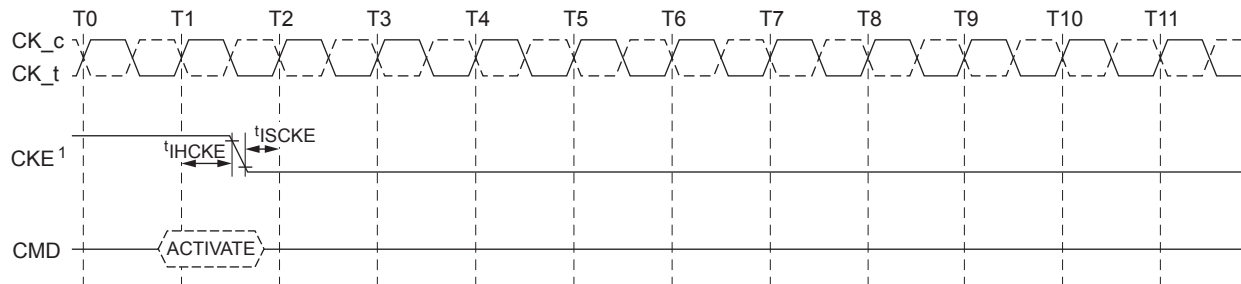


Figure 63: REFRESH Command to Power-Down Entry



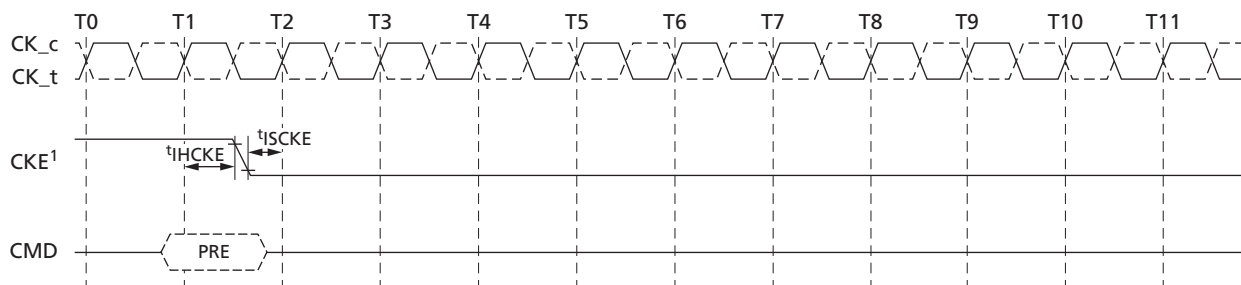
Note: 1. CKE can go LOW  $t_{IHCKE}$  after the clock on which the REFRESH command is registered.

Figure 64: ACTIVATE Command to Power-Down Entry

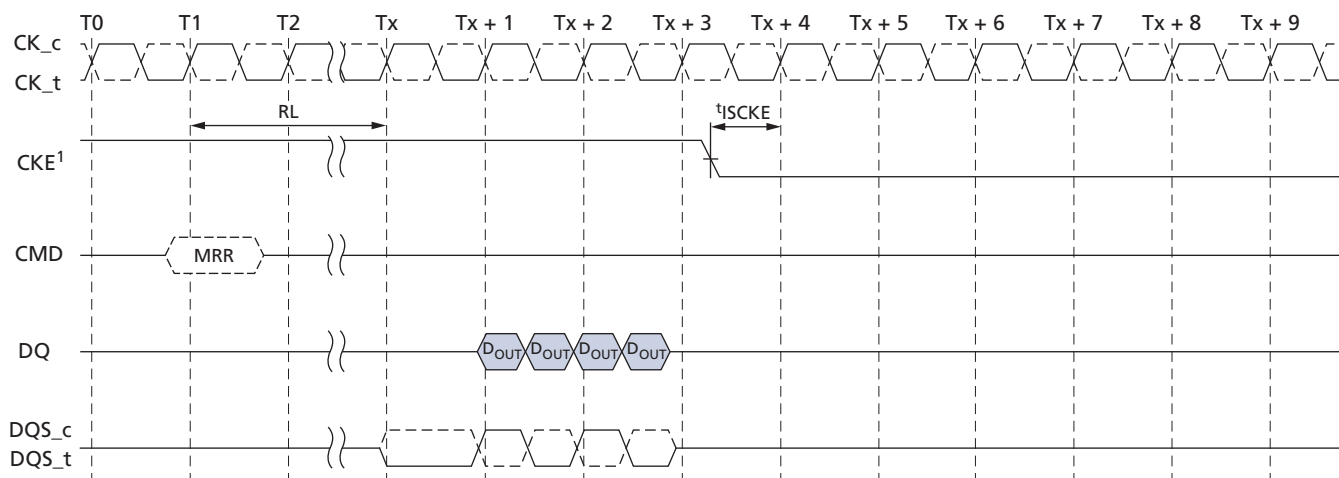


Note: 1. CKE can go LOW at  $t_{IHCKE}$  after the clock on which the ACTIVATE command is registered.

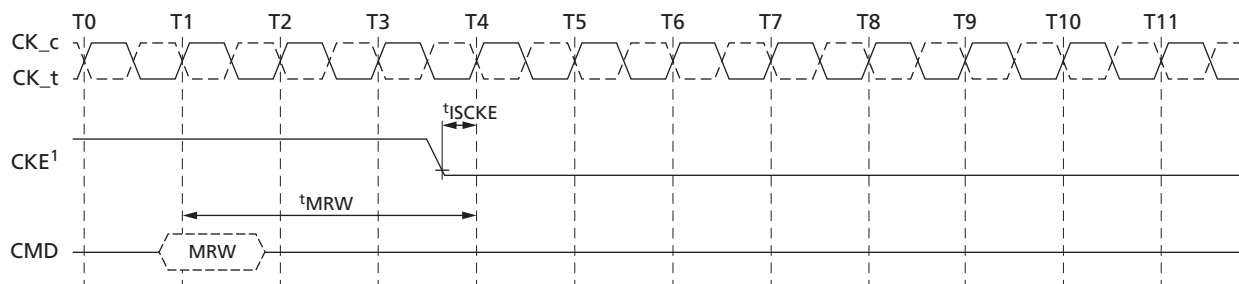
Figure 65: PRECHARGE Command to Power-Down Entry



Note: 1. CKE can go LOW  $t_{IHCKE}$  after the clock on which the PRECHARGE command is registered.


**Figure 66: MRR Command to Power-Down Entry**


Note: 1. CKE can be registered LOW at  $(RL + RU(t_{DQSC}/t_{CK}) + BL/2 + 1)$  clock cycles after the clock on which the MRR command is registered.

**Figure 67: MRW Command to Power-Down Entry**


Note: 1. CKE can be registered LOW  $t_{MRW}$  after the clock on which the MRW command is registered.

## Deep Power-Down

Deep power-down (DPD) is entered when CKE is registered LOW with CS<sub>n</sub> LOW, CA0 HIGH, CA1 HIGH, and CA2 LOW at the rising edge of the clock. The NOP command must be driven in the clock cycle following power-down entry. CKE must not go LOW while MRR or MRW operations are in progress. CKE can go LOW while other operations such as ACTIVATE, auto precharge, PRECHARGE, or REFRESH are in progress; however, deep power-down I<sub>DD</sub> specifications will not be applied until those operations complete. The contents of the array will be lost upon entering DPD mode.

In DPD mode, all input buffers except CKE, all output buffers, and the power supply to internal circuitry are disabled within the device. V<sub>REFDQ</sub> can be at any level between 0 and V<sub>DDQ</sub>, and V<sub>REFCA</sub> can be at any level between 0 and V<sub>DD2</sub> during DPD. All power supplies (including V<sub>REF</sub>) must be within the specified limits prior to exiting DPD (see AC and DC Operating Conditions).

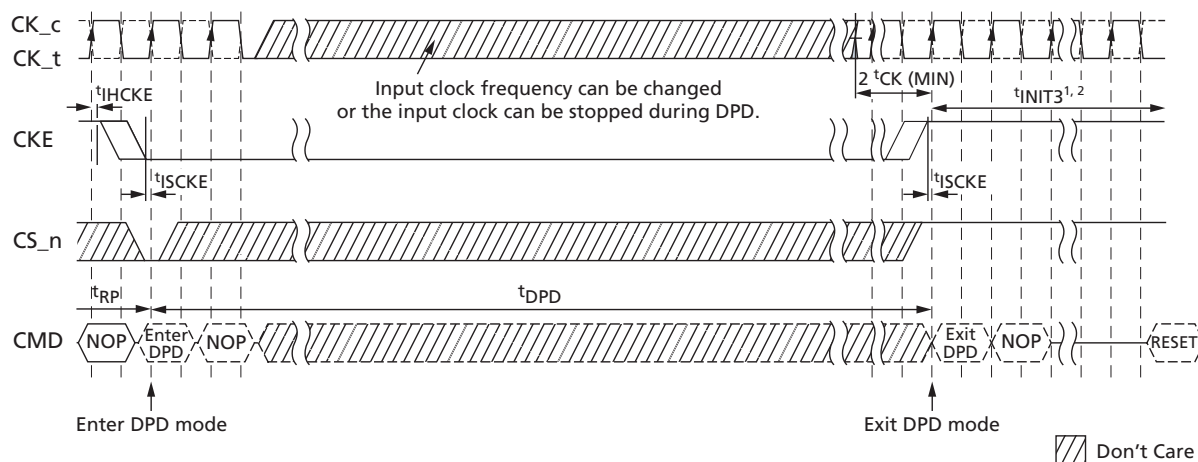


## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM

### Input Clock Frequency Changes and Stop Events

To exit DPD, CKE must be HIGH,  $t_{\text{ISCKE}}$  must be complete, and the clock must be stable. To resume operation, the device must be fully reinitialized using the power-up initialization sequence.

**Figure 68: Deep Power-Down Entry and Exit Timing**



- Notes:
1. The initialization sequence can start at any time after  $T_x + 1$ .
  2.  $t_{\text{INIT3}}$  and  $T_x + 1$  refer to timings in the initialization sequence. For details, see Mode Register Definition.

## Input Clock Frequency Changes and Stop Events

### Input Clock Frequency Changes and Clock Stop with CKE LOW

During CKE LOW, the mobile LPDDR2 device supports input clock frequency changes and clock stop under the following conditions:

- Refresh requirements are met
- Only REFab or REFpb commands can be in process
- Any ACTIVATE or PRECHARGE commands have completed prior to changing the frequency
- Related timing conditions,  $t_{\text{RCD}}$  and  $t_{\text{RP}}$ , have been met prior to changing the frequency
- The initial clock frequency must be maintained for a minimum of two clock cycles after CKE goes LOW
- The clock satisfies  $t_{\text{CH(abs)}}$  and  $t_{\text{CL(abs)}}$  for a minimum of two clock cycles prior to CKE going HIGH

For input clock frequency changes,  $t_{\text{CK(MIN)}}$  and  $t_{\text{CK(MAX)}}$  must be met for each clock cycle.

After the input clock frequency is changed and CKE is held HIGH, additional MRW commands may be required to set the WR, RL, etc. These settings may require adjustment to meet minimum timing requirements at the target clock frequency.

For clock stop, CK\_t is held LOW and CK\_c is held HIGH.





## Input Clock Frequency Changes and Clock Stop with CKE HIGH

During CKE HIGH, the LPDDR2 device supports input clock frequency changes and clock stop under the following conditions:

- REFRESH requirements are met
- Any ACTIVATE, READ, WRITE, PRECHARGE, MRW, or MRR commands must have completed, including any associated data bursts, prior to changing the frequency
- Related timing conditions,  $t_{RCD}$ ,  $t_{WR}$ ,  $t_{RP}$ ,  $t_{MRW}$ , and  $t_{MRR}$ , etc., are met
- CS\_n must be held HIGH
- Only REFab or REFpb commands can be in process

The device is ready for normal operation after the clock satisfies  $t_{CH(ABS)}$  and  $t_{CL(ABS)}$  for a minimum of  $2 \times t_{CK} + t_{XP}$ .

For input clock frequency changes,  $t_{CK(MIN)}$  and  $t_{CK(MAX)}$  must be met for each clock cycle.

After the input clock frequency is changed, additional MRW commands may be required to set the WR, RL, etc. These settings may require adjustment to meet minimum timing requirements at the target clock frequency.

For clock stop, CK\_t is held LOW and CK\_c is held HIGH.

## NO OPERATION Command

The NO OPERATION (NOP) command prevents the device from registering any unwanted commands issued between operations. A NOP command can be issued only at clock cycle N when the CKE level is constant for clock cycle N-1 and clock cycle N. The NOP command has two possible encodings: CS\_n HIGH at the clock rising edge N; and CS\_n LOW with CA0, CA1, CA2 HIGH at the clock rising edge N.

The NOP command will not terminate a previous operation that is still in process, such as a READ burst or WRITE burst cycle.

## Truth Tables

Truth tables provide complementary information to the state diagram. They also clarify device behavior and applicable restrictions when considering the actual state of the banks.

Unspecified operations and timings are illegal. To ensure proper operation after an illegal event, the device must be powered down and then restarted using the specified initialization sequence before normal operation can continue.

**Table 57: Command Truth Table**

Notes 1–13 apply to all parameters conditions

Command	Command Pins			CA Pins										CK Edge
	CKE		CS_n	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	
	CK(n-1)	CK(n)												
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	
	H	H	X	MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Truth Tables

**Table 57: Command Truth Table (Continued)**

Notes 1–13 apply to all parameters conditions

Command	Command Pins			CA Pins										CK Edge
	CKE		CS <sub>n</sub>	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	
	CK(n-1)	CK(n)												
MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	
	H	H	X	MA6	MA7	X								
REFRESH (per bank)	H	H	L	L	L	H	L	X						
	H	H	X	X										
REFRESH (all banks)	H	H	L	L	L	H	H	X						
	H	H	X	X										
Enter self refresh	H	L	L	L	L	H	X							
	X	L	X	X										
ACTIVATE (bank)	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	BA2	
	H	H	X	R0	R1	R2	R3	R4	R5	R6	R7	R13	R14	
WRITE (bank)	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2	
	H	H	X	AP	C3	C4	C5	C6	C7	C8	C9	C10	C11	
READ (bank)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2	
	H	H	X	AP	C3	C4	C5	C6	C7	C8	C9	C10	C11	
PRECHARGE (bank)	H	H	L	H	H	L	H	AB	X	X	BA0	BA1	BA2	
	H	H	X	X										
BST	H	H	L	H	H	L	L	X						
	H	H	X	X										
Enter DPD	H	L	L	H	H	L	X							
	X	L	X	X										
NOP	H	H	L	H	H	H	X							
	H	H	X	X										
Maintain PD, SREF, DPD, (NOP)	L	L	L	H	H	H	X							
	L	L	X	X										
NOP	H	H	H	X										
	H	H	X	X										
Maintain PD, SREF, DPD, (NOP)	L	L	H	X										
	L	L	X	X										
Enter power- down	H	L	H	X										
	X	L	X	X										


**Table 57: Command Truth Table (Continued)**

Notes 1–13 apply to all parameters conditions

Command	Command Pins			CA Pins									CK Edge	
	CKE		CS <sub>n</sub>	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8		CA9
	CK(n-1)	CK(n)												
Exit PD, SREF, DPD	L	H	H	X										
	X	H	X	X										

- Notes:
- All commands are defined by the current state of CS<sub>n</sub>, CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock.
  - Bank addresses (BA) determine which bank will be operated upon.
  - AP HIGH during a READ or WRITE command indicates that an auto precharge will occur to the bank associated with the READ or WRITE command.
  - X indicates a "Don't Care" state, with a defined logic level, either HIGH (H) or LOW (L).
  - Self refresh exit and DPD exit are asynchronous.
  - V<sub>REF</sub> must be between 0 and V<sub>DDQ</sub> during self refresh and DPD operation.
  - CA<sub>xr</sub> refers to command/address bit "x" on the rising edge of clock.
  - CA<sub>xf</sub> refers to command/address bit "x" on the falling edge of clock.
  - CS<sub>n</sub> and CKE are sampled on the rising edge of the clock.
  - Per-bank refresh is supported only in devices with eight banks.
  - The least-significant column address C0 is not transmitted on the CA bus, and is inferred to be zero.
  - RFU needs to input "H" or "L" (but a defined logic level).
  - AB "high" during Precharge command indicates that all bank Precharge will occur. In this case, Bank Address is don't care.

**Table 58: CKE Truth Table**

Notes 1–5 apply to all parameters and conditions; L = LOW, H = HIGH, X = "Don't Care"

Current State	CKE <sub>n-1</sub>	CKE <sub>n</sub>	CS <sub>n</sub>	Command <i>n</i>	Operation <i>n</i>	Next State	Notes
Active power-down	L	L	X	X	Maintain active power-down	Active power-down	
	L	H	H	NOP	Exit active power-down	Active	6, 7
Idle power-down	L	L	X	X	Maintain idle power-down	Idle power-down	
	L	H	H	NOP	Exit idle power-down	Idle	6, 7
Resetting idle power-down	L	L	X	X	Maintain resetting power-down	Resetting power-down	
	L	H	H	NOP	Exit resetting power-down	Idle or resetting	6, 7, 8
Deep power-down	L	L	X	X	Maintain deep power-down	Deep power-down	
	L	H	H	NOP	Exit deep power-down	Power-on	9
Self refresh	L	L	X	X	Maintain self refresh	Self refresh	
	L	H	H	NOP	Exit self refresh	Idle	10, 11
Bank(s) active	H	L	H	NOP	Enter active power-down	Active power-down	


**Table 58: CKE Truth Table (Continued)**

Notes 1–5 apply to all parameters and conditions; L = LOW, H = HIGH, X = “Don’t Care”

Current State	CKEn-1	CKEn	CS_n	Command n	Operation n	Next State	Notes	
All banks idle	H	L	H	NOP	Enter idle power-down	Idle power-down		
	H	L	L	Enter self refresh	Enter self refresh	Self refresh		
	H	L	L	DPD	Enter deep power-down	Deep power-down		
Resetting	H	L	H	NOP	Enter resetting power-down	Resetting power-down		
Other states	H	H	Refer to the command truth table					

- Notes:
1. Current state = the state of the device immediately prior to the clock rising edge  $n$ .
  2. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
  3. CKEn = the logic state of CKE at clock rising edge  $n$ ; CKEn-1 was the state of CKE at the previous clock edge.
  4. CS\_n = the logic state of CS\_n at the clock rising edge  $n$ .
  5. Command  $n$  = the command registered at clock edge  $n$ , and operation  $n$  is a result of command  $n$ .
  6. Power-down exit time ( $t^{\text{XP}}$ ) must elapse before any command other than NOP is issued.
  7. The clock must toggle at least twice prior to the  $t^{\text{XP}}$  period.
  8. Upon exiting the resetting power-down state, the device will return to the idle state if  $t^{\text{INIT5}}$  has expired.
  9. The DPD exit procedure must be followed as described in Deep Power Down.
  10. Self refresh exit time ( $t^{\text{XSR}}$ ) must elapse before any command other than NOP is issued.
  11. The clock must toggle at least twice prior to the  $t^{\text{XSR}}$  time.

**Table 59: Current State Bank  $n$  to Command to Bank  $n$  Truth Table**

Notes 1–5 apply to all parameters and conditions

Current State	Command	Operation	Next State	Notes
Any	NOP	Continue previous operation	Current state	
Idle	ACTIVATE	Select and activate row	Active	
	Refresh (per bank)	Begin to refresh	Refreshing (per bank)	6
	Refresh (all banks)	Begin to refresh	Refreshing (all banks)	7
	MRW	Load value to mode register	MR writing	7
	MRR	Read value from mode register	Idle, MR reading	
	RESET	Begin device auto initialization	Resetting	7, 8
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	9, 10
Row active	READ	Select column and start read burst	Reading	
	WRITE	Select column and start write burst	Writing	
	MRR	Read value from mode register	Active MR reading	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	9


**Table 59: Current State Bank *n* to Command to Bank *n* Truth Table (Continued)**

Notes 1–5 apply to all parameters and conditions

Current State	Command	Operation	Next State	Notes
Reading	READ	Select column and start new read burst	Reading	11, 12
	WRITE	Select column and start write burst	Writing	11, 12, 13
	BST	Read burst terminate	Active	14
Writing	WRITE	Select column and start new write burst	Writing	11, 12
	READ	Select column and start read burst	Reading	11, 12, 15
	BST	Write burst terminate	Active	14
Power-on	RESET	Begin device auto initialization	Resetting	7, 9
Resetting	MRR	Read value from mode register	Resetting MR reading	

- Notes:
- Values in this table apply when both  $CKEn - 1$  and  $CKEn$  are HIGH, and after  $t^{\text{XSR}}$  or  $t^{\text{XP}}$  has been met, if the previous state was power-down.
  - All states and sequences not shown are illegal or reserved.
  - Current state definitions:
    - Idle: The bank or banks have been precharged, and  $t^{\text{RP}}$  has been met.
    - Active: A row in the bank has been activated, and  $t^{\text{RCD}}$  has been met. No data bursts or accesses and no register accesses are in progress.
    - Reading: A READ burst has been initiated with auto precharge disabled and has not yet terminated or been terminated.
    - Writing: A WRITE burst has been initiated with auto precharge disabled and has not yet terminated or been terminated.
  - These states must not be interrupted by a command issued to the same bank. NOP commands or supported commands to the other bank must be issued on any clock edge occurring during these states. Supported commands to the other banks are determined by that bank's current state and the definitions given here.
    - Precharge: Starts with registration of a PRECHARGE command and ends when  $t^{\text{RP}}$  is met. After  $t^{\text{RP}}$  is met, the bank is in the idle state.
    - Row activate: Starts with registration of an ACTIVATE command and ends when  $t^{\text{RCD}}$  is met. After  $t^{\text{RCD}}$  is met, the bank is in the active state.
    - READ with AP enabled: Starts with registration of a READ command with auto precharge enabled and ends when  $t^{\text{RP}}$  is met. After  $t^{\text{RP}}$  is met, the bank is in the idle state.
    - WRITE with AP enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when  $t^{\text{RP}}$  is met. After  $t^{\text{RP}}$  is met, the bank is in the idle state.
  - These states must not be interrupted by any executable command. NOP commands must be applied to each rising clock edge during these states.
    - Refresh (per bank): Starts with registration of a REFRESH (per bank) command and ends when  $t^{\text{RFCpb}}$  is met. After  $t^{\text{RFCpb}}$  is met, the bank is in the idle state.
    - Refresh (all banks): Starts with registration of a REFRESH (all banks) command and ends when  $t^{\text{RFCab}}$  is met. After  $t^{\text{RFCab}}$  is met, the device is in the all banks idle state.
    - Idle MR reading: Starts with registration of the MRR command and ends when  $t^{\text{MRR}}$  is met. After  $t^{\text{MRR}}$  is met, the device is in the all banks idle state.



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Resetting MR reading: Starts with registration of the MRR command and ends when  $t^{\text{MRR}}$  is met. After  $t^{\text{MRR}}$  is met, the device is in the all banks idle state.

Active MR reading: Starts with registration of the MRR command and ends when  $t^{\text{MRR}}$  is met. After  $t^{\text{MRR}}$  is met, the bank is in the active state.

MR writing: Starts with registration of the MRW command and ends when  $t^{\text{MRW}}$  is met. After  $t^{\text{MRW}}$  is met, the device is in the all banks idle state.

Precharging all: Starts with registration of a PRECHARGE ALL command and ends when  $t^{\text{RP}}$  is met. After  $t^{\text{RP}}$  is met, the device is in the all banks idle state.

6. Bank-specific; requires that the bank is idle and no bursts are in progress.
7. Not bank-specific; requires that all banks are idle and no bursts are in progress.
8. Not bank-specific.
9. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
10. If a PRECHARGE command is issued to a bank in the idle state,  $t^{\text{RP}}$  still applies.
11. A command other than NOP should not be issued to the same bank while a burst READ or burst WRITE with auto precharge is enabled.
12. The new READ or WRITE command could be auto precharge enabled or auto precharge disabled.
13. A WRITE command can be issued after the completion of the READ burst; otherwise, a BST must be issued to end the READ prior to asserting a WRITE command.
14. Not bank-specific. The BST command affects the most recent READ/WRITE burst started by the most recent READ/WRITE command, regardless of bank.
15. A READ command can be issued after completion of the WRITE burst; otherwise, a BST must be used to end the WRITE prior to asserting another READ command.

**Table 60: Current State Bank  $n$  to Command to Bank  $m$  Truth Table**

Notes 1–6 apply to all parameters and conditions

Current State of Bank $n$	Command to Bank $m$	Operation	Next State for Bank $m$	Notes
Any	NOP	Continue previous operation	Current state of bank $m$	
Idle	Any	Any command supported to bank $m$	–	7
Row activating, active, or pre-charging	ACTIVATE	Select and activate row in bank $m$	Active	8
	READ	Select column and start READ burst from bank $m$	Reading	9
	WRITE	Select column and start WRITE burst to bank $m$	Writing	9
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	10
	MRR	READ value from mode register	Idle MR reading or active MR reading	11, 12, 13
	BST	READ or WRITE burst terminates an on-going READ/WRITE from/to bank $m$	Active	7


**Table 60: Current State Bank *n* to Command to Bank *m* Truth Table (Continued)**

Notes 1–6 apply to all parameters and conditions

Current State of Bank <i>n</i>	Command to Bank <i>m</i>	Operation	Next State for Bank <i>m</i>	Notes
Reading (auto precharge disabled)	READ	Select column and start READ burst from bank <i>m</i>	Reading	9
	WRITE	Select column and start WRITE burst to bank <i>m</i>	Writing	9, 14
	ACTIVATE	Select and activate row in bank <i>m</i>	Active	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	10
Writing (auto precharge disabled)	READ	Select column and start READ burst from bank <i>m</i>	Reading	9, 15
	WRITE	Select column and start WRITE burst to bank <i>m</i>	Writing	9
	ACTIVATE	Select and activate row in bank <i>m</i>	Active	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	10
Reading with auto precharge	READ	Select column and start READ burst from bank <i>m</i>	Reading	9, 16
	WRITE	Select column and start WRITE burst to bank <i>m</i>	Writing	9, 14, 16
	ACTIVATE	Select and activate row in bank <i>m</i>	Active	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	10
Writing with auto precharge	READ	Select column and start READ burst from bank <i>m</i>	Reading	9, 15, 16
	WRITE	Select column and start WRITE burst to bank <i>m</i>	Writing	9, 16
	ACTIVATE	Select and activate row in bank <i>m</i>	Active	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	10
Power-on	RESET	Begin device auto initialization	Resetting	17, 18
Resetting	MRR	Read value from mode register	Resetting MR reading	

- Notes:
1. This table applies when: the previous state was self refresh or power-down; after <sup>t</sup>XSR or <sup>t</sup>XP has been met; *and* both CKEn -1 and CKEn are HIGH.
  2. All states and sequences not shown are illegal or reserved.
  3. Current state definitions:

Idle: The bank has been precharged and <sup>t</sup>RP has been met.

Active: A row in the bank has been activated, <sup>t</sup>RCD has been met, no data bursts or accesses and no register accesses are in progress.

Read: A READ burst has been initiated with auto precharge disabled and the READ has not yet terminated or been terminated.

Write: A WRITE burst has been initiated with auto precharge disabled and the WRITE has not yet terminated or been terminated.

4. Refresh, self refresh, and MRW commands can be issued only when all banks are idle.



5. A BST command cannot be issued to another bank; it applies only to the bank represented by the current state.
6. These states must not be interrupted by any executable command. NOP commands must be applied during each clock cycle while in these states:
  - Idle MRR: Starts with registration of the MRR command and ends when  $t^{\text{MRR}}$  has been met. After  $t^{\text{MRR}}$  is met, the device is in the all banks idle state.
  - Reset MRR: Starts with registration of the MRR command and ends when  $t^{\text{MRR}}$  has been met. After  $t^{\text{MRR}}$  is met, the device is in the all banks idle state.
  - Active MRR: Starts with registration of the MRR command and ends when  $t^{\text{MRR}}$  has been met. After  $t^{\text{MRR}}$  is met, the bank is in the active state.
  - MRW: Starts with registration of the MRW command and ends when  $t^{\text{MRW}}$  has been met. After  $t^{\text{MRW}}$  is met, the device is in the all banks idle state.
7. BST is supported only if a READ or WRITE burst is ongoing.
8.  $t^{\text{RRD}}$  must be met between the ACTIVATE command to bank  $n$  and any subsequent ACTIVATE command to bank  $m$ .
9. READs or WRITEs listed in the command column include READs and WRITEs with or without auto precharge enabled.
10. This command may or may not be bank-specific. If all banks are being precharged, they must be in a valid state for precharging.
11. MRR is supported in the row-activating state.
12. MRR is supported in the precharging state.
13. The next state for bank  $m$  depends on the current state of bank  $m$  (idle, row-activating, precharging, or active).
14. A WRITE command can be issued after the completion of the READ burst; otherwise a BST must be issued to end the READ prior to asserting a WRITE command.
15. A READ command can be issued after the completion of the WRITE burst; otherwise, a BST must be issued to end the WRITE prior to asserting another READ command.
16. A READ with auto precharge enabled or a WRITE with auto precharge enabled can be followed by any valid command to other banks provided that the timing restrictions in the PRECHARGE and Auto Precharge Clarification table are met.
17. Not bank-specific; requires that all banks are idle and no bursts are in progress.
18. RESET command is achieved through MODE REGISTER WRITE command.

**Table 61: DM Truth Table**

Functional Name	DM	DQ	Notes
Write enable	L	Valid	1
Write inhibit	H	X	1

Note: 1. Used to mask write data, and is provided simultaneously with the corresponding input data.





## Absolute Maximum Ratings

Stresses greater than those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

**Table 62: Absolute Maximum DC Ratings**

Parameter	Symbol	Min	Max	Unit	Notes
V <sub>DD1</sub> supply voltage relative to V <sub>SS</sub>	V <sub>DD1</sub>	-0.4	+2.3	V	1
V <sub>DD2</sub> supply voltage relative to V <sub>SS</sub>	V <sub>DD2</sub> (1.2V)	-0.4	+1.6	V	1
V <sub>DDQ</sub> supply voltage relative to V <sub>SSQ</sub>	V <sub>DDQ</sub>	-0.4	+1.6	V	1, 3
Voltage on any ball relative to V <sub>SS</sub>	V <sub>IN</sub> , V <sub>OUT</sub>	-0.4	+1.6	V	
Storage temperature	T <sub>STG</sub>	-55	+125	°C	4

- Notes:
- See 1. Voltage Ramp under Power Up.
  - V<sub>REFCA</sub> 0.6 ≤ V<sub>DD2</sub>; however, V<sub>REFCA</sub> may be ≥ V<sub>DD2</sub> provided that V<sub>REFCA</sub> ≤ 300mV.
  - V<sub>REFDQ</sub> 0.6 ≤ V<sub>DDQ</sub>; however, V<sub>REFDQ</sub> may be ≥ V<sub>DDQ</sub> provided that V<sub>REFDQ</sub> ≤ 300mV.
  - Storage temperature is the case surface temperature on the center/top side of the device. For measurement conditions, refer to the JE51-2 standard.



## Input/Output Capacitance

**Table 63: Input/Output Capacitance**

Note 1 applies to all parameters and conditions

Parameter	Symbol	MIN	MAX	Unit	Notes
Input capacitance, CK and CK#	$C_{L1}$	1.0	3.0	pF	2
Input capacitance, all other LPDDR2 input only balls	$C_{L2}$	1.0	3.0	pF	2
Input/output capacitance, DQ, DM, DQS, DQS#	$C_{I/O}$	2.0	3.5	pF	2, 3
Input/output capacitance, ZQ	$C_{ZQ}$	2.0	3.0	pF	2, 3

- Notes:
1. This parameter is not subject to production testing. It is verified by design and characterization. The capacitance is measured according to JEP147 (procedure for measuring input capacitance using a vector network analyzer), with  $V_{DD1}$ ,  $V_{DD2}$ ,  $V_{DDQ}$ ,  $V_{SS}$ , and  $V_{SSQ}$  applied; all other pins are left floating.
  2. These parameters are measured on  $f = 100$  MHz,  $V_{OUT} = V_{DDQ2}$ ,  $T_A = 25^\circ\text{C}$ .
  3.  $D_{OUT}$  circuits are disabled.



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM

### Electrical Specifications – I<sub>DD</sub> Specifications and Conditions

## Electrical Specifications – I<sub>DD</sub> Specifications and Conditions

The following definitions and conditions are used in the I<sub>DD</sub> measurement tables unless stated otherwise:

- LOW:  $V_{IN} \leq V_{IL(DC)max}$
- HIGH:  $V_{IN} \geq V_{IH(DC)min}$
- STABLE: Inputs are stable at a HIGH or LOW level
- SWITCHING: See the following three tables

**Table 64: Switching for CA Input Signals**

Notes 1–3 apply to all parameters and conditions

	CK_t Rising/ CK_c Fall- ing	CK_t Fall- ing/ CK_c Rising	CK_t Rising/ CK_c Fall- ing	CK_t Fall- ing/ CK_c Rising	CK_t Rising/ CK_c Fall- ing	CK_t Fall- ing/ CK_c Rising	CK_t Rising/ CK_c Fall- ing	CK_t Fall- ing/ CK_c Rising
Cycle	N		N + 1		N + 2		N + 3	
CS_n	HIGH		HIGH		HIGH		HIGH	
CA0	H	L	L	L	L	H	H	H
CA1	H	H	H	L	L	L	L	H
CA2	H	L	L	L	L	H	H	H
CA3	H	H	H	L	L	L	L	H
CA4	H	L	L	L	L	H	H	H
CA5	H	H	H	L	L	L	L	H
CA6	H	L	L	L	L	H	H	H
CA7	H	H	H	L	L	L	L	H
CA8	H	L	L	L	L	H	H	H
CA9	H	H	H	L	L	L	L	H

- Notes:
1. CS# must always be driven HIGH.
  2. For each clock cycle, 50% of the CA bus is changing between HIGH and LOW.
  3. The noted pattern (N, N + 1, N + 2, N + 3...) is used continuously during I<sub>DD</sub> measurement for I<sub>DD</sub> values that require switching on the CA bus.

**Table 65: Switching for I<sub>DD4R</sub>**

Clock	CKE	CS_n	Clock Cycle Number	Command	CA[2:0]	CA[9:3]	All DQ
Rising	H	L	N	Read_Rising	HLH	LHLHLHL	L
Falling	H	L	N	Read_Falling	LLL	LLLLLLL	L
Rising	H	H	N + 1	NOP	LLL	LLLLLLL	H
Falling	H	H	N + 1	NOP	HLH	HLHLLHL	L
Rising	H	L	N + 2	Read_Rising	HLH	HLHLLHL	H
Falling	H	L	N + 2	Read_Falling	LLL	HHHHHHH	H
Rising	H	H	N + 3	NOP	LLL	HHHHHHH	H



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM

### Electrical Specifications – I<sub>DD</sub> Specifications and Conditions

**Table 65: Switching for I<sub>DD4R</sub> (Continued)**

Clock	CKE	CS_n	Clock Cycle Number	Command	CA[2:0]	CA[9:3]	All DQ
Falling	H	H	N + 3	NOP	HLH	LHLHLHL	L

- Notes: 1. Data strobe (DQS) is changing between HIGH and LOW with every clock cycle.  
 2. The noted pattern (N, N + 1...) is used continuously during I<sub>DD</sub> measurement for I<sub>DD4R</sub>.

**Table 66: Switching for I<sub>DD4W</sub>**

Clock	CKE	CS_n	Clock Cycle Number	Command	CA[2:0]	CA[9:3]	All DQ
Rising	H	L	N	Write_Rising	HLL	LHLHLHL	L
Falling	H	L	N	Write_Falling	LLL	LLLLLLL	L
Rising	H	H	N + 1	NOP	LLL	LLLLLLL	H
Falling	H	H	N + 1	NOP	HLH	HLHLLHL	L
Rising	H	L	N + 2	Write_Rising	HLL	HLHLLHL	H
Falling	H	L	N + 2	Write_Falling	LLL	HHHHHHH	H
Rising	H	H	N + 3	NOP	LLL	HHHHHHH	H
Falling	H	H	N + 3	NOP	HLH	LHLHLHL	L

- Notes: 1. Data strobe (DQS) is changing between HIGH and LOW with every clock cycle.  
 2. Data masking (DM) must always be driven LOW.  
 3. The noted pattern (N, N + 1...) is used continuously during I<sub>DD</sub> measurement for I<sub>DD4W</sub>.

**Table 67: I<sub>DD</sub> Specification Parameters and Operating Conditions**

Notes 1–3 apply to all parameters and conditions

Parameter/Condition	Symbol	Power Supply	Notes
<b>Operating one bank active-precharge current (SDRAM):</b> <sup>t</sup> CK = <sup>t</sup> CK <sub>min</sub> ; <sup>t</sup> RC = <sup>t</sup> RC <sub>min</sub> ; CKE is HIGH; CS_n is HIGH between valid commands; CA bus inputs are switching; Data bus inputs are stable	I <sub>DD01</sub>	V <sub>DD1</sub>	
	I <sub>DD02</sub>	V <sub>DD2</sub>	
	I <sub>DD0in</sub>	V <sub>DDQ</sub>	4
<b>Idle power-down standby current:</b> <sup>t</sup> CK = <sup>t</sup> CK <sub>min</sub> ; CKE is LOW; CS_n is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable	I <sub>DD2P1</sub>	V <sub>DD1</sub>	
	I <sub>DD2P2</sub>	V <sub>DD2</sub>	
	I <sub>DD2P,in</sub>	V <sub>DDQ</sub>	4
<b>Idle power-down standby current with clock stop:</b> CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is LOW; CS_n is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable	I <sub>DD2PS1</sub>	V <sub>DD1</sub>	
	I <sub>DD2PS2</sub>	V <sub>DD2</sub>	
	I <sub>DD2PS,in</sub>	V <sub>DDQ</sub>	4
<b>Idle non-power-down standby current:</b> <sup>t</sup> CK = <sup>t</sup> CK <sub>min</sub> ; CKE is HIGH; CS_n is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable	I <sub>DD2N1</sub>	V <sub>DD1</sub>	
	I <sub>DD2N2</sub>	V <sub>DD2</sub>	
	I <sub>DD2N,in</sub>	V <sub>DDQ</sub>	4



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM

### Electrical Specifications – I<sub>DD</sub> Specifications and Conditions

**Table 67: I<sub>DD</sub> Specification Parameters and Operating Conditions (Continued)**

Notes 1–3 apply to all parameters and conditions

Parameter/Condition	Symbol	Power Supply	Notes
<b>Idle non-power-down standby current with clock stopped:</b> CK <sub>t</sub> = LOW; CK <sub>c</sub> = HIGH; CKE is HIGH; CS <sub>n</sub> is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable	I <sub>DD2NS1</sub>	V <sub>DD1</sub>	
	I <sub>DD2NS2</sub>	V <sub>DD2</sub>	
	I <sub>DD2NS,in</sub>	V <sub>DDQ</sub>	4
<b>Active power-down standby current:</b> <sup>t</sup> CK = <sup>t</sup> CK <sub>min</sub> ; CKE is LOW; CS <sub>n</sub> is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable	I <sub>DD3P1</sub>	V <sub>DD1</sub>	
	I <sub>DD3P2</sub>	V <sub>DD2</sub>	
	I <sub>DD3P,in</sub>	V <sub>DDQ</sub>	4
<b>Active power-down standby current with clock stop:</b> CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is LOW; CS <sub>n</sub> is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable	I <sub>DD3PS1</sub>	V <sub>DD1</sub>	
	I <sub>DD3PS2</sub>	V <sub>DD2</sub>	
	I <sub>DD3PS,in</sub>	V <sub>DDQ</sub>	4
<b>Active non-power-down standby current:</b> <sup>t</sup> CK = <sup>t</sup> CK <sub>min</sub> ; CKE is HIGH; CS <sub>n</sub> is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable	I <sub>DD3N1</sub>	V <sub>DD1</sub>	
	I <sub>DD3N2</sub>	V <sub>DD2</sub>	
	I <sub>DD3N,in</sub>	V <sub>DDQ</sub>	4
<b>Active non-power-down standby current with clock stopped:</b> CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is HIGH; CS <sub>n</sub> is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable	I <sub>DD3NS1</sub>	V <sub>DD1</sub>	
	I <sub>DD3NS2</sub>	V <sub>DD2</sub>	
	I <sub>DD3NS,in</sub>	V <sub>DDQ</sub>	4
<b>Operating burst READ current:</b> <sup>t</sup> CK = <sup>t</sup> CK <sub>min</sub> ; CS <sub>n</sub> is HIGH between valid commands; One bank is active; BL = 4; RL = RL (MIN); CA bus inputs are switching; 50% data change each burst transfer	I <sub>DD4R1</sub>	V <sub>DD1</sub>	
	I <sub>DD4R2</sub>	V <sub>DD2</sub>	
<b>Operating burst WRITE current:</b> <sup>t</sup> CK = <sup>t</sup> CK <sub>min</sub> ; CS <sub>n</sub> is HIGH between valid commands; One bank is active; BL = 4; WL = WL <sub>min</sub> ; CA bus inputs are switching; 50% data change each burst transfer	I <sub>DD4W1</sub>	V <sub>DD1</sub>	
	I <sub>DD4W2</sub>	V <sub>DD2</sub>	
	I <sub>DD4W,in</sub>	V <sub>DDQ</sub>	4
<b>All-bank REFRESH burst current:</b> <sup>t</sup> CK = <sup>t</sup> CK <sub>min</sub> ; CKE is HIGH between valid commands; <sup>t</sup> RC = <sup>t</sup> RFC <sub>abmin</sub> ; Burst refresh; CA bus inputs are switching; Data bus inputs are stable	I <sub>DD51</sub>	V <sub>DD1</sub>	
	I <sub>DD52</sub>	V <sub>DD2</sub>	
	I <sub>DD5IN</sub>	V <sub>DDQ</sub>	4
<b>All-bank REFRESH average current:</b> <sup>t</sup> CK = <sup>t</sup> CK <sub>min</sub> ; CKE is HIGH between valid commands; <sup>t</sup> RC = <sup>t</sup> REFI; CA bus inputs are switching; Data bus inputs are stable	I <sub>DD5AB1</sub>	V <sub>DD1</sub>	
	I <sub>DD5AB2</sub>	V <sub>DD2</sub>	
	I <sub>DD5AB,in</sub>	V <sub>DDQ</sub>	4
<b>Per-bank REFRESH average current:</b> <sup>t</sup> CK = <sup>t</sup> CK <sub>min</sub> ; CKE is HIGH between valid commands; <sup>t</sup> RC = <sup>t</sup> REFI/8; CA bus inputs are switching; Data bus inputs are stable	I <sub>DD5PB1</sub>	V <sub>DD1</sub>	5
	I <sub>DD5PB2</sub>	V <sub>DD2</sub>	5
	I <sub>DD5PB,in</sub>	V <sub>DDQ</sub>	4, 5
<b>Self refresh current (–30°C to +85°C):</b> CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x self refresh rate	I <sub>DD61</sub>	V <sub>DD1</sub>	6
	I <sub>DD62</sub>	V <sub>DD2</sub>	6
	I <sub>DD6IN</sub>	V <sub>DDQ</sub>	4, 6
<b>Self refresh current (+85°C to +105°C):</b> CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable	I <sub>DD6ET1</sub>	V <sub>DD1</sub>	6, 7
	I <sub>DD6ET2</sub>	V <sub>DD2</sub>	6, 7
	I <sub>DD6ET,in</sub>	V <sub>DDQ</sub>	4, 6, 7



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM AC and DC Operating Conditions

**Table 67: I<sub>DD</sub> Specification Parameters and Operating Conditions (Continued)**

Notes 1–3 apply to all parameters and conditions

Parameter/Condition	Symbol	Power Supply	Notes
<b>Deep power-down current:</b> CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable	I <sub>DD81</sub>	V <sub>DD1</sub>	7
	I <sub>DD82</sub>	V <sub>DD2</sub>	7
	I <sub>DD8IN</sub>	V <sub>DDQ</sub>	4, 7

- Notes:
1. I<sub>DD</sub> values are the maximum of the distribution of the arithmetic mean.
  2. I<sub>DD</sub> current specifications are tested after the device is properly initialized.
  3. The 1x self refresh rate is the rate at which the device is refreshed internally during self refresh before going into the extended temperature range.
  4. Measured currents are the sum of V<sub>DDQ</sub> and V<sub>DD2</sub>.
  5. Per-bank REFRESH is only applicable for LPDDR2-S4 device densities 1Gb or higher.
  6. This is the general definition that applies to full-array self refresh. Refer to "IDD6 Full and Partial Array Self-Refresh Current" for details of Partial Array Self Refresh IDD6 specification.
  7. I<sub>DD6ET</sub> and I<sub>DD8</sub> are typical values, sampled only and not tested.

## AC and DC Operating Conditions

An operation or timing that is not specified is illegal. To ensure proper operation, the device must be initialized properly.

**Table 68: Recommended DC Operating Conditions**

Symbol	LPDDR2-S4B			Power Supply	Unit
	Min	Typ	Max		
V <sub>DD1</sub> <sup>1</sup>	1.70	1.80	1.95	Core power 1	V
V <sub>DD2</sub>	1.14	1.20	1.30	Core power 2	V
V <sub>DDQ</sub>	1.14	1.20	1.30	I/O buffer power	V

Note: 1. V<sub>DD1</sub> uses significantly less power than V<sub>DD2</sub>.

**Table 69: Input Leakage Current**

Parameter/Condition	Symbol	Min	Max	Unit	Notes
<b>Input leakage current:</b> For CA, CKE, CS <sub>n</sub> , CK <sub>t</sub> , CK <sub>c</sub> ; Any input 0V ≤ V <sub>IN</sub> ≤ V <sub>DD2</sub> ; (All other pins not under test = 0V)	I <sub>L</sub>	-2	2	μA	1
<b>V<sub>REF</sub> supply leakage current:</b> V <sub>REFDQ</sub> = V <sub>DDQ</sub> /2, or V <sub>REFCA</sub> = V <sub>DD2</sub> /2; (All other pins not under test = 0V)	I <sub>VREF</sub>	-1	1	μA	2

- Notes:
1. Although DM is for input only, the DM leakage must match the DQ and DQS<sub>t</sub>/DQS<sub>c</sub> output leakage specification.
  2. The minimum limit requirement is for testing purposes. The leakage current on V<sub>REFCA</sub> and V<sub>REFDQ</sub> pins should be minimal.



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM

### AC and DC Logic Input Measurement Levels for Single-Ended Signals

**Table 70: Operating Temperature Range**

Parameter/Condition	Symbol	Min	Max	Unit
Standard (WT) temperature range	$T_{CASE}^1$	-30	+85	°C
Industrial (IT) temperature range		-40	+85	°C
Automotive (AT) temperature range		-40	+105	°C

- Notes:
1. Operating temperature is the case surface temperature at the center of the top side of the device. For measurement conditions, refer to the JESD51-2 standard.
  2. Some applications require operation in the maximum case temperature range, between 85°C and 105°C. For some LPDDR2 devices, derating may be necessary to operate in this range (see the MR4 Device Temperature (MA[7:0] = 04h) table).
  3. Either the device operating temperature or the temperature sensor can be used to set an appropriate refresh rate, determine the need for AC timing derating, and/or monitor the operating temperature (see Temperature Sensor). When using the temperature sensor, the actual device case temperature may be higher than the  $T_{CASE}$  rating that applies for the operating temperature range. For example,  $T_{CASE}$  could be above 85°C when the temperature sensor indicates a temperature of less than 85°C.

## AC and DC Logic Input Measurement Levels for Single-Ended Signals

**Table 71: Single-Ended AC and DC Input Levels for CA and CS<sub>n</sub> Inputs**

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Unit	Notes
		Min	Max	Min	Max		
$V_{IHCA(AC)}$	AC input logic HIGH	$V_{REF} + 0.220$	Note 2	$V_{REF} + 0.300$	Note 2	V	1, 2
$V_{ILCA(AC)}$	AC input logic LOW	Note 2	$V_{REF} - 0.220$	Note 2	$V_{REF} - 0.300$	V	1, 2
$V_{IHCA(DC)}$	DC input logic HIGH	$V_{REF} + 0.130$	$V_{DD2}$	$V_{REF} + 0.200$	$V_{DD2}$	V	1
$V_{ILCA(DC)}$	DC input logic LOW	$V_{SS}$	$V_{REF} - 0.130$	$V_{SS}$	$V_{REF} - 0.200$	V	1
$V_{REFCA(DC)}$	Reference voltage for CA and CS <sub>n</sub> inputs	$0.49 \times V_{DD2}$	$0.51 \times V_{DD2}$	$0.49 \times V_{DD2}$	$0.51 \times V_{DD2}$	V	3, 4

- Notes:
1. For CA and CS<sub>n</sub> input-only pins.  $V_{REF} = V_{REFCA(DC)}$ .
  2. See Overshoot and Undershoot Definition.
  3. The AC peak noise on  $V_{REFCA}$  could prevent  $V_{REFCA}$  from deviating more than  $\pm 1\% V_{DD2}$  from  $V_{REFCA(DC)}$  (for reference, approximately  $\pm 12mV$ ).
  4. For reference, approximately  $V_{DD2}/2 \pm 12mV$ .

**Table 72: Single-Ended AC and DC Input Levels for CKE**

Symbol	Parameter	Min	Max	Unit	Notes
$V_{IHCKE}$	CKE input HIGH level	$0.8 \times V_{DD2}$	Note 1	V	1
$V_{ILCKE}$	CKE input LOW level	Note 1	$0.2 \times V_{DD2}$	V	1

- Note:
1. See Overshoot and Undershoot Definition.



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM

### AC and DC Logic Input Measurement Levels for Single-Ended Signals

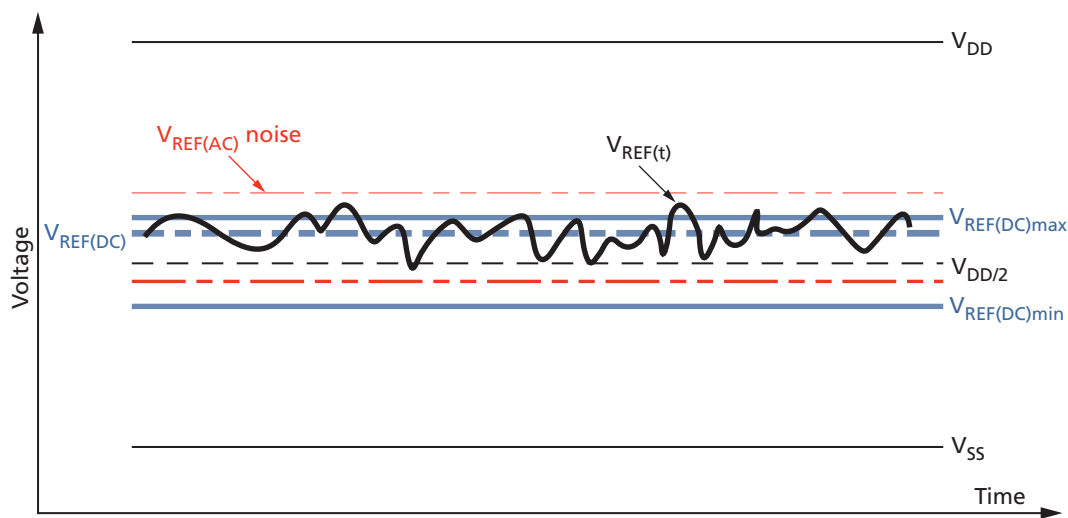
**Table 73: Single-Ended AC and DC Input Levels for DQ and DM**

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Unit	Notes
		Min	Max	Min	Max		
$V_{IHDQ(AC)}$	AC input logic HIGH	$V_{REF} + 0.220$	Note 2	$V_{REF} + 0.300$	Note 2	V	1, 2
$V_{ILDQ(AC)}$	AC input logic LOW	Note 2	$V_{REF} - 0.220$	Note 2	$V_{REF} - 0.300$	V	1, 2
$V_{IHDQ(DC)}$	DC input logic HIGH	$V_{REF} + 0.130$	$V_{DDQ}$	$V_{REF} + 0.200$	$V_{DDQ}$	V	1
$V_{ILDQ(DC)}$	DC input logic LOW	$V_{SS}$	$V_{REF} - 0.130$	$V_{SS}$	$V_{REF} - 0.200$	V	1
$V_{REFDQ(DC)}$	Reference voltage for DQ and DM inputs	$0.49 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	$0.49 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	3, 4

- Notes:
1. For DQ input-only pins.  $V_{REF} = V_{REFDQ(DC)}$ .
  2. See Overshoot and Undershoot Definition.
  3. The AC peak noise on  $V_{REFDQ}$  could prevent  $V_{REFDQ}$  from deviating more than  $\pm 1\% V_{DDQ}$  from  $V_{REFDQ(DC)}$  (for reference, approximately  $\pm 12mV$ ).
  4. For reference, approximately.  $V_{DDQ}/2 \pm 12mV$ .

## $V_{REF}$ Tolerances

The DC tolerance limits and AC noise limits for the reference voltages  $V_{REFCA}$  and  $V_{REFDQ}$  are illustrated below. This figure shows a valid reference voltage  $V_{REF}(t)$  as a function of time.  $V_{DD}$  is used in place of  $V_{DD2}$  for  $V_{REFCA}$ , and  $V_{DDQ}$  for  $V_{REFDQ}$ .  $V_{REF(DC)}$  is the linear average of  $V_{REF}(t)$  over a very long period of time (for example, 1 second) and is specified as a fraction of the linear average of  $V_{DDQ}$  or  $V_{DD2}$ , also over a very long period of time (for example, 1 second). This average must meet the MIN/MAX requirements in the Single-Ended AC and DC Input Levels for CA and CS<sub>n</sub> Inputs table. Additionally,  $V_{REF}(t)$  can temporarily deviate from  $V_{REF(DC)}$  by no more than  $\pm 1\% V_{DD}$ .  $V_{REF}(t)$  cannot track noise on  $V_{DDQ}$  or  $V_{DD2}$  if doing so would force  $V_{REF}$  outside these specifications.

**Figure 69:  $V_{REF}$  DC Tolerance and  $V_{REF}$  AC Noise Limits**






## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM

### AC and DC Logic Input Measurement Levels for Single-Ended Signals

The voltage levels for setup and hold time measurements  $V_{IH(AC)}$ ,  $V_{IH(DC)}$ ,  $V_{IL(AC)}$ , and  $V_{IL(DC)}$  are dependent on  $V_{REF}$ .

$V_{REF}$  DC variations affect the absolute voltage a signal must reach to achieve a valid HIGH or LOW, as well as the time from which setup and hold times are measured. When  $V_{REF}$  is outside the specified levels, devices will function correctly with appropriate timing deratings as long as:

- $V_{REF}$  is maintained between  $0.44 \times V_{DDQ}$  (or  $V_{DD2}$ ) and  $0.56 \times V_{DDQ}$  (or  $V_{DD2}$ ), *and*
- the controller achieves the required single-ended AC and DC input levels from instantaneous  $V_{REF}$  (see the Single-Ended AC and DC Input Levels for CA and CS\_n Inputs table).

System timing and voltage budgets must account for  $V_{REF}$  deviations outside this range.

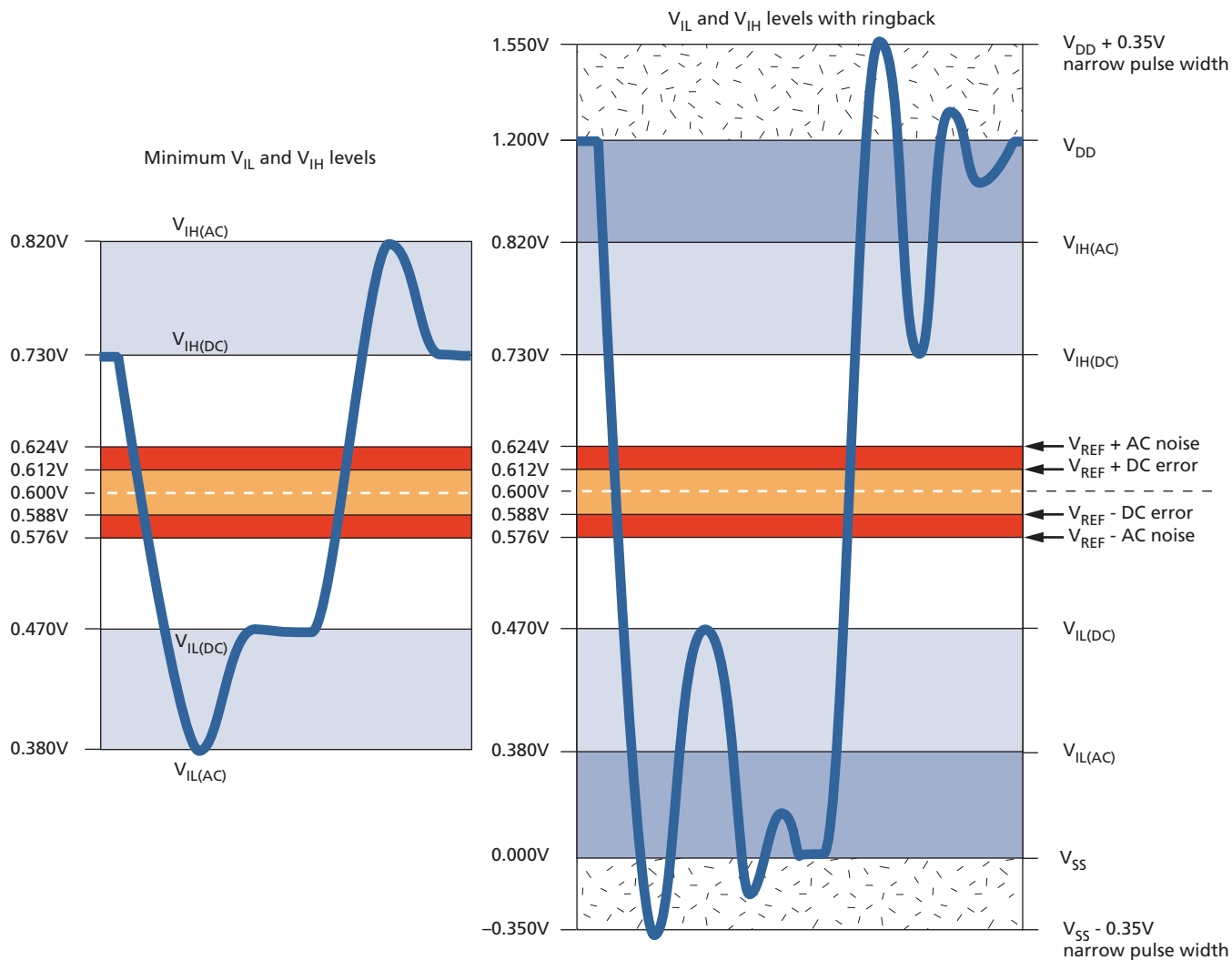
The setup/hold specification and derating values must include time and voltage associated with  $V_{REF}$  AC noise. Timing and voltage effects due to AC noise on  $V_{REF}$  up to the specified limit ( $\pm 1\% V_{DD}$ ) are included in LPDDR2 timings and their associated deratings.



# 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM AC and DC Logic Input Measurement Levels for Single-Ended Signals

## Input Signal

Figure 70: LPDDR2-466 to LPDDR2-1066 Input Signal

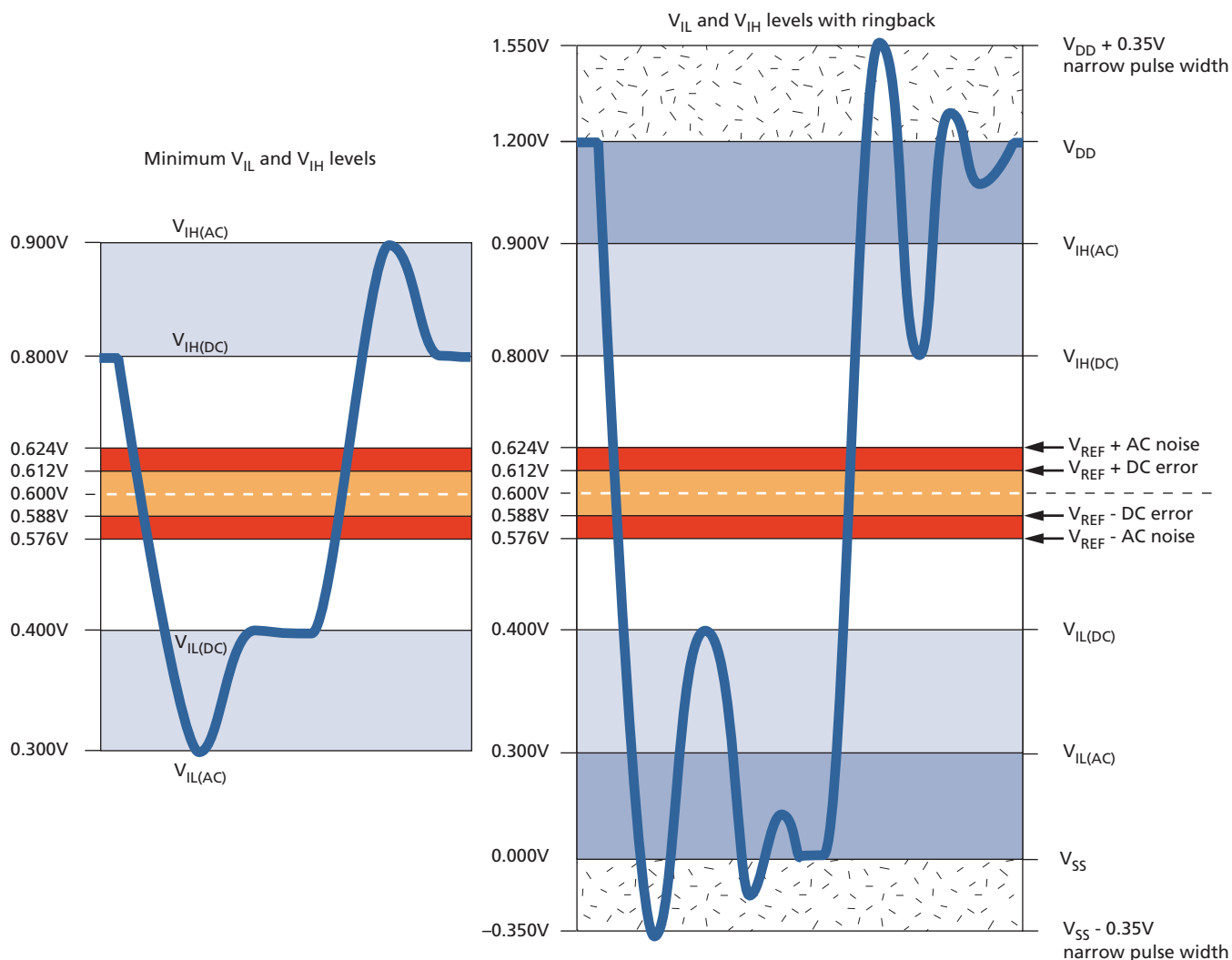


- Notes:
1. Numbers reflect typical values.
  2. For CA[9:0], CK\_t, CK\_c, and CS\_n  $V_{DD}$  stands for  $V_{DD2}$ . For DQ, DM, DQS\_t, and DQS\_c,  $V_{DD}$  stands for  $V_{DDQ}$ .
  3. For CA[9:0], CK\_t, CK\_c, and CS\_n are  $V_{SS}$ . For DQ, DM, DQS\_t, and DQS\_c,  $V_{SS}$  stands for  $V_{SSQ}$ .



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM AC and DC Logic Input Measurement Levels for Single-Ended Signals

**Figure 71: LPDDR2-200 to LPDDR2-400 Input Signal**



- Notes:
1. Numbers reflect typical values.
  2. For CA[9:0], CK\_t, CK\_c, and CS\_n  $V_{DD}$  stands for  $V_{DD2}$ . For DQ, DM, DQS\_t, and DQS\_c,  $V_{DD}$  stands for  $V_{DDQ}$ .
  3. For CA[9:0], CK\_t, CK\_c, and CS\_n are  $V_{SS}$ . For DQ, DM, DQS\_t, and DQS\_c,  $V_{SS}$  stands for  $V_{SSQ}$ .



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM AC and DC Logic Input Measurement Levels for Differential Signals

### AC and DC Logic Input Measurement Levels for Differential Signals

Figure 72: Differential AC Swing Time and  $t_{DVAC}$

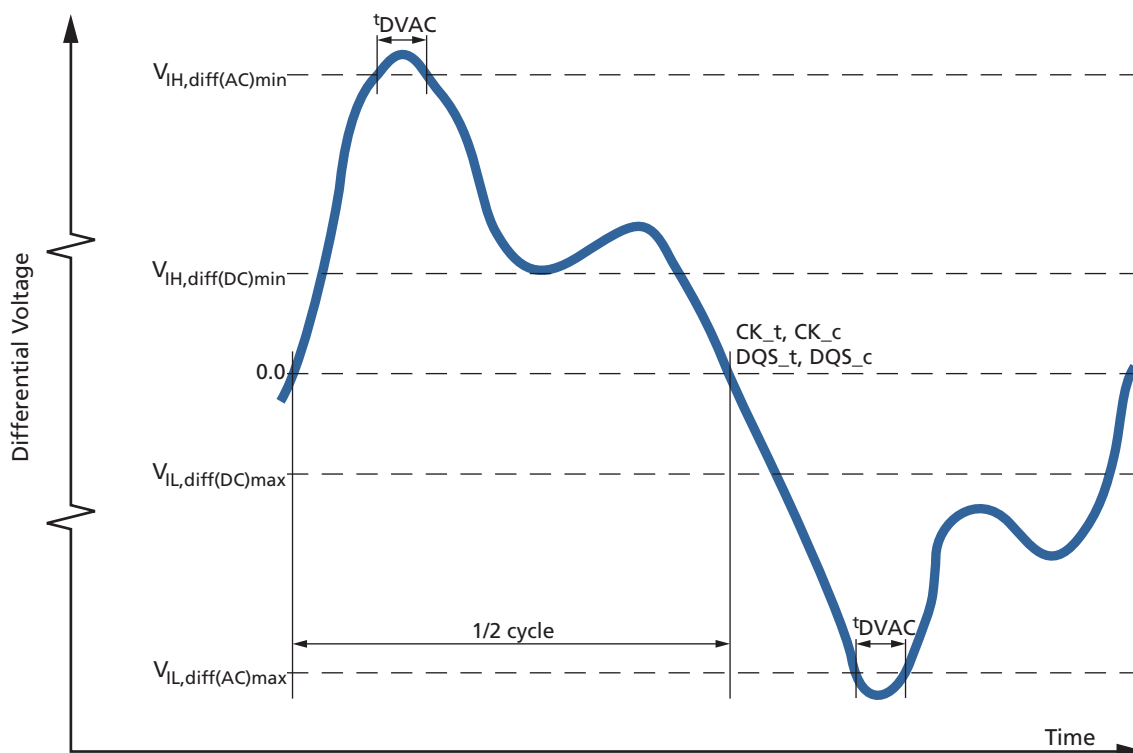


Table 74: Differential AC and DC Input Levels

For CK\_t and CK\_c,  $V_{REF} = V_{REFCA(DC)}$ ; For DQS\_t and DQS\_c  $V_{REF} = V_{REFDQ(DC)}$

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Unit	Notes
		Min	Max	Min	Max		
$V_{IH,diff(AC)}$	Differential input HIGH AC	$2 \times (V_{IH(AC)} - V_{REF})$	Note 1	$2 \times (V_{IH(AC)} - V_{REF})$	Note 1	V	2
$V_{IL,diff(AC)}$	Differential input LOW AC	Note 1	$2 \times (V_{IL(AC)} - V_{REF})$	Note 1	$2 \times (V_{IL(AC)} - V_{REF})$	V	2
$V_{IH,diff(DC)}$	Differential input HIGH	$2 \times (V_{IH(DC)} - V_{REF})$	Note 1	$2 \times (V_{IH(DC)} - V_{REF})$	Note 1	V	3
$V_{IL,diff(DC)}$	Differential input LOW	Note 1	$2 \times (V_{IL(DC)} - V_{REF})$	Note 1	$2 \times (V_{IL(DC)} - V_{REF})$	V	3

- Notes: 1. These values are not defined, however the single-ended signals CK\_t, CK\_c, DQS\_t, and DQS\_c must be within the respective limits ( $V_{IH(DC)max}$ ,  $V_{IL(DC)min}$ ) for single-ended signals and must comply with the specified limitations for overshoot and undershoot (see Overshoot and Undershoot Definitions).



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM AC and DC Logic Input Measurement Levels for Differential Signals

- For CK\_t and CK\_c, use  $V_{IH}/V_{IL(AC)}$  of CA and  $V_{REFCA}$ ; for DQS\_t and DQS\_c, use  $V_{IH}/V_{IL(AC)}$  of DQ and  $V_{REFDQ}$ . If a reduced AC HIGH or AC LOW is used for a signal group, the reduced voltage level also applies.
- Used to define a differential signal slew rate. For CK\_t - CK\_c use  $V_{IH}/V_{IL(dc)}$  of CA and  $V_{REFCA}$ ; for DQS\_t - DQS\_c, use  $V_{IH}/V_{IL(dc)}$  of DQs and  $V_{REFDQ}$ ; if a reduced dc-high or dc-low level is used for a signal group, then the reduced level applies also here.

**Table 75: CK\_t/CK\_c and DQS\_t/DQS\_c Time Requirements Before Ringback ( $t^{DVAC}$ )**

Slew Rate (V/ns)	$t^{DVAC}$ (ps) at $V_{IH}/V_{ILdiff(AC)} = 440mV$	$t^{DVAC}$ (ps) at $V_{IH}/V_{ILdiff(AC)} = 600mV$
	Min	Min
> 4.0	175	75
4.0	170	57
3.0	167	50
2.0	163	38
1.8	162	34
1.6	161	29
1.4	159	22
1.2	155	13
1.0	150	0
< 1.0	150	0

### Single-Ended Requirements for Differential Signals

Each individual component of a differential signal (CK\_t, CK\_c, DQS\_t, and DQS\_c) must also comply with certain requirements for single-ended signals.

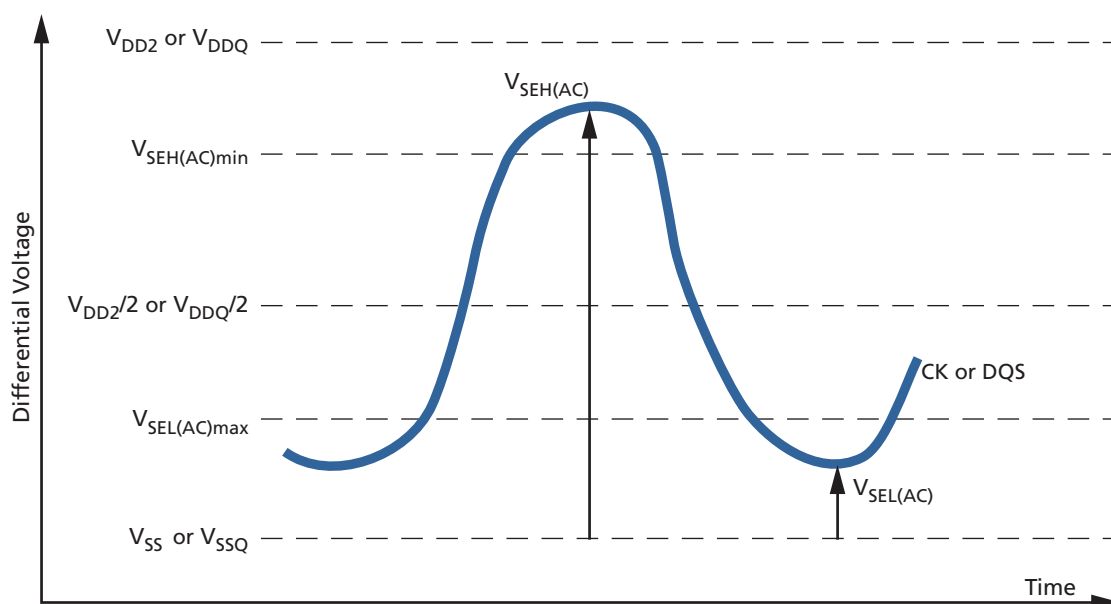
CK\_t and CK\_c must meet  $V_{SEH(AC)min}/V_{SEL(AC)max}$  in every half cycle. DQS\_t, DQS\_c must meet  $V_{SEH(AC)min}/V_{SEL(AC)max}$  in every half cycle preceding and following a valid transition.

The applicable AC levels for CA and DQ differ by speed bin.



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM AC and DC Logic Input Measurement Levels for Differential Signals

**Figure 73: Single-Ended Requirements for Differential Signals**



While CA and DQ signal requirements are referenced to  $V_{REF}$ , the single-ended components of differential signals also have a requirement with respect to  $V_{DDQ}/2$  for DQS, and  $V_{DD2}/2$  for CK.

The transition of single-ended signals through the AC levels is used to measure setup time. For single-ended components of differential signals, the requirement to reach  $V_{SEL(AC)max}$  or  $V_{SEH(AC)min}$  has no bearing on timing. This requirement does, however, add a restriction on the common mode characteristics of these signals (see Single-Ended AC and DC Input Levels for CA and CS<sub>n</sub> Inputs for CK<sub>t</sub>/CK<sub>c</sub> single-ended requirements, and Single-Ended AC and DC Input Levels for DQ and DM for DQ and DQM single-ended requirements).

**Table 76: Single-Ended Levels for CK<sub>t</sub>, CK<sub>c</sub>, DQS<sub>t</sub>, DQS<sub>c</sub>**

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Unit	Notes
		Min	Max	Min	Max		
$V_{SEH(AC)}$	Single-ended HIGH level for strobes	$(V_{DDQ}/2) + 0.220$	Note 1	$(V_{DDQ}/2) + 0.300$	Note 1	V	2, 3
	Single-ended HIGH level for CK <sub>t</sub> , CK <sub>c</sub>	$(V_{DD2}/2) + 0.220$	Note 1	$(V_{DD2}/2) + 0.300$	Note 1	V	2, 3
$V_{SEL(AC)}$	Single-ended LOW level for strobes	Note 1	$(V_{DDQ}/2) - 0.220$	Note 1	$(V_{DDQ}/2) + 0.300$	V	2, 3
	Single-ended LOW level for CK <sub>t</sub> , CK <sub>c</sub>	Note 1	$(V_{DD2}/2) - 0.220$	Note 1	$(V_{DD2}/2) + 0.300$	V	2, 3

Notes: 1. These values are not defined; however, the single-ended signals CK<sub>t</sub>, CK<sub>c</sub>, DQS0<sub>t</sub>, DQS0<sub>c</sub>, DQS1<sub>t</sub>, DQS1<sub>c</sub>, DQS2<sub>t</sub>, DQS2<sub>c</sub>, DQS3<sub>t</sub>, DQS3<sub>c</sub> must be within the respective limits ( $V_{IH(DC)max}/V_{IL(DC)min}$ ) for single-ended signals, and must comply with the



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM AC and DC Logic Input Measurement Levels for Differential Signals

specified limitations for overshoot and undershoot (see Overshoot and Undershoot Definition).

- For CK\_t and CK\_c, use  $V_{SEH}/V_{SEL(AC)}$  of CA; for strobes (DQS[3:0]\_t and DQS[3:0]\_c), use  $V_{IH}/V_{IL(AC)}$  of DQ.
- $V_{IH(AC)}$  and  $V_{IL(AC)}$  for DQ are based on  $V_{REFDQ}$ ;  $V_{SEH(AC)}$  and  $V_{SEL(AC)}$  for CA are based on  $V_{REFCA}$ . If a reduced AC HIGH or AC LOW is used for a signal group, the reduced level applies.

### Differential Input Crosspoint Voltage

To ensure tight setup and hold times as well as output skew parameters with respect to clock and strobe, each crosspoint voltage of differential input signals (CK\_t, CK\_c, DQS\_t, and DQS\_c) must meet the specifications listed in the Single-Ended Levels for CK\_t, CK\_c, DQS\_t, DQS\_c table. The differential input crosspoint voltage ( $V_{IX}$ ) is measured from the actual crosspoint of the true signal and its complement to the midlevel between  $V_{DD}$  and  $V_{SS}$ .

Figure 74:  $V_{IX}$  Definition

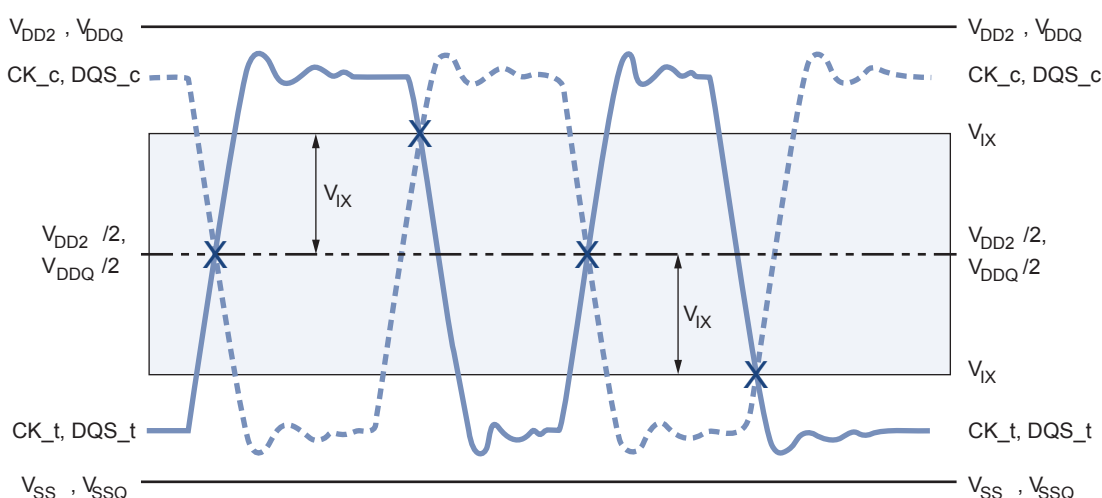


Table 77: Crosspoint Voltage for Differential Input Signals (CK\_t, CK\_c, DQS\_t, DQS\_c)

Symbol	Parameter	LPDDR2-1066 to LPDDR2-200		Unit	Notes
		Min	Max		
$V_{IXCA(AC)}$	Differential input crosspoint voltage relative to $V_{DD2}/2$ for CK_t and CK_c	-120	120	mV	1, 2
$V_{IXDQ(AC)}$	Differential input crosspoint voltage relative to $V_{DDQ}/2$ for DQS_t and DQS_c	-120	120	mV	1, 2

- Notes:
- The typical value of  $V_{IX(AC)}$  is expected to be about  $0.5 \times V_{DD}$  of the transmitting device, and it is expected to track variations in  $V_{DD}$ .  $V_{IX(AC)}$  indicates the voltage at which differential input signals must cross.
  - For CK\_t and CK\_c,  $V_{REF} = V_{REFCA(DC)}$ . For DQS\_t and DQS\_c,  $V_{REF} = V_{REFDQ(DC)}$ .



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Output Characteristics and Operating Conditions

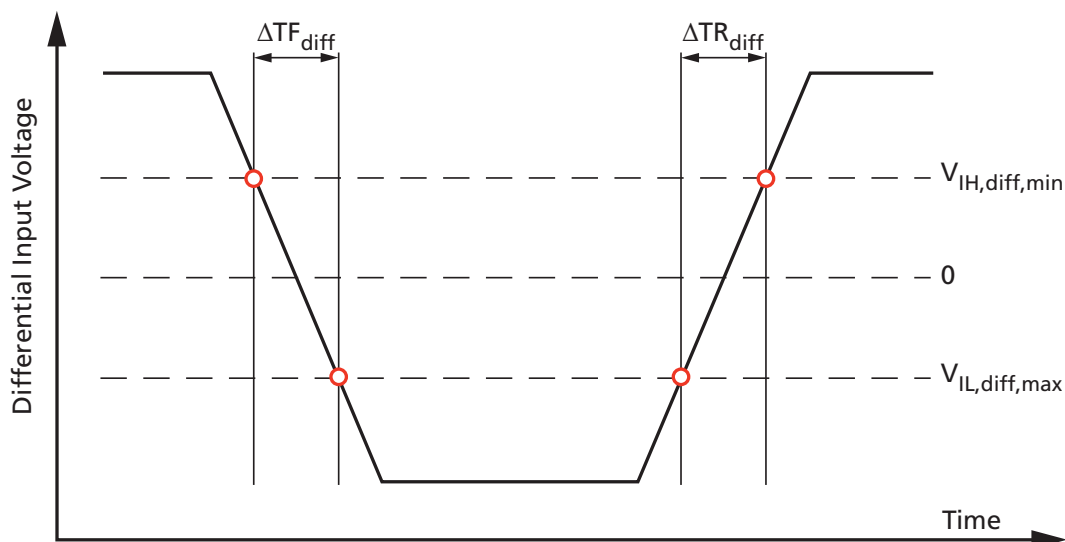
### Input Slew Rate

**Table 78: Differential Input Slew Rate Definition**

Description	Measured <sup>1</sup>		Defined by
	From	To	
Differential input slew rate for rising edge (CK_t/CK_c and DQS_t/DQS_c)	$V_{IL,diff,max}$	$V_{IH,diff,min}$	$[V_{IH,diff,min} - V_{IL,diff,max}] / \Delta TR_{diff}$
Differential input slew rate for falling edge (CK_t/CK_c and DQS_t/DQS_c)	$V_{IH,diff,min}$	$V_{IL,diff,max}$	$[V_{IH,diff,min} - V_{IL,diff,max}] / \Delta TF_{diff}$

Note: 1. The differential signals (CK\_t/CK\_c and DQS\_t/DQS\_c) must be linear between these thresholds.

**Figure 75: Differential Input Slew Rate Definition for CK\_t, CK\_c, DQS\_t, and DQS\_c**



### Output Characteristics and Operating Conditions

**Table 79: Single-Ended AC and DC Output Levels**

Symbol	Parameter	Value	Unit	Notes
$V_{OH(AC)}$	AC output HIGH measurement level (for output slew rate)	$V_{REF} + 0.12$	V	
$V_{OL(AC)}$	AC output LOW measurement level (for output slew rate)	$V_{REF} - 0.12$	V	
$V_{OH(DC)}$	DC output HIGH measurement level (for I-V curve linearity)	$0.9 \times V_{DDQ}$	V	1
$V_{OL(DC)}$	DC output LOW measurement level (for I-V curve linearity)	$0.1 \times V_{DDQ}$	V	2
$I_{OZ}$	Output leakage current (DQ, DM, DQS_t, DQS_c); DQ, DQS_t, DQS_c are disabled; $0V \leq V_{OUT} \leq V_{DDQ}$	MIN	-5	$\mu A$
		MAX	+5	$\mu A$





## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM

### Output Characteristics and Operating Conditions

**Table 79: Single-Ended AC and DC Output Levels (Continued)**

Symbol	Parameter		Value	Unit	Notes
MMpupd	Delta output impedance between pull-up and pull-down for DQ/DM	MIN	-15	%	
		MAX	+15	%	

- Notes: 1.  $I_{OH} = -0.1\text{mA}$ .  
2.  $I_{OL} = 0.1\text{mA}$ .

**Table 80: Differential AC and DC Output Levels**

Symbol	Parameter	Value	Unit
$V_{OH\text{diff}(AC)}$	AC differential output HIGH measurement level (for output SR)	$+ 0.2 \times V_{DDQ}$	V
$V_{OL\text{diff}(AC)}$	AC differential output LOW measurement level (for output SR)	$- 0.2 \times V_{DDQ}$	V

### Single-Ended Output Slew Rate

With the reference load for timing measurements, the output slew rate for falling and rising edges is defined and measured between  $V_{OL(AC)}$  and  $V_{OH(AC)}$  for single-ended signals.

**Table 81: Single-Ended Output Slew Rate Definition**

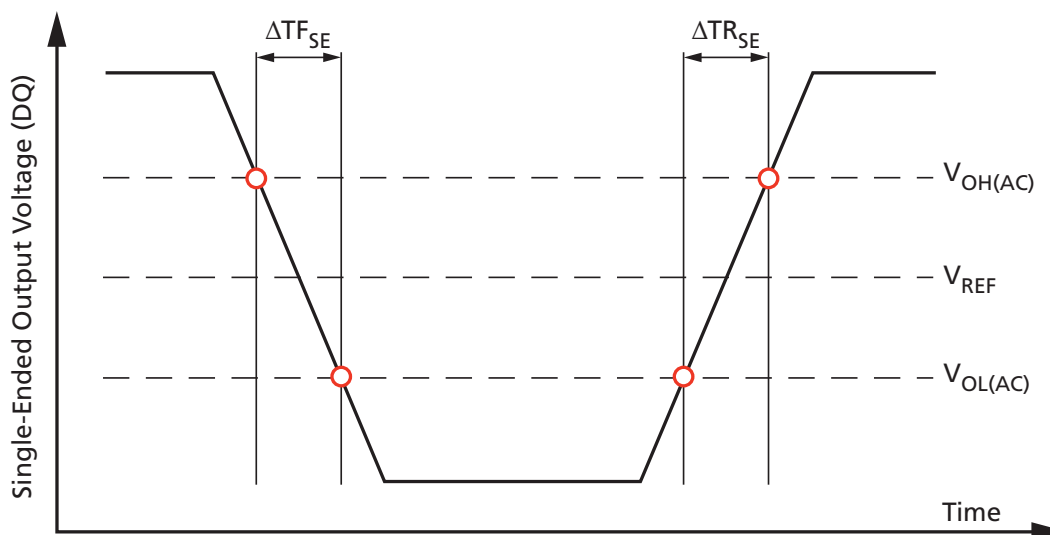
Description	Measured		Defined by
	From	To	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}] / \Delta TR_{SE}$
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}] / \Delta TF_{SE}$

- Note: 1. Output slew rate is verified by design and characterization and may not be subject to production testing.



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Output Characteristics and Operating Conditions

**Figure 76: Single-Ended Output Slew Rate Definition**



**Table 82: Single-Ended Output Slew Rate**

Notes 1–5 apply to all parameters conditions

Parameter	Symbol	Value		Unit
		Min	Max	
Single-ended output slew rate (output impedance = 40Ω ±30%)	SRQ <sub>SE</sub>	1.5	3.5	V/ns
Single-ended output slew rate (output impedance = 60Ω ±30%)	SRQ <sub>SE</sub>	1.0	2.5	V/ns
Output slew-rate-matching ratio (pull-up to pull-down)		0.7	1.4	–

- Notes:
- Definitions: SR = slew rate; Q = output (similar to DQ = data-in, data-out); SE = single-ended signals.
  - Measured with output reference load.
  - The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage over the entire temperature and voltage range. For a given output, the ratio represents the maximum difference between pull-up and pull-down drivers due to process variation.
  - The output slew rate for falling and rising edges is defined and measured between V<sub>OL(AC)</sub> and V<sub>OH(AC)</sub>.
  - Slew rates are measured under typical simultaneous switching output (SSO) conditions, with one-half of DQ signals per data byte driving HIGH and one-half of DQ signals per data byte driving LOW.

### Differential Output Slew Rate

With the reference load for timing measurements, the output slew rate for falling and rising edges is defined and measured between V<sub>OL,diff(AC)</sub> and V<sub>OH,diff(AC)</sub> for differential signals.

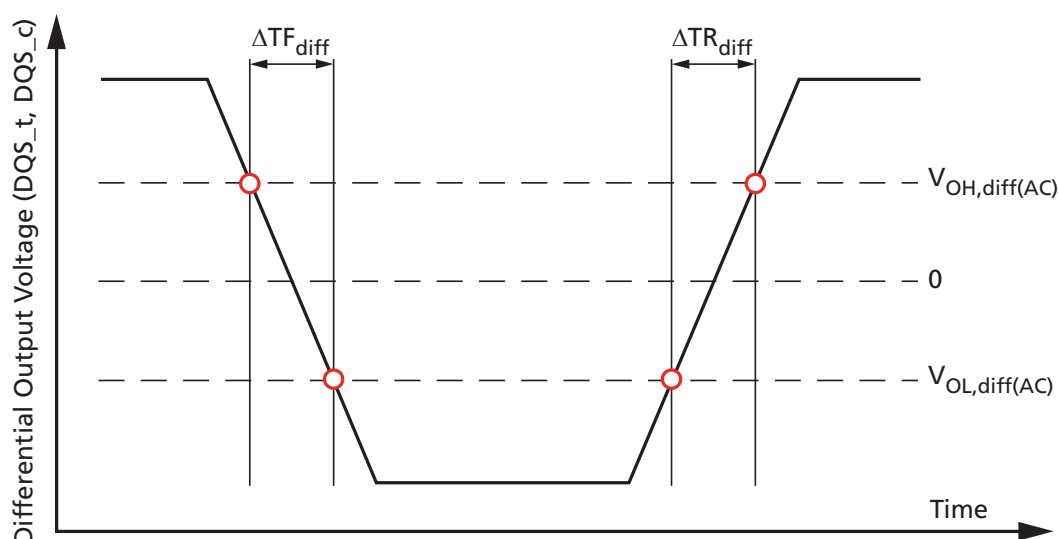


## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Output Characteristics and Operating Conditions

**Table 83: Differential Output Slew Rate Definition**

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	$V_{OL,diff(AC)}$	$V_{OH,diff(AC)}$	$[V_{OH,diff(AC)} - V_{OL,diff(AC)}] / \Delta TR_{diff}$
Differential output slew rate for falling edge	$V_{OH,diff(AC)}$	$V_{OL,diff(AC)}$	$[V_{OH,diff(AC)} - V_{OL,diff(AC)}] / \Delta TF_{diff}$

Note: 1. Output slew rate is verified by design and characterization and may not be subject to production testing.

**Figure 77: Differential Output Slew Rate Definition**

**Table 84: Differential Output Slew Rate**

Parameter	Symbol	Value		Unit
		Min	Max	
Differential output slew rate (output impedance = $40\Omega \pm 30\%$ )	$SRQ_{diff}$	3.0	7.0	V/ns
Differential output slew rate (output impedance = $60\Omega \pm 30\%$ )	$SRQ_{diff}$	2.0	5.0	V/ns

- Notes:
1. Definitions: SR = slew rate; Q = output (similar to DQ = data-in, data-out); SE = single-ended signals.
  2. Measured with output reference load.
  3. The output slew rate for falling and rising edges is defined and measured between  $V_{OL(AC)}$  and  $V_{OH(AC)}$ .
  4. Slew rates are measured under typical simultaneous switching output (SSO) conditions, with one-half of DQ signals per data byte driving HIGH and one-half of DQ signals per data byte driving LOW.



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Output Characteristics and Operating Conditions

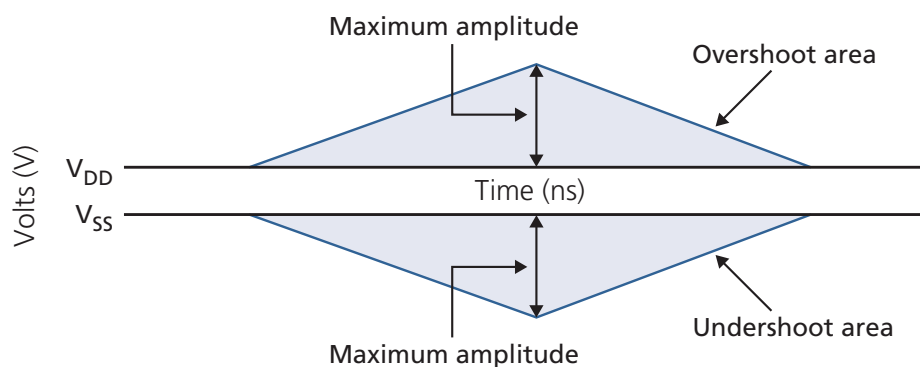
**Table 85: AC Overshoot/Undershoot Specification**

Applies for CA[9:0], CS\_n, CKE, CK\_t, CK\_c, DQ, DQS\_t, DQS\_c, DM

Parameter	1066	933	800	667	533	466	400	333	266	200	Unit
Maximum peak amplitude provided for overshoot area	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	V
Maximum peak amplitude provided for undershoot area	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	V
Maximum area above $V_{DD}^1$	0.15	0.17	0.20	0.24	0.30	0.35	0.40	0.48	0.60	0.80	V-ns
Maximum area below $V_{SS}^2$	0.15	0.17	0.20	0.24	0.30	0.35	0.40	0.48	0.60	0.80	V-ns

- Notes: 1.  $V_{DD}$  stands for  $V_{DD2}$  for CA[9:0], CK\_t, CK\_c, CS\_n, and CKE.  $V_{DD}$  stands for  $V_{DDQ}$  for DQ, DM, DQS\_t, and DQS\_c.  
2.  $V_{SS}$  is for CA[9:0], CK\_t, CK\_c, CS\_n, and CKE.  $V_{SS}$  stands for  $V_{SSQ}$  for DQ, DM, DQS\_t, and DQS\_c.

**Figure 78: Overshoot and Undershoot Definition**



- Notes: 1.  $V_{DD}$  stands for  $V_{DD2}$  for CA[9:0], CK\_t, CK\_c, CS\_n, and CKE.  $V_{DD}$  stands for  $V_{DDQ}$  for DQ, DM, DQS\_t, and DQS\_c.  
2.  $V_{SS}$  is for CA[9:0], CK\_t, CK\_c, CS\_n, and CKE.  $V_{SS}$  stands for  $V_{SSQ}$  for DQ, DM, DQS\_t, and DQS\_c.

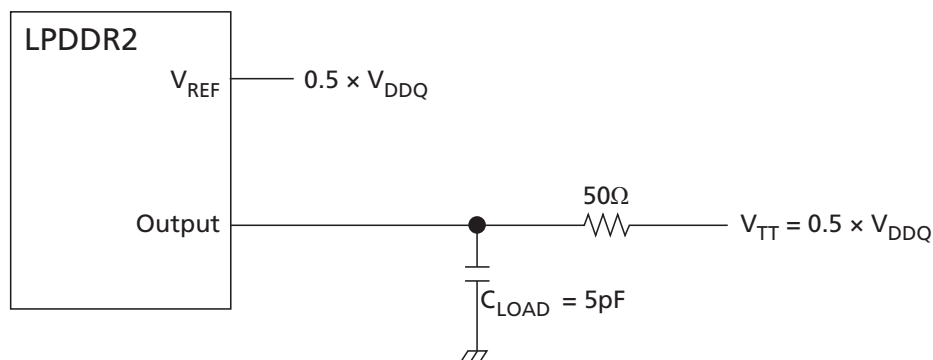
### HSUL\_12 Driver Output Timing Reference Load

The timing reference loads are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally with one or more coaxial transmission lines terminated at the tester electronics.



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Output Driver Impedance

Figure 79: HSUL\_12 Driver Output Reference Load for Timing and Slew Rate



Note: 1. All output timing parameter values ( $t_{DQSCK}$ ,  $t_{DQSQ}$ ,  $t_{QHS}$ ,  $t_{HZ}$ ,  $t_{RPRE}$  etc.) are reported with respect to this reference load. This reference load is also used to report slew rate.

### Output Driver Impedance

Output driver impedance is selected by a mode register during initialization. To achieve tighter tolerances, ZQ calibration is required. Output specifications refer to the default output drive unless specifically stated otherwise. The output driver impedance  $R_{ON}$  is defined by the value of the external reference resistor  $R_{ZQ}$  as follows:

$$R_{ONPU} = \frac{V_{DDQ} - V_{OUT}}{ABS(I_{OUT})}$$

When  $R_{ONPD}$  is turned off.

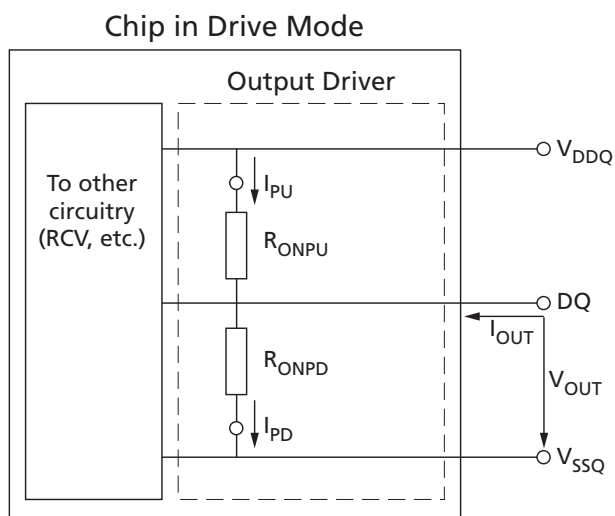
$$R_{ONPD} = \frac{V_{OUT}}{ABS(I_{OUT})}$$

When  $R_{ONPU}$  is turned off.



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Output Driver Impedance

Figure 80: Output Driver



### Output Driver Impedance Characteristics with ZQ Calibration

Output driver impedance is defined by the value of the external reference resistor  $R_{ZQ}$ . Typical  $R_{ZQ}$  is 240 ohms.

Table 86: Output Driver DC Electrical Characteristics with ZQ Calibration

Notes 1–4 apply to all parameters and conditions

$R_{ONnom}$	Resistor	$V_{OUT}$	Min	Typ	Max	Unit	Notes
34.3 $\Omega$	$R_{ON34PD}$	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/7$	
	$R_{ON34PU}$	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/7$	
40.0 $\Omega$	$R_{ON40PD}$	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/6$	
	$R_{ON40PU}$	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/6$	
48.0 $\Omega$	$R_{ON48PD}$	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/5$	
	$R_{ON48PU}$	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/5$	
60.0 $\Omega$	$R_{ON60PD}$	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/4$	
	$R_{ON60PU}$	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/4$	
80.0 $\Omega$	$R_{ON80PD}$	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/3$	
	$R_{ON80PU}$	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/3$	
120.0 $\Omega$ (optional)	$R_{ON120PD}$	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/2$	
	$R_{ON120PU}$	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/2$	
Mismatch between pull-up and pull-down	$MM_{PUPD}$		-15.00		+15.00	%	5

- Notes:
1. Applies across entire operating temperature range after calibration.
  2.  $R_{ZQ} = 240\Omega$ .
  3. The tolerance limits are specified after calibration, with fixed voltage and temperature. For behavior of the tolerance limits if temperature or voltage changes after calibration, see Output Driver Temperature and Voltage Sensitivity.



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Output Driver Impedance

- Pull-down and pull-up output driver impedances should be calibrated at  $0.5 \times V_{DDQ}$ .
- Measurement definition for mismatch between pull-up and pull-down,  $MM_{PUPD}$ : Measure  $R_{ONPU}$  and  $R_{ONPD}$ , both at  $0.5 \times V_{DDQ}$ :

$$MM_{PUPD} = \frac{R_{ONPU} - R_{ONPD}}{R_{ON,nom}} \times 100$$

For example, with  $MM_{PUPD}(\text{MAX}) = 15\%$  and  $R_{ONPD} = 0.85$ ,  $R_{ONPU}$  must be less than 1.0.

### Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen.

**Table 87: Output Driver Sensitivity Definition**

Resistor	$V_{OUT}$	Min	Max	Unit
$R_{ONPD}$	$0.5 \times V_{DDQ}$	$85 - (dR_{ONdT} \cdot  \Delta T ) - (dR_{ONdV} \cdot  \Delta V )$	$115 + (dR_{ONdT} \cdot  \Delta T ) + (dR_{ONdV} \cdot  \Delta V )$	%
$R_{ONPU}$				

- Notes:
- $\Delta T = T - T$  (at calibration).  $\Delta V = V - V$  (at calibration).
  - $dR_{ONdT}$  and  $dR_{ONdV}$  are not subject to production testing; they are verified by design and characterization.

**Table 88: Output Driver Temperature and Voltage Sensitivity**

Symbol	Parameter	Min	Max	Unit
$R_{ONdT}$	$R_{ON}$ temperature sensitivity	0.00	0.75	%/°C
$R_{ONdV}$	$R_{ON}$ voltage sensitivity	0.00	0.20	%/mV

### Output Impedance Characteristics Without ZQ Calibration

Output driver impedance is defined by design and characterization as the default setting.

**Table 89: Output Driver DC Electrical Characteristics Without ZQ Calibration**

$R_{ON,nom}$	Resistor	$V_{OUT}$	Min	Typ	Max	Unit
34.3Ω	$R_{ON34PD}$	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/7$
	$R_{ON34PU}$	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/7$
40.0Ω	$R_{ON40PD}$	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/6$
	$R_{ON40PU}$	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/6$
48.0Ω	$R_{ON48PD}$	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/5$
	$R_{ON48PU}$	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/5$
60.0Ω	$R_{ON60PD}$	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/4$
	$R_{ON60PU}$	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/4$
80.0Ω	$R_{ON80PD}$	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/3$
	$R_{ON80PU}$	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/3$



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Output Driver Impedance

**Table 89: Output Driver DC Electrical Characteristics Without ZQ Calibration (Continued)**

$R_{ON_{nom}}$	Resistor	$V_{OUT}$	Min	Typ	Max	Unit
120.0 $\Omega$ (optional)	$R_{ON120PD}$	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/2$
	$R_{ON120PU}$	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/2$

- Notes: 1. Applies across entire operating temperature range without calibration.  
2.  $R_{ZQ} = 240\Omega$ .

**Table 90: I-V Curves**

Voltage (V)	$R_{ON} = 240\Omega (R_{ZQ})$							
	Pull-Down				Pull-Up			
	Current (mA) / $R_{ON}$ (ohms)				Current (mA) / $R_{ON}$ (ohms)			
	Default Value after ZQRESET		With Calibration		Default Value after ZQRESET		With Calibration	
	Min (mA)	Max (mA)	Min (mA)	Max (mA)	Min (mA)	Max (mA)	Min (mA)	Max (mA)
0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
0.05	0.19	0.32	0.21	0.26	-0.19	-0.32	-0.21	-0.26
0.10	0.38	0.64	0.40	0.53	-0.38	-0.64	-0.40	-0.53
0.15	0.56	0.94	0.60	0.78	-0.56	-0.94	-0.60	-0.78
0.20	0.74	1.26	0.79	1.04	-0.74	-1.26	-0.79	-1.04
0.25	0.92	1.57	0.98	1.29	-0.92	-1.57	-0.98	-1.29
0.30	1.08	1.86	1.17	1.53	-1.08	-1.86	-1.17	-1.53
0.35	1.25	2.17	1.35	1.79	-1.25	-2.17	-1.35	-1.79
0.40	1.40	2.46	1.52	2.03	-1.40	-2.46	-1.52	-2.03
0.45	1.54	2.74	1.69	2.26	-1.54	-2.74	-1.69	-2.26
0.50	1.68	3.02	1.86	2.49	-1.68	-3.02	-1.86	-2.49
0.55	1.81	3.30	2.02	2.72	-1.81	-3.30	-2.02	-2.72
0.60	1.92	3.57	2.17	2.94	-1.92	-3.57	-2.17	-2.94
0.65	2.02	3.83	2.32	3.15	-2.02	-3.83	-2.32	-3.15
0.70	2.11	4.08	2.46	3.36	-2.11	-4.08	-2.46	-3.36
0.75	2.19	4.31	2.58	3.55	-2.19	-4.31	-2.58	-3.55
0.80	2.25	4.54	2.70	3.74	-2.25	-4.54	-2.70	-3.74
0.85	2.30	4.74	2.81	3.91	-2.30	-4.74	-2.81	-3.91
0.90	2.34	4.92	2.89	4.05	-2.34	-4.92	-2.89	-4.05
0.95	2.37	5.08	2.97	4.23	-2.37	-5.08	-2.97	-4.23
1.00	2.41	5.20	3.04	4.33	-2.41	-5.20	-3.04	-4.33
1.05	2.43	5.31	3.09	4.44	-2.43	-5.31	-3.09	-4.44
1.10	2.46	5.41	3.14	4.52	-2.46	-5.41	-3.14	-4.52
1.15	2.48	5.48	3.19	4.59	-2.48	-5.48	-3.19	-4.59
1.20	2.50	5.55	3.23	4.65	-2.50	-5.55	-3.23	-4.65





# 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Output Driver Impedance

Figure 81: Output Impedance = 240 Ohms, I-V Curves After ZQRESET

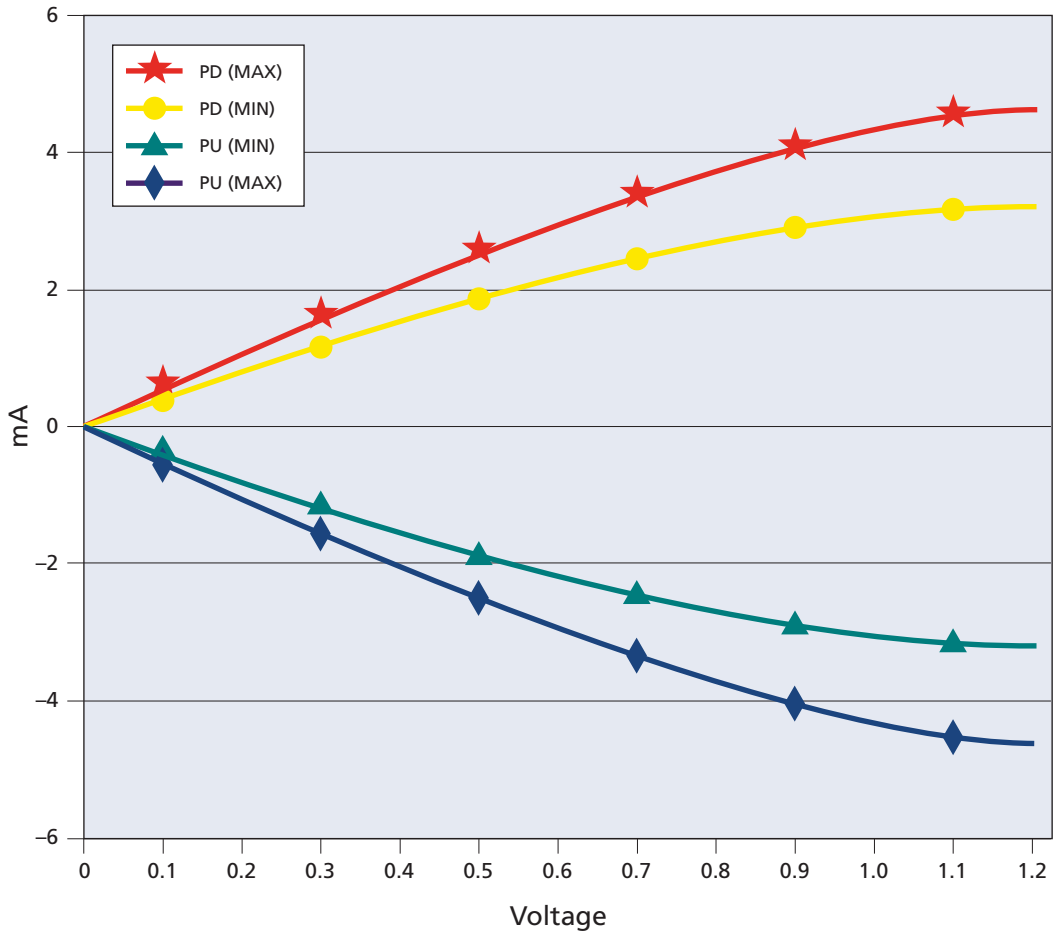
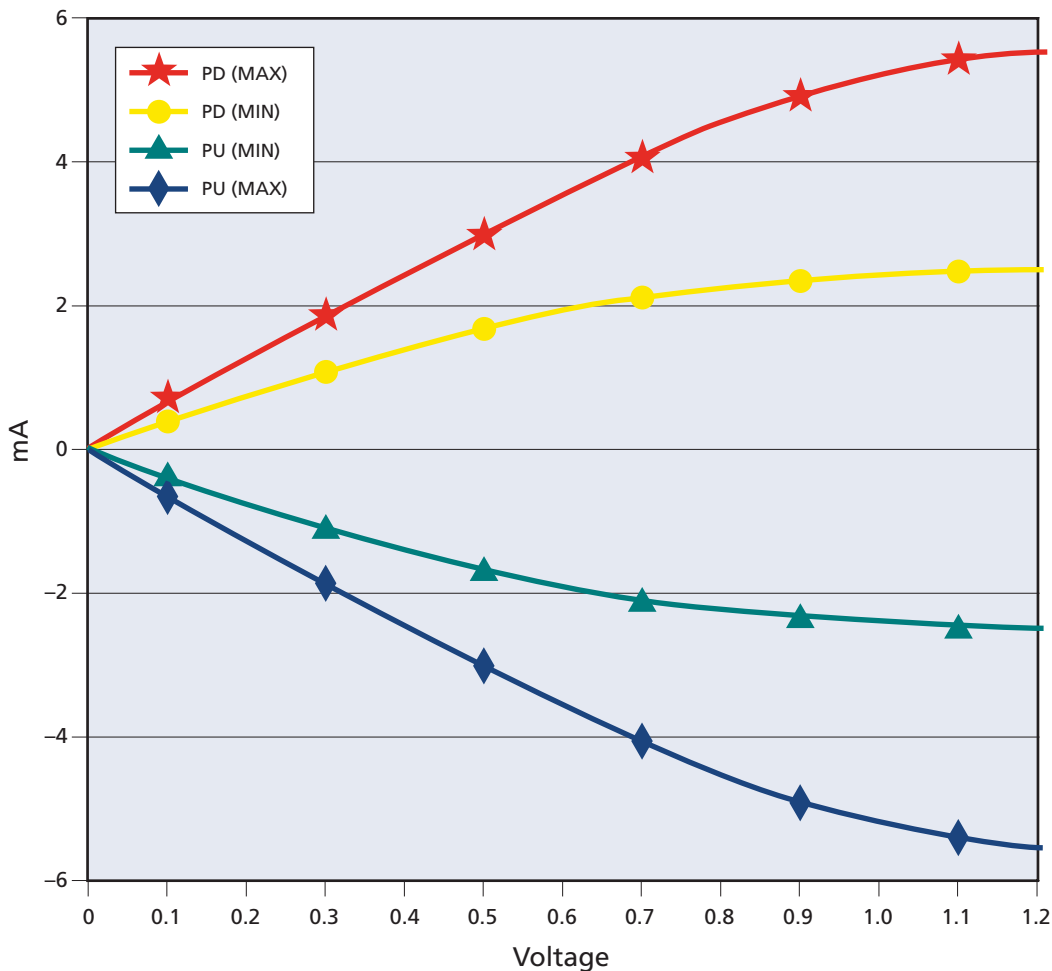




Figure 82: Output Impedance = 240 Ohms, I-V Curves After Calibration



### Clock Specification

The specified clock jitter is a random jitter with Gaussian distribution. Input clocks violating minimum or maximum values may result in device malfunction.



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Clock Specification

**Table 91: Definitions and Calculations**

Symbol	Description	Calculation	Notes
$t_{CK(avg)}$ and $n_{CK}$	<p>The average clock period across any consecutive 200-cycle window. Each clock period is calculated from rising clock edge to rising clock edge.</p> <p>Unit <math>t_{CK(avg)}</math> represents the actual clock average <math>t_{CK(avg)}</math> of the input clock under operation. Unit <math>n_{CK}</math> represents one clock cycle of the input clock, counting from actual clock edge to actual clock edge.</p> <p><math>t_{CK(avg)}</math> can change no more than <math>\pm 1\%</math> within a 100-clock-cycle window, provided that all jitter and timing specifications are met.</p>	$t_{CK(avg)} = \left( \sum_{j=1}^N t_{CK_j} \right) / N$ <p>Where <math>N = 200</math></p>	
$t_{CK(abs)}$	The absolute clock period, as measured from one rising clock edge to the next consecutive rising clock edge.		1
$t_{CH(avg)}$	The average HIGH pulse width, as calculated across any 200 consecutive HIGH pulses.	$t_{CH(avg)} = \left( \sum_{j=1}^N t_{CH_j} \right) / (N \times t_{CK(avg)})$ <p>Where <math>N = 200</math></p>	
$t_{CL(avg)}$	The average LOW pulse width, as calculated across any 200 consecutive LOW pulses.	$t_{CL(avg)} = \left( \sum_{j=1}^N t_{CL_j} \right) / (N \times t_{CK(avg)})$ <p>Where <math>N = 200</math></p>	
$t_{JIT(per)}$	The single-period jitter defined as the largest deviation of any signal $t_{CK}$ from $t_{CK(avg)}$ .	$t_{JIT(per)} = \min/\max \text{ of } \left( t_{CK_i} - t_{CK(avg)} \right)$ <p>Where <math>i = 1</math> to 200</p>	1
$t_{JIT(per),act}$	The actual clock jitter for a given system.		
$t_{JIT(per),allowed}$	The specified clock period jitter allowance.		
$t_{JIT(cc)}$	The absolute difference in clock periods between two consecutive clock cycles. $t_{JIT(cc)}$ defines the cycle-to-cycle jitter.	$t_{JIT(cc)} = \max \text{ of } \left( t_{CK_{i+1}} - t_{CK_i} \right)$	1
$t_{ERR(nper)}$	The cumulative error across $n$ multiple consecutive cycles from $t_{CK(avg)}$ .	$t_{ERR(nper)} = \left( \sum_{j=i}^{i+n-1} t_{CK_j} \right) - (n \times t_{CK(avg)})$	1
$t_{ERR(nper),act}$	The actual cumulative error over $n$ cycles for a given system.		
$t_{ERR(nper),allowed}$	The specified cumulative error allowance over $n$ cycles.		
$t_{ERR(nper),min}$	The minimum $t_{ERR(nper)}$ .	$t_{ERR(nper),min} = (1 + 0.68LN(n)) \times t_{JIT(per),min}$	2
$t_{ERR(nper),max}$	The maximum $t_{ERR(nper)}$ .	$t_{ERR(nper),max} = (1 + 0.68LN(n)) \times t_{JIT(per),max}$	2

**Table 91: Definitions and Calculations (Continued)**

Symbol	Description	Calculation	Notes
$t_{\text{JIT}}(\text{duty})$	Defined with absolute and average specifications for $t_{\text{CH}}$ and $t_{\text{CL}}$ , respectively.	$t_{\text{JIT}}(\text{duty}),\text{min} = \text{MIN}((t_{\text{CH}}(\text{abs}),\text{min} - t_{\text{CH}}(\text{avg}),\text{min}), (t_{\text{CL}}(\text{abs}),\text{min} - t_{\text{CL}}(\text{avg}),\text{min})) \times t_{\text{CK}}(\text{avg})$ $t_{\text{JIT}}(\text{duty}),\text{max} = \text{MAX}((t_{\text{CH}}(\text{abs}),\text{max} - t_{\text{CH}}(\text{avg}),\text{max}), (t_{\text{CL}}(\text{abs}),\text{max} - t_{\text{CL}}(\text{avg}),\text{max})) \times t_{\text{CK}}(\text{avg})$	

- Notes: 1. Not subject to production testing.  
2. Using these equations,  $t_{\text{ERR}}(\text{nper})$  tables can be generated for each  $t_{\text{JIT}}(\text{per}),\text{act}$  value.

### $t_{\text{CK}}(\text{abs})$ , $t_{\text{CH}}(\text{abs})$ , and $t_{\text{CL}}(\text{abs})$

These parameters are specified with their average values; however, the relationship between the average timing and the absolute instantaneous timing (defined in the following table) is applicable at all times.

**Table 92:  $t_{\text{CK}}(\text{abs})$ ,  $t_{\text{CH}}(\text{abs})$ , and  $t_{\text{CL}}(\text{abs})$  Definitions**

Parameter	Symbol	Minimum	Unit
Absolute clock period	$t_{\text{CK}}(\text{abs})$	$t_{\text{CK}}(\text{avg}),\text{min} + t_{\text{JIT}}(\text{per}),\text{min}$	ps <sup>1</sup>
Absolute clock HIGH pulse width	$t_{\text{CH}}(\text{abs})$	$t_{\text{CH}}(\text{avg}),\text{min} + t_{\text{JIT}}(\text{duty}),\text{min}^2/t_{\text{CK}}(\text{avg}),\text{min}$	$t_{\text{CK}}(\text{avg})$
Absolute clock LOW pulse width	$t_{\text{CL}}(\text{abs})$	$t_{\text{CL}}(\text{avg}),\text{min} + t_{\text{JIT}}(\text{duty}),\text{min}^2/t_{\text{CK}}(\text{avg}),\text{min}$	$t_{\text{CK}}(\text{avg})$

- Notes: 1.  $t_{\text{CK}}(\text{avg}),\text{min}$  is expressed in ps for this table.  
2.  $t_{\text{JIT}}(\text{duty}),\text{min}$  is a negative value.

## Clock Period Jitter

The LPDDR2 device can tolerate some clock period jitter without core timing parameter derating. This section describes device timing requirements with clock period jitter ( $t_{\text{JIT}}(\text{per})$ ) in excess of the values found in the AC Timing section. Calculating cycle time derating and clock cycle derating are also described.

### Clock Period Jitter Effects on Core Timing Parameters

Core timing parameters ( $t_{\text{RCD}}$ ,  $t_{\text{RP}}$ ,  $t_{\text{RTP}}$ ,  $t_{\text{WR}}$ ,  $t_{\text{WRA}}$ ,  $t_{\text{WTR}}$ ,  $t_{\text{RC}}$ ,  $t_{\text{RAS}}$ ,  $t_{\text{RRD}}$ ,  $t_{\text{FAW}}$ ) extend across multiple clock cycles. Clock period jitter impacts these parameters when measured in numbers of clock cycles. Within the specification limits, the device is characterized and verified to support  $t_{\text{nPARAM}} = \text{RU}[t_{\text{PARAM}}/t_{\text{CK}}(\text{avg})]$ . During device operation where clock jitter is outside specification limits, the number of clocks or  $t_{\text{CK}}(\text{avg})$ , may need to be increased based on the values for each core timing parameter.



## Cycle Time Derating for Core Timing Parameters

For a given number of clocks ( $t_{nPARAM}$ ), when  $t_{CK(avg)}$  and  $t_{ERR}(t_{nPARAM},act)$  exceed  $t_{ERR}(t_{nPARAM},allowed)$ , cycle time derating may be required for core timing parameters.

$$\text{CycleTimeDerating} = \max\left\{\left\{\frac{t_{PARAM} + t_{ERR}(t_{nPARAM},act) - t_{ERR}(t_{nPARAM},allowed)}{t_{nPARAM}} - t_{CK(avg)}\right\}, 0\right\}$$

Cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time deratings determined for each individual core timing parameter.

## Clock Cycle Derating for Core Timing Parameters

For each core timing parameter and a given number of clocks ( $t_{nPARAM}$ ), clock cycle derating should be specified with  $t_{JIT(per)}$ .

For a given number of clocks ( $t_{nPARAM}$ ), when  $t_{CK(avg)}$  plus  $t_{ERR}(t_{nPARAM},act)$  exceed the supported cumulative  $t_{ERR}(t_{nPARAM},allowed)$ , derating is required. If the equation below results in a positive value for a core timing parameter ( $t_{CORE}$ ), the required clock cycle derating will be that positive value (in clocks).

$$\text{ClockCycleDerating} = RU \left\{ \frac{t_{PARAM} + t_{ERR}(t_{nPARAM},act) - t_{ERR}(t_{nPARAM},allowed)}{t_{CK(avg)}} \right\} - t_{nPARAM}$$

Cycle-time derating analysis should be conducted for each core timing parameter.

## Clock Jitter Effects on Command/Address Timing Parameters

Command/address timing parameters ( $t_{IS}$ ,  $t_{IH}$ ,  $t_{ISCKE}$ ,  $t_{IHCKE}$ ,  $t_{ISb}$ ,  $t_{IHb}$ ,  $t_{ISCKEb}$ ,  $t_{IHCKEb}$ ) are measured from a command/address signal (CKE, CS\_n, or CA[9:0]) transition edge to its respective clock signal (CK\_t/CK\_c) crossing. The specification values are not affected by the  $t_{JIT(per)}$  applied, because the setup and hold times are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

## Clock Jitter Effects on READ Timing Parameters

### $t_{RPRE}$

When the device is operated with input clock jitter,  $t_{RPRE}$  must be derated by the  $t_{JIT(per),act,max}$  of the input clock that exceeds  $t_{JIT(per),allowed,max}$ . Output deratings are relative to the input clock:

$$t_{RPRE}(min,derated) = 0.9 - \left( \frac{t_{JIT(per),act,max} - t_{JIT(per),allowed,max}}{t_{CK(avg)}} \right)$$

For example, if the measured jitter into a LPDDR2-800 device has  $t_{CK(avg)} = 2500ps$ ,  $t_{JIT(per),act,min} = -172ps$ , and  $t_{JIT(per),act,max} = +193ps$ , then  $t_{RPRE,min,derated} = 0.9 - (t_{JIT(per),act,max} - t_{JIT(per),allowed,max})/t_{CK(avg)} = 0.9 - (193 - 100)/2500 = 0.8628 t_{CK(avg)}$ .

$t_{LZ(DQ)}$ ,  $t_{HZ(DQ)}$ ,  $t_{DQSCK}$ ,  $t_{LZ(DQS)}$ ,  $t_{HZ(DQS)}$



These parameters are measured from a specific clock edge to a data signal transition (DM $n$  or DQ $m$ , where:  $n = 0, 1, 2,$  or  $3$ ; and  $m = \text{DQ}[31:0]$ ), and specified timings must be met with respect to that clock edge. Therefore, they are not affected by  $t_{\text{JIT}}(\text{per})$ .

#### $t_{\text{QSH}}, t_{\text{QSL}}$

These parameters are affected by duty cycle jitter, represented by  $t_{\text{CH}}(\text{abs})\text{min}$  and  $t_{\text{CL}}(\text{abs})\text{min}$ . These parameters determine the absolute data valid window at the device pin. The absolute minimum data valid window at the device pin =  $\min [ (t_{\text{QSH}}(\text{abs})\text{min} \times t_{\text{CK}}(\text{avg})\text{min} - t_{\text{DQSQ}}\text{max} - t_{\text{QHS}}\text{max}), (t_{\text{QSL}}(\text{abs})\text{min} \times t_{\text{CK}}(\text{avg})\text{min} - t_{\text{DQSQ}}\text{max} - t_{\text{QHS}}\text{max}) ]$ . This minimum data valid window must be met at the target frequency regardless of clock jitter.

#### $t_{\text{RPST}}$

$t_{\text{RPST}}$  is affected by duty cycle jitter, represented by  $t_{\text{CL}}(\text{abs})$ . Therefore,  $t_{\text{RPST}}(\text{abs})\text{min}$  can be specified by  $t_{\text{CL}}(\text{abs})\text{min}$ .  $t_{\text{RPST}}(\text{abs})\text{min} = t_{\text{CL}}(\text{abs})\text{min} - 0.05 = t_{\text{QSL}}(\text{abs})\text{min}$ .

## Clock Jitter Effects on WRITE Timing Parameters

#### $t_{\text{DS}}, t_{\text{DH}}$

These parameters are measured from a data signal (DM $n$  or DQ $m$ , where  $n = 0, 1, 2, 3$ ; and  $m = \text{DQ}[31:0]$ ) transition edge to its respective data strobe signal (DQS $n_t$ , DQS $n_c$ :  $n = 0, 1, 2, 3$ ) crossing. The specification values are not affected by the amount of  $t_{\text{JIT}}(\text{per})$  applied, because the setup and hold times are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

#### $t_{\text{DSS}}, t_{\text{DSH}}$

These parameters are measured from a data strobe signal crossing (DQS $x_t$ , DQS $x_c$ ) to its clock signal crossing (CK $_t$ /CK $_c$ ). The specification values are not affected by the amount of  $t_{\text{JIT}}(\text{per})$  applied, because the setup and hold times are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

#### $t_{\text{DQSS}}$

$t_{\text{DQSS}}$  is measured from the clock signal crossing (CK $_t$ /CK $_c$ ) to the first latching data strobe signal crossing (DQS $x_t$ , DQS $x_c$ ). When the device is operated with input clock jitter, this parameter must be derated by the actual  $t_{\text{JIT}}(\text{per})_{\text{act}}$  of the input clock in excess of  $t_{\text{JIT}}(\text{per})_{\text{allowed}}$ .

$$t_{\text{DQSS}}(\text{min,derated}) = 0.75 - \left( \frac{t_{\text{JIT}}(\text{per})_{\text{act,min}} - t_{\text{JIT}}(\text{per})_{\text{allowed,min}}}{t_{\text{CK}}(\text{avg})} \right)$$

$$t_{\text{DQSS}}(\text{max,derated}) = 1.25 - \left( \frac{t_{\text{JIT}}(\text{per})_{\text{act,max}} - t_{\text{JIT}}(\text{per})_{\text{allowed,max}}}{t_{\text{CK}}(\text{avg})} \right)$$

For example, if the measured jitter into an LPDDR2-800 device has  $t_{\text{CK}}(\text{avg}) = 2500\text{ps}$ ,  $t_{\text{JIT}}(\text{per})_{\text{act,min}} = -172\text{ps}$ , and  $t_{\text{JIT}}(\text{per})_{\text{act,max}} = +193\text{ps}$ , then:

$$t_{\text{DQSS}}(\text{min,derated}) = 0.75 - (t_{\text{JIT}}(\text{per})_{\text{act,min}} - t_{\text{JIT}}(\text{per})_{\text{allowed,min}}) / t_{\text{CK}}(\text{avg}) = 0.75 - (-172 + 100) / 2500 = 0.7788 t_{\text{CK}}(\text{avg}), \text{ and}$$

$$t_{\text{DQSS}}(\text{max,derated}) = 1.25 - (t_{\text{JIT}}(\text{per})_{\text{act,max}} - t_{\text{JIT}}(\text{per})_{\text{allowed,max}}) / t_{\text{CK}}(\text{avg}) = 1.25 - (193 - 100) / 2500 = 1.2128 t_{\text{CK}}(\text{avg}).$$



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Refresh Requirements Parameters

### Refresh Requirements Parameters

**Table 93: Refresh Requirement Parameters (Per Density)**

Parameter	Symbol	64Mb	128Mb	256Mb	512Mb	1Gb	2Gb	4Gb	8Gb	Unit	
Number of banks		4	4	4	4	8	8	8	8		
Refresh window: $T_{CASE} \leq 85^{\circ}$	$t_{REFW}$	32	32	32	32	32	32	32	32	ms	
Refresh window: $85^{\circ}C < T_{CASE} \leq 105^{\circ}C$	$t_{REFW}$	8	8	8	8	8	8	8	8	ms	
Required number of REFRESH commands (MIN)	R	2048	2048	4096	4096	4096	8192	8192	8192		
Average time between REFRESH commands (for reference only) $T_{CASE} \leq 85^{\circ}C$	REFab	$t_{REFI}$	15.6	15.6	7.8	7.8	7.8	3.9	3.9	3.9	$\mu s$
	REFpb	$t_{REFIpb}$	(REFpb not supported below 1Gb)				0.975	0.4875	0.4875	0.4875	$\mu s$
Refresh cycle time	$t_{RFCab}$	90	90	90	90	130	130	130	210	ns	
Per-bank REFRESH cycle time	$t_{RFCpb}$	na					60	60	60	90	ns
Burst REFRESH window = $4 \times 8 \times t_{RFCab}$	$t_{REFBW}$	2.88	2.88	2.88	2.88	4.16	4.16	4.16	6.72	$\mu s$	

### AC Timing

**Table 94: AC Timing**

Notes 1–2 apply to all parameters and conditions. AC timing parameters must satisfy the  $t_{CK}$  minimum conditions (in multiples of  $t_{CK}$ ) as well as the timing specifications when values for both are indicated.

Parameter	Symbol	Min/Max	$t_{CK}$ Min	Data Rate							Unit	Notes
				1066	933	800	667	533	400	333		
Maximum frequency		–	–	533	466	400	333	266	200	166	MHz	
<b>Clock Timing</b>												
Average clock period	$t_{CK}(avg)$	MIN	–	1.875	2.15	2.5	3	3.75	5	6	ns	
		MAX	–	100	100	100	100	100	100	100		
Average HIGH pulse width	$t_{CH}(avg)$	MIN	–	0.45	0.45	0.45	0.45	0.45	0.45	0.45	$t_{CK}(avg)$	
		MAX	–	0.55	0.55	0.55	0.55	0.55	0.55	0.55		
Average LOW pulse width	$t_{CL}(avg)$	MIN	–	0.45	0.45	0.45	0.45	0.45	0.45	0.45	$t_{CK}(avg)$	
		MAX	–	0.55	0.55	0.55	0.55	0.55	0.55	0.55		
Absolute clock period	$t_{CK}(abs)$	MIN	–	$t_{CK}(avg)min \pm t_{JIT}(per)min$							ps	
Absolute clock HIGH pulse width (with allowed jitter)	$t_{CH}(abs)$ , allowed	MIN	–	0.43	0.43	0.43	0.43	0.43	0.43	0.43	$t_{CK}(avg)$	
		MAX	–	0.57	0.57	0.57	0.57	0.57	0.57	0.57		
Absolute clock LOW pulse width (with allowed jitter)	$t_{CL}(abs)$ , allowed	MIN	–	0.43	0.43	0.43	0.43	0.43	0.43	0.43	$t_{CK}(avg)$	
		MAX	–	0.57	0.57	0.57	0.57	0.57	0.57	0.57		
Clock period jitter (with supported jitter)	$t_{JIT}(per)$ , allowed	MIN	–	-90	-95	-100	-110	-120	-140	-150	ps	
		MAX	–	90	95	100	110	120	140	150		



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM AC Timing

**Table 94: AC Timing (Continued)**

Notes 1–2 apply to all parameters and conditions. AC timing parameters must satisfy the  $t_{CK}$  minimum conditions (in multiples of  $t_{CK}$ ) as well as the timing specifications when values for both are indicated.

Parameter	Symbol	Min/ Max	$t_{CK}$ Min	Data Rate							Unit	Notes
				1066	933	800	667	533	400	333		
Maximum clock jitter between two consecutive clock cycles (with allowed jitter)	$t_{JIT(cc)}$ , allowed	MAX	–	180	190	200	220	240	280	300	ps	
Duty cycle jitter (with allowed jitter)	$t_{JIT(duty)}$ , allowed	MIN	–	MIN ( $(t_{CH(ABS),min} - t_{CH(avg),min})$ , $(t_{CL(ABS),min} - t_{CL(avg),min}) \times t_{CK(avg)}$ )							ps	
		MAX	–	MAX ( $(t_{CH(ABS),max} - t_{CH(avg),max})$ , $(t_{CL(ABS),max} - t_{CL(avg),max}) \times t_{CK(avg)}$ )								
Cumulative errors across 2 cycles	$t_{ERR(2per)}$ , allowed	MIN	–	-132	-140	-147	-162	-177	-206	-221	ps	
		MAX	–	132	140	147	162	177	206	221		
Cumulative errors across 3 cycles	$t_{ERR(3per)}$ , allowed	MIN	–	-157	-166	-175	-192	-210	-245	-262	ps	
		MAX	–	157	166	175	192	210	245	262		
Cumulative errors across 4 cycles	$t_{ERR(4per)}$ , allowed	MIN	–	-175	-185	-194	-214	-233	-272	-291	ps	
		MAX	–	175	185	194	214	233	272	291		
Cumulative errors across 5 cycles	$t_{ERR(5per)}$ , allowed	MIN	–	-188	-199	-209	-230	-251	-293	-314	ps	
		MAX	–	188	199	209	230	251	293	314		
Cumulative errors across 6 cycles	$t_{ERR(6per)}$ , allowed	MIN	–	-200	-211	-222	-244	-266	-311	-333	ps	
		MAX	–	200	211	222	244	266	311	333		
Cumulative errors across 7 cycles	$t_{ERR(7per)}$ , allowed	MIN	–	-209	-221	-232	-256	-279	-325	-348	ps	
		MAX	–	209	221	232	256	279	325	348		
Cumulative errors across 8 cycles	$t_{ERR(8per)}$ , allowed	MIN	–	-217	-229	-241	-266	-290	-338	-362	ps	
		MAX	–	217	229	241	266	290	338	362		
Cumulative errors across 9 cycles	$t_{ERR(9per)}$ , allowed	MIN	–	-224	-237	-249	-274	-299	-349	-374	ps	
		MAX	–	224	237	249	274	299	349	374		
Cumulative errors across 10 cycles	$t_{ERR(10per)}$ , allowed	MIN	–	-231	-244	-257	-282	-308	-359	-385	ps	
		MAX	–	231	244	257	282	308	359	385		
Cumulative errors across 11 cycles	$t_{ERR(11per)}$ , allowed	MIN	–	-237	-250	-263	-289	-316	-368	-395	ps	
		MAX	–	237	250	263	289	316	368	395		
Cumulative errors across 12 cycles	$t_{ERR(12per)}$ , allowed	MIN	–	-242	-256	-269	-296	-323	-377	-403	ps	
		MAX	–	242	256	269	296	323	377	403		
Cumulative errors across $n = 13, 14, 15, \dots, 49, 50$ cycles	$t_{ERR(nper)}$ , allowed	MIN		$t_{ERR(nper),allowed,min} = (1 + 0.68 \ln(n)) \times t_{JIT(per),allowed,min}$							ps	
		MAX		$t_{ERR(nper),allowed,max} = (1 + 0.68 \ln(n)) \times t_{JIT(per),allowed,max}$								
<b>ZQ Calibration Parameters</b>												
Initialization calibration time	$t_{ZQINIT}$	MIN	–	1	1	1	1	1	1	1	$\mu$ s	
Long calibration time	$t_{ZQCL}$	MIN	6	360	360	360	360	360	360	360	ns	
Short calibration time	$t_{ZQCS}$	MIN	6	90	90	90	90	90	90	90	ns	





## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM AC Timing

**Table 94: AC Timing (Continued)**

Notes 1–2 apply to all parameters and conditions. AC timing parameters must satisfy the  $t_{CK}$  minimum conditions (in multiples of  $t_{CK}$ ) as well as the timing specifications when values for both are indicated.

Parameter	Symbol	Min/ Max	$t_{CK}$ Min	Data Rate							Unit	Notes
				1066	933	800	667	533	400	333		
Calibration RESET time	$t_{ZQRESET}$	MIN	3	50	50	50	50	50	50	50	ns	
<b>READ Parameters<sup>3</sup></b>												
DQS output access time from CK_t/CK_c	$t_{DQSK}$	MIN	–	2500	2500	2500	2500	2500	2500	2500	ps	
		MAX	–	5500	5500	5500	5500	5500	5500	5500		
DQSK delta short	$t_{DQSKDS}$	MAX	–	330	380	450	540	670	900	1080	ps	4
DQSK delta medium	$t_{DQSKDM}$	MAX	–	680	780	900	1050	1350	1800	1900	ps	5
DQSK delta long	$t_{DQSKDL}$	MAX	–	920	1050	1200	1400	1800	2400	–	ps	6
DQS-DQ skew	$t_{DQSQ}$	MAX	–	200	220	240	280	340	400	500	ps	
Data-hold skew factor	$t_{QHS}$	MAX	–	230	260	280	340	400	480	600	ps	
DQS output HIGH pulse width	$t_{QSH}$	MIN	–	$t_{CH(ABS)} - 0.05$							$t_{CK}$ (avg)	
DQS output LOW pulse width	$t_{QSL}$	MIN	–	$t_{CL(ABS)} - 0.05$							$t_{CK}$ (avg)	
Data half period	$t_{QHP}$	MIN	–	MIN ( $t_{QSH}$ , $t_{QSL}$ )							$t_{CK}$ (avg)	
DQ/DQS output hold time from DQS	$t_{QH}$	MIN	–	$t_{QHP} - t_{QHS}$							ps	
READ preamble	$t_{RPRE}$	MIN	–	0.9	0.9	0.9	0.9	0.9	0.9	0.9	$t_{CK}$ (avg)	7
READ postamble	$t_{RPST}$	MIN	–	$t_{CL(ABS)} - 0.05$							$t_{CK}$ (avg)	8
DQS Low-Z from clock	$t_{LZ(DQS)}$	MIN	–	$t_{DQSK}(\text{MIN}) - 300$							ps	
DQ Low-Z from clock	$t_{LZ(DQ)}$	MIN	–	$t_{DQSK}(\text{MIN}) - (1.4 \times t_{QHS}(\text{MAX}))$							ps	
DQS High-Z from clock	$t_{HZ(DQS)}$	MAX	–	$t_{DQSK}(\text{MAX}) - 100$							ps	
DQ High-Z from clock	$t_{HZ(DQ)}$	MAX	–	$t_{DQSK}(\text{MAX}) + (1.4 \times t_{DQSQ}(\text{MAX}))$							ps	
<b>WRITE Parameters<sup>3</sup></b>												
DQ and DM input hold time ( $V_{REF}$ based)	$t_{DH}$	MIN	–	210	235	270	350	430	480	600	ps	
DQ and DM input setup time ( $V_{REF}$ based)	$t_{DS}$	MIN	–	210	235	270	350	430	480	600	ps	
DQ and DM input pulse width	$t_{DIPW}$	MIN	–	0.35	0.35	0.35	0.35	0.35	0.35	0.35	$t_{CK}$ (avg)	
Write command to first DQS latching transition	$t_{DQSS}$	MIN	–	0.75	0.75	0.75	0.75	0.75	0.75	0.75	$t_{CK}$ (avg)	
		MAX	–	1.25	1.25	1.25	1.25	1.25	1.25	1.25	$t_{CK}$ (avg)	
DQS input high-level width	$t_{DQSH}$	MIN	–	0.4	0.4	0.4	0.4	0.4	0.4	0.4	$t_{CK}$ (avg)	



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM AC Timing

**Table 94: AC Timing (Continued)**

Notes 1–2 apply to all parameters and conditions. AC timing parameters must satisfy the  $t_{CK}$  minimum conditions (in multiples of  $t_{CK}$ ) as well as the timing specifications when values for both are indicated.

Parameter	Symbol	Min/ Max	$t_{CK}$ Min	Data Rate							Unit	Notes
				1066	933	800	667	533	400	333		
DQS input low-level width	$t_{DQSL}$	MIN	–	0.4	0.4	0.4	0.4	0.4	0.4	0.4	$t_{CK}$ (avg)	
DQS falling edge to CK setup time	$t_{DSS}$	MIN	–	0.2	0.2	0.2	0.2	0.2	0.2	0.2	$t_{CK}$ (avg)	
DQS falling edge hold time from CK	$t_{DSH}$	MIN	–	0.2	0.2	0.2	0.2	0.2	0.2	0.2	$t_{CK}$ (avg)	
Write postamble	$t_{WPST}$	MIN	–	0.4	0.4	0.4	0.4	0.4	0.4	0.4	$t_{CK}$ (avg)	
Write preamble	$t_{WPRE}$	MIN	–	0.35	0.35	0.35	0.35	0.35	0.35	0.35	$t_{CK}$ (avg)	
<b>CKE Input Parameters</b>												
CKE minimum pulse width (HIGH and LOW pulse width)	$t_{CKE}$	MIN	3	3	3	3	3	3	3	3	$t_{CK}$ (avg)	
CKE input setup time	$t_{ISCKE}$	MIN	–	0.25	0.25	0.25	0.25	0.25	0.25	0.25	$t_{CK}$ (avg)	9
CKE input hold time	$t_{IHCKE}$	MIN	–	0.25	0.25	0.25	0.25	0.25	0.25	0.25	$t_{CK}$ (avg)	10
<b>Command Address Input Parameters<sup>3</sup></b>												
Address and control input setup time ( Vref based )	$t_{IS}$	MIN	–	220	250	290	370	460	600	740	ps	11
Address and control input hold time ( Vref based )	$t_{IH}$	MIN	–	220	250	290	370	460	600	740	ps	11
Address and control input pulse width	$t_{IPW}$	MIN	–	0.40	0.40	0.40	0.40	0.40	0.40	0.40	$t_{CK}$ (avg)	
<b>Boot Parameters (10 MHz–55 MHz)<sup>12, 13, 14</sup></b>												
Clock cycle time	$t_{CKb}$	MAX	–	100	100	100	100	100	100	100	ns	
		MIN	–	18	18	18	18	18	18	18		
CKE input setup time	$t_{ISCKEb}$	MIN	–	2.5	2.5	2.5	2.5	2.5	2.5	2.5	ns	
CKE input hold time	$t_{IHCKEb}$	MIN	–	2.5	2.5	2.5	2.5	2.5	2.5	2.5	ns	
Address and control input setup time	$t_{ISb}$	MIN	–	1150	1150	1150	1150	1150	1150	1150	ps	
Address and control input hold time	$t_{IHb}$	MIN	–	1150	1150	1150	1150	1150	1150	1150	ps	
DQS output data access time from CK_t/CK_c	$t_{DQSCKb}$	MIN	–	2.0	2.0	2.0	2.0	2.0	2.0	2.0	ns	
		MAX	–	10.0	10.0	10.0	10.0	10.0	10.0	10.0		
Data strobe edge to output data edge $t_{DQSQb} - 1.2$	$t_{DQSQb}$	MAX	–	1.2	1.2	1.2	1.2	1.2	1.2	1.2	ns	
Data hold skew factor	$t_{QHSb}$	MAX	–	1.2	1.2	1.2	1.2	1.2	1.2	1.2	ns	



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM AC Timing

**Table 94: AC Timing (Continued)**

Notes 1–2 apply to all parameters and conditions. AC timing parameters must satisfy the  $t_{CK}$  minimum conditions (in multiples of  $t_{CK}$ ) as well as the timing specifications when values for both are indicated.

Parameter	Symbol	Min/ Max	$t_{CK}$ Min	Data Rate							Unit	Notes
				1066	933	800	667	533	400	333		
<b>Mode Register Parameters</b>												
MODE REGISTER WRITE command period	$t_{MRW}$	MIN	5	5	5	5	5	5	5	5	$t_{CK}$ (avg)	
MODE REGISTER READ command period	$t_{MRR}$	MIN	2	2	2	2	2	2	2	2	$t_{CK}$ (avg)	
<b>Core Parameters<sup>15</sup></b>												
READ latency	RL	MIN	3	8	7	6	5	4	3	3	$t_{CK}$ (avg)	
WRITE latency	WL	MIN	1	4	4	3	2	2	1	1	$t_{CK}$ (avg)	
ACTIVATE-to-ACTIVATE command period	$t_{RC}$	MIN	–	$t_{RAS} + t_{RPab}$ (with all-bank precharge), $t_{RAS} + t_{RPpb}$ (with per-bank precharge)							ns	17
CKE minimum pulse width during SELF REFRESH (low pulse width during SELF REFRESH)	$t_{CKESR}$	MIN	3	15	15	15	15	15	15	15	ns	
SELF REFRESH exit to next valid command delay	$t_{XSR}$	MIN	2	$t_{RFCab} + 10$							ns	
Exit power-down to next valid command delay	$t_{XP}$	MIN	2	7.5	7.5	7.5	7.5	7.5	7.5	7.5	ns	
CAS-to-CAS delay	$t_{CCD}$	MIN	2	2	2	2	2	2	2	2	$t_{CK}$ (avg)	
Internal READ to PRECHARGE command delay	$t_{RTP}$	MIN	2	7.5	7.5	7.5	7.5	7.5	7.5	7.5	ns	
RAS-to-CAS delay	$t_{RCD}$	MIN	3	18	18	18	18	18	18	18	ns	
Row precharge time (single bank)	$t_{RPpb}$	MIN	3	18	18	18	18	18	18	18	ns	
Row precharge time (all banks)	$t_{RPab}$ 4-bank	MIN	3	18	18	18	18	18	18	18	ns	
Row precharge time (all banks)	$t_{RPab}$ 8-bank	MIN	3	21	21	21	21	21	21	21	ns	
Row active time	$t_{RAS}$	MIN	3	42	42	42	42	42	42	42	ns	
		MAX	–	70	70	70	70	70	70	70	$\mu s$	
WRITE recovery time	$t_{WR}$	MIN	3	15	15	15	15	15	15	15	ns	
Internal WRITE-to-READ command delay	$t_{WTR}$	MIN	2	7.5	7.5	7.5	7.5	7.5	10	10	ns	
Active bank <i>a</i> to active bank <i>b</i>	$t_{RRD}$	MIN	2	10	10	10	10	10	10	10	ns	
Four-bank activate window	$t_{FAW}$	MIN	8	50	50	50	50	50	50	60	ns	
Minimum deep power-down time	$t_{DPD}$	MIN	–	500	500	500	500	500	500	500	$\mu s$	
<b>Temperature Derating<sup>16</sup></b>												


**Table 94: AC Timing (Continued)**

Notes 1–2 apply to all parameters and conditions. AC timing parameters must satisfy the  $t_{CK}$  minimum conditions (in multiples of  $t_{CK}$ ) as well as the timing specifications when values for both are indicated.

Parameter	Symbol	Min/ Max	$t_{CK}$ Min	Data Rate						Unit	Notes	
				1066	933	800	667	533	400			333
$t_{DQCK}$ derating	$t_{DQCK}$ (derated)	MAX	–	5620	6000	6000	6000	6000	6000	6000	ps	
Core timing temperature derating	$t_{RCD}$ (derated)	MIN	–	$t_{RCD} + 1.875$						ns		
	$t_{RC}$ (derated)	MIN	–	$t_{RC} + 1.875$						ns		
	$t_{RAS}$ (derated)	MIN	–	$t_{RAS} + 1.875$						ns		
	$t_{RP}$ (derated)	MIN	–	$t_{RP} + 1.875$						ns		
	$t_{RRD}$ (derated)	MIN	–	$t_{RRD} + 1.875$						ns		

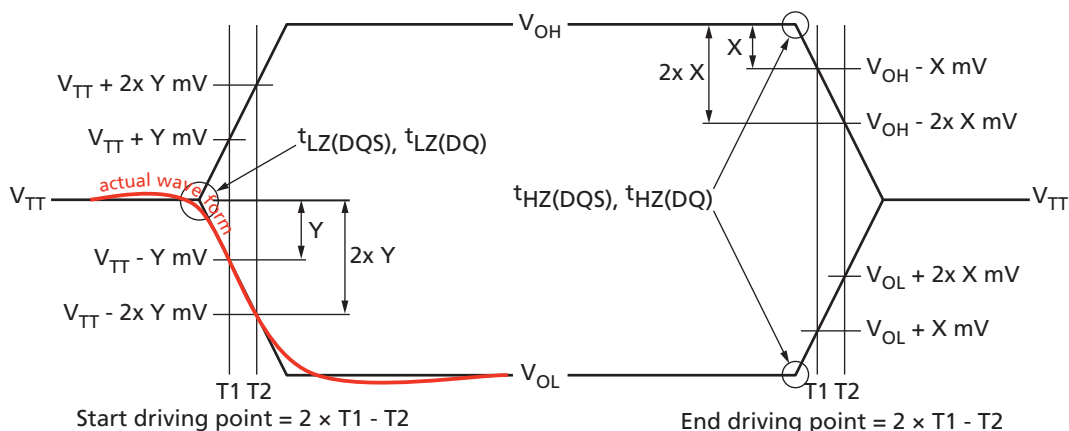
- Notes:
1. Frequency values are for reference only. Clock cycle time ( $t_{CK}$ ) is used to determine device capabilities.
  2. All AC timings assume an input slew rate of 1 V/ns.
  3. READ, WRITE, and input setup and hold values are referenced to  $V_{REF}$ .
  4.  $t_{DQCKDS}$  is the absolute value of the difference between any two  $t_{DQCK}$  measurements (in a byte lane) within a contiguous sequence of bursts in a 160ns rolling window.  $t_{DQCKDS}$  is not tested and is guaranteed by design. Temperature drift in the system is  $<10^{\circ}C/s$ . Values do not include clock jitter.
  5.  $t_{DQCKDM}$  is the absolute value of the difference between any two  $t_{DQCK}$  measurements (in a byte lane) within a 1.6 $\mu$ s rolling window.  $t_{DQCKDM}$  is not tested and is guaranteed by design. Temperature drift in the system is  $<10^{\circ}C/s$ . Values do not include clock jitter.
  6.  $t_{DQCKDL}$  is the absolute value of the difference between any two  $t_{DQCK}$  measurements (in a byte lane) within a 32ms rolling window.  $t_{DQCKDL}$  is not tested and is guaranteed by design. Temperature drift in the system is  $<10^{\circ}C/s$ . Values do not include clock jitter.

For LOW-to-HIGH and HIGH-to-LOW transitions, the timing reference is at the point when the signal crosses the transition threshold ( $V_{TT}$ ).  $t_{HZ}$  and  $t_{LZ}$  transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for  $t_{RPST}$ ,  $t_{HZ}(DQS)$  and  $t_{HZ}(DQ)$ ), or begins driving (for  $t_{RPRE}$ ,  $t_{LZ}(DQS)$ ,  $t_{LZ}(DQ)$ ). The figure below shows a method to calculate the point when the device is no longer driving  $t_{HZ}(DQS)$  and  $t_{HZ}(DQ)$  or begins driving  $t_{LZ}(DQS)$  and  $t_{LZ}(DQ)$  by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters  $t_{LZ}(DQS)$ ,  $t_{LZ}(DQ)$ ,  $t_{HZ}(DQS)$ , and  $t_{HZ}(DQ)$  are defined as single-ended. The timing parameters  $t_{RPRE}$  and  $t_{RPST}$  are determined from the differential signal  $DQS_t/DQS_c$ .

### Output Transition Timing



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM CA and CS\_n Setup, Hold, and Derating



7. Measured from the point when DQS\_t/DQS\_c begins driving the signal, to the point when DQS\_t/DQS\_c begins driving the first rising strobe edge.
8. Measured from the last falling strobe edge of DQS\_t/DQS\_c to the point when DQS\_t/DQS\_c finishes driving the signal.
9. CKE input setup time is measured from CKE reaching a HIGH/LOW voltage level to CK\_t/CK\_c crossing.
10. CKE input hold time is measured from CK\_t/CK\_n crossing to CKE reaching a HIGH/LOW voltage level.
11. Input setup/hold time for signal (CA[9:0], CS\_n).
12. To ensure device operation before the device is configured, a number of AC boot timing parameters are defined in this table. The letter b is appended to the boot parameter symbols (for example,  $t_{CK}$  during boot is  $t_{CKb}$ ).
13. Mobile LPDDR2 devices set some mode register default values upon receiving a RESET (MRW) command, as specified in Mode Register Definition.
14. The output skew parameters are measured with default output impedance settings using the reference load.
15. The minimum  $t_{CK}$  column applies only when  $t_{CK}$  is greater than 6ns.
16. Timing derating applies for operation at 85°C to 105°C when the requirement to derate is indicated by mode register 4 op-code (see the MR4 Device Temperature (MA[7:0] = 04h) table).
17. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in reduction of the product lifetime.

## CA and CS\_n Setup, Hold, and Derating

For all input signals (CA and CS\_n), the total required setup time ( $t_{IS}$ ) and hold time ( $t_{IH}$ ) are calculated by adding the data sheet  $t_{IS}$  (base) and  $t_{IH}$  (base) values to the  $\Delta t_{IS}$  and  $\Delta t_{IH}$  derating values, respectively. Example:  $t_{IS}$  (total setup time) =  $t_{IS}(\text{base}) + \Delta t_{IS}$ . (See the series of tables following this section.)

The typical setup slew rate ( $t_{IS}$ ) for a rising signal is defined as the slew rate between the last crossing of  $V_{REF(DC)}$  and the first crossing of  $V_{IH(AC)\min}$ . The typical setup slew rate for a falling signal is defined as the slew rate between the last crossing of  $V_{REF(DC)}$  and the first crossing of  $V_{IL(AC)\max}$ . If the actual signal is consistently earlier than the typical slew rate line between the shaded  $V_{REF(DC)}$ -to-(AC) region, use the typical slew rate for the derating value (see Figure 83 (page 145)). If the actual signal is later than the typical slew rate line anywhere between the shaded  $V_{REF(DC)}$ -to-AC region, the slew rate of a



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM CA and CS<sub>n</sub> Setup, Hold, and Derating

tangent line to the actual signal from the AC level to the DC level is used for the derating value (see Figure 85 (page 147)).

The hold ( $t_{IH}$ ) typical slew rate for a rising signal is defined as the slew rate between the last crossing of  $V_{IL(DC)max}$  and the first crossing of  $V_{REF(DC)}$ . The hold ( $t_{IH}$ ) typical slew rate for a falling signal is defined as the slew rate between the last crossing of  $V_{IH(DC)min}$  and the first crossing of  $V_{REF(DC)}$ . If the actual signal is consistently later than the typical slew rate line between the shaded DC-to- $V_{REF(DC)}$  region, use the typical slew rate for the derating value (see Figure 84 (page 146)). If the actual signal is earlier than the typical slew rate line anywhere between the shaded DC-to- $V_{REF(DC)}$  region, the slew rate of a tangent line to the actual signal from the DC level to  $V_{REF(DC)}$  level is used for the derating value (see Figure 86 (page 148)).

For a valid transition, the input signal must remain above or below  $V_{IH}/V_{IL(AC)}$  for a specified time,  $t_{VAC}$  (see Table 99 (page 143)).

For slow slew rates the total setup time could be a negative value; that is, a valid input signal will not have reached  $V_{IH}/V_{IL(AC)}$  at the time of the rising clock transition. A valid input signal is still required to complete the transition and reach  $V_{IH}/V_{IL(AC)}$ .

For slew rates between the values listed in Table 97, the derating values are obtained using linear interpolation. Typically, slew rate values are not subject to production testing. They are verified by design and characterization.

**Table 95: CA and CS<sub>n</sub> Setup and Hold Base Values (>400 MHz, 1 V/ns Slew Rate)**

Parameter	Data Rate						Reference
	1066	933	800	667	533	466	
$t_{IS}$ (base)	0	30	70	150	240	300	$V_{IH}/V_{IL(AC)} = V_{REF(DC)} \pm 220mV$
$t_{IH}$ (base)	90	120	160	240	330	390	$V_{IH}/V_{IL(DC)} = V_{REF(DC)} \pm 130mV$

Note: 1. AC/DC referenced for 1 V/ns CA and CS<sub>n</sub> slew rate, and 2 V/ns differential CK<sub>t</sub>/CK<sub>c</sub> slew rate.

**Table 96: CA and CS<sub>n</sub> Setup and Hold Base Values (<400 MHz, 1 V/ns Slew Rate)**

Parameter	Data Rate				Reference
	400	333	266	200	
$t_{IS}$ (base)	300	440	600	850	$V_{IH}/V_{IL(AC)} = V_{REF(DC)} \pm 300mV$
$t_{IH}$ (base)	400	540	700	950	$V_{IH}/V_{IL(DC)} = V_{REF(DC)} \pm 200mV$

Note: 1. AC/DC referenced for 1 V/ns CA and CS<sub>n</sub> slew rate, and 2 V/ns differential CK<sub>t</sub>/CK<sub>c</sub> slew rate.



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM

### CA and CS\_n Setup, Hold, and Derating

**Table 97: Derating Values for AC/DC-Based  $t_{IS}/t_{IH}$  (AC220)**
 $\Delta t_{IS}$ ,  $\Delta t_{IH}$  derating in ps

 AC220 Threshold ->  $V_{IH}(ac)=V_{REF}(dc)+220mV$ ,  $V_{IL}(ac)=V_{REF}(dc)-220mV$ 

 DC100 Threshold ->  $V_{IH}(dc)=V_{REF}(dc)+130mV$ ,  $V_{IL}(dc)=V_{REF}(dc)-130mV$ 

		CK_t, CK_c Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$
CA, CS_n slew rate V/ns	2.0	110	65	110	65	110	65										
	1.5	74	43	73	43	73	43	89	59								
	1.0	0	0	0	0	0	0	16	16	32	32						
	0.9			-3	-5	-3	-5	13	11	29	27	45	43				
	0.8					-8	-13	8	3	24	19	40	35	56	55		
	0.7							2	-6	18	10	34	26	50	46	66	78
	0.6									10	-3	26	13	42	33	58	65
	0.5											4	-4	20	16	36	48
	0.4													-7	2	17	34

Note: 1. Shaded cells are not supported.

**Table 98: Derating Values for AC/DC-Based  $t_{IS}/t_{IH}$  (AC300)**
 $\Delta t_{IS}$ ,  $\Delta t_{IH}$  derating in ps

 AC300 Threshold ->  $V_{IH}(ac)=V_{REF}(dc)+300mV$ ,  $V_{IL}(ac)=V_{REF}(dc)-300mV$ 

 DC200 Threshold ->  $V_{IH}(dc)=V_{REF}(dc)+200mV$ ,  $V_{IL}(dc)=V_{REF}(dc)-200mV$ 

		CK_t, CK_c Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$
CA, CS_n slew rate V/ns	2.0	150	100	150	100	150	100										
	1.5	100	67	100	67	100	67	116	83								
	1.0	0	0	0	0	0	0	16	16	32	32						
	0.9			-4	-8	-4	-8	12	8	28	24	44	40				
	0.8					-12	-20	4	-4	20	12	36	28	52	48		
	0.7							-3	-18	13	-2	29	14	45	34	61	66
	0.6									2	-21	18	-5	34	15	50	47
	0.5											-12	-32	4	-12	20	20
	0.4													-35	-40	-11	-8

Note: 1. Shaded cells are not supported.

**Table 99: Required Time for Valid Transition –  $t_{VAC} > V_{IH}(AC)$  and  $< V_{IL}(AC)$** 

Slew Rate (V/ns)	$t_{VAC}$ at 300mV (ps)		$t_{VAC}$ at 220mV (ps)	
	Min	Max	Min	Max
>2.0	75	–	175	–



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM CA and CS<sub>n</sub> Setup, Hold, and Derating

**Table 99: Required Time for Valid Transition –  $t_{VAC} > V_{IH(AC)}$  and  $< V_{IL(AC)}$  (Continued)**

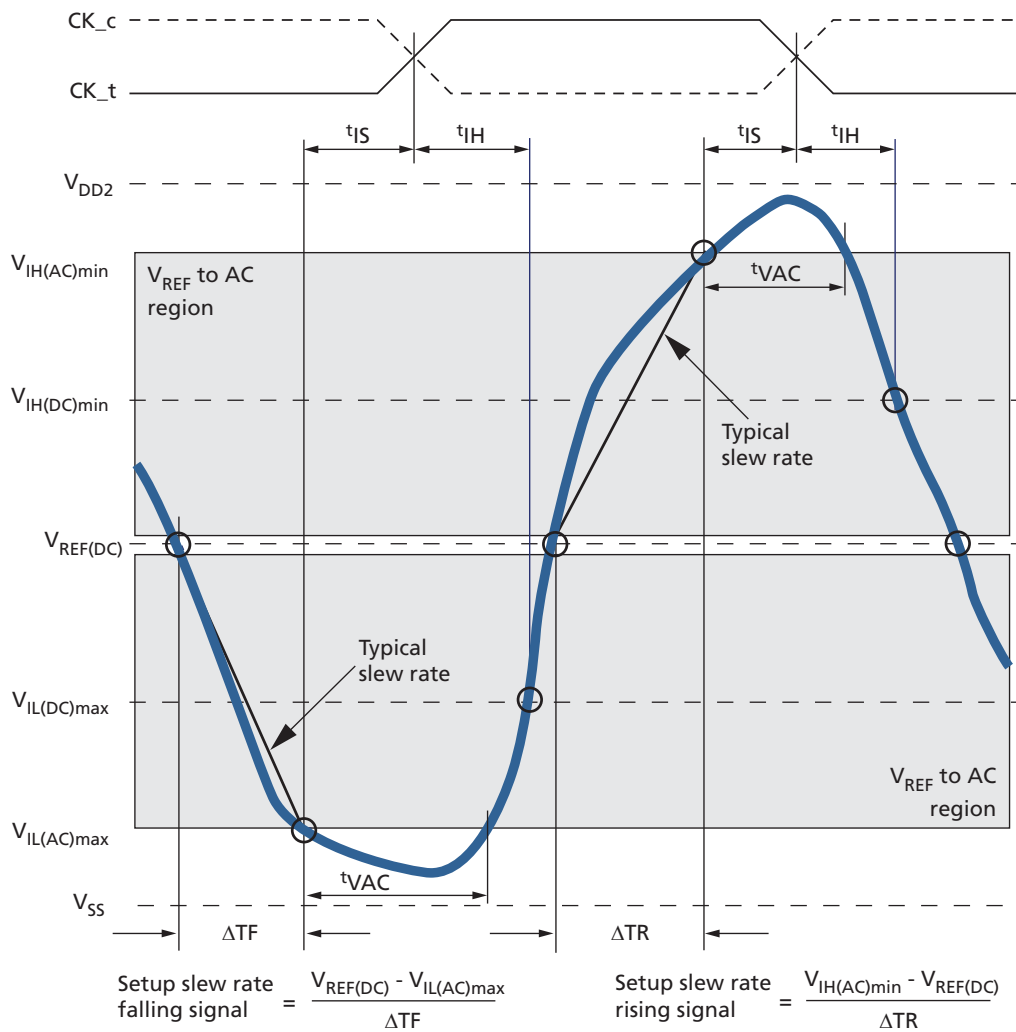
Slew Rate (V/ns)	$t_{VAC}$ at 300mV (ps)		$t_{VAC}$ at 220mV (ps)	
	Min	Max	Min	Max
2.0	57	–	170	–
1.5	50	–	167	–
1.0	38	–	163	–
0.9	34	–	162	–
0.8	29	–	161	–
0.7	22	–	159	–
0.6	13	–	155	–
0.5	0	–	150	–
<0.5	0	–	150	–





## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM CA and CS\_n Setup, Hold, and Derating

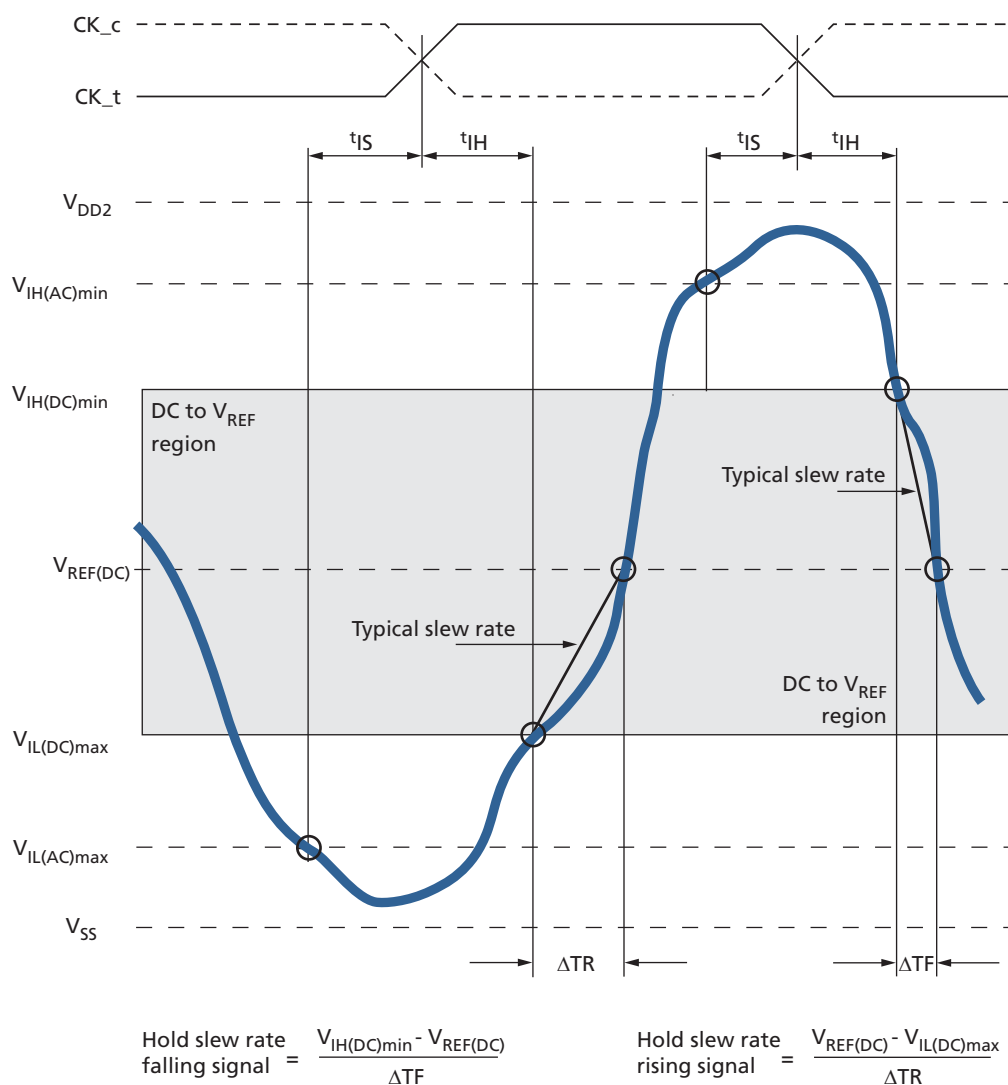
**Figure 83: Typical Slew Rate and  $t_{VAC} - t_{IS}$  for CA and CS\_n Relative to Clock**





## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM CA and CS\_n Setup, Hold, and Derating

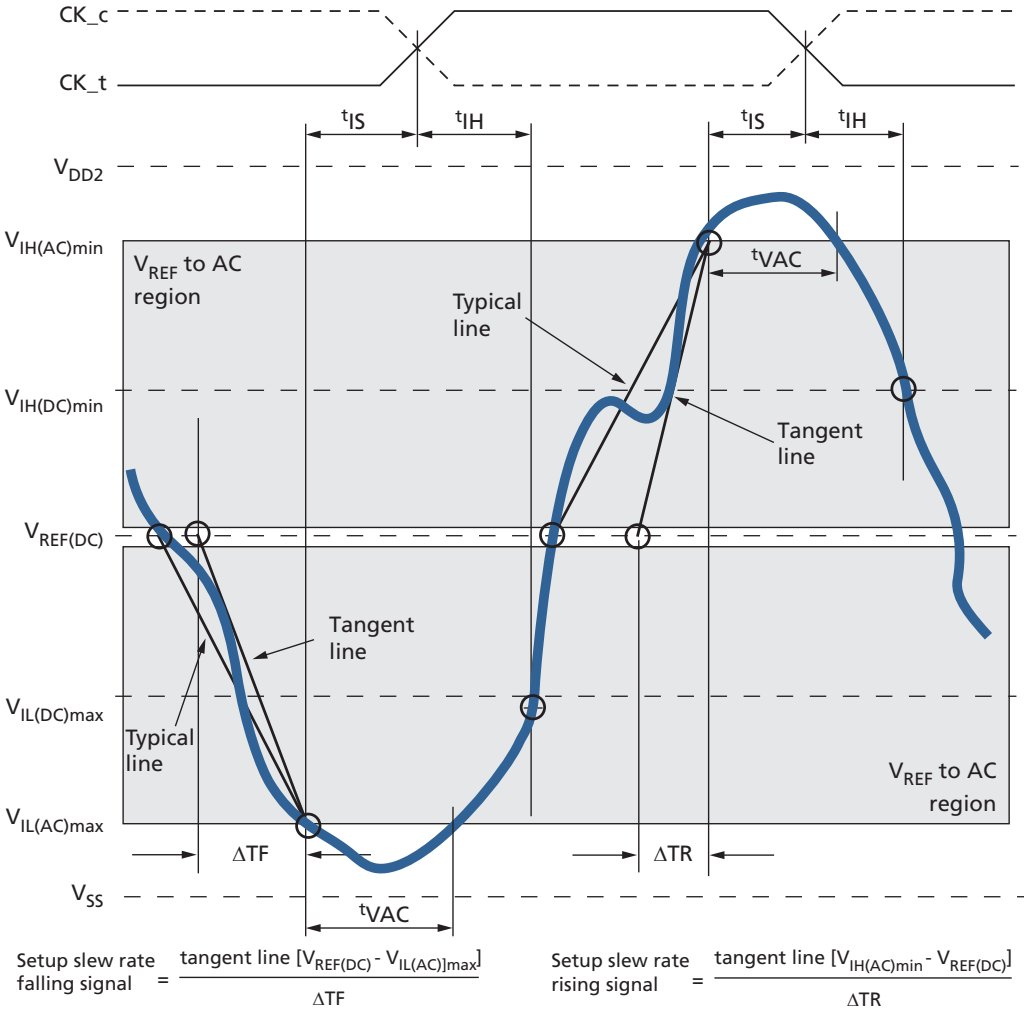
**Figure 84: Typical Slew Rate – t<sub>IH</sub> for CA and CS\_n Relative to Clock**





# 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM CA and CS\_n Setup, Hold, and Derating

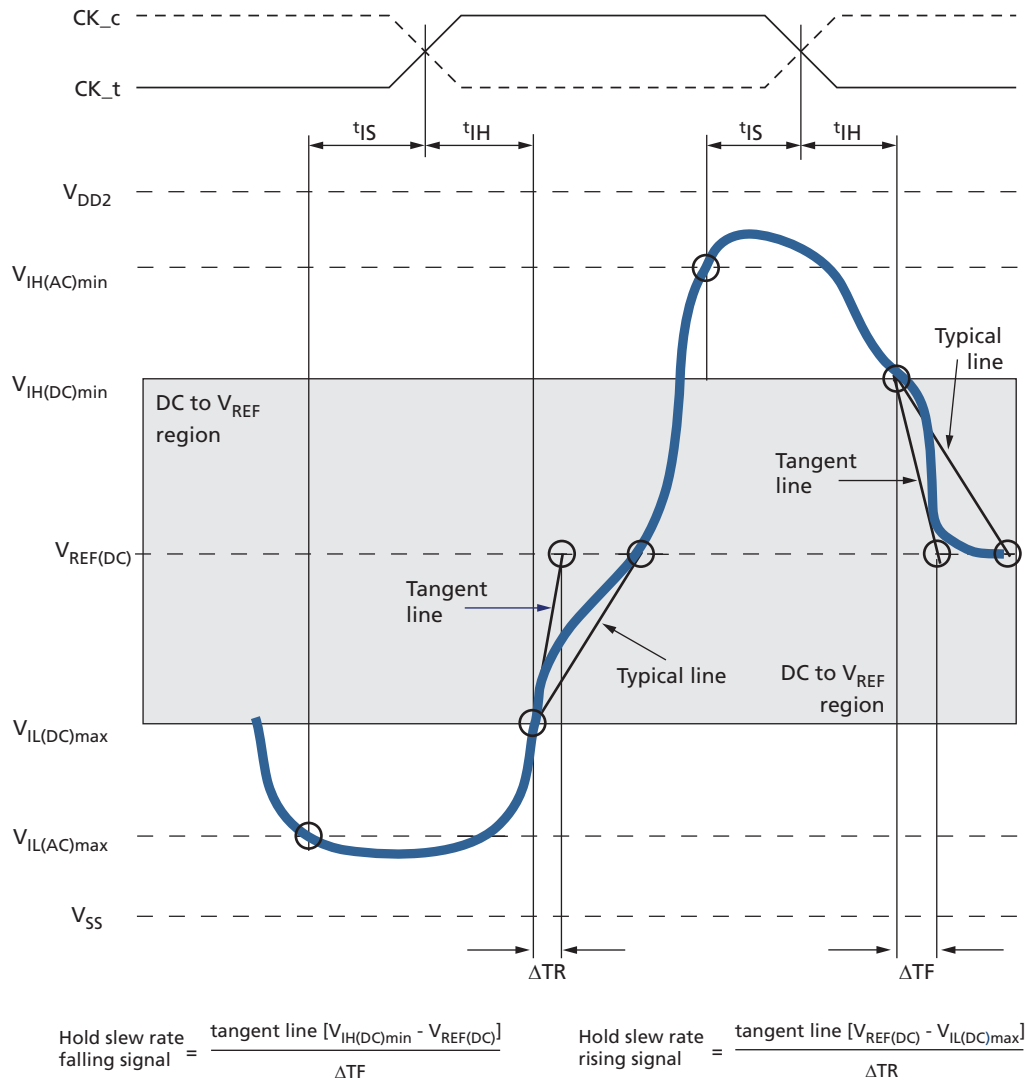
Figure 85: Tangent Line - t<sub>IS</sub> for CA and CS\_n Relative to Clock





## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM CA and CS\_n Setup, Hold, and Derating

**Figure 86: Tangent Line – t<sub>IH</sub> for CA and CS\_n Relative to Clock**





## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Data Setup, Hold, and Slew Rate Derating

### Data Setup, Hold, and Slew Rate Derating

For all input signals (DQ, DM) the total required setup time ( $t_{DS}$ ) and hold time ( $t_{DH}$ ) are calculated by adding the data sheet  $t_{DS}(\text{base})$  and  $t_{DH}(\text{base})$  values (see the following table) to the  $\Delta t_{DS}$  and  $\Delta t_{DH}$  derating values, respectively (see the following derating tables). Example:  $t_{DS} = t_{DS}(\text{base}) + \Delta t_{DS}$ .

The typical  $t_{DS}$  slew rate for a rising signal is defined as the slew rate between the last crossing of  $V_{REF(DC)}$  and the first crossing of  $V_{IH(AC)\min}$ . The typical  $t_{DS}$  slew rate for a falling signal is defined as the slew rate between the last crossing of  $V_{REF(DC)}$  and the first crossing of  $V_{IL(AC)\max}$  (see the Typical Slew Rate and  $t_{VAC} - t_{DS}$  for DQ Relative to Strobe figure).

If the actual signal is consistently earlier than the typical slew rate line in the figure, "Typical Slew Rate and  $t_{VAC} - t_{IS}$  for CA and CS\_n Relative to Clock (CA and CS\_n Setup, Hold, and Derating), the area shaded gray between the  $V_{REF(DC)}$  region and the AC region, use the typical slew rate for the derating value. If the actual signal is later than the typical slew rate line anywhere between the shaded  $V_{REF(DC)}$  region and the AC region, the slew rate of a tangent line to the actual signal from the AC level to the DC level is used for the derating value (see figure "Tangent Line -  $t_{IS}$  for CA and CS\_n Relative to Clock" in CA and CS\_n Setup, Hold, and Derating).

The typical  $t_{DH}$  slew rate for a rising signal is defined as the slew rate between the last crossing of  $V_{IL(DC)\max}$  and the first crossing of  $V_{REF(DC)}$ . The typical  $t_{DH}$  slew rate for a falling signal is defined as the slew rate between the last crossing of  $V_{IH(DC)\min}$  and the first crossing of  $V_{REF(DC)}$  (see the Typical Slew Rate - DH for DQ Relative to Strobe figure).

If the actual signal is consistently later than the typical slew rate line between the shaded DC-level-to- $V_{REF(DC)}$  region, the typical slew rate should be used for the derating value. If the actual signal is earlier than the typical slew rate line anywhere between shaded DC-to- $V_{REF(DC)}$  region, the slew rate of a tangent line to the actual signal from the DC level to the  $V_{REF(DC)}$  level is used for the derating value (see the Tangent Line -  $t_{DH}$  for DQ with Respect to Strobe figure).

For a valid transition, the input signal must remain above or below  $V_{IH}/V_{IL(AC)}$  for the specified time,  $t_{VAC}$  (see the Required Time for Valid Transition -  $t_{VAC} > V_{IH(AC)}$  or  $< V_{IL(AC)}$  table).

The total setup time for slow slew rates could be negative; that is, a valid input signal may not have reached  $V_{IH}/V_{IL(AC)}$  at the time of the rising clock transition. A valid input signal is still required to complete the transition and reach  $V_{IH}/V_{IL(AC)}$ .

For slew rates between the values listed in the following tables, the derating values can be obtained using linear interpolation. Typically, slew rate values are not subject to production testing. They are verified by design and characterization.

**Table 100: Data Setup and Hold Base Values (>400 MHz, 1 V/ns Slew Rate)**

Parameter	Data Rate						Reference
	1066	933	800	667	533	466	
$t_{DS}(\text{base})$	-10	15	50	130	210	230	$V_{IH}/V_{IL(AC)} = V_{REF(DC)} \pm 220\text{mV}$



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM

### Data Setup, Hold, and Slew Rate Derating

**Table 100: Data Setup and Hold Base Values (>400 MHz, 1 V/ns Slew Rate) (Continued)**

Parameter	Data Rate						Reference
	1066	933	800	667	533	466	
$t_{DH}^{(base)}$	80	105	140	220	300	320	$V_{IH}/V_{IL(DC)} = V_{REF(DC)} \pm 130mV$

Note: 1. AC/DC referenced for 1 V/ns DQ, DM slew rate, and 2 V/ns differential DQS<sub>t</sub>/DQS<sub>c</sub> slew rate.

**Table 101: Data Setup and Hold Base Values (<400 MHz, 1 V/ns Slew Rate)**

Parameter	Data Rate				Reference
	400	333	266	200	
$t_{DS}^{(base)}$	180	300	450	700	$V_{IH}/V_{IL(AC)} = V_{REF(DC)} \pm 300mV$
$t_{DH}^{(base)}$	280	400	550	800	$V_{IH}/V_{IL(DC)} = V_{REF(DC)} \pm 200mV$

Note: 1. AC/DC referenced for 1 V/ns DQ, DM slew rate, and 2 V/ns differential DQS<sub>t</sub>/DQS<sub>c</sub> slew rate.

**Table 102: Derating Values for AC/DC-Based  $t_{DS}/t_{DH}$  (AC220)**

$\Delta t_{DS}$ ,  $\Delta t_{DH}$  derating in ps

AC220 Threshold ->  $V_{IH(ac)} = V_{REF(dc)} + 220mV$ ,  $V_{IL(ac)} = V_{REF(dc)} - 220mV$

DC130 Threshold ->  $V_{IH(dc)} = V_{REF(dc)} + 130mV$ ,  $V_{IL(dc)} = V_{REF(dc)} - 130mV$

		DQS <sub>t</sub> , DQS <sub>c</sub> Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$
DQ, DM slew rate V/ns	2.0	110	65	110	65	110	65										
	1.5	74	43	73	43	73	43	89	59								
	1.0	0	0	0	0	0	0	16	16	32	32						
	0.9			-3	-5	-3	-5	13	11	29	27	45	43				
	0.8					-8	-13	8	3	24	19	40	35	56	55		
	0.7							2	-6	18	10	34	26	50	46	66	78
	0.6									10	-3	26	13	42	33	58	65
	0.5											4	-4	20	16	36	48
	0.4													-7	2	17	34

Note: 1. Shaded cells are not supported.



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM

### Data Setup, Hold, and Slew Rate Derating

**Table 103: Derating Values for AC/DC-Based  $t_{DS}/t_{DH}$  (AC300)**
 $\Delta t_{DS}$ ,  $\Delta t_{DH}$  derating in ps

 AC300 Threshold ->  $V_{IH}(ac)=V_{REF}(dc)+300mV$ ,  $V_{IL}(ac)=V_{REF}(dc)-300mV$ 

 DC200 Threshold ->  $V_{IH}(dc)=V_{REF}(dc)+200mV$ ,  $V_{IL}(dc)=V_{REF}(dc)-200mV$ 

		DQS_t, DQS_c Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$
DQ, DM slew rate V/ns	2.0	150	100	150	100	150	100										
	1.5	100	67	100	67	100	67	116	83								
	1.0	0	0	0	0	0	0	16	16	32	32						
	0.9			-4	-8	-4	-8	12	8	28	24	44	40				
	0.8					-12	-20	4	-4	20	12	36	28	52	48		
	0.7							-3	-18	13	-2	29	14	45	34	61	66
	0.6									2	-21	18	-5	34	15	50	47
	0.5											-12	-32	4	-12	20	20
	0.4													-35	-40	-11	-8

Note: 1. Shaded cells are not supported.

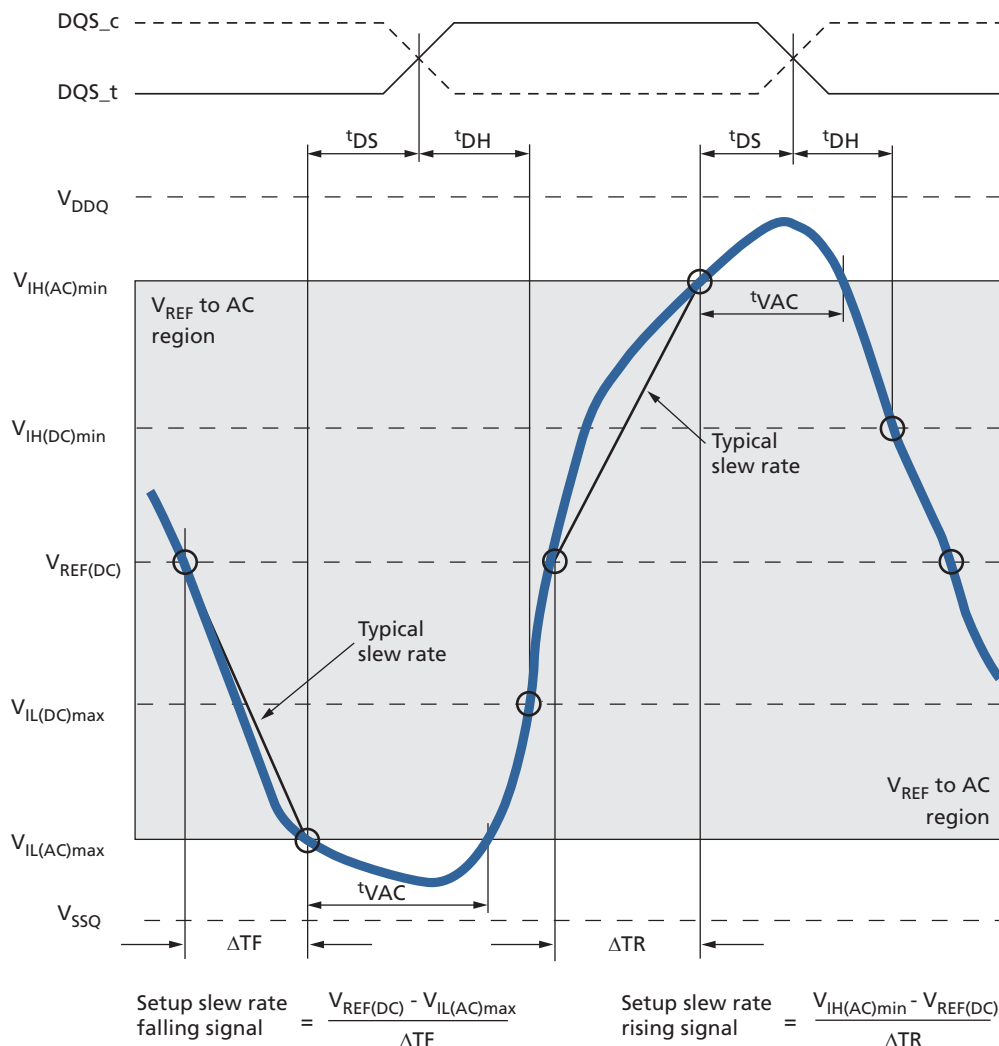
**Table 104: Required Time for Valid Transition –  $t_{VAC} > V_{IH}(AC)$  or  $< V_{IL}(AC)$** 

Slew Rate (V/ns)	$t_{VAC}$ at 300mV (ps)		$t_{VAC}$ at 220mV (ps)	
	Min	Max	Min	Max
>2.0	75	–	175	–
2.0	57	–	170	–
1.5	50	–	167	–
1.0	38	–	163	–
0.9	34	–	162	–
0.8	29	–	161	–
0.7	22	–	159	–
0.6	13	–	155	–
0.5	0	–	150	–
<0.5	0	–	150	–



## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Data Setup, Hold, and Slew Rate Derating

**Figure 87: Typical Slew Rate and  $t_{VAC} - t_{DS}$  for DQ Relative to Strobe**

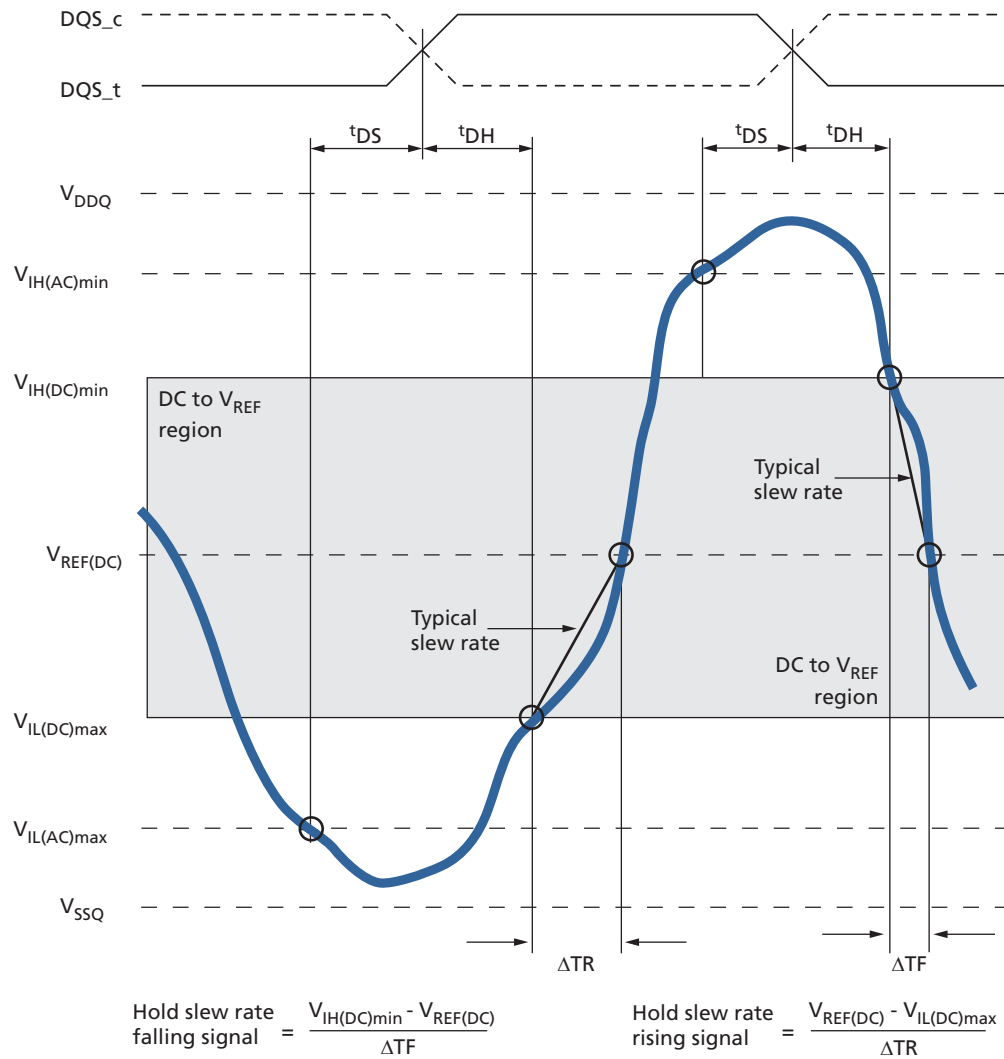






## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Data Setup, Hold, and Slew Rate Derating

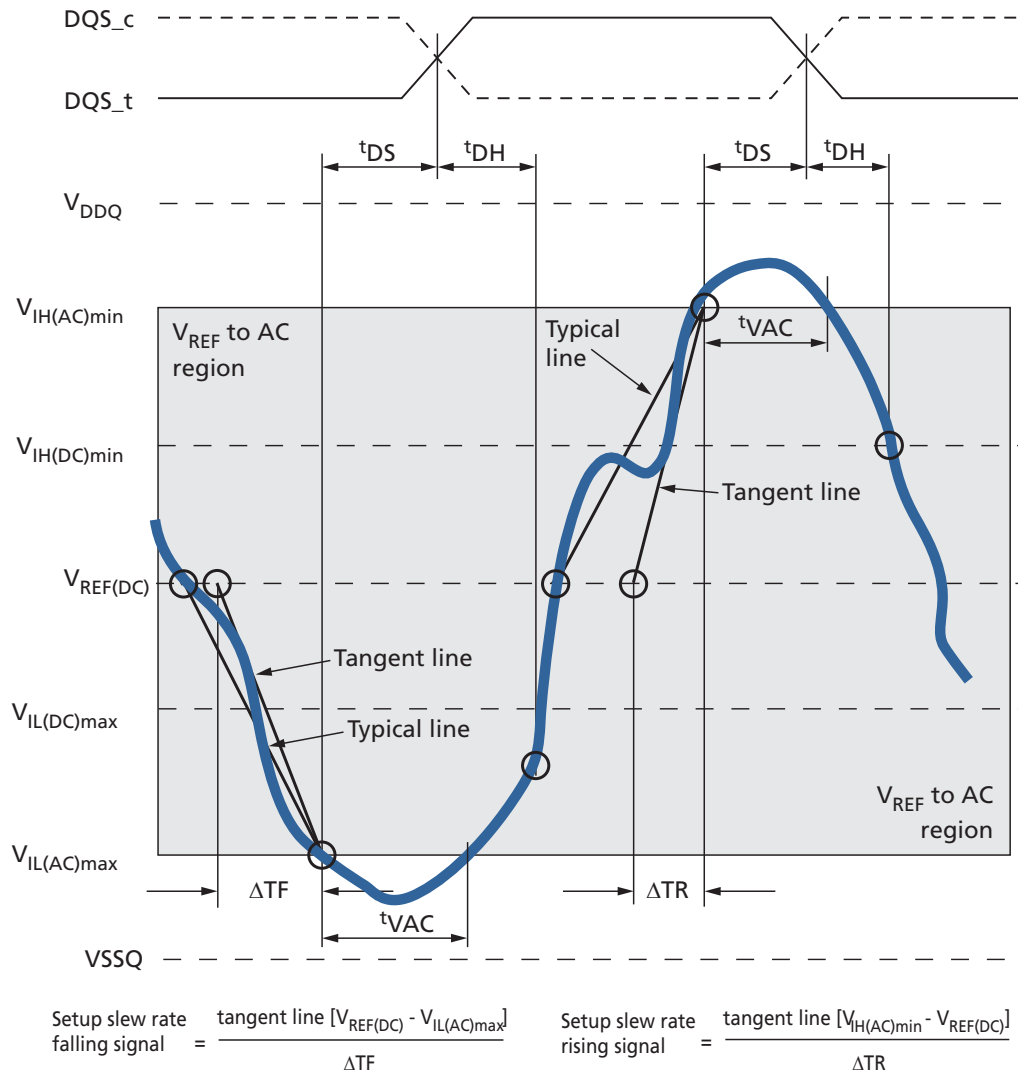
**Figure 88: Typical Slew Rate – t<sub>DH</sub> for DQ Relative to Strobe**





## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Data Setup, Hold, and Slew Rate Derating

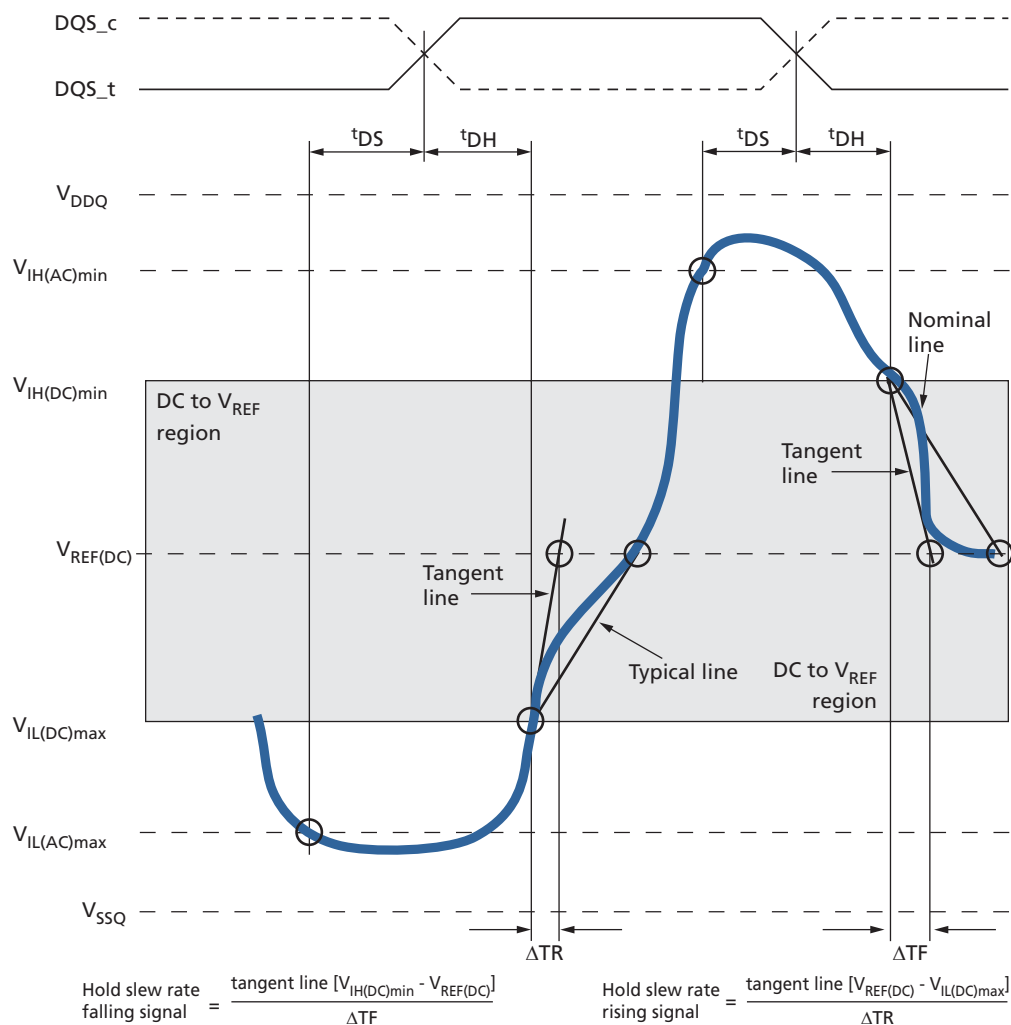
**Figure 89: Tangent Line – t<sub>DS</sub> for DQ with Respect to Strobe**





## 216-Ball and 220-Ball, Dual-Channel Embedded LPDDR2 SDRAM Data Setup, Hold, and Slew Rate Derating

**Figure 90: Tangent Line – t<sub>DH</sub> for DQ with Respect to Strobe**





## Revision History

### Rev. D – 03/16

- Updated Ballout Diagrams for 216-Ball Dual-Channel FBGA – 2 x 4Gb Die and 4x4Gb Die to match Ball Description table

### Rev. C – 02/16

- Preliminary DDP release

### Rev. B – 01/15

- Added 220-ball ballout and a 14x14 package

### Rev. A – 9/14

- Initial release created from the 216b\_2c0e\_2channel Rev. A data sheet

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