

# 1.35V DDR3L SDRAM SODIMM

**MT16KTF25664HZ – 2GB**

**MT16KTF51264HZ – 4GB**

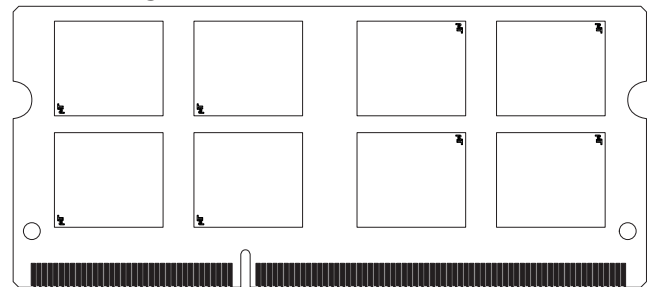
**MT16KTF1G64HZ – 8GB**

## Features

- DDR3L functionality and operations supported as defined in the component data sheet
- 204-pin, small outline dual in-line memory module (SODIMM)
- Fast data transfer rates: PC3-14900, PC3-12800, PC3-10600, PC3-8500, or PC3-6400
- 2GB (256 Meg x 64), 4GB (512 Meg x 64), 8GB (1 Gig x 64)
- $V_{DD} = 1.35V$  (1.283V–1.45V)
- $V_{DD} = 1.5V$  (1.425–1.575V)
- Backward compatible to  $V_{DD} = 1.5V \pm 0.075V$
- $V_{DDSPD} = 3.0\text{--}3.6V$
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Dual rank
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- On-board I<sup>2</sup>C serial presence-detect (SPD) EEPROM
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated control, command, and address bus

**Figure 1: 204-Pin SODIMM (MO-268 R/C F)**

Module height: 30mm (1.181in)



## Options

- Operating temperature
  - Commercial ( $0^{\circ}C \leq T_A \leq +70^{\circ}C$ )
- Package
  - 240-pin DIMM (halogen-free)
- Frequency/CAS latency
  - 1.07ns @ CL = 13 (DDR3-1866)
  - 1.25ns @ CL = 11 (DDR3-1600)
  - 1.5ns @ CL = 9 (DDR3-1333)
  - 1.87ns @ CL = 7 (DDR3-1066)

## Marking

None  
Z  
-1G9  
-1G6  
-1G4  
-1G1

**Table 1: Key Timing Parameters**

Speed Grade	Industry Nomenclature	Data Rate (MT/s)								t <sub>RCD</sub> (ns)	t <sub>RP</sub> (ns)	t <sub>RC</sub> (ns)
		CL = 13	CL = 11	CL = 10	CL = 9	CL = 8	CL = 7	CL = 6	CL = 5			
-1G9	PC3-14900	1866	1600	1333	1333	1066	1066	800	667	13.125	13.125	47.125
-1G6	PC3-12800	–	1600	1333	1333	1066	1066	800	667	13.125	13.125	48.125
-1G4	PC3-10600	–	–	1333	1333	1066	1066	800	667	13.125	13.125	49.125
-1G1	PC3-8500	–	–	–	–	1066	1066	800	667	13.125	13.125	50.625
-1G0	PC3-8500	–	–	–	–	1066	–	800	667	15	15	52.5
-80B	PC3-6400	–	–	–	–	–	–	800	667	15	15	52.5



**Table 2: Addressing**

Parameter	2GB	4GB	8GB
Refresh count	8K	8K	8K
Row address	16K A[13:0]	32K A[14:0]	64K A[15:0]
Device bank address	8 BA[2:0]	8 BA[2:0]	8 BA[2:0]
Device configuration	1Gb (128 Meg x 8)	2Gb (256 Meg x 8)	4Gb (512 Meg x 8)
Column address	1K A[9:0]	1K A[9:0]	1K A[9:0]
Module rank address	2 S#[1:0]	2 S#[1:0]	2 S#[1:0]

**Table 3: Part Numbers and Timing Parameters – 2GB Modules**

Base device: MT41K128M8,<sup>1</sup> 1Gb 1.35V DDR3L SDRAM

Part Number <sup>2</sup>	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL- <sup>t</sup> RCD- <sup>t</sup> RP)
MT16KTF25664HZ-1G6__	2GB	256 Meg x 64	12.8 GB/s	1.25ns/1600 MT/s	11-11-11
MT16KTF25664HZ-1G4__	2GB	256 Meg x 64	10.6 GB/s	1.5ns/1333 MT/s	9-9-9
MT16KTF25664HZ-1G1__	2GB	256 Meg x 64	8.5 GB/s	1.87ns/1066 MT/s	7-7-7

**Table 4: Part Numbers and Timing Parameters – 4GB Modules**

Base device: MT41K256M8,<sup>1</sup> 2Gb 1.35V DDR3L SDRAM

Part Number <sup>2</sup>	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL- <sup>t</sup> RCD- <sup>t</sup> RP)
MT16KTF51264HZ-1G6__	4GB	512 Meg x 64	12.8 GB/s	1.25ns/1600 MT/s	11-11-11
MT16KTF51264HZ-1G6__	4GB	512 Meg x 64	12.8 GB/s	1.25ns/1600 MT/s	11-11-11
MT16KTF51264HZ-1G4__	4GB	512 Meg x 64	10.6 GB/s	1.5ns/1333 MT/s	9-9-9
MT16KTF51264HZ-1G1__	4GB	512 Meg x 64	8.5 GB/s	1.87ns/1066 MT/s	7-7-7

**Table 5: Part Numbers and Timing Parameters – 8GB Modules**

Base device: MT41K512M8,<sup>1</sup> 4Gb 1.35V DDR3L SDRAM

Part Number <sup>2</sup>	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL- <sup>t</sup> RCD- <sup>t</sup> RP)
MT16KTF1G64HZ-1G9__	8GB	1 Gig x 64	14.9 GB/s	1.07ns/1866 MT/s	13-13-13
MT16KTF1G64HZ-1G6__	8GB	1 Gig x 64	12.8 GB/s	1.25ns/1600 MT/s	11-11-11
MT16KTF1G64HZ-1G4__	8GB	1 Gig x 64	10.6 GB/s	1.5ns/1333 MT/s	9-9-9
MT16KTF1G64HZ-1G1__	8GB	1 Gig x 64	8.5 GB/s	1.87ns/1066 MT/s	7-7-7

- Notes:
1. The data sheet for the base device can be found on Micron’s Web site.
  2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MT16KTF51264HZ-1G4M1.



## Pin Assignments

Table 6: Pin Assignments

204-Pin DDR3 SODIMM Front								204-Pin DDR3 SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V <sub>REFDQ</sub>	53	DQ19	105	V <sub>DD</sub>	157	DQ42	2	V <sub>SS</sub>	54	V <sub>SS</sub>	106	V <sub>DD</sub>	158	DQ46
3	V <sub>SS</sub>	55	V <sub>SS</sub>	107	A10	159	DQ43	4	DQ4	56	DQ28	108	BA1	160	DQ47
5	DQ0	57	DQ24	109	BA0	161	V <sub>SS</sub>	6	DQ5	58	DQ29	110	RAS#	162	V <sub>SS</sub>
7	DQ1	59	DQ25	111	V <sub>DD</sub>	163	DQ48	8	V <sub>SS</sub>	60	V <sub>SS</sub>	112	V <sub>DD</sub>	164	DQ52
9	V <sub>SS</sub>	61	V <sub>SS</sub>	113	WE#	165	DQ49	10	DQ50#	62	DQS3#	114	S0#	166	DQ53
11	DM0	63	DM3	115	CAS#	167	V <sub>SS</sub>	12	DQ50	64	DQS3	116	ODT0	168	V <sub>SS</sub>
13	V <sub>SS</sub>	65	V <sub>SS</sub>	117	V <sub>DD</sub>	169	DQS6#	14	V <sub>SS</sub>	66	V <sub>SS</sub>	118	V <sub>DD</sub>	170	DM6
15	DQ2	67	DQ26	119	A13	171	DQS6	16	DQ6	68	DQ30	120	ODT1	172	V <sub>SS</sub>
17	DQ3	69	DQ27	121	S1#	173	V <sub>SS</sub>	18	DQ7	70	DQ31	122	NC	174	DQ54
19	V <sub>SS</sub>	71	V <sub>SS</sub>	123	V <sub>DD</sub>	175	DQ50	20	V <sub>SS</sub>	72	V <sub>SS</sub>	124	V <sub>DD</sub>	176	DQ55
21	DQ8	73	CKE0	125	NC	177	DQ51	22	DQ12	74	CKE1	126	V <sub>REFCA</sub>	178	V <sub>SS</sub>
23	DQ9	75	V <sub>DD</sub>	127	V <sub>SS</sub>	179	V <sub>SS</sub>	24	DQ13	76	V <sub>DD</sub>	128	V <sub>SS</sub>	180	DQ60
25	V <sub>SS</sub>	77	NC	129	DQ32	181	DQ56	26	V <sub>SS</sub>	78	NC/A15 <sup>1</sup>	130	DQ36	182	DQ61
27	DQS1#	79	BA2	131	DQ33	183	DQ57	28	DM1	80	NC/A14 <sup>2</sup>	132	DQ37	184	V <sub>SS</sub>
29	DQS1	81	V <sub>DD</sub>	133	V <sub>SS</sub>	185	V <sub>SS</sub>	30	RESET#	82	V <sub>DD</sub>	134	V <sub>SS</sub>	186	DQS7#
31	V <sub>SS</sub>	83	A12	135	DQS4#	187	DM7	32	V <sub>SS</sub>	84	A11	136	DM4	188	DQS7
33	DQ10	85	A9	137	DQS4	189	V <sub>SS</sub>	34	DQ14	86	A7	138	V <sub>SS</sub>	190	V <sub>SS</sub>
35	DQ11	87	V <sub>DD</sub>	139	V <sub>SS</sub>	191	DQ58	36	DQ15	88	V <sub>DD</sub>	140	DQ38	192	DQ62
37	V <sub>SS</sub>	89	A8	141	DQ34	193	DQ59	38	V <sub>SS</sub>	90	A6	142	DQ39	194	DQ63
39	DQ16	91	A5	143	DQ35	195	V <sub>SS</sub>	40	DQ20	92	A4	144	V <sub>SS</sub>	196	V <sub>SS</sub>
41	DQ17	93	V <sub>DD</sub>	145	V <sub>SS</sub>	197	SA0	42	DQ21	94	V <sub>DD</sub>	146	DQ44	198	NF
43	V <sub>SS</sub>	95	A3	147	DQ40	199	V <sub>DDSPD</sub>	44	V <sub>SS</sub>	96	A2	148	DQ45	200	SDA
45	DQS2#	97	A1	149	DQ41	201	SA1	46	DM2	98	A0	150	V <sub>SS</sub>	202	SCL
47	DQS2	99	V <sub>DD</sub>	151	V <sub>SS</sub>	203	V <sub>TT</sub>	48	V <sub>SS</sub>	100	V <sub>DD</sub>	152	DQS5#	204	V <sub>TT</sub>
49	V <sub>SS</sub>	101	CK0	153	DM5	-	-	50	DQ22	102	CK1	154	DQS5	-	-
51	DQ18	103	CK0#	155	V <sub>SS</sub>	-	-	52	DQ23	104	CK1#	156	V <sub>SS</sub>	-	-

- Notes: 1. Pin 78 is NC for 2GB and 4GB, A15 for 8GB.  
2. Pin 80 is NC for 2GB, A14 for 4GB and 8GB.

## Pin Descriptions

The pin description table below is a comprehensive list of all possible pins for all DDR3 modules. All pins listed may not be supported on this module. See Pin Assignments for information specific to this module.

**Table 7: Pin Descriptions**

Symbol	Type	Description
Ax	Input	<b>Address inputs:</b> Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BAx) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. See the Pin Assignments table for density-specific addressing information.
BAx	Input	<b>Bank address inputs:</b> Define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command.
CKx, CKx#	Input	<b>Clock:</b> Differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKEx	Input	<b>Clock enable:</b> Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
DMx	Input	<b>Data mask (x8 devices only):</b> DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. Although DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins.
ODTx	Input	<b>On-die termination:</b> Enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
Par_In	Input	<b>Parity input:</b> Parity bit for Ax, RAS#, CAS#, and WE#.
RAS#, CAS#, WE#	Input	<b>Command inputs:</b> RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input (LVCMOS)	<b>Reset:</b> RESET# is an active LOW asynchronous input that is connected to each DRAM and the registering clock driver. After RESET# goes HIGH, the DRAM must be reinitialized as though a normal power-up was executed.
Sx#	Input	<b>Chip select:</b> Enables (registered LOW) and disables (registered HIGH) the command decoder.
SAx	Input	<b>Serial address inputs:</b> Used to configure the temperature sensor/SPD EEPROM address range on the I <sup>2</sup> C bus.
SCL	Input	<b>Serial clock for temperature sensor/SPD EEPROM:</b> Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I <sup>2</sup> C bus.
CBx	I/O	<b>Check bits:</b> Used for system error detection and correction.
DQx	I/O	<b>Data input/output:</b> Bidirectional data bus.
DQSx, DQSx#	I/O	<b>Data strobe:</b> Differential data strobes. Output with read data; edge-aligned with read data; input with write data; center-aligned with write data.

Table 7: Pin Descriptions (Continued)

Symbol	Type	Description
SDA	I/O	<b>Serial data:</b> Used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM on the I <sup>2</sup> C bus.
TDQSx, TDQSx#	Output	<b>Redundant data strobe (x8 devices only):</b> TDQS is enabled/disabled via the LOAD MODE command to the extended mode register (EMR). When TDQS is enabled, DM is disabled and TDQS and TDQS# provide termination resistance; otherwise, TDQS# are no function.
Err_Out#	Output (open drain)	<b>Parity error output:</b> Parity error found on the command and address bus.
EVENT#	Output (open drain)	<b>Temperature event:</b> The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded.
V <sub>DD</sub>	Supply	<b>Power supply:</b> 1.35V (1.283–1.45V) backward-compatible to 1.5V (1.425–1.575V). The component V <sub>DD</sub> and V <sub>DDQ</sub> are connected to the module V <sub>DD</sub> .
V <sub>DDSPD</sub>	Supply	<b>Temperature sensor/SPD EEPROM power supply:</b> 3.0–3.6V.
V <sub>REFCA</sub>	Supply	<b>Reference voltage:</b> Control, command, and address V <sub>DD</sub> /2.
V <sub>REFDQ</sub>	Supply	<b>Reference voltage:</b> DQ, DM V <sub>DD</sub> /2.
V <sub>SS</sub>	Supply	Ground.
V <sub>TT</sub>	Supply	<b>Termination voltage:</b> Used for control, command, and address V <sub>DD</sub> /2.
NC	–	<b>No connect:</b> These pins are not connected on the module.
NF	–	<b>No function:</b> These pins are connected within the module, but provide no functionality.



## DQ Map

Table 8: Component-to-Module DQ Map (Front)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	2	15	U2	0	18	51
	1	5	6		1	21	42
	2	3	17		2	19	53
	3	0	5		3	16	39
	4	6	16		4	22	50
	5	4	4		5	20	40
	6	7	18		6	23	52
	7	1	7		7	17	41
U5	0	42	157	U6	0	58	191
	1	45	148		1	61	182
	2	43	159		2	59	193
	3	40	147		3	56	181
	4	46	158		4	62	192
	5	44	146		5	60	180
	6	47	160		6	63	194
	7	41	149		7	57	183
U7	0	13	24	U8	0	26	67
	1	10	33		1	29	58
	2	8	21		2	27	69
	3	11	35		3	24	57
	4	9	23		4	30	68
	5	15	36		5	28	56
	6	12	22		6	31	70
	7	14	34		7	25	59
U9	0	34	141	U10	0	53	166
	1	37	132		1	50	175
	2	35	143		2	48	163
	3	32	129		3	51	177
	4	38	140		4	49	165
	5	36	130		5	55	176
	6	39	142		6	52	164
	7	33	131		7	54	174

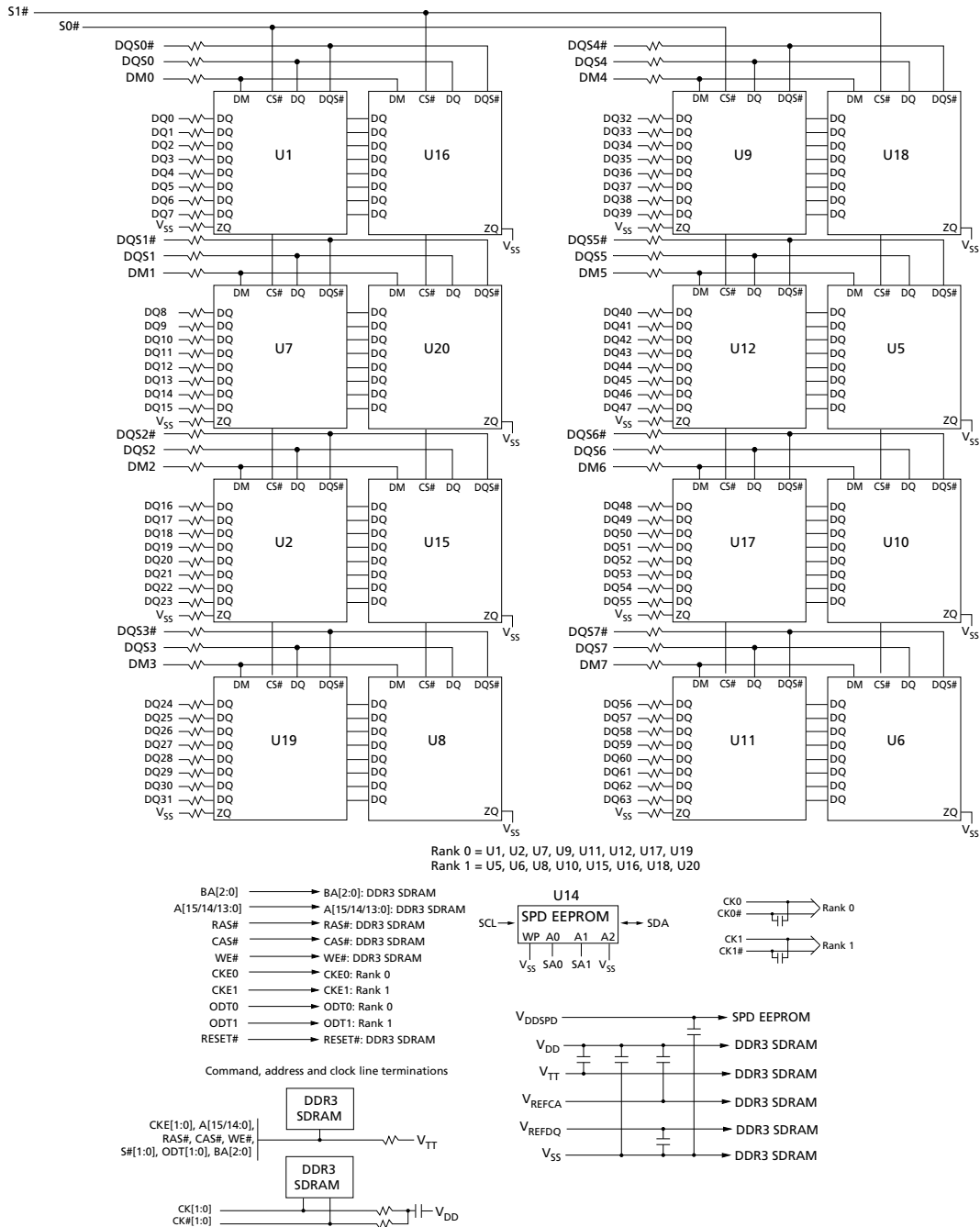


Table 9: Component-to-Module DQ Map (Back)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U11	0	61	182	U12	0	45	148
	1	58	191		1	42	157
	2	56	181		2	40	147
	3	59	193		3	43	159
	4	57	183		4	41	149
	5	63	194		5	47	160
	6	60	180		6	44	146
	7	62	192		7	46	158
U15	0	21	42	U16	0	5	6
	1	18	51		1	2	15
	2	16	39		2	0	5
	3	19	53		3	3	17
	4	17	41		4	1	7
	5	23	52		5	7	18
	6	20	40		6	4	4
	7	22	50		7	6	16
U17	0	50	175	U18	0	37	132
	1	53	166		1	34	141
	2	51	177		2	32	129
	3	48	163		3	35	143
	4	54	174		4	33	131
	5	52	164		5	39	142
	6	55	176		6	36	130
	7	49	165		7	38	140
U19	0	29	58	U20	0	10	33
	1	26	67		1	13	24
	2	24	57		2	11	35
	3	27	69		3	8	21
	4	25	59		4	14	34
	5	31	70		5	12	22
	6	28	56		6	15	36
	7	30	68		7	9	23

## Functional Block Diagram

**Figure 2: Functional Block Diagram**



Note: 1. The ZQ ball on each DDR3 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.



## General Description

DDR3 SDRAM modules are high-speed, CMOS dynamic random access memory modules that use internally configured 8-bank DDR3 SDRAM devices. DDR3 SDRAM modules use DDR architecture to achieve high-speed operation. DDR3 architecture is essentially an  $8n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM module effectively consists of a single  $8n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding  $n$ -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR3 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

## Fly-By Topology

DDR3 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR3.

## Serial Presence-Detect EEPROM Operation

DDR3 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to comply with JEDEC standard JC-45, "Appendix X: Serial Presence Detect (SPD) for DDR3 SDRAM Modules." These bytes identify module-specific timing parameters, configuration information, and physical attributes. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I<sup>2</sup>C bus using the DIMM's SCL (clock) SDA (data), and SA (address) pins. Write protect (WP) is connected to V<sub>SS</sub>, permanently disabling hardware write protection. For further information refer to Micron technical note TN-04-42, "Memory Module Serial Presence-Detect."



## Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

**Table 10: Absolute Maximum Ratings**

Symbol	Parameter	Min	Max	Units
$V_{DD}$	$V_{DD}$ supply voltage relative to $V_{SS}$	-0.4	1.975	V
$V_{IN}, V_{OUT}$	Voltage on any pin relative to $V_{SS}$	-0.4	1.975	V

**Table 11: Operating Conditions**

Symbol	Parameter	Min	Nom	Max	Units	Notes	
$V_{DD}$	$V_{DD}$ supply voltage	1.283	1.35	1.45	V		
		1.425	1.5	1.575	V	1	
$I_{VTT}$	Termination reference current from $V_{TT}$	-600	-	600	mA		
$V_{TT}$	Termination reference voltage (DC) – command/address bus	$0.49 \times V_{DD} - 20\text{mV}$	$0.5 \times V_{DD}$	$0.51 \times V_{DD} + 20\text{mV}$	V	2	
$I_I$	Input leakage current; Any input $0V \leq V_{IN} \leq V_{DD}$ ; $V_{REF}$ input $0V \leq V_{IN} \leq 0.95V$ (All other pins not under test = 0V)	Address inputs, RAS#, CAS#, WE#, BA	-32	0	32	$\mu\text{A}$	
		S#, CKE, ODT, CK, CK#	-16	0	16		
		DM	-4	0	4		
$I_{OZ}$	Output leakage current; $0V \leq V_{OUT} \leq V_{DD}$ ; DQ and ODT are disabled; ODT is HIGH	DQ, DQS, DQS#	-10	0	10	$\mu\text{A}$	
$I_{VREF}$	$V_{REF}$ supply leakage current; $V_{REFDQ} = V_{DD}/2$ or $V_{REFCA} = V_{DD}/2$ (All other pins not under test = 0V)	-16	0	16	$\mu\text{A}$		
$T_A$	Module ambient operating temperature	Commercial	0	-	70	$^{\circ}\text{C}$	3, 4
$T_C$	DDR3 SDRAM component case operating temperature	Commercial	0	-	95	$^{\circ}\text{C}$	3, 4, 5

- Notes:
1. Module is backward-compatible with 1.5V operation. Refer to device specification for details and operation guidance.
  2.  $V_{TT}$  termination voltage in excess of the stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.
  3.  $T_A$  and  $T_C$  are simultaneous requirements.
  4. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.
  5. The refresh rate is required to double when  $85^{\circ}\text{C} < T_C \leq 95^{\circ}\text{C}$ .



## DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR3 component data sheets. Component specifications are available on Micron's web site. Module speed grades correlate with component speed grades, as shown below.

**Table 12: Module and Component Speed Grades**

DDR3 components may exceed the listed module speed grades; module may not be available in all listed speed grades

Module Speed Grade	Component Speed Grade
-2G1	-093
-1G9	-107
-1G6	-125
-1G4	-15E
-1G1	-187E
-1G0	-187
-80C	-25E
-80B	-25

## Design Considerations

### Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

### Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

## I<sub>DD</sub> Specifications

**Table 13: DDR3 I<sub>DD</sub> Specifications and Conditions – 2GB (Die Revision G)**

Values are for the MT41K128M8 DDR3L SDRAM only and are computed from values specified in the 1Gb (128 Meg x 8) component data sheet

Parameter	Symbol	1600	1333	1066	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I <sub>DD0</sub> <sup>1</sup>	696	656	616	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I <sub>DD1</sub> <sup>1</sup>	816	776	736	mA
Precharge power-down current: Slow exit	I <sub>DD2P0</sub> <sup>2</sup>	192	192	192	mA
Precharge power-down current: Fast exit	I <sub>DD2P1</sub> <sup>2</sup>	560	480	400	mA
Precharge quiet standby current	I <sub>DD2Q</sub> <sup>2</sup>	720	720	640	mA
Precharge standby current	I <sub>DD2N</sub> <sup>2</sup>	720	720	640	mA
Precharge standby ODT current	I <sub>DD2NT</sub> <sup>1</sup>	636	496	496	mA
Active power-down current	I <sub>DD3P</sub> <sup>2</sup>	560	560	480	mA
Active standby current	I <sub>DD3N</sub> <sup>2</sup>	720	720	640	mA
Burst read operating current	I <sub>DD4R</sub> <sup>1</sup>	1256	1136	976	mA
Burst write operating current	I <sub>DD4W</sub> <sup>1</sup>	1296	1176	1016	mA
Refresh current	I <sub>DD5B</sub> <sup>1</sup>	1496	1456	1416	mA
Self refresh temperature current: MAX T <sub>C</sub> = 85°C	I <sub>DD6</sub> <sup>2</sup>	128	128	128	mA
Self refresh temperature current (SRT-enabled): MAX T <sub>C</sub> = 95°C	I <sub>DD6ET</sub> <sup>2</sup>	160	160	160	mA
All banks interleaved read current	I <sub>DD7</sub> <sup>1</sup>	2096	2056	1696	mA
Reset current	I <sub>DD8</sub> <sup>2</sup>	224	224	224	mA

- Notes: 1. One module rank in the active I<sub>DD</sub>; the other rank in I<sub>DD2P0</sub> (slow exit).  
2. All ranks in this I<sub>DD</sub> condition.



**Table 14: DDR3 I<sub>DD</sub> Specifications and Conditions – 4GB (Die Revision M)**

Values are for the MT41K256M8 DDR3L SDRAM only and are computed from values specified in the 2Gb (256 Meg x 8) component data sheet

Parameter	Symbol	1600	1333	1066	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I <sub>DD0</sub> <sup>1</sup>	576	536	496	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I <sub>DD1</sub> <sup>1</sup>	696	656	616	mA
Precharge power-down current: Slow exit	I <sub>DD2P0</sub> <sup>2</sup>	192	192	192	mA
Precharge power-down current: Fast exit	I <sub>DD2P1</sub> <sup>2</sup>	528	448	368	mA
Precharge quiet standby current	I <sub>DD2Q</sub> <sup>2</sup>	528	448	368	mA
Precharge standby current	I <sub>DD2N</sub> <sup>2</sup>	560	480	400	mA
Precharge standby ODT current	I <sub>DD2NT</sub> <sup>1</sup>	416	376	336	mA
Active power-down current	I <sub>DD3P</sub> <sup>2</sup>	752	672	592	mA
Active standby current	I <sub>DD3N</sub> <sup>2</sup>	832	752	672	mA
Burst read operating current	I <sub>DD4R</sub> <sup>1</sup>	1216	1096	976	mA
Burst write operating current	I <sub>DD4W</sub> <sup>1</sup>	1096	976	856	mA
Refresh current	I <sub>DD5B</sub> <sup>1</sup>	1616	1576	1536	mA
Self refresh temperature current: MAX T <sub>C</sub> = 85°C	I <sub>DD6</sub> <sup>2</sup>	192	192	192	mA
Self refresh temperature current (SRT-enabled): MAX T <sub>C</sub> = 95°C	I <sub>DD6ET</sub> <sup>2</sup>	240	240	240	mA
All banks interleaved read current	I <sub>DD7</sub> <sup>1</sup>	1856	1736	1616	mA
Reset current	I <sub>DD8</sub> <sup>2</sup>	224	224	224	mA

- Notes: 1. One module rank in the active I<sub>DD</sub>; the other rank in I<sub>DD2P0</sub> (slow exit).  
2. All ranks in this I<sub>DD</sub> condition.



**Table 15: DDR3 I<sub>DD</sub> Specifications and Conditions – 4GB (Die Revision K)**

Values are for the MT41K256M8 DDR3L SDRAM only and are computed from values specified in the 2Gb (256 Meg x 8) component data sheet

Parameter	Symbol	1866	1600	1333	1066	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I <sub>DD0</sub> <sup>1</sup>	416	408	400	384	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I <sub>DD1</sub> <sup>1</sup>	528	512	496	464	mA
Precharge power-down current: Slow exit	I <sub>DD2P0</sub> <sup>2</sup>	192	192	192	192	mA
Precharge power-down current: Fast exit	I <sub>DD2P1</sub> <sup>2</sup>	224	224	224	224	mA
Precharge quiet standby current	I <sub>DD2Q</sub> <sup>2</sup>	320	320	320	320	mA
Precharge standby current	I <sub>DD2N</sub> <sup>2</sup>	336	336	336	336	mA
Precharge standby ODT current	I <sub>DD2NT</sub> <sup>1</sup>	360	344	328	304	mA
Active power-down current	I <sub>DD3P</sub> <sup>2</sup>	336	336	336	336	mA
Active standby current	I <sub>DD3N</sub> <sup>2</sup>	544	512	480	448	mA
Burst read operating current	I <sub>DD4R</sub> <sup>1</sup>	928	848	752	640	mA
Burst write operating current	I <sub>DD4W</sub> <sup>1</sup>	960	872	776	680	mA
Refresh current	I <sub>DD5B</sub> <sup>1</sup>	1552	1536	1528	1512	mA
Self refresh temperature current: MAX T <sub>C</sub> = 85°C	I <sub>DD6</sub> <sup>2</sup>	192	192	192	192	mA
Self refresh temperature current (SRT-enabled): MAX T <sub>C</sub> = 95°C	I <sub>DD6ET</sub> <sup>2</sup>	240	240	240	240	mA
All banks interleaved read current	I <sub>DD7</sub> <sup>1</sup>	1408	1344	1296	1064	mA
Reset current	I <sub>DD8</sub> <sup>2</sup>	224	224	224	224	mA

- Notes: 1. One module rank in the active I<sub>DD</sub>; the other rank in I<sub>DD2P0</sub> (slow exit).  
2. All ranks in this I<sub>DD</sub> condition.



**Table 16: DDR3 I<sub>DD</sub> Specifications and Conditions – 8GB (Die Revision D)**

Values are for the MT41K512M8 DDR3L SDRAM only and are computed from values specified in the 4Gb (512 Meg x 8) component data sheet

Parameter	Symbol	1600	1333	1066	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I <sub>DD0</sub> <sup>1</sup>	760	680	640	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I <sub>DD1</sub> <sup>1</sup>	856	816	776	mA
Precharge power-down current: Slow exit	I <sub>DD2P0</sub> <sup>2</sup>	320	320	320	mA
Precharge power-down current: Fast exit	I <sub>DD2P1</sub> <sup>2</sup>	592	512	480	mA
Precharge quiet standby current	I <sub>DD2Q</sub> <sup>2</sup>	752	704	624	mA
Precharge standby current	I <sub>DD2N</sub> <sup>2</sup>	800	720	672	mA
Precharge standby ODT current	I <sub>DD2NT</sub> <sup>1</sup>	560	520	480	mA
Active power-down current	I <sub>DD3P</sub> <sup>2</sup>	1008	928	848	mA
Active standby current	I <sub>DD3N</sub> <sup>2</sup>	992	912	832	mA
Burst read operating current	I <sub>DD4R</sub> <sup>1</sup>	1656	1472	1336	mA
Burst write operating current	I <sub>DD4W</sub> <sup>1</sup>	1480	1320	1160	mA
Refresh current	I <sub>DD5B</sub> <sup>1</sup>	1920	1840	1800	mA
Self refresh temperature current: MAX T <sub>C</sub> = 85°C	I <sub>DD6</sub> <sup>2</sup>	352	352	352	mA
Self refresh temperature current (SRT-enabled): MAX T <sub>C</sub> = 95°C	I <sub>DD6ET</sub> <sup>2</sup>	448	448	448	mA
All banks interleaved read current	I <sub>DD7</sub> <sup>1</sup>	2480	2160	1840	mA
Reset current	I <sub>DD8</sub> <sup>2</sup>	352	352	352	mA

- Notes: 1. One module rank in the active I<sub>DD</sub>; the other rank in I<sub>DD2P0</sub> (slow exit).  
2. All ranks in this I<sub>DD</sub> condition.



**Table 17: DDR3 I<sub>DD</sub> Specifications and Conditions – 8GB (Die Revisions E and J)**

Values are for the MT41K512M8 DDR3L SDRAM only and are computed from values specified in the 4Gb (512 Meg x 8) component data sheet

Parameter	Symbol	1866	1600	1333	1066	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I <sub>DD0</sub> <sup>1</sup>	640	584	520	496	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I <sub>DD1</sub> <sup>1</sup>	704	672	640	616	mA
Precharge power-down current: Slow exit	I <sub>DD2P0</sub> <sup>2</sup>	288	288	288	288	mA
Precharge power-down current: Fast exit	I <sub>DD2P1</sub> <sup>2</sup>	592	512	448	426	mA
Precharge quiet standby current	I <sub>DD2Q</sub> <sup>2</sup>	560	512	448	432	mA
Precharge standby current	I <sub>DD2N</sub> <sup>2</sup>	560	512	464	448	mA
Precharge standby ODT current	I <sub>DD2NT</sub> <sup>1</sup>	480	456	424	400	mA
Active power-down current	I <sub>DD3P</sub> <sup>2</sup>	656	608	560	512	mA
Active standby current	I <sub>DD3N</sub> <sup>2</sup>	656	608	560	512	mA
Burst read operating current	I <sub>DD4R</sub> <sup>1</sup>	1536	1400	1264	1128	mA
Burst write operating current	I <sub>DD4W</sub> <sup>1</sup>	1272	1144	1024	904	mA
Refresh current	I <sub>DD5B</sub> <sup>1</sup>	2080	2024	1968	1936	mA
Self refresh temperature current: MAX T <sub>C</sub> = 85°C	I <sub>DD6</sub> <sup>2</sup>	320	320	320	320	mA
Self refresh temperature current (SRT-enabled): MAX T <sub>C</sub> = 95°C	I <sub>DD6ET</sub> <sup>2</sup>	400	400	400	400	mA
All banks interleaved read current	I <sub>DD7</sub> <sup>1</sup>	2152	1904	1664	1424	mA
Reset current	I <sub>DD8</sub> <sup>2</sup>	320	320	320	320	mA

- Notes: 1. One module rank in the active I<sub>DD</sub>; the other rank in I<sub>DD2P0</sub> (slow exit).  
2. All ranks in this I<sub>DD</sub> condition.





## Serial Presence-Detect EEPROM

For the latest SPD data, refer to Micron's SPD page: [www.micron.com/SPD](http://www.micron.com/SPD).

**Table 18: Serial Presence-Detect EEPROM DC Operating Conditions**

All voltages referenced to  $V_{DDSPD}$

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	$V_{DDSPD}$	3.0	3.6	V
Input low voltage: Logic 0; All inputs	$V_{IL}$	-0.45	$V_{DDSPD} \times 0.3$	V
Input high voltage: Logic 1; All inputs	$V_{IH}$	$V_{DDSPD} \times 0.7$	$V_{DDSPD} + 1.0$	V
Output low voltage: $I_{OUT} = 3\text{mA}$	$V_{OL}$	-	0.4	V
Input leakage current: $V_{IN} = \text{GND to } V_{DD}$	$I_{LI}$	0.1	2.0	$\mu\text{A}$
Output leakage current: $V_{OUT} = \text{GND to } V_{DD}$	$I_{LO}$	0.05	2.0	$\mu\text{A}$

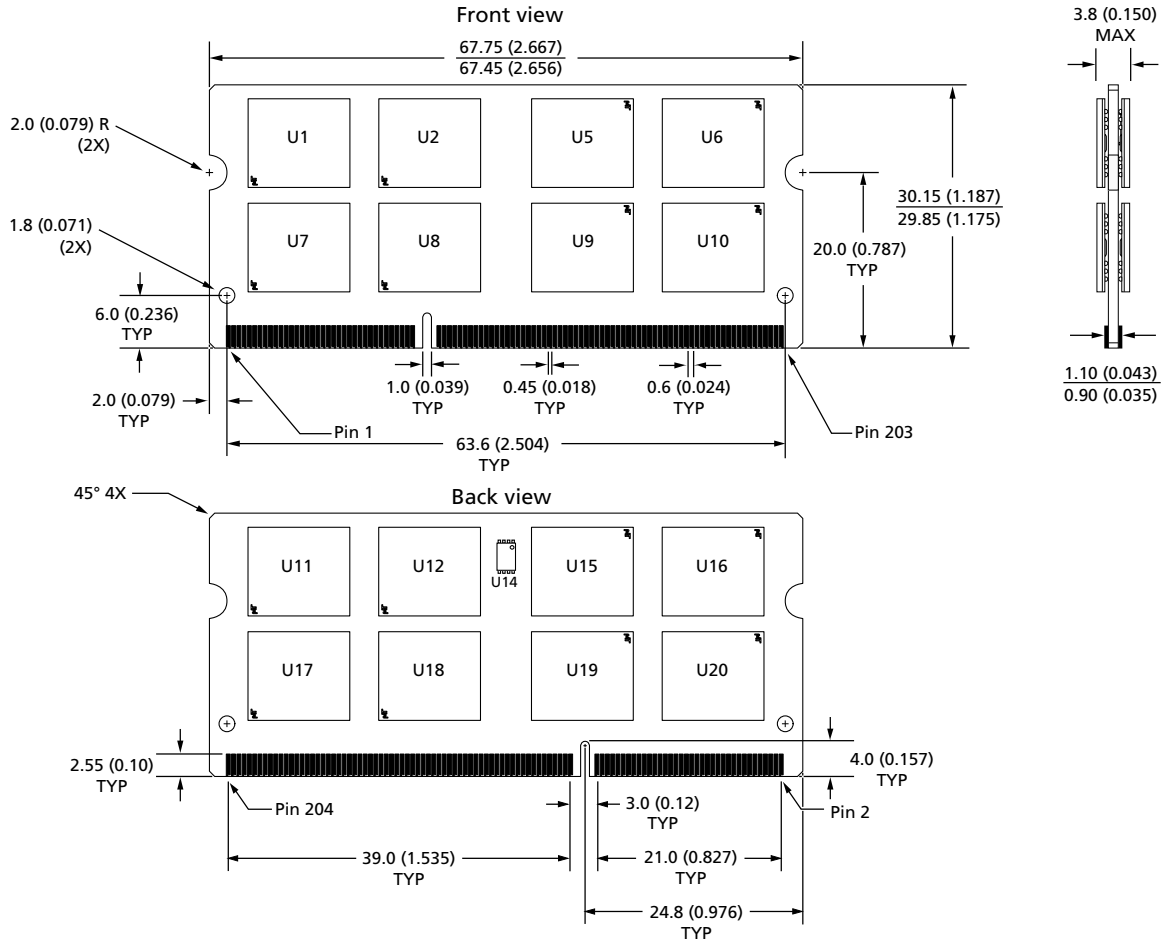
**Table 19: Serial Presence-Detect EEPROM AC Operating Conditions**

Parameter/Condition	Symbol	Min	Max	Units	Notes
Clock frequency	$t_{SCL}$	10	400	kHz	
Clock pulse width HIGH time	$t_{HIGH}$	0.6	-	$\mu\text{s}$	
Clock pulse width LOW time	$t_{LOW}$	1.3	-	$\mu\text{s}$	
SDA rise time	$t_R$	-	300	$\mu\text{s}$	1
SDA fall time	$t_F$	20	300	ns	1
Data-in setup time	$t_{SU:DAT}$	100	-	ns	
Data-in hold time	$t_{HD:DI}$	0	-	$\mu\text{s}$	
Data-out hold time	$t_{HD:DAT}$	200	900	ns	
Data out access time from SCL LOW	$t_{AA:DAT}$	0.2	0.9	$\mu\text{s}$	2
Start condition setup time	$t_{SU:STA}$	0.6	-	$\mu\text{s}$	3
Start condition hold time	$t_{HD:STA}$	0.6	-	$\mu\text{s}$	
Stop condition setup time	$t_{SU:STO}$	0.6	-	$\mu\text{s}$	
Time the bus must be free before a new transition can start	$t_{BUF}$	1.3	-	$\mu\text{s}$	
WRITE time	$t_W$	-	10	ms	

- Notes:
1. Guaranteed by design and characterization, not necessarily tested.
  2. To avoid spurious start and stop conditions, a minimum delay is placed between the falling edge of SCL and the falling or rising edge of SDA.
  3. For a restart condition, or following a WRITE cycle.

## Module Dimensions

**Figure 3: 204-Pin DDR3 SODIMM**



- Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.  
2. The dimensional diagram is for reference only.

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[25.320.4853.1](#) [25.320.5253.1](#) [25.325.3653.1](#) [25.326.3253.1](#) [25.326.3553.1](#) [25.330.1653.1](#) [25.330.4753.1](#) [25.330.5253.1](#) [25.334.3253.1](#)