Addendum Automotive DDR3L SDRAM

MT41K128M8 – 16 Meg x 8 x 8 banks
MT41K64M16 – 8 Meg x 16 x 8 banks

Description

This addendum provides information to add Automotive Ultra-high Temperature (AUT) option for the data sheet. This addendum does not provide detailed information about the device. Refer to the data sheet (1Gb: x8, x16 Automotive DDR3L SDRAM, Rev. B 2/15 EN) for a complete description of device functionality, operating modes, and specifications for the same Micron part number products. The 1.35V DDR3L SDRAM device is a low-voltage version of the 1.5V DDR3 SDRAM device. Refer to the DDR3 (1.5V) SDRAM data sheet specifications when running in 1.5V compatible mode.

Features

- $V_{DD} = V_{DDQ}$ = 1.35V (1.283V to 1.45V)
- Backward compatible to $V_{DD} = V_{DDQ}$ = 1.5V ±0.075V
- Differential bidirectional data strobe
- 8*n*-bit prefetch architecture
- Differential clock inputs (CK, CK#)
- 8 internal banks
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Programmable CAS (READ) latency (CL)
- Programmable CAS additive latency (AL)
- Programmable CAS (WRITE) latency (CWL)
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self refresh mode
- T_C of –40°C to 125°C
  - 64ms, 8192-cycle refresh at –40°C to 85°C
  - 32ms at 85°C to 105°C
  - 16ms at 105°C to 115°C
  - 8ms at 115°C to 125°C
- Self refresh temperature (SRT)
- Automatic self refresh (ASR)
- Write leveling
- Multipurpose register
- Output driver calibration
- AEC-Q100
- PPAP submission
- 8D response time

Options[1]	Marking
• Configuration	
– 128 Meg x 8	128M8
– 64 Meg x 16	64M16
• FBGA package (Pb-free) – x8	
– 78-ball FBGA (8mm x 10.5mm)	DA
• FBGA package (Pb-free) – x16	
– 96-ball FBGA (8mm x 14mm)	TW
• Timing – cycle time	
– 1.07ns @ CL = 13 (DDR3-1866)	-107
• Product certification	
– Automotive	A
• Operating temperature	
– Industrial (–40°C ≤ T_C ≤ +95°C)	IT
– Automotive (–40°C ≤ T_C ≤ +105°C)	AT
– Ultra-high (–40°C ≤ T_C ≤ +125°C)[3]	UT
• Revision	:J

Notes:
1. Not all options listed can be combined to define an offered product. Use the part catalog search on http://www.micron.com for available offerings.
2. The datasheet does not support ×4 mode even though ×4 mode description exists in the following sections.
3. The UT option use based on automotive usage model. Contact Micron sales representative for further information.

Table 1: Key Timing Parameters

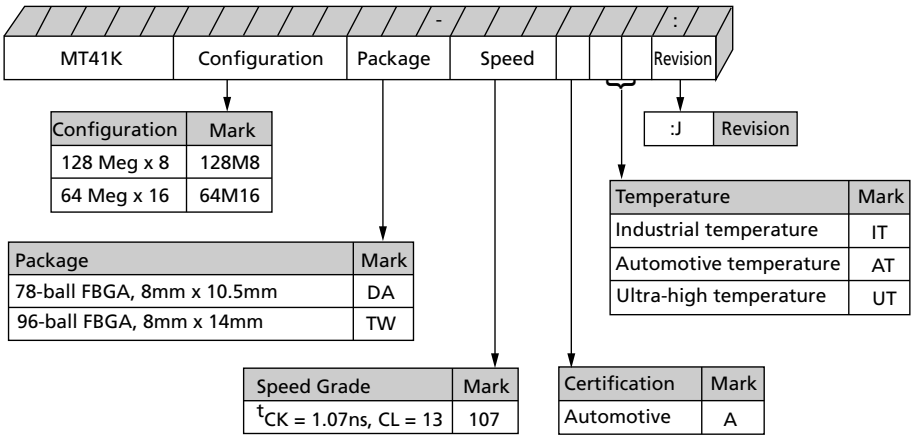
Speed Grade	Data Rate (MT/s)	Target ^{t}RCD-^{t}RP-CL	^{t}RCD (ns)	^{t}RP (ns)	CL (ns)
-107	1866	13-13-13	13.91	13.91	13.91

Table 2: Addressing

Parameter	128 Meg x 8	64 Meg x 16
Configuration	16 Meg x 8 x 8 banks	8 Meg x 16 x 8 banks
Refresh count	8K	8K
Row address	16K A[13:0]	8K A[12:0]
Bank address	8 BA[2:0]	8 BA[2:0]
Column address	1K A[9:0]	1K A[9:0]
Page Size	1KB	2KB

Figure 1: DDR3L Part Numbers

Example Part Number: MT41K64M16DA-107AAT:J



Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on http://www.micron.com for available offerings.

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Functional Description

DDR3 SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR3 SDRAM effectively consists of a single 8*n*-bit-wide, four-clock-

cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

The differential data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the DDR3 SDRAM input receiver. DQS is center-aligned with data for WRITEs. The read data is transmitted by the DDR3 SDRAM and edge-aligned to the data strobes.

The DDR3 SDRAM operates from a differential clock (CK and CK#). The crossing of CK going HIGH and CK# going LOW is referred to as the positive edge of CK. Control, command, and address signals are registered at every positive edge of CK. Input data is registered on the first rising edge of DQS after the WRITE preamble, and output data is referenced on the first rising edge of DQS after the READ preamble.

Read and write accesses to the DDR3 SDRAM are burst-oriented. Accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE commands are used to select the bank and the starting column location for the burst access.

The device uses a READ and WRITE BL8 and BC4. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard DDR SDRAM, the pipelined, multibank architecture of DDR3 SDRAM allows for concurrent operation, thereby providing high bandwidth by hiding row precharge and activation time.

A self refresh mode is provided, along with a power-saving, power-down mode.

Industrial Temperature

The industrial temperature (IT) device requires that the case temperature not exceed –40°C or 95°C. JEDEC specifications require the refresh rate to double when T_C exceeds 85°C; this also requires use of the high-temperature self refresh option. Additionally, ODT resistance and the input/output impedance must be derated when T_C is <0°C or >85°C.

Automotive Temperature

The automotive temperature (AT) device requires that the case temperature not exceed –40°C or 105°C. JEDEC specifications require the refresh rate to double when T_C exceeds 85°C; this also requires use of the high-temperature self refresh option. Additionally, ODT resistance and the input/output impedance must be derated when T_C is <0°C or >85°C.

Utra-high Temperature

The Utra-high temperature (UT) device requires that the case temperature not exceed –40°C or 125°C. JEDEC specifications require the refresh rate to double when T_C exceeds 85°C; this also requires use of the high-temperature auto refresh option. When T_C > +85°C, the refresh rate must be increased to 2X, when T_C > +105°C, the refresh rate must be increased to 4X and when T_C > +115°C, the refresh rate must be increased to 8X. Self-

refresh mode is not available for T_C > +105°C. Additionally, ODT resistance and the input/output impedance must be derated when T_C is <0°C or >85°C.

General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL enable mode of operation (normal operation).
- Throughout this data sheet, various figures and text refer to DQs as "DQ." DQ is to be interpreted as any and all DQ collectively, unless specifically stated otherwise.
- The terms "DQS" and "CK" found throughout this data sheet are to be interpreted as DQS, DQS# and CK, CK# respectively, unless specifically stated otherwise.
- Complete functionality may be described throughout the document; any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
- Any specific requirement takes precedence over a general statement.
- Any functionality not specifically stated is considered undefined, illegal, and not supported, and can result in unknown operation.
- Row addressing is denoted as A[*n*:0]. *For example,* 1Gb: *n* = 12 (x16); 1Gb: *n* = 13 (x4, x8); 2Gb: *n* = 13 (x16) and 2Gb: *n* = 14 (x4, x8); 4Gb: *n* = 14 (x16); and 4Gb: *n* = 15 (x4, x8).
- Dynamic ODT has a special use case: when DDR3 devices are architected for use in a single rank memory array, the ODT ball can be wired HIGH rather than routed. Refer to the Dynamic ODT Special Use Case section.
- A x16 device's DQ bus is comprised of two bytes. If only one of the bytes needs to be used, use the lower byte for data transfers and terminate the upper byte as noted:
  - Connect UDQS to ground via 1kΩ* resistor.
  - Connect UDQS# to V_{DD} via 1kΩ* resistor.
  - Connect UDM to V_{DD} via 1kΩ* resistor.
  - Connect DQ[15:8] individually to either V_{SS}, V_{DD}, or V_{REF} via 1kΩ resistors,* or float DQ[15:8].

  *If ODT is used, 1kΩ resistor should be changed to 4x that of the selected ODT.

Electrical Specifications

Absolute Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 3: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
V_{DD}	V_{DD} supply voltage relative to V_{SS}	–0.4	1.975	V	1
V_{DDQ}	V_{DD} supply voltage relative to V_{SSQ}	–0.4	1.975	V	
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.4	1.975	V	
T_C	Operating case temperature – Commercial	0	95	°C	2, 3
	Operating case temperature – Industrial	–40	95	°C	2, 3
	Operating case temperature – Automotive	–40	105	°C	2, 3
	Operating case temperature – Ultra-high	–40	125	°C	2, 3
T_{STG}	Storage temperature	–55	150	°C	

Notes:
1. V_{DD} and V_{DDQ} must be within 300mV of each other at all times, and V_{REF} must not be greater than 0.6 × V_{DDQ}. When V_{DD} and V_{DDQ} are <500mV, V_{REF} can be ≤300mV.
2. MAX operating case temperature. T_C is measured in the center of the package.
3. Device functionality is not guaranteed if the DRAM device exceeds the maximum T_C during operation.
4. Ultra-high temperature use based on automotive usage model. Please contact Micron sales representative if you have questions.

Input/Output Capacitance

Table 4: DDR3L Input/Output Capacitance

Note 1 applies to the entire table;

Capacitance Parameters	Symbol	DDR3L-1866		Unit	Notes
		Min	Max		
CK and CK#	C_{CK}	0.8	1.3	pF	
ΔC: CK to CK#	C_{DCK}	0.0	0.15	pF	
Single-end I/O: DQ, DM	C_{IO}	1.4	2.1	pF	2
Differential I/O: DQS, DQS#, TDQS, TDQS#	C_{IO}	1.4	2.1	pF	3
ΔC: DQS to DQS#, TDQS, TDQS#	C_{DDQS}	0.0	0.15	pF	3
ΔC: DQ to DQS	C_{DIO}	–0.5	0.3	pF	4
Inputs (CTRL, CMD, ADDR)	C_I	0.75	1.2	pF	5
ΔC: CTRL to CK	C_{DI_CTRL}	–0.4	0.2	pF	6
ΔC: CMD_ADDR to CK	$C_{DI\_CMD\_ADDR}$	–0.4	0.4	pF	7

Table 4: DDR3L Input/Output Capacitance (Continued)

Note 1 applies to the entire table;

Capacitance Parameters	Symbol	DDR3L-1866		Unit	Notes
		Min	Max		
ZQ pin capacitance	C_{ZQ}	–	3.0	pF	
Reset pin capacitance	C_{RE}	–	3.0	pF	

Notes:
1. V_{DD} = 1.35V (1.283–1.45V), V_{DDQ} = V_{DD}, V_{REF} = V_{SS}, *f* = 100 MHz, T_C = 25°C. $V_{OUT(DC)}$ = 0.5 × V_{DDQ}, V_{OUT} = 0.1V (peak-to-peak).
2. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
3. Includes TDQS, TDQS#. C_{DDQS} is for DQS vs. DQS# and TDQS vs. TDQS# separately.
4. C_{DIO} = $C_{IO(DQ)}$ - 0.5 × ($C_{IO(DQS)}$ + $C_{IO(DQS\#)}$).
5. Excludes CK, CK#; CTRL = ODT, CS#, and CKE; CMD = RAS#, CAS#, and WE#; ADDR = A[*n*:0], BA[2:0].
6. C_{DI_CTRL} = $C_{I(CTRL)}$ - 0.5 × ($C_{CK(CK)}$ + $C_{CK(CK\#)}$).
7. $C_{DI\_CMD\_ADDR}$ = $C_{I(CMD\_ADDR)}$ - 0.5 × ($C_{CK(CK)}$ + $C_{CK(CK\#)}$).

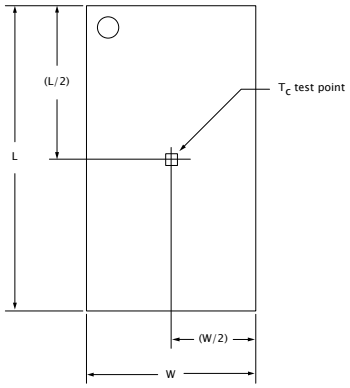
Thermal Characteristics

Table 5: Thermal Characteristics

Parameter/Condition		Value	Units	Symbol	Notes
Operating case temperature – Commercial		0 to +85	°C	T_C	1, 2, 3
Operating case temperature – Industrial		–40 to +95	°C	T_C	1, 2, 3, 4
Operating case temperature – Automotive		–40 to +105	°C	T_C	1, 2, 3, 4
Operating case temperature – Ultra-high		–40 to +125	°C	T_C	1, 2, 3, 4, 6
Junction-to-case (TOP)	78-ball "DA"	10.1	°C/W	ΘJC	5
	96-ball "TW"	9.4			

Notes:
1. MAX operating case temperature. T_C is measured in the center of the package.
2. A thermal solution must be designed to ensure the DRAM device does not exceed the maximum T_C during operation.
3. Device functionality is not guaranteed if the DRAM device exceeds the maximum T_C during operation.
4. If T_C exceeds 85°C, the DRAM must be refreshed externally at 2x refresh, which is a 3.9µs interval refresh rate. The use of SRT or ASR must be enabled.
5. The thermal resistance data is based off of a number of samples from multiple lots and should be viewed as a typical number.
6. Ultra-high temperature use based on automotive usage model. Please contact Micron sales representative if you have questions.

Figure 2: Thermal Measurement Point



Electrical Characteristics – I_{DD} Specifications

Table 6: I_{DD} Maximum Limits

Parameter	Symbol	Width	DDR3L -1866	Units	Notes
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I_{DD0}	x8	36	mA	1, 2
		x16	46	mA	1, 2
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}	x8	47	mA	1, 2
		x16	63	mA	1, 2
Precharge power-down current: Slow exit	I_{DD2P0} (slow)	All	12	mA	1, 2, 6
Precharge power-down current: Fast exit	I_{DD2P1} (fast)	All	12	mA	1, 2, 6
Precharge quiet standby	I_{DD2Q}	All	15	mA	1, 2, 6
Precharge standby current	I_{DD2N}	All	17	mA	1, 2, 6
Precharge standby ODT current	I_{DD2NT}	x8	27	mA	1, 2, 6
		x16	28	mA	1, 2, 6
Active power-down current	I_{DD3P}	All	14	mA	1, 2, 6
Active standby current	I_{DD3N}	x8	26	mA	1, 2, 6
		x16	28	mA	1, 2, 6
Burst read operating current	I_{DD4R}	x8	95	mA	1, 2
		x16	135	mA	1, 2
Burst write operating current	I_{DD4W}	x8	99	mA	1, 2
		x16	149	mA	1, 2
Burst refresh current	I_{DD5B}	All	165	mA	1, 2
Room temperature self refresh	I_{DD6}	All	12	mA	1, 2, 3, 7
Extended temperature self refresh	I_{DD6ET}	All	14	mA	1, 4, 7
All banks interleaved read current	I_{DD7}	x8	162	mA	1, 2
		x16	219	mA	1, 2
Reset current	I_{DD8}	All	14	mA	1, 2

Notes:
1. T_C = 85°C; SRT and ASR are disabled.
2. Enabling ASR could increase $I_{DD}x$ by up to an additional 2mA.
3. Restricted to T_C (MAX) = 85°C.
4. T_C = 85°C; ASR and ODT are disabled; SRT is enabled.
5. The I_{DD} values must be derated (increased) on IT-option and AT-option devices when operated outside of the range 0°C ≤ T_C ≤ +85°C:

   5a. When T_C < 0°C: I_{DD2P0}, I_{DD2P1} and I_{DD3P} must be derated by 4%; I_{DD4R} and I_{DD4W} must be derated by 2%; and I_{DD6} and I_{DD7} must be derated by 7%.

   5b. When T_C > 85°C: I_{DD0}, I_{DD1}, I_{DD2N}, I_{DD2NT}, I_{DD2Q}, I_{DD3N}, I_{DD3P}, I_{DD4R}, I_{DD4W}, and I_{DD5B} must be derated by 2%; I_{DD2Px} must be derated by 30%.
6. The I_{DD} values must be derated (increased) on UT-option. When T_C > +105°C: I_{DD2p0}, I_{DD2p1}, I_{DD2N}, I_{DD2NT}, I_{DD2Q}, I_{DD3P}, and I_{DD3N} must be derated by 60% from the 85°C specs.
7. When T_C >105°C, self refresh mode is not available.

Electrical Characteristics and AC Operating Conditions

Table 7: Electrical Characteristics and AC Operating Conditions for Speed Extensions

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3L-1866		Unit	Notes
			Min	Max		
Clock Timing						
Clock period average: DLL disable mode	–40°C ≤ T_C ≤ 85°C	^{t}CK (DLL_DIS)	8	7800	ns	9, 42
	85°C < T_C ≤ 95°C		8	3900	ns	42
	95°C < T_C ≤ 105°C		8	3900	ns	42
	105°C < T_C ≤ 125°C		8	3900	ns	42
Clock period average: DLL enable mode		^{t}CK (AVG)	See Speed Bin Tables for ^{t}CK range allowed		ns	10, 11
High pulse width average		^{t}CH (AVG)	0.47	0.53	CK	12
Low pulse width average		^{t}CL (AVG)	0.47	0.53	CK	12
Clock period jitter	DLL locked	^{t}JITper	–60	60	ps	13
	DLL locking	^{t}JITper,lck	–50	50	ps	13
Clock absolute period		^{t}CK (ABS)	MIN = ^{t}CK (AVG) MIN +^{t}JITper MIN; MAX = ^{t}CK (AVG) MAX + ^{t}JITper MAX		ps	
Clock absolute high pulse width		^{t}CH (ABS)	0.43	–	^{t}CK (AVG)	14
Clock absolute low pulse width		^{t}CL (ABS)	0.43	–	^{t}CK (AVG)	15
Cycle-to-cycle jitter	DLL locked	^{t}JITcc	120		ps	16
	DLL locking	^{t}JITcc,lck	100		ps	16
Cumulative error across	2 cycles	^{t}ERR2per	–88	88	ps	17
	3 cycles	^{t}ERR3per	–105	105	ps	17
	4 cycles	^{t}ERR4per	–117	117	ps	17
	5 cycles	^{t}ERR5per	–126	126	ps	17
	6 cycles	^{t}ERR6per	–133	133	ps	17
	7 cycles	^{t}ERR7per	–139	139	ps	17
	8 cycles	^{t}ERR8per	–145	145	ps	17
	9 cycles	^{t}ERR9per	–150	150	ps	17
	10 cycles	^{t}ERR10per	–154	154	ps	17
	11 cycles	^{t}ERR11per	–158	158	ps	17
	12 cycles	^{t}ERR12per	–161	161	ps	17
	n = 13, 14 . . . 49, 50 cycles	^{t}ERR*n*per	^{t}ERR*n*per MIN = (1 + 0.68ln[*n*]) × ^{t}JITper MIN ^{t}ERR*n*per MAX = (1 + 0.68ln[*n*]) × ^{t}JITper MAX		ps	17
DQ Input Timing						

Table 7: Electrical Characteristics and AC Operating Conditions for Speed Extensions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3L-1866		Unit	Notes
			Min	Max		
Data setup time to DQS, DQS#	Base (specification) @ 2 V/ns	tDS (AC130)	70	–	ps	18, 19
	V_{REF} @ 2 V/ns		135	–	ps	19, 20
Data hold time from DQS, DQS#	Base (specification) @ 2 V/ns	tDH (DC90)	75	–	ps	18, 19
	V_{REF} @ 2 V/ns		110	–	ps	19, 20
Minimum data pulse width		tDIPW	320	–	ps	41
DQ Output Timing						
DQS, DQS# to DQ skew, per access		tDQSQ	–	85	ps	
DQ output hold time from DQS, DQS#		tQH	0.38	–	tCK (AVG)	21
DQ Low-Z time from CK, CK#		tLZDQ	–390	195	ps	22, 23
DQ High-Z time from CK, CK#		tHZDQ	–	195	ps	22, 23
DQ Strobe Input Timing						
DQS, DQS# rising to CK, CK# rising		tDQSS	–0.27	0.27	CK	25
DQS, DQS# differential input low pulse width		tDQSL	0.45	0.55	CK	
DQS, DQS# differential input high pulse width		tDQSH	0.45	0.55	CK	
DQS, DQS# falling setup to CK, CK# rising		tDSS	0.18	–	CK	25
DQS, DQS# falling hold from CK, CK# rising		tDSH	0.18	–	CK	25
DQS, DQS# differential WRITE preamble		tWPRE	0.9	–	CK	
DQS, DQS# differential WRITE postamble		tWPST	0.3	–	CK	
DQ Strobe Output Timing						
DQS, DQS# rising to/from rising CK, CK#		tDQSCK	–195	195	ps	23
DQS, DQS# rising to/from rising CK, CK# when DLL is disabled		tDQSCK (DLL_DIS)	1	10	ns	26
DQS, DQS# differential output high time		tQSH	0.40	–	CK	21
DQS, DQS# differential output low time		tQSL	0.40	–	CK	21
DQS, DQS# Low-Z time (RL - 1)		tLZDQS	–390	195	ps	22, 23
DQS, DQS# High-Z time (RL + BL/2)		tHZDQS	–	195	ps	22, 23
DQS, DQS# differential READ preamble		tRPRE	0.9	Note 24	CK	23, 24
DQS, DQS# differential READ postamble		tRPST	0.3	Note 27	CK	23, 27
Command and Address Timing						
DLL locking time		tDLLK	512	–	CK	28
CTRL, CMD, ADDR setup to CK,CK#	Base (specification)	tIS (AC135)	65	–	ps	29, 30, 44
	V_{REF} @ 1 V/ns		200	–	ps	20, 30
CTRL, CMD, ADDR setup to CK,CK#	Base (specification)	tIS (AC125)	150	–	ps	29, 30, 44
	V_{REF} @ 1 V/ns		275	–	ps	20, 30

Table 7: Electrical Characteristics and AC Operating Conditions for Speed Extensions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3L-1866		Unit	Notes
			Min	Max		
CTRL, CMD, ADDR hold from CK,CK#	Base (specification)	tIH (DC90)	110	–	ps	29, 30
	V_{REF} @ 1 V/ns		200	–	ps	20, 30
Minimum CTRL, CMD, ADDR pulse width		tIPW	535	–	ps	41
ACTIVATE to internal READ or WRITE delay		tRCD	See Speed Bin Tables for tRCD		ns	31
PRECHARGE command period		tRP	See Speed Bin Tables for tRP		ns	31
ACTIVATE-to-PRECHARGE command period		tRAS	See Speed Bin Tables for tRAS		ns	31, 32
ACTIVATE-to-ACTIVATE command period		tRC	See Speed Bin Tables for tRC		ns	31, 43
ACTIVATE-to-ACTIVATE minimum command period	1KB page size	tRRD	MIN = greater of 4CK or 5ns		CK	31
	2KB page size		MIN = greater of 4CK or 6ns		CK	31
Four ACTIVATE windows	1KB page size	tFAW	27	–	ns	31
	2KB page size		35	–	ns	31
Write recovery time		tWR	MIN = 15ns; MAX = N/A		ns	31, 32, 33
Delay from start of internal WRITE transaction to internal READ command		tWTR	MIN = greater of 4CK or 7.5ns; MAX = N/A		CK	31, 34
READ-to-PRECHARGE time		tRTP	MIN = greater of 4CK or 7.5ns; MAX = N/A		CK	31, 32
CAS#-to-CAS# command delay		tCCD	MIN = 4CK; MAX = N/A		CK	
Auto precharge write recovery + precharge time		tDAL	MIN = WR + tRP/tCK (AVG); MAX = N/A		CK	
MODE REGISTER SET command cycle time		tMRD	MIN = 4CK; MAX = N/A		CK	
MODE REGISTER SET command update delay		tMOD	MIN = greater of 12CK or 15ns; MAX = N/A		CK	
MULTIPURPOSE REGISTER READ burst end to mode register set for multipurpose register exit		tMPRR	MIN = 1CK; MAX = N/A		CK	
Calibration Timing						
ZQCL command: Long calibration time	POWER-UP and RESET operation	tZQinit	MAX = N/A MIN = MAX(512nCK, 640ns)		CK	
	Normal operation	tZQoper	MAX = N/A MIN = MAX(256nCK, 320ns)		CK	
ZQCS command: Short calibration time			MAX = N/A MIN = MAX(64nCK, 80ns) tZQCS		CK	
Initialization and Reset Timing						

Table 7: Electrical Characteristics and AC Operating Conditions for Speed Extensions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3L-1866 Min	DDR3L-1866 Max	Unit	Notes
Exit reset from CKE HIGH to a valid command		^{t}XPR	MIN = greater of 5CK or ^{t}RFC + 10ns; MAX = N/A		CK	
Begin power supply ramp to power supplies stable		^{t}VDDPR	MIN = N/A; MAX = 200		ms	
RESET# LOW to power supplies stable		^{t}RPS	MIN = 0; MAX = 200		ms	
RESET# LOW to I/O and R_{TT} High-Z		^{t}IOZ	MIN = N/A; MAX = 20		ns	35
Refresh Timing						
REFRESH-to-ACTIVATE or REFRESH command period		^{t}RFC – 1Gb	MIN = 110; MAX = 70,200		ns	
		^{t}RFC – 2Gb	MIN = 160; MAX = 70,200		ns	
		^{t}RFC – 4Gb	MIN = 260; MAX = 70,200		ns	
		^{t}RFC – 8Gb	MIN = 350; MAX = 70,200		ns	
Maximum refresh period	$T_C \leq 85°C$	–	64 (1X)		ms	36
	$T_C > 85°C$		32 (2X)		ms	36
	$T_C > 105°C$		16 (4X)		ms	36
	$T_C > 115°C$		8 (8X)		ms	36
Maximum average periodic refresh	$T_C \leq 85°C$	^{t}REFI	7.8 (64ms/8192)		µs	36
	$T_C > 85°C$		3.9 (32ms/8192)		µs	36
	$T_C > 105°C$		1.95 (16ms/8192)		µs	36
	$T_C > 115°C$		0.977 (8ms/8192)		µs	36
Self Refresh Timing[45]						
Exit self refresh to commands not requiring a locked DLL		^{t}XS	MIN = greater of 5CK or ^{t}RFC + 10ns; MAX = N/A		CK	
Exit self refresh to commands requiring a locked DLL		^{t}XSDLL	MIN = ^{t}DLLK (MIN); MAX = N/A		CK	28
Minimum CKE low pulse width for self refresh entry to self refresh exit timing		^{t}CKESR	MIN = ^{t}CKE (MIN) + CK; MAX = N/A		CK	
Valid clocks after self refresh entry or power-down entry		^{t}CKSRE	MIN = greater of 5CK or 10ns; MAX = N/A		CK	
Valid clocks before self refresh exit, power-down exit, or reset exit		^{t}CKSRX	MIN = greater of 5CK or 10ns; MAX = N/A		CK	
Power-Down Timing						
CKE MIN pulse width		^{t}CKE (MIN)	Greater of 3CK or 5ns		CK	
Command pass disable delay		^{t}CPDED	MIN = 2; MAX = N/A		CK	
Power-down entry to power-down exit timing		^{t}PD	MIN = ^{t}CKE (MIN); MAX = 9 × ^{t}REFI		CK	
Begin power-down period prior to CKE registered HIGH		^{t}ANPD	WL - 1CK		CK	

Table 7: Electrical Characteristics and AC Operating Conditions for Speed Extensions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3L-1866 Min	DDR3L-1866 Max	Unit	Notes
Power-down entry period: ODT either synchronous or asynchronous		PDE	Greater of tANPD or tRFC - REFRESH command to CKE LOW time		CK	
Power-down exit period: ODT either synchronous or asynchronous		PDX	tANPD + tXPDLL		CK	
Power-Down Entry Minimum Timing						
ACTIVATE command to power-down entry		tACTPDEN	MIN = 2		CK	
PRECHARGE/PRECHARGE ALL command to power-down entry		tPRPDEN	MIN = 2		CK	
REFRESH command to power-down entry		tREFPDEN	MIN = 2		CK	37
MRS command to power-down entry		tMRSPDEN	MIN = tMOD (MIN)		CK	
READ/READ with auto precharge command to power-down entry		tRDPDEN	MIN = RL + 4 + 1		CK	
WRITE command to power-down entry	BL8 (OTF, MRS) BC4OTF	tWRPDEN	MIN = WL + 4 + tWR/tCK (AVG)		CK	
	BC4MRS	tWRPDEN	MIN = WL + 2 + tWR/tCK (AVG)		CK	
WRITE with auto precharge command to power-down entry	BL8 (OTF, MRS) BC4OTF	tWRAPDEN	MIN = WL + 4 + WR + 1		CK	
	BC4MRS	tWRAPDEN	MIN = WL + 2 + WR + 1		CK	
Power-Down Exit Timing						
DLL on, any valid command, or DLL off to commands not requiring locked DLL		tXP	MIN = greater of 3CK or 6ns; MAX = N/A		CK	
Precharge power-down with DLL off to commands requiring a locked DLL		tXPDLL	MIN = greater of 10CK or 24ns; MAX = N/A		CK	28
ODT Timing						
R_{TT} synchronous turn-on delay		ODTL on	CWL + AL - 2CK		CK	38
R_{TT} synchronous turn-off delay		ODTL off	CWL + AL - 2CK		CK	40
R_{TT} turn-on from ODTL on reference		tAON	–195	195	ps	23, 38
R_{TT} turn-off from ODTL off reference		tAOF	0.3	0.7	CK	39, 40
Asynchronous R_{TT} turn-on delay (power-down with DLL off)		tAONPD	MIN = 2; MAX = 8.5		ns	38
Asynchronous R_{TT} turn-off delay (power-down with DLL off)		tAOFPD	MIN = 2; MAX = 8.5		ns	40
ODT HIGH time with WRITE command and BL8		ODTH8	MIN = 6; MAX = N/A		CK	
ODT HIGH time without WRITE command or with WRITE command and BC4		ODTH4	MIN = 4; MAX = N/A		CK	
Dynamic ODT Timing						

Table 7: Electrical Characteristics and AC Operating Conditions for Speed Extensions (Continued)

Notes 1–8 apply to the entire table

Parameter	Symbol	DDR3L-1866		Unit	Notes
		Min	Max		
$R_{TT,nom}$-to-$R_{TT(WR)}$ change skew	ODTLcnw	WL - 2CK		CK	
$R_{TT(WR)}$-to-$R_{TT,nom}$ change skew - BC4	ODTLcwn4	4CK + ODTLoff		CK	
$R_{TT(WR)}$-to-$R_{TT,nom}$ change skew - BL8	ODTLcwn8	6CK + ODTLoff		CK	
R_{TT} dynamic change skew	^{t}ADC	0.3	0.7	CK	39
Write Leveling Timing					
First DQS, DQS# rising edge	^{t}WLMRD	40	–	CK	
DQS, DQS# delay	^{t}WLDQSEN	25	–	CK	
Write leveling setup from rising CK, CK# crossing to rising DQS, DQS# crossing	^{t}WLS	140	–	ps	
Write leveling hold from rising DQS, DQS# crossing to rising CK, CK# crossing	^{t}WLH	140	–	ps	
Write leveling output delay	^{t}WLO	0	7.5	ns	
Write leveling output error	^{t}WLOE	0	2	ns	

Notes:
1. AC timing parameters are valid from specified T_C MIN to T_C MAX values.
2. All voltages are referenced to V_{SS}.
3. Output timings are only valid for R_{ON34} output buffer selection.
4. The unit ^{t}CK (AVG) represents the actual ^{t}CK (AVG) of the input clock under operation. The unit CK represents one clock cycle of the input clock, counting the actual clock edges.
5. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 900mV in the test environment, but input timing is still referenced to V_{REF} (except ^{t}IS, ^{t}IH, ^{t}DS, and ^{t}DH use the AC/DC trip points and CK, CK# and DQS, DQS# use their crossing points). The minimum slew rate for the input signals used to test the device is 1 V/ns for single-ended inputs (DQs are at 2V/ns for DDR3-1866 and DDR3-2133) and 2 V/ns for differential inputs in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$.
6. All timings that use time-based values (ns, µs, ms) should use ^{t}CK (AVG) to determine the correct number of clocks (Table 7 (page 10) uses CK or ^{t}CK [AVG] interchangeably). In the case of noninteger results, all minimum limits are to be rounded up to the nearest whole integer, and all maximum limits are to be rounded down to the nearest whole integer.
7. Strobe or DQSdiff refers to the DQS and DQS# differential crossing point when DQS is the rising edge. Clock or CK refers to the CK and CK# differential crossing point when CK is the rising edge.
8. This output load is used for all AC timing (except ODT reference timing) and slew rates. The actual test load may be different. The output signal voltage reference point is V_{DDQ}/2 for single-ended signals and the crossing point for differential signals (see Figure 25: Differential Output Signal in the data sheet).
9. When operating in DLL disable mode, Micron does not warrant compliance with normal mode timings or functionality.
10. The clock's ^{t}CK (AVG) is the average clock over any 200 consecutive clocks and ^{t}CK (AVG) MIN is the smallest clock rate allowed, with the exception of a deviation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.

11. Spread spectrum is not included in the jitter specification values. However, the input clock can accommodate spread-spectrum at a sweep rate in the range of 20–60 kHz with an additional 1% of ^{t}CK (AVG) as a long-term jitter component; however, the spread spectrum may not use a clock rate below ^{t}CK (AVG) MIN.
12. The clock's ^{t}CH (AVG) and ^{t}CL (AVG) are the average half clock period over any 200 consecutive clocks and is the smallest clock half period allowed, with the exception of a deviation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.
13. The period jitter (^{t}JITper) is the maximum deviation in the clock period from the average or nominal clock. It is allowed in either the positive or negative direction.
14. ^{t}CH (ABS) is the absolute instantaneous clock high pulse width as measured from one rising edge to the following falling edge.
15. ^{t}CL (ABS) is the absolute instantaneous clock low pulse width as measured from one falling edge to the following rising edge.
16. The cycle-to-cycle jitter ^{t}JITcc is the amount the clock period can deviate from one cycle to the next. It is important to keep cycle-to-cycle jitter at a minimum during the DLL locking time.
17. The cumulative jitter error ^{t}ERRnper, where *n* is the number of clocks between 2 and 50, is the amount of clock time allowed to accumulate consecutively away from the average clock over *n* number of clock cycles.
18. ^{t}DS (base) and ^{t}DH (base) values are for a single-ended 1 V/ns slew rate DQs (DQs are at 2V/ns for DDR3-1866 and DDR3-2133) and 2 V/ns slew rate differential DQS, DQS#; when DQ single-ended slew rate is 2V/ns, the DQS differential slew rate is 4V/ns.
19. These parameters are measured from a data signal (DM, DQ0, DQ1, and so forth) transition edge to its respective data strobe signal (DQS, DQS#) crossing.
20. The setup and hold times are listed converting the base specification values (to which derating tables apply) to V_{REF} when the slew rate is 1 V/ns (DQs are at 2V/ns for DDR3-1866 and DDR3-2133). These values, with a slew rate of 1 V/ns (DQs are at 2V/ns for DDR3-1866 and DDR3-2133), are for reference only.
21. When the device is operated with input clock jitter, this parameter needs to be derated by the actual ^{t}JITper (larger of ^{t}JITper (MIN) or ^{t}JITper (MAX) of the input clock (output deratings are relative to the SDRAM input clock).
22. Single-ended signal parameter.
23. The DRAM output timing is aligned to the nominal or average clock. Most output parameters must be derated by the actual jitter error when input clock jitter is present, even when within specification. This results in each parameter becoming larger. The following parameters are required to be derated by subtracting ^{t}ERR10per (MAX): ^{t}DQSCK (MIN), ^{t}LZDQS (MIN), ^{t}LZDQ (MIN), and ^{t}AON (MIN). The following parameters are required to be derated by subtracting ^{t}ERR10per (MIN): ^{t}DQSCK (MAX), ^{t}HZ (MAX), ^{t}LZDQS (MAX), ^{t}LZDQ (MAX), and ^{t}AON (MAX). The parameter ^{t}RPRE (MIN) is derated by subtracting ^{t}JITper (MAX), while ^{t}RPRE (MAX) is derated by subtracting ^{t}JITper (MIN).
24. The maximum preamble is bound by ^{t}LZDQS (MAX).
25. These parameters are measured from a data strobe signal (DQS, DQS#) crossing to its respective clock signal (CK, CK#) crossing. The specification values are not affected by the amount of clock jitter applied, as these are relative to the clock signal crossing. These parameters should be met whether clock jitter is present.
26. The ^{t}DQSCK (DLL_DIS) parameter begins CL + AL - 1 cycles after the READ command.
27. The maximum postamble is bound by ^{t}HZDQS (MAX).
28. Commands requiring a locked DLL are: READ (and RDAP) and synchronous ODT commands. In addition, after any change of latency ^{t}XPDLL, timing must be met.
29. ^{t}IS (base) and ^{t}IH (base) values are for a single-ended 1 V/ns control/command/address slew rate and 2 V/ns CK, CK# differential slew rate.

30. These parameters are measured from a command/address signal transition edge to its respective clock (CK, CK#) signal crossing. The specification values are not affected by the amount of clock jitter applied as the setup and hold times are relative to the clock signal crossing that latches the command/address. These parameters should be met whether clock jitter is present.
31. For these parameters, the DDR3 SDRAM device supports ^{t}nPARAM (nCK) = RU(^{t}PARAM [ns]/^{t}CK[AVG] [ns]), assuming all input clock jitter specifications are satisfied. For example, the device will support ^{t}nRP (nCK) = RU(^{t}RP/^{t}CK[AVG]) if all input clock jitter specifications are met. This means that for DDR3-800 6-6-6, of which ^{t}RP = 5ns, the device will support ^{t}nRP = RU(^{t}RP/^{t}CK[AVG]) = 6 as long as the input clock jitter specifications are met. That is, the PRECHARGE command at T0 and the ACTIVATE command at T0 + 6 are valid even if six clocks are less than 15ns due to input clock jitter.
32. During READs and WRITEs with auto precharge, the DDR3 SDRAM will hold off the internal PRECHARGE command until ^{t}RAS (MIN) has been satisfied.
33. When operating in DLL disable mode, the greater of 4CK or 15ns is satisfied for ^{t}WR.
34. The start of the write recovery time is defined as follows:
    - For BL8 (fixed by MRS or OTF): Rising clock edge four clock cycles after WL
    - For BC4 (OTF): Rising clock edge four clock cycles after WL
    - For BC4 (fixed by MRS): Rising clock edge two clock cycles after WL
35. RESET# should be LOW as soon as power starts to ramp to ensure the outputs are in High-Z. Until RESET# is LOW, the outputs are at risk of driving and could result in excessive current, depending on bus activity.
36. The refresh period is 64ms when T_C is less than or equal to 85°C. This equates to an average refresh rate of 7.8125µs. However, nine REFRESH commands should be asserted at least once every 70.3µs. When T_C is greater than 85°C, the refresh period is 32ms. When T_C is greater than 105°C, the refresh period is 16ms. When T_C is greater than 115°C, the refresh period is 8ms.
37. Although CKE is allowed to be registered LOW after a REFRESH command when ^{t}REFPDEN (MIN) is satisfied, there are cases where additional time such as ^{t}XPDLL (MIN) is required.
38. ODT turn-on time MIN is when the device leaves High-Z and ODT resistance begins to turn on. ODT turn-on time maximum is when the ODT resistance is fully on. The ODT reference load is shown in Figure 19: ODT Timing Reference Load in the data sheet. Designs that were created prior to JEDEC tightening the maximum limit from 9ns to 8.5ns will be allowed to have a 9ns maximum.
39. Half-clock output parameters must be derated by the actual ^{t}ERR10per and ^{t}JITdty when input clock jitter is present. This results in each parameter becoming larger. The parameters ^{t}ADC (MIN) and ^{t}AOF (MIN) are each required to be derated by subtracting both ^{t}ERR10per (MAX) and ^{t}JITdty (MAX). The parameters ^{t}ADC (MAX) and ^{t}AOF (MAX) are required to be derated by subtracting both ^{t}ERR10per (MAX) and ^{t}JITdty (MAX).
40. ODT turn-off time minimum is when the device starts to turn off ODT resistance. ODT turn-off time maximum is when the DRAM buffer is in High-Z. The ODT reference load is shown in Figure 19: ODT Timing Reference Load in the data sheet. This output load is used for ODT timings (Figure 26: Reference Output Load for AC Timing and Output Slew Rate in the data sheet).
41. Pulse width of a input signal is defined as the width between the first crossing of $V_{REF(DC)}$ and the consecutive crossing of $V_{REF(DC)}$.
42. Should the clock rate be larger than ^{t}RFC (MIN), an AUTO REFRESH command should have at least one NOP command between it and another AUTO REFRESH command. Additionally, if the clock rate is slower than 40ns (25 MHz), all REFRESH commands should be followed by a PRECHARGE ALL command.

43. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in a reduction of REFRESH characteristics or product lifetime.
44. When two $V_{IH(AC)}$ values (and two corresponding $V_{IL(AC)}$ values) are listed for a specific speed bin, the user may choose either value for the input AC level. Whichever value is used, the associated setup time for that AC level must also be used. Additionally, one $V_{IH(AC)}$ value may be used for address/command inputs and the other $V_{IH(AC)}$ value may be used for data inputs.

    For example, for DDR3-800, two input AC levels are defined: $V_{IH(AC175),min}$ and $V_{IH(AC150),min}$ (corresponding $V_{IL(AC175),min}$ and $V_{IL(AC150),min}$). For DDR3-800, the address/command inputs must use either $V_{IH(AC175),min}$ with $^{t}IS(AC175)$ of 200ps or $V_{IH(AC150),min}$ with $^{t}IS(AC150)$ of 350ps; independently, the data inputs must use either $V_{IH(AC175),min}$ with $^{t}DS(AC175)$ of 75ps or $V_{IH(AC150),min}$ with $^{t}DS(AC150)$ of 125ps.
45. Self refresh is not available when $T_C > 105°C$.

Extended Temperature Usage

Micron's DDR3 SDRAM support the optional extended case temperature (T_C) range of 0°C to 125°C. Thus, the SRT and ASR options must be used at a minimum.

The extended temperature range DRAM must be refreshed externally at 2x (double refresh) anytime the case temperature is above 85°C (and does not exceed 105°C), 4x anytime the case temperature is above 105°C (and does not exceed 115°C) and 8x anytime the case temperature is above 115°C (and does not exceed 125°C). However, self refresh mode requires either ASR or SRT to support the extended temperatures between 85°C and 105°C and is not supported for temperatures above 105°C.

Table 8: Self Refresh Temperature and Auto Self Refresh Description

Field	MR2 Bits	Description
Self Refresh Temperature (SRT)		
SRT	7	If ASR is disabled (MR2[6] = 0), SRT must be programmed to indicate T_{OPER} during self refresh: *MR2[7] = 0: Normal operating temperature range (–40°C to 85°C) *MR2[7] = 1: Extended operating temperature range (–40°C to 105°C) If ASR is enabled (MR2[7] = 1), SRT must be set to 0, even if the extended temperature range is supported *MR2[7] = 0: SRT is disabled
Auto Self Refresh (ASR)		
ASR	6	When ASR is enabled, the DRAM automatically provides SELF REFRESH power management functions, (refresh rate for all supported operating temperature values) * MR2[6] = 1: ASR is enabled (M7 must = 0) When ASR is not enabled, the SRT bit must be programmed to indicate T_{OPER} during SELF REFRESH operation * MR2[6] = 0: ASR is disabled; must use manual self refresh temperature (SRT)

Table 9: Self Refresh Mode Summary

MR2[6] (ASR)	MR2[7] (SRT)	SELF REFRESH Operation	Permitted Operating Temperature Range for Self Refresh Mode
0	0	Self refresh mode is supported in the normal temperature range	Normal (–40°C to 85°C)
0	1	Self refresh mode is supported in normal and extended temperature ranges; When SRT is enabled, it increases self refresh power consumption	Normal and extended (–40°C to 105°C)
1	0	Self refresh mode is supported in normal and extended temperature ranges; Self refresh power consumption may be temperature-dependent	Normal and extended (–40°C to 105°C)
1	1	Illegal	

Revision History

Rev. D – 5/18

- Added Important Notes and Warnings section for further clarification aligning to industry standards

Rev. C – 2/17

- Typo correction in Calibration Timing in Electrical Characteristics and AC Operating Conditions for Speed Extensions table

Rev. B – 4/16

- Updated refresh rate specification through the data sheet: 16ms at 105°C to 115°C, and 8ms at 115°C to 125°C
- Updated the description of Utra-high Temperature in Functional Description section
- Updated Electrical Characteristics and AC Operating Conditions for Speed Extensions table in Electrical Characteristics and AC Operating Conditions: Updated Refresh Timing and note
- Updated Self Refresh Temperature and Auto Self Refresh Description table and Self Refresh Mode Summary table in Extended Temperature Usage section

Rev. A – 9/15

- Initial release

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