GDDR5 SGRAM

MT51J256M32 – 16 Meg x 32 I/O x 16 banks, 32 Meg x 16 I/O x 16 banks

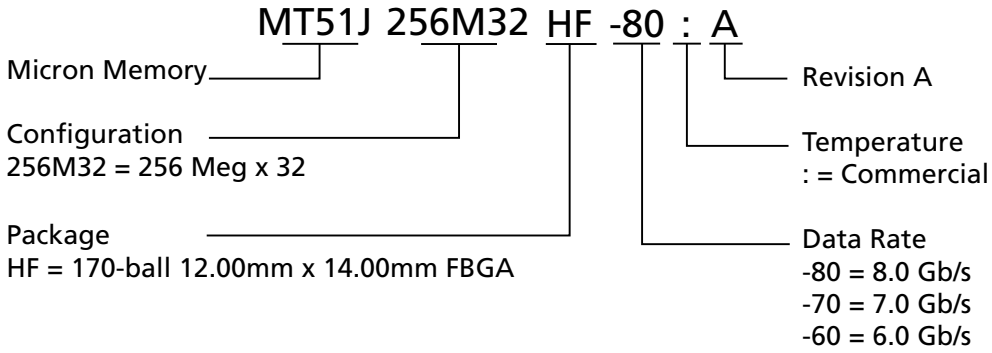
Features

- $V_{DD} = V_{DDQ}$ = 1.5V ±3% and 1.35V ±3%
- Data rate: 6.0 Gb/s, 7.0 Gb/s, 8.0 Gb/s
- 16 internal banks
- Four bank groups for ^{t}CCDL = 3 ^{t}CK
- 8*n*-bit prefetch architecture: 256-bit per array read or write access for x32; 128-bit for x16
- Burst length (BL): 8 only
- Programmable CAS latency: 7–24
- Programmable WRITE latency: 4–7
- Programmable CRC READ latency: 2–3
- Programmable CRC WRITE latency: 8–14
- Programmable EDC hold pattern for CDR
- Precharge: Auto option for each burst access
- Auto refresh and self refresh modes
- Refresh cycles: 16,384 cycles/32ms
- Interface: Pseudo open drain (POD-15) compatible outputs: 40Ω pull-down, 60Ω pull-up
- On-die termination (ODT): 60Ω or 120Ω (NOM)
- ODT and output driver strength auto calibration with external resistor ZQ pin: 120Ω
- Programmable termination and driver strength offsets
- Selectable external or internal V_{REF} for data inputs; programmable offsets for internal V_{REF}
- Separate external V_{REF} for address/command inputs
- x32/x16 mode configuration set at power-up with EDC pin
- Single-ended interface for data, address, and command
- Quarter data rate differential clock inputs CK_t, CK_c for address and commands
- Two half data rate differential clock inputs, WCK_t and WCK_c, each associated with two data bytes (DQ, DBI_n, EDC)
- DDR data (WCK) and addressing (CK)
- SDR command (CK)
- Write data mask function via address bus (single/double byte mask)
- Data bus inversion (DBI) and address bus inversion (ABI)
- Digital RAS lockout
- Address training: Address input monitoring via DQ pins
- WCK2CK clock training: Phase information via EDC pins
- Data read and write training via read FIFO (FIFO depth = 6)
- Read FIFO pattern preloaded by LDFF command
- Direct write data load to read FIFO by WRTR command
- Consecutive read of read FIFO by RDTR command
- Read/write data transmission integrity secured by cyclic redundancy check (CRC-8)
- Read/write EDC on/off mode
- Low power modes
- RDQS mode on EDC pin
- On-die temperature sensor with readout
- Automatic temperature sensor controlled self refresh rate
- Vendor ID, FIFO depth and density info fields for identification
- Mirror function with MF pin
- Boundary scan function with SEN pin
- Lead-free (RoHS-compliant) and halogen-free packaging
- T_C = 0°C to +95°C

Options[1]	Marking
• Organization	
– 256 Meg x 32 (words x bits)	256M32
• FBGA package	
– 170-ball (12mm x 14mm)	HF
• Timing – maximum data rate	
– 6.0 Gb/s, 5.0 Gb/s	-60
– 7.0 Gb/s, 6.0 Gb/s	-70
– 8.0 Gb/s, 6.0 Gb/s	-80
• Operating temperature	
– Commercial (0°C ≤ T_C ≤ +95°C)	None
• Revision	A

Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on http://www.micron.com for available offerings.

Figure 1: Part Numbering



Note: 1. This Micron GDDR5 SGRAM is available in different speed bins. The operating range and AC timings of a faster speed bin are a superset of all slower speed bins. Therefore it is safe to use a faster bin device as a drop-in replacement of a slower bin device when operated within the supply voltage and frequency range of the slower bin device.

FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA Part Marking Decoder on Micron's web site: http://www.micron.com.

Ball Assignments and Descriptions

Figure 2: 170-Ball FBGA – MF = 0 (Top View)

Note: 1. Balls shown with a heavy, solid outline are off in x16 mode.

Figure 3: 170-Ball FBGA – MF = 1 (Top View)

Note: 1. Balls shown with a heavy, solid outline are off in x16 mode.

Table 1: 170-Ball FBGA Ball Descriptions

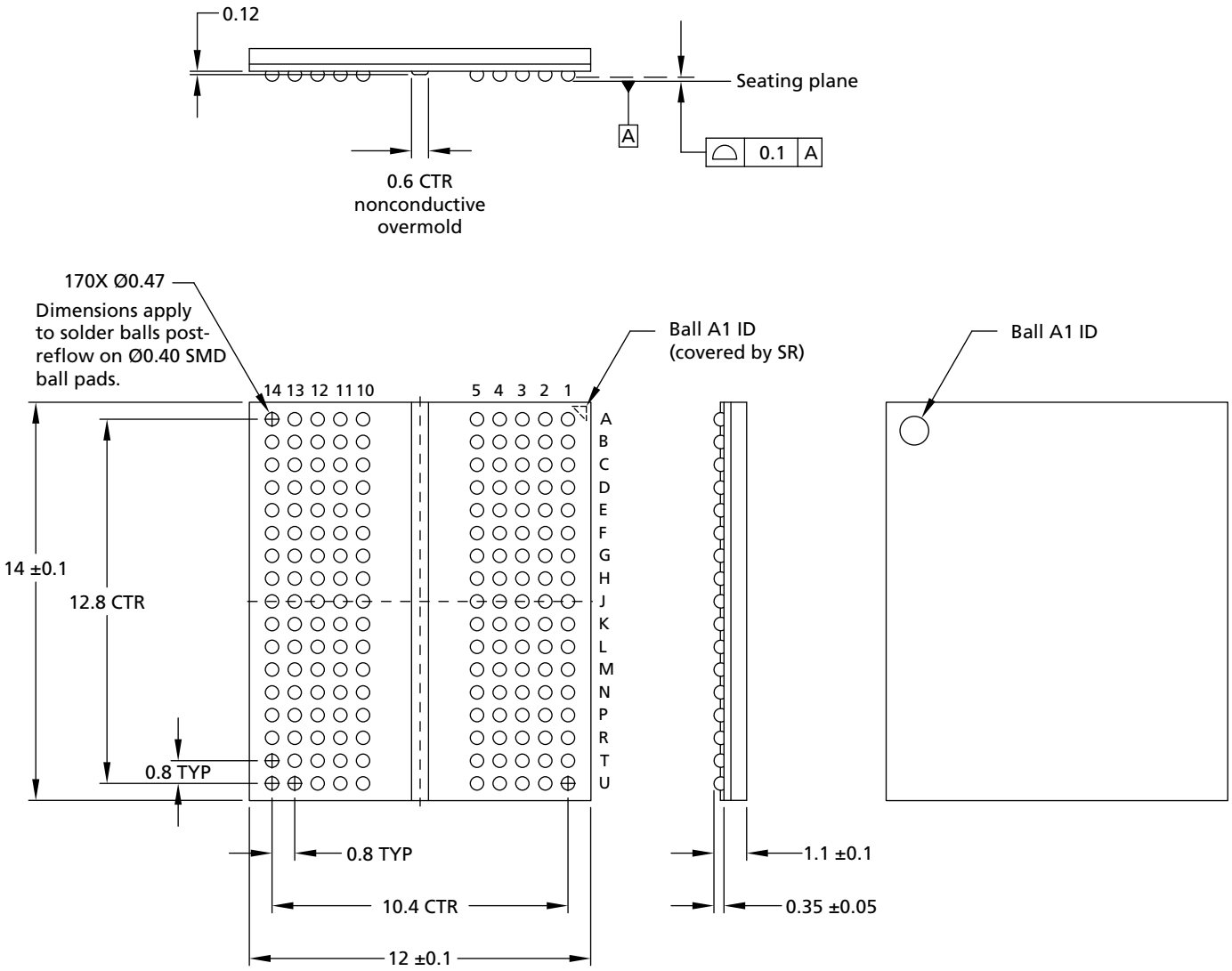
Symbol	Type	Description
A[13:0]	Input	**Address inputs:** Provide the row address for ACTIVE commands. A[6:0] (A7) provide the column address and A8 defines the auto precharge bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A8 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A8 LOW, bank selected by BA[3:0]) or all banks (A8 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command and the data bits during LDFF commands. A[12:8] are sampled with the rising edge of CK_t and A[7:0], A13 are sampled with the rising edge of CK_c.
ABI_n	Input	**Address bus inversion:** Reduces the power requirements on address pins by limiting the number of address lines driving LOW to 5. ABI_n is enabled by the corresponding ABI mode register bit.
BA[3:0]	Input	**Bank address inputs:** Define the bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA[3:0] define which mode register is loaded during the MODE REGISTER SET command. BA[3:0] are sampled with the rising edge of CK_t.
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. Command inputs are latched on the rising edge of CK_t. Address inputs are latched on the rising edge of CK_t and the rising edge of CK_c. All latencies are referenced to CK_t. CK_t and CK_c are externally terminated.
WCK01_t, WCK01_c/ WCK23_t, WCK23_c	Input	**Data Clocks:** WCK_t and WCK_c are differential clocks used for write data capture and read data output. WCK01_t and WCK01_c are associated with DQ[15:0], DBI0_n, DBI1_n, EDC0, and EDC1. WCK23_t and WCK23_c are associated with DQ[31:16], DBI2_n, DBI3_n, EDC2, and EDC3. WCK clocks operate at nominally twice the CK clock frequency.
CKE_n	Input	**Clock enable:** CKE_n enables (registered LOW) and disables (registered HIGH) internal circuitry and clocks on the device. The specific circuitry that is enabled/disabled is dependent upon the device configuration and operating mode. Taking CKE_n HIGH provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE_n is synchronous for power-down entry and exit and for self refresh entry. CKE_n must be maintained LOW throughout read and write accesses. Input buffers (excluding CKE_n) are disabled during SELF REFRESH operation. The value of CKE_n latched at power-up with RESET_n going HIGH determines the termination value of the address and command inputs.
CS_n	Input	**Chip select:** CS_n enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS_n is registered HIGH, but internal command execution continues. CS_n is considered part of the command code.
MF	Input	**Mirror function:** V_{DDQ} CMOS input. Must be tied to V_{DDQ} or V_{SS}.
RAS_n, CAS_n, WE_n	Input	**Command inputs:** RAS_n, CAS_n, and WE_n (along with CS_n) define the command being entered.
RESET_n	Input	**Reset:** RESET_n is an active LOW CMOS input referenced to V_{SS}. A full chip reset may be performed at any time by pulling RESET_n LOW. With RESET_n LOW all ODTs are disabled.
SEN	Input	**Scan enable:** V_{DDQ} CMOS input. Must be tied to V_{SS} when not in use.

Table 1: 170-Ball FBGA Ball Descriptions (Continued)

Symbol	Type	Description
DQ[31:0]	I/O	**Data input/output:** Bidirectional 32-bit data bus.
DBI[3:0]_n	I/O	**Data bus inversion:** Reduces the DC power consumption and supply noise induced jitter on data pins. DBI0_n is associated with DQ[7:0], DBI1_n with DQ[15:8], DBI2_n with DQ[23:16], and DBI3_n with DQ[31:24].
EDC[3:0]	Output	**Error detection code:** The calculated CRC data is transmitted on these pins. In addition, these pins drive a hold pattern when idle and can be used as an RDQS function. EDC0 is associated with DQ[7:0], EDC1 with DQ[15:8], EDC2 with DQ[23:16], and EDC3 with DQ[31:24].
V_{DD}	Supply	**Power supply:** 1.5V ±3% and 1.35V ±3%.
V_{DDQ}	Supply	**DQ power supply:** 1.5V ±3% and 1.35V ±3%. Isolated on the device for improved noise immunity.
V_{REFC}	Supply	**Reference voltage for control and address:** V_{REFC} must be maintained at all times (including self refresh) for proper device operation.
V_{REFD}	Supply	**Reference voltage for data:** V_{REFD} must be maintained at all times (including self refresh) for proper device operation.
V_{SS}	Supply	Ground.
V_{SSQ}	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
ZQ	Reference	**External reference ball for impedance calibration:** This ball is tied to an external 120Ω resistor (ZQ), which is tied to V_{SSQ}.
NC	–	**No connect:** These balls should be left unconnected (the ball has no connection to the device or to other balls).

Package Dimensions

Figure 4: 170-Ball FBGA (BG)



Notes:
1. All dimensions are in millimeters.
2. Solder ball material: SAC-Q (92.5% Sn, 4% Ag, 3% Bi, 0.5% Cu).

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