DDR4 SDRAM SODIMM Addendum

MTA16ATF4G64HZ – 32GB

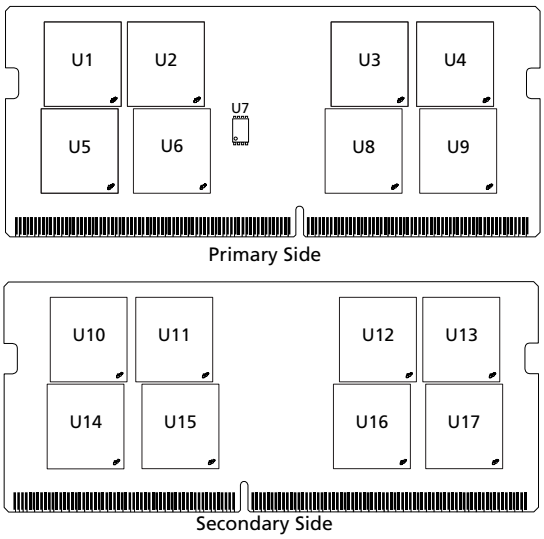
Introduction

Information provided here is in addition to or supersedes information provided in the Micron DDR4 SODIMM Core data sheet.

Features

- DDR4 functionality and operations supported as defined in the component data sheet
- Features and specifications supported in the Micron DDR4 SODIMM Core data sheet
- Fast data transfer rates: PC4-3200, PC4-2666
- 32GB (4 Gig x 64)
- Data bus inversion (DBI) for data bus
- Dual-rank
- 16 internal banks; 4 groups of 4 banks each

Figure 1: 260-Pin SODIMM



Options	Marking
• Operating temperature	
– Commercial ($0°C \leq T_{OPER} \leq 95°C$)	None
• Package	
– 260-pin DIMM (halogen-free)	Z
• Frequency/CAS latency	
– 0.625ns @ CL = 22 (DDR4-3200)	-3G2
– 0.75ns @ CL = 19 (DDR4-2666)	-2G6

Table 1: Addressing

Parameter	32GB
Row address	128K A[16:0]
Column address	1K A[9:0]
Device bank group address	4 BG[1:0]
Device bank address per group	4 BA[1:0]
Device configuration	16Gb (2 Gig x 8), 16 banks
Module rank address	2 CS_n[1:0]

Table 2: Part Numbers and Timing Parameters – 32GB Modules

Base device: MT40A2G8,[1] 16Gb DDR4 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles ($CL\text{-}_nRCD\text{-}_nRP$)
MTA16ATF4G64HZ-3G2__	32GB	4 Gig x 64	25.6 GB/s	0.625ns/3200 MT/s	22-22-22
MTA16ATF4G64HZ-2G6__	32GB	4 Gig x 64	21.3 GB/s	0.75ns/2666 MT/s	19-19-19

Notes:
1. The data sheet for the base device can be found on micron.com.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MTA16ATF4G64HZ-3G2E1.

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DQ Map

Table 3: Component-to-Module DQ Map, R/C-E1

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	11	42	U2	0	27	84
	1	8	28		1	25	71
	2	10	41		2	26	83
	3	9	29		3	24	70
	4	14	38		4	31	80
	5	12	24		5	29	67
	6	15	37		6	30	79
	7	13	25		7	28	66
U3	0	34	187	U4	0	51	229
	1	33	173		1	49	215
	2	35	186		2	50	228
	3	32	174		3	48	216
	4	39	182		4	55	225
	5	36	170		5	53	212
	6	38	183		6	54	224
	7	37	169		7	52	211
U5	0	2	20	U6	0	22	58
	1	0	8		1	20	46
	2	3	21		2	23	59
	3	1	7		3	21	45
	4	6	16		4	18	62
	5	4	4		5	16	50
	6	7	17		6	19	63
	7	5	3		7	17	49
U8	0	42	207	U9	0	59	250
	1	40	195		1	57	236
	2	43	208		2	58	249
	3	41	194		3	56	237
	4	46	203		4	63	246
	5	45	190		5	61	233
	6	47	204		6	62	245
	7	44	191		7	60	232

Table 3: Component-to-Module DQ Map, R/C-E1 (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U10	0	49	215	U11	0	33	173
	1	51	229		1	34	187
	2	48	216		2	32	174
	3	50	228		3	35	186
	4	53	212		4	36	170
	5	55	225		5	39	182
	6	52	211		6	37	169
	7	54	224		7	38	183
U12	0	25	71	U13	0	8	28
	1	27	84		1	11	42
	2	24	70		2	9	29
	3	26	83		3	10	41
	4	29	67		4	12	24
	5	31	80		5	14	38
	6	28	66		6	13	25
	7	30	79		7	15	37
U14	0	57	236	U15	0	40	195
	1	59	250		1	42	207
	2	56	237		2	41	194
	3	58	249		3	43	208
	4	61	233		4	45	190
	5	63	246		5	46	203
	6	60	232		6	44	191
	7	62	245		7	47	204
U16	0	20	46	U17	0	0	8
	1	22	58		1	2	20
	2	21	45		2	1	7
	3	23	59		3	3	21
	4	16	50		4	4	4
	5	18	62		5	6	16
	6	17	49		6	5	3
	7	19	63		7	7	17

I_{DD} Specifications

Table 4: DDR4 I_{DD} Specifications and Conditions (0° ≤ T_C ≤ 85°) – 32GB (Die Revision E)

Values are for the MT40A2G8 DDR4 SDRAM only and are computed from values specified in the 16Gb (2 Gig x 8) component data sheet

Parameter	Symbol	3200	2666	Units
One bank ACTIVATE-PRECHARGE current	I_{DD0}[1]	784	768	mA
One bank ACTIVATE-PRECHARGE, wordline boost, I_{PP} current	I_{PP0} [1]	40	40	mA
One bank ACTIVATE-READ-PRECHARGE current	I_{DD1}[1]	872	856	mA
Precharge standby current	I_{DD2N}[2]	720	688	mA
Precharge standby ODT current	I_{DD2NT}[1]	712	696	mA
Precharge power-down current	I_{DD2P}[2]	608	608	mA
Precharge quite standby current	I_{DD2Q}[2]	672	672	mA
Active standby current	I_{DD3N}[2]	976	944	mA
Active standby I_{PP} current	I_{PP3N}[2]	32	32	mA
Active power-down current	I_{DD3P}[2]	800	768	mA
Burst read current	I_{DD4R}[1]	1600	1472	mA
Burst write current	I_{DD4W}[1]	1328	1240	mA
Different logic rank burst refresh current (1x REF)	I_{DD5R}[1]	848	848	mA
Different logic rank burst refresh I_{PP} current (1x REF)	I_{PP5R}[1]	48	48	mA
Self refresh current: Normal temperature range (0°C to 85°C)	$I_{DD6N\ (0–85°C)}$[2]	848	848	mA
Self refresh current: Extended temperature range (0°C to 95°C)	$I_{DD6E\ (0–95°C)}$[2]	1808	1808	mA
Self refresh current: Reduced temperature range (0°C to 45°C)	$I_{DD6R\ (0–45°C)}$[2]	320	320	mA
Auto self refresh current (25°C)	$I_{DD6A\ (25°C)}$[2]	176	176	mA
Auto self refresh current (45°C)	$I_{DD6A\ (45°C)}$[2]	320	320	mA
Auto self refresh current (75°C)	$I_{DD6A\ (75°C)}$[2]	816	816	mA
Auto self refresh current (95°C)	$I_{DD6A\ (95°C)}$[2]	1808	1808	mA
Auto self refresh I_{PP} current (0°C to 95°C)	I_{PP6X}[2]	96	96	mA
Bank interleave read current	I_{DD7}[1]	1784	1752	mA
Bank interleave read I_{PP} current	I_{PP7}[1]	128	128	mA
Maximum power-down current	I_{DD8}[2]	576	576	mA

Notes:
1. One module rank in the active $I_{DD/PP}$, the other rank in $I_{DD2P/PP3N}$.
2. All ranks in this $I_{DD/PP}$ condition.
3. When T_C > 85°C, the I_{DD} and I_{PP} values must be derated. Refer to the base device data sheet I_{DD} and I_{PP} specification tables for derating values for the applicable die-revision.

Table 5: DDR4 I_{DD} Specifications and Conditions (0° ≤ T_C ≤ 85°) – 32GB (Die Revision B)

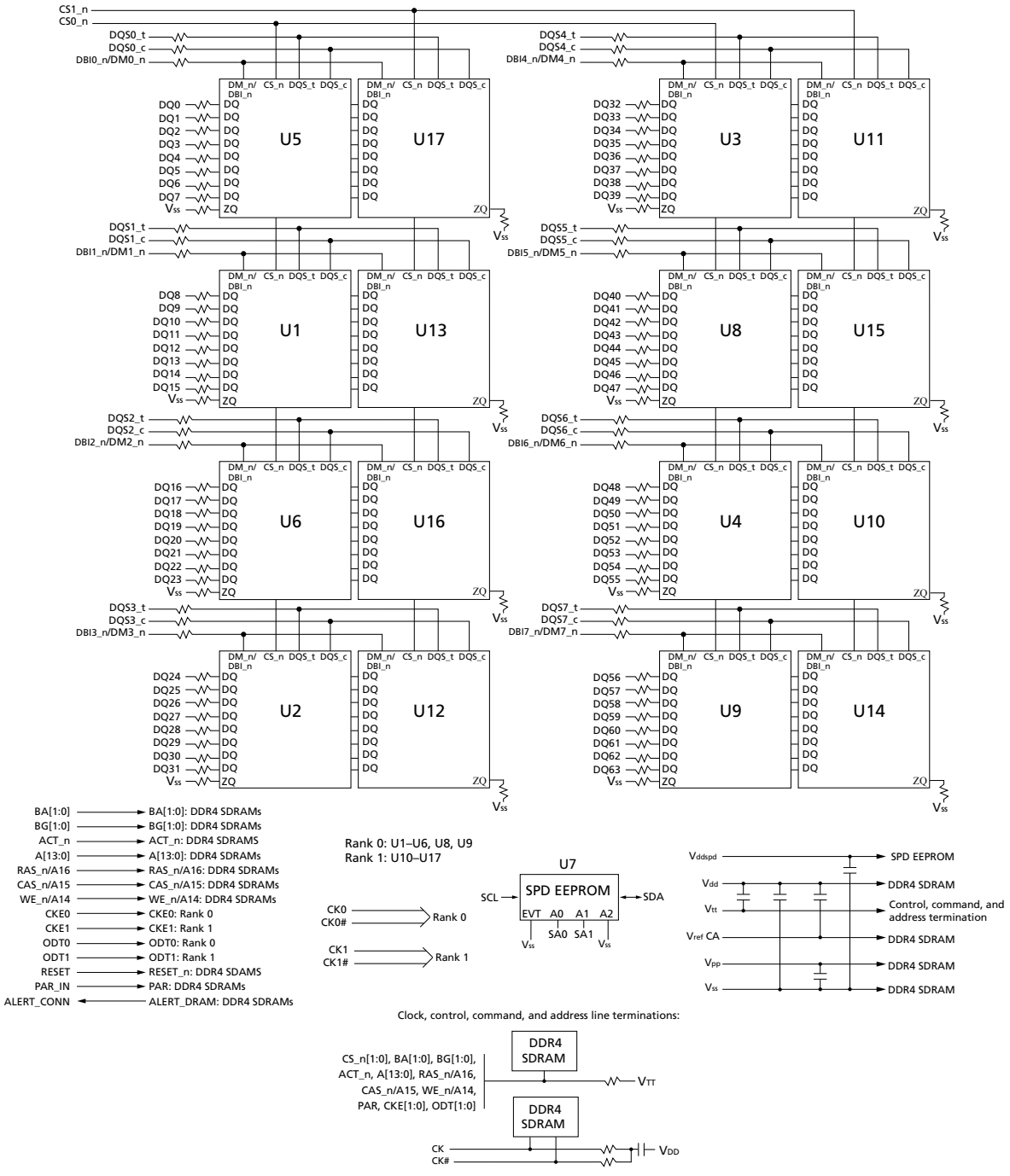
Values are for the MT40A2G8 DDR4 SDRAM only and are computed from values specified in the 16Gb (2 Gig x 8) component data sheet

Parameter	Symbol	3200	2666	Units
One bank ACTIVATE-PRECHARGE current	I_{DD0}[1]	848	832	mA
One bank ACTIVATE-PRECHARGE, wordline boost, I_{PP} current	I_{PP0} [1]	56	56	mA
One bank ACTIVATE-READ-PRECHARGE current	I_{DD1}[1]	936	920	mA
Precharge standby current	I_{DD2N}[2]	832	800	mA
Precharge standby ODT current	I_{DD2NT}[1]	792	776	mA
Precharge power-down current	I_{DD2P}[2]	688	688	mA
Precharge quite standby current	I_{DD2Q}[2]	752	752	mA
Active standby current	I_{DD3N}[2]	1280	1248	mA
Active standby I_{PP} current	I_{PP3N}[2]	48	48	mA
Active power-down current	I_{DD3P}[2]	1104	1088	mA
Burst read current	I_{DD4R}[1]	1960	1800	mA
Burst write current	I_{DD4W}[1]	1808	1672	mA
Different logic rank burst refresh current (1x REF)	I_{DD5R}[1]	976	960	mA
Different logic rank burst refresh I_{PP} current (1x REF)	I_{PP5R}[1]	64	64	mA
Self refresh current: Normal temperature range (0°C to 85°C)	$I_{DD6N\ (0–85°C)}$[2]	1072	1072	mA
Self refresh current: Extended temperature range (0°C to 95°C)	$I_{DD6E\ (0–95°C)}$[2]	1936	1936	mA
Self refresh current: Reduced temperature range (0°C to 45°C)	$I_{DD6R\ (0–45°C)}$[2]	464	464	mA
Auto self refresh current (25°C)	$I_{DD6A\ (25°C)}$[2]	160	160	mA
Auto self refresh current (45°C)	$I_{DD6A\ (45°C)}$[2]	464	464	mA
Auto self refresh current (75°C)	$I_{DD6A\ (75°C)}$[2]	976	976	mA
Auto self refresh current (95°C)	$I_{DD6A\ (95°C)}$[2]	1936	1936	mA
Auto self refresh I_{PP} current (0°C to 95°C)	I_{PP6X}[2]	176	176	mA
Bank interleave read current	I_{DD7}[1]	1912	1864	mA
Bank interleave read I_{PP} current	I_{PP7}[1]	104	104	mA
Maximum power-down current	I_{DD8}[2]	640	640	mA

Notes:
1. One module rank in the active $I_{DD/PP}$, the other rank in $I_{DD2P/PP3N}$.
2. All ranks in this $I_{DD/PP}$ condition.
3. When T_C > 85°C, the I_{DD} and I_{PP} values must be derated. Refer to the base device data sheet I_{DD} and I_{PP} specification tables for derating values for the applicable die-revision.

Functional Block Diagram

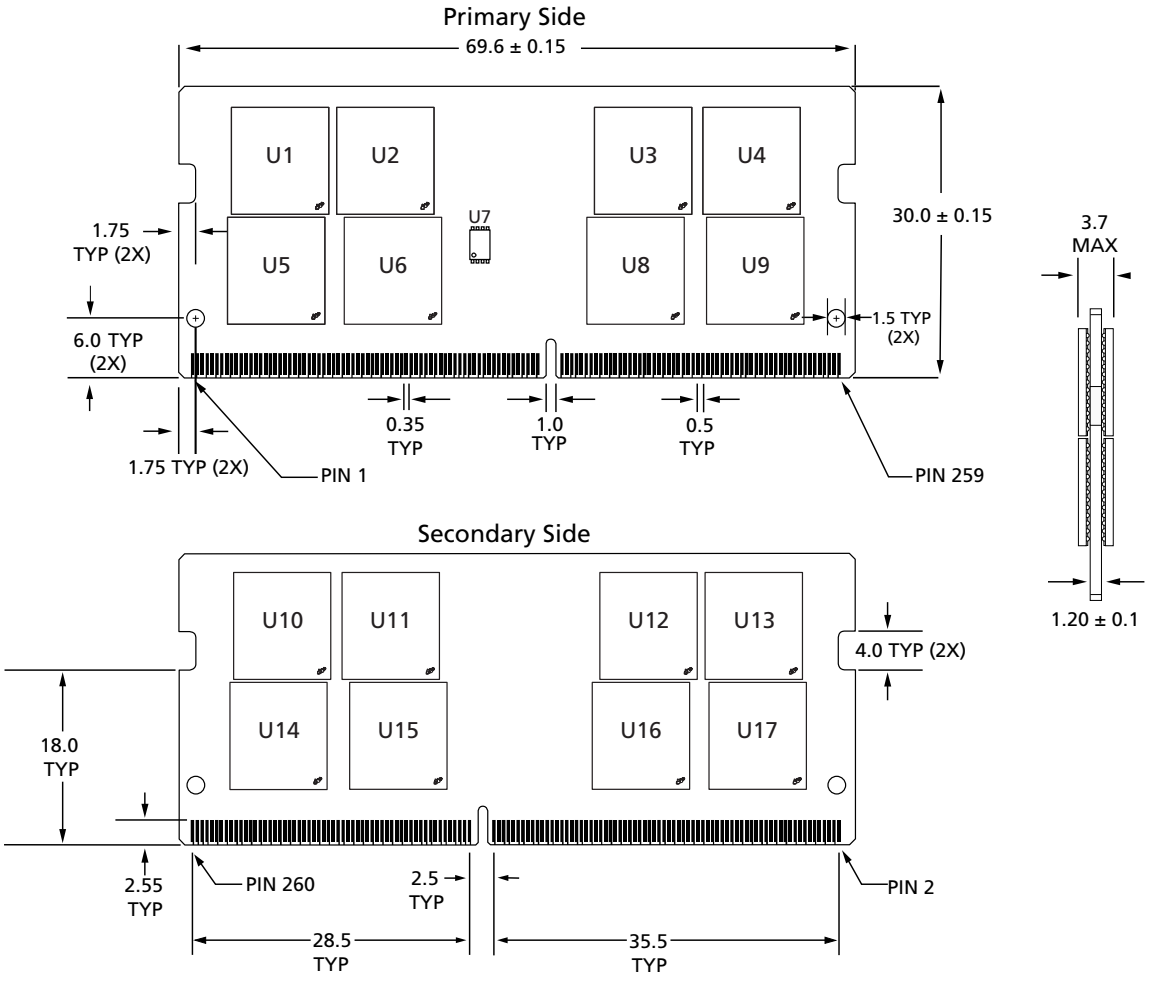
Figure 2: Functional Block Diagram, R/C-E1



Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

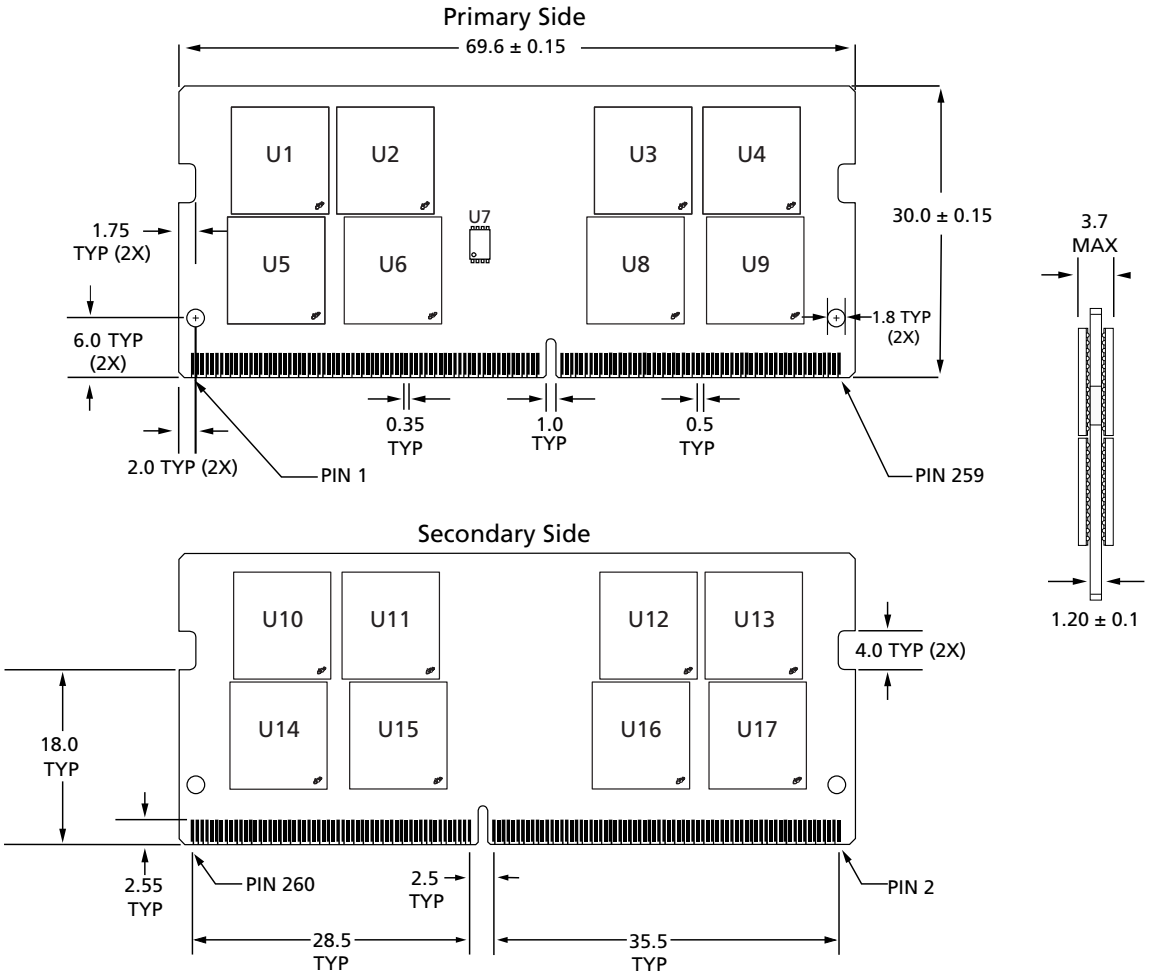
Module Dimensions

Figure 3: 260-Pin DDR4 SODIMM - PCB 2762, 2868 (R/C E1)



Notes:
1. All dimensions are in millimeters; MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.
3. Tooling hole dimensions on this PCB do not conform to the JEDEC MO-310 specification. All other dimensions conform to MO-310. Contact factory for further detail.

Figure 4: 260-Pin DDR4 SODIMM - PCB 3220 (R/C E1)



Notes:
1. All dimensions are in millimeters; MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only. Refer to JEDEC MO-310.

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