DDR4 SDRAM RDIMM

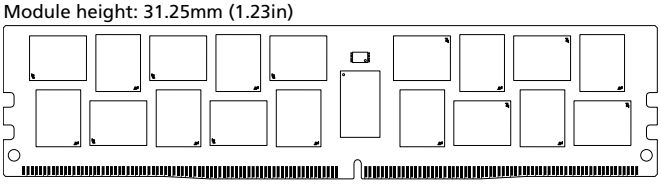
MTA36ASF2G72PZ – 16GB

Features

- DDR4 functionality and operations supported as defined in the component data sheet
- 284-pin, registered dual in-line memory module (RDIMM)
- Fast data transfer rates: PC4-2400, PC4-2133, or PC4-1866
- 16GB (2 Gig x 72)
- V_{DD} = 1.2V ±60mV
- V_{PP} = 2.5V ±125mV
- V_{DDSPD} = 3.0–3.6V
- Supports ECC error detection and correction
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Low-power auto self refresh (LPASR)
- Data bus inversion (DBI) for data bus
- On-die V_{REFDQ} generation and calibration
- Dual-rank
- On-board I^2C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- 16 internal banks; 4 groups of 4 banks each
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated control, command, and address bus

Figure 1: 284-Pin RDIMM (MO-309, R/C-B)

Module height: 31.25mm (1.23in)



Options	Marking
• Operating temperature	
– Commercial (0°C ≤ T_A ≤ +95°C)	None
• Package	
– 284-pin DIMM (halogen-free)	Z
• Frequency/CAS latency	
– 0.83ns @ CL = 16 (DDR4-2400)	-2G4
– 0.93ns @ CL = 15 (DDR4-2133)	-2G1
– 1.07ns @ CL = 13 (DDR4-1866)	-1G9

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)								^tRCD (ns)	^tRP (ns)	^tRC (ns)
		CL = 18	CL = 16	CL = 15	CL = 14	CL = 13	CL = 12	CL = 11	CL = 9			
-2G4	PC4-2400	2400	2133	2133	1866	1866	1600	1600	1333	13.32	13.32	45.32
-2G1	PC4-2133	–	2133	2133	1866	1866	1600	1600	1333	13.5	13.5	46.5
-1G9	PC4-1866	–	–	–	1866	1866	1600	1600	1333	13.5	13.5	47.5

Table 2: Addressing

Parameter	16GB
Row address	64K A[15:0]
Column address	1K A[9:0]
Device bank group address	4 BG[1:0]
Device bank address per group	4 BA[1:0]
Device configuration	4Gb (1 Gig x 4), 16 banks
Module rank address	2 CS_n[1:0]

Table 3: Part Numbers and Timing Parameters – 16GB Modules

Base device: MT40A1G4,[1] 4Gb DDR4 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MTA36ASF2G72PZ-2G4__	16GB	2 Gig x 72	19.2 GB/s	0.83ns/2400 MT/s	16-16-16
MTA36ASF2G72PZ-2G1__	16GB	2 Gig x 72	17.0 GB/s	0.93ns/2133 MT/s	15-15-15
MTA36ASF2G72PZ-1G9__	16GB	2 Gig x 72	14.9 GB/s	1.07ns/1866 MT/s	13-13-13

Notes:
1. The data sheet for the base device can be found on Micron's web site.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MTA36ASF2G72PZ-2G1A1.

Pin Assignments

Table 4: Pin Assignments

284-Pin DDR4 RDIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	37	DQ24	73	CK0_t	109	DQS14_t
2	DQ4	38	V_{SS}	74	CK0_c	110	DQS14_c
3	V_{SS}	39	DQS12_t	75	V_{DD}	111	V_{SS}
4	DQ0	40	DQS12-c	76	V_{TT}	112	DQ46
5	V_{SS}	41	V_{SS}	77	EVENT_n	113	V_{SS}
6	DQS9_t	42	DQ30	78	A0	114	DQ42
7	DQS09_c	43	V_{SS}	79	V_{DD}	115	V_{SS}
8	V_{SS}	44	DQ26	80	BA0	116	DQ52
9	DQ6	45	V_{SS}	81	RAS_n/ A16	117	V_{SS}
10	V_{SS}	46	CB4	82	V_{DD}	118	DQ48
11	DQ2	47	V_{SS}	83	S0_n	119	V_{SS}
12	V_{SS}	48	CB0	84	V_{DD}	120	DQS15_t
13	DQ12	49	DQS8	85	CAS_n/ A15	121	DQS15_c
14	V_{SS}	50	DQS17_t	86	ODT0	122	V_{SS}
15	DQ8	51	DQS17_c	87	V_{DD}	123	DQ54
16	V_{SS}	52	V_{SS}	88	S1_n	124	V_{SS}
17	DQS10_t	53	CB6	89	V_{DD}	125	DQ50
18	DQS10_c	54	V_{SS}	90	ODT1	126	V_{SS}
19	V_{SS}	55	CB2	91	V_{DD}	127	DQ60
20	DQ14	56	V_{SS}	92	NF	128	V_{SS}
21	V_{SS}	57	RESET_n	93	V_{SS}	129	DQ56
22	DQ10	58	V_{DD}	94	DQ36	130	V_{SS}
23	V_{SS}	59	CKE0	95	V_{SS}	131	DQS16_t
24	DQ20	60	V_{DD}	96	DQ32	132	DQS16_c
25	V_{SS}	61	ACT_n	97	V_{SS}	133	V_{SS}
26	DQ16	62	BG0	98	DQS13_t	134	DQ62
27	V_{SS}	63	V_{DD}	99	DQS13_c	135	V_{SS}
28	DQS11_t	64	A12	100	V_{SS}	136	DQ58
29	DQS11_c	65	A9	101	DQ38	137	V_{SS}
30	V_{SS}	66	V_{DD}	102	V_{ss}	138	SA0
31	DQ22	67	A8	103	DQ34	139	SA1
32	V_{SS}	68	A6	104	V_{SS}	140	SCL
33	DQ18	69	V_{DD}	105	DQ44	141	V_{PP}
34	V_{SS}	70	A3	106	V_{SS}	142	NF
35	DQ28	71	A1	107	DQ40		
36	V_{SS}	72	V_{DD}	108	V_{SS}		

284-Pin DDR4 RDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
143	V_{REFCA}	179	V_{SS}	215	CK1_t	251	V_{SS}
144	V_{SS}	180	DQ25	216	CK1_c	252	DQS5_c
145	DQ5	181	V_{SS}	217	V_{DD}	253	DQS5_t
146	V_{SS}	182	DQS3_c	218	V_{TT}	254	V_{SS}
147	DQ1	183	DQS3_t	219	PARITY	255	DQ47
148	V_{SS}	184	V_{SS}	220	V_{DD}	256	V_{SS}
149	DQS0_c	185	DQ31	221	BA1	257	DQ43
150	DQS0_t	186	V_{SS}	222	A10_AP	258	V_{SS}
151	V_{SS}	187	DQ27	223	V_{DD}	259	DQ53
152	DQ7	188	V_{SS}	224	NC	260	V_{SS}
153	V_{SS}	189	CB5	225	WE_n/ A14	261	DQ53
154	DQ3	190	V_{SS}	226	V_{DD}	262	V_{SS}
155	V_{SS}	191	CB1	227	NC	263	DQ49
156	DQ13	192	V_{SS}	228	V_{DD}	264	V_{SS}
157	V_{SS}	193	DQS8_c	229	A13	265	DQS6_c
158	DQ9	194	DQS8_t	230	V_{DD}	266	DQS6_t
159	V_{SS}	195	V_{SS}	231	A17	267	V_{SS}
160	DQS1_c	196	CB7	232	NF	268	DQ55
161	DQS1_t	197	V_{SS}	233	V_{DD}	269	V_{SS}
162	V_{SS}	198	CB3	234	NF	270	DQ51
163	DQ15	199	V_{SS}	235	SA2	271	V_{SS}
164	V_{SS}	200	CKE1	236	V_{SS}	272	DQ61
165	DQ11	201	V_{DD}	237	DQ37	273	V_{SS}
166	V_{SS}	202	NC	238	V_{SS}	274	DQS7_c
167	DQ21	203	V_{DD}	239	DQ33	275	DQS7_t
168	V_{SS}	204	BG1	240	V_{SS}	276	V_{SS}
169	DQ17	205	ALERT_n	241	DQS4_c	277	DQ63
170	V_{SS}	206	V_{DD}	242	DQS4_t	278	V_{SS}
171	DQS2_c	207	A11	243	V_{SS}	279	DQ59
172	DQS2_t	208	A7	244	DQ39	280	V_{SS}
173	V_{SS}	209	V_{DD}	245	V_{SS}	281	V_{DDSPD}
174	DQ23	210	A5	246	DQ35	282	SDA
175	V_{SS}	211	A4	247	V_{SS}	283	V_{PP}
176	DQ19	212	V_{DD}	248	DQ45	284	NF
177	V_{SS}	213	A2	249	V_{SS}		
178	DQ19	214	V_{DD}	250	DQ41		

Pin Descriptions

The pin description table below is a comprehensive list of all possible pins for all DDR4 modules. All pins listed may not be supported on this module. See Pin Assignments for information specific to this module.

Table 5: Pin Descriptions

Symbol	Type	Description
Ax	Input	**Address inputs:** Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, WE_n/A14, CAS_n/A15, and RAS_n/A16 have additional functions; see individual entries in this table). The address inputs also provide the op-code during the MODE REGISTER SET command.
A10/AP	Input	**Auto precharge:** A10 is sampled during READ and WRITE commands to determine whether auto precharge should be performed to the accessed bank after a READ or WRITE operation (HIGH = Auto precharge; LOW = No auto precharge). A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by the bank group and bank addresses.
A12/BC_n	Input	**Burst chop:** A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. (HIGH = No burst chop; LOW = Burst-chopped). See the Command Truth Table.
ACT_n	Input	**Command input:** ACT_n indicates an ACTIVATE command. When ACT_n (along with CS_n) is LOW, the input pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are treated as row address inputs for the ACTIVATE command. When ACT_n is HIGH (along with CS_n LOW), the input pins RAS_n/ A16, CAS_n/A15, and WE_n/A14 are treated as normal commands that use the RAS_n, CAS_n, and WE_n signals. See the Command Truth Table.
BAx	Input	**Bank address inputs:** Define the bank (within a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command.
BGx	Input	**Bank group address inputs:** Define the bank group to which a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command. BG[1:0] are used in the x4 and x8 configurations. BG1 is not used in the x16 configuration.
C0/CKE1 C1/CS1_n C2/ODT1	Input	**Stack address inputs:** These inputs are used only when devices are stacked, i.e., 2H, 4H, and 8H stacks for x4 and x8 configurations. These pins are not used in the x16 configuration. DDR4 supports a traditional DDP package, which uses these three signals to control the second die (CS1_n, CKE1, ODT1). DDR4 is not anticipated to support a traditional QDP package. For all other stack configurations, such as a 4H or 8H, it is assumed to be a single-load (master/slave)-type configuration where C0, C1, and C2 are used as chip ID selects in conjunction with a single CS_n, CKE, and ODT.
CK_t CK_c	Input	**Clock:** Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c.

Table 5: Pin Descriptions (Continued)

Symbol	Type	Description
CKEx	Input	**Clock enable:** CKE HIGH activates, and CKE LOW deactivates, the internal clock signals, device input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self refresh exit. After V_{REFCA} has become stable during the power-on and initialization sequence, it must be maintained during all operations (including SELF REFRESH). CKE must be held HIGH throughout read and write accesses. Input buffers (excluding CK_t, CK_c, ODT, RESET_n, and CKE) are disabled during power-down. Input buffers (excluding CKE and RESET#) are disabled during self refresh.
CS_n	Input	**Chip select:** All commands are masked when CS_n is registered HIGH. CS_n provides external rank selection on systems with multiple ranks. CS_n is considered part of the command code.
DM_n UDM_n LDM_n	Input	**Input data mask:** DM_n is an input mask signal for write data. Input data is masked when DM is sampled LOW coincident with that input data during a write access. DM is sampled on both edges of DQS. DM is not supported in x4 configurations. The UDM_n and LDM_n pins are used in the x16 configuration, UDM_n is associated with DQ[15:8]; LDM_n is associated with DQ[7:0]. The DM, DBI, and TDQS functions are enabled by mode register settings. See Data Mask (DM).
ODT	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When ODT is enabled, on-die termination (R_{TT}) is applied only to each DQ, DQS_t, DQS_c, DM_n/DBI_n/TDQS_t, and TDQS_c signal for x4, x8 configurations (when the TDQS function is enabled via mode register). For the x16 configuration, R_{TT} is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, UDM_n, and LDM_n signal. The ODT pin will be ignored if the mode registers are programmed to disable R_{TT}.
PAR	Input	**Parity for command and address:** This function can be enabled or disabled via the mode register. When enabled, the PARITY signal covers all command and address inputs, including RAS_n/A16, CAS_n/A15, WE_n/A14, A[17:0], A10/AP, A12/BC_n, BA[1:0], BG[1:0], C0/A18, C1/A19, and C2/A20. Control pins CS_n, CKE, and ODT are not covered by the PARITY signal. Unused address pins that are density- and configuration-specific should be treated internally as 0s by the DRAM parity logic.
RAS_n/A16 CAS_n/A15 WE_n/A14	Input	**Command inputs:** RAS_n/A16 , CAS_n/A15, and WE_n/A14 (along with CS_n and ACT_n) define the command and/or address being entered. See the ACT_n description in this table.
RESET_n	Input	**Active LOW asynchronous reset:** Reset is active when RESET_n is LOW; inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of V_{DD}, i.e., 960mV for DC HIGH; 240mV for DC LOW.
TEN	Input	**Connectivity test mode:** Active when TEN is HIGH; inactive when TEN is LOW. TEN must be LOW during normal operation. TEN is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of V_{DD} (960mV for DC HIGH; 240mV for DC LOW).
DQ	I/O	**Data input/output:** Bidirectional data bus. DQ represents DQ[3:0], DQ[7:0], and DQ[15:0] for the x4, x8, and x16 configurations, respectively. If CRC is enabled via the mode register, then CRC code is added at the end of the data burst. Either one or all of DQ0, DQ1, DQ2, or DQ3 is/are used for monitoring of internal V_{REF} level during test via mode register setting MR[4] A[4] = HIGH; training times change when enabled.

Table 5: Pin Descriptions (Continued)

Symbol	Type	Description
DBI_n UDBI_n LDBI_n	I/O	**DBI input/output:** Data bus inversion. DBI_n is an input/output signal used for data bus inversion in the x8 configuration. UDBI_n and LDBI_n are used in the x16 configuration; UDBI_n is associated with DQ[15:8], and LDBI_n is associated with DQ[7:0]. The DBI feature is not supported on x4 configurations. DBI can be configured for both READ (output) and WRITE (input) operations depending on the mode register settings. The DM, DBI, and TDQS functions are enabled by mode register settings. See data bus inversion (DBI).
DQS_t DQS_c DQSU_t DQSU_c DQSL_t DQSL_c	I/O	**Data strobe:** Output with READ data, input with WRITE data. Edge-aligned with READ data, centered-aligned with WRITE data. For x16 configurations, DQSL corresponds to the data on DQ[7:0]; DQSU corresponds to the data on DQ[15:8]. For the x4 and x8 configurations, DQS corresponds to the data on DQ[3:0] and DQ[7:0] respectively. DDR4 SDRAM support a differential data strobe only and do not support a single-ended data strobe.
ALERT_n	Output	**Alert output:** This signal allows the SDRAM to indicate to the system's memory controller that a specific alert or event has occurred. Alerts will include command/address parity errors and CRC data errors when either of those functions is enabled in the mode register.
TDQS_t TDQS_c	Output	**Termination data strobe:** TDQS_t and TDQS_c are applicable for x8 SDRAM only. When enabled via the mode register, the SDRAM enable the same R_{TT} termination resistance on TDQS_t and TDQS_c that is applied to DQS_t and DQS_c. When the TDQS function is disabled via the mode register, the DM/TDQS_t pin provides the data mask (DM) function, and the TDQS_c pin is not used. The TDQS function must be disabled in the mode register for both the x4 and x16 configurations. The DM function is supported only in x8 and x16 configurations.
V_{DD}	Supply	**Power supply:** 1.2V ±0.060V
V_{DDQ}	Supply	**DQ power supply:** 1.2V ±0.060V
V_{PP}	Supply	**DRAM activating power supply:** 2.5V -0.125V / +0.250V
V_{REFCA}	Supply	Reference voltage for control, command, and address pins.
V_{SS}	Supply	Ground.
V_{SSQ}	Supply	DQ ground.
ZQ	Reference	**Reference ball for ZQ calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to V_{SSQ}.
RFU	–	Reserved for future use.
NC	–	**No connect:** No internal electrical connection is present.
NF	–	**No function:** Internal connection may be present but has no function.

DQ Map

Table 6: Component-to-Module DQ Map Front

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	3	154	U11	0	3	154
	1	0	4		1	0	4
	2	2	11		2	2	11
	3	1	147		3	1	147
U2	0	14	20	U12	0	14	20
	1	13	156		1	13	156
	2	15	163		2	15	163
	3	12	13		3	12	13
U3	0	22	31	U13	0	22	31
	1	21	167		1	21	167
	2	23	174		2	23	174
	3	20	24		3	20	24
U4	0	30	42	U14	0	30	42
	1	28	35		1	28	35
	2	31	185		2	31	185
	3	29	178		3	29	178
U5	0	CB3	198	U15	0	CB3	198
	1	CB0	48		1	CB0	48
	2	CB2	55		2	CB2	55
	3	CB1	191		3	CB1	191
U7	0	38	101	U17	0	38	101
	1	37	237		1	37	237
	2	39	244		2	39	244
	3	36	94		3	36	94
U8	0	43	257	U18	0	43	257
	1	41	250		1	41	250
	2	42	114		2	42	114
	3	40	107		3	40	107
U9	0	55	266	U19	0	55	266
	1	52	116		1	52	116
	2	54	123		2	54	123
	3	53	259		3	53	259

Table 6: Component-to-Module DQ Map Front (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U10	0	62	134	U20	0	62	134
	1	60	127		1	60	127
	2	63	277		2	63	277
	3	61	270		3	61	270

Table 7: Component-to-Module DQ Map Back

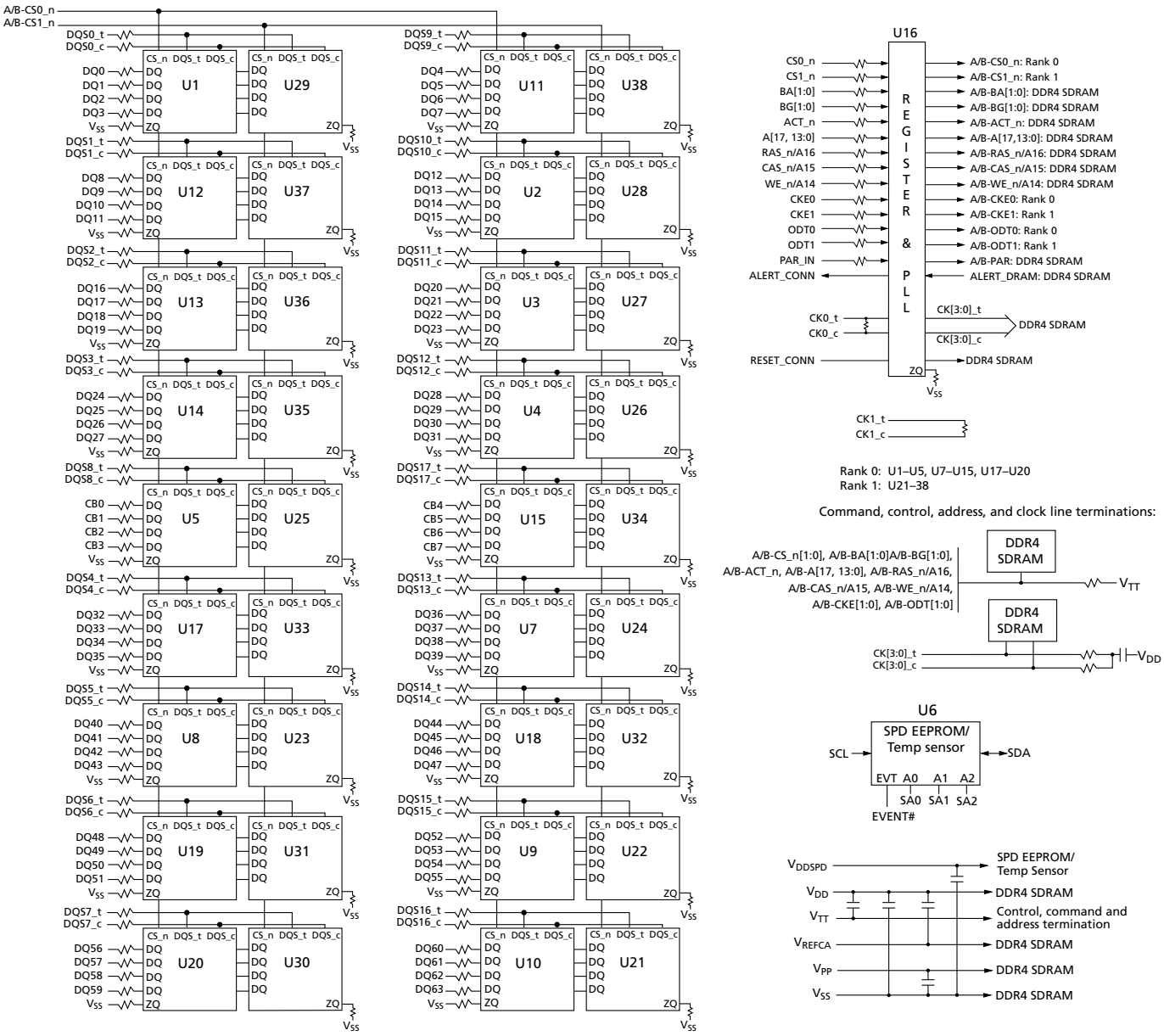
Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U21	0	60	127	U30	0	56	129
	1	62	134		1	58	136
	2	61	270		2	57	272
	3	63	277		3	59	279
U22	0	52	116	U31	0	48	118
	1	55	266		1	51	268
	2	53	259		2	49	261
	3	54	123		3	50	125
U23	0	41	250	U32	0	45	248
	1	43	257		1	46	112
	2	40	107		2	44	105
	3	42	114		3	47	255
U24	0	37	237	U33	0	34	103
	1	38	101		1	32	96
	2	36	94		2	35	246
	3	39	244		3	33	239
U25	0	CB0	48	U34	0	CB6	53
	1	CB3	198		1	CB5	189
	2	CB1	191		2	CB7	196
	3	CB2	55		3	CB4	46
U26	0	28	35	U35	0	25	180
	1	30	42		1	27	187
	2	29	178		2	24	37
	3	31	185		3	26	44

Table 7: Component-to-Module DQ Map Back (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U27	0	21	167	U36	0	18	33
	1	22	31		1	17	169
	2	20	24		2	19	176
	3	23	174		3	16	26
U28	0	13	156	U37	0	9	158
	1	14	20		1	11	165
	2	12	13		2	8	15
	3	15	163		3	10	22
U29	0	0	4	U38	0	5	145
	1	3	154		1	6	9
	2	1	147		2	4	2
	3	2	11		3	7	152

Functional Block Diagram

Figure 2: Functional Block Diagram



Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

General Description

High-speed DDR4 SDRAM modules use DDR4 SDRAM devices with 2 or 4 internal memory bank groups. DDR4 SDRAM modules utilizing 4- and 8-bit-wide DDR4 SDRAM have 4 internal bank groups consisting of 4 memory banks each, providing a total of 16 banks. Sixteen-bit-wide DDR4 SDRAM has 2 internal bank groups consisting of 4 memory banks each, providing a total of 8 banks. DDR4 SDRAM modules benefit from DDR4 SDRAM's use of an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single READ or WRITE operation for the DDR4 SDRAM effectively consists of a single 8*n*-bit-wide, four-clock data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR4 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

Fly-By Topology

DDR4 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR4.

Registering Clock Driver Operation

Registered DDR4 SDRAM modules use a registering clock driver device consisting of a register and a phase-lock loop (PLL). The device complies with the JEDEC DDR4 Register Specification.

The register section of the registering clock driver latches command and address input signals on the rising clock edge. The PLL section of the registering clock driver receives and redrives the differential clock signals (CK, CK#) to the DDR4 SDRAM devices. The registering clock driver(s) reduces clock, control, command, and address signal loading by isolating DRAM from the system controller.

Parity Operations

The registering clock driver includes a parity-checking function that can be enabled or disabled in control word RC0E. When parity checking is enabled, the registering clock driver forwards sampled commands to the SDRAM only when no parity error has occurred. If the parity error function has been disabled, the registering clock driver forwards sampled commands to the DRAM regardless of whether a parity error has occurred. Parity is also checked during control word WRITE operations unless parity checking is disabled.

The registering clock driver receives a parity bit at the DPAR input from the memory controller and compares it with the data received on the qualified CA inputs and indicates on its open-drain ALERT_n pin whether a parity error has occurred. Valid parity is

defined as an even number of 1s across the address and command inputs qualified by at least one of the DCS[n:0] signals being LOW.

Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 8: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	V_{DD} supply voltage relative to V_{SS}	–0.4	1.5	V	1
V_{DDQ}	V_{DDQ} supply voltage relative to V_{SS}	–0.4	1.5	V	1
V_{PP}	Voltage on VPP pin relative to Vss	-0.4	3.0	V	3
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.4	1.5	V	

Table 9: Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units	Notes
V_{DD}	V_{DD} supply voltage		1.14	1.2	1.26	V	2
V_{PP}	DRAM Activating Power Supply		2.375	2.5	2.750	V	3
$V_{REFCA(DC)}$	Input reference voltage command/address bus		0.49 × V_{DD}	0.5 × V_{DD}	0.51 × V_{DD}	V	
V_{TT}	Termination reference voltage (DC) – command/address bus		0.49 × V_{DD} - 20mV	0.5 × V_{DD}	0.51 × V_{DD} + 20mV	V	4
I_I	Input leakage current; Any input 0V ≤ V_{IN} ≤ V_{DD}; V_{REF} input 0V ≤ V_{IN} ≤ 0.75V (All other pins not under test = 0V)	Address inputs, RAS_n, CAS_n, WE_n, CS_n, CKE, ODT, BA, BG, CK_t, CK_c	–	–	–	µA	5
I_{OZ}	Output leakage current; 0V ≤ V_{OUT} ≤ V_{DD}; DQ and ODT are disabled; ODT is HIGH	DQ, DQS_t, DQS_c, ALERT_n	–10	0	10	µA	
I_{VREF}	V_{REF} supply leakage current; V_{REFDQ} = V_{DD}/2 or V_{REFCA} = V_{DD}/2 (All other pins not under test = 0V)		–36	0	72	µA	
T_{OPER}	Normal operating temperature range		0	–	85	°C	7
	Extended temperature operating range (optional)		>85	–	95	°C	6, 7

Notes:
1. V_{DD} and V_{DDQ} must be within 300mV of each other at all times; V_{REFCA} must not be greater than 0.6 x V_{DDQ} or less than 500mV; V_{REF} may be less than or equal to 300mV.
2. V_{DDQ} tracks with V_{DD}; V_{DDQ} and V_{DD} are tied together.
3. V_{PP} must be greater than or equal to V_{DD} at all times.
4. V_{TT} termination voltages in excess of specification limit will adversely affect command and address signals' voltage margins, and reduce timing margins.
5. Inputs are terminated to V_{DD}/2. Input current is dependent on terminating resistance selected in register.
6. The refresh rate is required to double when 85°C < T_{OPER} ≤ 95°C.
7. For additional information, refer to technical note TN-00-08: "Thermal Applications" available on Micron's web site.

DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR4 component data sheets. Component specifications are available on Micron's web site. Module speed grades correlate with component speed grades, as shown below.

Table 10: Module and Component Speed Grades

DDR3 components may exceed the listed module speed grades; module may not be available in all listed speed grades

Module Speed Grade	Component Speed Grade
-2G4	-083E
-2G1	-093E
-1G9	-107E

Design Considerations

Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level.

Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

I_{DD} Specifications

Table 11: DDR4 I_{DD} Specifications and Conditions – 16GB (Die Revision A)

Values are for the MT40A1G4 DDR4 SDRAM only and are computed from values specified in the 4Gb (1 Gig x 4) component data sheet

Parameter	Symbol	2400	2133	1866	Units
One bank ACTIVATE-PRECHARGE current	I_{DD0}[1]	1152	1116	1080	mA
One bank ACTIVATE-PRECHARGE, wordline boost, I_{PP} current	I_{PP0}[1]	126	126	126	mA
One bank ACTIVATE-READ-PRECHARGE current	I_{DD1}[1]	1350	1314	1278	mA
Precharge standby current	I_{DD2N}[2]	1224	1152	1080	mA
Precharge standby ODT current	I_{DD2NT}[1]	1224	1170	1116	mA
Precharge power-down current	I_{DD2P}[2]	576	576	576	mA
Precharge quite standby current	I_{DD2Q}[2]	900	900	900	mA
Active standby current	I_{DD3N}[2]	1404	1332	1260	mA
Active standby I_{PP} current	I_{PP3N}[2]	108	108	108	mA
Active power-down current	I_{DD3P}[2]	720	720	720	mA
Burst read current	I_{DD4R}[1]	2898	2718	2538	mA
Burst read I_{DDQ} current	I_{DDQ4R}[1]	936	864	792	mA
Burst write current	I_{DD4W}[1]	3168	2808	2538	mA
Burst refresh current (1x REF)	I_{DD5B}[1]	2178	2178	2178	mA
Burst refresh I_{PP} current (1 x REF)	I_{PP5B}[1]	270	270	270	mA
Self refresh current: Normal temperature range (0–85°C)	I_{DD6N}[2]	684	684	684	mA
Self refresh current: Extended temperature range (0–95°C)	I_{DD6E}[2]	828	828	828	mA
Self refresh current: Reduced temperature range (0–45°C)	I_{DD6R}[2]	324	324	324	mA
Auto self refresh current (25°C)	I_{DD6A}[2]	216	216	216	mA
Auto self refresh current (45°C)	I_{DD6A}[2]	324	324	324	mA
Auto self refresh current (75°C)	I_{DD6A}[2]	432	432	432	mA
Bank interleave read current	I_{DD7}[1]	4068	3618	3168	mA
Bank interleave read I_{PP} current	I_{PP7}[1]	306	270	234	mA
Maximum power-down current	I_{DD8}[2]	648	648	648	mA

Notes:
1. One module rank in the active $I_{DD/PP}$, the other rank in $I_{DD2P/PP3N}$.
2. All ranks in this $I_{DD/PP}$ condition.

Registering Clock Driver Specifications

Table 12: Registering Clock Driver Electrical Characteristics

SSTE32882 devices or equivalent

Parameter	Symbol	Pins	Min	Nom	Max	Units
DC supply voltage	V_{DD}	–	1.425	1.5	1.575	V
DC reference voltage	V_{REF}	–	0.49 × V_{DD} - 20mV	0.5 × V_{DD}	0.51 × V_{DD} + 20mV	V
DC termination voltage	V_{TT}	–	0.49 × V_{DD} - 20mV	0.5 × V_{DD}	0.51 × V_{DD} + 20mV	V
AC high-level input voltage	$V_{IH(AC)}$	Control, command, address	V_{REF} + 175mV	–	V_{DD} + 400mV	V
AC low-level input voltage	$V_{IL(AC)}$	Control, command, address	–0.4	–	V_{REF} - 175mV	V
DC high-level input voltage	$V_{IH(DC)}$	Control, command, address	V_{REF} + 100mV	–	V_{DD} + 0.4	V
DC low-level input voltage	$V_{IL(DC)}$	Control, command, address	–0.4	–	V_{REF} - 100mV	V
High-level input voltage	$V_{IH(CMOS)}$	RESET#, MIRROR	0.65 × V_{DD}	–	V_{DD}	V
Low-level input voltage	$V_{IL(CMOS)}$	RESET#, MIRROR	0	–	0.35 × V_{DD}	V
Differential input crosspoint voltage range	$V_{IX(AC)}$	CK, CK#, FBIN, FBIN#	0.5 × V_{DD} - 175mV	0.5 × V_{DD}	0.5 × V_{DD} + 175mV	V
Differential input voltage	$V_{ID(AC)}$	CK, CK#	350	–	V_{DD} + TBD	mV
High-level output current	I_{OH}	Err_Out#	–	–	TBD	mA
Low-level output current	I_{OL}	Err_Out#	TBD	–	TBD	mA

Note: 1. Timing and switching specifications for the register listed are critical for proper operation of the DDR4 SDRAM RDIMMs. These are meant to be a subset of the parameters for the specific device used on the module.

Temperature Sensor with Serial Presence-Detect EEPROM

The temperature sensor continuously monitors the module's temperature and can be read back at any time over the I^2C bus shared with the SPD EEPROM. Refer to JEDEC JC-42.4 EE1004 and TSE2004 device specification for complete details.

Serial Presence-Detect

For the latest SPD data, refer to Micron's SPD page: www.micron.com/SPD.

Table 13: Temperature Sensor with SPD EEPROM Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	2.2	3.6	V
Input low voltage: Logic 0; All inputs	V_{IL}	–0.5	V_{DDSPD} * 0.3	V
Input high voltage: Logic 1; All inputs	V_{IH}	V_{DDSPD} * 0.7	V_{DDSPD} + 0.5	V
Output low voltage: 3 mA sink current V_{DDSPD} >2V	V_{OL}	–	0.4	V
Input leakage current: (SCL, SDA) $V_{IN} = V_{DDSPD}$ or V_{SSSPD}	I_{LI}	–	±5	µA
Output leakage current: $V_{OUT} = V_{DDSPD}$ or V_{SSSPD}, SDA in Hi-Z	I_{LO}	–	±5	µA

Table 14: Temperature Sensor and EEPROM Serial Interface Timing

Parameter/Condition	Symbol	Min	Max	Units
Clock frequency	^tSCL	10	1000	kHz
Clock pulse width HIGH time	^tHIGH	260	–	ns
Clock pulse width LOW time	^tLOW	500	–	ns
Detect Clock Low Timeout	$^tTIMEOUT$	25	35	ms
SDA rise time	^tR	–	120	ns
SDA fall time	^tF	–	120	ns
Data-in setup time	$^tSU:DAT$	50	–	ns
Data-in hold time	$^tHD:DI$	0	–	ns
Data out hold time	$^tHD:DAT$	0	350	ns
Start condition setup time	$^tSU:STA$	260	–	ns
Start condition hold time	$^tHD:STA$	260	–	ns
Stop condition setup time	$^tSU:STO$	260	–	ns
Time the bus must be free before a new transition can start	^tBUF	500	–	ns
WRITE time	^tW	–	5	ms
Warm power cycle time off	^tPOFF	1	–	ms
Time from power on to first command	^tINIT	10	–	ms

EVENT# Pin

The temperature sensor also adds the EVENT# pin. This is an open-drain output that requires a pull-up to VDDSPD. Not used by the SPD EEPROM, EVENT# is a temperature sensor output used to flag critical events that can be set up in the sensor's configuration registers.

EVENT# has three defined modes of operation: interrupt mode, comparator mode, and TCRIT Only.

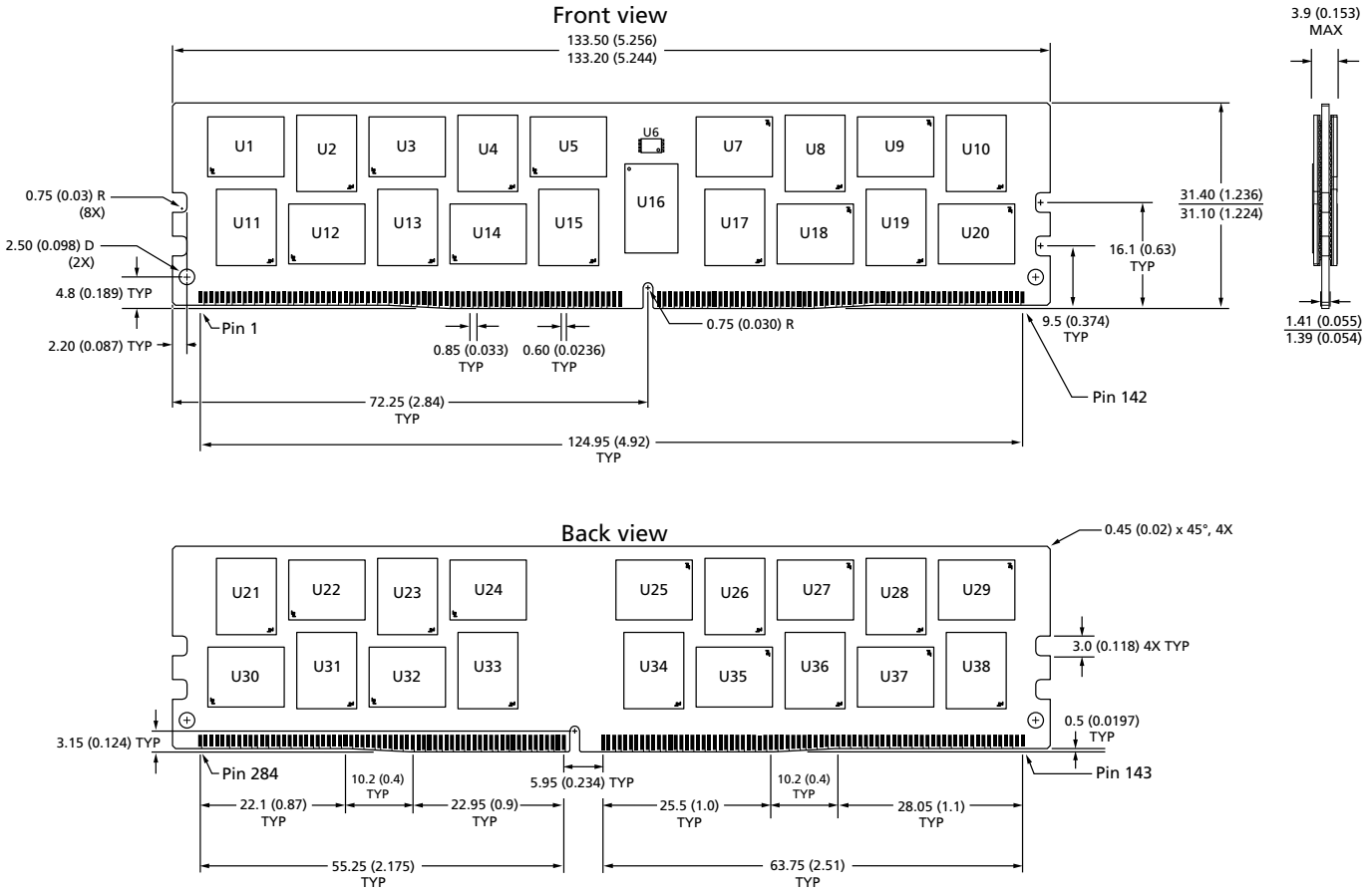
In Interrupt Mode the EVENT# pin will remain asserted until it is released by writing a "1" to the Clear Event bit in the Status Register.

In Comparator Mode the EVENT# pin will clear itself when the error condition is removed. This mode is always used when the temperature is compared against the TCRIT limit.

In TCRIT Only Mode the EVENT# pin will only be asserted if the measured temperature exceeds the TCRIT limit. It will remain asserted until the temperature drops below the TCRIT Limits minus the TCRIT Hysteresis.

Module Dimensions

Figure 3: 284-Pin DDR4 RDIMM



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.

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