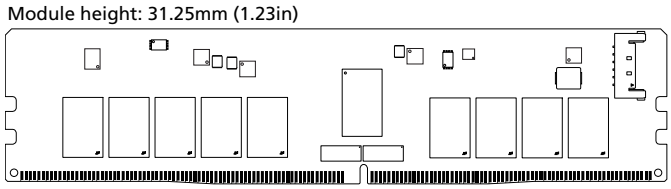
DDR4 SDRAM NVRDIMM

MTA36ASS4G72PF1Z – 32GB

Features

- Nonvolatile registered DIMM (NVRDIMM)
  - Highly reliable nonvolatile memory solution
  - DDR4 RDIMM, NAND Flash, and PowerGEM management integrated in a single module
  - Persistent energy source options
    - Option 1: Battery-free power source (PowerGEM)
    - Option 2: Persistent DDR4 12V pin
  - 32GB (4 Gig x 72) DDR4 RDIMM
  - 64GB SLC Flash
  - DDR4 functionality and operations supported as defined in the component data sheet
  - JEDEC-compliant DDR4 288-pin dual in-line memory module connector
  - Fast data transfer rate: PC4-2933
  - V_{DD} = 1.20V (typical)
  - V_{PP} = 2.5V (typical)
  - V_{DDSPD} = 2.2–2.8V
  - Supports ECC error detection and correction
  - Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
  - Low-power auto self refresh (LPASR)
  - On-die V_{REFDQ} generation and calibration
  - Dual-rank, comprised of TwinDie, x4 DRAM components
  - On-board I^2C temperature sensor with integrated serial presence-detect (SPD) EEPROM
  - 16 internal banks; 4 groups of 4 banks each
  - Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
  - Selectable BC4 or BL8 on-the-fly (OTF)
  - Gold edge contacts
  - Halogen-free
  - Fly-by topology
  - Terminated control, command, and address bus
- Battery-free power source (ultra capacitor based PowerGEM)
  - Powers the Micron NVDIMM when the host system loses power
  - 5-year operating life
  - No catastrophic failure modes
  - RoHS-, REACH-, and UL-compliant
- Nonvolatile memory (NVM) system-level features
  - In-system health monitoring of PowerGEM and NAND Flash
  - Automatic history tracking: tracks critical internal system parameters
  - Interlocked control sequence for safe and reliable operation (system protocol)
  - I^2C command/control bus
  - Multiple backup trigger methods
    - ADR, SAVE_n (DDR4 pin 230) assert, pull up to 2.5V through resistor on the NVDIMM
    - RESET_n (DDR4 pin 58)
    - SMBus command

Figure 1: 288-Pin NVDIMM (PCB 2562)



Options	Marking
• Operating temperature	
– Commercial (0°C ≤ T_{OPER} ≤ +95°C)	None
– Storage (–25°C ≤ T_{STG} ≤ +125°C)	
• Package	
– 288-pin DIMM (halogen-free)	Z
• Frequency/CAS latency	
– 0.68ns @ CL = 21 (DDR4-2933)	-2G9

Table 1: Key Timing Parameters

Speed Grade	PC4-	Data Rate (MT/s) CL = 24	22	21	20\ 19	18\ 17	16\ 15	14\ 13	12\ 11	10\ 9	^{t}RCD ns	^{t}RP ns	^{t}RC ns
-3G2	3200	3200, 2933	3200, 2933	2933	2666\ 2666	2400\ 2400	2133\ 2133	1866\ 1866	1600\ 1600	1333\ –	13.75	13.75	45.75
-2G9	2933	–	2933	2933	2666\ 2666	2400\ 2400	2133\ 2133	1866\ 1866	1600\ 1600	1333\ –	14.32 (13.75)[1]	14.32 (13.75)[1]	46.32 (45.75)[1]
-2G6	2666	–	–	–	2666\ 2666	2400\ 2400	2133\ 2133	1866\ 1866	1600\ 1600	1333\ –	14.25 (13.75)[1]	14.25 (13.75)[1]	46.25 (45.75)[1]
-2G3	2400	–	–	–	–	2400\ 2400	2133\ 2133	1866\ 1866	1600\ 1600	1333\ –	14.16 (13.75)[1]	14.16 (13.75)[1]	46.16 (45.75)[1]
-2G1	2133	–	–	–	–	–	2133\ 2133	1866\ 1866	1600\ 1600	1333\ 1333	14.06 (13.5)[1]	14.06 (13.5)[1]	47.06 (46.5)[1]

Note: 1. Down-bin timing, refer to component data sheet Speed Bin Tables for details.

Table 2: Addressing

Parameter	32GB
Row address	128K A[16:0]
Column address	1K A[9:0]
Device bank group address	4 BG[1:0]
Device bank address per group	4 BA[1:0]
Device configuration	16Gb TwinDie (4 Gig x 4), 16 banks
Module rank address	2 CS_n [1:0]

Table 3: Part Numbers and Timing Parameters – 32GB Modules

Base device: MT40A4G4,[1] 16Gb TwinDie DDR4 SDRAM

Part Number	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-$_{n}$RCD-$_{n}$RP)
MTA36ASS4G72PF1Z-2G9__	32GB	4 Gig x 72	23.47 GB/s	0.68ns/2933 MT/s	21-21-21

Notes: 1. The data sheet for the base device can be found on micron.com.
2. All NVDIMM part numbers end with a five-character code (not shown) that designates die revision, PCB revision and controller type. Consult factory for current revision/controller codes. Example: MTA36ASS4G72PF1Z-2G9PR1AB.

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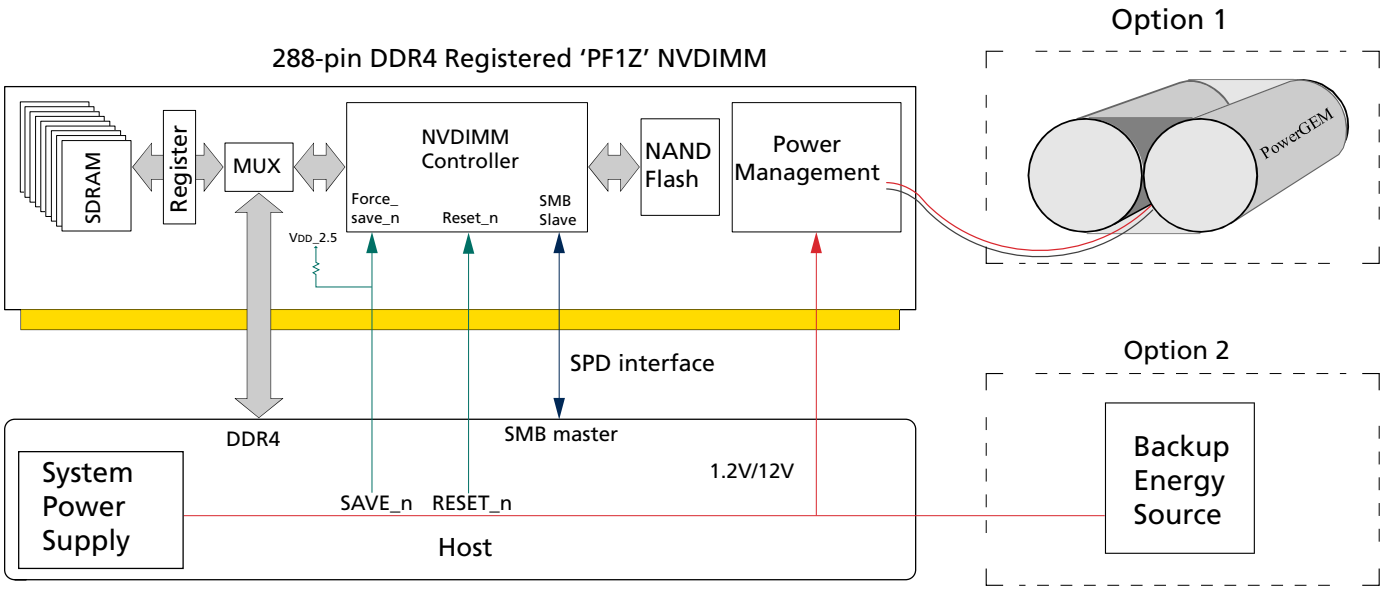
NVDIMM System Block Diagram

This Micron NVDIMM is available as a 288-pin DDR4 RDIMM with a 72-bit-wide data bus in a dual-rank x4 configuration, using 16Gb TwinDie DRAM components for 32GB DRAM density.

Figure 2: Micron DDR4 NVDIMM System Block Diagram



A persistent energy source ensures continuity of power to the Micron NVDIMM after the system power supply is interrupted. This enables the NVDIMM to save the contents of the DDR4 SDRAM to the nonvolatile NAND Flash memory and shut down independently from the system's power supply.

The persistent energy source can be provided to the NVDIMM in one of two ways:

- **Option 1 – PowerGEM (green energy module):** Designed by Agiga Tech,® this ultracapacitor-based energy source is connected to the Micron NVDIMM via a proprietary cable and connection, providing backup power as well as health monitoring features. The ultracaps are charged through the 12V power pin on the DDR4 connector. Please refer to the Ultracapacitor Power Module data sheet available from micron.com for further information.
- **Option 2 – Backup Energy Source:** Consists of a rechargeable energy source provided by the system. After power interruption, the persistent 12V power pin on the JEDEC-compliant DDR4 DIMM connector supplies the power needed to backup the data from the DDR4 SDRAM to the NAND Flash. Implementation of this option requires further system design. Without implementation of the PowerGEM, health monitoring and power management become dependent on the system design.

Host Coordination Using Micron NVDIMM Control Signal

To prevent SDRAM data corruption due to a sudden power failure, the host must take steps to ensure the SDRAM is placed in a safe state as soon as a power failure has been detected.

The Micron NVDIMM will be able to provide proper coordination if the host meets the following requirements:

- The host must have early warning that power is failing, allowing it to perform an orderly shutdown. Typically, this is achieved by the system monitoring the system power supply and providing a signal that indicates power is failing.
- The host must put the DDR4 SDRAM into self refresh before handing it off to the Micron NVDIMM subsystem. After this state is entered, the clock enable (CKE0) signal is LOW and all SDRAM control signals except CKE0 and RESET_n are "Don't Care." The SDRAM refreshes itself in this mode, preserving its contents as the host triggers the NVDIMM to take control of the SDRAM, and the SDRAM contents are backed up to the Flash memory.
- When the host regains control of the DDR4 SDRAM from the Micron NVDIMM controller (for example, after performing a RESTORE operation), the host must remove the DDR4 SDRAM from self refresh. The host should take care not to assert the RESET_n signal after a RESTORE operation completes, as the RESET_n signal resets the internal SDRAM state machine and restored data can be potentially lost.

For more detailed information regarding host coordination with the Micron NVDIMM controller, refer to the Micron NVDIMM firmware specification.

Pin Assignments

The pin assignment table below is a comprehensive list of all possible pin assignments for DDR4 RDIMM modules. See the Functional Block Diagram for pins specific to this module.

Table 4: Pin Assignments

288-Pin DDR4 NVDIMM Front								288-Pin DDR4 NVDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	12V	37	V_{SS}	73	V_{DD}	109	V_{SS}	145	12V	181	DQ29	217	V_{DD}	253	DQ41
2	V_{SS}	38	DQ24	74	CK0_t	110	DQS14_t/ TDQS14_t	146	V_{REFCA}	182	V_{SS}	218	CK1_t	254	V_{SS}
3	DQ4	39	V_{SS}	75	CK0_c	111	DQS14_c/ TDQS14_c	147	V_{SS}	183	DQ25	219	CK1_c	255	DQS5_c
4	V_{SS}	40	DQS12_t/ TDQS12_t	76	V_{DD}	112	V_{SS}	148	DQ5	184	V_{SS}	220	V_{DD}	256	DQS5_t
5	DQ0	41	DQS12_c/ TDQS12_c	77	V_{TT}	113	DQ46	149	V_{SS}	185	DQS3_c	221	V_{TT}	257	V_{SS}
6	V_{SS}	42	V_{SS}	78	EVENT_n	114	V_{SS}	150	DQ1	186	DQS3_t	222	PARITY	258	DQ47
7	DQS9_t/ TDQS9_t	43	DQ30	79	A0	115	DQ42	151	V_{SS}	187	V_{SS}	223	V_{DD}	259	V_{SS}
8	DQS09_c/ TDQS9_c	44	V_{SS}	80	V_{DD}	116	V_{SS}	152	DQS0_c	188	DQ31	224	BA1	260	DQ43
9	V_{SS}	45	DQ26	81	BA0	117	DQ52	153	DQS0_t	189	V_{SS}	225	A10/ AP	261	V_{SS}
10	DQ6	46	V_{SS}	82	RAS_n/ A16	118	V_{SS}	154	V_{SS}	190	DQ27	226	V_{DD}	262	DQ53
11	V_{SS}	47	CB4	83	V_{DD}	119	DQ48	155	DQ7	191	V_{SS}	227	NC	263	V_{SS}
12	DQ2	48	V_{SS}	84	CS0_n	120	V_{SS}	156	V_{SS}	192	CB5	228	WE_n/ A14	264	DQ49
13	V_{SS}	49	CB0	85	V_{DD}	121	DQS15_t/ TDQS15_t	157	DQ3	193	V_{SS}	229	V_{DD}	265	V_{SS}
14	DQ12	50	V_{SS}	86	CAS_n/ A15	122	DQS15_c/ TDQS15_c	158	V_{SS}	194	CB1	230	SAVE_n	266	DQS6_c
15	V_{SS}	51	DQS17_t/ TDQS17_t	87	ODT0	123	V_{SS}	159	DQ13	195	V_{SS}	231	V_{DD}	267	DQS6_t
16	DQ8	52	DQS17_c/ TDQS17_c	88	V_{DD}	124	DQ54	160	V_{SS}	196	DQS8_c	232	A13	268	V_{SS}
17	V_{SS}	53	V_{SS}	89	CS1_n/ NC	125	V_{SS}	161	DQ9	197	DQS8_t	233	V_{DD}	269	DQ55
18	DQS10_t/ TDQS10_t	54	CB6	90	V_{DD}	126	DQ50	162	V_{SS}	198	V_{SS}	234	A17	270	V_{SS}
19	DQS10_c/ TDQS10_c	55	V_{SS}	91	ODT1/ NC	127	V_{SS}	163	DQS1_c	199	CB7	235	NC/ C2	271	DQ51
20	V_{SS}	56	CB2	92	V_{DD}	128	DQ60	164	DQS1_t	200	V_{SS}	236	V_{DD}	272	V_{SS}
21	DQ14	57	V_{SS}	93	CS2_n/ C0	129	V_{SS}	165	V_{SS}	201	CB3	237	CS3_n/ C1, NC	273	DQ61
22	V_{SS}	58	RESET_n	94	V_{SS}	130	DQ56	166	DQ15	202	V_{SS}	238	SA2	274	V_{SS}
23	DQ10	59	V_{DD}	95	DQ36	131	V_{SS}	167	V_{SS}	203	CKE1/ NC	239	V_{SS}	275	DQ57
24	V_{SS}	60	CKE0	96	V_{SS}	132	DQS16_t/ TDQS16_t	168	DQ11	204	V_{DD}	240	DQ37	276	V_{SS}

Table 4: Pin Assignments (Continued)

288-Pin DDR4 NVDIMM Front								288-Pin DDR4 NVDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
25	DQ20	61	V_{DD}	97	DQ32	133	DQS16_c/ TDQS16_c	169	V_{SS}	205	NC	241	V_{SS}	277	DQS7_c
26	V_{SS}	62	ACT_n	98	V_{SS}	134	V_{SS}	170	DQ21	206	V_{DD}	242	DQ33	278	DQS7_t
27	DQ16	63	BG0	99	DQS13_t/ TDQ13_t	135	DQ62	171	V_{SS}	207	BG1	243	V_{SS}	279	V_{SS}
28	V_{SS}	64	V_{DD}	100	DQS13_c/ TDQS13_c	136	V_{SS}	172	DQ17	208	ALERT_n	244	DQS4_c	280	DQ63
29	DQS11_t/ TDQS11_t	65	A12/BC_n	101	V_{SS}	137	DQ58	173	V_{SS}	209	V_{DD}	245	DQS4_t	281	V_{SS}
30	DQS11_c/ TDQS11_c	66	A9	102	DQ38	138	V_{SS}	174	DQS2_c	210	A11	246	V_{SS}	282	DQ59
31	V_{SS}	67	V_{DD}	103	V_{SS}	139	SA0	175	DQS2_t	211	A7	247	DQ39	283	V_{SS}
32	DQ22	68	A8	104	DQ34	140	SA1	176	V_{SS}	212	V_{DD}	248	V_{SS}	284	V_{DDSPD}
33	V_{SS}	69	A6	105	V_{SS}	141	SCL	177	DQ23	213	A5	249	DQ35	285	SDA
34	DQ18	70	V_{DD}	106	DQ44	142	V_{PP}	178	V_{SS}	214	A4	250	V_{SS}	286	V_{PP}
35	V_{SS}	71	A3	107	V_{SS}	143	V_{PP}	179	DQ19	215	V_{DD}	251	DQ45	287	V_{PP}
36	DQ28	72	A1	108	DQ40	144	NC	180	V_{SS}	216	A2	252	V_{SS}	288	V_{PP}

Pin Descriptions

The pin description table below is a comprehensive list of all possible pins for DDR4 UDIMM, RDIMM, SODIMM, and LRDIMM modules. All pins listed may not be supported on the module defined in this data sheet. See functional block diagram specific to this module to review all pins utilized on this module.

Table 5: Pin Descriptions

Symbol	Type	Description
Ax	Input	**Address inputs:** Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, WE_n/A14, CAS_n/A15, and RAS_n/A16 have additional functions; see individual entries in this table). The address inputs also provide the op-code during the MODE REGISTER SET command. A17 is only defined for x4 SDRAM configuration.
A10/AP	Input	**Auto precharge:** A10 is sampled during READ and WRITE commands to determine whether auto precharge should be performed to the accessed bank after a READ or WRITE operation (HIGH = Auto precharge; LOW = No auto precharge). A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by the bank group and bank addresses.
A12/BC_n	Input	**Burst chop:** A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. (HIGH = No burst chop; LOW = Burst-chopped). See the Command Truth Table in DDR4 component data sheet for more information.

Table 5: Pin Descriptions (Continued)

Symbol	Type	Description
ACT_n	Input	**Command input:** ACT_n defines the activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 will be considered as row address A16, A15, and A14. See the Command Truth Table in DDR4 component data sheet for more information.
BAx	Input	**Bank address inputs:** Define to which bank an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determines which mode register is to be accessed during a MODE REGISTER SET command.
BGx	Input	**Bank group address inputs:** Define to which bank group a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determines which mode register is to be accessed during a MODE REGISTER SET command. BG[1:0] are used in the x4 and x8 configurations. x16-based SDRAMs only have BG0.
C0, C1, C2 (RDIMM/LRDIMM only)	Input	**Chip ID:** These inputs are used only when devices are stacked, that is, 2H, 4H, and 8H stacks for x4 and x8 configurations using though-silicon vias (TSVs). These pins are not used in the x16 configuration. Some DDR4 modules support a traditional DDP package, which use CS1_n, CKE1, and ODT1 to control the second die. For all other stack configurations, such as a 4H or 8H, it is assumed to be a single-load (master/slave)-type configuration where C0, C1, and C2 are used as chip ID selects in conjunction with a single CS_n, CKE, and ODT. Chip ID is considered part of the command code.
CKx_t CKx_c	Input	**Clock:** Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c.
CKEx	Input	**Clock enable:** CKE HIGH activates, and CKE LOW deactivates, the internal clock signals, device input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self refresh exit. After V_{REFCA} has become stable during the power-on and initialization sequence, it must be maintained during all operations (including SELF REFRESH). CKE must be held HIGH throughout read and write accesses. Input buffers (excluding CK_t, CK_c, ODT, RESET_n, and CKE) are disabled during power-down. Input buffers (excluding CKE and RESET_n) are disabled during self refresh.
CSx_n	Input	**Chip select:** All commands are masked when CS_n is registered HIGH. CS_n provides external rank selection on systems with multiple ranks. CS_n is considered part of the command code. CS2_n and CS3_n are not used on UDIMMs.
ODTx	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When ODT is enabled, on-die termination (R_{TT}) is applied only to each DQ, DQS_t, DQS_c, DM_n/DBI_n/TDQS_t, and TDQS_c signal for x4 and x8 configurations (when the TDQS function is enabled via the mode register). For the x16 configuration, R_{TT} is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, UDM_n, and LDM_n signal. The ODT pin will be ignored if the mode registers are programmed to disable R_{TT}.
PARITY	Input	**Parity for command and address:** This function can be enabled or disabled via the mode register. When enabled in MR5, then DRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG[1:0], BA[1:0], A[16:0]. Input parity should be maintained at the rising edge of the clock and at the same time with command and address with CS_n LOW.

Table 5: Pin Descriptions (Continued)

Symbol	Type	Description
RAS_n/A16 CAS_n/A15 WE_n/A14	Input	**Command inputs:** RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n) define the command and/or address being entered. Those pins have multifunction. For example, for activation with ACT_n LOW, these are addresses like A16, A15, and A14, but for a non-activation command with ACT_n HIGH, these are command pins for READ, WRITE, and other commands defined in the command truth table.
RESET_n	CMOS Input	**Active LOW asynchronous reset:** Reset is active when RESET_n is LOW; inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is blocked when NVDIMM is armed.
SAx	Input	**Serial address inputs:** Used to configure the temperature sensor/SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for temperature sensor/SPD EEPROM:** Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I^2C bus.
DQx, CBx	I/O	**Data input/output and check bit input/output:** Bidirectional data bus. DQ represents DQ[3:0], DQ[7:0], and DQ[15:0] for the x4, x8, and x16 configurations, respectively. If cyclic redundancy checksum (CRC) is enabled via the mode register, then CRC code is added at the end of the data burst. Either one or all of DQ0, DQ1, DQ2, or DQ3 is/are used for monitoring the internal V_{REF} level during test via mode register setting MR[4] A[4] = HIGH; training times change when enabled.
DM_n/DBI_n/ TDQS_t(DMU_n,DBIU_n),(DML_n/ DBIl_n)	I/O	**Input data mask and data bus inversion:** DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. DM is mux'ed with DBI function by mode register A10, A11, A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by mode register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in x8 SDRAM configurations. TDQS is not valid for UDIMMs.
DQS_t DQS_c DQSU_t DQSU_c DQSL_t DQSL_c	I/O	**Data strobe:** Output with read data, input with write data. Edge-aligned with read data, centered-aligned with WRITE data. For x16 configurations, DQSL corresponds to the data on DQ[7:0]; DQSU corresponds to the data on DQ[15:8]. For the x4 and x8 configurations, DQS corresponds to the data on DQ[3:0] and DQ[7:0], respectively. DDR4 SDRAM supports a differential data strobe only and does not support a single-ended data strobe.
ALERT_n	Output	**Alert output:** Possesses multifunctions such as CRC error flag and command and address parity error flag as output signal. If there is a CRC error, then ALERT_n goes LOW for the time interval and returns HIGH. If there is an error in command address parity check, then ALERT_n goes LOW until ongoing DRAM internal recovery transaction is complete. During connectivity test mode this pin functions as an input. Using this signal or not is dependent on the system. If not connected as a signal, ALERT_n must be connected to V_{DD} on the DIMM.
EVENT_n	Output	**Temperature event:** EVENT_n is asserted by the temperature sensor when critical temperature thresholds have been exceeded. This pin has no function (NF) on modules without temperature sensors.

Table 5: Pin Descriptions (Continued)

Symbol	Type	Description
SAVE_n	Input (open drain)	**Force save:** Active LOW, open drain input pulled to 2.5V through a 2K ohm resistor on module. Commands the Micron NVDIMM to switch its internal MUXs and copy the data in the SDRAM to internal NAND Flash. The SDRAM must be placed in self refresh mode before asserting this pin to ensure that no data is lost during this operation.
TDQS_t TDQS_c (x8 DRAM based RDIMM only)	Output	**Termination data strobe:** TDQS_t and TDQS_c are not valid for UDIMMs. When enabled via the mode register, the SDRAM enables the same R_{TT} termination resistance on TDQS_t and TDQS_c that is applied to DQS_t and DQS_c. When the TDQS function is disabled via the mode register, DM/TDQS_t provides the data mask (DM) function, and TDQS_c is not used. The TDQS function must be disabled in the mode register for both the x4 and x16 configurations. The DM function is supported only in the x8 and x16 configurations. DM, DBI, and TDQS are a shared pin and are enabled/disabled by mode register settings. For further information about TDQS, refer to the DDR4 DRAM data sheet.
V_{DD}	Supply	**Module power supply:** 1.21V (typical)
V_{PP}	Supply	**DRAM activating power supply:** 2.5V –0.125V/+0.250V
V_{REFCA}	Supply	Reference voltage for control, command, and address pins.
V_{SS}	Supply	Ground.
V_{TT}	Supply	Power supply for termination of address, command, and control, $V_{DD}/2$.
V_{DDSPD}	Supply	Power supply used to power the I^2C bus used for SPD.
12V	Supply	Power supply for charging NVDIMM backup energy storage device (PowerGEM): 12V ±1.8V. Normal operation can be supported down to 6V; however, if these pins are being used to charge a PowerGEM, the charge time will be extended. Alternatively, these pins can be a persistent power supply for NVDIMM during SAVE operation: 6V to 13.8V.
RFU	–	Reserved for future use.
NC	–	**No connect:** No internal electrical connection is present.
NF	–	**No function:** Internal connection may be present but has no function.

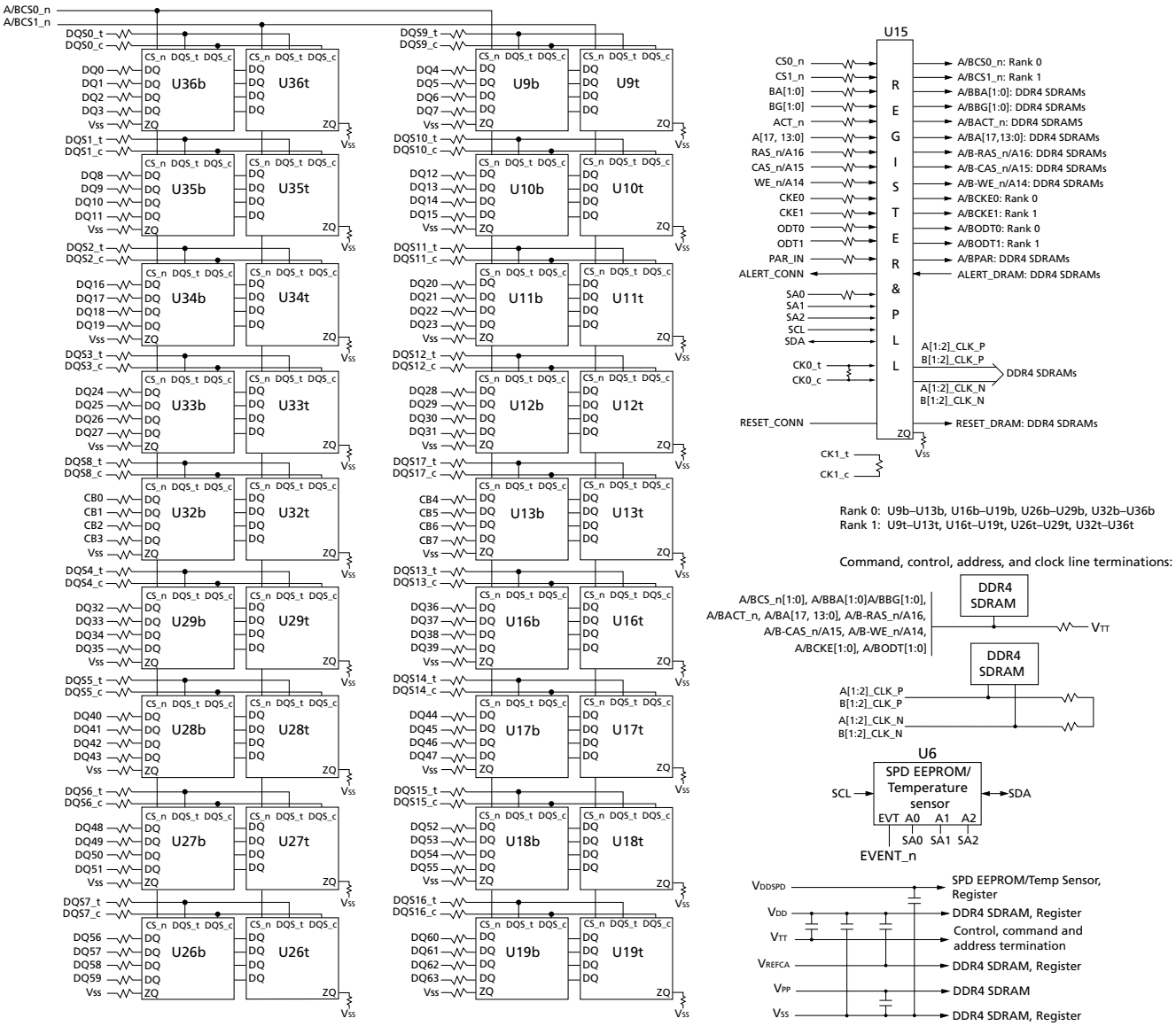
DQ Map

Table 6: Component-to-Module DQ Map

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U9	0	6	10	U10	0	14	21
	1	4	3		1	12	14
	2	7	155		2	15	166
	3	5	148		3	13	159
U11	0	22	32	U12	0	30	43
	1	20	25		1	28	36
	2	23	177		2	31	188
	3	21	170		3	29	181
U13	0	CB6	54	U16	0	39	247
	1	CB4	47		1	36	95
	2	CB7	199		2	38	102
	3	CB5	192		3	37	240
U17	0	47	258	U18	0	55	269
	1	44	106		1	52	117
	2	46	113		2	54	124
	3	45	251		3	53	262
U19	0	63	280	U26	0	57	275
	1	60	128		1	59	282
	2	62	135		2	56	130
	3	61	273		3	58	137
U27	0	49	264	U28	0	41	253
	1	51	271		1	43	260
	2	48	119		2	40	108
	3	50	126		3	42	115
U29	0	33	242	U32	0	CB0	49
	1	35	249		1	CB3	201
	2	32	97		2	CB1	194
	3	34	104		3	CB2	56
U33	0	24	24	U34	0	16	27
	1	27	27		1	19	179
	2	25	25		2	17	172
	3	26	26		3	18	34
U35	0	8	16	U36	0	0	5
	1	11	168		1	3	157
	2	9	161		2	1	150
	3	10	23		3	2	12

SDRAM Functional Block Diagram

Figure 3: SDRAM Functional Block Diagram



Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

Micron NVDIMM General Description

Micron NVDIMM is a new class of nonvolatile memory developed to meet the need for higher-density, higher-performance memory for enterprise-class storage and server applications. By combining DRAM, flash, an intelligent system controller, and an ultracapacitor power source, Micron NVDIMM provides a highly reliable memory subsystem that runs with the latency and endurance of the fastest DRAM, and with the persistence of flash. Until recently, designers have reluctantly used batteries to maintain their data during power outages. Others have moved toward new flash-based technologies for memory persistence, but this option falls short of DRAM in terms of latency, speed, endurance, and reliability. Micron NVDIMM enables the fastest possible system performance while eliminating the many problems associated with batteries, such as hazardous material disposal, short operating life, and extensive maintenance.

The Micron DDR4 NVDIMM has been specifically designed to operate with host systems that have implemented the asynchronous DRAM refresh (ADR) feature, although it is possible to integrate into systems that do not have this enabled. Please contact Micron for more details on system integration requirements and instructions.

During normal operation, bypass mode, the Micron DDR4 NVDIMM appears as a standard registered DDR4 DIMM to the host system, providing all the benefits and speed of a high-speed, high-density SDRAM. In the event of a power loss, the Micron NVDIMM controller can be commanded to take control of the SDRAM, transferring its contents to flash memory using energy from its own battery-free power source or from a system-level persistent power source, thereby preserving all of the SDRAM data. After power is restored, the Micron NVDIMM controller can be commanded to transfer the contents from the flash back to the SDRAM and return control to the host system.

DDR4 RDIMM Functionality

DDR4 SDRAM modules are high-speed, CMOS dynamic random access memory modules that use internally configured 16-bank DDR4 SDRAM devices. DDR4 SDRAM modules use DDR architecture to achieve high-speed operation. DDR4 is essentially an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR4 SDRAM module effectively consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR4 modules use two sets of differential signals: DQS_t/DQS_c to capture data and CK_t/CK_c to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

Fly-By Topology

DDR4 modules, such as this NVDIMM, use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR4.

Registering Clock Driver Operation

Registered DDR4 SDRAM modules use a registering clock driver device consisting of a register and a phase-lock loop (PLL). The device complies with the JEDEC DDR4 RCD specification.

To reduce the electrical load on the host memory controller's command, address, and control bus, Micron's RDIMMs use a DDR4 registering clock driver (RCD). The RCD presents a single load to the controller while redriving signals to the DDR4 SDRAM devices, which helps enable higher densities and increase signal integrity. The RCD also provides a low-jitter, low-skew PLL that redistributes a differential clock pair to multiple differential pairs of clock outputs.

Control Words

The RCD device(s) used on DDR4 RDIMMs, LRDIMMs, and NVDIMMs contain configuration registers known as control words, which the host uses to configure the RCD based on criteria determined by the module design. Control words can be set by the host controller through either the DRAM address and control bus or the I^2C bus interface. The RCD I^2C bus interface resides on the same I^2C bus interface as the module temperature sensor and EEPROM.

Parity Operations

The RCD includes a parity-checking function that can be enabled or disabled in control word RC0E. The RCD receives a parity bit at the DPAR input from the memory controller and compares it with the data received on the qualified command and address inputs; it indicates on its open-drain ALERT_n pin whether a parity error has occurred. If parity checking is enabled, the RCD forwards commands to the SDRAM when no parity error has occurred. If the parity error function is disabled, the RCD forwards sampled commands to the SDRAM regardless of whether a parity error has occurred. Parity is also checked during control word WRITE operations unless parity checking is disabled.

Rank Addressing

The chip select pins (CS_n) on Micron's modules are used to select a specific rank of DRAM. The RDIMM is capable of selecting ranks in one of three different operating modes, dependent on setting DA[1:0] bits in the DIMM configuration control word located within the RCD. Direct DualCS mode is utilized for single- or dual-rank modules. For quad-rank modules, either direct or encoded QuadCS mode is used.

Temperature Sensor with Serial Presence-Detect EEPROM

Thermal Sensor Operations

The integrated thermal sensor continuously monitors the temperature of the DIMM PCB directly below the device and updates the temperature data register. Temperature data may be read from the bus host at any time providing the host real time feedback of module temperature. Thermal senors will provide a temperature resolution of 0.5, 0.25, 0.125, or 0.0625 °C. It is recommended that the system read the Temperature Sensor Capabilities register during system initialization to determine the temperature resolution utilized. System designers may utilize the multiple programmable and read-only temperature registers to create a custom temperature sensing solution based on system requirements and JEDEC JC-42.2.

EVENT_n Pin

The temperature sensor also adds the EVENT_n pin. This is an open-drain output that requires a pull-up to V_{DDSPD}. Not used by the SPD EEPROM, EVENT_n is a temperature sensor output used to flag critical events that can be set up in the sensor's configuration registers. The Micron NVDIMM controller can also be configured to drive EVENT_n LOW to indicate that "good-to-go" status is LOW and that the Micron NVDIMM may no longer be nonvolatile. See the NVDIMM firmware document for details on how this is configured.

- EVENT_n has three defined modes of operation: interrupt mode, comparator mode, and TCRIT only.
- In interrupt mode the EVENT_n pin will remain asserted until it is released by writing a 1 to the clear event bit in the status register.
- In comparator mode the EVENT_n pin will clear itself when the error condition is removed. This mode is always used when the temperature is compared against the TCRIT limit.
- In TCRIT only mode the EVENT_n pin will only be asserted if the measured temperature exceeds the TCRIT limit. It will remain asserted until the temperature drops below the TCRIT limits minus the TCRIT hysteresis.

Serial Presence-Detect EEPROM Operation

DDR4 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 512-byte JEDEC JC-42.4 compliant EEPROM that is segregated into 4, 128-byte, write protectable blocks. The SPD content is aligned with these blocks as follows.

Block	Range		Description
0	0–127	0x000–0x07F	Configuration and DRAM parameters
1	128–255	0x080–0x0FF	Module parameters
2	256–319	0x100–0x13F	Reserved – All bytes coded as 0x00
	320–383	0x140–0x17F	Manufacturing information
3	384–511	0x180–0x1FF	End user programmable

The first 384 bytes are programmed by Micron, the remaining 128 bytes of storage are available for use by the customer.

The EEPROM resides on a two-wire I^2C serial interface and is not integrated with the memory bus in any manner. It operates as a slave device in the I^2C bus protocol, with all operations synchronized by the serial clock. Transfer rates of up to 1 MHz are achievable at 2.2–3.6V.

Micron implements reversible software write protection on DDR4 SDRAM-based modules. This prevents the lower 384 bytes (bytes 0–383) from being inadvertently programmed or corrupted. The upper 128 bytes remain available for customer use and unprotected.

I^2C Address Map

Micron NVDIMMs have multiple devices connected to the system I^2C-compatible SMBus. The system accessible address spaces for these devices are provided below for reference as these devices may have content or configurable registers that can be accessed by the system. All applicable specifications must be followed when accessing these address spaces to ensure proper operation of the NVDIMM.

I^2C Address Map	
NVDIMM controller	0x40–0x47
Temperature sensor	0x18–0x1F
SPD EEPROM – PAGE/WRITE PROTECT	0x30–0x37
SPD EEPROM – READ/WRITE	0x50–0x57
Registering clock drive (RCD)	0x58–0x5F

Notes:
1. SA[2:0] must be set accordingly to address a device on a specific module.
2. SPD EEPROM: PAGE and WRITE PROTECT do not use SA[2:0]. These commands are broadcast to SPD EEPROMs on all the modules in the bus.

Timing Parameters

Several system-level timing parameters are specific to the operation of the Micron NVDIMM.

Table 7: Timing Parameters

Parameter/Condition	Symbol		Typ	Max	Units	Notes
Micron NVDIMM controller able to receive commands via I^2C bus from a power-up; energy source charge time not included	^{t}HW_RDY		9	120	sec	1
Micron NVDIMM controller charging PowerGEM ultracapacitors	^{t}ES_CHRG		–	240	sec	2
Micron NVDIMM controller copying DRAM contents to NAND Flash	^{t}SAVE	32GB	113	115	sec	3
Micron NVDIMM controller copying an image from NAND Flash to DRAM	^{t}RESTORE	32GB	125	200	sec	4

Notes:
1. Maximum time will be reached when the NVDIMM is reset following a firmware update.
2. All conditions defined in the NVDIMM firmware specification must be met for the NVDIMM_READY register to be set indicating to the host that the NVDIMM can be used as nonvolatile memory. ^{t}ES_CHRG MAX is defined as the charge time of the ultracapacitors from a completely discharged state. Values shown in this table reflect times observed with a typical PowerGEM configuration for the given NVDIMM density. The actual maximum time will depend on the specific PowerGEM used. See the PowerGEM data sheet for details.
3. If the NVDIMM encounters errors during the SAVE, it will continue to attempt to save until it either runs out of power or a command is sent to the NVDIMM to cancel the SAVE operation.
4. Maximum restore time based on 10,000 ECC correction limit on the NAND Flash.

Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 8: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	V_{DD} supply voltage relative to V_{SS}	–0.4	1.5	V	1
V_{DDQ}	V_{DDQ} supply voltage relative to V_{SS}	–0.4	1.5	V	1
V_{PP}	Voltage on V_{PP} pin relative to V_{SS}	–0.4	3.0	V	2
12V	Voltage on 12V pin relative to V_{SS}	–0.4	13.8	V	
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.4	1.5	V	

Notes:
1. V_{DDQ} balls on DRAM are tied to V_{DD}.
2. V_{PP} must be greater than or equal to V_{DD} at all times.

Table 9: Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units	Notes
V_{DD}	V_{DD} supply voltage		1.14	1.2	1.26	V	1
V_{PP}	DRAM activating power supply		2.375	2.5	2.750	V	2
12V	Auxiliary NVDIMM power supply		6	12	13.8	V	
$V_{REFCA(DC)}$	Input reference voltage command/address bus		0.49 × V_{DD}	0.5 × V_{DD}	0.51 × V_{DD}	V	3
V_{TT}	Termination reference voltage (DC) – command/address bus		0.49 × V_{DD} - 20mV	0.5 × V_{DD}	0.51 × V_{DD} + 20mV	V	4
I_{IN}	Input leakage current; Any input excluding ZQ; 0V ≤ V_{IN} ≤ 1.1V		–2	–	+2	µA	5
I_{ZQ}	Input leakage current; ZQ		–3	–	+3	µA	6, 7
$I_{I/O}$	Output leakage current; 0V ≤ V_{OUT} ≤ V_{DD}	DQ, DQS_t, DQS_c, ALERT_n	–4	0	+4	µA	7
$I_{I/O}$	Output leakage current; V_{OUT} = V_{DD}; DQ and ODT are disabled		–	–	5	µA	
$I_{I/O}$	Output leakage current; V_{OUT} = V_{SS}; DQ and ODT are disabled with ODT input HIGH		–	–	50	µA	
I_{VREFCA}	V_{REF} supply leakage current; V_{REFDQ} = V_{DD}/2 or V_{REFCA} = V_{DD}/2 (All other pins not under test = 0V)		–2	0	+2	µA	7

Notes:
1. V_{DDQ} balls on DRAM are tied to V_{DD}.
2. V_{PP} must be greater than or equal to V_{DD} at all times.
3. V_{REFCA} must not be greater than 0.6 x V_{DD}. When V_{DD} is less than 500mV, V_{REF} may be less than or equal to 300mV.
4. V_{TT} termination voltages in excess of specification limit will adversely affect command and address signals' voltage margins, and reduce timing margins.

5. Command and address inputs are terminated to $V_{DD}/2$ in the registering clock driver. Input current is dependent on terminating resistance selected in registering clock driver.
6. Tied to ground. Not connected to edge connector.
7. Multiply by number of DRAM die on module.

The NVDIMM consists of many devices with differing temperature specifications. It is the responsibility of the system designer to ensure the temperature specifications are maintained for all devices.

Table 10: Thermal Characteristics

Device	Parameter/Condition	Temp	Units	Notes
DRAM	DRAM case temperature, measured at the center top of die. The DRAM consumes power in all modes as per I_{DD} tables in Micron's DDR4 component data sheets. The memory bus operates at a lower frequency during backup and restore operations and therefore dissipates less power than it does when operating in bypass mode.	T_{CASE}	0 to 85°C	1, 2, 3
		T_{CASE}	>85 to 95°C	1, 2, 3, 4
		$T_{JUNCTION}$	0 to100°C	
		ΘJC	4.2°C/watt	
NAND Flash	NAND Flash is utilized during backup and restore operations. The NAND Flash is not utilized during bypass mode, therefore making temperature specifications relatively simple to maintain.	T_{CASE}	0 to 80°C	1, 2, 3
		$T_{JUNCTION}$	0 to 85°C	
		ΘJC	0.7°C/watt	
FPGA (NV Controller)	Powered during bypass mode and only fully utilized during a restore or backup operation. DRAM bus is operated at a lower clock frequency during backup and restore operations.	T_{CASE}	Not specified	1, 2, 3
		$T_{JUNCTION}$	85°C MAX	5
		ΘJC	3.25°C/watt	5
PSOC (NV Controller)	Powered during bypass mode and only fully utilized during a restore or backup operation. DRAM bus is operated at a lower clock frequency during backup and restore operations.	T_{CASE}	Not specified	1, 2, 3
		$T_{JUNCTION}$	–40 to 100°C	5
		ΘJC	13°C/watt	5
NOR	Holds the code and fabric for the NV controller. Utilized during initialization.	T_{CASE}	Not specified	1, 2, 3
		$T_{JUNCTION}$	0 to 90°C	
		ΘJC	5°C/watt	
RCD	Resides on the command/address bus and consumes power in all modes. DRAM bus is operated at a lower frequency during backup and restore operations, therefore consuming less power.	T_{CASE}	0 to 103°C	1, 2, 3, 5
		$T_{JUNCTION}$	0 to 125°C	5

Notes:
1. Maximum operating case temperature. T_C is measured in the center of the device package.
2. A thermal solution must be designed to ensure the device does not exceed the maximum temperature during operation.
3. Device functionality is not guaranteed if the device exceeds the maximum temperature during operation.
4. If T_C exceeds 85°C, the DRAM device must be refreshed externally at 2X refresh (3.9µs interval refresh rate).
5. Devices not designed and manufactured by Micron are provided for reference only.

Table 11: LED Activity Table

LED	State	Function
D1 Green Power	On	Power is present at NV controller.
	Off	Power is not present at NV controller.
D2 Blue Save/Restore	Fast blink (on for 100ms/ off for 200ms)	When a CSAVE or a RESTORE operation is in progress.
	Slow blink (every 15 seconds)	Normal operation: Controller fabric and firmware have been loaded. NVDIMM is operational from host perspective.
D3 Amber User Defined	On/off	The state of this LED is user configurable. The host may write 0x01 to the LED register (page 0x0a, Offset 0x11) to turn the amber LED ON, and 0x00 to turn the amber LED off. Reading this register returns the state of the output register, not the buffered LED driver output.

Table 12: PowerGEM Proprietary Interface Connector (J1 and J2)

Pin	Signal Name	Signal Type	Description
1	PGM_SCL	Output	SMB clock for PGEM slave unit.
2	PGM_SDA	I/O	SMB data for PGEM slave unit.
3	Present/ discharge	I/O	This open drain signal is used by the NVDIMM to force the PowerGEM to begin discharging by driving LOW. A low voltage level detected by the NV controller on this pin indicates the PowerGEM is connected. A high voltage level indicates the PowerGEM is not connected.
4	Power_Fail_Int#	Input	Active LOW signal indicates input power is below defined threshold. Can be used as an alternative trigger for CSAVE. See PowerGEM data sheet.
5	V_{SS}	Supply	Ground.
6	12C/V_{DD_cap}	Supply	12V supply to PowerGEM from host. 12V supply from PowerGEM to NVDIMM when 12V rail is removed at host.

DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR4 component data sheets. Component specifications are available at micron.com. Module speed grades correlate with component speed grades, as shown below.

Table 13: Module and Component Speed Grades

DDR4 components may exceed the listed module speed grades; module may not be available in all listed speed grades

Module Speed Grade	Component Speed Grade
-3G2	-062E
-2G9	-068
-2G6	-075
-2G3	-083
-2G1	-093E

Design Considerations

Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

Operating voltages are specified at the edge connector of the module, not at the DRAM. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

I_{DD}, I_{PP}, and I_{DDQ} Specifications

I_{DD} and I_{PP} values are only for the DDR4 SDRAM and are calculated from values in the supporting component data sheet. I_{PP} and I_{DDQ} currents are not included in I_{DD} currents. I_{DD} and I_{DDQ} currents are not included in I_{PP} currents. Micron does not specify I_{DDQ} currents. In DRAM module application, I_{DDQ} cannot be measured separately because V_{DD} and V_{DDQ} use a merged power layer in the module PCB.

Certain I_{DD}/I_{PP} conditions must be derated for optional modes of operation, such as CA parity, DBI, write CRC, additive latency, geardown, CAL, 2X and 4X REF, and DLL disabled. Refer to the base device data sheet I_{DD} and I_{PP} specification tables for derating values for the applicable die revision.

I_{DD} Specifications

Table 14: DDR4 I_{DD} Specifications and Conditions – 32GB (Die Revision D, NVDIMM Designation PR)

Values are for the MT40A4G4 DDR4 TwinDie SDRAM only and are computed from values specified in the 16Gb (4 Gig x 4) component data sheet

Parameter	Symbol	2933	Units
One bank ACTIVATE-PRECHARGE current	I_{CDD0}	1386	mA
One bank ACTIVATE-PRECHARGE, wordline boost, I_{PP} current	I_{CPP0}	108	mA
One bank ACTIVATE-READ-PRECHARGE current	I_{CDD1}	1602	mA
Precharge standby current	I_{CDD2N}	1098	mA
Precharge standby ODT current	I_{CDD2NT}	1440	mA
Precharge power-down current	I_{CDD2P}	900	mA
Precharge quite standby current	I_{CDD2Q}	990	mA
Active standby current	I_{CDD3N}	1332	mA
Active standby I_{PP} current	I_{CPP3N}	108	mA
Active power-down current	I_{CDD3P}	1098	mA
Burst read current	I_{CDD4R}	2880	mA
Burst write current	I_{CDD4W}	2844	mA
Burst refresh current (1x REF)	I_{CDD5R}	1602	mA
Burst refresh I_{PP} current (1x REF)	I_{CPP5R}	144	mA
Self refresh current: Normal temperature range (0°C to 85°C)	I_{CDD6N}	1116	mA
Self refresh current: Extended temperature range (0°C to 95°C)	I_{CDD6E}	1296	mA
Self refresh current: Reduced temperature range (0°C to 45°C)	I_{CDD6R}	756	mA
Auto self refresh current (25°C)	I_{CDD6A}	310	mA
Auto self refresh current (45°C)	I_{CDD6A}	756	mA
Auto self refresh current (75°C)	I_{CDD6A}	1116	mA
Auto self refresh I_{PP} current	I_{CPP6X}	180	mA
Bank interleave read current	I_{CDD7}	4374	mA
Bank interleave read I_{PP} current	I_{CPP7}	396	mA
Maximum power-down current	I_{CDD8}	900	mA

Power Distribution

The NVDIMM consists of multiple subsystems that require several different voltage rails as described in the following table.

Device	Normal and Restore Operations	Back up or Save Operations
DDR4 DRAM	1.2V - V_{DD} supplied from edge connector	1.2V - regulated from 12V backup supply
DDR4 DRAM	2.5V - V_{PP} supplied from edge connector	2.5V - regulated from 12V backup supply
DDR4 DRAM	0.6V - V_{REF} supplied from edge connector	0.6V - regulated from 12V backup supply
DDR4 DRAM	0.6V - V_{TT} supplied from edge connector	0.6V - regulated from 12V backup supply
NAND	1.8V and 3.3V regulated from 12V rail	1.8V and 3.3V regulated from 12V backup supply
NOR FLASH	1.8V regulated from 12V rail	1.8V regulated from 12V backup supply
NV controller (FPGA)	0.6V, 1.0, 1.0V, 1.1V, 1.2V, 1.8V, 2.5V, 3.3V regulated from 12V rail	0.6V, 1.0V, 1.1V, 1.2V, 1.8V, 2.5V, 3.3V regulated from 12V backup supply
NV controller (PSOC)	2.5V - V_{DDSPD} supplied from edge connector	2.5V - regulated from 12V backup supply
RCD (registering clock driver)	1.2V - V_{DD} supplied from edge connector 2.5V - V_{DDSPD} supplied from edge connector	1.2V - regulated from 12V backup supply 2.5V - Regulated from 12V backup supply
Integrated data muxes	2.5V - V_{PP} supplied from edge connector	2.5V - regulated from 12V backup supply
SPD EEPROM/TS	2.5V - V_{DDSPD} supplied from edge connector	Not energized
VPD EEPROM	2.5V - V_{DDSPD} supplied from edge connector	2.5V - regulated from 12V backup supply

Registering Clock Driver Specifications

Table 15: Registering Clock Driver Electrical Characteristics

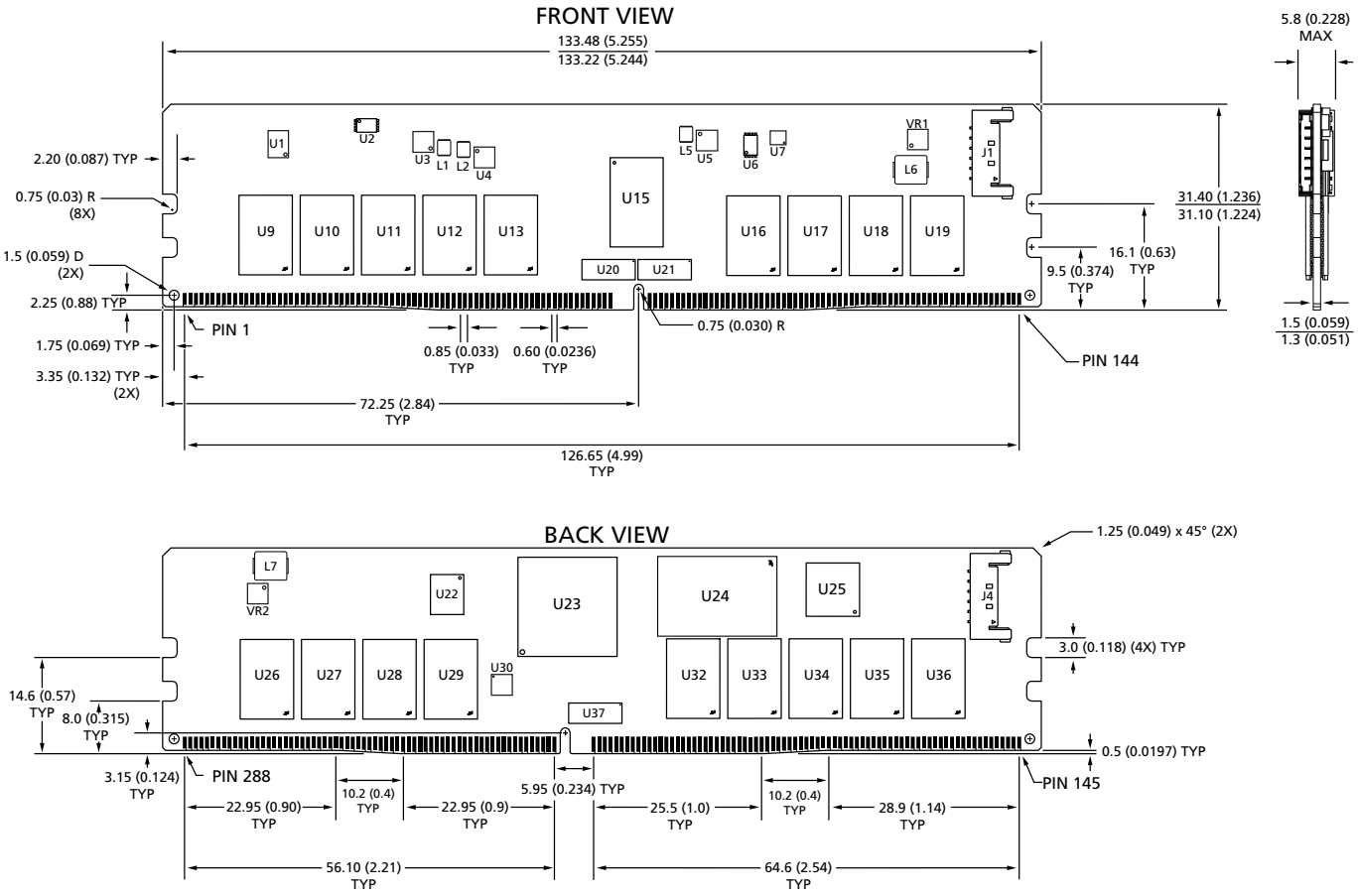
DDR4 RCD01 devices or equivalent

Parameter	Symbol	Pins	Min	Nom	Max	Units
DC supply voltage	V_{DD}	–	1.14	1.2	1.26	V
DC reference voltage	V_{REF}	V_{REFCA}	0.49 × V_{DD}	0.5 × V_{DD}	0.51 × V_{DD}	V
DC termination voltage	V_{TT}	–	V_{REF} - 40mV	V_{REF}	V_{REF} + 40mV	V
High-level input voltage	$V_{IH.\ CMOS}$	DRST_n	0.65 × V_{DD}	–	V_{DD}	V
Low-level input voltage	$V_{IL.\ CMOS}$		0	–	0.35 × V_{DD}	V
DRST_n pulse width	^{t}IN-IT_Pow-er_stable	–	1.0	–	–	µs
AC high-level output voltage	$V_{OH(AC)}$	All outputs except ALERT_n	V_{TT} + (0.15 × V_{DD})	–	–	V
AC low-level output voltage	$V_{OL(AC)}$		–	–	V_{TT} + (0.15 × V_{DD})	V
AC differential output high measurement level (for output slew rate)	$V_{OHdiff(AC)}$	Yn_t - Yn_c, BCK_t - BCK_c	–	0.3 × V_{DD}	–	mV
AC differential output low measurement level (for output slew rate)	$V_{OLdiff(AC)}$		–	–0.3 × V_{DD}	–	mV

Note: 1. Timing and switching specifications for the register listed are critical for proper operation of DDR4 SDRAM RDIMMs. These are meant to be a subset of the parameters for the specific device used on the module. See the JEDEC RCD01 specification for complete operating electrical characteristics. Registering clock driver parametric values are specified for device default control word settings, unless otherwise stated. The RC0A control word setting does not affect parametric values.

Module Dimensions

Figure 4: 288-Pin DDR4 NVDIMM



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.
3. Weight of module is approximately 25 grams.

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