M2S090TS-EVAL-KIT
SmartFusion2 Security Evaluation Kit

User Guide

Microsemi

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1 – Introduction

The SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) Security Evaluation Kit (M2S090TS-EVAL-KIT) is restriction of hazardous substances (RoHS) compliant and enables you to develop applications that involve the following:

- Data security
- Motor control
- System management
- Industrial automation
- High-speed serial I/O applications:
  - Peripheral component interconnect express (PCIe)
  - Serial gigabit media independent interface (SGMII)
  - User customizable serial interfaces

SmartFusion2 Security Evaluation Kit Contents

Table 1 lists the M2S090TS-EVAL-KIT contents.

Table 1 Kit Contents

Quantity	Description
1	SmartFusion2 Security Evaluation Board with the 90 K LE M2S090TS-1FGG484 device
1	12 V/2 A Wall-Mounted Power Adapter
1	FlashPro4 JTAG programmer
1	USB 2.0 A-Male to Mini-B cable for UART/power interface (up to 1 A) to PC
1	Quickstart Card
1	Free one-year Libero SoC Platinum Software License (v11.5 or later)
1	PCIe Control Plane Demo Design already programmed on the device
Note: The SmartFusion2 device can be programmed using on board SPI Slave (FlashPro5) mode or external FlashPro4 programmer. SoftConsole debugging cannot be performed using SPI Slave mode. FlashPro4 programmer is required to develop/debug the embedded applications with SoftConsole, Identity, or SmartDebug tool.	

SmartFusion2 Security Evaluation Kit Web Resources

M2S090TS-EVAL-KIT web resources are available at:

www.microsemi.com/products/fpga-soc/design-resources/dev-kits/SmartFusion2/smartfusion2-evaluation-kit#overview

Board Description

The M2S090TS-EVAL-KIT offers a full-featured Evaluation Board for SmartFusion2 SoC FPGAs. This board has the following features integrated on a single chip:

- Reliable flash-based FPGA fabric
- 166 MHz ARM® Cortex®-M3 processor
- Advanced security processing accelerators
- Digital signal processing (DSP) blocks

- Static random-access memory (SRAM)
- Embedded non-volatile memory (eNVM)
- High-performance communication interfaces

The SmartFusion2 Security Evaluation board has numerous standard interfaces such as:

- An RJ45 for 10/100/1000 Ethernet
- One full-duplex serializer/deserializer (SERDES) lane through sub-miniature version A (SMA) connectors
- A 64-bit GPIO Header
- Various connectors for serial peripheral interface (SPI) support

The SmartFusion2 memory management system supports 512 Mb on-board low-power double data rate (LPDDR) SDRAM memory and 64 Mb SPI flash memory. The SERDES block can be accessed using the PCIe edge connector or high-speed SMA connectors.

The board supports the M2S090TS device in an FGG484 package. The PCB has eight layers and manufactured with FR4 dielectric material.

Block Diagram

Figure 1 shows the SmartFusion2 Security Evaluation Kit block diagram:

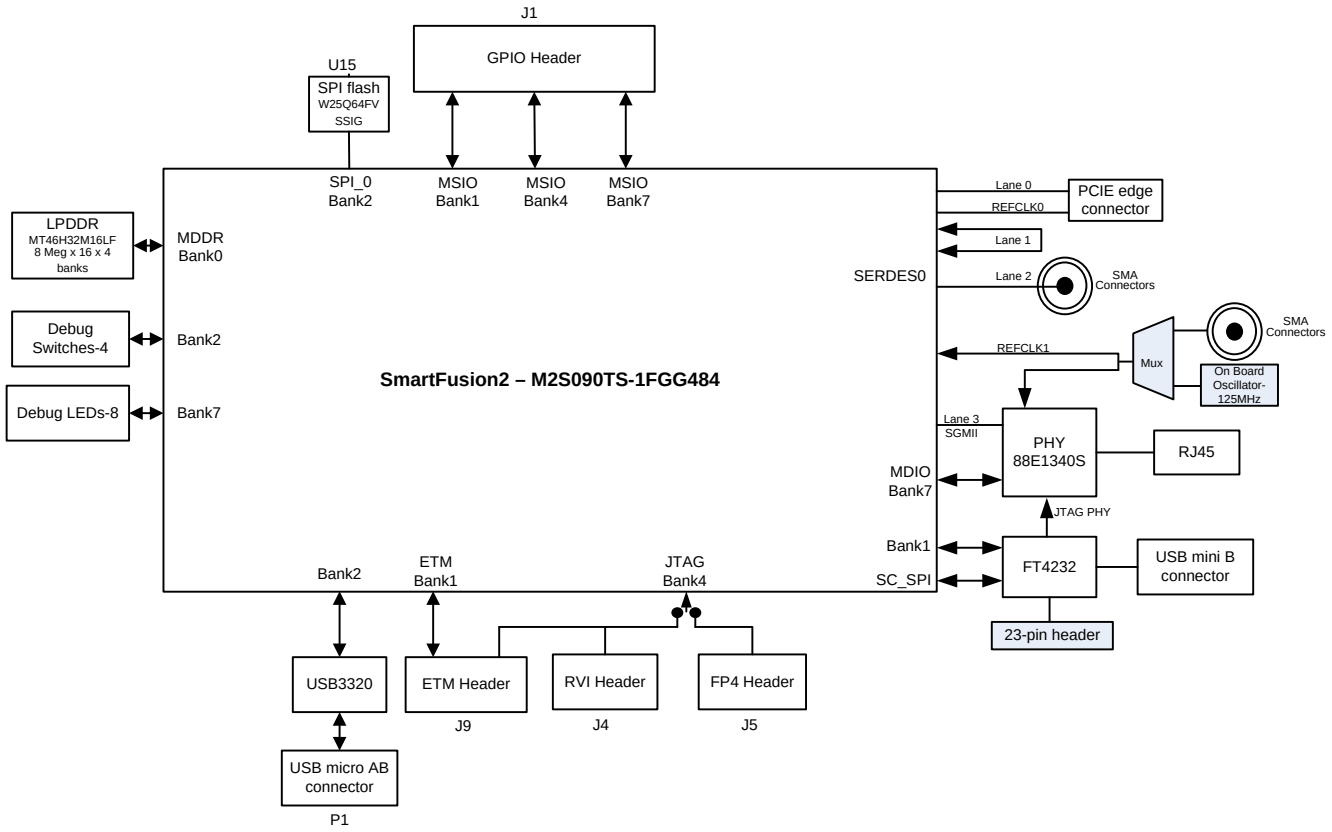

Figure 1 SmartFusion2 Security Evaluation Kit Block Diagram

Board Overview

Figure 2 shows the snapshot of the SmartFusion2 Security Evaluation board with engineering silicon.

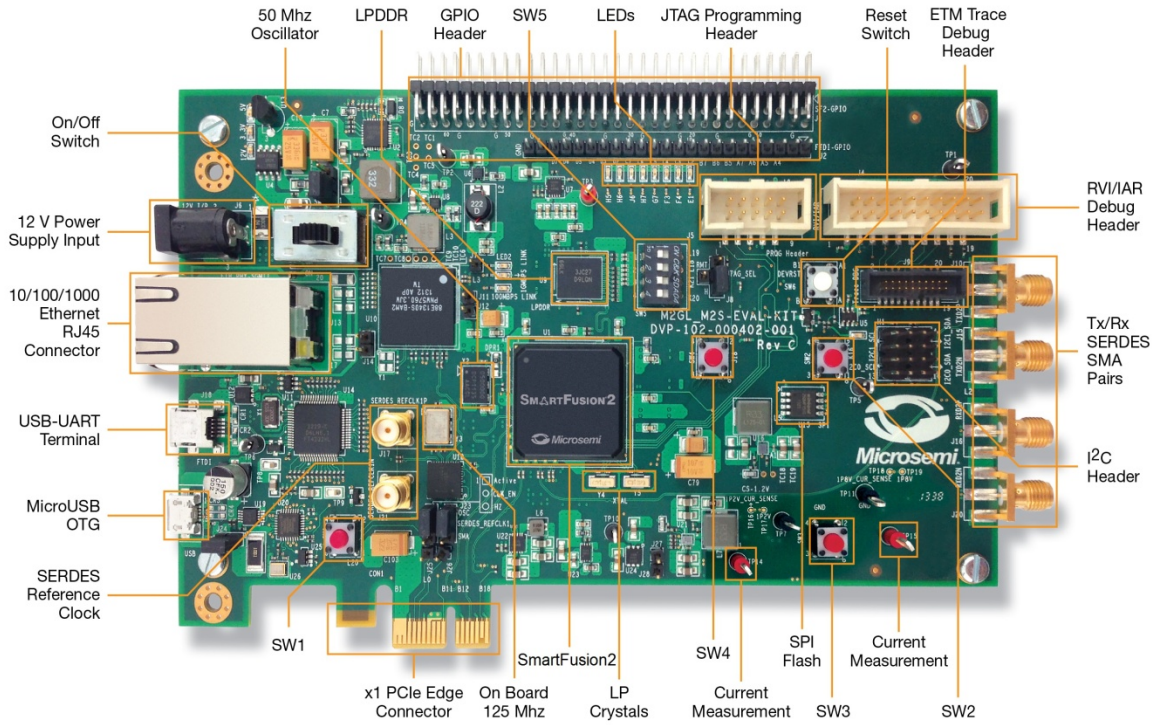

Figure 2 SmartFusion2 Security Evaluation Board

Note: Microsemi® recommends using SMA Male to SMA Male Precision Cable 12 Inch length using PE-SR405FLJ Coax, RoHS with SmartFusion2 Security Evaluation Kit. For more information, refer to www.pasternack.com/sma-male-sma-male-pe-sr405flj-cable-assembly-pe39429-12-p.aspx

Board Key Components

Table 2 shows key components of the SmartFusion2 Security Evaluation Kit.

Table 2 SmartFusion2 Security Evaluation Kit Components

Name	Description
SmartFusion2	M2S090TS-1FGG484 with data security feature
On Board 125 MHz	125 MHz clock oscillator(differential output)
x1 PCIe edge connector	PCI Express edge connector with one lane
SW1, SW2, SW3, and SW4 switches	Push button switches for user interface debugging applications.
SERDES reference clock connectors	J17 and J21 - External clock is sourced through SMA connectors.
MicroUSB OTG	P1 - USB Micro AB connector, interfacing with the high-speed USB2.0 ULPI transceiver chip USB3320, interfacing with FPGA pins of the SmartFusion2 MSS.
USB-UART terminal	J18 - FTDI programmer interface to program the external SPI flash.
10/100/1000 Ethernet RJ45 Connector	J13 - RJ45 connector (Ethernet jack with magnetic) interfacing with Marvell 10/100/1000 BASE-T PHY chip 88E1340S in SGMII mode, interfacing with the Ethernet port of the SmartFusion2 MSS (on-chip MAC and external PHY).
12 V power supply input	J6 - The board is powered by a 12 V power source using an external +12 V/2 A DC jack.
On/Off Switch	SW7 - Power ON or OFF switch from external DC Jack, +12 V DC.
50 MHz Oscillator	50 MHz clock oscillator
Low-Power DDR (LPDDR)	512 Mb (MT46H32M16LF – 8 Meg x 16 x 4 banks) for storing the data bits.
GPIO header	J1 - General purpose input/output (GPIO) header for multi standard I/O (MSIO) signals to be routed.
SW5	Four DIP switches for test and navigation.
Light-emitting diodes (LEDs)	Eight active low LEDs that are connected to some of the user I/Os for debugging. Three active high LEDs that are used for power supply indication.
JTAG programming header	J5 - The SmartFusion2 device on the Evaluation Kit can be programmed using a FlashPro4 programmer. FlashPro4 can be used to program the SmartFusion2 device. Programming header for FlashPro4 programmer to program and debug the SmartFusion2 device.
Reset Switch	SW6 - Push-button system reset for the SmartFusion2 device.
Embedded trace macro (ETM) debug header	J9 - ETM header for debugging.
RVI/IAR debug header	J4 - RVI header for application programming and debugging with Keil ULINK or IAR J-Link.
Tx/Rx SERDES SMA pairs	J10 - SERDES0 TXD2 P J15 - SERDES0 TXD2 N J16 - SERDES0 RXD2 P J20 - SERDES0 RXD2 N
I^2C header	H1 - Two I^2C ports routed to header
Current measurement	TP14 - 1.2 V current sensing test point.
SPI flash	64 Mb SPI flash Winbond electronics W25Q64FVSSIG connected to SPI port 0 of the SmartFusion2 microcontroller subsystem (MSS).
LP crystals	Y4 and Y5 are 32.768 KHz crystal oscillators.

2 – Installation and Settings

Software Settings

Download and install the latest release of Microsemi Libero® System-on-Chip (SoC) software v11.5 or later from the Microsemi website and register for a free Platinum software one year license. The Libero v11.5 or later installer has FlashPro4 drivers. For instructions on how to install Libero and SoftConsole, refer to the *Libero Installation and Licensing Guide*.

For instructions on how to download and install Microsemi DirectCores, SGCores, and driver firmware cores, refer to *Installing IP Cores and Drivers User Guide*. These must be installed on the PC where the Libero software is installed while designing with Microsemi FPGAs.

Hardware Settings

Jumpers, Switches, LEDs, and DIP Switch Settings

The recommended default jumpers, switches, LEDs, and DIP switch settings are defined in Table 3 through Table 5.

- Table 3 Jumper Settings
- Table 4 LEDs
- Table 5 Test Points

Connect the jumpers with the default settings to evaluate the pre-programmed demo design. Table 3 shows the jumpers settings.

Note: Location of all the jumpers and test points are searchable in Figure 18 (page 42) and Figure 19 (page 43) of 5 – Board Components Placement section.

Table 3 Jumper Settings

Jumper	Description	Pin	Default Settings
J23	Jumper to select switch-side Mux inputs of A or B to the line side.	Pin 1-2 (Input A to the line side) that is on board 125 MHz differential clock oscillator output will be routed to line side.	Close
		Pin 2-3 (Input B to the line side) that is external clock required to source through SMA connectors to the line side.	Open
J22	Jumper to select the output enable control for the line side outputs.	Pin 1-2 (Line side output enabled)	Close
		Pin 2-3 (Line side output disabled)	Open
J24	Jumper to provide the VBUS supply to USB when using in Host mode.		Open
J8	JTAG selection jumper to select between RVI header or FlashPro4 header for application debug.	Pin 1-2 FP4 for SoftConsole/FlashPro	Close
		Pin 2-3 RVI for Keil ULINK™/IAR J-Link®	Open
		Pin 2-4 for Toggling JTAG_SEL signal remotely using GPIO capability of FT4232 chip.	Open
J3	Jumpers to select either SW2 input or signal ENABLE_FT4232 from FT4232H chip.	Pin 1-2 for Manual power switching using SW7 switch.	Close
		Pin 2-3 for Remote power switch using GPIO capability of FT4232 chip.	Open

Table 4 shows the power supply and Ethernet LEDs.

Table 4 LEDs

LED	Description
DS1 - Green	5 V rail.
DS2 - Green	3.3 V rail.
DS3 - Green	12 V power source.
DS5 - Green	Connected to parallel LED output port 0 (P0_LED[0]) of Marvell PHY.
DS4 - Green	Connected to parallel LED output port 0 (P0_LED[2]) of Marvell PHY.
DS6 - Green	Connected to parallel LED output port 0 (P0_LED[3]) of Marvell PHY.

Table 5 shows the USB, ground, and other test points.

Table 5 Test Points

Test Point	Description
TP8	USB switch I/O for DP signal.
TP9	USB switch I/O for DM signal.
TP1, TP2, TP4, TP5, TP6, TP7, TP10, TP11	GND
TP3	Test point for DDR_VTT
TP12	Test point to measure the voltage at TP12 with reference to GND.
TP14	1.2 V current sensing test point
TP15	1.8 V current sensing test point
TP16, TP17	Test points across current sense resistor 0.05 Ohms for 1.2 V
TP18, TP19	Test points across current sense resistor 0.05 Ohms for 1.8 V

SmartFusion2 Power Sources

All the power supply devices used in the SmartFusion2 Security Evaluation Kit are Microsemi devices. For more information on power supply devices refer to www.microsemi.com/product-directory/ics/853-power-management

Figure 3 shows Voltage rails (12 V, 5 V, 3.3 V, 2.5 V, 1.8 V, 1.5 V, and 1.0 V) available in the SmartFusion2 Security Evaluation Kit.

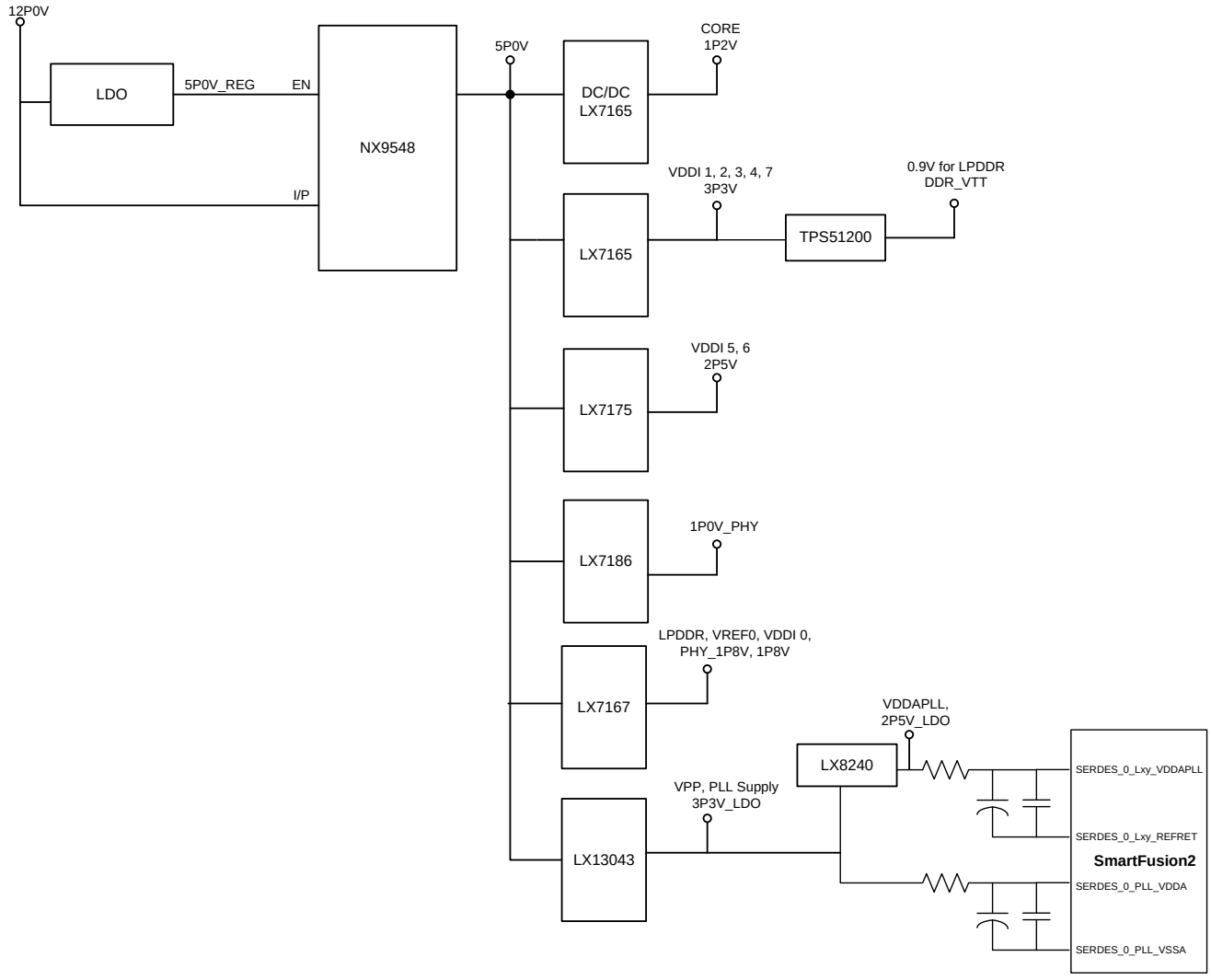

Figure 3 Voltage Rails in the SmartFusion2 Security Evaluation Kit

I/O Voltage Rails

Table 6 shows the major power supplies for normal operation of the SmartFusion2 Security Evaluation Kit.

Table 6 I/O Voltage Rails

SmartFusion2 Bank	I/O Rail	Voltage
Bank0	VDDI0	1.8 V
Bank2	VDDI2	3.3 V
Bank3	VDDI3	3.3 V
Bank4	VDDI4	3.3 V
Bank5	VDDI5	3.3 V
Bank6	VDDI6	2.5 V
Bank7	VDDI7	2.5 V
Bank 8	VDDI8	3.3 V

3 – Key Components Description and Operation

This section describes the key component interfaces of the SmartFusion2 Security Evaluation Kit. For device datasheets, refer to: http://www.microsemi.com/products/fpga-soc/design-resources/dev-kits/smartfusion2-kits

Powering Up the Board

The board is powered by a 12 V source using an external +12 V/2 A DC jack or PCIe connector, as shown in Figure 4. Protection mechanism enables the external DC jack supply.

When both the power sources are ON, board takes power from the external DC jack as Diode D3 becomes reverse biased and path will be open for 12P0_PCIE. When the external DC voltage is not present, the board can be powered up using the PCIe connector.

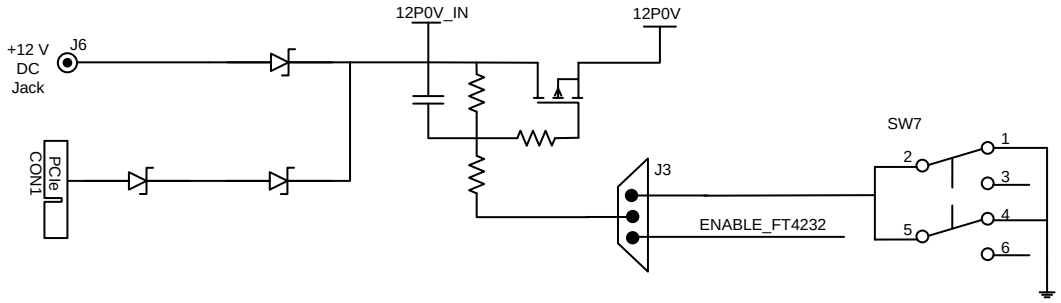

Figure 4 Powering Up the Board

Current Measurement

1.2 V Current Sensing for Normal Operation

For applications which require current measurement, a high precision operational amplifier circuitry (U31 with gain 100) is provided on the board to measure the output voltage at test point TP14.

The following steps describe how to measure the core power:

1. Measure the output voltage (V_{OUT}) at TP14.
2. I = (V_{OUT}/5)
3. Core power consumed, P= (1.2 V)*I

For example, when the voltage measured across TP14 is 0.5 V then the consumed core power is 0.12 W.

Figure 5 shows the on board core power measurement circuitry.

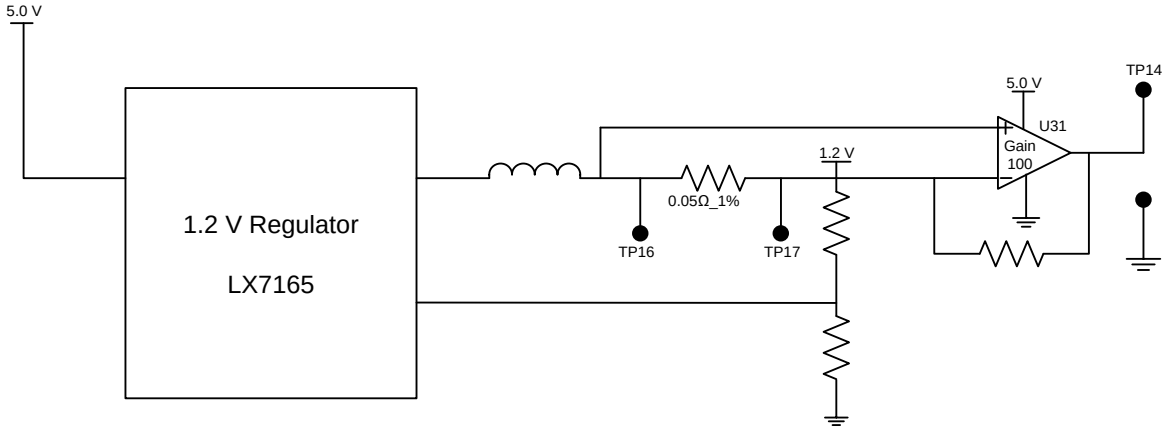

Figure 5 Core Power Measurement Circuitry

1.2 V Current Sensing for Flash*Freeze

The SmartFusion2 device consumes very less power in Flash*Freeze mode. The voltage across the sense resistor (0.05 Ω) must be measured directly using a precision digital multi-meter that can read sub milli-volts. Use TP16 and TP17 test points to directly measure the voltage across the 1.2 V sense resistor.

To convert the voltage measured across sense resistor to power, use the following equation:

$$Power = (\frac{\text{voltage\_measured\_in\_milli\_volts}}{0.05}) * 1.2$$

EQ1

Note: Accuracy is ± 10%.

1.8 V Current Sensing

For applications which require current measurement, a high precision Operational Amplifier circuitry (U32 with gain 100) is provided on the board to measure the output voltage at test point TP15.

The following steps describe how to measure the core power:

1. Measure the output voltage (V_{OUT}) at TP15.
2. I = (V_{OUT}/5)
3. Core power consumed, P = (1.8 V)*I

For example, when the voltage measured across TP15 is 0.5 V then the consumed core power is 0.18 W.

Figure 6 shows the on board 1.8 V power measurement circuitry.

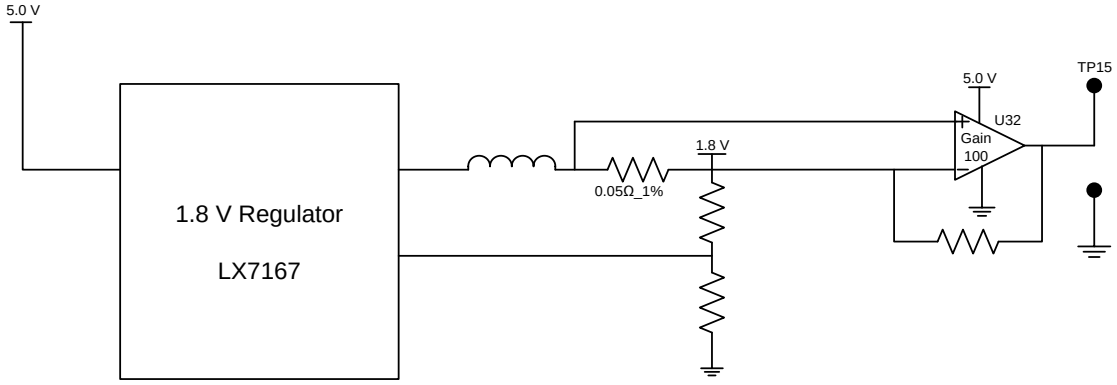

Figure 6 1.8 V Power Measurement Circuitry

Note: Accuracy is ± 10%.

Memory Interface

Dedicated I/Os are provided for the MSS DDR and fabric DDR for the SmartFusion2 device. Apart from the dedicated I/Os, regular I/Os can also be used to connect to other memory devices. Refer to Figure 7.

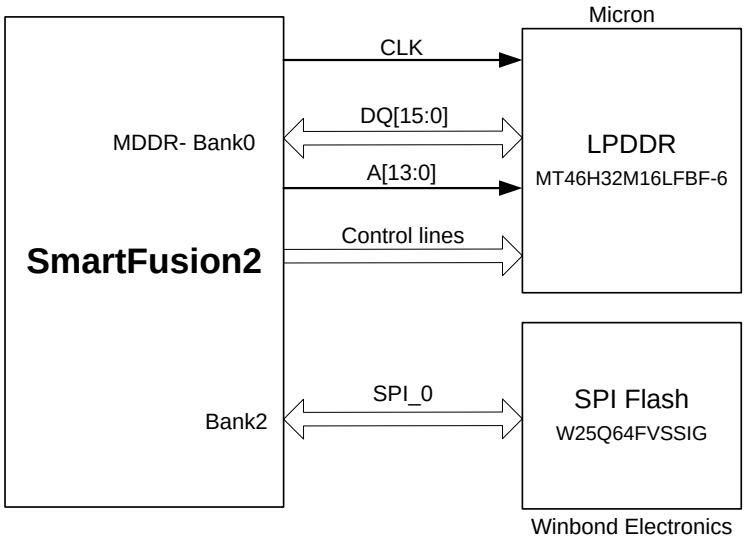

Figure 7 SmartFusion2 Memory Interface

LPDDR SDRAM

An individual chip with 512 Mb LPDDR SDRAM memory is provided as flexible volatile memory for user applications. The LPDDR interface is implemented in bank 0.

Following are the LPDDR SDRAM specifications:

- MT46H32M16LF – 8 Meg x 16 x 4 banks
- Density: 512 Mb
- Data rate: LPDDR 16-bit at 400 Mbps = 6.4 Gbps

Note: For more information, refer to page 3 of Board Level Schematics document (provided separately).

SPI Serial Flash

Following are the SPI Flash specifications:

- Density: 64 Mb
- Voltage: 2.7 V - 3.6 V
- Frequency: 104 MHz
- Supports: SPI modes 0 and 3
- SmartFusion2 MSS - SPI0 interfaced to SPI flash

Note: For more information, refer to page 8 of Board Level Schematics document (provided separately).

SERDES0 Interface

The SERDES0 has four lanes connected as below:

1. Lane 0 is directly routed to the PCIe connector.
   - TX Pad → trace → AC Coupling→trace → via (to bottom layer) → trace → PCIe connector pad
   - RX Pad → trace → PCIe connector pad
2. Lane 1 is used for loopback testing. This path is routed between the TX and RX pads with a 6 inch trace and 2 vias.
   - TX Pad → via (to Bottom layer) → trace → AC Coupling → trace → via (to top layer) → RX pad
3. Lane 2 routed to SMA connectors.

- TX Pad → trace → AC Coupling→trace → SMA connector pad
- RX Pad → trace → via (to bottom layer) → trace → via (to top layer) → SMA connector Pad

4. Lane 3 is routed to Marvell PHY (88E1340S).
   - TX pad → trace→ AC Coupling → trace → via → trace routed in (6th layer) → via (to top layer) → Marvel PHY pin
   - RX pad → via → trace routed in 6th layer → via (to top layer) → trace → AC Coupling → trace → Marvel PHY pin

The SERDES0 reference clock 0 is routed directly from the PCIe connector to the SmartFusion2 device.

The SERDES0 reference clock 1 is routed from the onboard 125 MHz clock oscillator and optionally routed from SMA connectors through LVDS Mux/Buffer chip.

Expected SERDES reference clock specifications:

- Voltage level: 3.3 (± 0.3)V
- Differential LVDS
  - Symmetry: 50% (± 10%)
  - Rise/Fall Time: 1 ns Max @ 20% to 80% of supply (3.3 V)
  - Output Voltage Levels: 0 = 0.90 Minimum, 1.10 Typical
    1 = 1.43 Typical, 1.60 Maximum
  - Differential Output Voltage: 247 mV Minimum, 454 mV Maximum

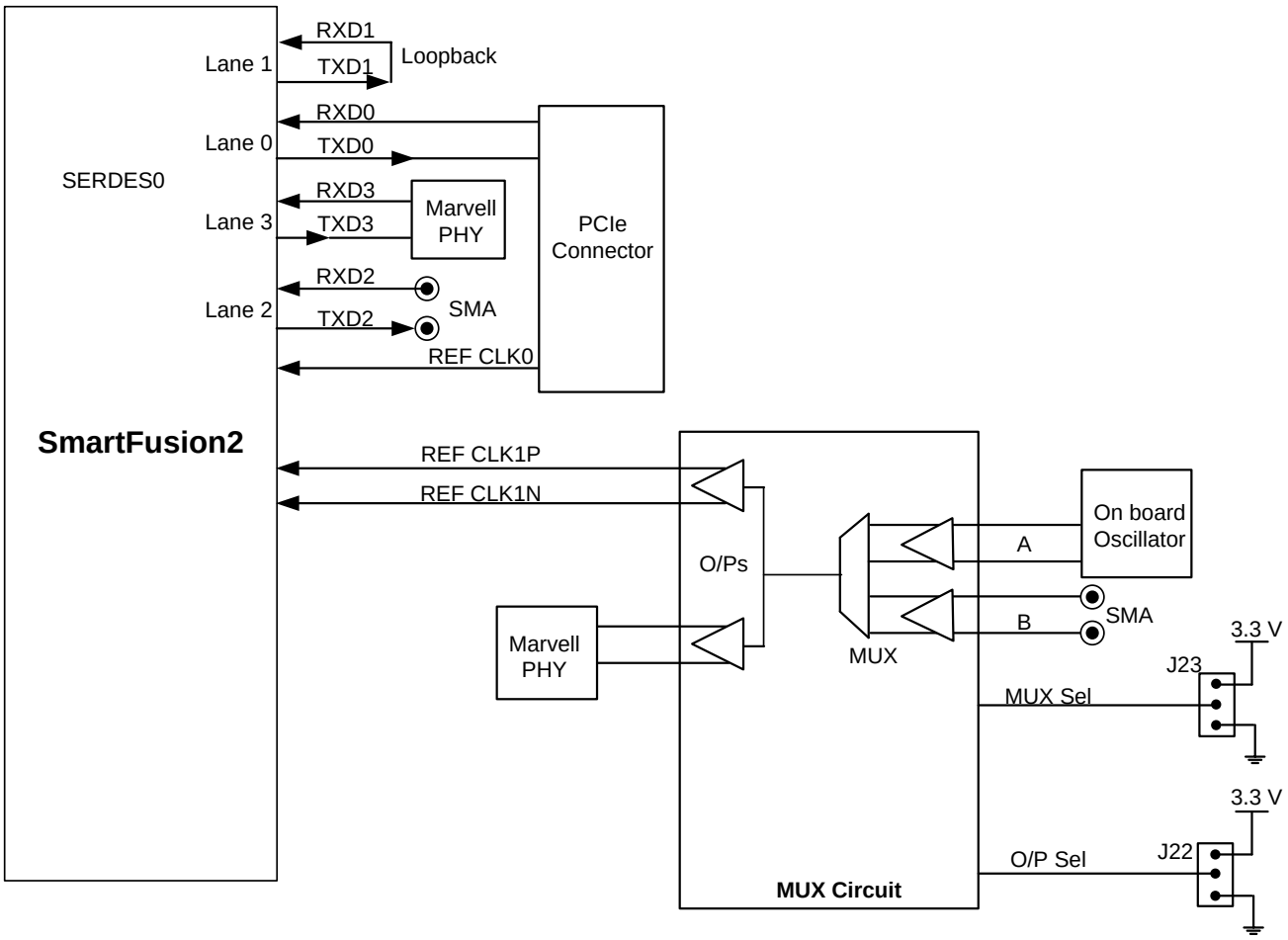

Figure 8 SERDES0 Interface

For more information on J22 and J23 jumpers, refer to Table 3.

Note:

- SERDES0 TXD pairs are capacitively coupled to the SmartFusion2 device. Series AC coupling capacitors are used to provide common mode voltage independence.
- The AC coupling capacitors are not provided for SERDES 0 RXD signals. The mating board must have the AC coupling capacitors.
- For more information, refer to page 4 of Board Level Schematics document (provided separately).

USB Interface

The SMSC USB3320 is a high-speed USB 2.0 ULPI transceiver. It supports the optional OTG protocol.

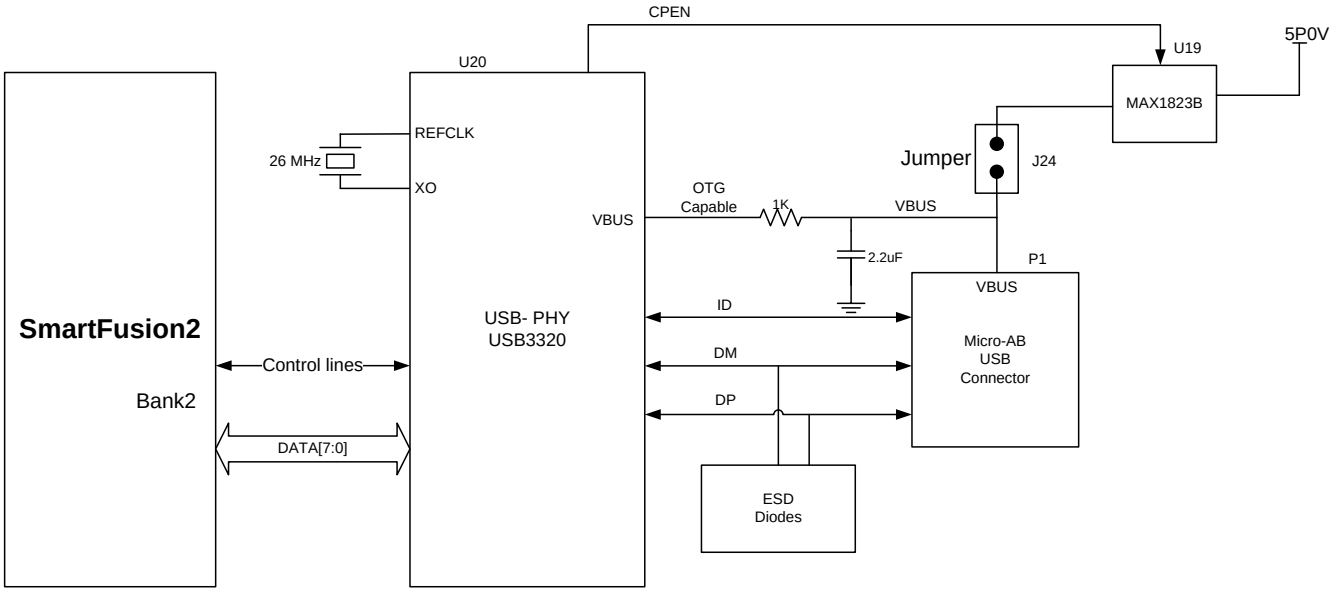

Figure 9 USB Interface

Note: For more information, refer to page 10 of Board Level Schematics document (provided separately).

Marvell PHY (88E1340S)

The SmartFusion2 Security Evaluation Kit uses the Marvell Alaska PHY device (88E1340S) for Ethernet communications at 10/100/1000 Mbps. The 88E1340S device has four independent Giga Bit Ethernet transceivers. However, the board uses only one transceiver. Each transceiver performs all the physical layer functions for 10BASE-T, 100BASE-TX, and 1000BASE-T full-duplex or half-duplex Ethernet on the CAT5 twisted pair cable. The PHY device is connected to a user-provided Ethernet cable through an RJ45 connector with built-in magnetics.

The 88E1340S device supports the quad SGMII for direct connection to a SmartFusion2 chip. Refer to Figure 10. It is configured through the CONFIG [3:0] and CLK_SEL [1:0] registers.

CLK_SEL [1:0] is used to select the reference clock input option. On board, the status of the CLK_SEL0 register is High and CLK_SEL1 is Low. REF_CLK is the 125 MHz reference differential clock input. It consists of LVDS differential inputs with a 100 Ω differential internal termination resistor.

- RCLK – Giga Bit recovered clock
- SCLK – 25 MHz synchronous input reference clock
- Expected reference clock (REF_CLK) specifications
  - Voltage level: 3.3 (± 0.3)V
  - Differential LVDS
    - Symmetry: 50% (± 10%)
    - Rise/Fall Time: 1 ns Max - 20% to 80% of supply (3.3 V)
    - Output Voltage Levels: 0 = 0.90 Minimum, 1.10 Typical
      1 = 1.43 Typical, 1.60 Maximum
    - Differential Output Voltage: 247 mV Minimum, 454 mV Maximum

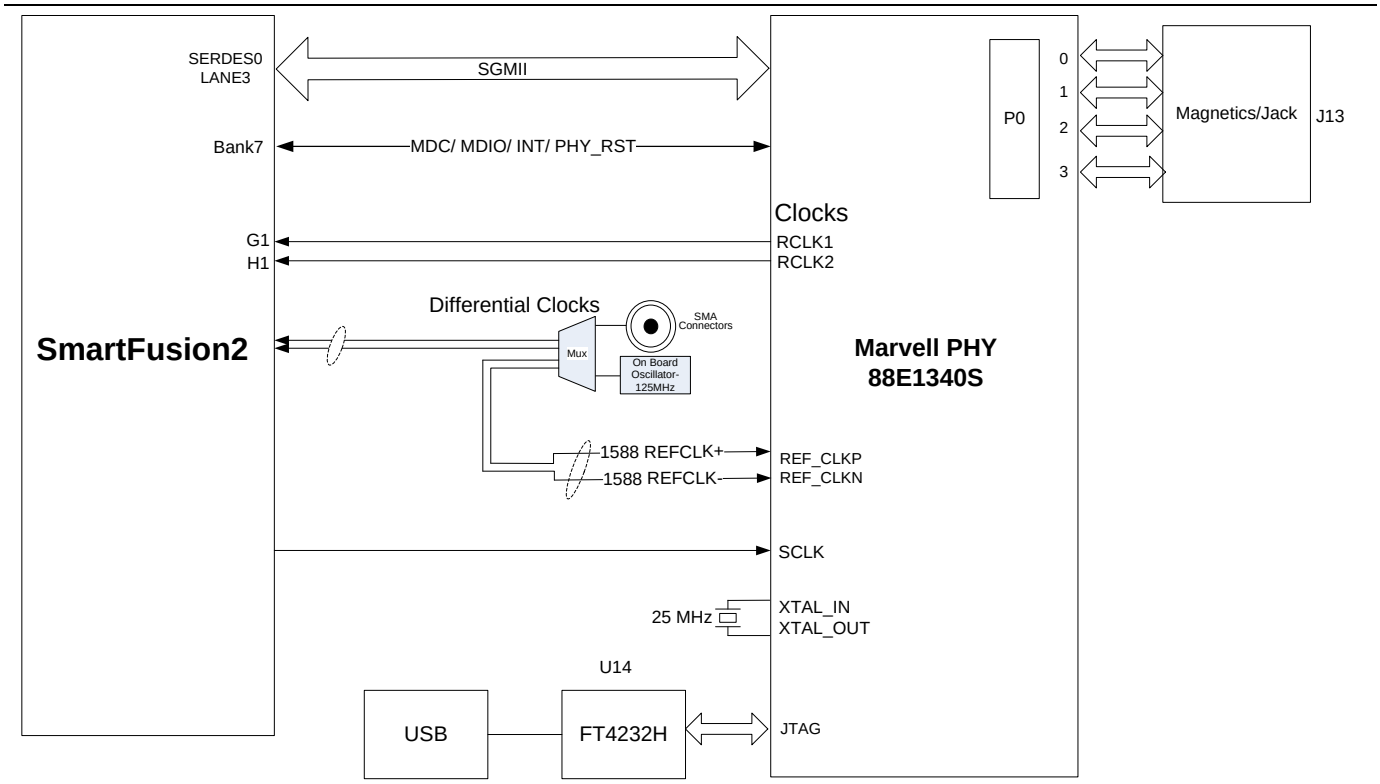

Figure 10 SmartFusion2 Marvell PHY Interface

Note: For more information, refer to page 11 and 12 of Board Level Schematics document (provided separately).

Programming

The SmartFusion2 device can be programmed through the SPI Slave/JTAG interface. Figure 11 shows various ways of SmartFusion2 programming. Refer to Appendix 2 – FPGA Programming using FlashPro4 section for programming the device using SPI Slave interface.

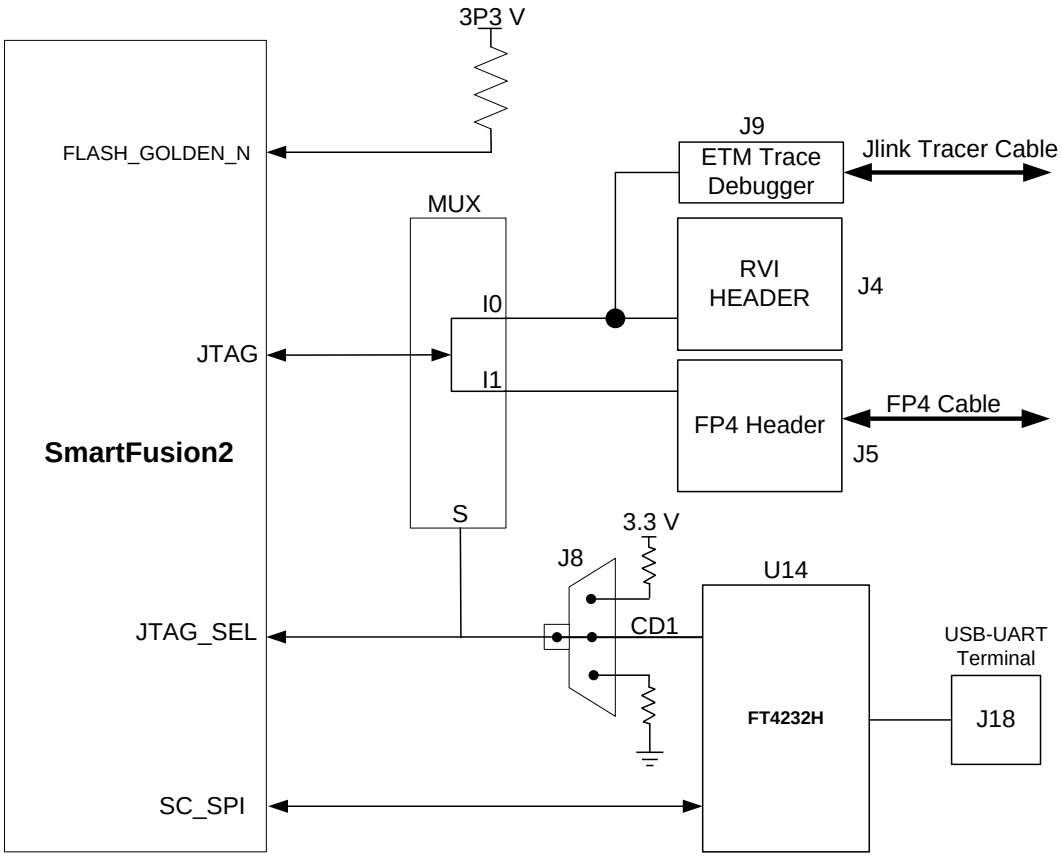

Figure 11 SmartFusion2 Programming Interface

JTAG_SEL: JTAG_SEL is used to switch between FlashPro4 header (High) and RVI header or ETM header (Low). For more information on J8 jumper, refer to Table 3.

RVI Header: A 10×2 RVI header is provided on the board for debugging. This header allows plugging in the Keil ULINK debugger or IAR J-Link debugger.

FlashPro4 Programming Header: The SmartFusion2 device on the Evaluation Kit can be programmed using on board SPI Slave (FlashPro5) or external FlashPro4 programmer. In addition, the FlashPro4 programmer is used to debug the software using SoftConsole.

Note:

- For more information, refer to page 13 of Board Level Schematics document (provided separately).
- For more details, refer to the *SmartFusion2 Programming User Guide*.

FTDI Interface

Following are the FT4232H chip features:

- USB 2.0 high-speed (480 Mbps) to UART/MPSSE IC.
- Single-chip USB to quad serial ports with different configurations.
- Entire USB protocol is handled on the chip. USB specific firmware programming is not required.
- USB 2.0 high-speed (480 Mbps) and full Speed (12 Mbps) compatible.
- Two MPSSE on channel A and channel B, to simplify synchronous serial protocol (USB to JTAG, I2C, SPI, or bit-bang) design.
- Fully assisted hardware or X-On or X-Off software handshaking.
- +1.8 V (chip core) and +3.3 V I/O interfacing (+5 V tolerant).

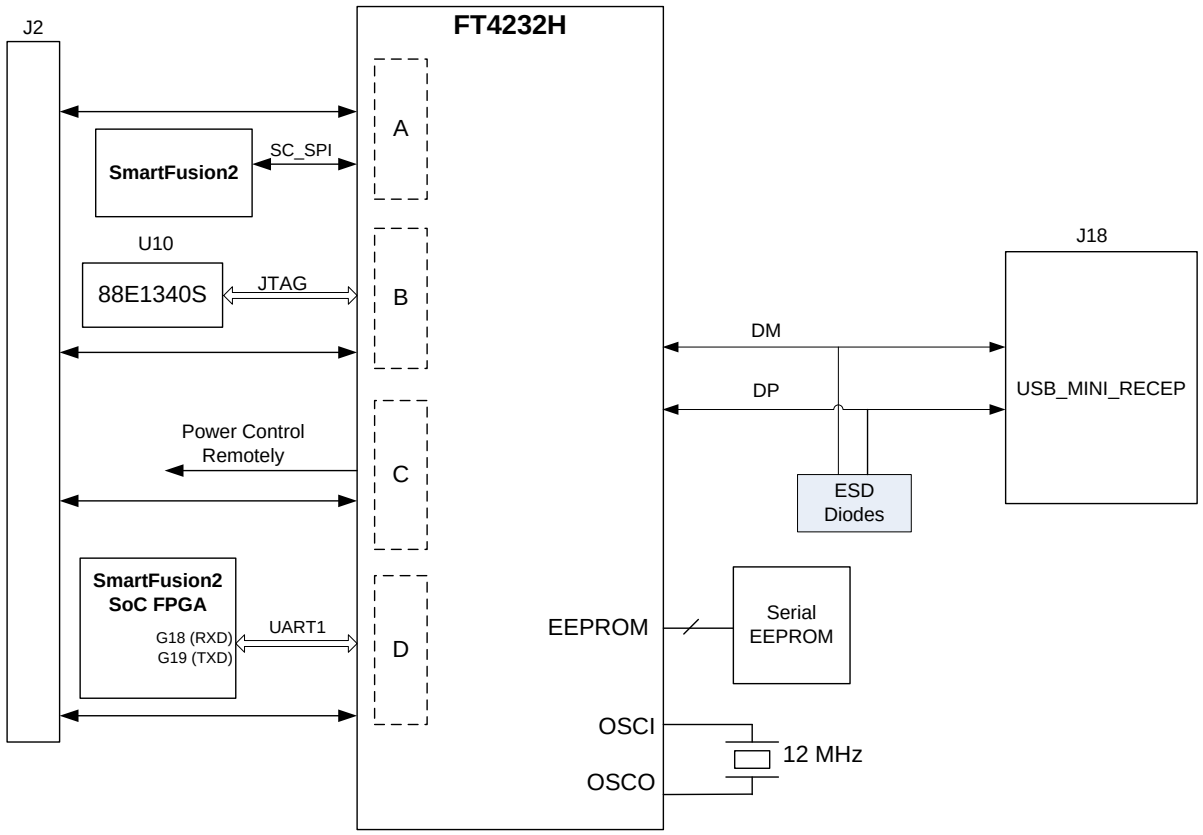

Figure 12 FTDI Interface

Note: For more information, refer to page 14 of Board Level Schematics document (provided separately).

I2C Port Header

Table 7 shows the two I2C ports routed to header – H1:

Table 7 I2C Port Header

Pin Number	SmartFusion2 Pin Name	Board Signal Name	Header - H1
G16	MSIO61NB2/I2C_0_SCL/GPIO_31_B/USB_DATA1_C	I2C0_SCL	10, 14
G17	MSIO61PB2/I2C_0_SDA/GPIO_30_B/USB_DATA0_C	I2C0_SDA	11, 15
R22	MSIO11NB3/CCC_NE1_CLKI0/I2C_1_SCL/GPIO_1_A/USB_DATA4_A	I2C1_SCL	2, 6
P22	MSIO11PB3/CCC_NE0_CLKI0/I2C_1_SDA/GPIO_0_A/USB_DATA3_A	I2C1_SDA	3, 7

Note: For more information, refer to page 8 of Board Level Schematics document (provided separately).

System Reset

The DEVRST_N signal (active low) is asserted in the following cases:

- When you press the SW6 (push-button switch) switch
- When the power supply level 3.3 V or 1.2 V falls below the threshold level

DEVRST_N is an input-only reset pad that allows assertion of a full reset to the chip at any time.

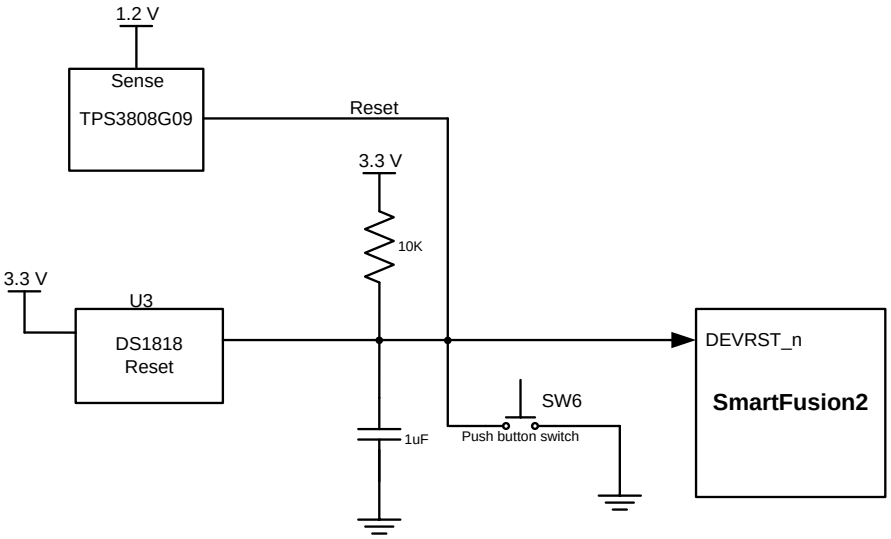

Figure 13 System Reset Interface

Note: For more information, refer to page13 of Board Level Schematics document (provided separately).

Clock Oscillator

50 MHz Clock Source

A 50 MHz clock oscillator with an accuracy of +/-50 ppm is available on the board, refer to Figure 14. This clock oscillator is connected to the FPGA fabric to provide a system reference clock.

An on-chip SmartFusion2 PLL can be configured to generate a wide range of high precision clock frequencies.

Table 8 50 MHz Clock

SmartFusion2 Security Evaluation Kit	SmartFusion2 - Package No	SmartFusion2 Pin Name
50MHZ_ SECLK_ WST_K1	K1	MSIOD178PB7/CCC_SW0_CLKI0

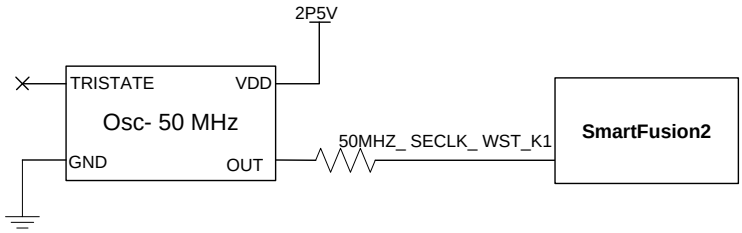

Figure 14 50 MHz Clock Oscillator Interface

Note: For more information, refer to page 6 of Board Level Schematics document (provided separately).

Different Clock Sources

Following are the different clock sources used in the SmartFusion2 Security Evaluation Kit:

- 125 MHz clock oscillator. For more information refer to SERDES0 Interface.
- 32.768 KHz crystal oscillators for main and auxiliary oscillators of SmartFusion2.

User Interface

User LEDs

The board has eight active low LEDs, which are connected to the SmartFusion2 device. Table 9 shows the on board user LEDs.

Table 9 LEDs

SmartFusion2 Security Evaluation Board Pin	SmartFusion2 - Package Pin Number	SmartFusion2 Device Pin Name
LED0 - Yellow	E1	MSIO143PB8
LED1 – Yellow	F4	MSIO145NB8
LED2 – Green	F3	MSIO145PB8
LED3 – Green	G7	MSIO146NB8
LED4 – Red	H7	MSIO146PB8
LED5 – Red	J6	MSIO148NB8
LED6 – Blue	H6	MSIO148PB8

SmartFusion2 Security Evaluation Board Pin	SmartFusion2 - Package Pin Number	SmartFusion2 Device Pin Name
LED7 - Blue	H5	MSIO150NB8

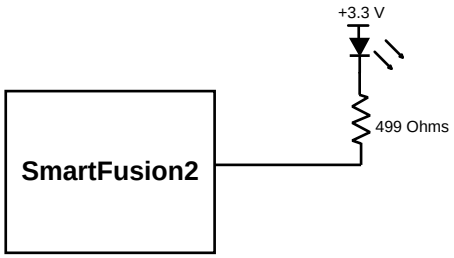

Figure 15 LEDs Interface

Note: For more information, refer to page 15 of Board Level Schematics document (provided separately).

Push-Button Switches

The SmartFusion2 Security Evaluation Kit comes with five push-button tactile switches that are connected to the SmartFusion2 device. Table 10 shows the on board push-button switches.

Table 10 Push-Button Switches

SmartFusion2 Security Evaluation Board Pin	SmartFusion2 - Package Pin Number	SmartFusion2 Device Pin Name
SWITCH1	L20	MSIO17NB3/SPI_1_SS0/GPIO_13_A
SWITCH2	K16	MSIO23NB3/SPI_1_SS1/GPIO_14_A
SWITCH3	K18	MSIO24PB3/SPI_1_SS2/GPIO_15_A
SWITCH4	J18	MSIO24NB3/SPI_1_SS3/GPIO_16_A
SW6	R15	DEVRST_N

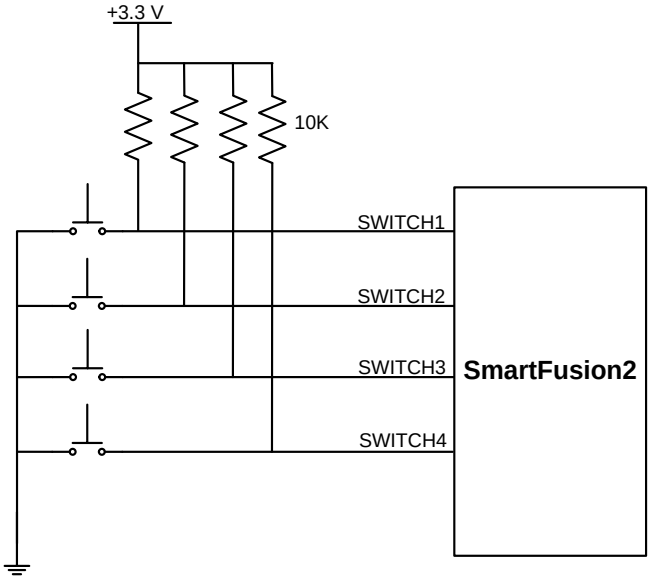

Figure 16 Switches Interface

Note: For more information, refer to page 15 of Board Level Schematics document (provided separately).

Slide Switches–DPDT

SW7 - Power ON or OFF switch from external DC Jack, +12 V DC.

DIP Switch- SPST

SW5 - A DIP switch that has four connections to the SmartFusion2 device. Table 11 shows the onboard DIP switches.

Table 11 DIP Switches

SmartFusion2 Security Evaluation Board Pin	SmartFusion2 - Package Pin Number	SmartFusion2 Device Pin Name
DIP1	L19	MSIO18PB3/SPI_1_SS4/GPIO_17_A
DIP2	L18	MSIO18NB3/SPI_1_SS5/GPIO_18_A
DIP3	K21	MSIO19PB3/SPI_1_SS6/GPIO_23_A
DIP4	K20	MSIO19NB3/SPI_1_SS7/GPIO_24_A

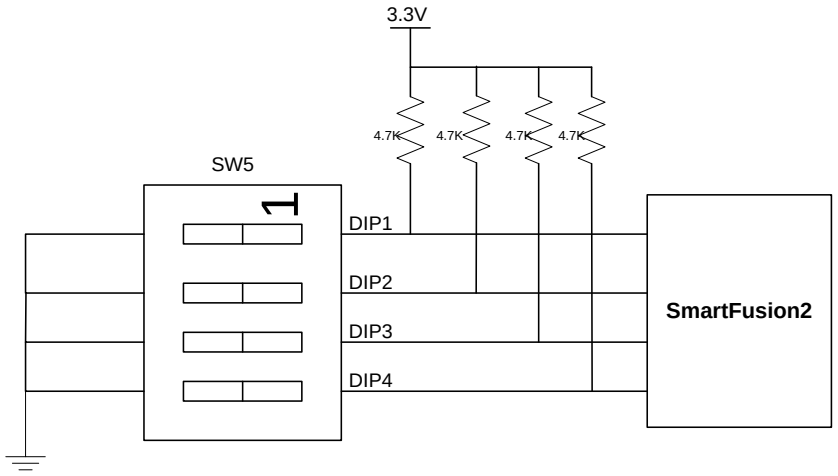

Figure 17 SPST Interface

Note: For more information, refer to page 15 of Board Level Schematics document (provided separately).

GPIO Header Pin Out

Bank 4, bank 7, and bank 1 signals are routed to the GPIO header for user applications. Table 12 shows the GPIO header pin out details.

Table 12 GPIO Header PinOut

GPIO Header-J1	SmartFusion2 – U1		GPIO Header-J1	SmartFusion2 – U1	
Pin Number	**Package Number**	**Pin Name**	**Pin Number**	**Package Number**	**Pin Number**
1	AB15	MSIO213PB5/VCCC_SE1_CLKI	2		3P3V
3	AA15	MSIO213NB5	4		VSS
5		VSS	6	AA16	MSIO222PB5
7	AB18	MSIO230PB5	8	AA17	MSIO222NB5

GPIO Header-J1	SmartFusion2 – U1		GPIO Header-J1	SmartFusion2 – U1	
Pin Number	**Package Number**	**Pin Name**	**Pin Number**	**Package Number**	**Pin Number**
9	AB19	MSIO230NB5	10		VSS
11		VSS	12	AB17	MSIO221PB5
13	Y18	MSIO228PB5	14	AA18	MSIO221NB5
15	Y19	MSIO228NB5	16		VSS
17		VSS	18	Y17	MSIO226PB5
19	W16	MSIO224PB5	20	W17	MSIO226NB5
21	V16	MSIO224NB5	22		VSS
23		VSS	24	U14	MSIO218PB5
25	C22	MSIO60PB2/MMUART_0_RXD/GPIO_28_B/USB_STP_C	26	U15	MSIO218NB5
27	B22	MSIO60NB2/MMUART_0_CLK/GPIO_29_B/USB_NXT_C	28		VSS
29		VSS	30	V13	MSIO211PB5
31	Y15	MSIO216PB5	32	V14	MSIO211NB5
33	W15	MSIO216NB5	34		VSS
35		VSS	36	G5	MSIO98PB8
37	F5	MSIO132PB8	38	G6	MSIO131NB8
39	F6	MSIO132NB8	40		VSS
41		VSS	42	E4	MSIO138PB8
43	C4	MSIO127PB8	44	E5	MSIO138NB8
45	D5	MSIO127NB8	46		VSS
47		VSS	48	C3	MSIO129PB8
49	B2	MSIO136PB8	50	B3	MSIO129NB8
51	A2	MSIO136NB8	52		VSS
53		VSS	54	C1	MSIO140PB8
55	D1	MSIO142PB8	56	B1	MSIO140NB8
57	D2	MSIO142NB8	58		VSS
59		VSS	60	D3	MSIO134PB8
61		3P3V	62	D4	MSIO134NB8
63		3P3V	64		VSS

4 – Pin List

Table 13 lists the pins for SmartFusion2 M2S090TS-FGG484 devices.

Note: *D21- Pin cannot be used as a fabric output and it is only an Input.

Table 13 Pin List update with latest of M2S090TS-FGG484

Package Pin	M2S090TS-FGG484 Pin Name
A1	VSS
A2	MSIO136NB8
A3	DDRIO99NB1
A4	DDRIO99PB1
A5	DDRIO98NB1
A6	DDRIO92NB1/GB4/CCC_NW1_CLKI2
A7	DDRIO89PB1/MDDR_DQ_ECC1
A8	DDRIO89NB1/MDDR_DQ_ECC0
A9	DDRIO87NB1/MDDR_DQ1
A10	DDRIO84PB1/MDDR_DM_RDQS0
A11	DDRIO84NB1/MDDR_DQ4
A12	DDRIO81PB1/MDDR_DQ8
A13	DDRIO81NB1/MDDR_DQ9
A14	DDRIO77PB1/GB12/CCC_NE1_CLKI2/MDDR_DQ12
A15	DDRIO77NB1/MDDR_DQ13
A16	DDRIO72PB1/MDDR_CLK
A17	DDRIO72NB1/MDDR_CLK_N
A18	DDRIO71PB1/MDDR_BA0
A19	DDRIO71NB1/MDDR_BA1
A20	DDRIO67NB1/MDDR_ADDR6
A21	DDRIO64PB1/MDDR_ADDR10
A22	VSS
AA1	VSS
AA2	SERDES_0_TXD0_N
AA3	VSS
AA4	SERDES_0_TXD1_N
AA5	VSS
AA6	SERDES_0_TXD2_N
AA7	VSS
AA8	SERDES_0_TXD3_N
AA9	VSS
AA10	MSIO198PB5

Package Pin	M2S090TS-FGG484 Pin Name
AA11	MSIO203PB5
AA12	MSIO204PB5
AA13	MSIO209PB5/VCCC_SE0_CLKI
AA14	VSS
AA15	MSIO213NB5
AA16	MSIO222PB5
AA17	MSIO222NB5
AA18	MSIO221NB5
AA19	VDDI5
AA20	XTLOSC_AUX_EXTAL
AA21	XTLOSC_MAIN_EXTAL
AA22	JTAGSEL
AB1	VSS
AB2	SERDES_0_TXD0_P
AB3	VSS
AB4	SERDES_0_TXD1_P
AB5	VSS
AB6	SERDES_0_TXD2_P
AB7	VSS
AB8	SERDES_0_TXD3_P
AB9	VSS
AB10	MSIO198NB5
AB11	MSIO203NB5
AB12	VDDI5
AB13	MSIO208PB5/CCC_SW1_CLKI3
AB14	MSIO208NB5
AB15	MSIO213PB5/VCCC_SE1_CLKI
AB16	VSS
AB17	MSIO221PB5
AB18	MSIO230PB5
AB19	MSIO230NB5
AB20	XTLOSC_AUX_XTAL
AB21	XTLOSC_MAIN_XTAL
AB22	VSS
B1	MSIO140NB8
B2	MSIO136PB8
B3	MSIO129NB8
B4	VSS
B5	DDRIO98PB1
B6	DDRIO92PB1/GB0/CCC_NW0_CLKI3

Package Pin	M2S090TS-FGG484 Pin Name
B7	DDRIO91NB1/MDDR_DQS_ECC_N
B8	VDDI1
B9	DDRIO87PB1/MDDR_DQ0
B10	VSS
B11	DDRIO85PB1/MDDR_DQS0
B12	VDDI1
B13	DDRIO79PB1/GB8/CCC_NE0_CLKI3/MDDR_DQS1
B14	VSS
B15	DDRIO74PB1/MDDR_CKE
B16	VDDI1
B17	DDRIO70NB1/MDDR_ADDR0
B18	VSS
B19	DDRIO67PB1/MDDR_ADDR5
B20	VDDI1
B21	DDRIO64NB1/MDDR_ADDR11
B22	MSIO60NB2/MMUART_0_CLK/GPIO_29_B/USB_NXT_C
C1	MSIO140PB8
C2	VDDI8
C3	MSIO129PB8
C4	MSIO127PB8
C5	DDRIO97PB1
C6	VDDI1
C7	DDRIO91PB1/MDDR_DQS_ECC
C8	VSS
C9	DDRIO88NB1
C10	VDDI1
C11	DDRIO85NB1/MDDR_DQS0_N
C12	VSS
C13	DDRIO79NB1/MDDR_DQS1_N
C14	VDDI1
C15	DDRIO74NB1/MDDR_CS_N
C16	DDRIO70PB1/MDDR_BA2
C17	DDRIO68PB1/MDDR_ADDR3
C18	DDRIO68NB1/MDDR_ADDR4
C19	DDRIO66NB1/MDDR_ADDR7
C20	DDRIO66PB1/MDDR_ODT
C21	VSS
C22	MSIO60PB2/MMUART_0_RXD/GPIO_28_B/USB_STP_C
D1	MSIO142PB8
D2	MSIO142NB8

Package Pin	M2S090TS-FGG484 Pin Name
D3	MSIO134PB8
D4	MSIO134NB8
D5	MSIO127NB8
D6	DDRIO97NB1
D7	MDDR_IMP_CALIB
D8	DDRIO90NB1/MDDR_DM_RDQS_ECC
D9	DDRIO88PB1/CCC_NW1_CLKI3
D10	DDRIO83PB1/MDDR_DQ5
D11	DDRIO83NB1/MDDR_DQ6
D12	DDRIO80PB1/MDDR_DQ10/CCC_NE0_CLKI2
D13	DDRIO80NB1/MDDR_DQ11
D14	DDRIO76PB1/CCC_NE1_CLKI3/MDDR_DQ14
D15	VSS
D16	DDRIO69PB1/MDDR_ADDR1
D17	VDDI1
D18	DDRIO62PB1/MDDR_ADDR14
D19	VSS
D20	DDRIO63NB1/MDDR_ADDR13
D21	**MSI59NB2**/MMUART_0_TXD/GPIO_27_B/USB_DIR_C
D22	FLASH_GOLDEN_N
E1	MSIO143PB8
E2	MSIO143NB8
E3	VSS
E4	MSIO138PB8
E5	MSIO138NB8
E6	VSS
E7	DDRIO93PB1/MDDR_TMATCH_ECC_OUT
E8	DDRIO90PB1/MDDR_TMATCH_ECC_IN
E9	VSS
E10	DDRIO86NB1/MDDR_DQ3
E11	VDDI1
E12	DDRIO82PB1/MDDR_DQ7
E13	DDRIO76NB1/MDDR_DQ15
E14	VSS
E15	DDRIO73PB1/MDDR_RESET_N
E16	DDRIO69NB1/MDDR_ADDR2
E17	DDRIO65PB1/MDDR_ADDR8
E18	DDRIO62NB1/MDDR_ADDR15
E19	DDRIO63PB1/MDDR_ADDR12
E20	VDDI2

Package Pin	M2S090TS-FGG484 Pin Name
E21	MSIO58NB2/MMUART_0_DCD/GPIO_22_B
E22	MSIO58PB2/MMUART_0_RI/GPIO_21_B
F1	VDDI8
F2	MSIO152NB8
F3	MSIO145PB8
F4	MSIO145NB8
F5	MSIO132PB8
F6	MSIO132NB8
F7	VDDI1
F8	DDRIO93NB1/CCC_NW0_CLKI2
F9	VDDI1
F10	DDRIO86PB1/MDDR_DQ2
F11	VSS
F12	DDRIO82NB1/MDDR_TMATCH_0_OUT
F13	VDDI1
F14	DDRIO75PB1/MDDR_RAS_N
F15	DDRIO73NB1/MDDR_CAS_N
F16	VSS
F17	DDRIO65NB1/MDDR_ADDR9
F18	MSIO57NB2/MMUART_0_DSR/GPIO_20_B
F19	MSIO57PB2/MMUART_0_CTS/GPIO_19_B/USB_DATA7_C
F20	MSIO56NB2/MMUART_0_DTR/GPIO_18_B/USB_DATA6_C
F21	MSIO56PB2/MMUART_0_RTS/GPIO_17_B/USB_DATA5_C
F22	VDDI2
G1	MSIO156NB8
G2	MSIO152PB8
G3	MSIO154NB8
G4	VDDI8
G5	MSIO131PB8
G6	MSIO131NB8
G7	MSIO146NB8
G8	CCC_NW1_PLL_VSSA
G9	CCC_NW1_PLL_VDDA
G10	VREF
G11	VREF
G12	DDRIO78PB1/MDDR_TMATCH_0_IN
G13	DDRIO78NB1/MDDR_DM_RDQS1
G14	DDRIO75NB1/MDDR_WE_N
G15	VREF
G16	MSIO61NB2/I2C_0_SCL/GPIO_31_B/USB_DATA1_C

Package Pin	M2S090TS-FGG484 Pin Name
G17	MSIO61PB2/I2C_0_SDA/GPIO_30_B/USB_DATA0_C
G18	MSIO55NB2/MMUART_1_RXD/GPIO_26_B/USB_DATA3_C
G19	MSIO55PB2/GB14/VCCC_SE1_CLKI/MMUART_1_CLK/GPIO_25_B/USB_DATA4_C
G20	VSS
G21	MSIO53NB2/MMUART_1_DCD/GPIO_16_B
G22	MSIO53PB2/CCC_NE1_CLKI1/MMUART_1_RI/GPIO_15_B
H1	MSIO156PB8/GB6/CCC_NW1_CLKI1
H2	VSS
H3	MSIO154PB8
H4	MSIO150PB8
H5	MSIO150NB8
H6	MSIO148PB8
H7	MSIO146PB8
H8	CCC_NW0_PLL_VDDA
H9	VSS
H10	VDD
H11	VSS
H12	VDDI1
H13	VSS
H14	VDDI1
H15	CCC_NE0_PLL_VDDA
H16	MSS_MDDR_PLL_VDDA
H17	MSS_MDDR_PLL_VSSA
H18	VDDI2
H19	MSIO54NB2/MMUART_1_TXD/GPIO_24_B/USB_DATA2_C
H20	MSIO54PB2/GB10/VCCC_SE0_CLKI/USB_XCLK_C
H21	MSIO51NB2/MMUART_1_DTR/GPIO_12_B
H22	MSIO51PB2/MMUART_1_RTS/GPIO_11_B
J1	MSIO158PB8/CCC_NW1_CLKI0
J2	MSIO158NB8
J3	MSIO157PB8/GB2/CCC_NW0_CLKI1
J4	MSIO157NB8
J5	VSS
J6	MSIO148NB8
J7	VDDI8
J8	CCC_NW0_PLL_VSSA
J9	VDD
J10	VSS
J11	VDD
J12	VSS

Package Pin	M2S090TS-FGG484 Pin Name
J13	VDD
J14	VSS
J15	CCC_NE0_PLL_VSSA
J16	CCC_NE1_PLL_VSSA
J17	CCC_NE1_PLL_VDDA
J18	MSIO24NB3/SPI_1_SS3/GPIO_16_A
J19	MSIO52NB2/MMUART_1_DSR/GPIO_14_B
J20	MSIO52PB2/CCC_NE0_CLKI1/MMUART_1_CTS/GPIO_13_B
J21	VDDI2
J22	MSIO20NB3/GB13/VCCC_SE1_CLKI/GPIO_26_A
K1	MSIOD178PB7/CCC_SW0_CLKI0
K2	MSIOD178NB7
K3	VDDI7
K4	MSIOD175PB7/GB5/CCC_SW1_CLKI1
K5	MSIOD175NB7
K6	MSIO159PB8/CCC_NW0_CLKI0
K7	MSIO159NB8
K8	MSIOD176PB7/GB1/CCC_SW0_CLKI1
K9	VSS
K10	VDD
K11	VSS
K12	VDD
K13	VSS
K14	VDD
K15	MSIO22NB3/SPI_0_SS2/GPIO_9_A/USB_DATA6_A
K16	MSIO23NB3/SPI_1_SS1/GPIO_14_A
K17	MSIO23PB3/SPI_0_SS3/GPIO_10_A/USB_DATA7_A
K18	MSIO24PB3/SPI_1_SS2/GPIO_15_A
K19	VSS
K20	MSIO19NB3/SPI_1_SS7/GPIO_24_A
K21	MSIO19PB3/SPI_1_SS6/GPIO_23_A
K22	MSIO20PB3/GB9/VCCC_SE0_CLKI/GPIO_25_A
L1	VSS
L2	MSIOD179PB7
L3	MSIOD179NB7
L4	MSIOD180PB7
L5	MSIOD180NB7
L6	VDDI7
L7	MSIOD177NB7
L8	MSIOD176NB7

Package Pin	M2S090TS-FGG484 Pin Name
L9	VDD
L10	VSS
L11	VDD
L12	VSS
L13	VDD
L14	VSS
L15	VPP
L16	MSIO22PB3/SPI_0_SS1/GPIO_8_A/USB_DATA5_A
L17	VDDI3
L18	MSIO18NB3/SPI_1_SS5/GPIO_18_A
L19	MSIO18PB3/SPI_1_SS4/GPIO_17_A
L20	MSIO17NB3/SPI_1_SS0/GPIO_13_A
L21	MSIO17PB3/SPI_1_SDO/GPIO_12_A
L22	VSS
M1	MSIOD185NB7
M2	MSIOD183NB7
M3	MSIOD183PB7
M4	VSS
M5	MSIOD181PB7
M6	MSIOD181NB7
M7	MSIOD177PB7/CCC_SW1_CLKI0
M8	MSIOD188NB7
M9	VSS
M10	VDD
M11	VSS
M12	VDD
M13	VSS
M14	VDD
M15	VPPNVM
M16	MSIO14PB3/SPI_0_SS4/GPIO_19_A
M17	MSIO14NB3/SPI_0_SS5/GPIO_20_A
M18	MSIO15PB3/SPI_0_SS6/GPIO_21_A
M19	MSIO15NB3/SPI_0_SS7/GPIO_22_A
M20	VDDI3
M21	MSIO16PB3/SPI_1_CLK
M22	MSIO16NB3/SPI_1_SDI/GPIO_11_A
N1	MSIOD185PB7
N2	VDDI7
N3	MSIOD184PB7
N4	MSIOD184NB7

Package Pin	M2S090TS-FGG484 Pin Name
N5	MSIOD182PB7
N6	MSIOD182NB7
N7	VSS
N8	MSIOD188PB7
N9	VDD
N10	VSS
N11	VDD
N12	VSS
N13	VDD
N14	VSS
N15	VSSNVM
N16	MSIO8PB3/CAN_RX/GPIO_3_A/USB_DATA1_A
N17	MSIO8NB3/CAN_TX_EN_N/GPIO_4_A/USB_DATA2_A
N18	VSS
N19	MSIO12PB3/SPI_0_CLK/USB_XCLK_A
N20	MSIO12NB3/SPI_0_SDI/GPIO_5_A/USB_DIR_A
N21	MSIO13PB3/SPI_0_SDO/GPIO_6_A/USB_STP_A
N22	MSIO13NB3/SPI_0_SS0/GPIO_7_A/USB_NXT_A
P1	MSIOD187PB7
P2	MSIOD187NB7
P3	MSIOD186NB7
P4	MSIOD186PB7
P5	VDDI7
P6	MSIOD189PB7
P7	MSIOD189NB7
P8	SERDES_0_VDD
P9	VSS
P10	VDD
P11	VSS
P12	VDD
P13	VSS
P14	VDD
P15	VPP
P16	MSIO7NB3/CAN_TX/GPIO_2_A/USB_DATA0_A
P17	MSIO6PB3/USB_DATA6_B
P18	MSIO6NB3
P19	SC_SPI_SDO
P20	SC_SPI_SS
P21	VSS
P22	MSIO11PB3/CCC_NE0_CLKI0/I2C_1_SDA/GPIO_0_A/USB_DATA3_A

Package Pin	M2S090TS-FGG484 Pin Name
R1	MSIOD190NB7
R2	MSIOD190PB7
R3	MSIOD191PB7
R4	MSIOD191NB7
R5	VSS
R6	CCC_SW0_PLL_VSSA
R7	CCC_SW1_PLL_VDDA
R8	SERDES_0_L01_VDDAIO
R9	VSS
R10	VSS
R11	VDD
R12	VSS
R13	VDD
R14	VSS
R15	DEVRST_N
R16	MSIO7PB3
R17	MSIO1PB3/USB_XCLK_B
R18	MSIO1NB3/USB_DIR_B
R19	VDDI3
R20	SC_SPI_CLK
R21	SC_SPI_SDI
R22	MSIO11NB3/CCC_NE1_CLKI0/I2C_1_SCL/GPIO_1_A/USB_DATA4_A
T1	MSIOD193NB6/SERDES_0_REFCLK0_N
T2	VSS
T3	MSIOD192NB7
T4	MSIOD192PB7
T5	CCC_SW0_PLL_VDDA
T6	SERDES_0_PLL_VSSA
T7	CCC_SW1_PLL_VSSA
T8	SERDES_0_PLL_VDDA
T9	SERDES_0_VDD
T10	SERDES_0_L23_VDDAIO
T11	NC
T12	NC
T13	MSIO210NB5
T14	VDDI5
T15	VSS
T16	MSIO232NB5
T17	VSS
T18	MSIO2PB3/USB_STP_B

Package Pin	M2S090TS-FGG484 Pin Name
T19	MSIO2NB3/USB_NXT_B
T20	MSIO5PB3/USB_DATA4_B
T21	MSIO5NB3/USB_DATA5_B
T22	VDDI3
U1	MSIOD193PB6/SERDES_0_REFCLK0_P
U2	VDDI6
U3	MSIOD194PB6/SERDES_0_REFCLK1_P
U4	MSIOD194NB6/SERDES_0_REFCLK1_N
U5	SERDES_0_L01_REXT
U6	SERDES_0_L01_REFRET
U7	SERDES_0_L01_VDDAPLL
U8	SERDES_0_L23_VDDAPLL
U9	VPP
U10	MSIO199PB5
U11	MSIO199NB5
U12	VSS
U13	MSIO210PB5/GB11/VCCC_SE0_CLKI
U14	MSIO218PB5
U15	MSIO218NB5
U16	MSIO232PB5
U17	MSIO234NB5
U18	MSIO238NB5
U19	MSIO0PB3
U20	VSS
U21	MSIO4NB3/USB_DATA3_B
U22	MSIO4PB3/USB_DATA2_B
V1	VSS
V2	VSS
V3	VSS
V4	VSS
V5	VSS
V6	VSS
V7	VSS
V8	SERDES_0_L23_REXT
V9	SERDES_0_L23_REFRET
V10	VDDI5
V11	MSIO201PB5/GB3/CCC_SW0_CLKI3
V12	MSIO206NB5
V13	MSIO211PB5
V14	MSIO211NB5

Package Pin	M2S090TS-FGG484 Pin Name
V15	VSS
V16	MSIO224NB5
V17	MSIO234PB5
V18	MSIO238PB5
V19	MSIO0NB3/USB_DATA7_B
V20	JTAG_TMS/M3_TMS/M3_SWDIO
V21	MSIO3NB3/USB_DATA1_B
V22	MSIO3PB3/USB_DATA0_B
W1	SERDES_0_RXD0_P
W2	VSS
W3	SERDES_0_RXD1_P
W4	VSS
W5	SERDES_0_RXD2_P
W6	VSS
W7	SERDES_0_RXD3_P
W8	VSS
W9	MSIO196PB5
W10	MSIO197PB5/PROBE_A
W11	MSIO201NB5/GB7/CCC_SW1_CLKI2
W12	MSIO206PB5
W13	VDDI5
W14	MSIO212NB5
W15	MSIO216NB5
W16	MSIO224PB5
W17	MSIO226NB5
W18	VSS
W19	MSIO236NB5
W20	JTAG_TCK/M3_TCK
W21	VDDI4
W22	JTAG_TDI/M3_TDI
Y1	SERDES_0_RXD0_N
Y2	VSS
Y3	SERDES_0_RXD1_N
Y4	VSS
Y5	SERDES_0_RXD2_N
Y6	VSS
Y7	SERDES_0_RXD3_N
Y8	VSS
Y9	MSIO196NB5/CCC_SW0_CLKI2
Y10	MSIO197NB5/PROBE_B

Package Pin	M2S090TS-FGG484 Pin Name
Y11	VSS
Y12	MSIO204NB5
Y13	MSIO209NB5
Y14	MSIO212PB5/GB15/VCCC_SE1_CLKI
Y15	MSIO216PB5
Y16	VDDI5
Y17	MSIO226PB5
Y18	MSIO228PB5
Y19	MSIO228NB5
Y20	MSIO236PB5
Y21	JTAG_TDO/M3_TDO/M3_SWO
Y22	JTAG_TRSTB/M3_TRSTB

5 – Board Components Placement

The SmartFusion2 Security Evaluation Kit components placement on top and bottom sides are shown in the following figures.

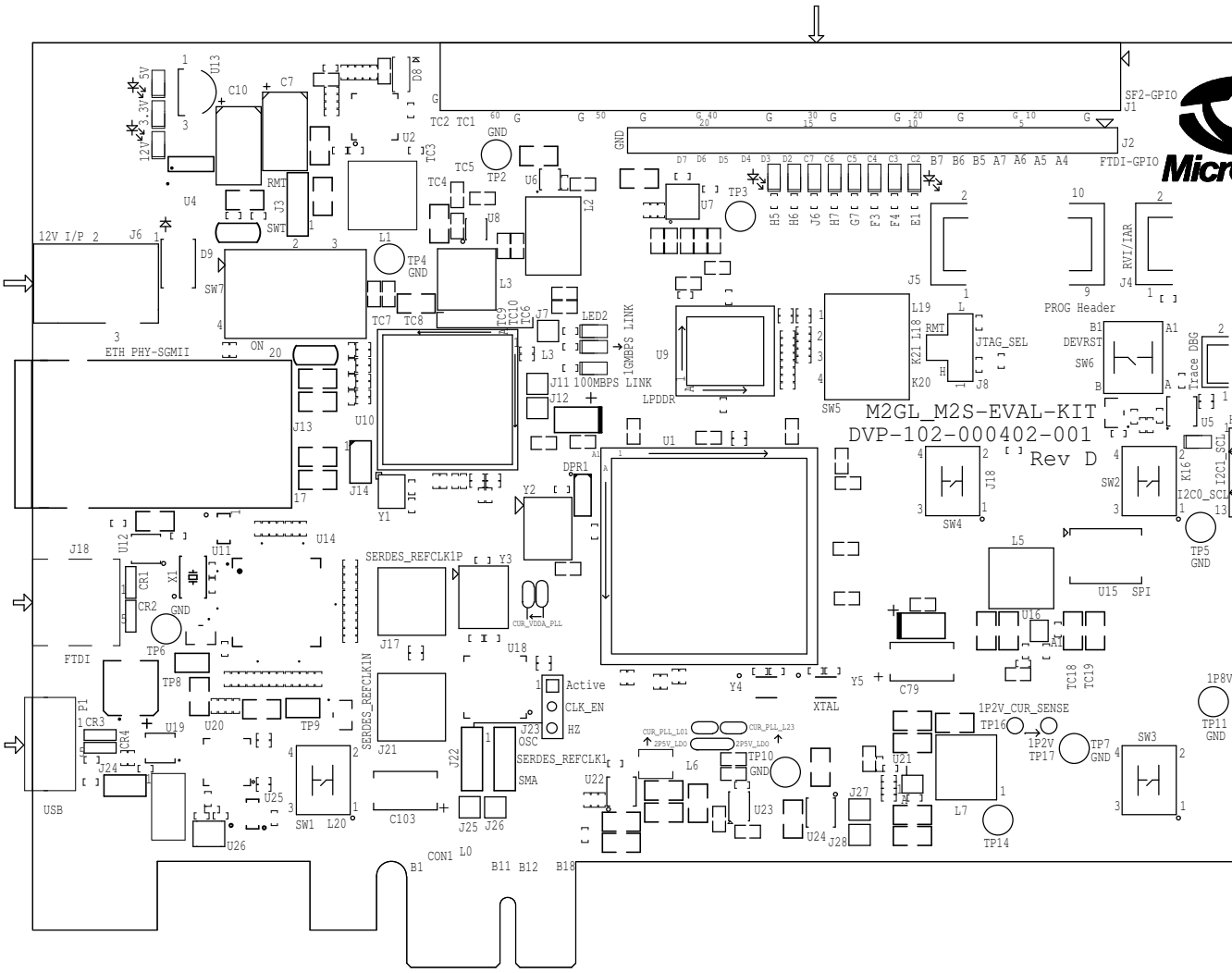

Figure 18 Silkscreen Top View

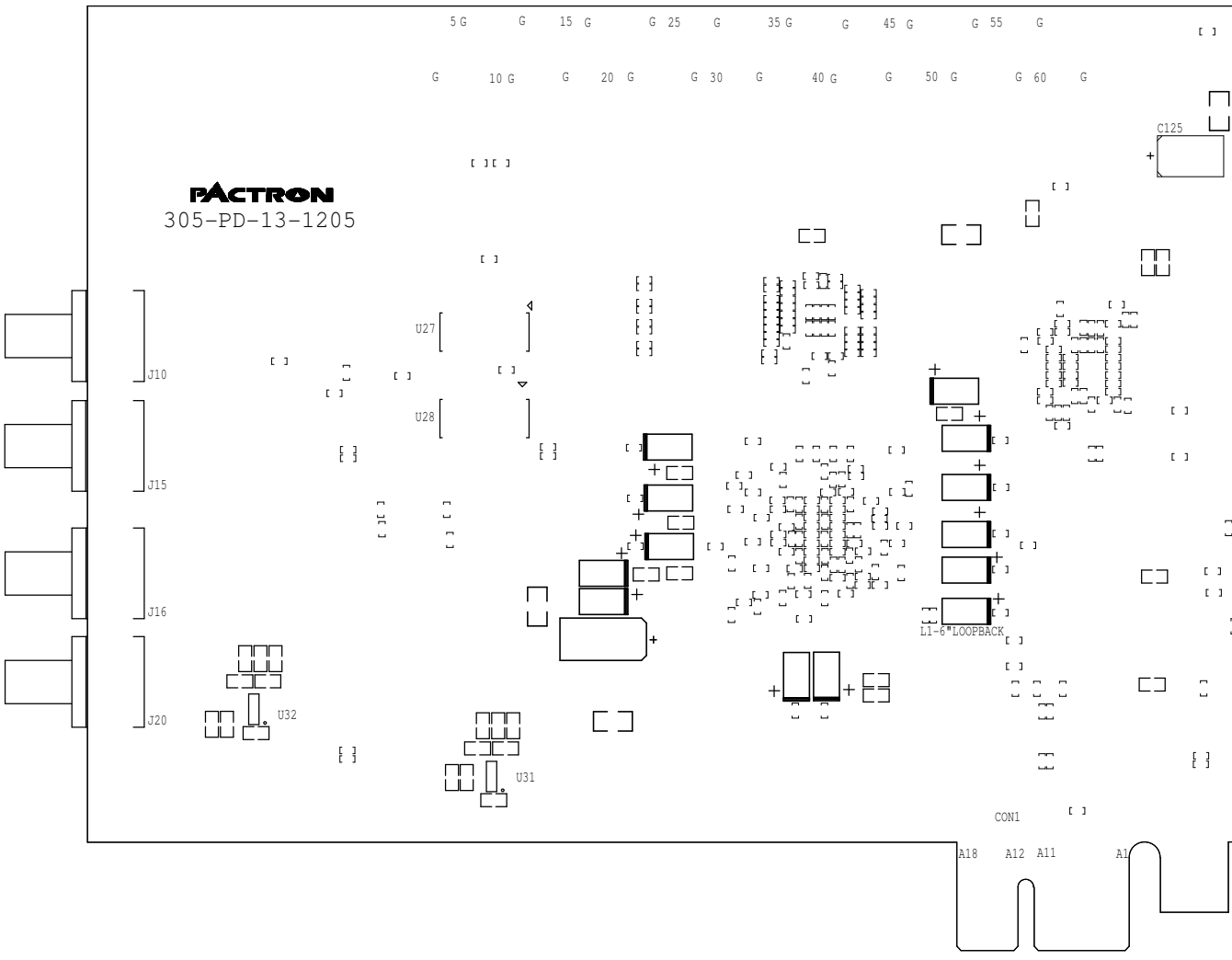

Figure 19 Silkscreen Bottom View

6 – Demo Design

M2S090TS-EVAL-KIT Board Demo Design

The SmartFusion2 M2S090TS-EVAL-KIT comes with a preloaded PCIe control plane demo design. This demo design demonstrates PCIe interface of the SmartFusion2 device. Table 14 lists the PCIe demo design requirements.

Table 14 PCIe Demo Design Requirements

Design Requirements	Version
Host PC or Laptop with an available PCIe 2.0 Gen 1 or Gen 2 compliant slot	64-bit Windows 7 OS or 64-bit Red Hat Linux OS (Kernel Version: 2.6.18-308)
Express Card slot and PCIe Express card adapter for Laptop only (not provided with the kit contents)	–
PCIe Edge Card Ribbon cable (not provided with the kit contents)	–
Host PC Drivers (provided along with the design files)	–
GUI executable (provided along with the design files)	–

The design files for this demo can be downloaded from the Microsemi website: http://soc.microsemi.com/download/rsc/?f=sf2_pcie_control_plane_demo_advanced_and_evaluation_kit_liberov11p4_dg_df

Refer to Appendix 1 – Running the PCIe Demo Design on Windows to run the demo design.

7 – Manufacturing Test

The M2S090TS-EVAL-KIT contains a manufacturing test program that can be run to verify the functionality of the board. The test program contains a list of options that can be run as diagnostics. After setting up the HyperTerminal and the board is powered up, the tests are displayed, as shown in Figure 37. From the list of options, any test(s) can be selected to verify the functionality.

Before testing the SmartFusion2 Security Evaluation board:

- Download `M2S090_EVAL_KIT_MTD_SP1.prjx` file from http://soc.microsemi.com/download/rsc/?f=M2S090TS_EVAL_KIT_DF
- Download and install the FTD drivers from: http://www.ftdichip.com/Drivers/D2XX.htm

Programming M2S090TS-EVAL-KIT

Installing Libero v11.5 or Later

While starting manufacturing test, make sure the Libero SoC software and other required tools are installed as mentioned in the Software Settings section. Once you successfully install the Libero v11.5 software, connect the USB cable (mini USB to Type A USB cable) to J18 and connect the other end to USB port of the Host PC.

Power Supply Validation

The following steps describe how to test and validate the power supply to the board:

1. Connect the following jumpers on the SmartFusion2 Security Evaluation board:
   - J3 short pin 1-2
   - J8 short pin 1-2
   - J22 and J23 short pin 1-2
   - H1 short pin 6-10
   - H1 short pin 7-11
   - J24 short pin 1-2

Note: Before making the jumper connections, switch off the power supply switch, **SW7**.

2. Connect the **12V/5** Amps power supply brick to the **J6** jumper.
3. Switch **ON** the **SW7** power supply switch. Once the board is set up, DS1, DS2, and DS3 LEDs will glow.

SPI Slave Programming (FlashPro5) on M2S090TS EVAL KIT

An external hardware programmer is not required to program the device in SPI Slave (FlashPro5) mode. SPI Slave programming is done through the dedicated System Controller SPI (SC_SPI) port in Slave mode. In this mode, SmartFusion2 device is programmed by an external SPI Flash device configured in Master mode.

Ensure that Libero 11.5 or later and FlashPro 11.5 or later are successfully installed in the Host PC. Do not connect any FlashPro programmer to the Host PC.

SPI Slave Programming Test Procedure

1. Connect USB cable (mini USB to Type A USB cable) to J18 and connect the other end to the USB port of the Host PC.
2. Open the Libero v11.5 software on the Host PC.

Figure 20 Libero Start Page

3. Select **Open Project** from the **Project** menu.

Figure 21 Opening a Project

4. Select the **M2S090_EVAL_KIT_MTD_SP1.prjx** project on the Host PC and click **Open**.
5. The M2S090_EVAL_KIT_MTD_SP1 project file is provided along with MTD folder.

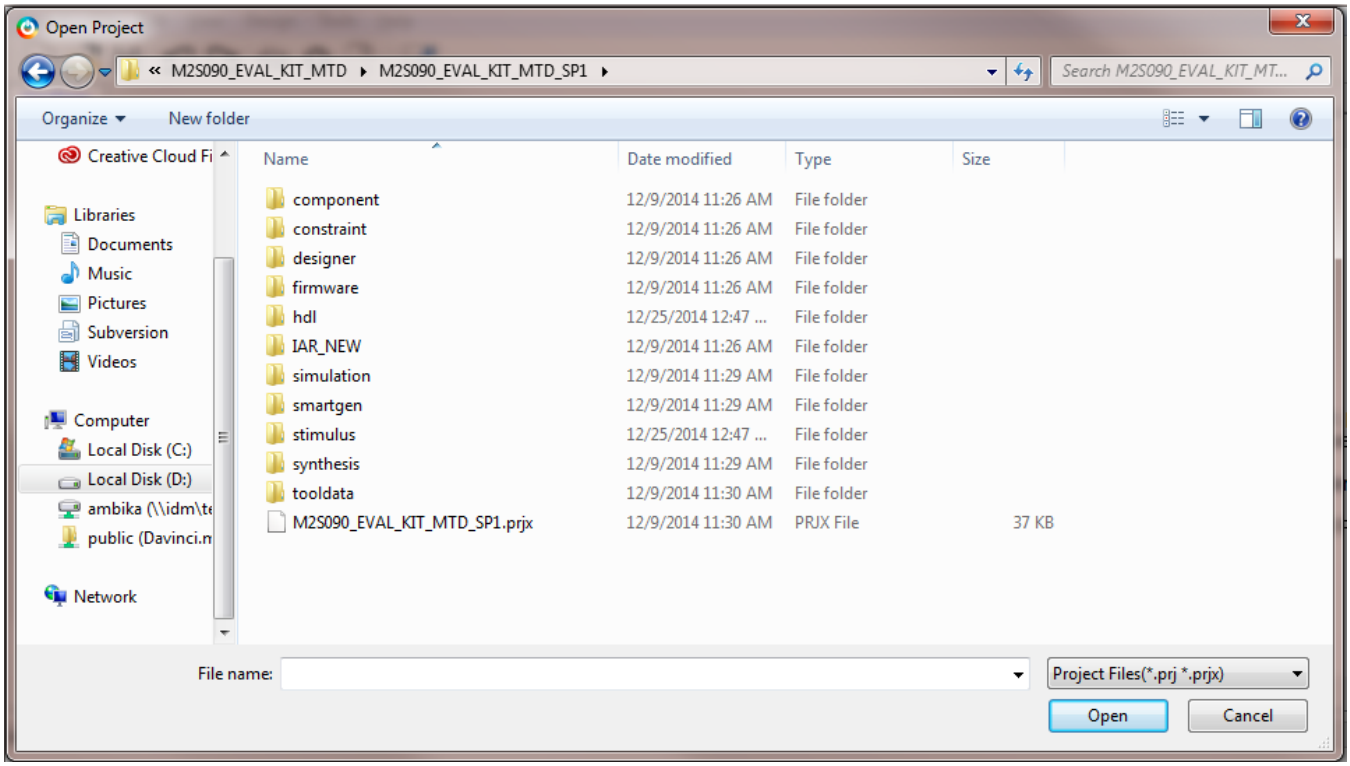

Figure 22 Selecting Counter Project

6. The M2S090_EVAL_KIT_MTD_SP1 project window is displayed, as shown in Figure 23.

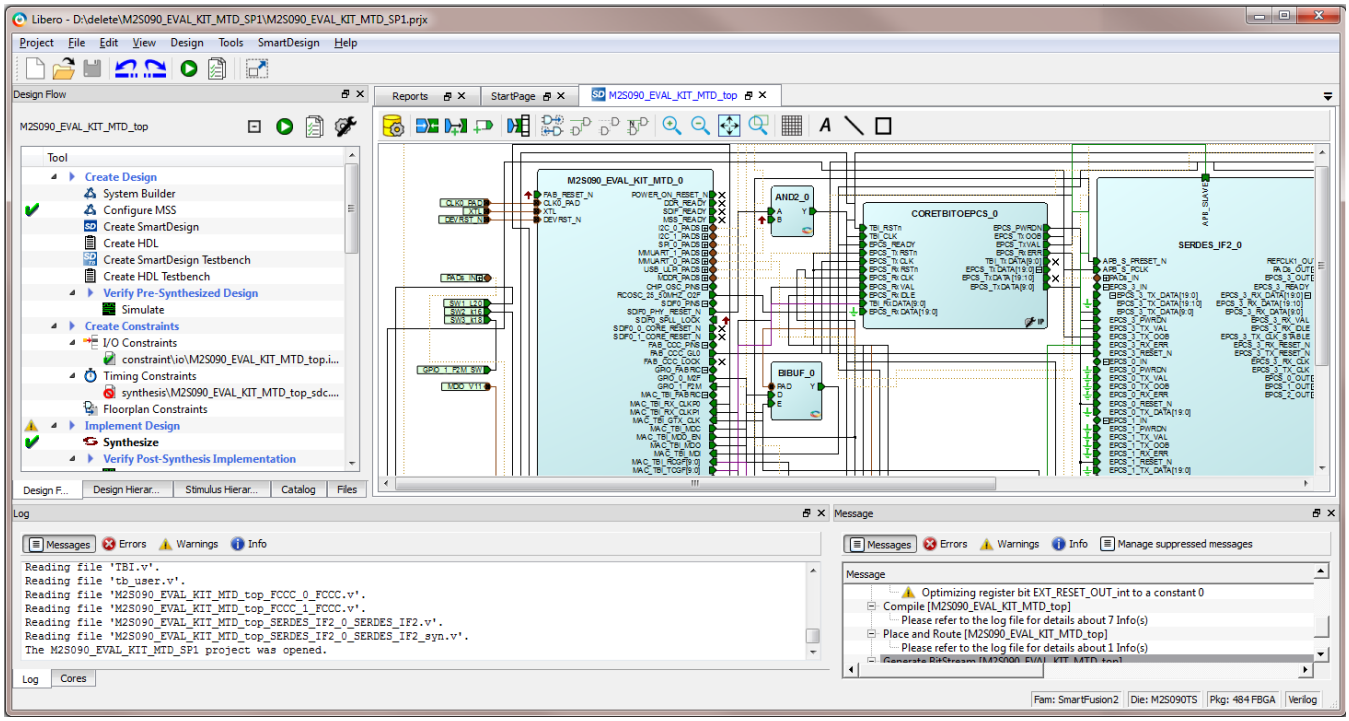

Figure 23 Project Top Module

Note: Ensure that the board is connected to the PC and power is supplied.

7. From the **Design Flow** tab on the left-side, double-click **Program Connectivity and Interface** under Edit Design Hardware Configuration.

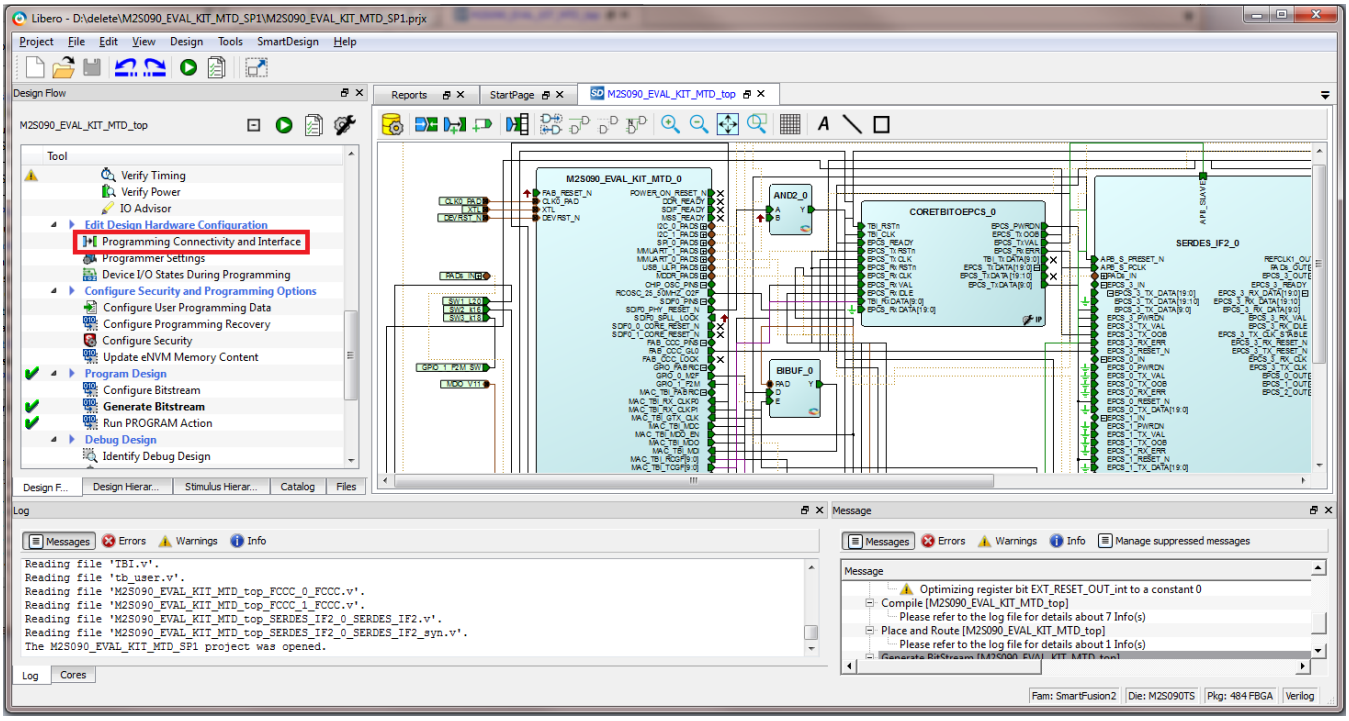

Figure 24 Selecting Programming Connectivity and Interface

8. The Programming Connectivity and Interface window is displayed as shown in Figure 25.

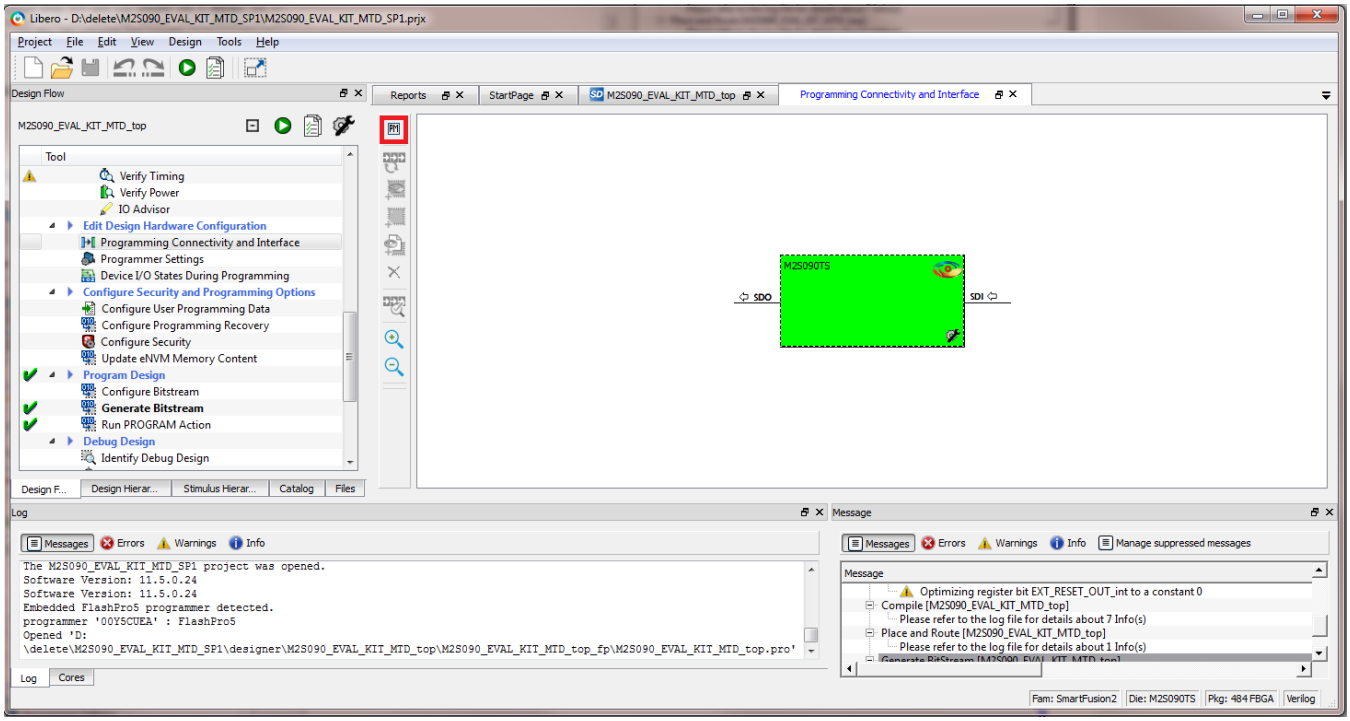

Figure 25 Programming Connectivity and Interface Window

9. Select the **SPI Slave (FlashPro5 only)** option and click **OK**.

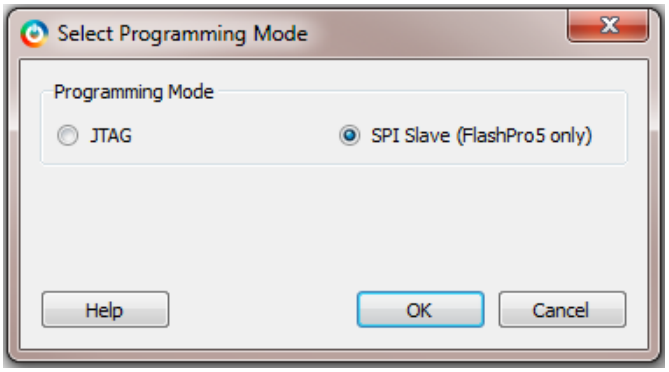

Figure 26 Selecting Programming Mode

10. From the **Design Flow** tab on the left-side, double-click **Run Program Action** under Program Design to program the device using SPI slave programming mode.

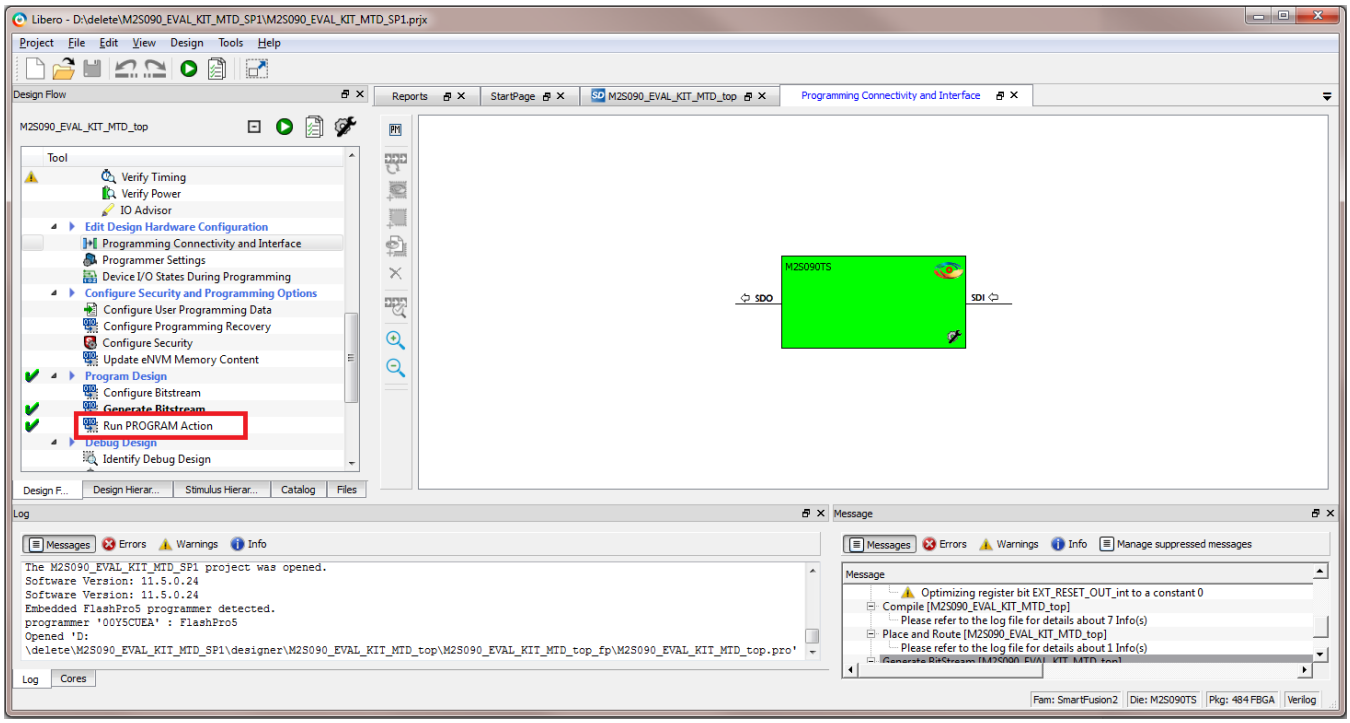

Figure 27 Programming the Device

11. When the programming begins, the window is displayed as shown in Figure 28.

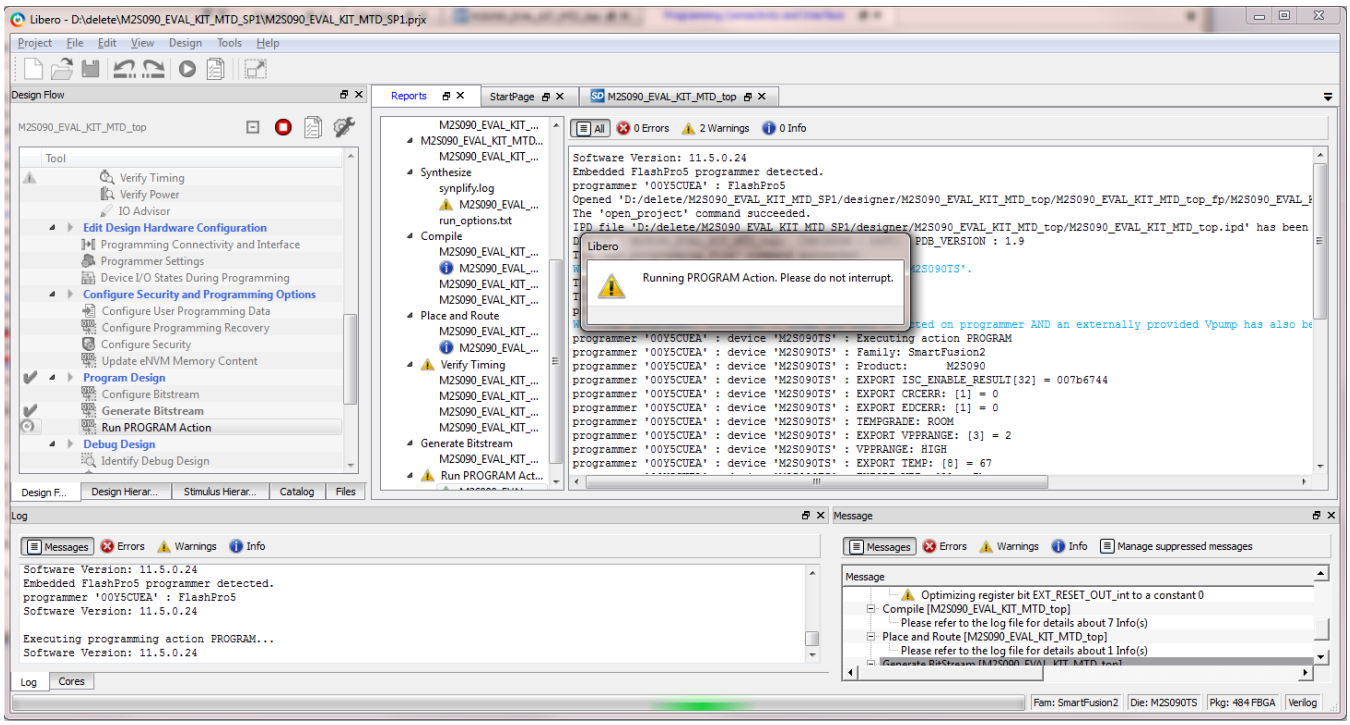

Figure 28 Running Program Action

12. Once the device is programmed, LEDs at E1 and F4 will glow and window is displayed as shown in Figure 29.

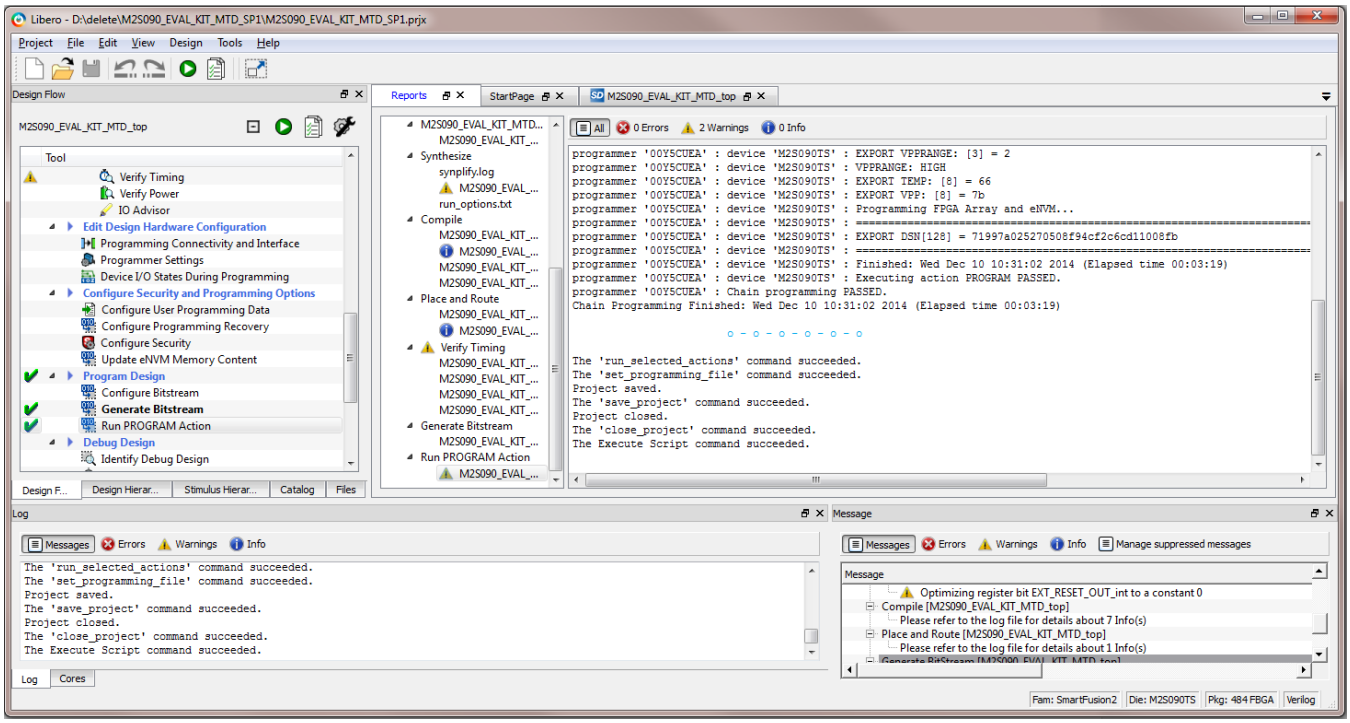

Figure 29 Successful Run Program Action

Running the Manufacturing Test

Setting Up the HyperTerminal

The following steps describe how to set up HyperTerminal to perform the manufacturing test:

1. Connect the USB cable (mini USB to Type A USB cable) to J18 and other end of the cable to the USB port of the Host PC.
2. Open **HyperTerminal** from the Start menu.

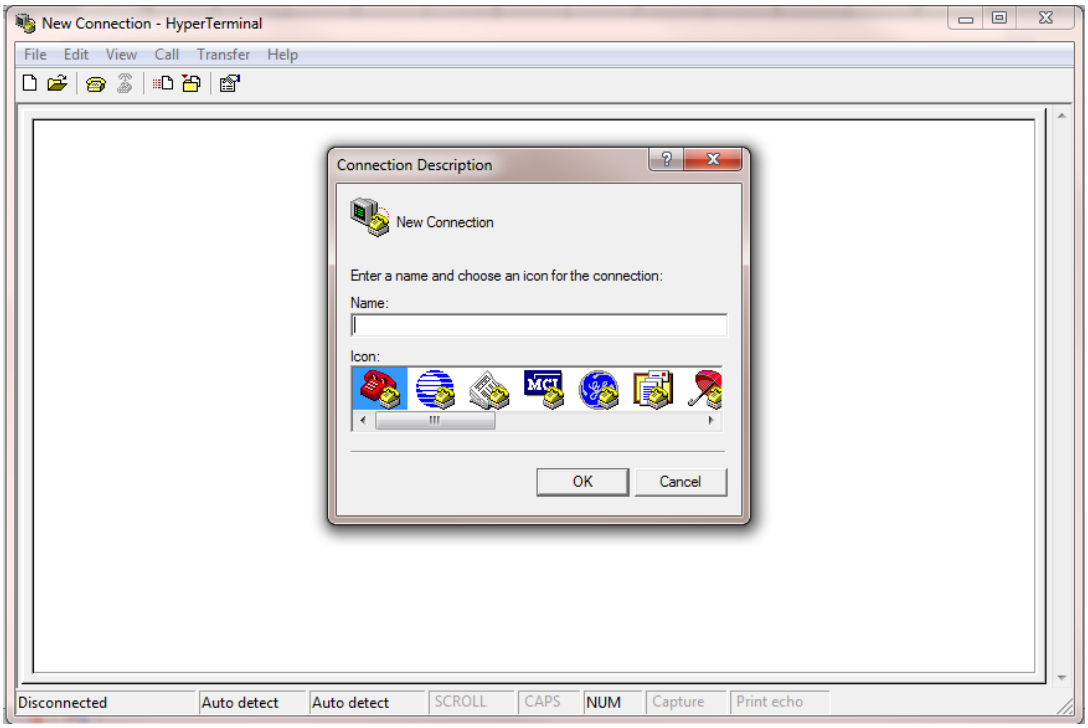

Figure 30 Connection Description Window

3. Enter **M2S090-KIT-MTD** as connection name and click **OK**. The **Connect To** dialog-box is displayed as shown in Figure 31.

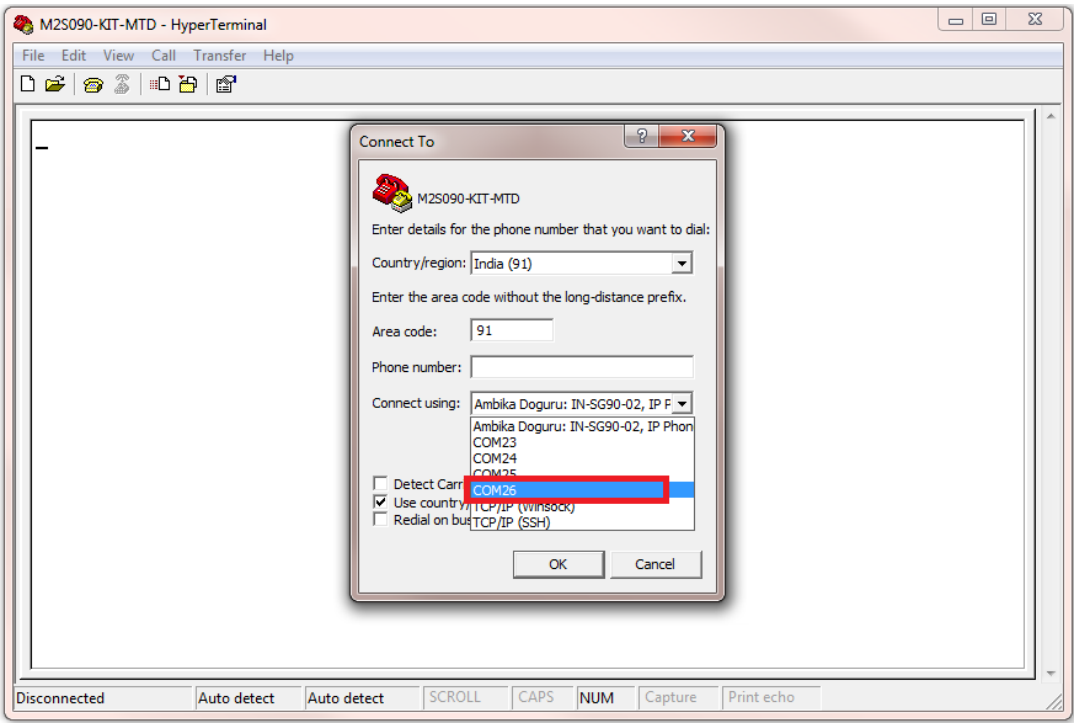

Figure 31 Connect To Window

4. Select the highest value COM port from the **Connect using** drop-down list and click **OK**. The **COM<port number> Properties** dialog-box is displayed.

Note:

- When using USB cable for HyperTerminal communication, four COM ports are available in the Connect using drop-down list. Select the **highest** COM port to establish connection with the Host PC.

5. In case only one COM port appears select that COM port to establish connection with the Host PC.

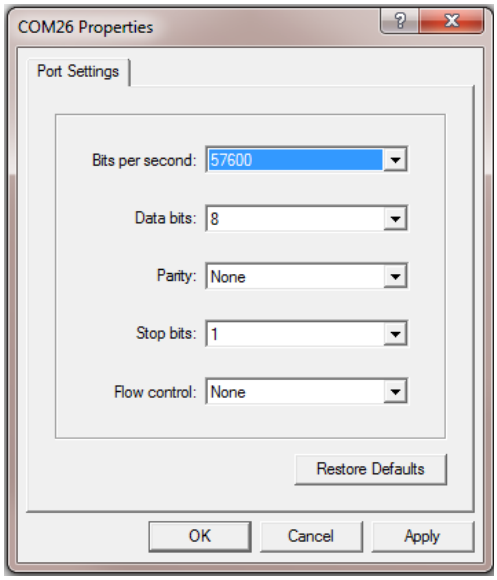

Figure 32 Port Settings Window

6. Select the following settings from the **Port Settings** window and click **Apply** and **OK**.
   - Bits per second: 57600
   - Data bits: 8
   - Parity: None
   - Stop bits: 1
   - Flow control: None
7. Select **Properties** from the **File** menu in the HyperTerminal window. The **M2S090-KIT-MTD Properties** window is displayed.

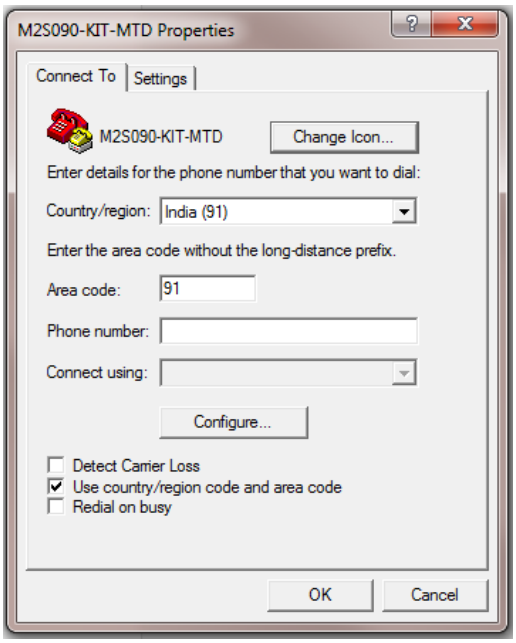

Figure 33 M2S090-KIT-MTD Properties Window

8. Select **Settings** tab.

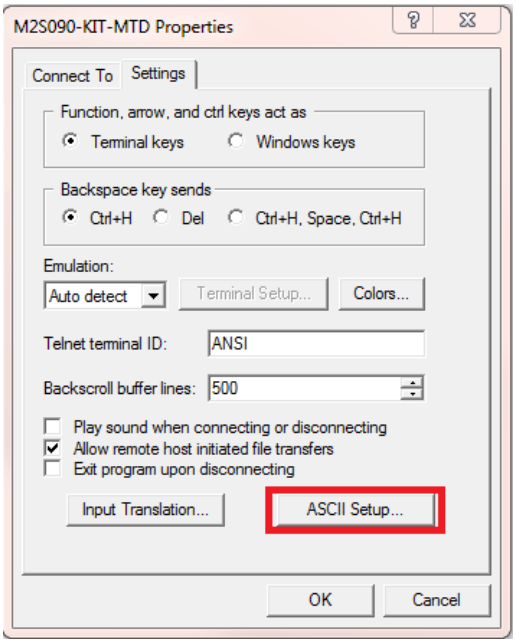

Figure 34 Settings Tab

9. Keep the default settings and click **ASCII Setup**. The ASCII Setup dialog-box is displayed, as shown in Figure 35.

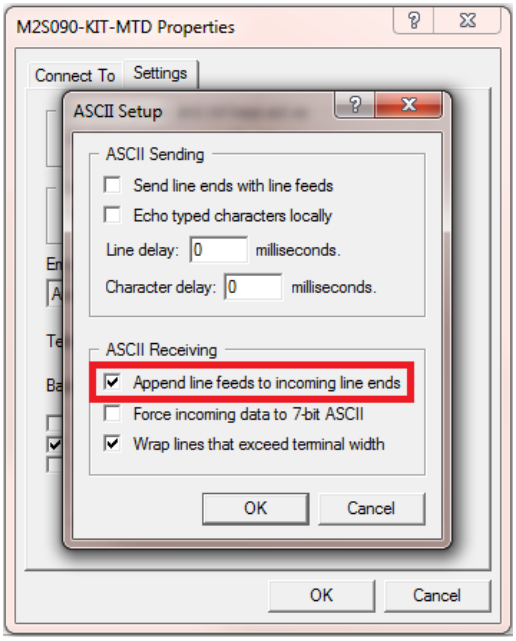

Figure 35 ASCII Setup Window

10. Select the **Append line feeds to incoming line ends** check box and click **OK**.
11. Click **OK** to save the properties and close the **M2S090-KIT-MTD Properties** window.
12. Press SW6 switch to restart the board with the settings. The HyperTerminal window is displayed, as shown in Figure 36.

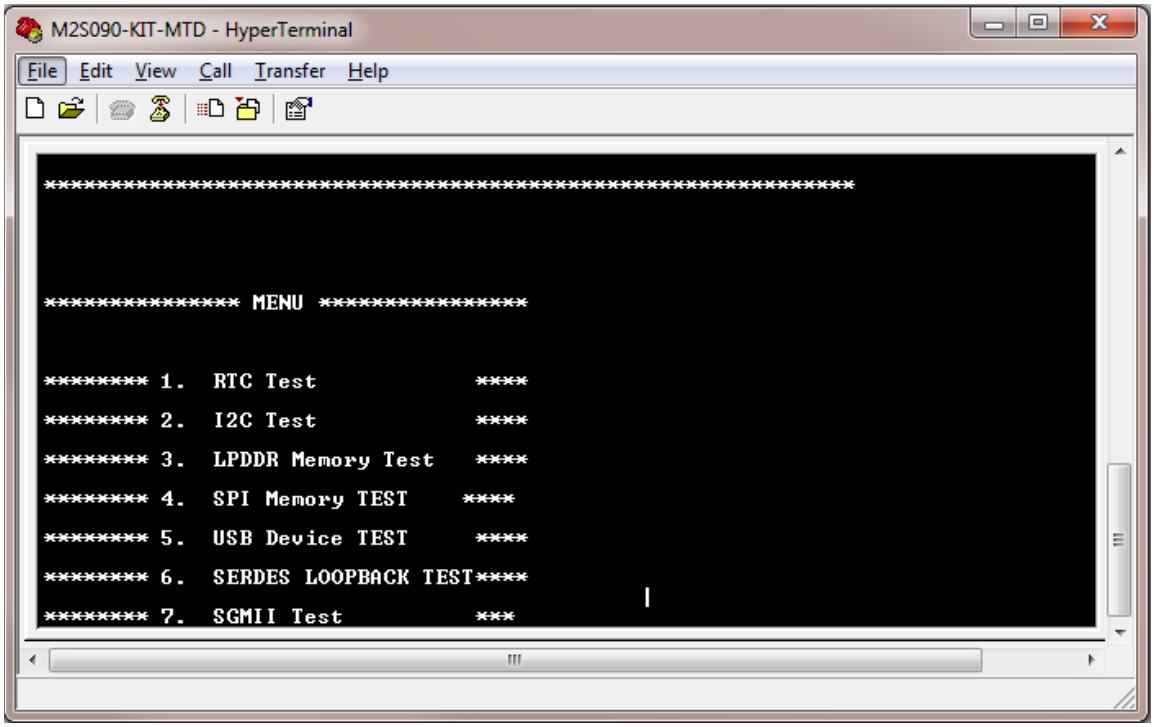

Figure 36 HyperTerminal Window

Jumper Settings

Table 15 describes the jumper settings required to perform the tests on the SmartFusion2 Security Evaluation board.

Table 15 Jumper Settings

Interface	Jumper Settings
HyperTerminal Communication Test	Connect USB cable (mini USB to Type A USB cable) to J18 and connect other end of the cable to the Host PC.
RTC Test	–
I2C Test	Short H1 pin 6-10 and 7-11
LDDR3 Memory Test	–
SPI Memory Test	–
USB Device Test	Connect Micro B to P1 and connect other end of the cable to the Host PC (type A). This cable is required for testing on board USB device interface.
SERDES Loopback Test	Connect J20 to J15 and J16 to J10 using SMA to SMA cable
	Loopback cable (5 Gbps data rate)
SGMII Test	Connect Ethernet cable to J13 and connect other end of the cable to the Ethernet switch or network (1 Gbps)

Once the device is programmed and jumper settings are done, use the following steps to run the manufacturing test:

1. Press the **SW6** reset switch on the M2S090TS-EVAL-KIT to reset and begin the tests.
2. When the set up completed, all tests are listed in the HyperTerminal window as shown in Figure 37. If this message does not appear, press the **SW6** reset switch again. If the message still does not appear, then check all the jumpers and the HyperTerminal settings.

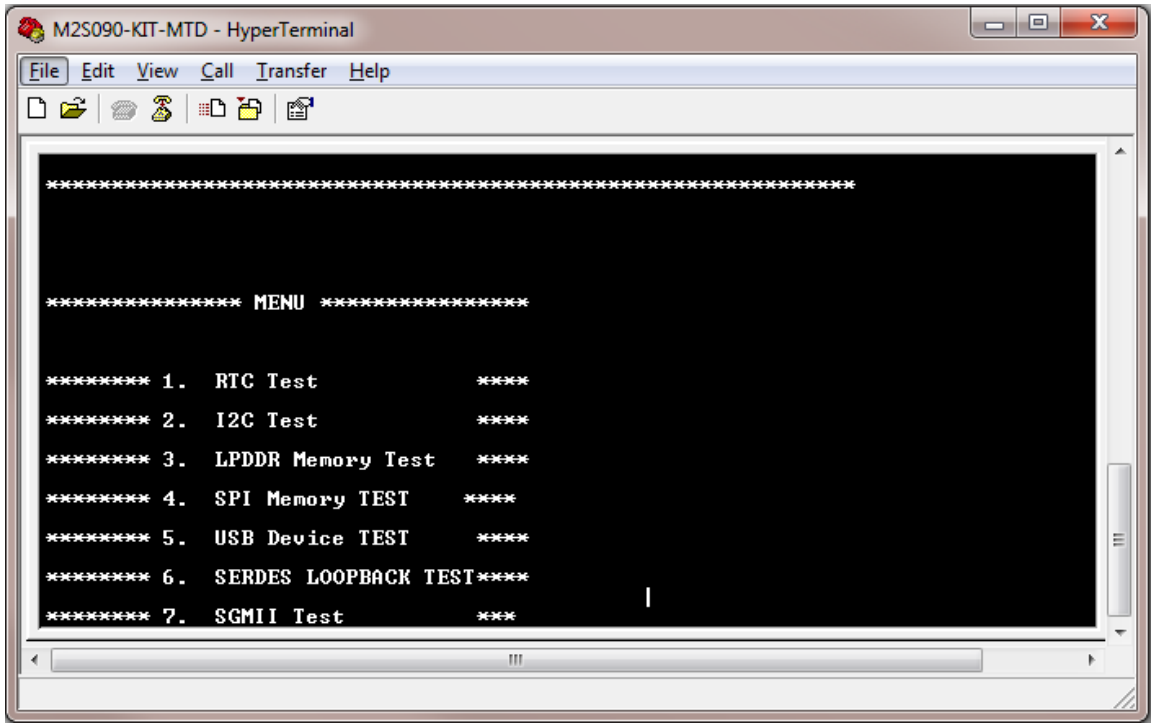

Figure 37 Test Menu

3. Press **1** to run the RTC test. Wait for 5 seconds to complete the test.

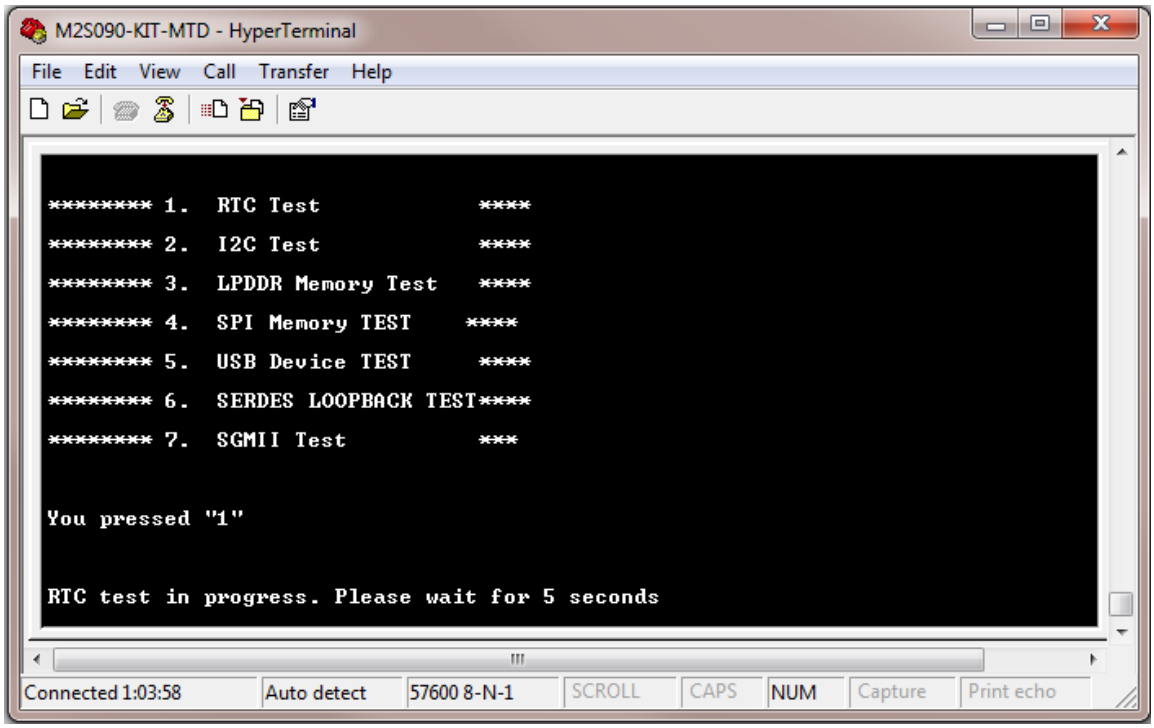

Figure 38 Running RTC Test

4. When the test is passed, a message is displayed as shown in Figure 39.

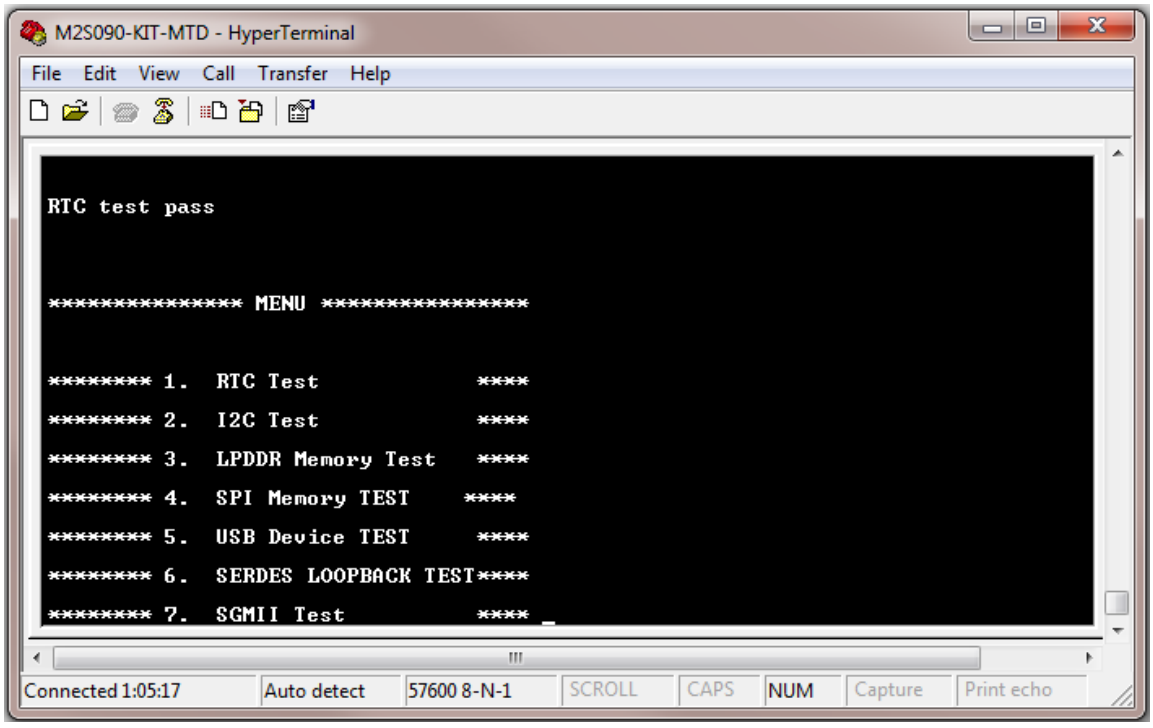

Figure 39 RTC Test Passed

5. Press **2** to run the I^2C loopback test. Refer to Figure 40.

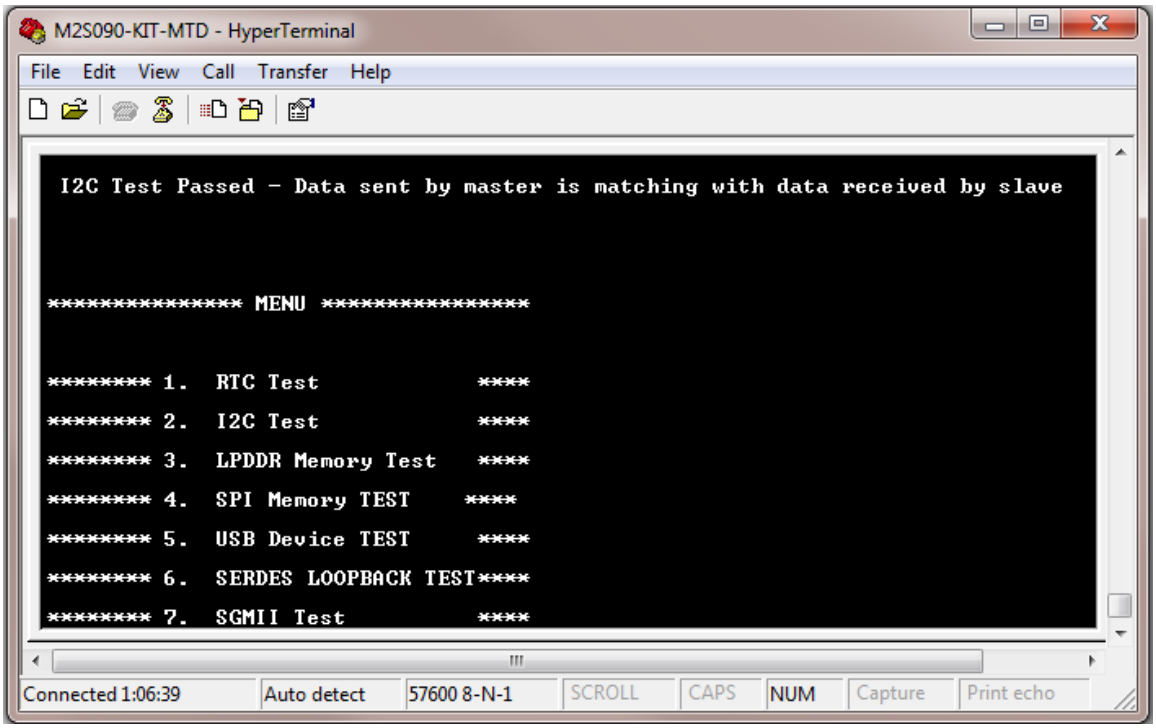

Figure 40 I2C Test Passed

6. Press **3** to run the LPDDR Memory Test.
7. Wait for 1 minute to complete the test. When the test is passed, a message is displayed. Refer to Figure 41.

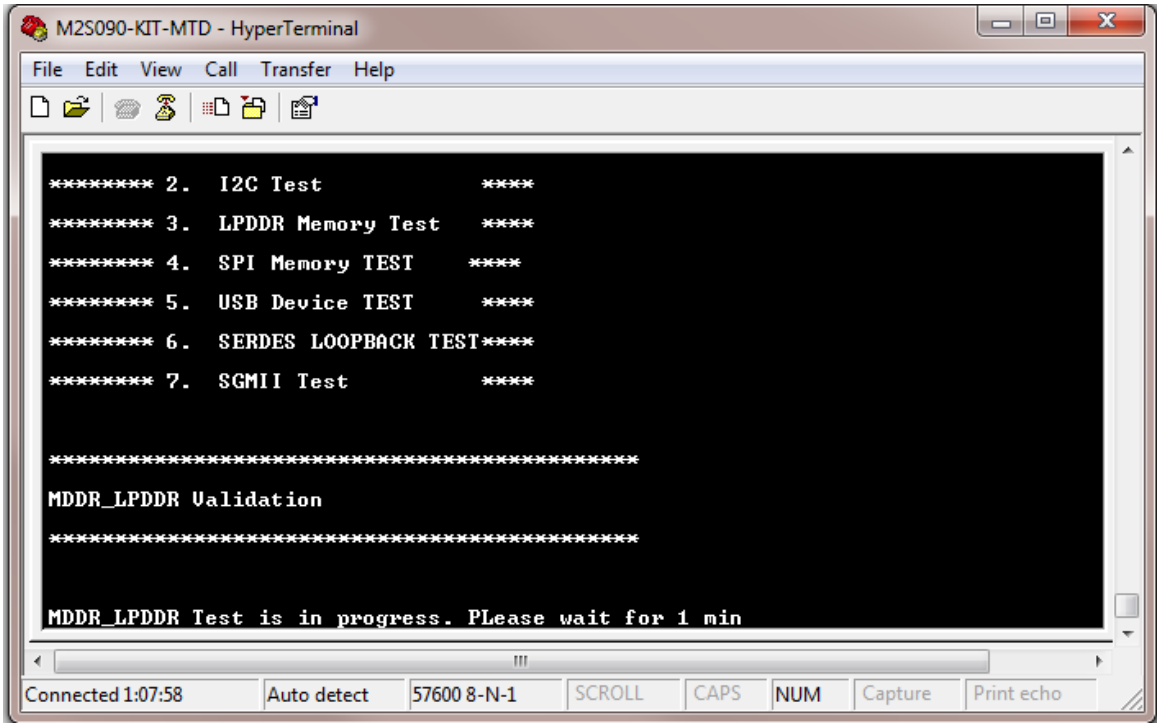

Figure 41 LPDDR Memory Test

8. When the test is passed, a message is displayed. Refer to Figure 42.

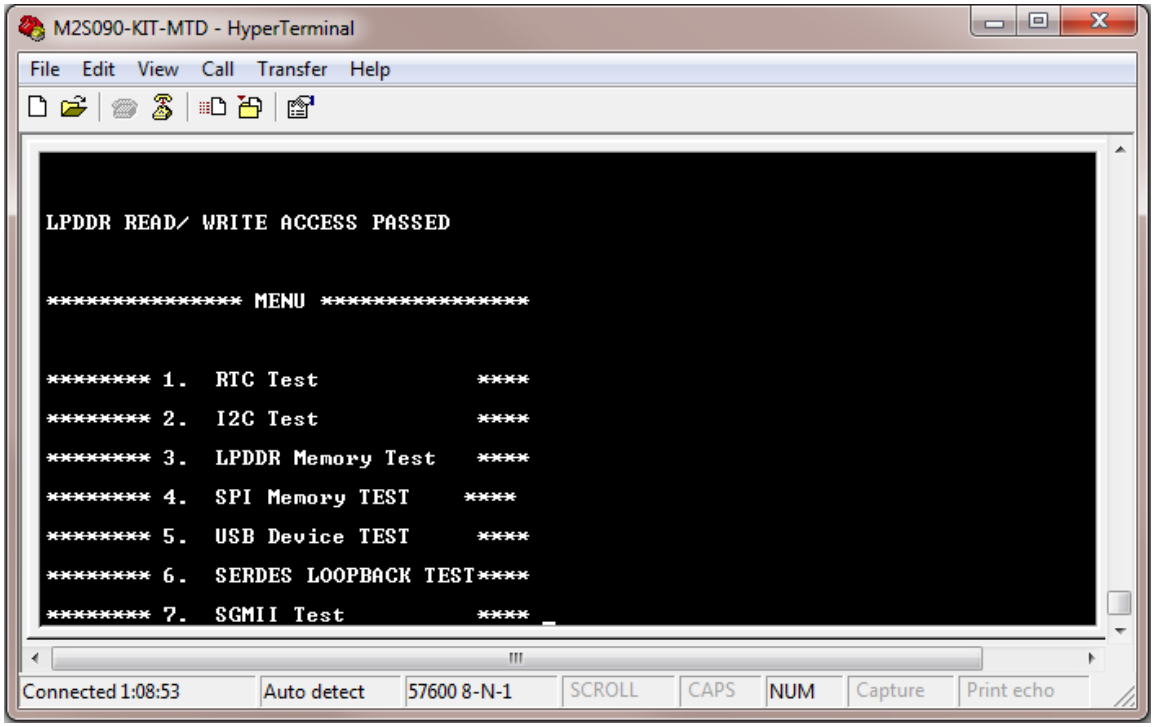

Figure 42 LPDDR Memory Test Passed

9. Press **4** to run the SPI Memory Test.
10. When the test is passed, a message is displayed. Refer to Figure 43.

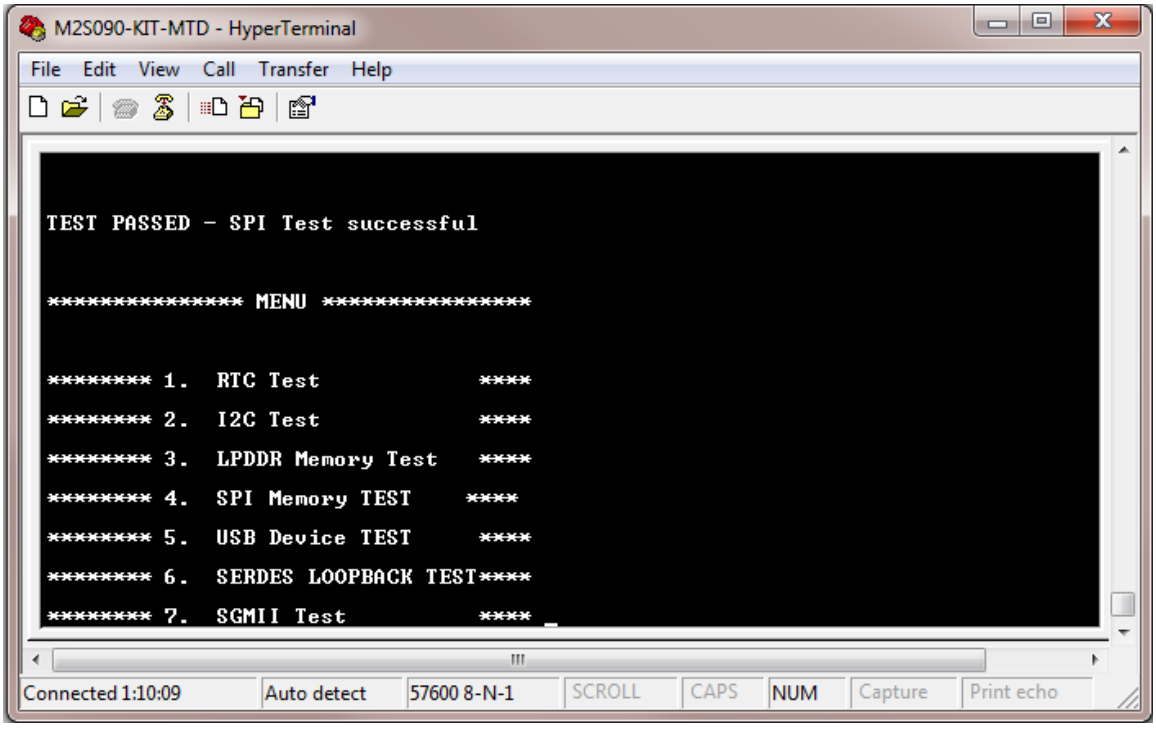

Figure 43 SPI Memory Test Passed

11. Press **6** to run the USB device test.
12. When the test is started, a message is displayed. Refer to Figure 44.

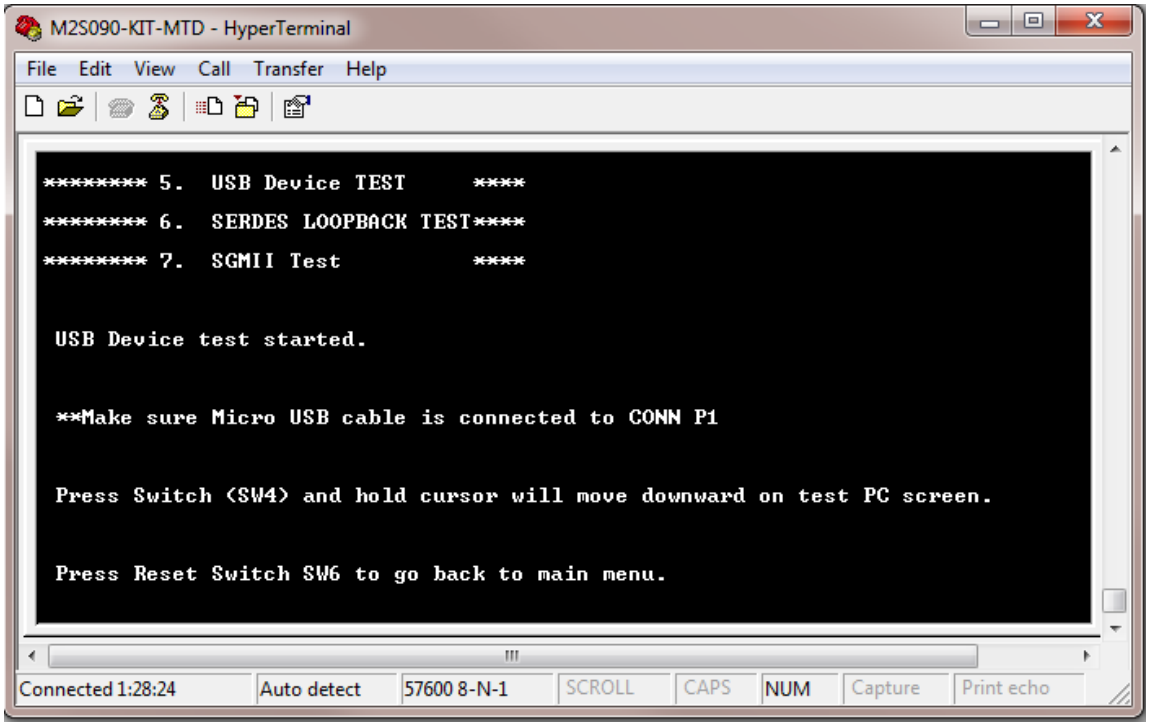

Figure 44 USB Device Test Passed

13. Press and hold the **SW2** switch, on the board and observe the mouse cursor moving to the right side.
14. Press **SW6** reset switch to go back to the main menu.
15. Press **6** to run the SERDES loopback test. Refer to Figure 45.
16. Make sure that the loopback cable is connected. Refer to Jumper Settings.

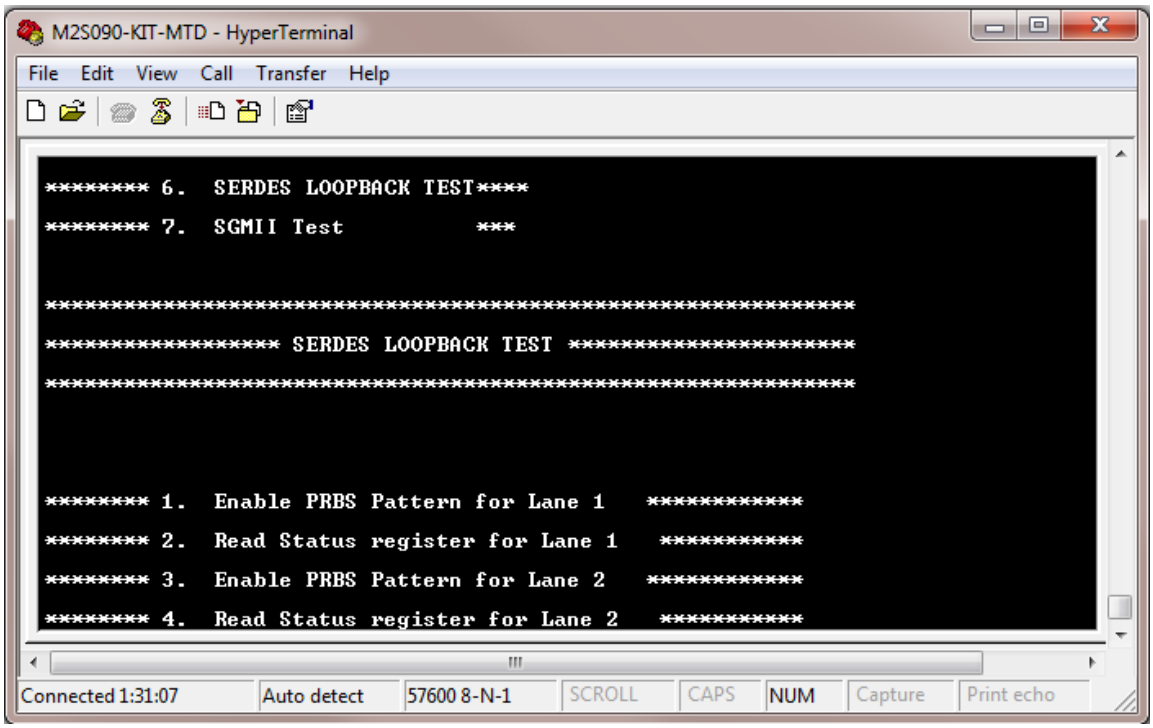

Figure 45 SERDES Loopback Test

17. Press **1** to enable PRBS pattern for Lane 1. Refer to Figure 46.

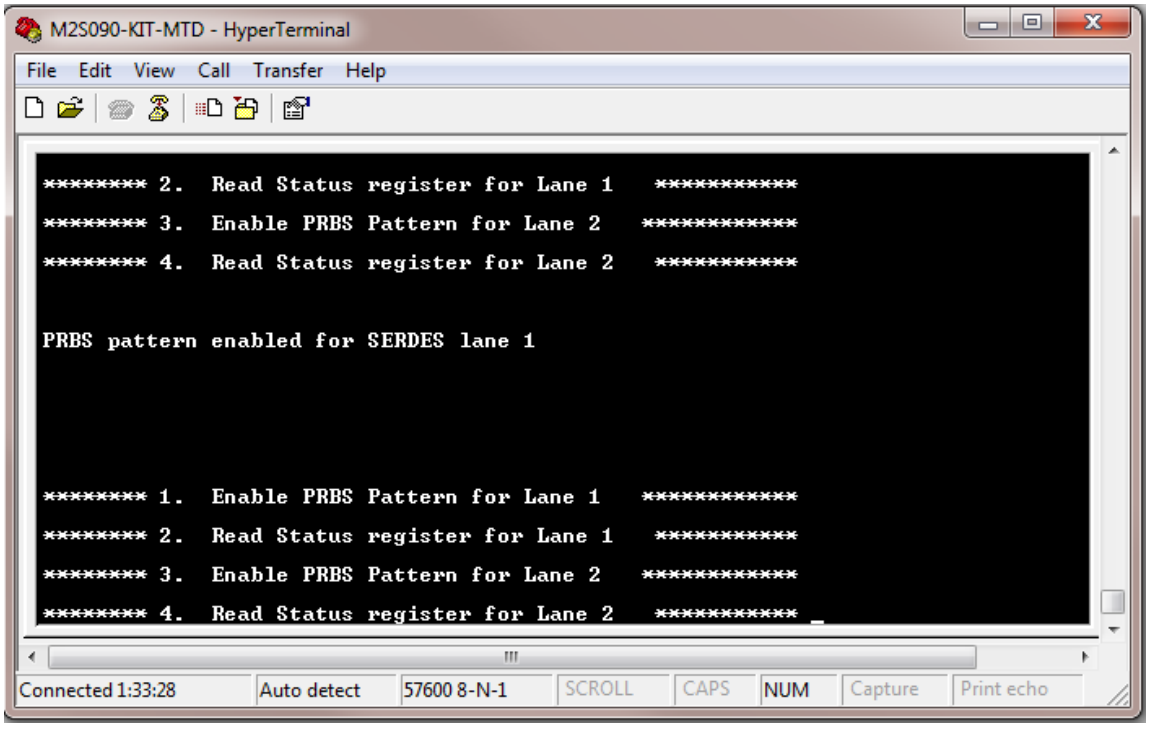

Figure 46 SERDES Lane1 Loopback Test

a. Press **2** to read Status register for Lane 1.

18. When the test is started, a message is displayed. Refer to Figure 47.

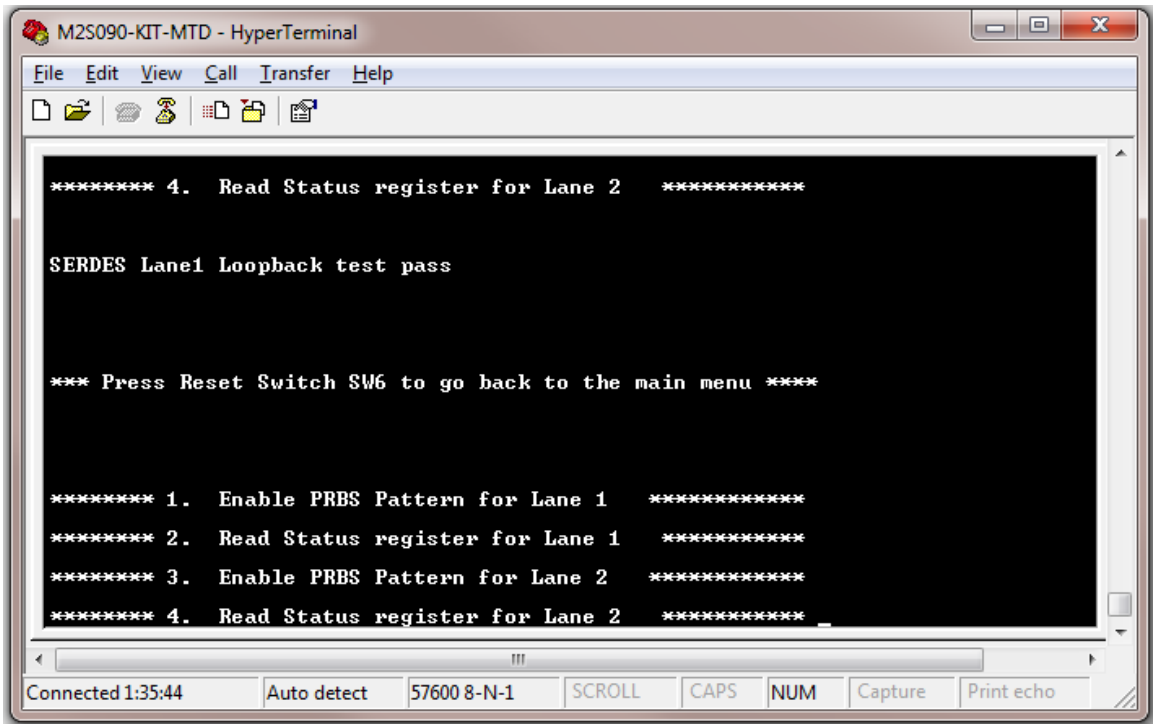

Figure 47 SERDES Lane1 Loopback Test Passed

This message shows loopback test on lane 1 pass.

19. Press **3** to enable PRBS pattern for Lane 2. Refer to Figure 48.

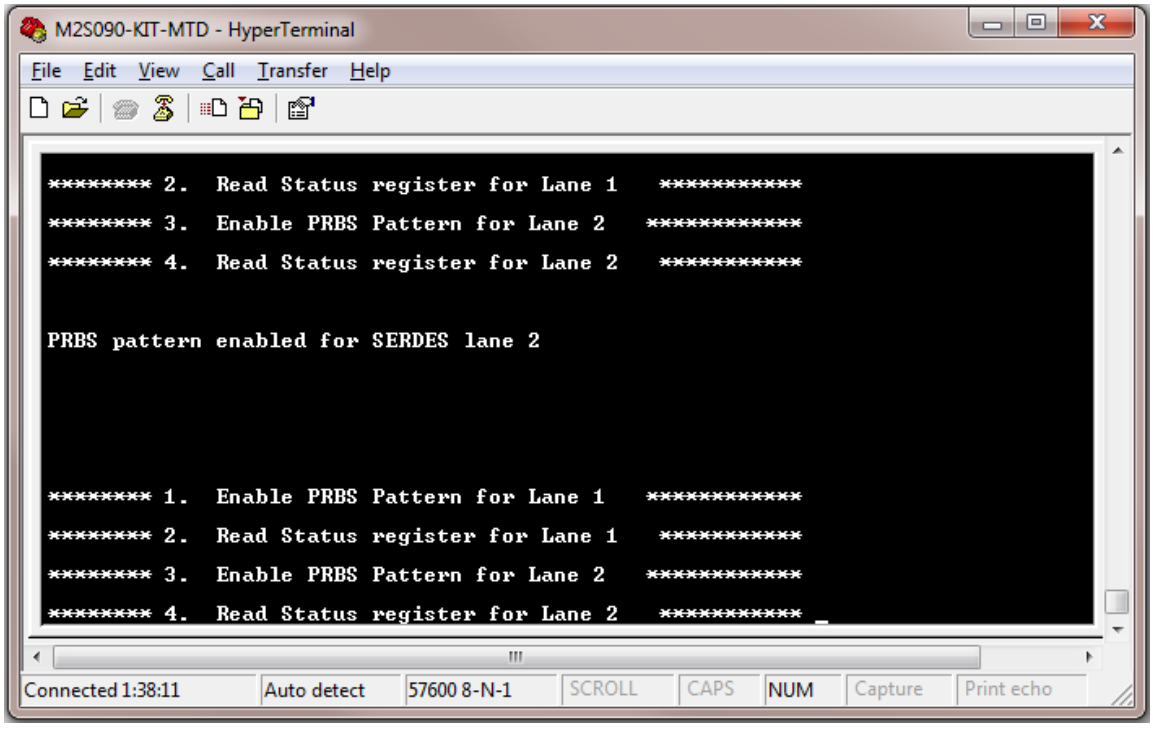

Figure 48 SERDES Lane2 Loopback Test

a. Press **4** to read Status register for Lane 2.

20. When the test is started, a message is displayed. Refer to Figure 49.

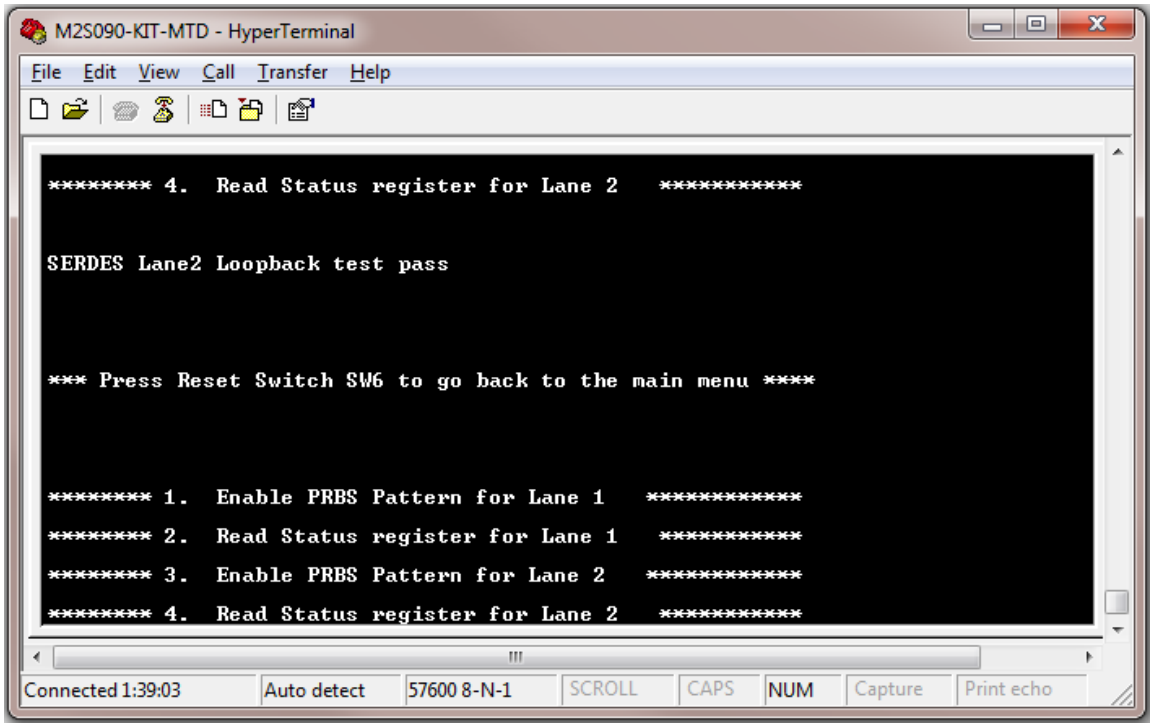

Figure 49 SERDES Lane2 Loopback Test Passed

Note:

- Make sure that SMA connector J20 and J15 are shorted using SMA Cable.
- Make sure that SMA connector J16 and J10 are shorted using SMA Cable.
- Loopback cable used must support 5 Gbps data rate.
- Follow the sequence given in the HyperTerminal.

21. Press **7** to run the SGMII test.

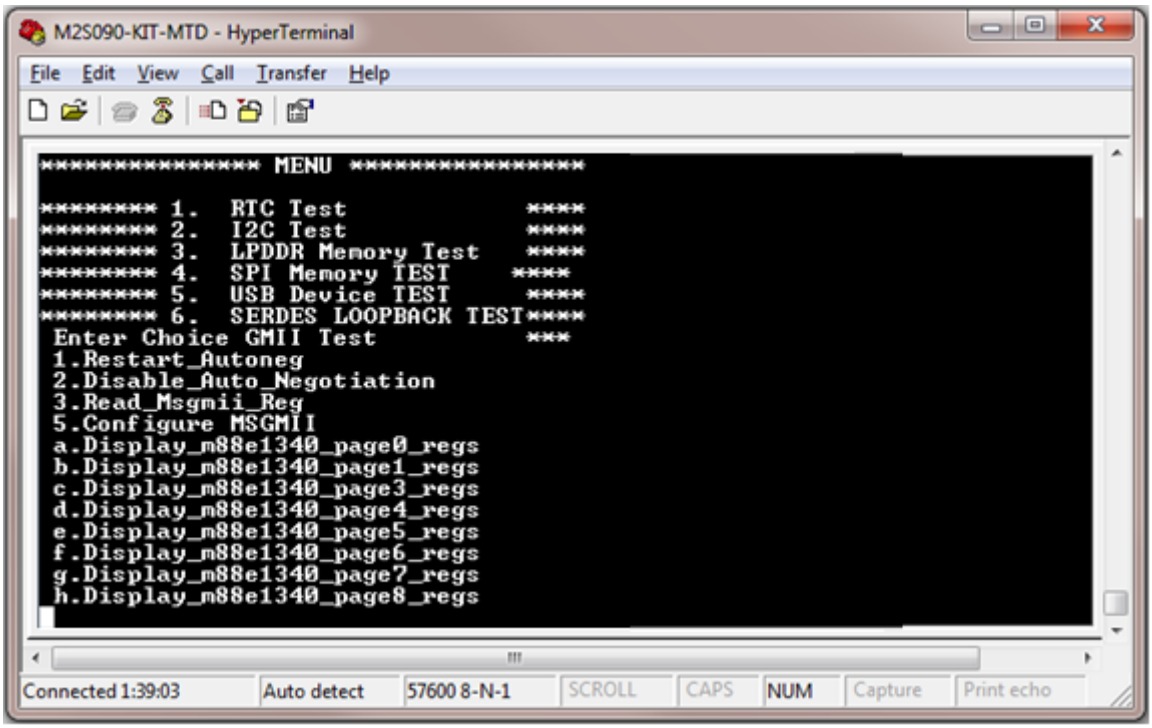

Figure 50 SGMII Test

a. If the message is not displayed, switch **ON** and **OFF** the SW7 power supply switch on the board.
b. Press **7** to repeat the SGMII test.
c. A confirmation message is displayed, Press **n** twice. Refer to Figure 51. When the test is passed, the IP address of the Host PC is displayed.

22. Press **2** on terminal window and then press **y** to repeat the SGMII test. Refer to Figure 51.
23. Press **n** twice on the HyperTerminal window. The Host PC's IP address will be displayed. Refer to Figure 51.

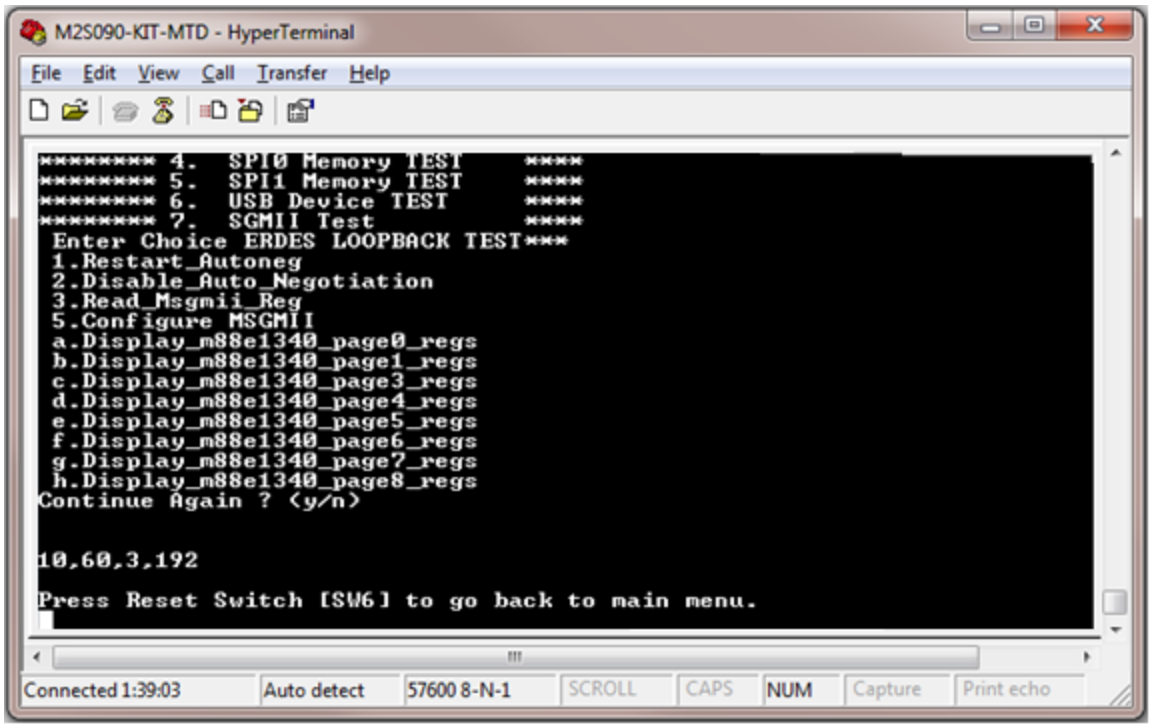

Figure 51 SGMII Test Passed

Note: IP address may vary from one PC to the other PC.

If the IP address is not displayed, perform the following steps to get the IP address.

24. Press **SW6** to go back to the main menu.

Appendix 1 – Running the PCIe Demo Design on Windows

The SmartFusion2 M2S090TS-EVAL-KIT comes with a preloaded PCIe control plane demo design. Refer to Appendix 2 – FPGA Programming using FlashPro4 to reprogram the board with PCIe Control Plane demo, if required.

Connecting the Board to the Host PC

1. After successful programming, power **OFF** the SmartFusion2 Security Evaluation board and shut down the Host PC.
2. Follow the steps to connect the **CON1-PCIe Edge Connector** either to Host PC or laptop:
   a. Connect the **CON1-PCIe Edge Connector** to Host PC PCIe Gen 2 slot or Gen 1 slot as applicable. If the Host PC does not support the Gen 2 compliant slot, the design switches to the Gen 1 slot.
   b. Connect the **CON1-PCIe Edge Connector** to the laptop PCIe slot using the express card adapter. If you are using a laptop, the express card adapters typically support only Gen 1 and the design works on Gen 1 slot.

   CAUTION: Host PC or laptop must be powered OFF while inserting the PCIe Edge Connector. If the system is not powered OFF, the PCIe device detection and selection of Gen 1 or Gen 2 do not occur properly. It is recommended that the Host PC or laptop must be powered OFF during the PCIe card insertion.

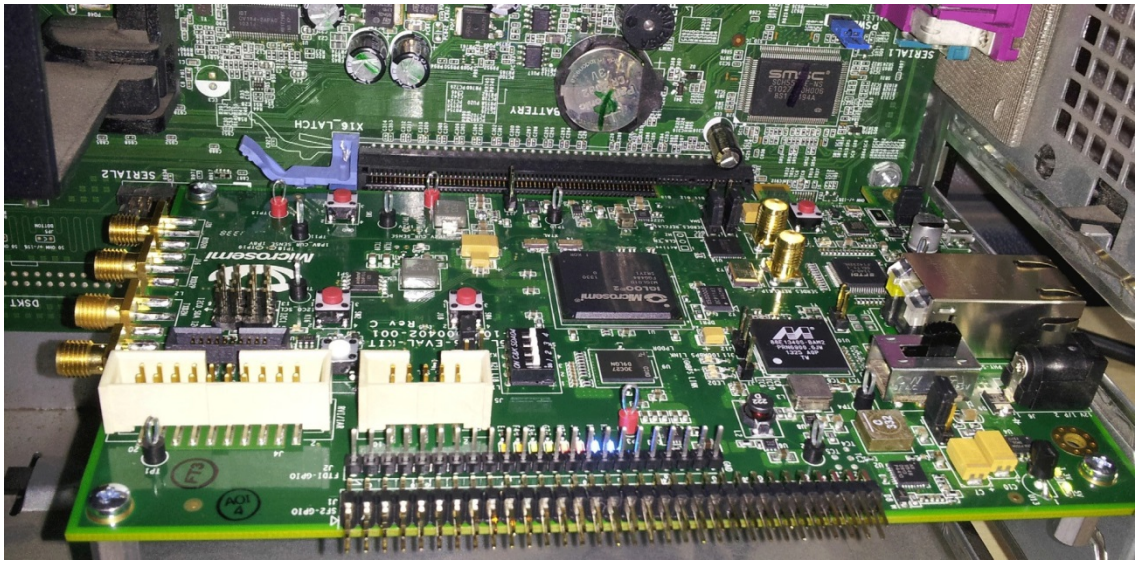

Figure 52 SmartFusion2 Security Evaluation Kit Setup for Host PC

Running the Demo Design

1. Power on the Host PC and open the Host PC Device Manager for PCIe device, as shown in Figure 54. If the PCIe device is not detected, power-cycle the SmartFusion2 Security Evaluation board. Right-click **PCIe Device > Scan for hardware changes** in Device Manager.

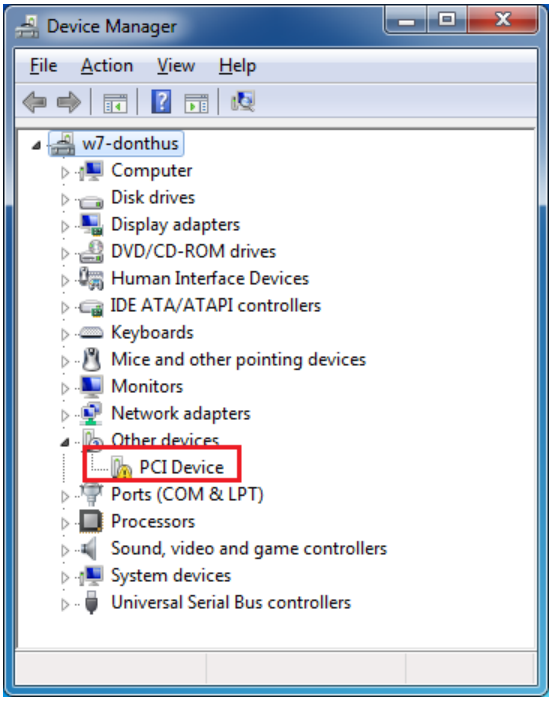

Figure 53 Device Manager

Note:

- If the device is still not detected, check whether or not the BIOS version in Host PC is the latest, and if PCIe is enabled in the Host PC BIOS.
- If the Host PC has any other installed drivers (previous versions of Jungo drivers) for the SmartFusion2 PCIe device, uninstall them.

  Follow the steps to uninstall previous versions of Jungo drivers:

  a. Navigate to device manager and right-click **DEVICE** and select **Uninstall** as shown in Figure 54. The **Confirm Device Uninstall** dialog box is displayed.

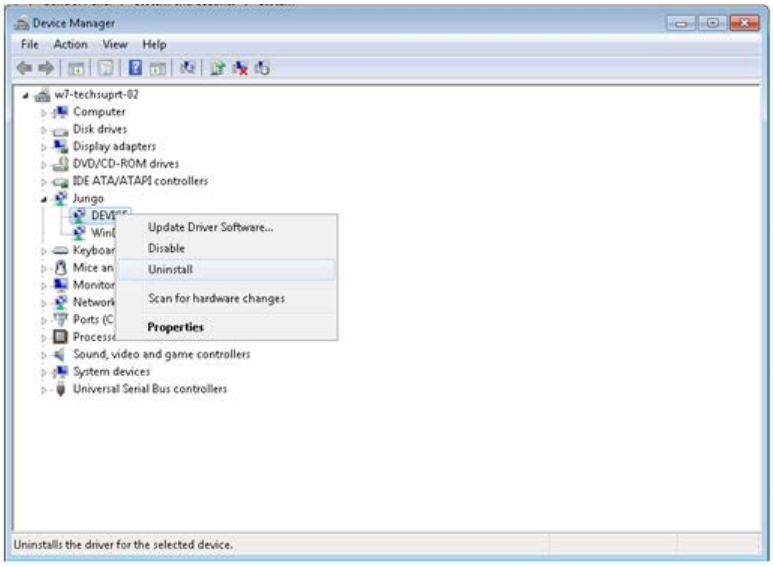

Figure 54 Device Uninstall

b. Select the **Delete the driver software for this device** check box as shown in Figure 55.

c. Click **OK**.

Figure 55 Confirm Device Uninstall

After uninstalling previous Jungo drivers, make sure that the PCIe device is detected in the Device Manager window as shown in Figure 53.

Drivers Installation

The PCIe Demo uses a driver framework provided by Jungo WinDriverPro. To install the PCIe drivers on Host PC for SmartFusion2 Security Evaluation board, use the following steps:

1. Extract the **PCIe_Demo.rar** to C:\ drive. The PCIe_Demo.rar is located in the provided design files: *M2S150_M2S25_PCIe_Control_Plane_DF\Windows_64bit\Drivers\PCIe_Demo.rar*

   Note: Installing these drivers requires the Host PC administration rights.
2. Run the batch file **C:\PCIe_Demo\DriverInstall\Jungo_KP_install.bat**.
3. Click **Install** if the window is displayed as shown in Figure 56.

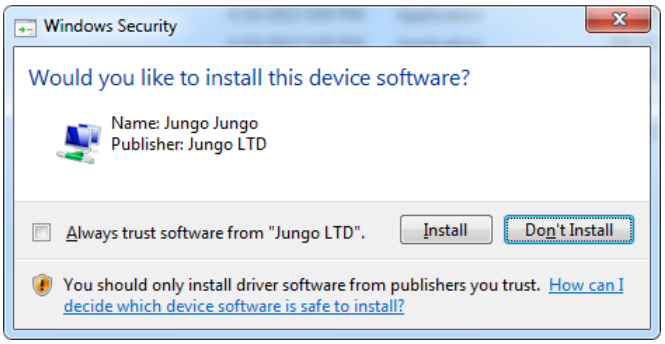

Figure 56 Jungo Driver Installation

Note: If the installation is not in progress, right-click on the command prompt and select Run as administrator. Run the batch file **C:\PCIe_Demo\DriverInstall\Jungo_KP_install.bat** from command prompt.

4. Click **Install this driver software anyway** if the window appears as shown in Figure 57.

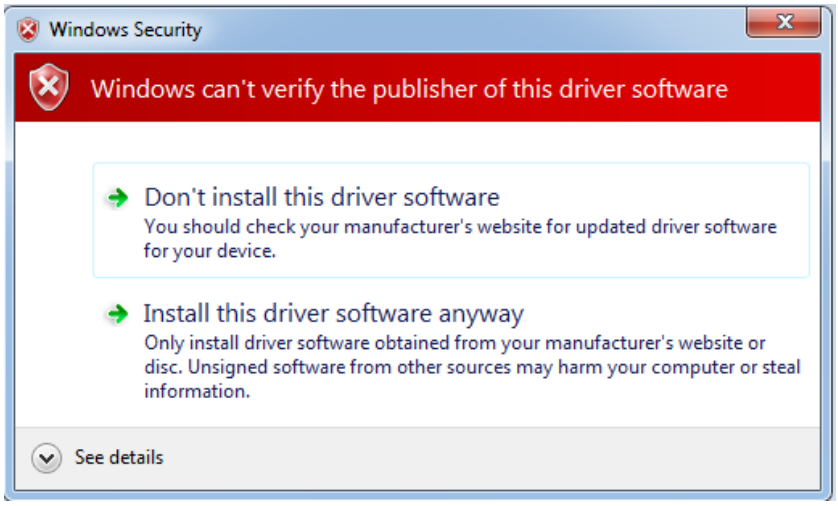

Figure 57 Windows Security

PCIe Demo GUI Installation

The SmartFusion2 PCIe demo GUI is a simple GUI that runs on the Host PC to communicate with the SmartFusion2 PCIe EP device. The GUI provides the PCIe link status, driver information, and demo controls. The GUI invokes the PCIe driver installed on the Host PC and provides commands to the driver according to the user selection.

Use the following steps to install the GUI:

1. Extract the **PCIe_Demo_GUI_Installer.rar** from the provided design files: *M2S150_M2S25_PCIe_Control_Plane_DF\Windows_64bit\GUI*.
2. Double-click the **setup.exe** in the provided GUI installation (*PCIe_Demo_GUI_Installer\setup.exe*). Apply default options as shown in Figure 58.

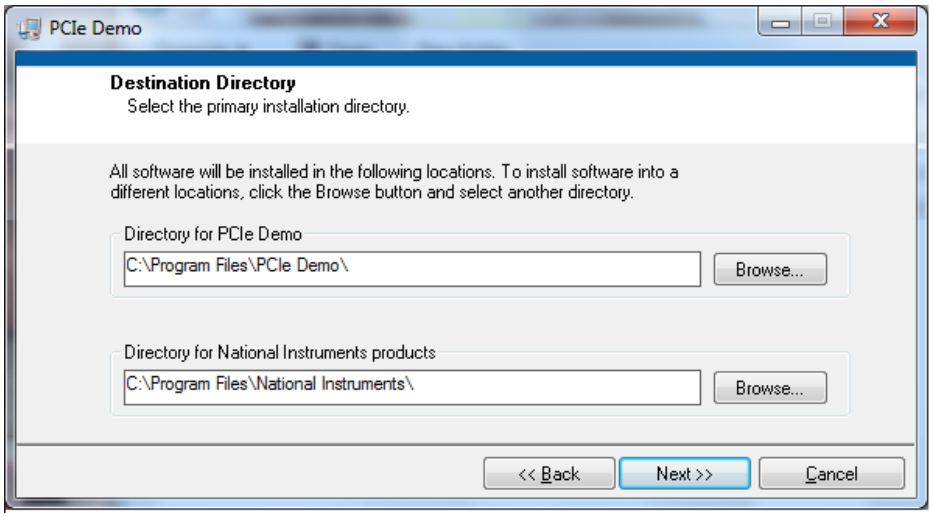

Figure 58 GUI Installation

3. Click **Next** and **Finish** to complete the installation. Figure 59 shows the **Successful GUI Installation** window.

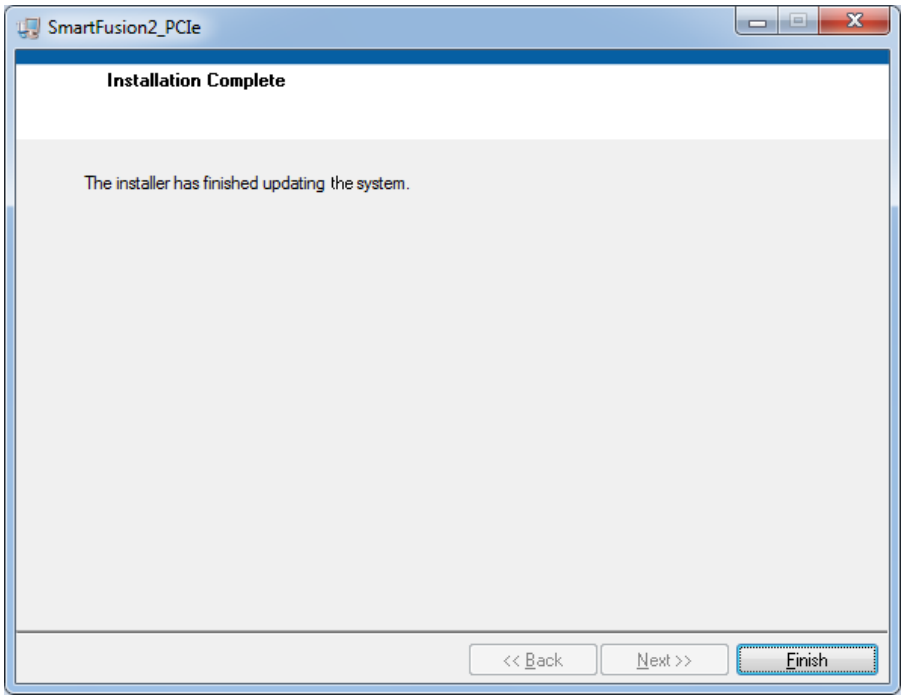

Figure 59 Successful GUI Installation

4. Restart the Host PC.

Running the PCIe GUI

1. Check the Host PC Device Manager for the drivers. If the device is not detected, power-cycle the SmartFusion2 Evaluation board.
2. Right-click **DEVICE > Scan for hardware changes** in Device Manager. Make sure that the board is switched ON.

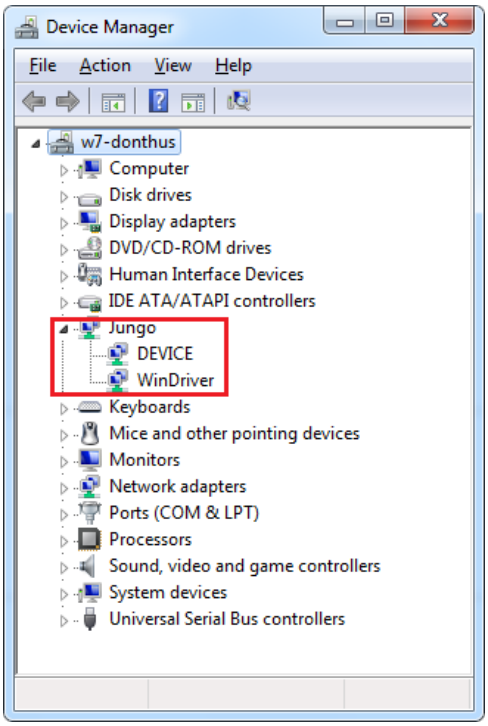

Figure 60 Device Manager - PCIe Device Detection

Note: If a warning symbol is displayed on the DEVICE or WinDriver icon in the Device Manager, uninstall them and start from step1 of Drivers Installation section.

3. Invoke the GUI from **ALL Programs > PCIeDemo > PCIe Demo GUI**. Figure 61 shows the PCIe Demo GUI window.

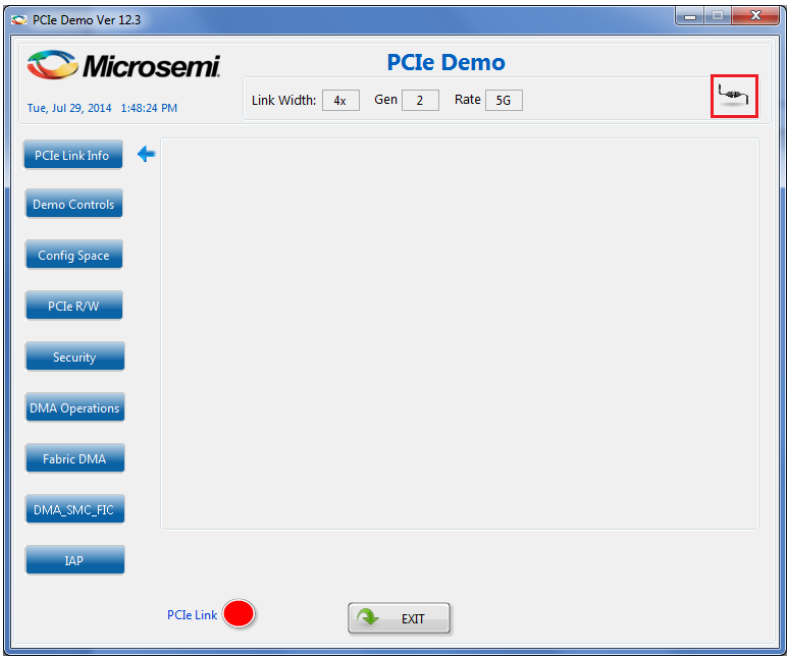

Figure 61 PCIe Demo GUI

4. Click **Connect** icon at the top-right corner of the GUI. The Link Width, Gen, Rate, and Type of Kit are displayed on the GUI as shown in Figure 62.

   Note:

   - The Security Evaluation Kit provides x1 PCIe lane width for configuration.
   - If the Host PC does not support Gen 2 slot, the design automatically changes to Gen 1 slot.

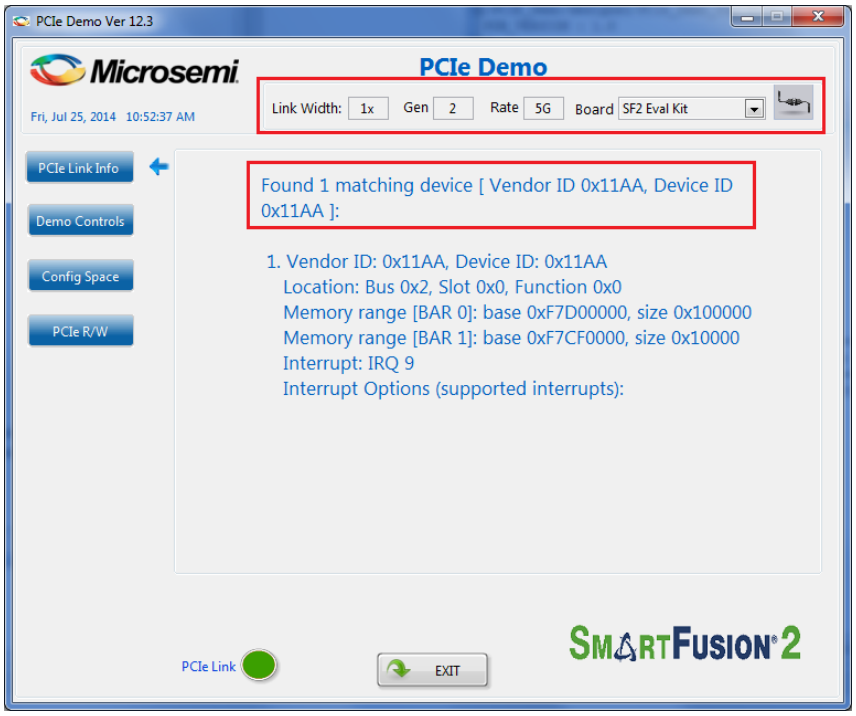

Figure 62 Version Information

5. Click **Demo Controls**. Figure 63 shows the LED options and DIP switch status.

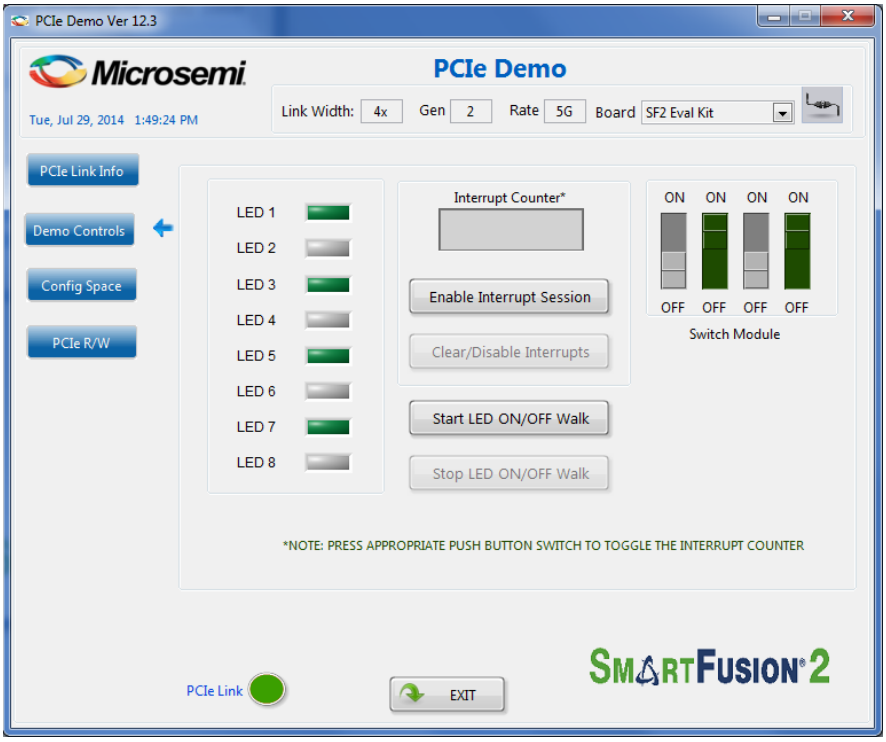

Figure 63 Demo Controls

6. Click LEDs on GUI to **ON/OFF** the LEDs on the SmartFusion2 Security Evaluation board.
7. Click **Start LED ON/OFF Walk** to blink the LEDs on SmartFusion2 Security Evaluation board.
8. Click **Stop LED ON/OFF Walk** to stop the LEDs blinking.
9. Change the DIP switch positions (**1 to 4**) on the SmartFusion2 Security Evaluation board (**SW5**) and observe the similar position of switches in **GUI SWITCH MODULE**.
10. Click **Enable Interrupt Session** to enable the PCIe interrupt.
11. Press the push button **SW4** on the SmartFusion2 Evaluation board and observe the interrupt count in the **Interrupt Counter** field, as shown in Figure 64.

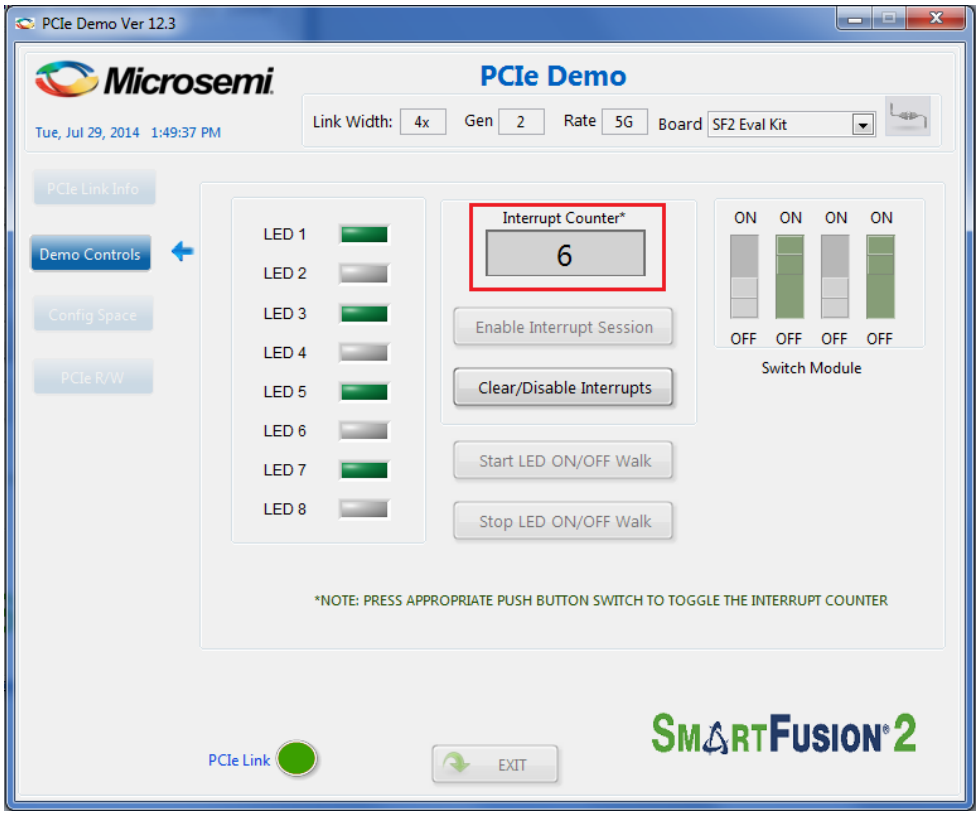

Figure 64 Interrupt Counter

12. Click **Clear/Disable Interrupts** to clear and disable the PCIe interrupts.
13. Click **Config Space** to read details about the PCIe configuration space. Figure 65 shows the PCIe configuration space.

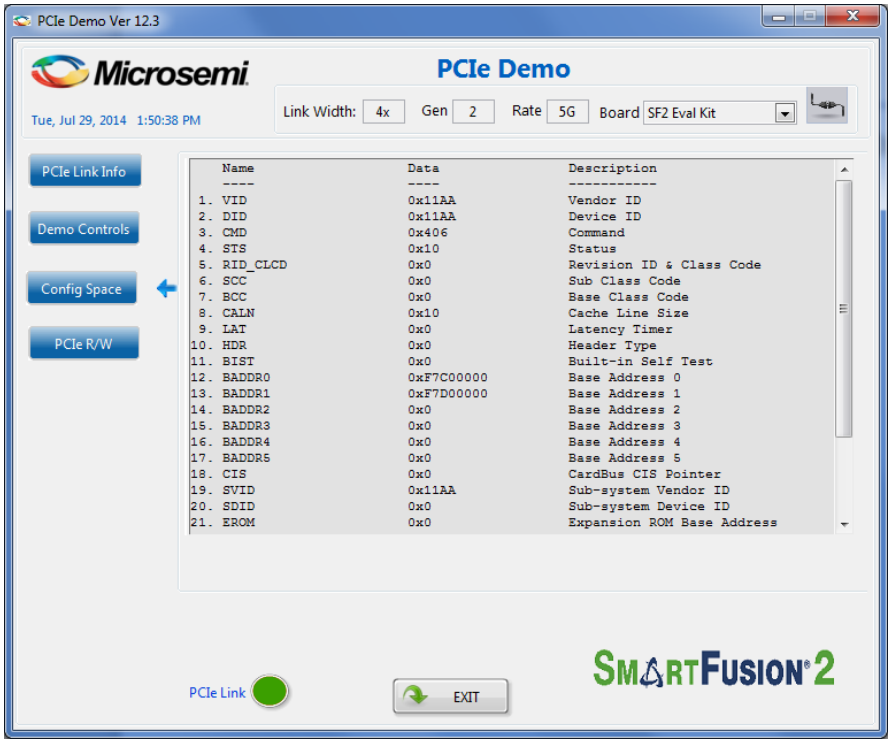

Figure 65 Configuration Space

14. Click **PCIe R/W** to perform read and writes to LSRAM memory through **BAR1** space. Figure 66 shows the **PCIe R/W** window.
15. Enter **Address** between 0x0000 to 0xFFFC range.
16. Enter **Data**. The data field accepts a 32-bit hexadecimal value.

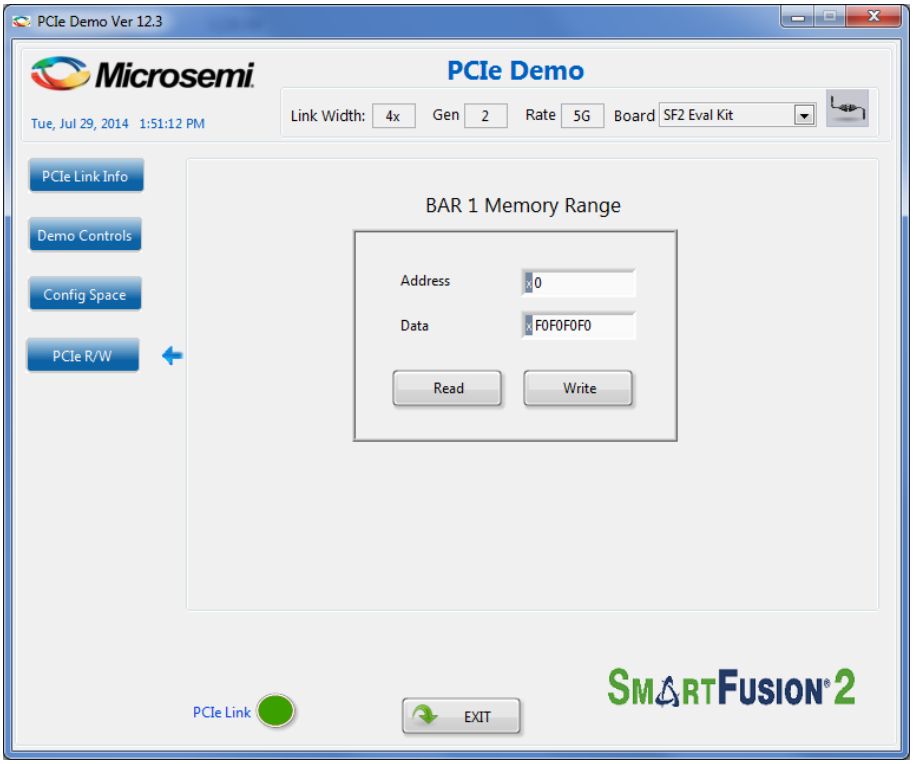

Figure 66 Perform Read and Write to LSRAM Using PCIe

17. Click **Exit** to quit the demo.

Note: For running the demo design on Linux, refer to the *SmartFusion2 SoC FPGA PCIe Control Plane Demo For Advanced Dev Kit and Evaluation Kit Demo Guide*.

Appendix 2 – FPGA Programming using FlashPro4

M2S090TS-EVAL-KIT can be programmed or debugged using the FlashPro4 programmer.

Board Setup

Snapshot of the SmartFusion2 Security Evaluation board with the complete set up is shown in Figure 67.

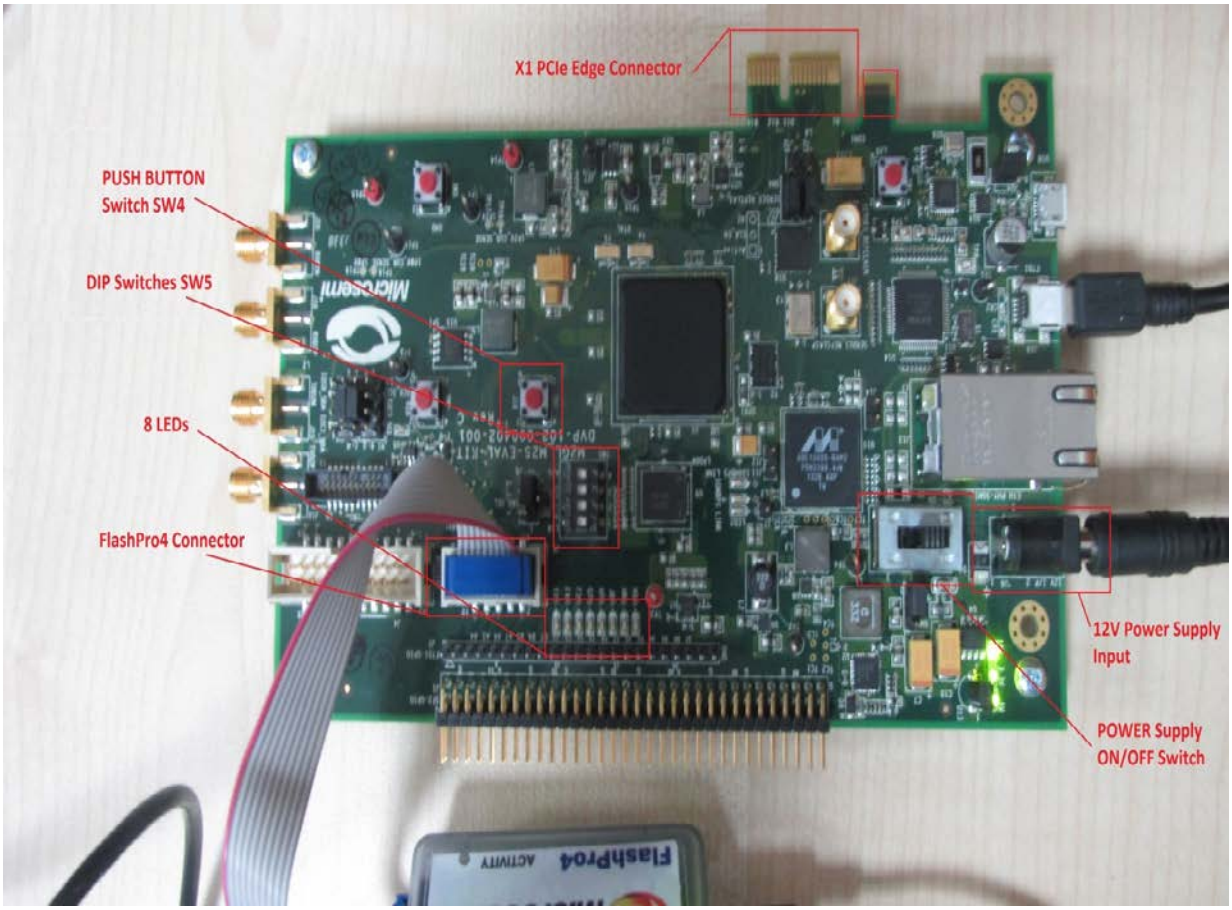

Figure 67 Lining up the SmartFusion2 Evaluation Board

Note: The Notch (highlighted in red) does not go into the adapter card.

Programming the Device using Embedded FlashPro4

FlashPro4 must be installed on the Host PC to program the device using FlashPro4.

To program the board using FlashPro4, connect the FlashPro4 header to J5

1. Switch **ON** the **SW7** power supply switch.
2. Open the **FlashPro4** software.

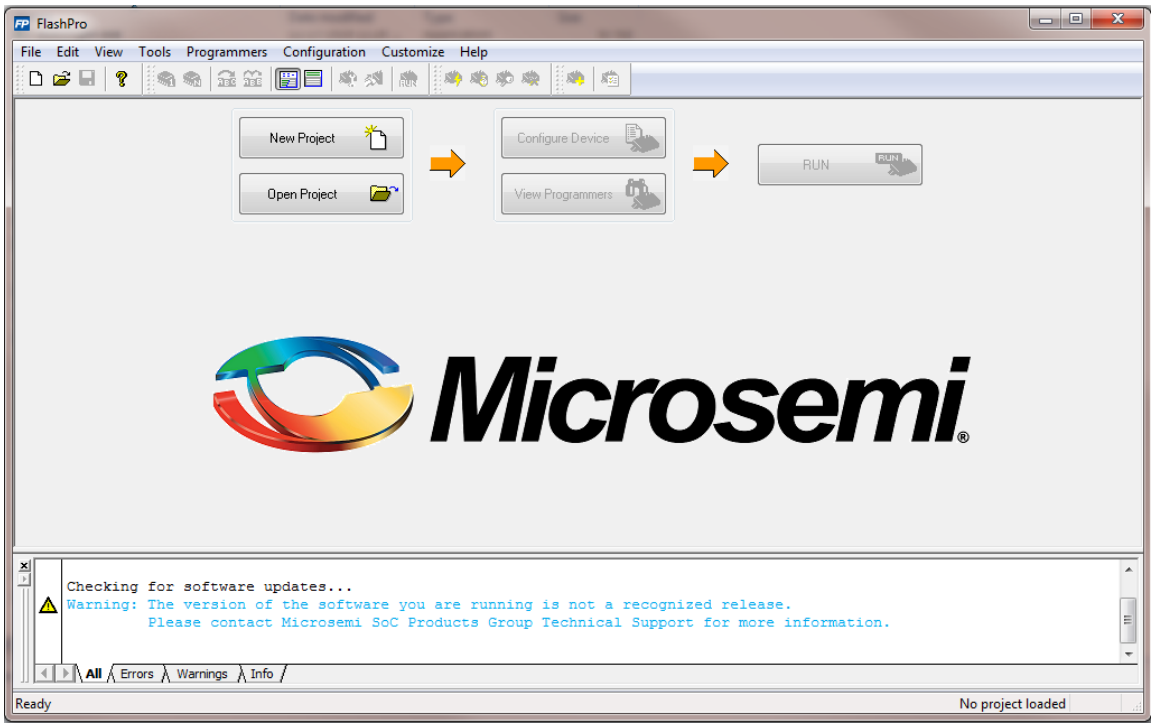

Figure 68 FlashPro Window

3. Click **New Project** to create a new project. Refer to Figure 69.

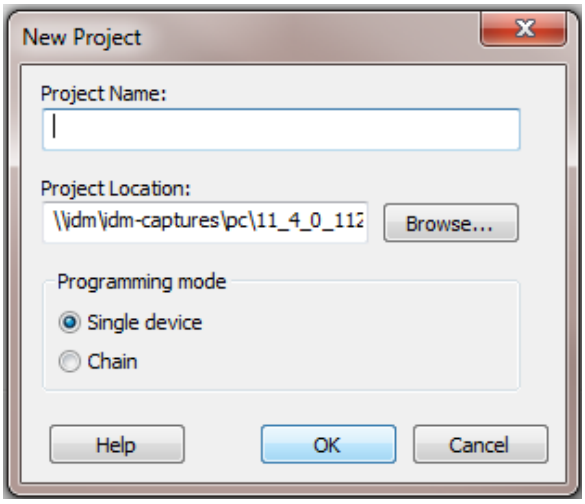

Figure 69 Creating a New Project

a. Enter the **Project Name**.
b. Select **Single device** as the Programming mode and click **OK**.
4. Click **Configure Device**.

Figure 70 Configuring the Device

a. Click **Browse** and select the `M2S090_EVAL_KIT_MTD_top_rev1.stp` file from the **Load Programming File** window.

5. Click **Program** to program the device.
6. Once the device is programmed successfully, **Run Program PASSED** status is displayed.

List of Changes

The following table lists critical changes that were made in the current version of this User Guide.

Revision	Changes	Page
Revision 1 (January 2015)	Initial release.	N/A

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Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA

Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
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