UG0786
User Guide
PolarFire FPGA Splash Kit

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Figures

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 4.0

Following is a list of changes that are made in this revision.

- Updated Installing PowerMonitor, page 28
- Updated About Microsemi PowerMonitor GUI, page 28

1.2 Revision 3.0

Revision 3.0 is published in November 2019. Following is a list of changes that are made in this revision.

- Updated the MPF300TS-1FCG484EES device name with MPF300T-1FCG484E across the document.
- Removed Flash*Freeze mode references from this document.

1.3 Revision 2.0

The following was a summary of the changes made in this revision.

- Corrected the DIP switch label to SW8 in DIP Switches (SPST), page 18 and updated Figure 16, page 19 to indicate ON and OFF directions.
- Updated the Transceivers, page 11 section to include the supported PCIe protocol and added cross-references to PolarFire PCI Express and Transceiver user guides.
- Added Table 6, page 9 that lists the suggested power regulators.

1.4 Revision 1.0

The first publication of this document.

2 Getting Started

The Microsemi PolarFire® FPGA Splash Kit (MPF300-SPLASH-KIT) is an RoHS-compliant, cost-optimized kit with general-purpose interfaces that enables you to evaluate the basic features of the PolarFire family of FPGAs. The PolarFire Splash Kit supports the following interfaces:

- PCI Express Gen1 and Gen2
- 1 GbE
- DDR4 memory
- FMC LPC with one transceiver lane
- UART interface to FTDI device
- SPI interface to SPI flash device

The PolarFire device is programmed using the on-board FlashPro5 programmer. The on-board FlashPro5 programmer is used to develop and debug embedded applications using SoftConsole, Identify, or SmartDebug.

2.1 Kit Contents

The following table lists the contents of the PolarFire Splash Kit.

Table 1 • **Kit Contents**

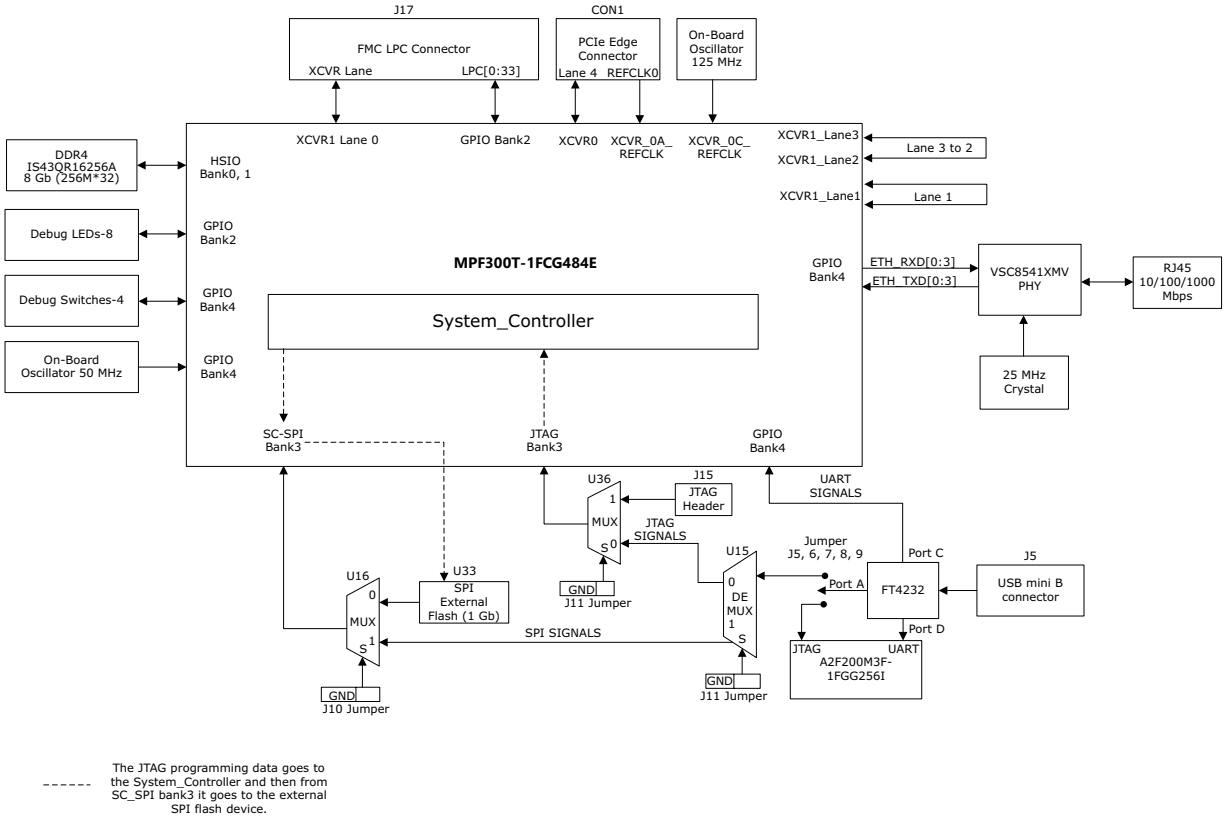
Item	Quantity
PolarFire Splash Board featuring the MPF300T-1FCG484E device with 300K logic elements	1
12 V/5 A wall-mounted power adapter	1
USB 2.0 A male to mini-USB B cable for UART/power interface (up to 1 A) to PC	1
Quickstart card	1
One-year Libero® Gold software license[1]	1

1. License value USD 995. Supports PolarFire 100K LE devices, 200K LE devices, and the MPF300TS-1FCG1152I/EES and MPF300TS-1FCG4842E/EES kit devices.

2.2 Block Diagram

The following block diagram shows all the components of the PolarFire Splash Board.

Figure 1 • **PolarFire Splash Board Block Diagram**



2.3 Web Resources

For more information about the PolarFire Splash Board, see *PolarFire Splash Kit webpage*.

2.4 Board Overview

The PolarFire Splash Board features a PolarFire MPF300T-1FCG484E FPGA with the following capabilities:

- 20-Kb dual-port or two-port LSRAM block with a built-in single error correct double error detect (SECDED) capability
- 64 × 12 two-port µSRAM block implemented as an array of latches
- 18 × 18 multiply-accumulate (MACC) block with a pre-adder, a 48-bit accumulator, and an optional 16 deep × 18 coefficient RO
- Built-in µPROM, modifiable at program time and readable at run time, for user data storage
- Digest integrity check for FPGA, µPROM, and sNVM
- Low-power features:
  - Low device static power
  - Low inrush current

- Low power transceivers
- High-performance communication interfaces

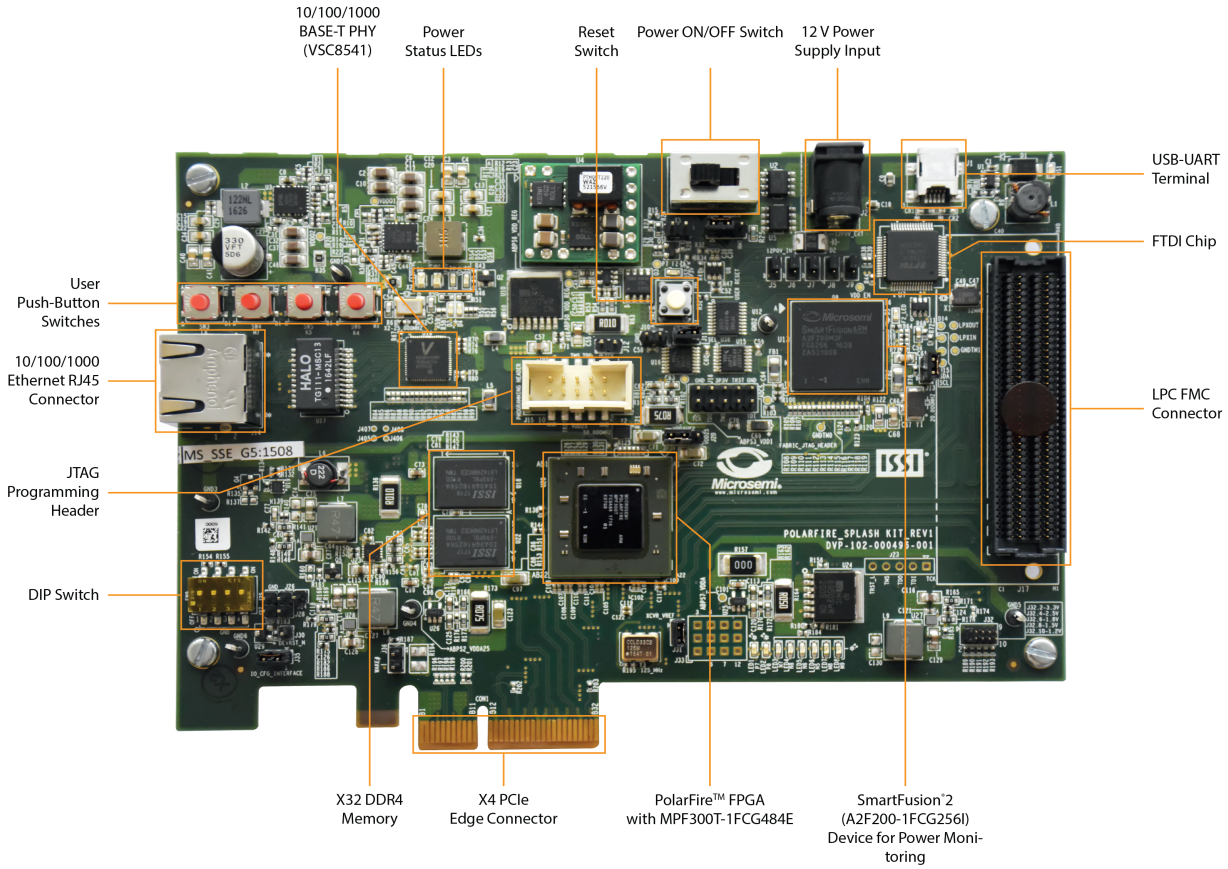
The PolarFire Splash Board supports several standard interfaces, including:

- VSC8541 with an RJ45 connector for 10/100/1000 Mbps Ethernet
- One full-duplex transceiver lane connected through FMC LPC connector
- FMC LPC connector
- DDR4 memory
- Power sequence and monitor module
- PCIe edge connector with four lanes
- One SPI flash device

The PolarFire Splash Board has 12 layers, all of which are made of the Nelco 13 dielectric material.

The following illustration highlights various components of the PolarFire Splash Board.

Figure 2 • **PolarFire Splash Board**



The following table lists the important components of the PolarFire Splash Board.

Table 2 • **PolarFire Splash Board Components**

Component	Label on Board	Description
Featured Device		
PolarFire FPGA		MPF300T-1FCG484E
Power Supply and Monitoring		
12 V power supply input	J2	The board is powered by a 12 V power source using an external +12 V/5 A DC jack.
ON/OFF switch	SW1	Power ON/OFF switch from +12 V external DC jack.

Table 2 • **PolarFire Splash Board Components *(continued)***

Component	Label on Board	Description
Power-monitoring FPGA	U13	Microsemi SmartFusion® FPGA (A2F200M3F-1FGG256I) used for power sequence and monitoring the voltage rails on the PolarFire Splash Board.
Clocks		
On-board 50-MHz clock oscillator	Y2	50-MHz clock oscillator with single-ended output.
OSC	Y3	125-MHz oscillator (differential LVDS output) which is the input to the DS08MB200TSQ clock MUX buffer.
FPGA Programming and Debugging		
USB-UART terminal	J1	FTDI programmer interface to program the PolarFire device based on the jumper settings.
SPI flash	U33	1-Gb Micron MT25QL01GBBB8ESF-0SIT SPI flash memory device connected to SPI pins on bank3 of the PolarFire device.
FT4232H	U7	USB-to-quad serial ports in various configurations.
JTAG programming header	J15	Header to program and debug the PolarFire device using FlashPro4 or FlashPro5. The appropriate programmer (FlashPro4 or FlashPro5) must be selected in the FlashPro software.
Communication Interfaces		
x4 PCIe edge connector	CON1	PCIe edge connector with four XCVR0 lanes.
One 10/100/1000 Ethernet RJ45 connector	J14	Ethernet (RJ45) jack with external magnetics interfacing with Microsemi 10/100/1000 BASE-T PHY (VSC8541) in RGMII mode. The PHY interfaces with the Ethernet ports of the PolarFire device.
FMC LPC connector	J17	FMC connector with one XCVR lane and 34 differential pairs (LPC[0:33])
Memory Chips		
DDR4 Memory	U18 and U22	Two 4-GB (IS43QR16256A 256M × 16) chips are connected in Fly-by topology with a 32-bit data bus for storing data bits. For more information, request the datasheet from the *ISSI website*.
General Purpose I/O		
Switches	SW3, SW4, SW5, and SW6	Push-button switches for user-interface debugging applications.
DIP Switches	SW8	Eight DIP switches for testing.
Light-emitting diodes (LEDs)	LED4 to LED11	Eight active-high LEDs connected to some of the user I/Os for debugging, and twelve active high LEDs used for indicating power supply.
Reset switch	SW2	Push-button system reset for the PolarFire device. Users must program thi.s GPIO for PolarFire device reset function.

2.5 Handling the Board

Pay attention to the following points while handling or operating the board to avoid possible damage or malfunction:

- Handle the board with electrostatic discharge (ESD) precautions to avoid damage. For information about using the board with ESD precautions, see https://www.microsemi.com/document-portal/doc_view/126483-esd-appnote.
- Power down the board to switch between programming headers J17 and PCIe CONN (CON1).

2.6 Operating Temperature

A future version of this document will have information on this topic.

2.7 Powering Up the Board

The PolarFire Splash Board is powered up using either the 12 V DC jack or the PCIe connector.

To power up the board, connect the 12 V DC jack to the board.

Install the software required for developing designs and set the jumpers for the pre-programmed design. For more information, see Installation and Settings, page 7.

3 Installation and Settings

This section provides information about the software and hardware settings required to run the pre-programmed demo design on the PolarFire Splash Board.

3.1 Software Settings

Download and install the latest release of Microsemi Libero® SoC PolarFire software from the Microsemi website, and register for a free one-year Gold License to the Libero software. The Libero SoC PolarFire installer includes FlashPro5 drivers. For instructions about installing Libero SoC PolarFire and SoftConsole, see the *Libero Software Installation and Licensing Guide*. For instructions about how to download and install Microsemi DirectCores and driver firmware cores on the PC where Libero SoC is installed, see the *Installing IP Cores and Drivers User's Guide*.

3.2 Hardware Settings

This section provides information about jumper settings, switches, LEDs, and DIP switches on the PolarFire Splash Board.

3.2.1 Jumper Settings

Connect the jumpers according to the settings specified in the following table.

Table 3 • **Jumper Settings**

Jumper	Description	Pin	Default Setting
J5, J6, J7, J8, and J9	Jumpers to select the PolarFire JTAG or A2F JTAG	Close pin 1 and 2 for programming the power sequence and monitoring chip through the FTDI. Close pin 2 and 3 for programming the PolarFire FPGA through FTDI. Always retain the default jumper setting.	Open Closed
J11	Jumper to select the external JTAG or the on-board FTDI chip for programming the PolarFire device	Close pin 1 and 2 for programming through the FTDI chip. Open pin 1 and 2 for programming through an external FlashPro4 or FlashPro5 device.	Closed
J10	Jumper to select between FTDI chip or external SPI Flash to program the device	Close pin 1 and 2 for programming through the external SPI flash. If J10 is open, it allows SPI slave programming using the FTDI chip. However, this feature is not available in PolarFire devices yet. It is expected to be supported in future releases.	Open
J3	Jumper to select the core voltage	Close pin 1 and 2 for 1.05 V. Open pin 1 and 2 for 1.0 V.	Open
J4	Jumper to select the on-board slide switch or remote power ON/OFF	Close pin 1 and 2 for manual power switching using SW1. Close pin 2 and 3 for remote power switching using the GPIO capability of the A2F200M3F-1FGG256I chip.	Closed Open

Table 3 • **Jumper Settings**

Jumper	Description	Pin	Default Setting
J32	Jumper to select the PolarFire VCCIO voltage (VCCIO_LPC_VADJ) to 1.2V, 1.5V, 1.8V, 2.5V, or 3.3V	Close pin 1 and 2 for 3.3 V. Close pin 3 and 4 for 2.5 V. Close pin 5 and 6 for 1.8 V. Close pin 7 and 8 for 1.5 V. Close pin 9 and 10 for 1.2 V.	Closed Open Open Open Open

For the locations of various jumpers and test points on the PolarFire Splash Board, see Figure 17, page 23.

3.2.2 Power Supply LEDs

The following table lists the power supply LEDs on the PolarFire Splash Board.

Table 4 • **Power Supply LEDs**

LED	Description
DS1 - Green	5V_F2 rail (for A2F200 device)
DS3 - Green	3.3 V rail
DS4 - Green	12 V rail
DS5 - Green	5 V rail
DS6 - Green	1 V rail

3.2.3 Test Points

The following test points available on the PolarFire Splash Board:

- GND1
- GND3
- GND4
- GND5
- GND6

3.3 Power Sources

The PolarFire Splash Board uses Microsemi power supply devices. For more information about these power supply devices, see *Microsemi Power Management web page*.

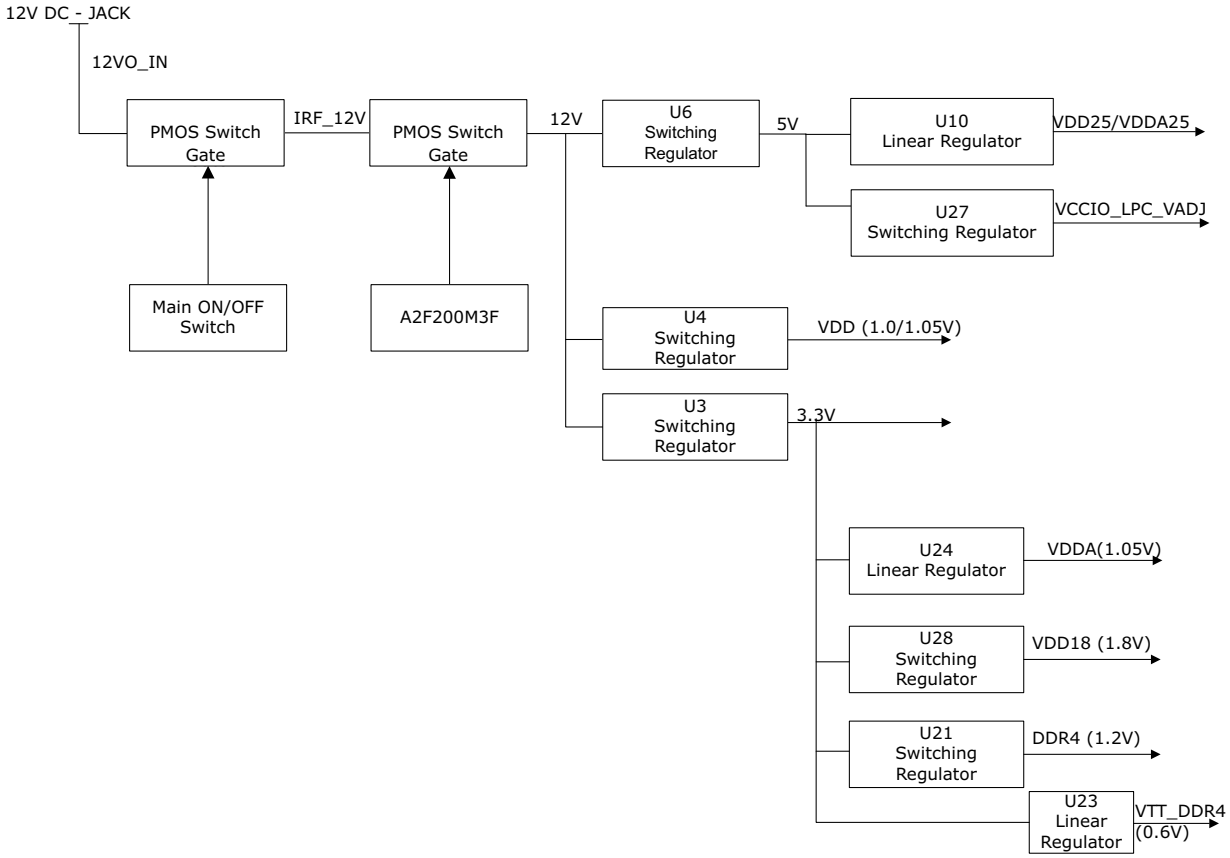
The following table lists the key power supplies required for normal operation of the PolarFire Splash Board.

Table 5 • **I/O Voltage Rails**

PolarFire Bank	I/O Rail	Voltage
Bank0, 1	1P2V_DDR4	1.2 V
Bank2	VCCIO_LPC_VADJ	3.3 V, 2.5 V, 1.8 V, 1.5 V, or 1.2 V
Bank3	VDD25	2.5 V
Bank4	3P3V	3.3 V

The following figure shows voltage rails (12 V, 5 V, 3.3 V, 2.5 V, 1.8 V, 1.2 V, and 1.0 V) available on the PolarFire Splash Board.

Figure 3 • **Voltage Rails on PolarFire Splash Board**



The following table lists the power regulators suggested to be used for PolarFire FPGA voltage rails.

Table 6 • **Power Regulators**[1]

Voltage Rail	Part Number	Description	Current
5V	MIC24055YJL-TR	IC REG BUCK ADJ 12A SYNC 28QFN	12A
VDD (1V)	MIC24055YJL-TR	IC REG BUCK ADJ 12A SYNC 28QFN	12A
DDR4 (1.2V)	MIC24046YFL-TR	IC REG BUCK PROG 5A SYNC 20VQFN	5A
FMC_LPC	MIC24046YFL-TR	IC REG BUCK PROG 5A SYNC 20VQFN	5A
VTT (0.6V)	MIC5166YML-TR	IC PWR SUP 3A HS DDR TERM 10MLF	3A
VDD18 (1.8V)	MIC24046YFL-TR	IC REG BUCK PROG 5A SYNC 20VQFN	5A
3V3_F2	MCP1726T-ADJE/MF	IC REG LINEAR POS ADJ 1A 8DFN	1A
1V5_F2	MCP1726T-ADJE/MF	IC REG LINEAR POS ADJ 1A 8DFN	1A
VDDA(1.05V)	MIC69502WR	IC REG LINEAR POS ADJ 5A SPAK-7	5A
VDD25, VDDA25	MIC69502WR	IC REG LINEAR POS ADJ 5A SPAK-7	5A

1. These regulators are not pin compatible with the existing Splash kit schematics. Use these regulators for new board designs.

4 Board Components and Operations

This section describes the key components of the PolarFire Splash Board and provides information about important board operations. For device datasheets, visit the *PolarFire Kits webpage*.

4.1 DDR4 Memory Interface

Two 4-Gb DDR4 SDRAM chips are provided to serve as flexible volatile memory for user applications. The DDR4 interface is implemented in HSIO bank0 and bank1.

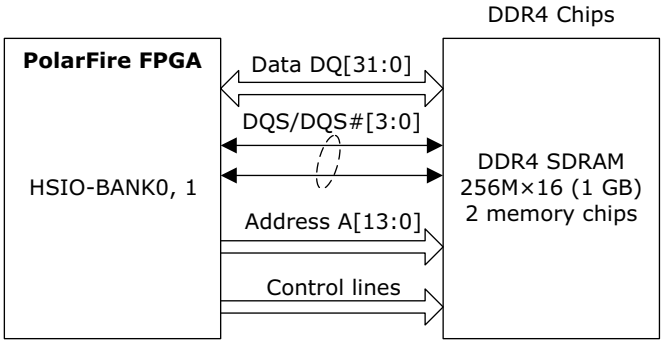
The DDR4 SDRAM specifications for the PolarFire device are:

- Two IS43QR16256A chips connected in fly-by topology
- Density: 1 GB
- Data rate: DDR4 32-bit at 200 MHz clock rate

The DDR4 memory operates at 1600 MHz with gearing 1:8 for the 200-MHz PolarFire fabric.

The PolarFire Splash Board design uses the DDR4 and POD12 standards for the DDR4 interface. The default board assembly available for the DDR4 standard has RC terminations.

Figure 4 • **DDR4 Memory Interface**



For more information, see the Board Level Schematics document (provided separately).

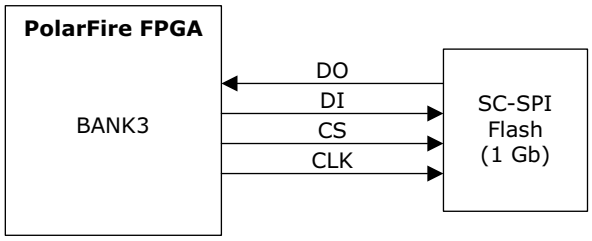
4.2 SPI Serial Flash

The SPI flash specifications for the PolarFire device are:

- Density: 1 Gb
- Voltage: 2.7 V to 3.6 V (MT25QL01GBBB8ESF-0SIT)
- Frequency: 90 MHz
- Quantity: 1
- SPI mode support: Modes 0 and 3
- Dedicated bank: Bank3

The following figure shows the SPI Flash interface of the PolarFire Splash Board.

Figure 5 • **SPI Flash Interface**



For more information, see the Board Level Schematics document (provided separately).

4.3 Transceivers

The PolarFire MPF300TS-1FCG484EES device has eight transceiver lanes, which can be accessed through the PCIe Edge connectors and FMC LPC connectors on the board. For more information about transceiver protocols, see *UG0677: PolarFire FPGA Transceiver User Guide*.

4.3.1 XCVR0 Interface

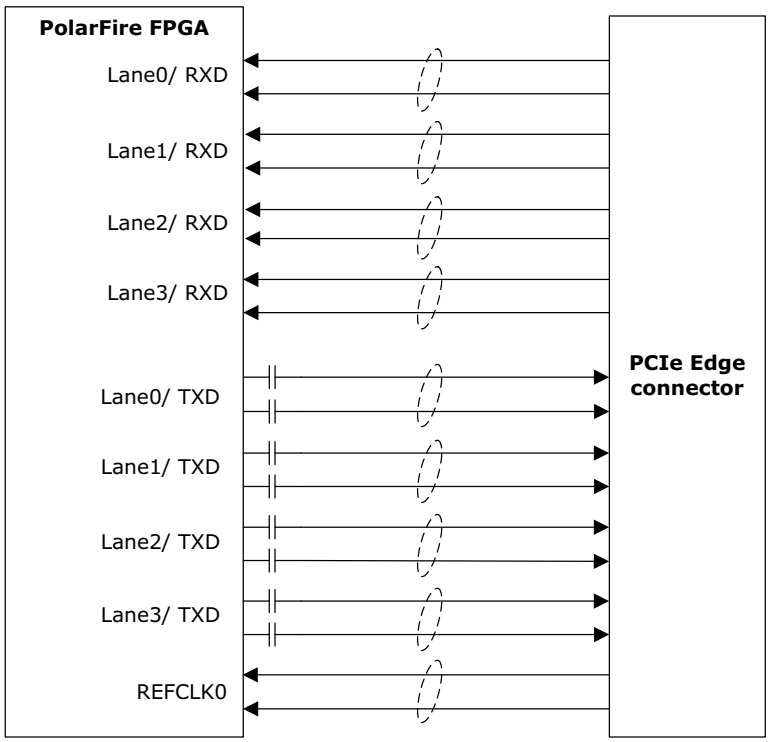
The XCVR0 interface has four lanes connected as follows:

- Lanes 0, 1, 2, and 3 are directly routed to the PCIe connector:
  - TX pad > trace > AC coupling > trace > via (to bottom layer) > trace > PCIe connector pad
  - RX pad > trace > via (to top layer) > trace > PolarFire device pad

The XCVR0 reference clock is routed directly from the PCIe connector to the PolarFire device. The XCVR0 TXD pairs are capacitively coupled to the PolarFire device. Serial AC-coupling capacitors are used to provide common-mode voltage independence. The PolarFire FPGA supports PCIe Gen2 protocol. For more information about PCIe, see *UG0685: PolarFire FPGA PCI Express User Guide*.

The following figure shows the XCVR0 interface of the PolarFire Splash Board.

Figure 6 • **XCVR0 Interface**



4.3.2 XCVR1 Interface

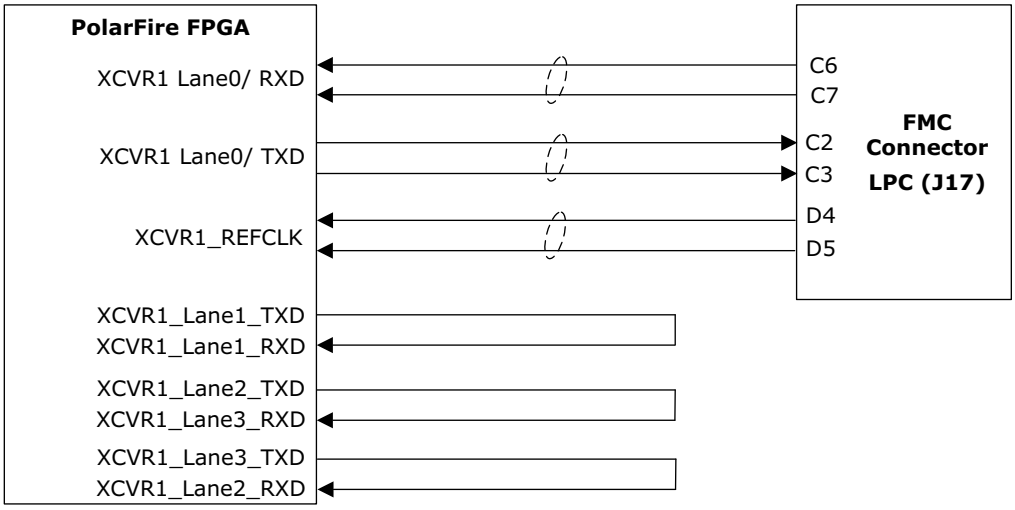
The XCVR1 interface has one lane that is connected to FMC LPC connector. The signals are routed in the PCB as follows:

- Lanes 0 is directly routed to the FMC LPC connector.
  - TX pad > trace > via (to top layer) > trace > FMC LPC connector pad
  - RX pad > trace > via (to top layer) > trace > PolarFire device pad

The XCVR1 reference clock is routed directly from the LPC connector to the PolarFire device.

The following figure shows the XCVR1 interface of the PolarFire Splash Board.

Figure 7 • **XCVR1 Interface**



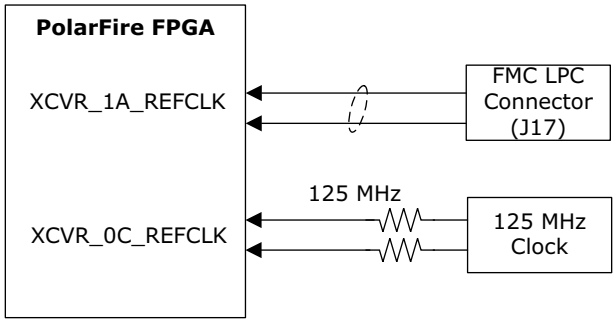
4.3.3 Transceiver Reference Clocks

The transceiver supports reference clocks connected as follows:

- XCVR 1A reference clock is connected to an FMC LPC connector.
- XCVR 0C reference clock is connected the on-board 125-MHz oscillator.

The following figure shows the XCVR reference clocks are interface of the PolarFire Splash Board.

Figure 8 • **Transceiver Reference Clocks**



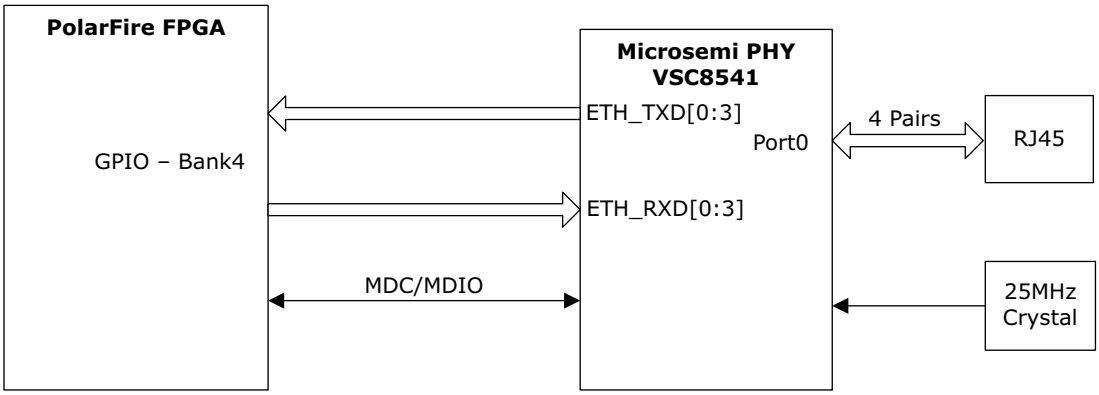
For more information, see the Board Level Schematics document (provided separately).

4.4 Microsemi PHY (VSC8541)

The VSC8541 device, offered in a small (8 mm × 8 mm), single-row, quad-flat no-leads (QFN) package is designed for space-constrained 10/100/1000BASE-T applications. It features integrated line-side termination to conserve board space, lower electromagnetic induction (EMI), and improve system performance. Additionally, the integrated RGMII version 2.0 standard timing-compliant compensation eliminates the need for on-board delay lines.

The device supports the industry's widest range of LVCMOS levels for a parallel MAC interface, including 1.5 V, 1.8 V, 2.5 V, and 3.3 V. It also supports 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V for the MDIO/MDC interface. The device includes Microsemi EcoEthernet™ 2.0 technology with energy-efficient Ethernet and other power saving features that reduce power based on link state and cable reach. These features enable the device to optimize power consumption at all link operating speeds.

Figure 9 • **PHY Interface**



4.5 Power Monitoring

The PolarFire Splash Board uses a Microsemi A2F200M3F-1FGG256I device to monitor the voltage rails. The A2F200M3F-1FGG256I device is programmed through the FTDI interface, and it supports the UART interface. The device needs an external 20-MHz crystal frequency.

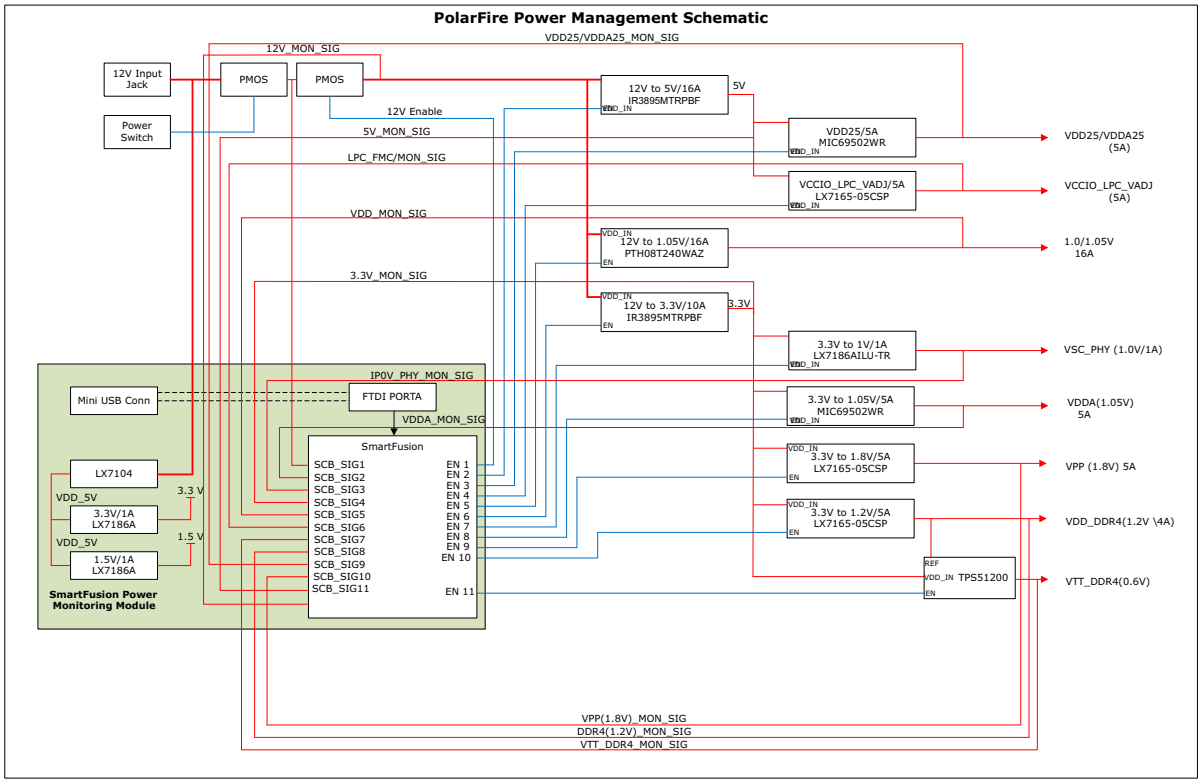
Key features of Microsemi A2F200M3F-1FGG256I are:

- Microcontroller subsystem (MSS)
- Analog compute engine (ACE)
- Programmable analog front-end (AFE)

For more information about how to monitor power on the board, see Appendix: Power Monitoring, page 27.

The following figure shows the power management system on the PolarFire Splash Board.

Figure 10 • **Power Management**



4.6 Programming

The PolarFire device is programmed using the on-board FlashPro5 programmer. For more information about how to program the device, see Appendix: Programming PolarFire FPGA Using the On-Board FlashPro5, page 26 and *UG0714: PolarFire FPGA Programming User Guide*.

4.6.1 FTDI

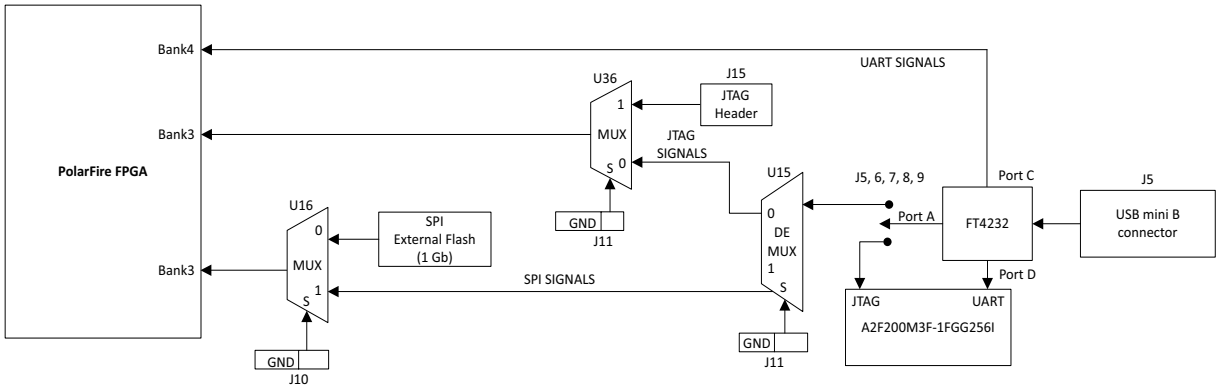
The key features of the FT4232H chip are:

- USB 2.0 high-speed (480 Mbps) to UART/MPSSE IC
- Single-chip USB-to-quad serial ports in various configurations
- Entire USB protocol handled on the chip without requiring USB-specific firmware programming
- USB 2.0 high-speed (480 Mbps) and full-speed (12 Mbps) compatibility
- Two multi-protocol synchronous serial engines (MPSSE) on channel A and channel B to simplify synchronous serial protocol (USB to JTAG, I2C, SPI, or bit-bang) design

Note: FTDI chip requires 1.8 V chip core voltage and +3.3 V I/O voltage

The following figure shows the FTDI interface of the PolarFire Splash Board.

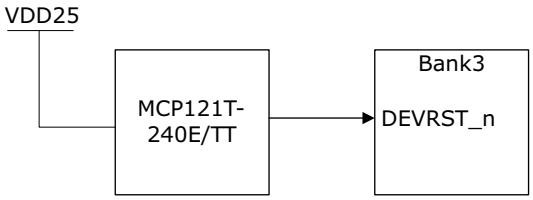
Figure 11 • **FTDI Interface**



4.7 System Reset

DEVRST_N is an input-only reset pad that allows a full reset of the chip to be asserted at any time. The following figure shows a sample reset circuit that uses a Microchip MCP121T-240E/TT device.

Figure 12 • **Reset Circuit**



4.8 50-MHz Oscillator

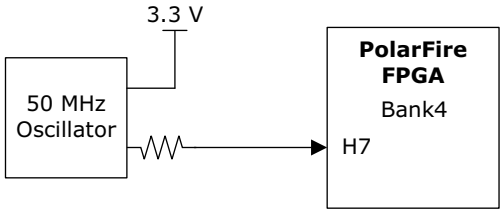
A 50-MHz clock oscillator with an accuracy of +/-50 ppm is available on the board. This clock oscillator is connected to the FPGA fabric to provide a system reference clock.

An on-chip PolarFire phase-locked loop (PLL) can be configured to generate a wide range of high-precision clock frequencies.

The pin number of the 50-MHz oscillator is H7, and the pin name is GPIO239PB5/CLKIN_W_2/CCC_SW_CLKIN_W_2/CCC_SW_PLL0_OUT0.

The following figure shows the 50-MHz clock oscillator interface.

Figure 13 • **50-MHz Clock Oscillator**



For more information, see the Board-Level Schematics document (provided separately).

4.9 User Interface

The PolarFire Splash Board has user LEDs and push-button switches.

4.9.1 User LEDs

The board has eight active-high LEDs that are connected to the PolarFire device. The following table lists the on-board user LEDs.

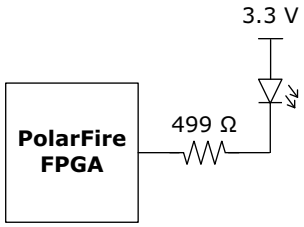
Table 7 • **User LEDs**

PolarFire Splash Board Ref Des	PolarFire FPGA Pin Number	PolarFire FPGA Pin Name	Bank
LED1	P7	GPIO186PB4	Bank4
LED2	P8	GPIO186NB4	Bank4
LED3	N7	GPIO187PB4/DQS	Bank4
LED4	N8	GPIO187NB4/DQS	Bank4
LED5	N6	GPIO188PB4	Bank4
LED6	N5	GPIO188NB4	Bank4
LED7	M8	GPIO189PB4	Bank4
LED8	M9	GPIO189NB4	Bank4
D5[1]	C16	O23NDB1V0	Bank1

1. SmartFusion power-monitoring FPGA (A2F200M3F-1FGG256I) user LED.

The following figure shows the LED interface of the PolarFire Splash Board.

Figure 14 • **LED Interface**



For more information, see the Board-Level Schematics document (provided separately).

4.9.2 Push-Button Switches

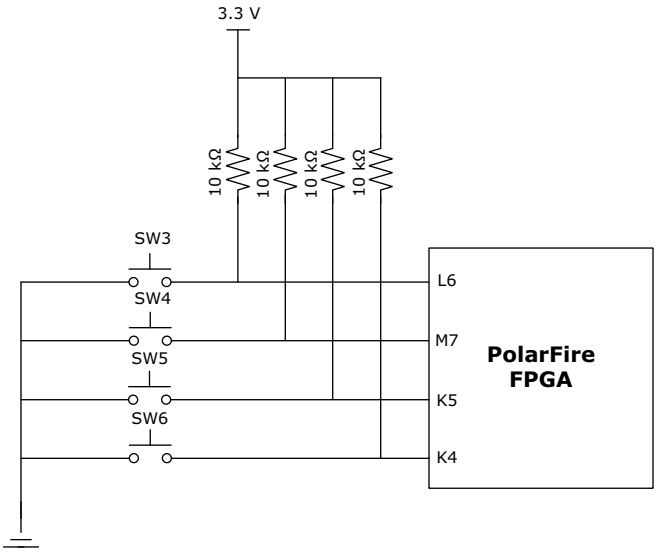
The PolarFire Splash Board comes with four push-button tactile switches that are connected to the PolarFire device. The following table lists the on-board push-button switches.

Table 8 • **Push-Button Switches**

PolarFire Splash Board Ref Des	PolarFire FPGA Pin Number	PolarFire FPGA Pin Name	Bank
SW3	L6	GPIO210PB4	Bank4
SW4	M7	GPIO210NB4	Bank4
SW5	K5	GPIO211PB4/DQS	Bank4
SW6	K4	GPIO211NB4/DQS	Bank4

The following figure shows the switches interface of the PolarFire Splash Board.

Figure 15 • **Switches Interface**



4.9.3 Slide Switches (DPDT)

The SW3 slide switch powers the device ON or OFF using a +12 V external DC jack.

4.9.4 DIP Switches (SPST)

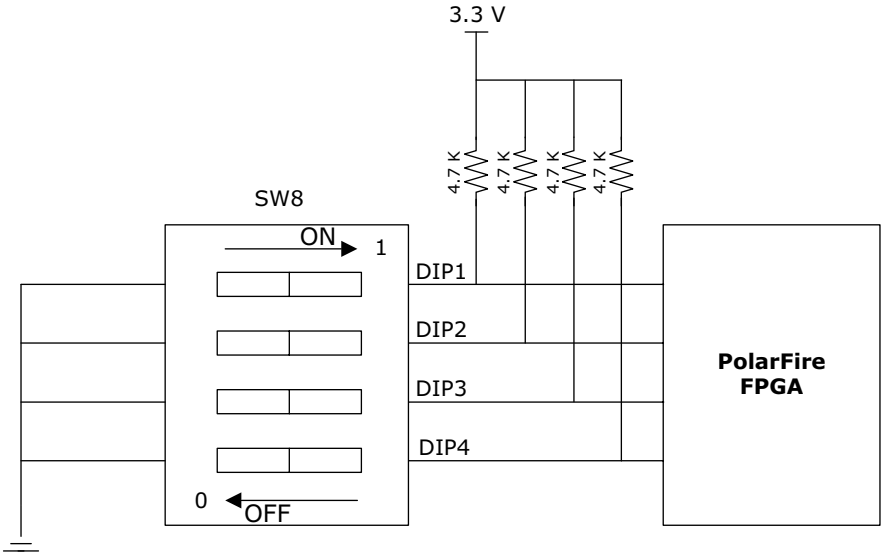
The SW8 DIP switch has four connections to the PolarFire device. The following table lists the on-board DIP switches.

Table 9 • **DIP Switches**

PolarFire Splash Board Net Name	PolarFire FPGA Pin Number	PolarFire FPGA Pin Name	Bank
DIP1	L3	GPIO212PB4	Bank4
DIP2	M4	GPIO212NB4	Bank4
DIP3	J6	GPIO238PB5/CCC_SW_PLL0_OUT1	Bank4
DIP4	K6	GPIO238NB5	Bank4

The following figure shows the SPST interface on the PolarFire Splash Board.

Figure 16 • **SPST Interface**



For more information, see the Board-Level Schematics document (provided separately).

4.9.5 FMC LPC Connector

The PolarFire Splash Board has an FMC LPC connector (J17) for the daughter cards for future expansion of interfaces. This FMC connector is compliant with VITA 57.1 specification. Any standard daughter board with an FMC LPC connector can be plugged into the PolarFire Splash Board.

The PolarFire GPIO and XCVR1 signals are routed to the FMC connector (J17) for application development.The following table provides the J17 FMC pinout details.

Table 10 • **J17 FMC Connector Pinout**

FMC Pin Number-J17	FMC Net Name	PolarFire Pin Number	PolarFire Pin Name
C2	FMC_LPC_SERDES1_TXD0_P	B22	XCVR_1_TX0_P
C3	FMC_LPC_SERDES1_TXD0_N	B21	XCVR_1_TX0_N
C6	FMC_LPC_SERDES1_RXD0_P	A20	XCVR_1_RX0_P
C7	FMC_LPC_SERDES1_RXD0_N	A19	XCVR_1_RX0_N
C10	LPC_LA06_P	B9	GPIO8PB2/DQS
C11	LPC_LA06_N	B10	GPIO8NB2/DQS
C14	LPC_LA10_P	A6	GPIO3PB2
C15	LPC_LA10_N	A7	GPIO3NB2
C18	LPC_LA14_P	A2	GPIO247PB2/CLKIN_S_2/CCC_SW_CLKIN_S_2/CCC_SW_PLL1_OUT0
C19	LPC_LA14_N	A3	GPIO247NB2
C22	LPC_LA18_CC_P	D2	GPIO245PB2/CCC_SW_CLKIN_S_1
C23	LPC_LA18_CC_N	C2	GPIO245NB2
C26	LPC_LA27_P	G14	GPIO30PB2
C27	LPC_LA27_N	H13	GPIO30NB2

Table 10 • **J17 FMC Connector Pinout *(continued)***

FMC Pin Number-J17	FMC Net Name	PolarFire Pin Number	PolarFire Pin Name
C30	LPC_SCL_B4	E1	GPIO244PB2/CCC_SW_CLKIN_S_0
C31	LPC_SDA_B4	D1	GPIO244NB2
D4	FMC_LPC_SERDES1_REFCLK0_P	G19	XCVR_1A_REFCLK_P
D5	FMC_LPC_SERDES1_REFCLK0_N	G20	XCVR_1A_REFCLK_N
D8	LPC_LA01_CC_P	G17	GPIO34PB2/CCC_SE_PLL1_OUT1
D9	LPC_LA01_CC_N	F17	GPIO34NB2
D11	LPC_LA05_P	D16	GPIO32PB2/DQS/CCC_SE_PLL1_OUT0
D12	LPC_LA05_N	D17	GPIO32NB2/DQS
D14	LPC_LA09_P	B8	GPIO5PB2
D15	LPC_LA09_N	A8	GPIO5NB2
D17	LPC_LA13_P	F13	GPIO21PB2
D18	LPC_LA13_N	F12	GPIO21NB2
D20	LPC_LA17_CC_P	E15	GPIO33PB2/CCC_SE_CLKIN_S_10/CCC_SE_PLL1_OUT0
D21	LPC_LA17_CC_N	E16	GPIO33NB2
D23	LPC_LA23_P	C1	GPIO246PB2/DQS/CCC_SW_PLL1_OUT0
D24	LPC_LA23_N	B1	GPIO246NB2/DQS
D26	LPC_LA26_P	F5	GPIO250PB2
D27	LPC_LA26_N	E5	GPIO250NB2
G2	LPC_CLK1_M2C_P	A15	GPIO29PB2/CLKIN_S_9/CCC_SE_CLKIN_S_9
G3	LPC_CLK1_M2C_N	A16	GPIO29NB2
G6	LPC_LA00_CC_P	A17	GPIO26PB2/DQS/CCC_SE_PLL0_OUT0
G7	LPC_LA00_CC_N	B17	GPIO26NB2/DQS
G9	LPC_LA03_P	A12	GPIO11PB2/CLKIN_S_7
G10	LPC_LA03_N	A13	GPIO11NB2
G12	LPC_LA08_P	C11	GPIO9PB2/CLKIN_S_6
G13	LPC_LA08_N	C12	GPIO9NB2
G15	LPC_LA12_P	C5	GPIO255PB2
G16	LPC_LA12_N	B5	GPIO255NB2
G18	LPC_LA16_P	C14	GPIO25PB2
G19	LPC_LA16_N	C15	GPIO25NB2
G21	LPC_LA20_P	D11	GPIO20PB2/DQS
G22	LPC_LA20_N	D12	GPIO20NB2/DQS
G24	LPC_LA22_P	C9	GPIO7PB2/CLKIN_S_5
G25	LPC_LA22_N	C10	GPIO7NB2
G27	LPC_LA25_P	E9	GPIO4PB2
G28	LPC_LA25_N	D9	LPC_LA25_N

Table 10 • **J17 FMC Connector Pinout *(continued)***

FMC Pin Number-J17	FMC Net Name	PolarFire Pin Number	PolarFire Pin Name
G30	LPC_LA29_P	E8	GPIO2PB2/DQS
G31	LPC_LA29_N	D8	GPIO2NB2/DQS
G33	LPC_LA31_P	C6	GPIO1PB2
G34	LPC_LA31_N	B7	GPIO1NB2
G36	LPC_LA33_P	B4	GPIO253PB2
G37	LPC_LA33_N	A5	GPIO253NB2
H2	LPC_PRSNT_M2C_L	E11	GPIO22PB2
H4	LPC_CLK0_M2C_P	C16	GPIO28PB2/CCC_SE_PLL0_OUT1
H5	LPC_CLK0_M2C_N	C17	GPIO28NB2
H7	LPC_LA02_P	B12	GPIO6PB2/CLKIN_S_4
H8	LPC_LA02_N	B13	GPIO6NB2
H10	LPC_LA04_P	F15	GPIO35PB2/CCC_SE_CLKIN_S_11
H11	LPC_LA04_N	F16	GPIO35NB2
H13	LPC_LA07_P	H15	GPIO31PB2
H14	LPC_LA07_N	G15	GPIO31NB2
H16	LPC_LA11_P	B2	GPIO249PB2/CLKIN_S_3/CCC_SW_CLKIN_S_3
H17	LPC_LA11_N	B3	GPIO249NB2
H19	LPC_LA15_P	D14	GPIO24PB2
H20	LPC_LA15_N	E14	GPIO24NB2
H22	LPC_LA19_P	G12	GPIO18PB2
H23	LPC_LA19_N	G13	GPIO18NB2
H25	LPC_LA21_P	F10	GPIO19PB2
H26	LPC_LA21_N	E10	GPIO19NB2
H28	LPC_LA24_P	F3	GPIO252PB2/DQS
H29	LPC_LA24_N	E4	GPIO252NB2/DQS
H31	LPC_LA28_P	E3	GPIO248PB2/CCC_SW_PLL1_OUT1
H32	LPC_LA28_N	D3	GPIO248NB2
H34	LPC_LA30_P	E6	GPIO254PB2
H35	LPC_LA30_N	D6	GPIO254NB2
H37	LPC_LA32_P	D4	GPIO251PB2
H38	LPC_LA32_N	C4	GPIO251NB2

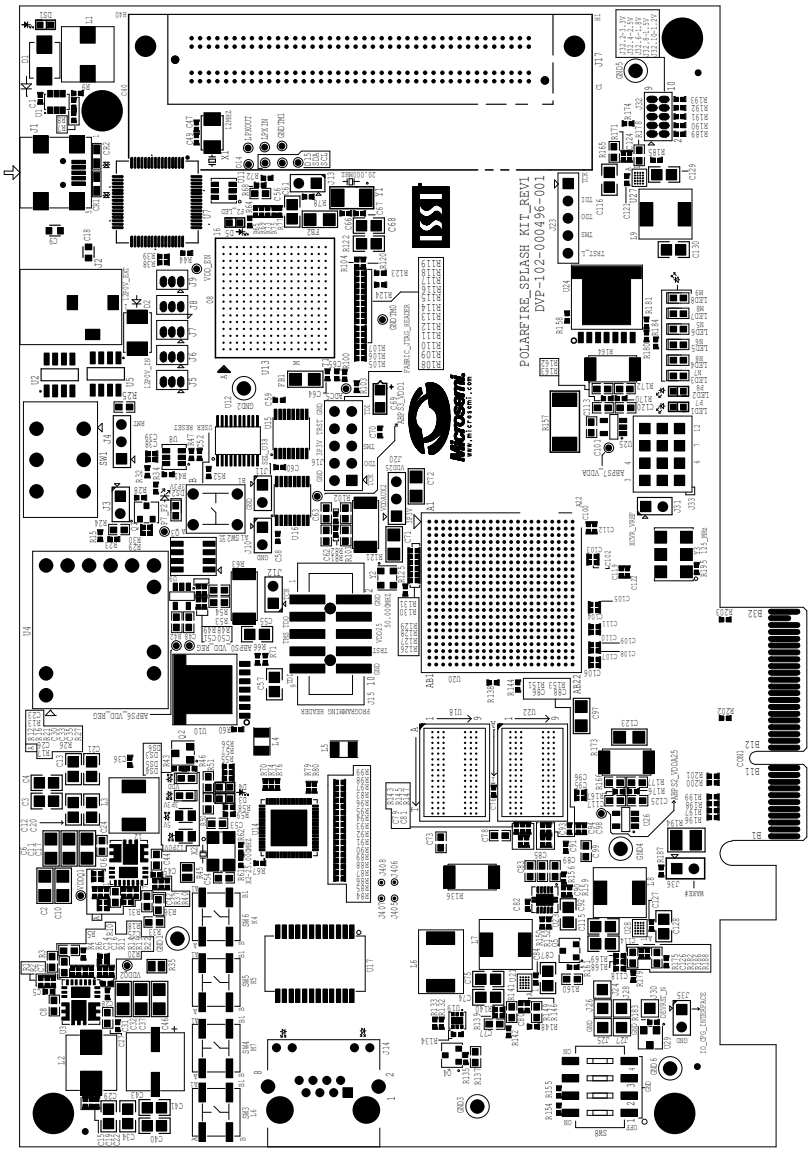
5 Pin List

For information about all package pins on the PolarFire device, see *Package Pin Assignment Table*.

6 Board Component Placement

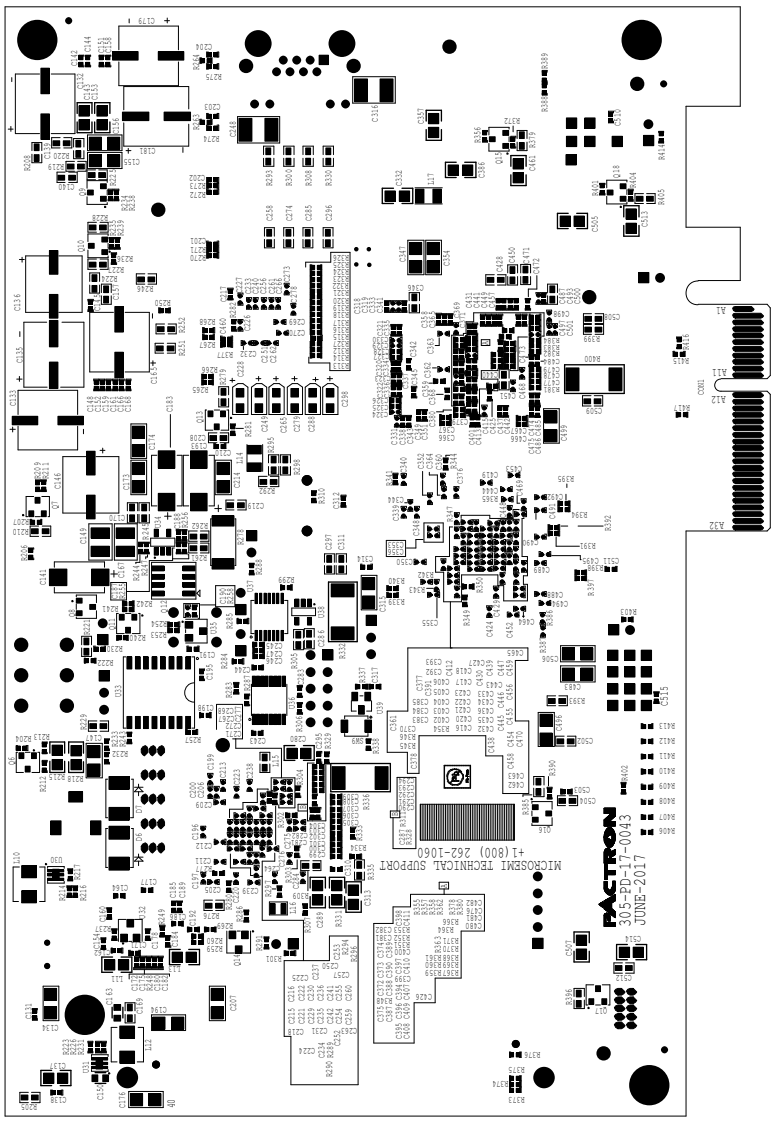
The following figure shows the placement of various components on the PolarFire Splash Board silkscreen.

Figure 17 • **Silkscreen Top View**



The following figure shows the bottom view of the PolarFire Splash Board silkscreen.

Figure 18 • **Silkscreen Bottom View**



7 Demo Design

For information about how to run the JESD204B standalone demo design, see *DG0796: PolarFire FPGA Splash Kit JESD204B Standalone Interface Demo Guide*.

8 Appendix: Programming PolarFire FPGA Using the On-Board FlashPro5

The PolarFire Splash Board includes an on-board FlashPro5 programmer. An external programmer hardware is, therefore, not required to program the PolarFire device. The device can be programmed using the FlashPro software installed on the host PC.

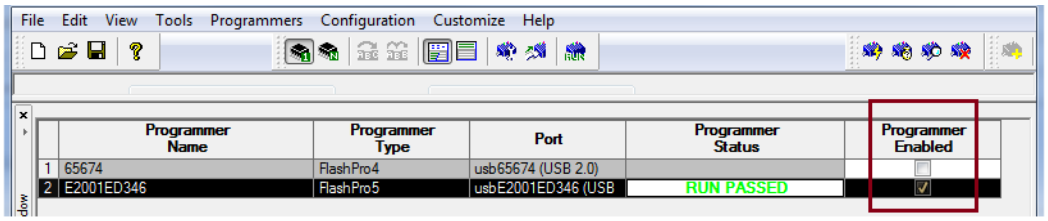
Follow these steps to program an on-board PolarFire device using the on-board FlashPro5 programmer:

1. Connect the power supply cable to the **J2** connector on the board.
2. Connect the USB cable from the host PC to the **J1** connector (FTDI port) on the board.
3. Power on the board using the **SW1** slide switch.
   When the board is successfully set up, the LEDs start glowing.
4. On the host PC, start the FlashPro software.
5. Click **New Project** to create a new project.
6. In the **New Project** window, do the following, and click OK:
   - Enter a project name.
   - Select **Single device** as the programming mode.
7. Click **Configure Device**.
8. Click **Browse**, and select the .stp file from the **Load Programming File** window.

Note: The programming file will be available in a future release.

9. From the **View Programmer** pane, select the on-board FlashPro5 programmer, as shown in the following figure.

Figure 19 • **Selecting the On-Board FlashPro5**



10. Click **Program** to program the device.
    The **Programmer List** window in the FlashPro software shows the programmer name, programmer type, port, programmer status, and information about whether the programmer is enabled.
11. When the device is programmed successfully, a **Run Program PASSED** status is displayed.

9 Appendix: Power Monitoring

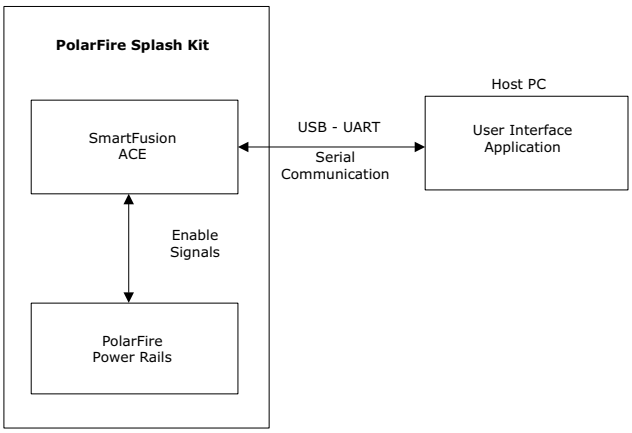
The SmartFusion A2F200 device on the PolarFire Splash Board has an in-built power monitoring program that monitors the voltage and current on different PolarFire power rails, as well as the total device power, eliminating the need for any manual measurements. The power measurements for various components are displayed in the Microsemi PowerMonitor GUI installed on the host PC.

The power monitoring program does the following:

- Monitors voltage on all PolarFire power rails.
- Measures current and power on the following rails:
  - VDD_REG: Power supply for fabric core.
  - VDDA_REG: Power supply for transceiver and common circuits.
  - VDDA25: Power supply for transceiver PLLs. This supply is isolated from other power supplies to keep the noise low and avoid leakage for PCIe, EXT_PLL, and GPSS.
  - VDD25_DUT: Power supply for the eight corner PLLs on the PolarFire device and the sNVM. These are tied together at the package level to keep the noise on the standalone PLLs low.
- Powers up and powers down the board when pins 2 and 3 of the **J4** jumper are closed.
- Powers down the board if voltage threshold violations are observed on a power rail.

The analog computing engine block in the SmartFusion device is configured to measure the voltage and current on the PolarFire power rails. The following illustration shows the PolarFire power monitoring process block diagram.

Figure 20 • **Power Monitoring Block Diagram**



9.1 Prerequisites for Installing PowerMonitor

Before installing PowerMonitor on the host PC:

1. Download the PowerMonitor application from the following location: http://soc.microsemi.com/download/rsc/?f=Polarfire_Splash_Kit_Power_Monitor
2. Ensure that pin 1 and 2 of the **J4** jumper are closed.
3. Connect the mini-USB cable from **J1** to the host PC.
4. Connect the power supply to **J2**, and turn ON the **SW1** switch.
5. Ensure that the screen resolution of the host PC is at least 1280 × 720. The screen resolution can be set from Control Panel > Appearance and Personalization > Display > Adjust screen resolution.
6. Ensure that the text size in the display settings of the host PC is set to either small (100%) or medium (150%). The text size can be set from Control Panel > Appearance and Personalization > Display > Make text and other items larger or smaller.

9.2 Installing PowerMonitor

To install PowerMonitor:

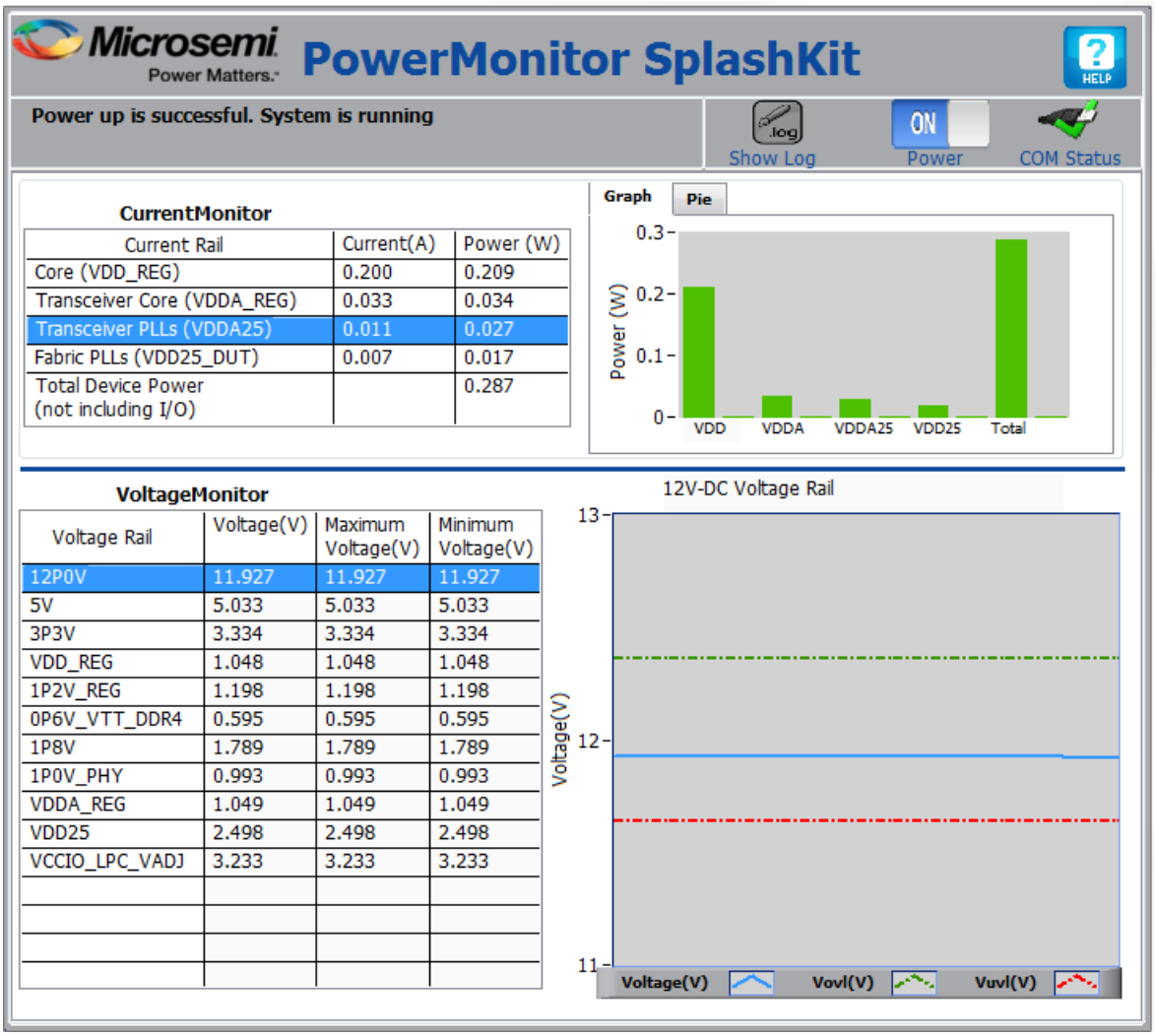
1. Extract the contents of the `Polarfire_Splash_Kit_Power_Monitor.zip` file.
2. In the `Polarfire_Splash_Kit_Power_Monitor\Installer` folder, double-click the `setup.exe` file.
3. Follow the instructions displayed in the installation wizard.
   After successful installation, PowerMonitor appears in the Start menu of the host PC.
4. Click Start, and then click **PowerMonitor**.
   The **COMPort SetUp** window opens.
5. Select the highest-numbered COM port, and click **Connect**.

The PowerMonitor GUI appears on the host PC.

9.3 About Microsemi PowerMonitor GUI

The following figure shows the PowerMonitor GUI.

Figure 21 • **PowerMonitor GUI**



The PowerMonitor GUI has the following panes:

- **CurrentMonitor**—This pane displays the current and power measured on the VDD_REG, VDDA_REG, VDDA25, and VDD25_DUT rails. It also displays total device power. The I/Os are excluded.
- **VoltageMonitor**—This pane displays the present voltage on each voltage rail. It also displays the maximum and minimum voltage measured on each voltage rail over the time period of the PowerMonitor application.The **Voltage Rail** plot in the pane displays the voltage plot of the selected rail as a blue line. The green and red lines in the plot represent the over-voltage (+3%) and under-voltage (-3%) tolerance levels of that rail. After staring the PowerMonitor GUI, the voltage plot takes minimum five seconds to plot the samples.

Note: For more information about the recommended minimum and maximum operating voltage of each rail, see the *Recommended Operating Conditions* section of *DS0141: PolarFire FPGA Datasheet*.

The PowerMonitor GUI has the following buttons:

- **Graph**—Click this button to view the power consumed by the VDD_REG, VDDA_REG, VDDA25, and VDD25_DUT rails, and also the total device power.
- **Pie**—Click this button to view the percentage of power consumed by the VDD_REG, VDDA_REG, VDDA25, and VDD25_DUT rails out of the total device power.
- **Show Log**—Click this button to view a file with all actions of the power monitoring program.
- **Power**—Click this button to power up or power down the board when pins 2 and 3 of **J4** jumper are closed.

Note: When pins 1 and 2 of **J4** jumper are closed, use the **SW1** switch to power up or power down the board.

10 Appendix: Errata

This section contains information about known issues specific to the PolarFire Splash Board.

10.1 Hot swapping not supported on programming headers and PCIe connector

Hot swapping is not supported on the programming headers (J15 and 16) and on the PCIe Connector (CON1).

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