SINGLE POWER SUPPLY SYNCHRONOUS PWM CONTROLLER

ADVANCED DATA SHEET

Pb Free Product

DESCRIPTION

The NX2155H controller IC is a single input supply synchronous Buck controller IC designed for step down DC to DC converter applications. NX2155H is optimized to convert bus voltages from 8V to 22V to output as low as 0.8V voltage. An internal regulator converts bus voltage to 5V, which provides voltage supply to internal logic and driver circuit. The NX2155H can operates at programmable frequency of 2MHz and employs loss-less current limiting by sensing the Rdson of synchronous MOSFET followed by hiccup feature.Feedback under voltage triggers Hiccup.

Other features of the device are: Internal schottky diode, thermal shutdown, 5V gate drive, adaptive deadband control, internal digital soft start, 5VREG undervoltage lock out and Shutdown capability via the comp pin.

FEATURES

- Single supply voltage from 8V to 22V
- Internal 5V regulator
- Programmable operational frequency of 2MHz
- Internal Digital Soft Start Function
- Less than 50 nS adaptive deadband
- Current limit triggers hiccup by sensing Rdson of Synchronous MOSFET
- Pb-free and RoHS compliant

APPLICATIONS

- LCD TV
- Graphic Card on board converters
- Memory Vddq Supply in mother board applications
- On board DC to DC such as 12V to 3.3V, 2.5V or 1.8V
- Hard Disk Drive
- Set Top Box

TYPICAL APPLICATION

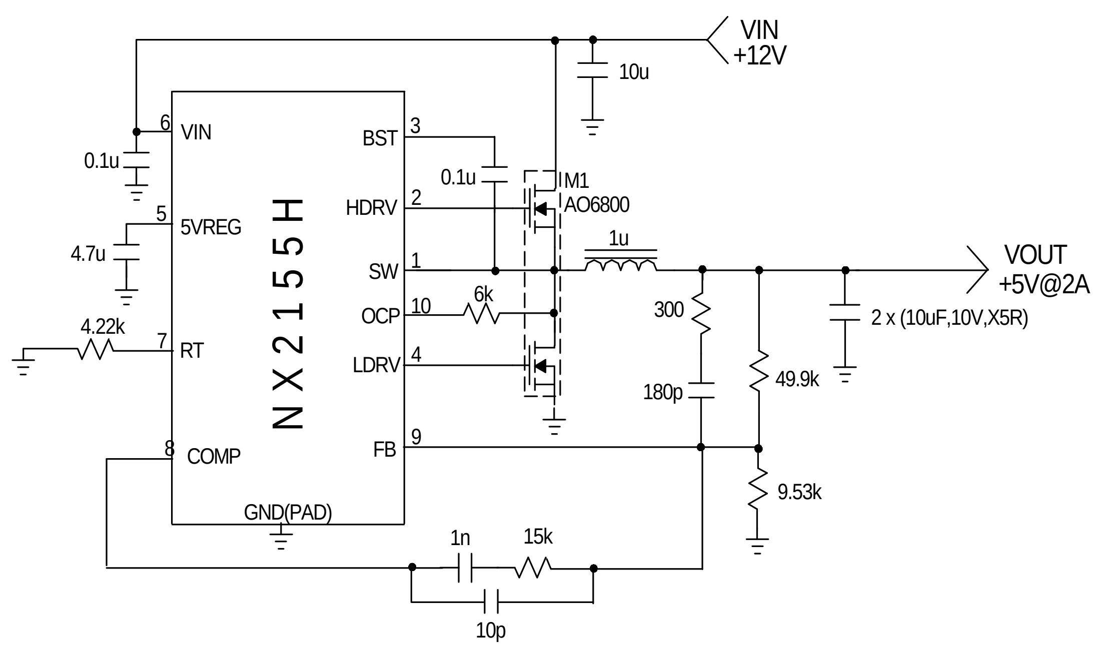


Figure1 - Typical application of 2155H

ORDERING INFORMATION

Device	Temperature	Package	Package Marking	Pb-Free
NX2155HCUPTR	0 to 70°C	MSOP-EP-10L	NX155HXXX	Yes

Note: XXX is date code. For example, 841 means that this NX2155H is packaged in the 41th week of 2008

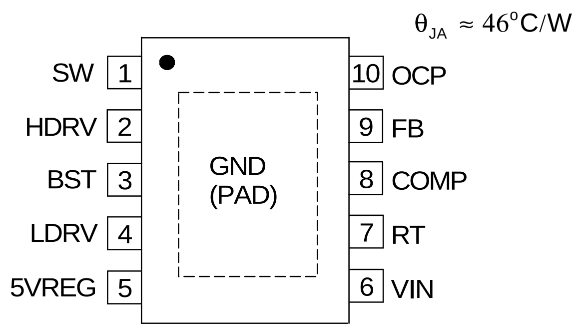
ABSOLUTE MAXIMUM RATINGS(NOTE1)

VCC to GND & BST to SW voltage 6.5V
BST to GND Voltage 30V
VIN to GND Voltage 25V
SW to GND .... -2V to 35V
All other pins .... -0.3V to 6.5V
Storage Temperature Range .... -65°C to 150°C
Operating Junction Temperature Range .... -40°C to 125°C

NOTE1: Stresses above those listed in "ABSOLUTE MAXIMUM RATINGS", may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

PACKAGE INFORMATION

10-LEAD PLASTIC MSOP-EP



ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vin = 12V, and T_A = 0 to 70°C. Followings are bypass capacitors:C_{VIN}=1uF, C_{5VREG}=4.7uF, all X5R ceramic capacitors. Typical values refer to T_A = 25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
Reference Voltage						
Ref Voltage	V_{REF}		0.784	0.8	0.816	V
Ref Voltage line regulation		V_{in}=8V to 22V		0.4		%
5VREG						
5VREG Voltage range			4.75	5	5.25	V
5VREG UVLO		5V REG rising		3.9	4.4	V
5VREG UVLO Hysteresis				0.2		V
5VREG Line Regulation		V_{IN}=9V to 22V		10	20	mV
5VREG Max Current			20	50		mA
Supply Voltage(Vin)						
V_{in} Voltage Range	V_{in}		8		22	V
Input Voltage Current(Static)		No switching	3.7	4.8	6.5	mA
Input Voltage Current (Dynamic)		Switching with HDRV and LDRV open @2.2MHz	5.4	8	11	mA

PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
Vin UVLO						
V_{in}-Threshold	V_{in}_UVLO	V_{in} Rising	6	6.5	7.5	V
V_{in}-Hysteresis	V_{in}_Hyst	V_{in} Falling		0.6		V
SS						
Soft Start time	Tss	F_S=2.2MHz		400		uS
Oscillator (Rt)						
Frequency	F_S	Rt=4.22k		2250		kHz
Ramp-Amplitude Voltage	V_{RAMP}		1.4	1.5	1.9	V
Max Duty Cycle		F_S=2.2MHz	62	71	80	%
Min Controlable On Time					150	nS
Error Amplifiers						
Transconductance			1500	2000	2500	umho
Input Bias Current	Ib			10		nA
Comp SD Threshold			0.24	0.3	0.36	V
FBUVLO						
Feedback UVLO threshold			0.54	0.6	0.66	V
High Side Driver(C_L=2200pF)						
Output Impedance , Sourcing	R_{source}(Hdrv)	I=200mA		1.9		ohm
Output Impedance , Sinking	R_{sink}(Hdrv)	I=200mA		1.7		ohm
Rise Time	THdrv(Rise)			14		ns
Fall Time	THdrv(Fall)			17		ns
Deadband Time	Tdead(L to H)	Ldrv going Low to Hdrv going High, 10%-10%	21	30	39	ns
Low Side Driver (C_L=2200pF)						
Output Impedance, Sourcing Current	R_{source}(Ldrv)	I=200mA		1.9		ohm
Output Impedance, Sinking	R_{sink}(Ldrv)	I=200mA		1		ohm
Rise Time	TLdrv(Rise)			13		ns
Fall Time	TLdrv(Fall)			12		ns
Deadband Time	Tdead(H to L)	SW going Low to Ldrv going High, 10% to 10%	7	10	13	ns
OCP						
OCP current			30	37	45	uA
Over temperature						
Threshold				150		^oC
Hysteresis				20		^oC
Internal Schottky Diode						
Forward voltage drop		forward current=20mA		350	500	mV

PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
5	5VREG	An internal 5V regulator provides supply voltage for the low side fet driver, BST and internal logic circuit. A high frequency 4.7uF X5R ceramic capacitor must be connected from this pin to the GND pin as close as possible.
6	VIN	Voltage supply for the internal 5V regulator. A high freuqncy 0.1uF ceramic capacitor must be connected from this pin to GND.
9	FB	This pin is the error amplifier inverting input. This pin is also connected to the output UVLO comparator. When this pin falls below threshold, both HDRV and LDRV outputs are in hiccup.
8	COMP	This pin is the output of the error amplifier and together with FB pin is used to compensate the voltage control feedback loop. This pin is also used as a shut down pin. When this pin is pulled below 0.3V, both drivers are turned off and internal soft start is reset.
3	BST	This pin supplies voltage to the high side driver. A high frequency ceramic capacitor of 0.1 to 1 uF must be connected from this pin to SW pin.
10	OCP	This pin is connected to the drain of the external low side MOSFET and is the input of the over current protection(OCP) comparator. An internal current source is flown to the external resistor which sets the OCP voltage across the Rdson of the low side MOSFET. Current limit point is this voltage divided by the Rds-on.
1	SW	This pin is connected to the source of the high side MOSFET and provides return path for the high side driver.
2	HDRV	High side MOSFET gate driver.
PAD	GND	Ground pin.
4	LDRV	Low side MOSFET gate driver.
7	RT	Oscillator's frequency can be set by using an external resistor from this pin to GND.

BLOCK DIAGRAM

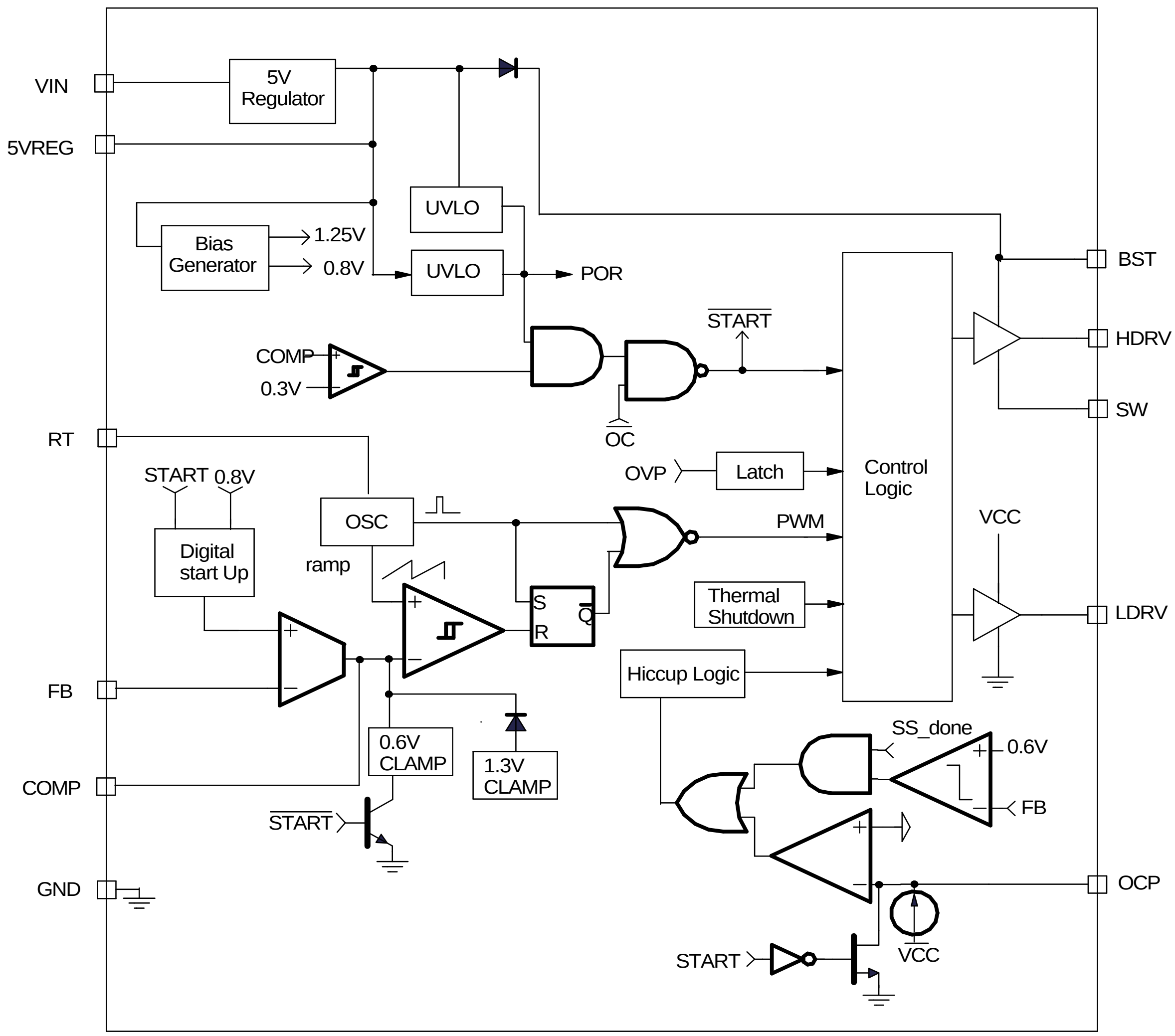
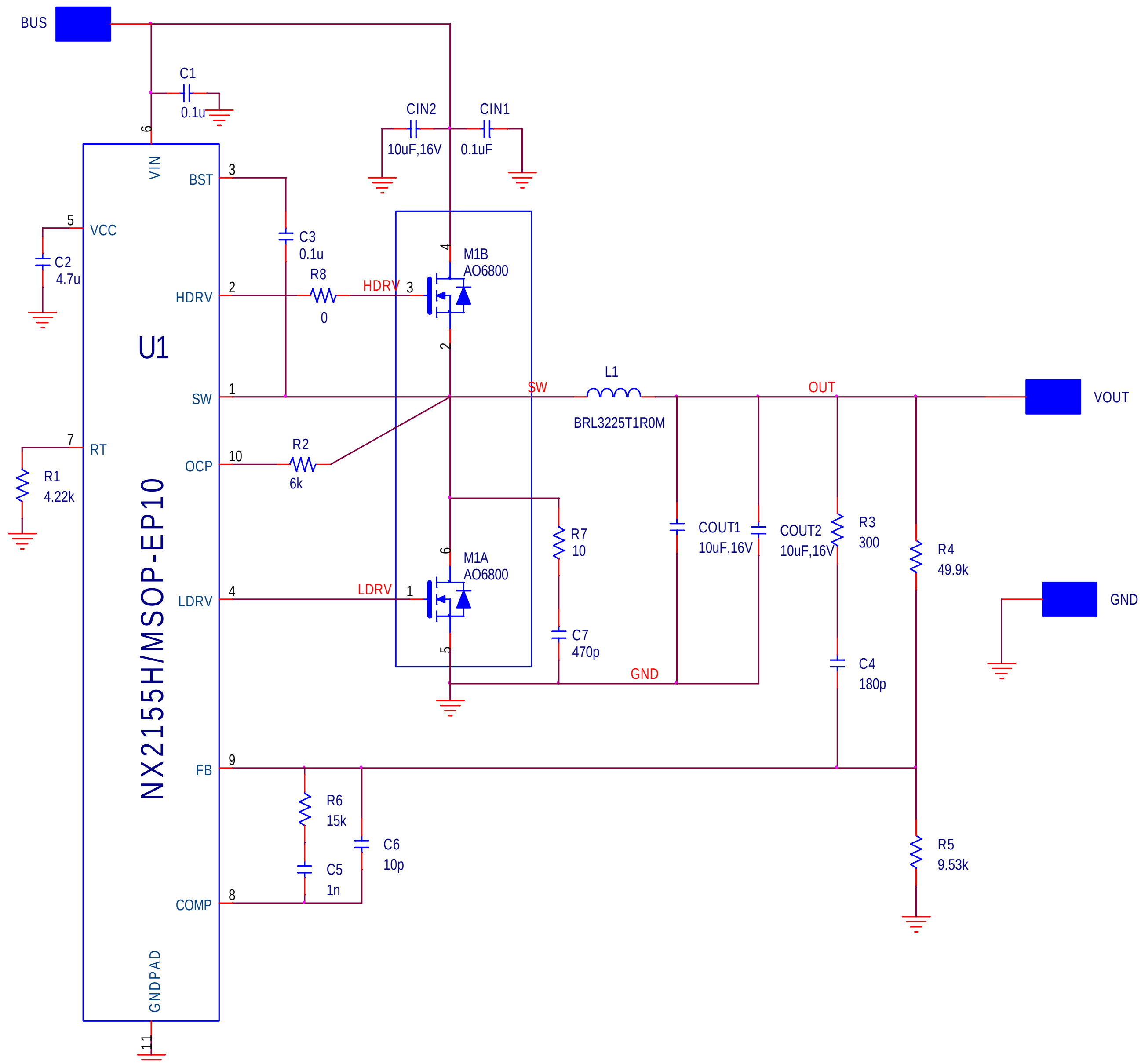


Figure 2 - Simplified block diagram of the NX2155H

Demoboard Design(VIN=12V, VOUT= 5V/2A, FREUQNCY=2.2MHz)



* R7 and C7 are optional.

Figure 3 - Simplified demoboard schematic of NX2155H

Bill of Materials

Item	Quantity	Reference	Part	Manufacturer
1	3	C1,C3,CIN1	0.1u	
2	1	C2	4.7uF,6.3V,X5R	
3	1	C4	180p	
4	1	C5	1n	
5	1	C6	10p	
6	1	C7	470p	
7	1	CIN2	10uF,16V,X5R	
8	2	COUT1,COUT2	10uF,10V,X5R	
9	1	L1	BRL3225T1R0M	TAIYO YUDEN
10	1	M1	AO6800	AOS
11	1	R1	4.22k	
12	1	R2	6k	
13	1	R3	300	
14	1	R4	49.9k	
15	1	R5	9.53k	
16	1	R6	15k	
17	1	R7	10	
18	1	R8	0	
19	1	U1	NX2155H/MSOP-EP10	NEXSEM INC.

Demoboard Waveforms

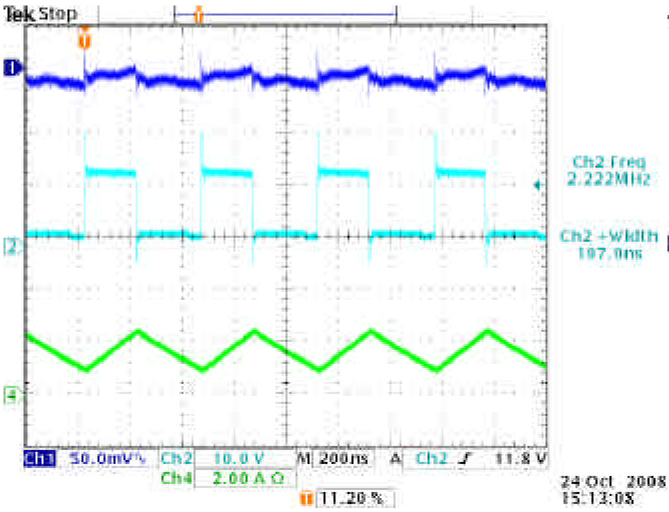


Fig.4 Output ripple(CH1 VOUT AC 50mV/DIV, CH2 SW 10V/DIV, CH4 OUTPUT CURRENT 2A/DIV)

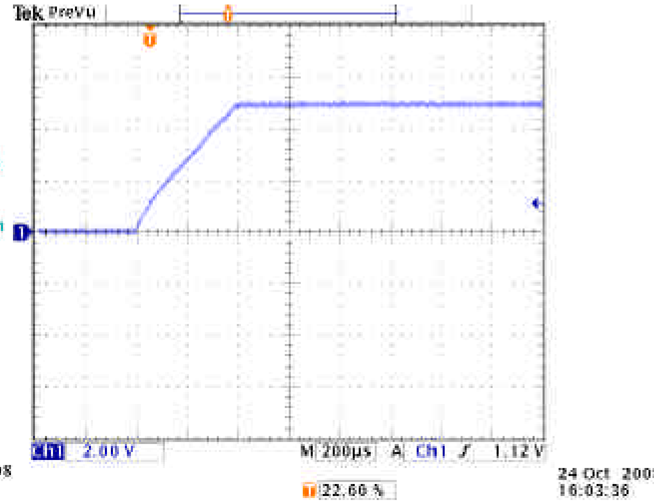


Fig.5 Startup(CH1 VOUT 2V/DIV)

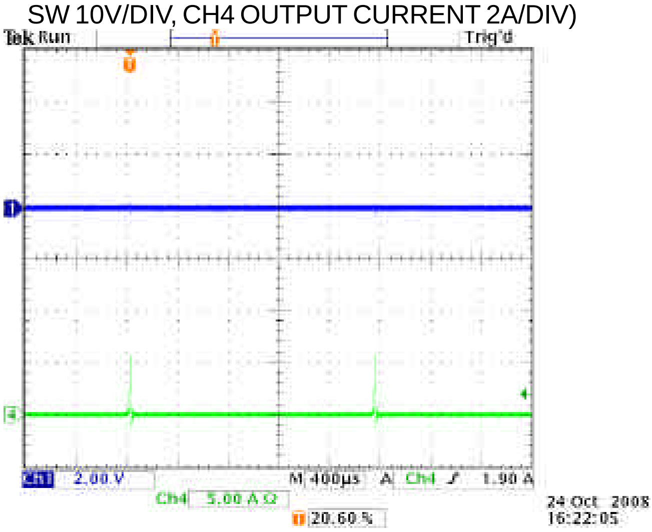


Fig.6 OCP protection during output short(CH1 VOUT 2V/DIV, CH4 OUTPUT CURRENT 5A/DIV)

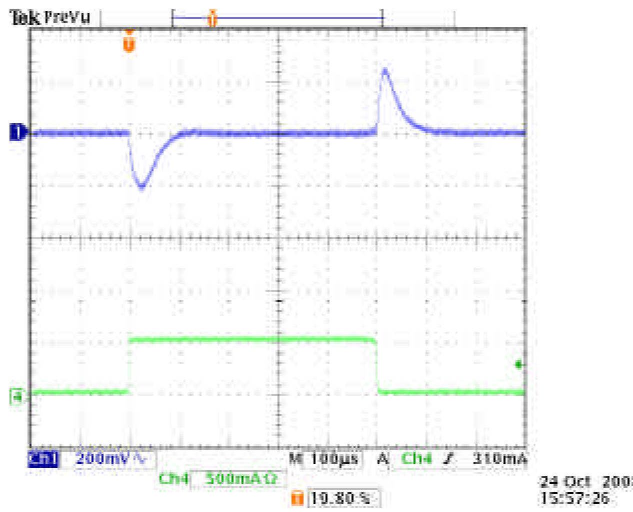


Fig.7 Output dynamic response(CH1 VOUT AC 200mV/DIV, CH4 OUTPUT CURRENT 500mA/DIV)

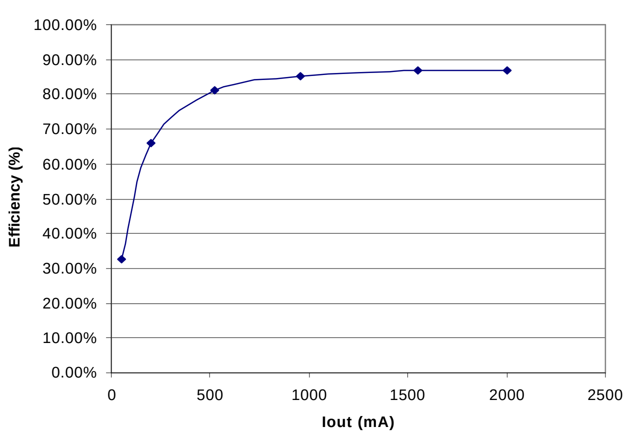


Fig.8 Output efficiency

Demoboard Layout

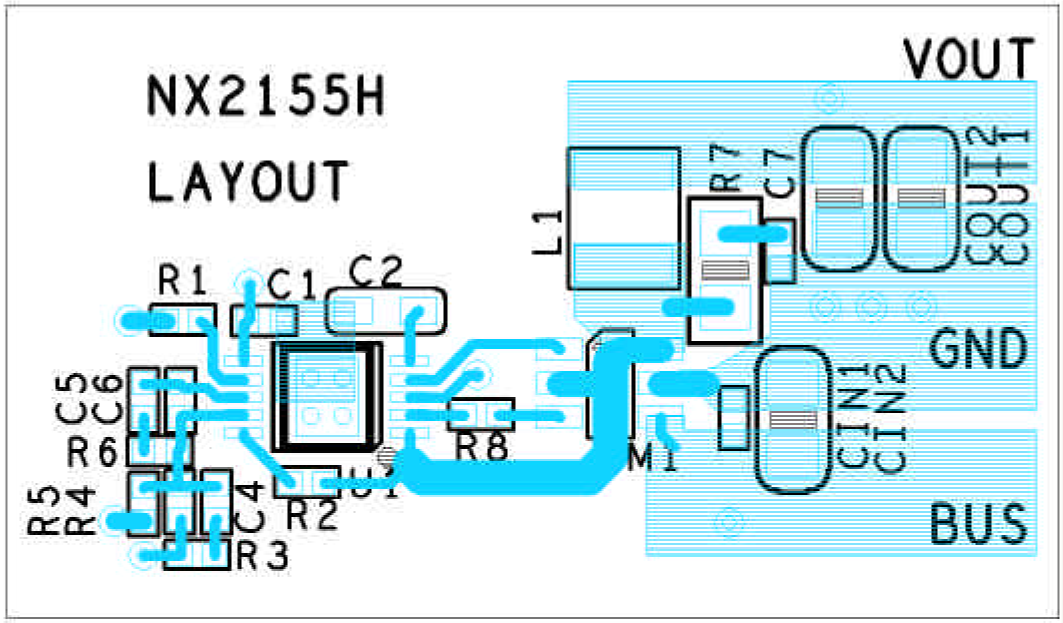


Figure 9 Top layer

Figure 10 Ground layer

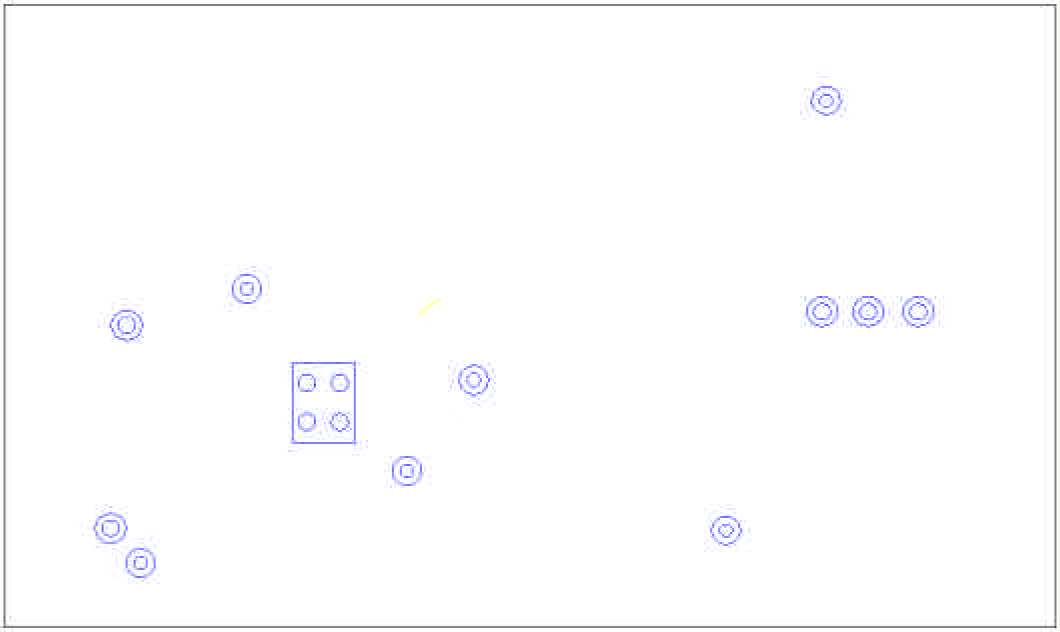


Figure 11 Power layer

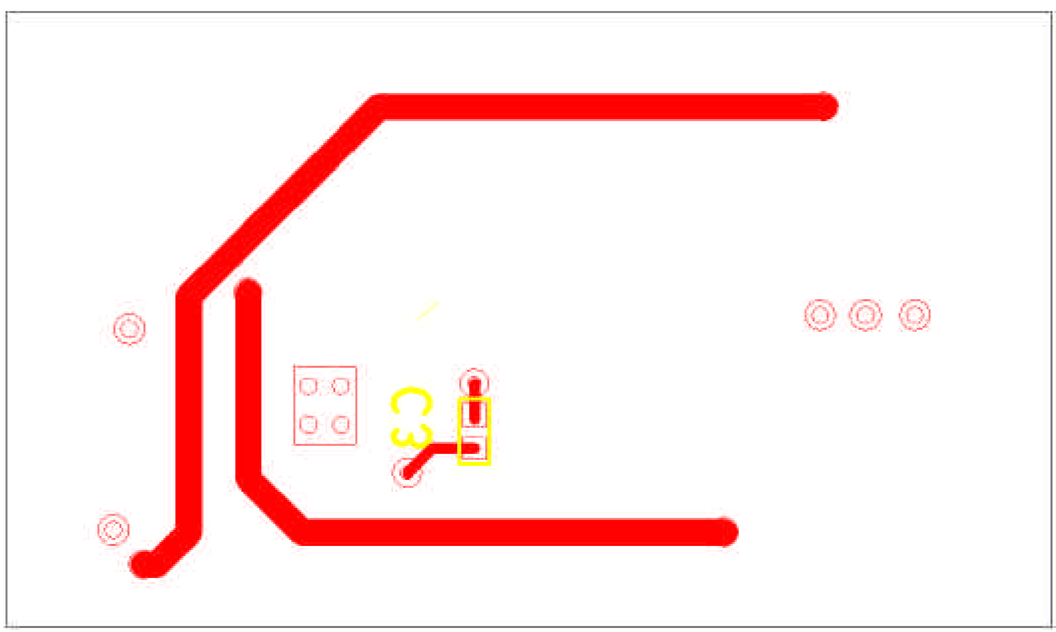


Figure 12 Bottom layer

Demoboard Design((VIN=12V, VOUT= 5V/10A, FREUQNCY=400kHz)

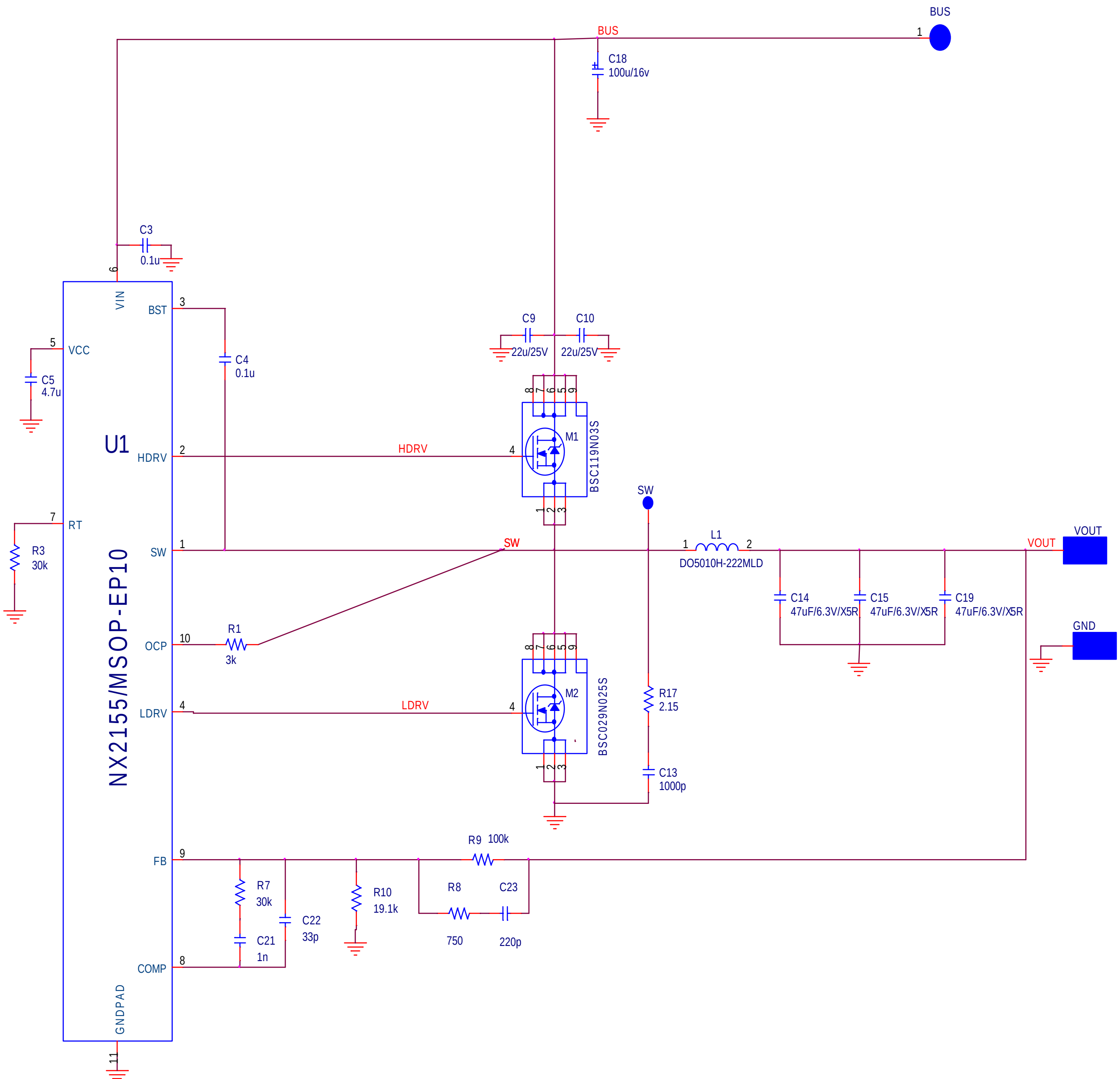


Figure 13 - Simplified demoboard schematic of NX2155H

Bill of Materials

Item	Quantity	Reference	Part	Manufacturer
1	2	C3,C4	0.1u	
2	1	C5	4.7u	
3	2	C9,C10	22u/25V/X5R	
4	1	C13	1000p	
5	3	C14,C15,C19	47uF/6.3V/X5R	
6	1	C18	100u/16v	
7	1	C21	1n	
8	1	C22	33p	
9	1	C23	220p	
10	1	L1	DO5010H-222MLD	COILCRAFT
11	1	M1	BSC119N03S	INFINEON
12	1	M2	BSC029N025S	INFINEON
13	1	R1	3k	
14	2	R3,R7	30k	
15	1	R8	750	
16	1	R9	100k	
17	1	R10	19.1k	
18	1	R17	2.15	
19	1	U1	NX2155/MSOP-EP10	NEXSEM INC.

Demoboard Waveforms

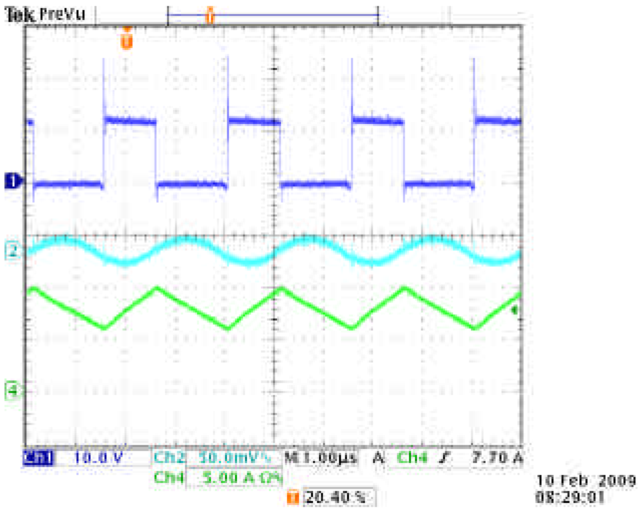


Fig.14 Output ripple(CH1 SW 10V/DIV, CH2 VOUT AC 50mV/DIV, CH4 INDUCTOR CURRENT 5A/DIV)

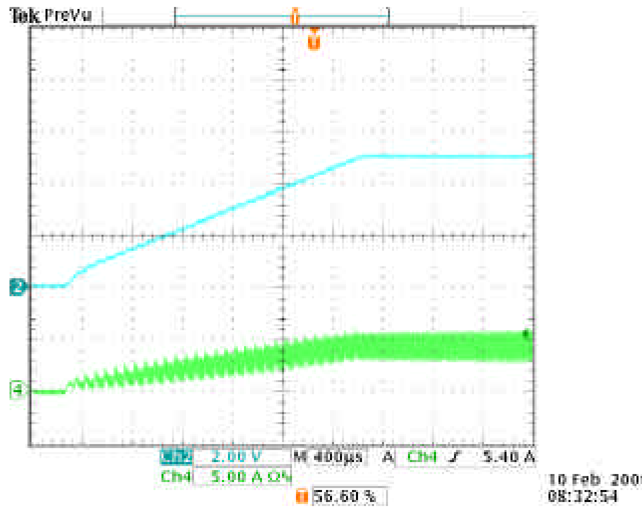


Fig.15 Startup(CH1 VOUT 2V/DIV, CH4 INDUCTOR CURRENT 5A/DIV)

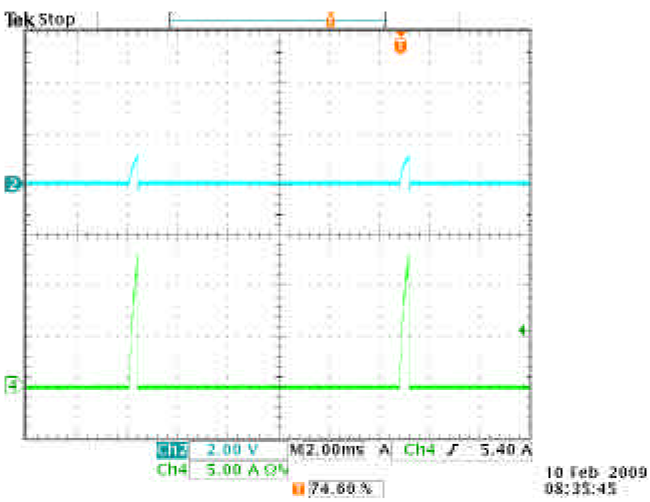


Fig.16 OCP protection during output short(CH2 VOUT 2V/DIV, CH4 OUTPUT CURRENT 5A/DIV)

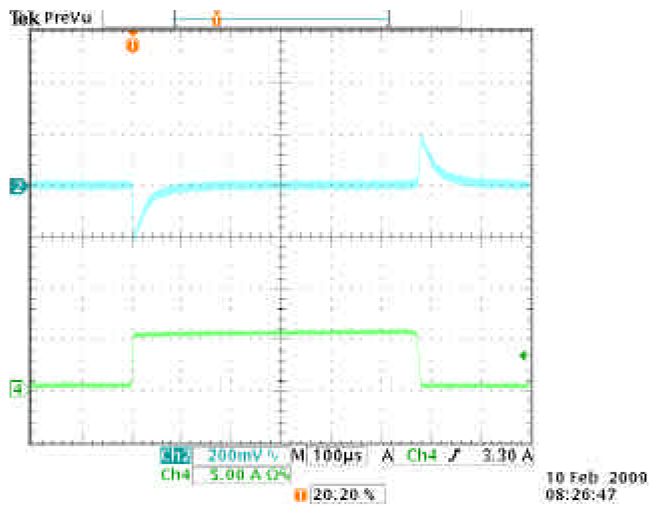


Fig.17 Output dynamic response(CH2 VOUT AC 200mV/DIV, CH4 OUTPUT CURRENT 5A/DIV)

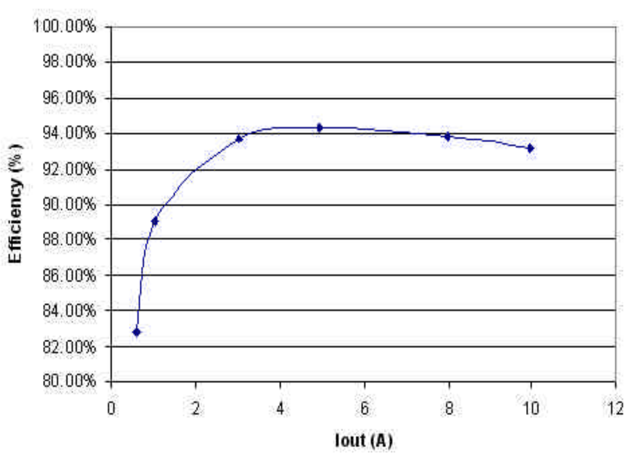


Fig.18 Output efficiency

APPLICATION INFORMATION

Symbol Used In Application Information:

V_{IN} - Input voltage

V_{OUT} - Output voltage

I_{OUT} - Output current

ΔV_{RIPPLE} - Output voltage ripple

F_S - Working frequency

ΔI_{RIPPLE} - Inductor current ripple

Output Inductor Selection

The selection of inductor value is based on inductor ripple current, power rating, working frequency and efficiency. Larger inductor value normally means smaller ripple current. However if the inductance is chosen too large, it brings slow response and lower efficiency. Usually the ripple current ranges from 20% to 40% of the output current. This is a design freedom which can be decided by design engineer according to various application requirements. The inductor value can be calculated by using the following equations:

$$L_{OUT}=\frac{V_{IN}-V_{OUT}}{\Delta I_{RIPPLE}}\times\frac{V_{OUT}}{V_{IN}}\times\frac{1}{F_S} \qquad ...(1)$$

$$I_{RIPPLE}=k\times I_{OUTPUT}$$

where k is between 0.2 to 0.4.

Output Capacitor Selection

Output capacitor is basically decided by the amount of the output voltage ripple allowed during steady state(DC) load condition as well as specification for the load transient. The optimum design may require a couple of iterations to satisfy both condition.

The amount of voltage ripple during the DC load condition is determined by equation(2).

$$\Delta V_{RIPPLE}=ESR\times\Delta I_{RIPPLE}+\frac{\Delta I_{RIPPLE}}{8\times F_S\times C_{OUT}} \qquad ...(2)$$

Where ESR is the output capacitors' equivalent series resistance,C_{OUT} is the value of output capacitors.

Typically when ceramic capacitors are selected as output capacitors, DC ripple spec is easy to be met, but mutiple ceramic capacitors are required at the output to meet transient requirement.

Compensator Design

Due to the double pole generated by LC filter of the power stage, the power system has 180^o phase shift , and therefore, is unstable by itself. In order to achieve accurate output voltage and fast transient response, compensator is employed to provide highest possible bandwidth and enough phase margin.Ideally,the Bode plot of the closed loop system has crossover frequency between1/10 and 1/5 of the switching frequency, phase margin greater than 50^o and the gain crossing 0dB with -20dB/decade. Power stage output capacitors usually decide the compensator type. If electrolytic capacitors are chosen as output capacitors, type II compensator can be used to compensate the system, because the zero caused by output capacitor ESR is lower than crossover frequency. Otherwise type III compensator should be chosen.

A. Type III compensator design

For low ESR output capacitors, typically such as Sanyo oscap and poscap, the frequency of ESR zero caused by output capacitors is higher than the crossover frequency. In this case, it is necessary to compensate the system with type III compensator. The following figures and equations show how to realize the type III compensator by transconductance amplifier.

$$F_{Z1}=\frac{1}{2\times\pi\times R_4\times C_2} \qquad ...(3)$$

$$F_{Z2}=\frac{1}{2\times\pi\times(R_2+R_3)\times C_3} \qquad ...(4)$$

$$F_{P1}=\frac{1}{2\times\pi\times R_3\times C_3} \qquad ...(5)$$

$$F_{P2}=\frac{1}{2\times\pi\times R_4\times\frac{C_1\times C_2}{C_1+C_2}} \qquad ...(6)$$

where F_{Z1},F_{Z2},F_{P1} and F_{P2} are poles and zeros in the compensator. Their locations are shown in figure 20.

The transfer function of type III compensator for transconductance amplifier is given by:

$$\frac{V_e}{V_{OUT}}=\frac{1-g_m\times Z_f}{1+g_m\times Z_{in}+Z_{in}/R_1}$$

For the voltage amplifier, the transfer function of compensator is

$$\frac{V_e}{V_{OUT}} = \frac{-Z_f}{Z_{in}}$$

To achieve the same effect as voltage amplifier, the compensator of transconductance amplifier must **satisfy this condition: R_4**>>2/gm. And it would be desirable if $R_1||R_2||R_3$>>1/gm can be met at the same time.

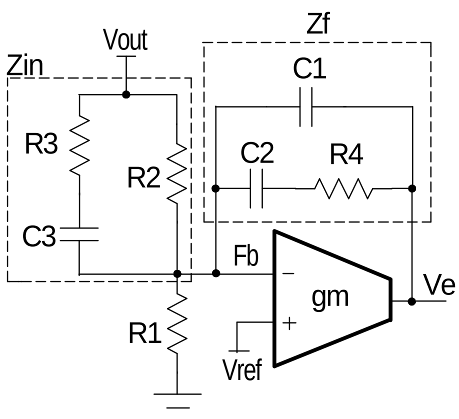


Figure 19 - Type III compensator using transconductance amplifier

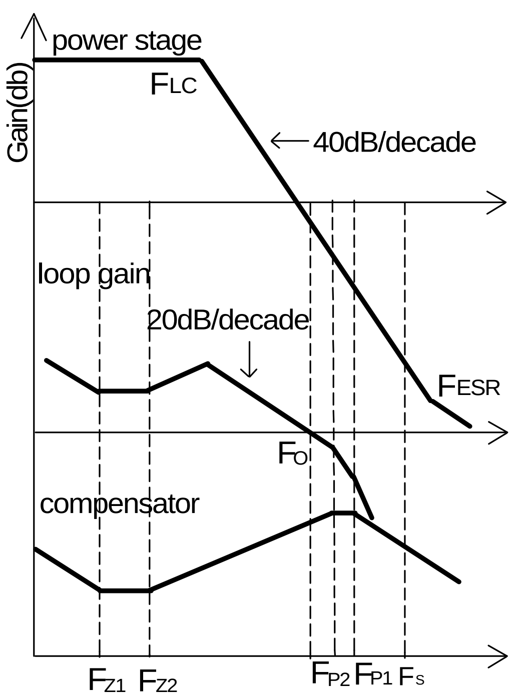


Figure 20 - Bode plot of Type III compensator

B. Type II compensator design

Type II compensator can be realized by simple RC circuit without feedback as shown in figure 22. R_3 and C_1 introduce a zero to cancel the double pole effect. C_2 introduces a pole to suppress the switching noise. The following equations show the compensator pole zero location and constant gain.

$$Gain = g_m \times \frac{R_1}{R_1 + R_2} \times R_3 \quad \text{... (7)}$$

$$F_z = \frac{1}{2 \times \pi \times R_3 \times C_1} \quad \text{... (8)}$$

$$F_p \approx \frac{1}{2 \times \pi \times R_3 \times C_2} \quad \text{... (9)}$$

For this type of compensator, F_O has to satisfy $F_{LC} < F_{ESR} << F_O <= 1/10 \sim 1/5 F_s$.

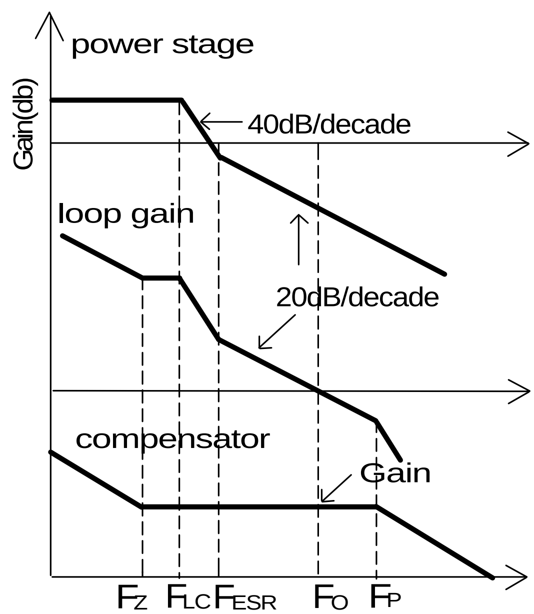


Figure 21 - Bode plot of Type II compensator

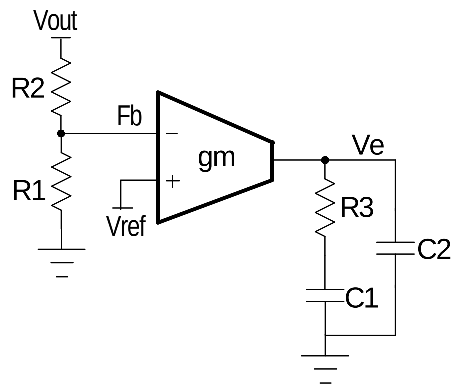


Figure 22 - Type II compensator with transconductance amplifier

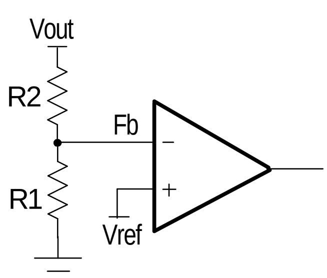
Output Voltage Calculation

Output voltage is set by reference voltage and external voltage divider. The reference voltage is fixed at 0.8V. The divider consists of two ratioed resistors so that the output voltage applied at the Fb pin is 0.8V when the output voltage is at the desired value. The following equation and picture show the relationship between V_{OUT} , V_{REF} and voltage divider.

$$R_1 = \frac{R_2 \times V_{REF}}{V_{OUT} - V_{REF}} \qquad ...(10)$$

where R_2 is part of the compensator, and the value of R_1 value can be set by voltage divider.

See compensator design for R_1 and R_2 selection.



Voltage divider

Figure 23 - Voltage divider

Over Current Protection

Over current protection is achieved by sensing current through the low side MOSFET. A typical internal current source of 37uA flowing through an external resistor connected from OCP pin to SW node sets the over current protection threshold. When synchronous FET is on, the voltage at node SW is given as

$$V_{SW} = -I_L \times R_{DSON}$$

The voltage at pin OCP is given as

$$I_{OCP} \times R_{OCP} + V_{SW}$$

When the voltage is below zero, the over current occurs.

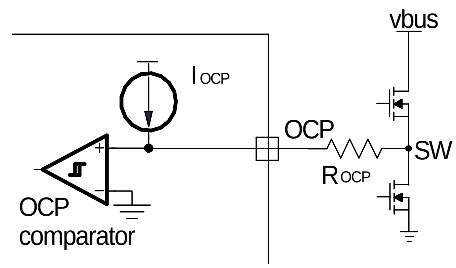


Figure 24 - Over current protection

The over current limit can be set by the following equation

$$I_{SET} = \frac{I_{OCP} \times R_{OCP}}{K \times R_{DSON}}$$

Frequency Selection

The frequency can be set by external Rt resistor. The relationship between frequency and RT pin is shown as follows.

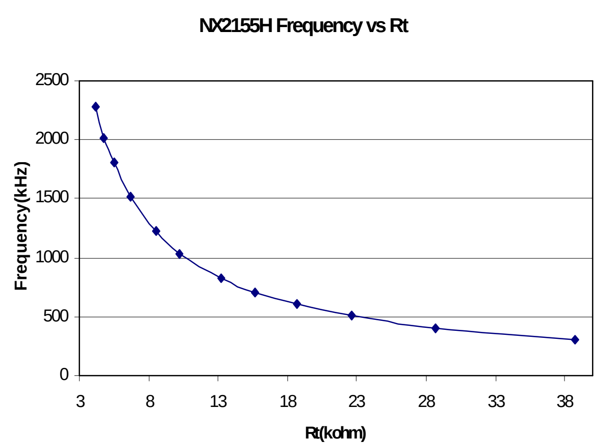
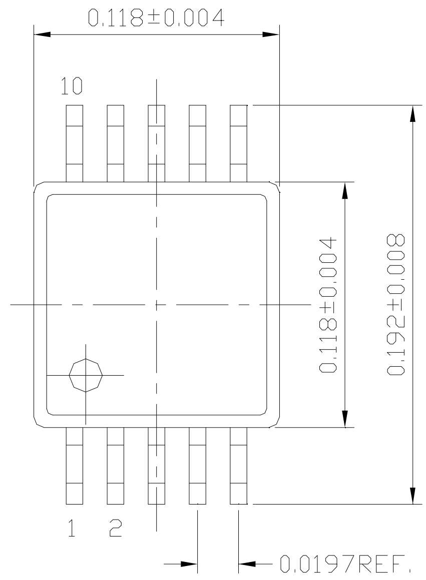
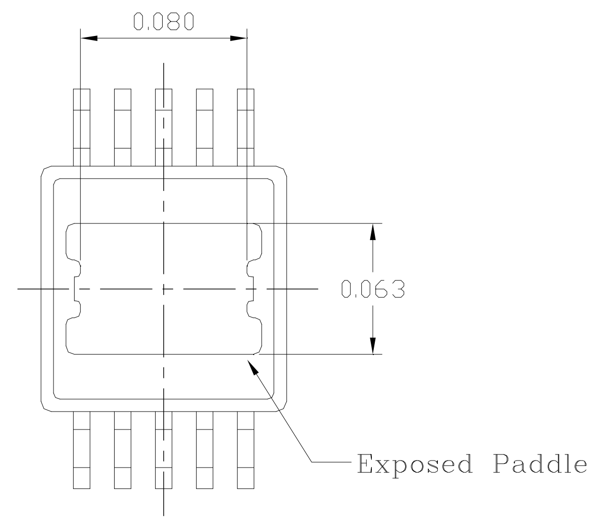


Figure 25 - Frequency versus Rt resistor

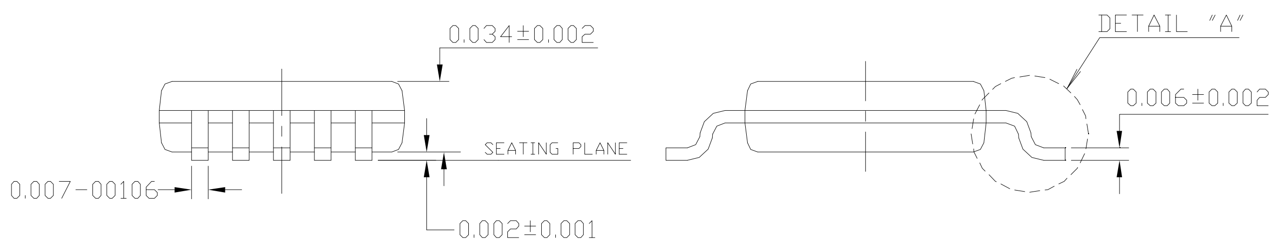
MSOP 10 PIN WITH EXPOSED PAD OUTLINE DIMENSIONS



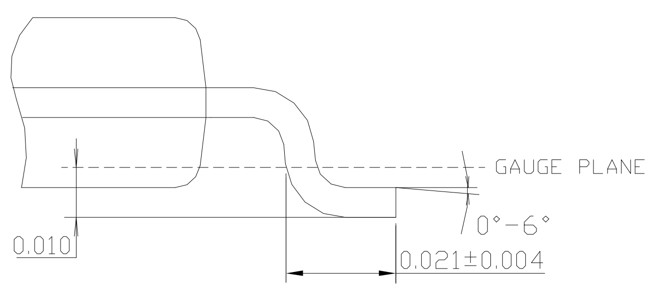
Top View



Bottom View



Side View



DETAIL "A"

NOTE: ALL DIMENSIONS ARE DISPLAYED IN INCHES.

Microsemi
Analog Mixed Signal Group
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