
CCGA to FBGA Adapter Sockets

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Introduction

Microsemi[®] SoC Products Group recently introduced RTAX-S/L, the next generation designed-for-space antifuse field programmable gate arrays (FPGAs). RTAX-S/L, with up to four million system gates, is SoC Products Group's highest density family, providing the space designer with nearly 250 k ASIC gates and error correction and detection (EDAC) protected static RAM. RTAX-S/L is the first SoC Products Group family designed for use in the ceramic column grid array (CCGA) package configuration. SoC Products Group has developed a low cost prototyping methodology for RTAX-S/L using the Axcelerator[®] family of FPGAs.

RTAX-S/L is a derivative of the Axcelerator family. RTAX-S/L FPGAs can be prototyped using the comparable commercial Axcelerator device at a much lower cost than the equivalent space device. SoC Products Group has developed a CCGA to fine pitch ball grid array (FBGA) adapter socket to reduce RTAX-S/L development costs. SoC Products Group is also offering the CG624 package with the RTSX72SU, using the A54SX72A as the prototyping vehicle.

This assembly procedure document covers the RTAX-S/L and RTSX-SU product families, which explains what a CCGA-FBGA adapter socket is, defines the component parts, and describes how to assemble the adapter. Once the adapter is assembled, the care and handling are similar to a CCGA packaged device.

The intention of the prototyping adaptors is to provide functional validation and not at-speed timing validation. The prototyping adaptors may limit the performance of the FPGA I/O buffers.

The CCGA to FBGA Adapter Socket

The CCGA to FBGA adapter socket has a CCGA ceramic package configuration on the bottom and an FBGA configuration on top. The SoC Products Group CG (abbreviated for CCGA or ceramic column grid array) to FG (abbreviated for FBGA or fine pitch ball grid array) adapter socket offering allows for easy prototyping when using an FG package to prototype a CG package. The ordering part numbers are listed in [Table 1 on page 2](#).

Table 1 • Ordering Part Numbers

Adapter Socket	Ordering Part Number	Prototyped and Prototype Device
CG624 to FG484	SK-SX72-CG624RTFG484	For prototyping RTSX72SU-CG624 or A54SX72A-CG624 using A54SX7A FG484
CG624 to FG896	SK-AX1-AX2-KITTOP and SK-AX1-CG624-KITBTM	For prototyping RTAX1000S-CG624, RTAX1000SL-CG624, or AX1000-CG624 using AX1000-FG896 package
CG624 to FG896	SK-AX1-AX2-KITTOP and SK-AX2-CG624-KITBTM	For prototyping RTAX2000S-CG624, RTAX2000SL-CG624, or AX2000-CG624 using AX2000-FG896 package

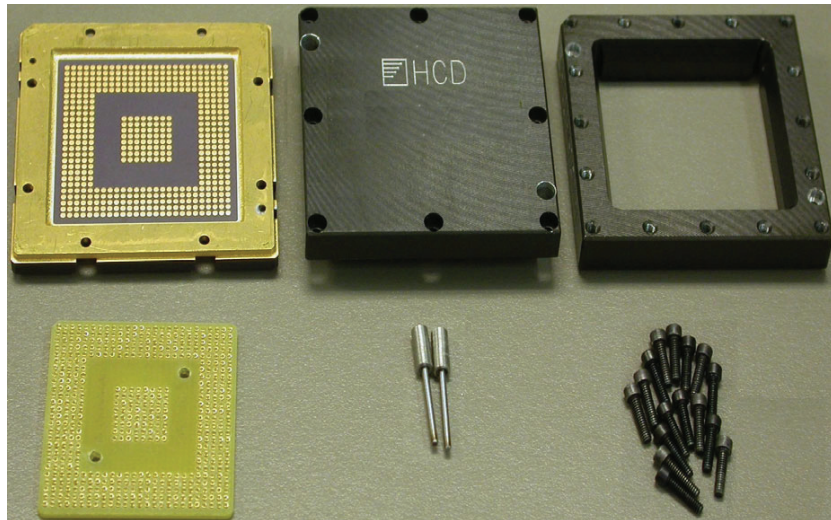


Figure 1 • CCGA to FBGA Adapter Socket Components

Notes:

1. Top, from left: ceramic adapter, socket lid, socket housing.
2. Bottom, from left: socket interposer, alignment pins, fixing screws.

CCGA to FBGA Ceramic Adapter Configurations

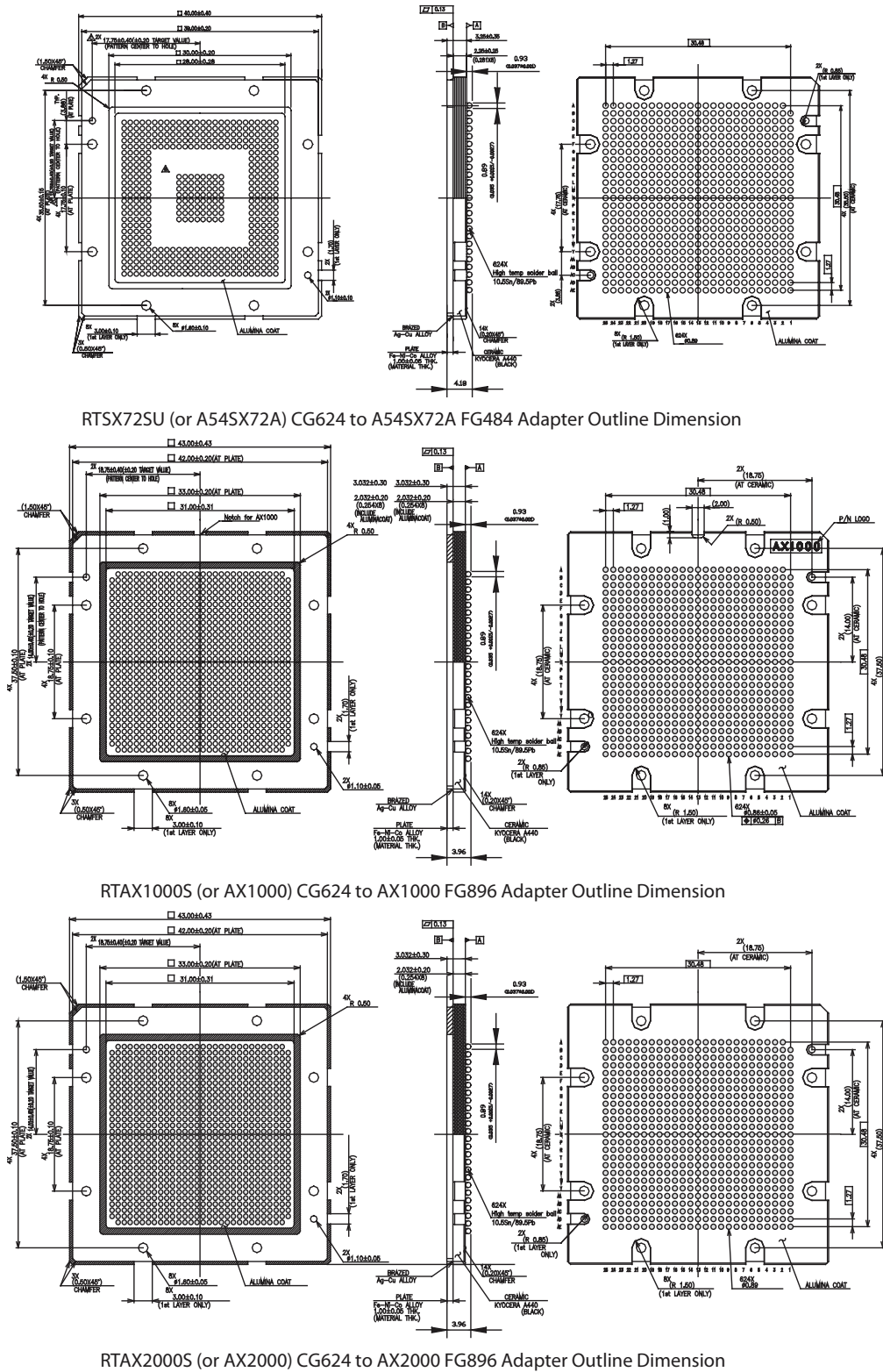


Figure 2 • Ceramic Adapter Top View (Left) and Bottom View (Right) with Dimensions

Assembly Procedure

Step 1

Note: The -KITBTM parts for CG624 devices contain all the parts needed for Step 1. Both the SK-AX1-CG624-KITBTM and SK-AX2-CG624-KITBTM contain the housing, ceramic adapter, eight screws and two alignment pins.

Note: See [Figure 11 on page 7](#) for an outline drawing of the CG624 to FG484 23x23 Adapter Socket. Alignment pins can (optionally) be used prior to step 1 to align the housing to the ceramic adapter. The same alignment pins can be (optionally) used to align the assembled housing plus adapter to the circuit board just prior to Step 2. Reflow in "[Step 2](#)" on [page 5](#) means that you must have put the solder onto the board, place the assembled ceramic adapter onto the PCB, and then complete the reflow. Placing the assembled adapter onto the PCB is made easier if the alignment pins are used, but corresponding alignment holes must have been pre-drilled into the PCB during PCB manufacture for this to work.

Tighten the socket housing to the adapter. Step 1 includes three sub-steps:

1. Turn the socket housing and ceramic adapter upside down ([Figure 3](#)).
2. Fasten the socket housing to the ceramic adapter using eight of the screws provided ([Figure 4](#)).
3. Turn the ceramic adapter (with socket housing) over ([Figure 5 on page 5](#)).

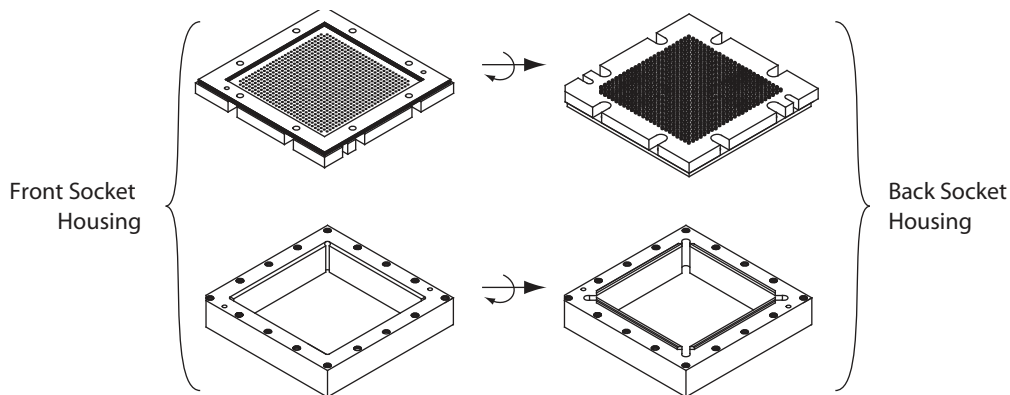


Figure 3 • View of Ceramic Adapter (Top) and Socket Housing (Bottom) Turned Over

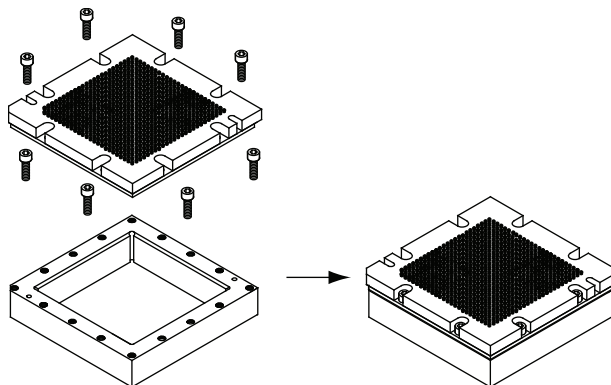


Figure 4 • View of Ceramic Adapter Fastened to Socket Housing Using the Screws Provided

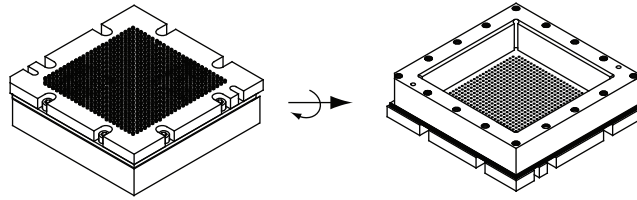


Figure 5 • View of Adapter Socket Assembly with Socket Housing Attached

Step 2

Reflow the adapter to the printed circuit board (PCB) (Figure 6).

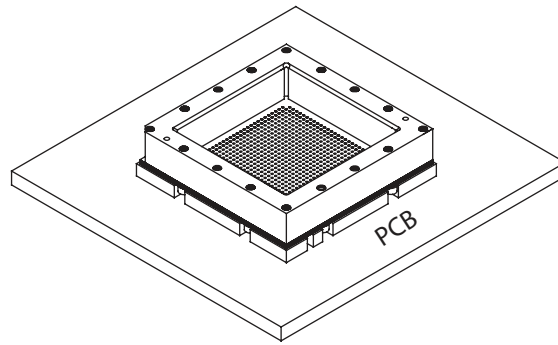


Figure 6 • Adapter Reflowed to the PCB

Step 3

Place the socket interposer into the adapter (Figure 7).

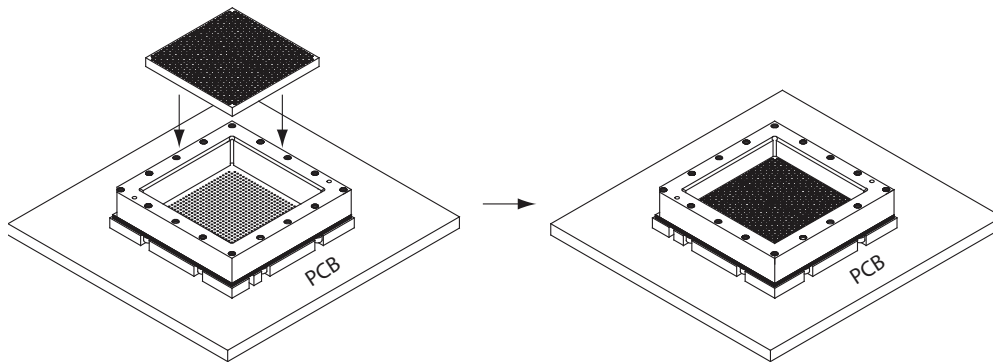


Figure 7 • Socket Interposer Placement in the Adapter Assembly

Step 4

Place the FBGA package into the adapter (Figure 8).

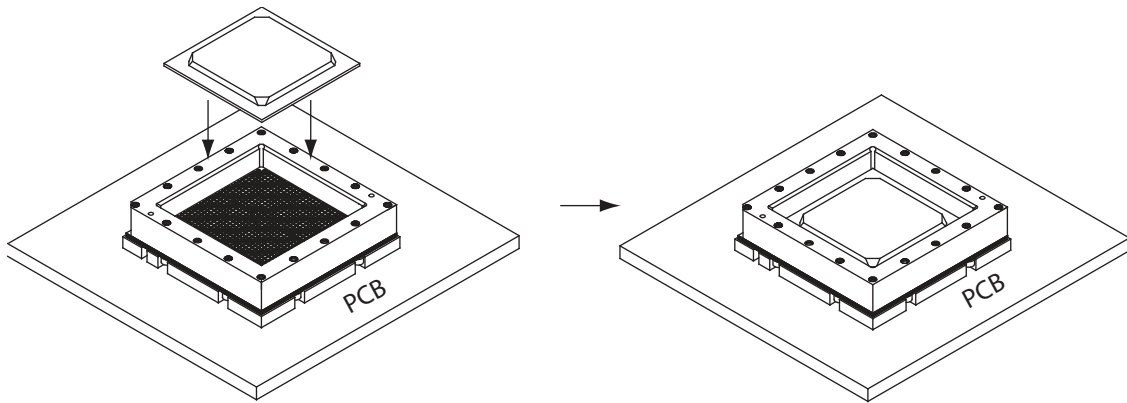


Figure 8 • View of the FPGA Package Placement in the Adapter Assembly

Step 5

Fasten the socket lid to the socket housing using the remaining eight screws provided (Figure 9).

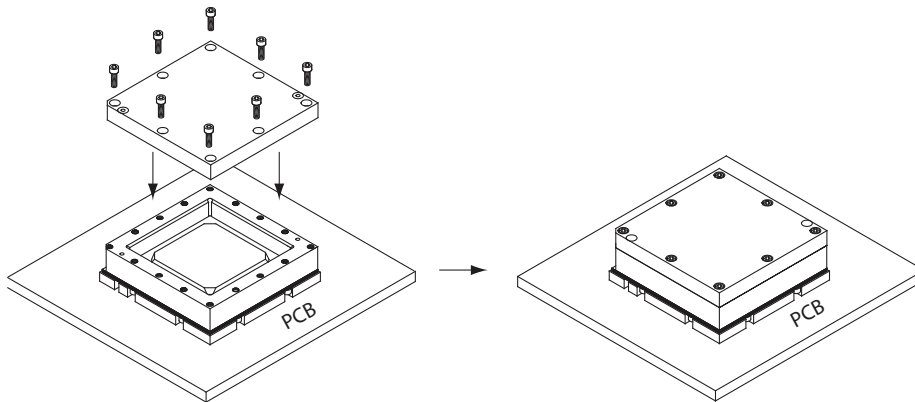


Figure 9 • View of the Socket Lid and Screw Placement

Note: If prototyping CG624 parts using AX1000-FG896 or AX2000-FG896, -KITTOP contains the screws, interposer, and lid. The SoC Products Group part for these components is SK-AX1-AX2-KITTOP.

PCB Pad Layout

Pads should be laid out according to the solder column dimensions of the CG package. Refer to the CG package drawing and the SoC Products Group application note, CCGA. Since the socket adapter's overall size is larger than the actual CG package, you must consider the size difference between the socket adapter and CG package during board layout, particularly if the same board will be used for both prototyping and production. Figure 10 shows PCB pad layout specifications.

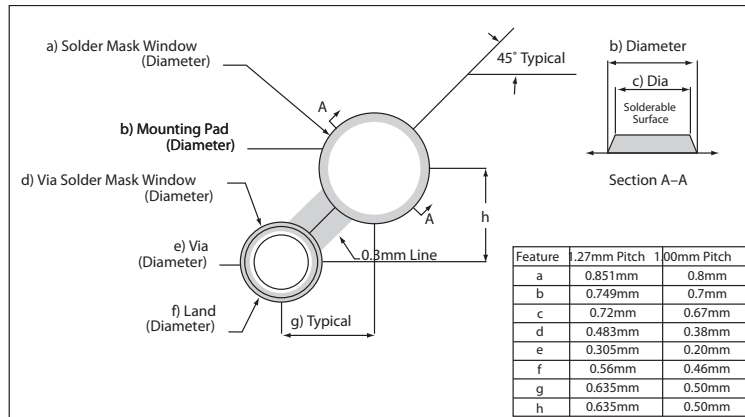


Figure 10 • PCB Pad Layout Specifications

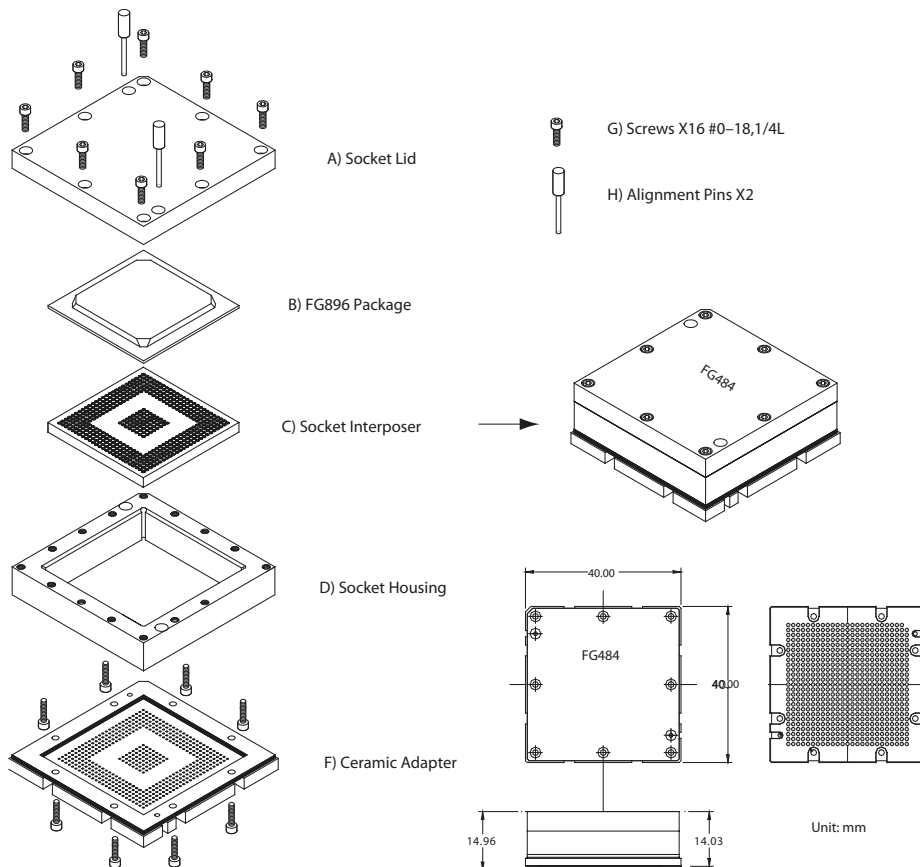


Figure 11 • CG624 to FG484 23x23 Adapter Socket Outline Drawing

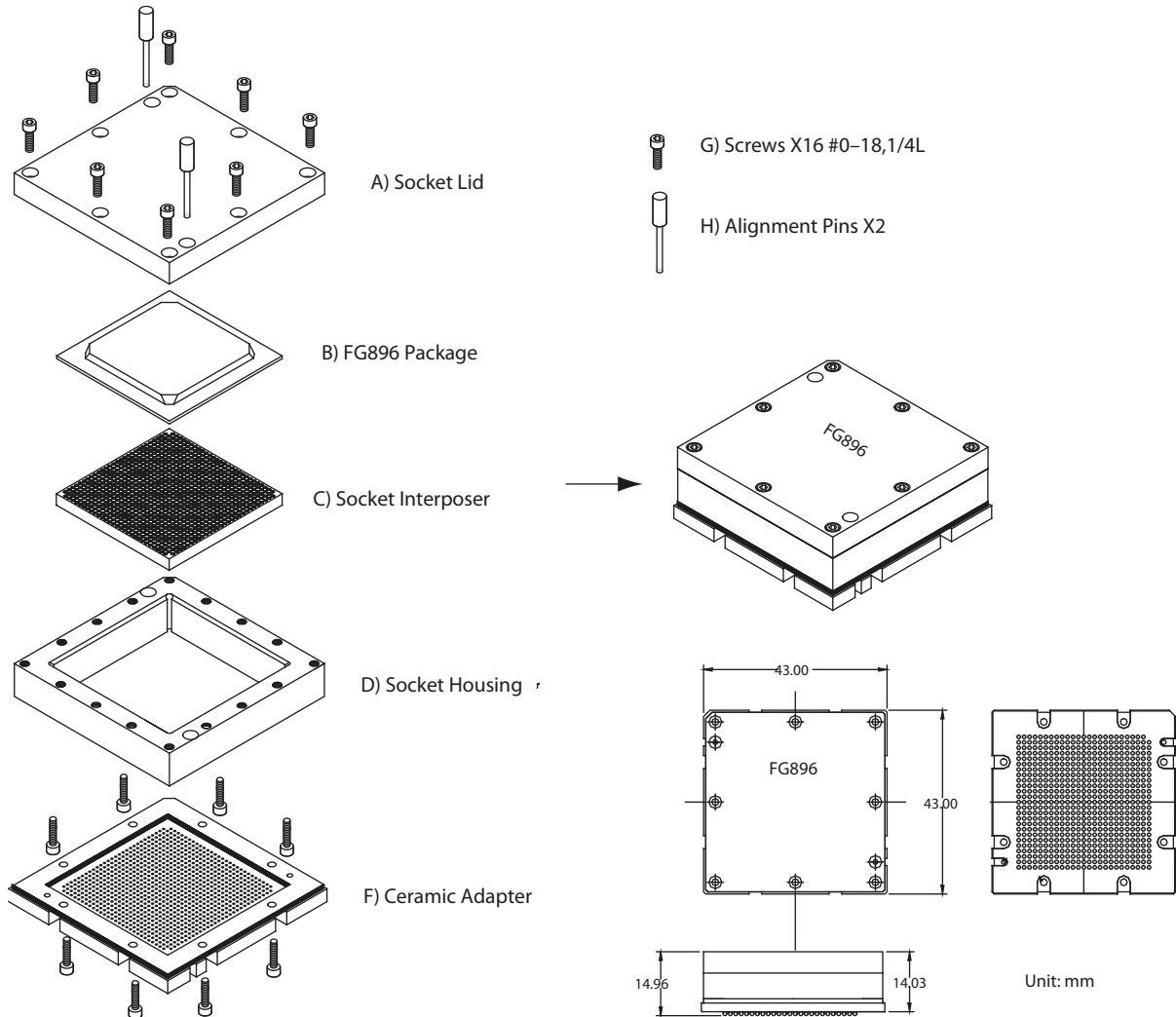


Figure 12 • CG624 to FG896 Adapter Socket Outline Drawing

Note:

1. A set of boards will require at least one -KITTOP and one -KITBTM kit for each board. The -KITTOP components may be moved from board to board for testing one at a time, if a cost saving is required.
2. SK-AX1-AX2-KITTOP contains a socket lid (A), an interposer (C), eight screws and two alignment pins (half of G). SK-AX1-CG624-KITBTM contains the socket housing (D) a unique ceramic adapter for AX1000 use (F), eight screws and two alignment pins. (half of G).
3. SK-AX2-CG624-KITBTM contains socket housing (D), a unique ceramic adapter for AX2000 use (F), eight screws and two alignment pins (half of G).

Alignment Pins

There are two alignment pins for aligning the socket housing to the adapter. The same pins can be used to align the assembled adapter socket to the PCB. Alignment holes on the PCB are optional. You must decide whether or not to include alignment holes on a board. Two alignment pins are included in the -KITBTM units. No alignment pins are included in -KITTOP units.

Reflow Profile

Since reflow profiles depend heavily upon the size of the board and other components, you must perform additional fine tuning from the general profile shown in [Figure 13](#).

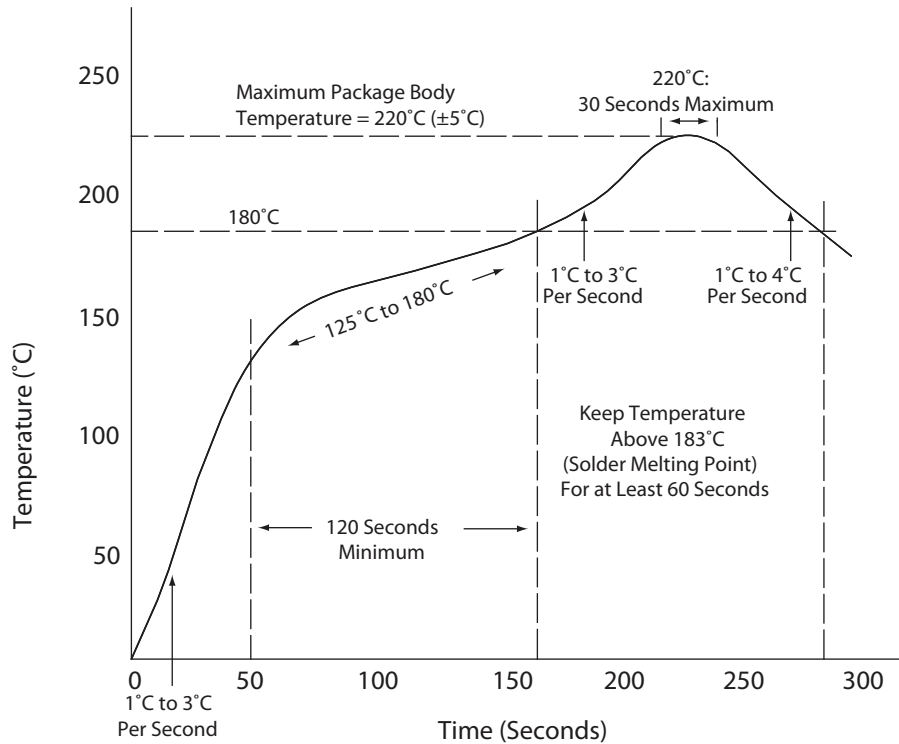


Figure 13 • Sample Temperature Profile for Infrared (IR) or Convection Reflow

CCGA to FBGA Adapter Pin Mapping List

The CCGA to FBGA adapter is routed from the FBGA package to match the existing die pad available to the CCGA device being prototyped ([Table 2 on page 10](#)).

Prototyped Product, Adapter, and PCB Design Matrix

Designing the PCB for a specific product requires an understanding of which adapter socket will work. Each adapter socket is routed differently, depending on the commercial Axcelerator FG package used for prototyping and the Axcelerator device or RadTolerant equivalent derivative being prototyped. [Table 3 on page 10](#) shows the combinations that will work.

Table 2 • CCGA to FBGA Adapter Pin Mapping List Documents

Adapter Socket	Ordering Part Number	Prototyped and Prototype Device	Adapter Pin Mapping List Document Number
CG624 to FG484	SK-SX72-CG624RTFG484	For prototyping RTSX72SU-CG624 or A54SX72A-CG624 using A54SX72A FG484	www.microsemi.com/soc/techdocs/package/default.aspx
CG624 to FG896	SK-AX1-AX2-KITTOP and SK-AX1-CG624-KITBTM	For prototyping RTAX1000S-CG624, RTAX1000SL-CG624, or AX1000-CG624 using AX1000-FG896 package	
CG624 to FG896	SK-AX1-AX2-KITTOP and SK-AX2-CG624-KITBTM	For prototyping RTAX2000S-CG624, RTAX2000SL-CG624, or AX2000-CG624 using AX2000-FG896 package	

Table 3 • PCB Design Matrix

Prototyped Product	Adapter Part Number	Prototype Vehicle	PCB Design
A54SX72A-CG624	SK-SX72-CG624RTFG484	A54SX72A-FG484	A54SX72A-CG624
RTSX72SU-CG624	SK-SX72-CG624RTFG484	A54SX72A-FG484	A54SX72A-CG624
AX1000-CG624	SK-AX1-AX2-KITTOP and SK-AX1-CG624-KITBTM	AX1000-FG896	AX1000-CG624
AX2000-CG624	SK-AX1-AX2-KITTOP and SK-AX2-CG624-KITBTM	AX2000-FG896	AX2000-CG624
RTAX1000SL-CG624	SK-AX1-AX2-KITTOP and SK-AX1-CG624-KITBTM	AX1000-FG896	AX1000-CG624 ¹
RTAX2000SL-CG624	SK-AX1-AX2-KITTOP and SK-AX2-CG624-KITBTM	AX2000-FG896	AX2000-CG624 ¹
RTAX1000SL-CG624	SK-AX1-AX2-KITTOP and SK-AX1-CG624-KITBTM	AX1000-FG896	RTAX1000S-CG624 ^{1,2}
RTAX2000SL-CG624	SK-AX1-AX2-KITTOP and SK-AX2-CG624-KITBTM	AX2000-FG896	RTAX2000S-CG624 ^{1,2}

Note:

1. The PCB designer should consider the eight pin-pairs of the Phase-Locked Loop (PLL) analog power supply (VCCPLA/VCOMPLA, VCCPLB/VCOMPLB, VCCPLC/VCOMPLC, VCCPLD/VCOMPLD, VCCPLE/VCOMPLE, VCCPLF/VCOMPLF, VCCPLG/VCOMPLG, and VCCPLH/VCOMPLH). They should be treated as follows:

VCCPLA/B/C/D/E/F/G/H – there are eight in each device. VCCPLA supports the PLL associated with global resource HCLKA, VCCPLB supports the PLL associated with global resource HCLKB, etc. These PLL analog power supply pins should be connected to 1.5 V, whether or not the PLL is used. Refer to the *Axcelerator Family FPGAs and RTAX-S/L Family FPGAs* datasheets for pin assignment information.

VCOMPLA/B/C/D/E/F/G/H – these are compensation reference signals for the internal PLLs. There are eight in each device. VCOMPLA supports the PLL associated with global resource HCLKA, VCOMPLE supports the PLL associated with global resource HCLKE, etc.

The VCOMPLX pins should be left floating if the PLL is not being used. Refer to the [Axcelerator Family FPGAs and RTAX-S/L Family FPGAs](#) datasheets for pin assignment information.

2. Since the AX and the RTAX-S/L devices are exactly pin compatible except for the PLL, which the RTAX-S/L does not have, designing the PCB with VCCPL(X) pins connected to 1.5 V will not affect the function of the RTAX-S/L devices. Pins for VCOMPL(X) can be designed with land patterns only. These 16 PLL pins are not connected internally inside the RTAX-S/L packages.

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Related Documents

Application Notes

Ceramic Column Grid Arrays (CCGA)

www.microsemi.com/soc/documents/CCGA_AN.pdf

Datasheets

Axcelerator Family FPGAs

www.microsemi.com/soc/documents/AX_DS.pdf

RTAX-S RadTolerant FPGAs

www.microsemi.com/soc/documents/RTAXS_DS.pdf

Pin Mapping Lists

All pin mapping lists are available at www.microsemi.com/soc/techdocs/package/default.aspx.

List of Changes

The following table lists critical changes that were made in each revision of the document.

Revision*	Changes	Page
55900016-4/11.11	Added 2 lines at the end of "Introduction" section (SAR 33472).	1
55900016-3/7.06	All tables were updated to include current ordering part numbers	1, 10, and 11
	Clarifying notes added to Step 5 and Figure 12	6, 9

Note: *The revision number is located in the part number after the hyphen. The part number is displayed at the bottom of the last page of the document. The digits following the slash indicate the month and year of publication.



Microsemi Corporate Headquarters
One Enterprise Drive, Aliso Viejo CA 92656
Within the USA: (800) 713-4113
Outside the USA: (949) 221-7100
Fax: (949) 756-0308 · www.microsemi.com

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