UC184xA / 284xA / 384xA

CURRENT MODE PWM CONTROLLER

PRODUCTION DATA SHEET

LINFINITY — A MICROSEMI COMPANY

THE INFINITE POWER OF INNOVATION

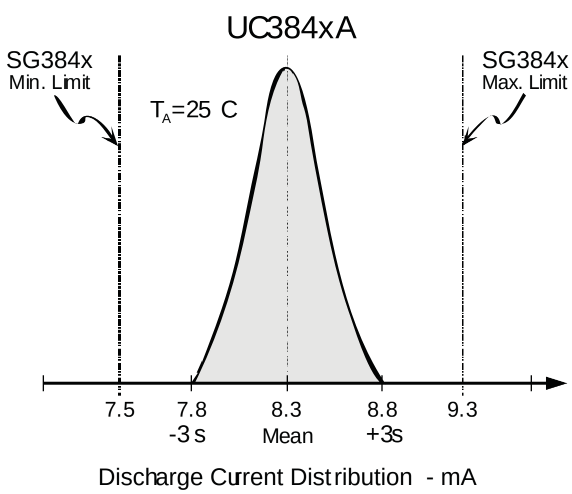
DESCRIPTION

The UC184xA family of control ICs provides all the necessary features to implement off-line fixed-frequency, current-mode switching power supplies with a minimum of external components. The current mode architecture demonstrates improved load regulation, pulse-by-pulse current limiting and inherent protection of the power supply output switch. The IC includes: A bandgap reference trimmed to ±1% accuracy, an error amplifier, a current sense comparator with internal clamp to 1V, a high current totem pole output stage for fast switching of power MOSFET's, and an externally programmable oscillator to set frequency and maximum duty cycle. The undervoltage lock-out is designed to operate with 250µA typ. start-up current, allowing an efficient bootstrap supply voltage design. Available options for this family of products, such as start-up voltage hysteresis and duty cycle, are summarized below in the Available Options section. The UC184xA family of control ICs is also available in 14-pin SOIC package which makes the Power Output Stage Collector and Ground pins available.

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: **http://www.microsemi.com**

PRODUCT HIGHLIGHT

COMPARISON OF UC384xA VS. SG384x DISCHARGE CURRENT



KEY FEATURES

- LOW START-UP CURRENT. (0.5mA max.)
- TRIMMED OSCILLATOR DISCHARGE CURRENT. (See Product Highlight)
- OPTIMIZED FOR OFF-LINE AND DC-TO-DC CONVERTERS.
- AUTOMATIC FEED FORWARD COMPENSATION.
- PULSE-BY-PULSE CURRENT LIMITING.
- ENHANCED LOAD RESPONSE CHARACTERISTICS.
- UNDER-VOLTAGE LOCKOUT WITH HYSTERESIS.
- DOUBLE PULSE SUPPRESSION.
- HIGH-CURRENT TOTEM POLE OUTPUT.
- INTERNALLY TRIMMED BANDGAP REFERENCE.
- 500KHz OPERATION.
- LOW RO ERROR AMPLIFIER.

KEY FEATURES

- ECONOMICAL OFF-LINE FLYBACK OR FORWARD CONVERTERS.
- DC-DC BUCK OR BOOST CONVERTERS.
- LOW COST DC MOTOR CONTROL.

Available Options

Part#	Start-Up Voltage	Hysteresis	Max. Duty Cycle
UCx842A	16V	6V	<100%
UCx843A	8.4V	0.8V	<100%
UCx844A	16V	6V	<50%
UCx845A	8.4A	0.8V	<50%

PACKAGE ORDER INFO

T_A (°C)	M Plastic DIP 8-Pin (RoHS Compliant / Pb-free Transition DC: 0503)	DM Plastic SOIC 8-Pin (RoHS Compliant / Pb-free Transition DC: 0440)	D Plastic SOIC 14-Pin (RoHS Compliant / Pb-free Transition DC: 0440)	Y Ceramic DIP 8-Pin
0 to 70	UC384xAM	UC384xADM	UC384xAD	-
-40 to +85	UC284xAM	UC284xADm	UC284xAD	UC284xAY
-55 to 125	-	-	-	UC184xAY

Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. UC3842ADM-TR)

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ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Low Impedance Source) (V_{CC}) 30V
Supply Voltage (I_{CC} < 30mA) .... Self Limiting
Output Current .... ±1A
Output Energy (Capacitive Load) 5µJ
Analog Inputs (V_{FB} & I_{SENSE}) .... -0.3V to +6.3V
Error Amp Output Sink Current 10mA
Power Dissipation at T_A = 25°C (M Package) 1W
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) .... 300°C
Peak Package Solder Reflow Temp. (40 second max. exposure) .... 260°C (+0, -5)

Note 1. Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal. Pin numbers refer to DIL packages only.

THERMAL DATA

M PACKAGE:

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	95°C/W

DM PACKAGE:

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	165°C/W

D PACKAGE:

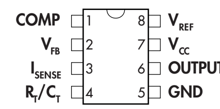
THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	120°C/W

Y PACKAGE:

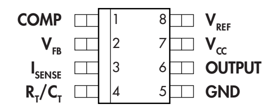
THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	130°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system.
All of the above assume no ambient airflow

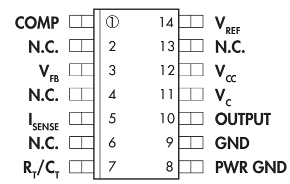
PACKAGE PIN OUTS



M & Y PACKAGE
(Top View)



DM PACKAGE
(Top View)



D PACKAGE
(Top View)

RoHS / Pb-free 100% Matte Tin Lead Finish

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ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for UC384xA with 0°C ≤ T_A ≤ 70°C, UC284xA with -40°C ≤ T_A ≤ 85°C, UC184xA with -55°C ≤ T_A ≤ 125°C; V_{CC}=15V; R_T=10K; C_T=3.3nF. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Symbol	Test Conditions	UC184xA/284xA Min.	UC184xA/284xA Typ.	UC184xA/284xA Max.	UC384xA Min.	UC384xA Typ.	UC384xA Max.	Units
Reference Section									
Output Voltage	V_{REF}	T_J = 25°C, I_L = 1mA	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation		12 ≤ V_{IN} ≤ 25V		6	20		6	20	mV
Load Regulation		1 ≤ I_O ≤ 20mA		6	25		6	25	mV
Temperature Stability (Note 2 & 7)				0.2	0.4		0.2	0.4	mV/°C
Total Output Variation		Over Line, Load, and Temperature	4.9		5.1	4.82		5.18	V
Output Noise Voltage (Note 2)	V_N	10Hz ≤ f ≤ 10kHz, T_J = 25°C		50			50		µV
Long Term Stability (Note 2)		T_A = 125°C, t = 1000hrs		5	25		5	25	mV
Output Short Circuit Current	I_{SC}		-30	-100	-180	-30	-100	-180	mA
Oscillator Section									
Initial Accuracy (Note 6)		T_J = 25°C	47	52	57	47	52	57	kHz
Voltage Stability		12 ≤ V_{CC} ≤ 25V		0.2	1		0.2	1	%
Temperature Stability (Note 2)		T_{MIN} ≤ T_A ≤ T_{MAX}		5			5		%
Amplitude (Note 2)				1.7			1.7		V
Discharge Current		T_J = 25°C, $V_{PIN 4}$ = 2V	7.8	8.3	8.8	7.8	8.3	8.8	mA
		$V_{PIN 4}$ = 2V, T_{MIN} ≤ T_A ≤ T_{MAX}	7.5		8.8	7.6		8.8	mA
Error Amp Section									
Input Voltage		$V_{PIN 1}$ = 2.5V	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current	I_B			-0.3	-1		-0.3	-2	µA
Open Loop Gain	A_{VOL}	2 ≤ V_O ≤ 4V	65	90		65	90		dB
Unity Gain Bandwidth (Note 2)	UGBW	T_J = 25°C	0.7	1		0.7	1		MHz
Power Supply Rejection Ratio (Note 3)	PSRR	12 ≤ V_{CC} ≤ 25V	60	70		60	70		dB
Output Sink Current	I_{OL}	$V_{PIN 2}$ = 2.7V, $V_{PIN 1}$ = 1.1V	2	6		2	6		mA
Output Source Current	I_{OH}	$V_{PIN 2}$ = 2.3V, $V_{PIN 1}$ = 5V	-0.5	-0.8		-0.5	-0.8		mA
Output Voltage High Level	V_{OH}	$V_{PIN 2}$ = 2.3V, R_L = 15K to ground	5	6		5	6		V
Output Voltage Low Level	V_{OL}	$V_{PIN 2}$ = 2.7V, R_L = 15K to V_{REF}		0.7	1.1		0.7	1.1	V
Current Sense Section									
Gain (Note 3 & 4)	A_{VOL}		2.85	3	3.15	2.85	3	3.15	V/V
Maximum Input Signal (Note 3)		$V_{PIN 1}$ = 5V	0.9	1	1.1	0.9	1	1.1	V
Power Supply Rejection Ratio (Note 3)	PSRR	12 ≤ V_{CC} ≤ 25V		70			70		dB
Input Bias Current	I_B			-2	-10		-2	-10	µA
Delay to Output (Note 2)	T_{pd}	$V_{PIN 3}$ = 0 to 2V		150	300		150	300	ns
Output Section									
Output Low Level	V_{OL}	I_{SINK} = 20mA		0.1	0.4		0.1	0.4	V
		I_{SINK} = 200mA		1.5	2.2		1.5	2.2	V
Output High Level	V_{OH}	I_{SOURCE} = 20mA	13	13.5		13	13.5		V
		I_{SOURCE} = 200mA	12	13.5		12	13.5		V
Rise Time (Note 2)	T_R	T_J = 25°C, C_L = 1nF		50	150		50	150	ns
Fall Time (Note 2)	T_F	T_J = 25°C, C_L = 1nF		50	150		50	150	ns
UVLO Saturation	V_{SAT}	V_{CC} = 5V, I_{SINK} = 10mA		0.7	1.2		0.7	1.2	V

(Electrical Characteristics continue next page.)

ELECTRICAL CHARACTERISTICS (Con't.)

Parameter	Symbol	Test Conditions	UC184xA/284xA Min.	UC184xA/284xA Typ.	UC184xA/284xA Max.	UC384xA Min.	UC384xA Typ.	UC384xA Max.	Units
Under-Voltage Lockout Section									
Start Threshold		x842A/4A	15	16	17	14.5	16	17.5	V
		x843A/5A	7.8	8.4	9.0	7.8	8.4	9.0	V
Min. Operation Voltage After Turn-On		x842A/4A	9	10	11	8.5	10	11.5	V
		x843A/5A	7.0	7.6	8.2	7.0	7.6	8.2	V
PWM Section									
Maximum Duty Cycle		x842A/3A	94	96	100	94	96	100	%
		x844A/5A	47	48	50	47	48	50	%
Minimum Duty Cycle					0			0	%
Total Standby Section									
Start-Up Current				0.3	0.5		0.3	0.5	mA
Operating Supply Current	I_{CC}			11	17		11	17	mA
Zener Voltage	V_Z	I_{CC} = 25mA	30	35		30	35		V

Notes: 2. These parameters, although guaranteed, are not 100% tested in production.

3. Parameter measured at trip point of latch with $V_{VFB} = 0$.

4. Gain defined as: $A_{VOL} = \frac{\Delta V_{COMP}}{\Delta V_{ISENSE}}$; $0 \le V_{ISENSE} \le 0.8V$.

5. Adjust V_{CC} above the start threshold before setting at 15V.

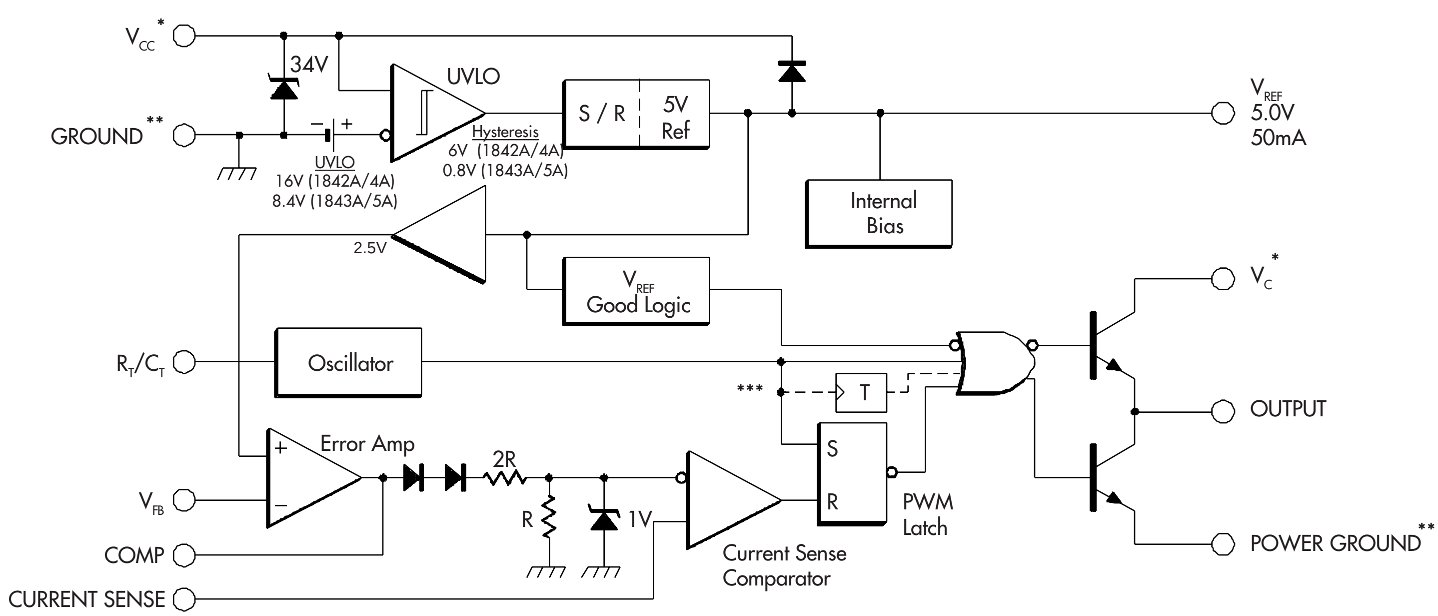
6. Output frequency equals oscillator frequency for the UC1842A and UC1843A. Output frequency is one half oscillator frequency for the UC1844A and UC1845A.

7. "Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation:

$$\text{Temp Stability} = \frac{V_{REF}\,(\text{max.}) - V_{REF}\,(\text{min.})}{T_J\,(\text{max.}) - T_J\,(\text{min.})}$$

V_{REF} (max.) & V_{REF} (min.) are the maximum & minimum reference voltage measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature."

BLOCK DIAGRAM



* - V_{CC} and V_C are internally connected for 8 pin packages.
** - POWER GROUND and GROUND are internally connected for 8 pin packages.
*** - Toggle flip flop used only in x844A and x845A series.

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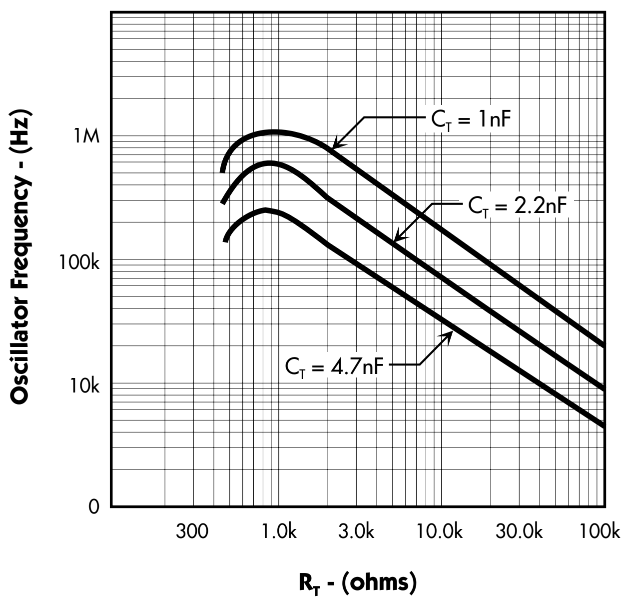
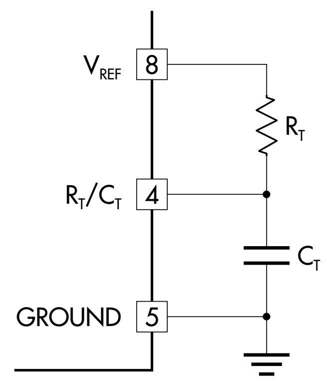
CHARACTERISTIC CURVES

FIGURE 1. — OSCILLATOR FREQUENCY vs. TIMING RESISTOR

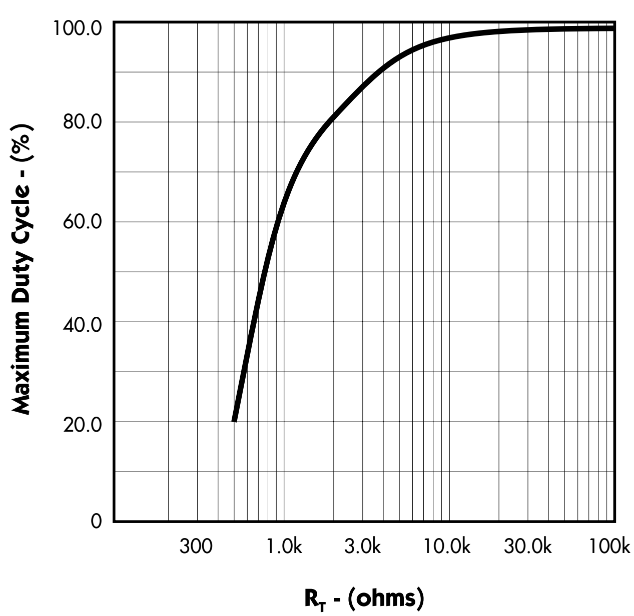




For R_T > 5k, f $\frac{1.72}{R_T\ C_T}$

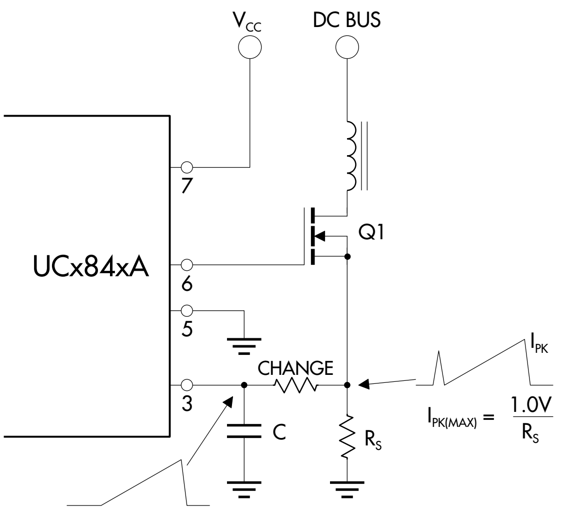
Note: Output drive frequency is half the oscillator frequency for the UCx844A/5A devices.

FIGURE 2. — MAXIMUM DUTY CYCLE vs. TIMING RESISTOR



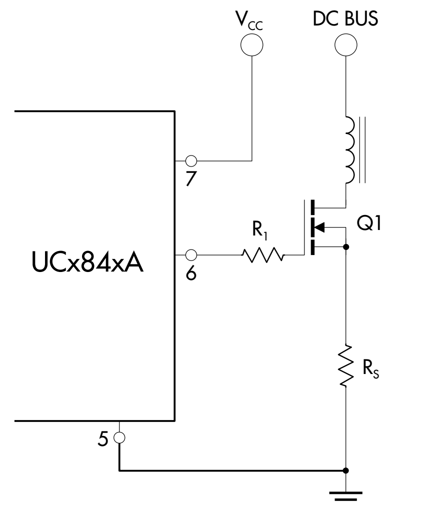
TYPICAL APPLICATION CIRCUITS

FIGURE 3. — CURRENT SENSE SPIKE SUPPRESSION



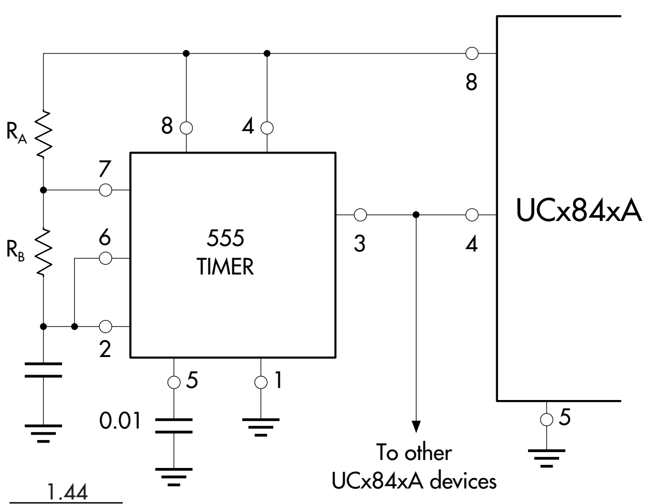
The RC low pass filter will eliminate the leading edge current spike caused by parasitics of Power MOSFET.

FIGURE 4. — MOSFET PARASITIC OSCILLATIONS



A resistor (R_1) in series with the MOSFET gate will reduce overshoot & ringing caused by the MOSFET input capacitance and any inductance in series with the gate drive. (Note: It is very important to have a low inductance ground path to insure correct operation of the I.C. This can be done by making the ground paths as short and as wide as possible.)

FIGURE 5. — EXTERNAL DUTY CYCLE CLAMP AND MULTI-UNIT SYNCHRONIZATION



$$f = \frac{1.44}{(R_A + 2R_B)C}$$

$$f = \frac{R_B}{R_A + 2R_B}$$

Precision duty cycle limiting as well as synchronizing several parts is possible with the above circuitry.

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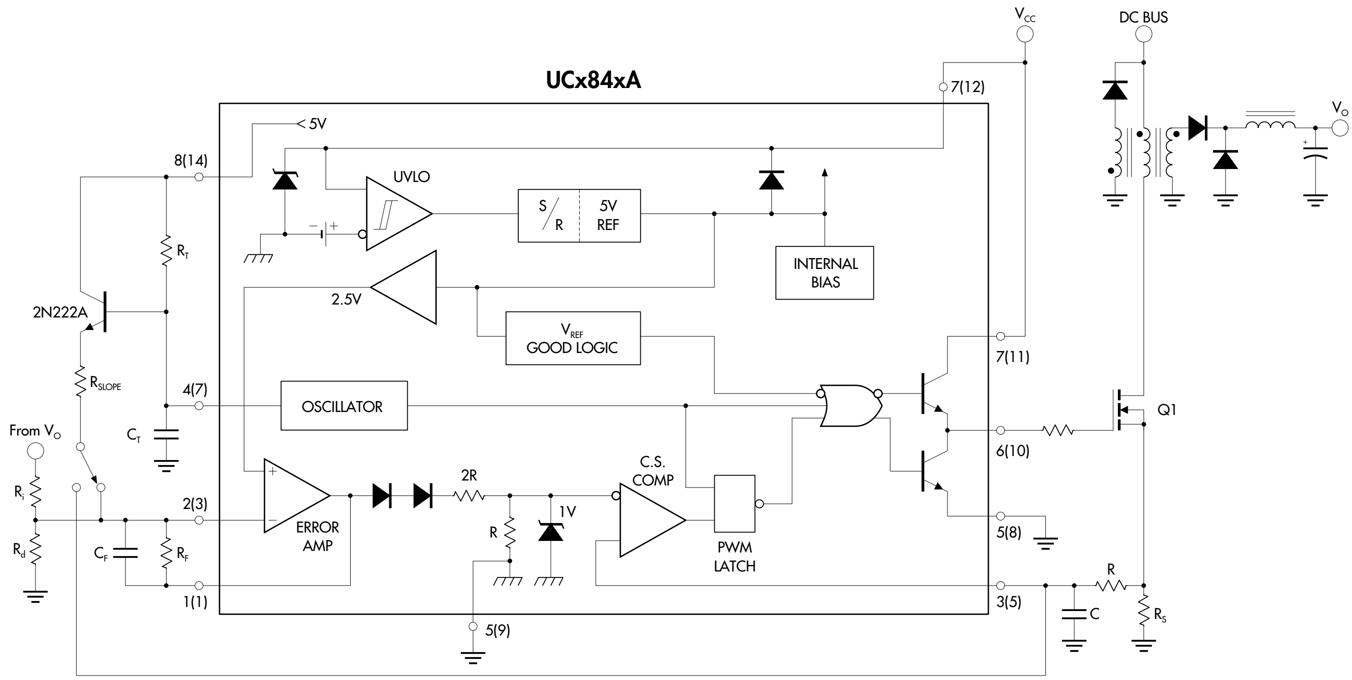
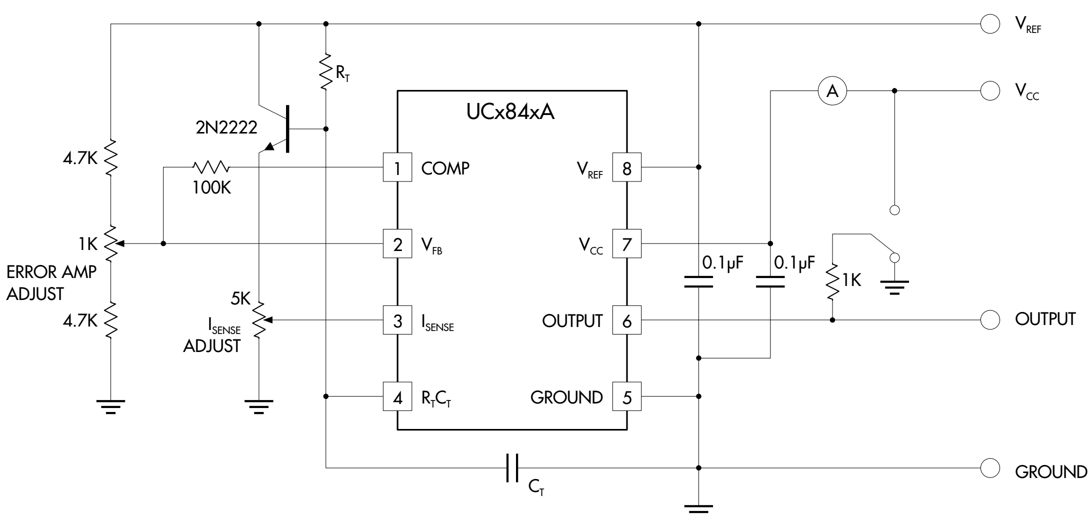
TYPICAL APPLICATION CIRCUITS (continued)

FIGURE 6. — SLOPE COMPENSATION



Due to inherent instability of current mode converters running above 50% duty cycle, slope compensation should be added to either the current sense pin or the error amplifier. Figure 6 shows a typical slope compensation technique.

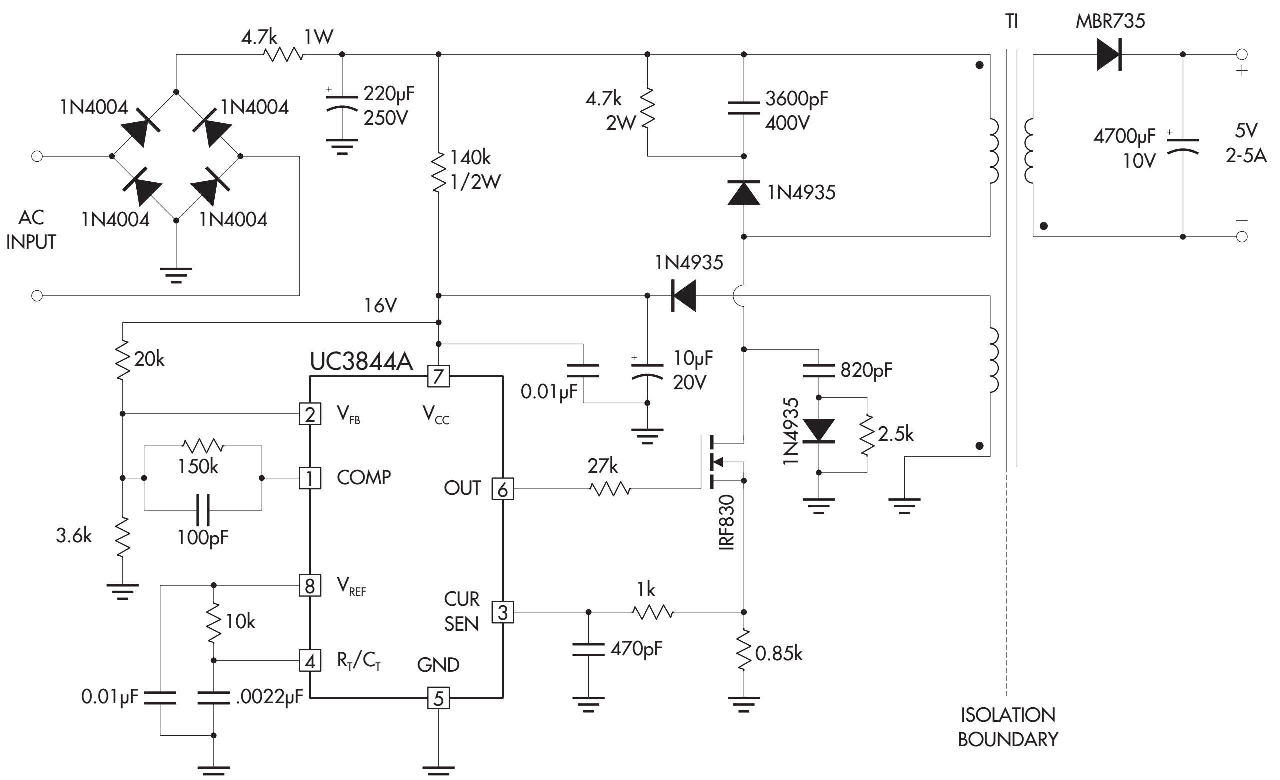
FIGURE 7. — OPEN LOOP LABORATORY FIXTURE



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected to pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

TYPICAL APPLICATION CIRCUITS (continued)

FIGURE 8. — OFF-LINE FLYBACK REGULATOR



SPECIFICATIONS

Input line voltage:	90VAC to 130VAC
Input frequency:	50 or 60Hz
Switching frequency:	40KHz ±10%
Output power:	25W maximum
Output voltage:	5V +5%
Output current:	2 to 5A
Line regulation:	0.01%/V
Load regulation:	8%/A*
Efficiency @ 25 Watts,	
V_{IN} = 90VAC:	70%
V_{IN} = 130VAC:	65%
Output short-circuit current:	2.5Amp average

* This circuit uses a low-cost feedback scheme in which the DC voltage developed from the primary-side control winding is sensed by the UC3844A error amplifier. Load regulation is therefore dependent on the coupling between secondary and control windings, and on transformer leakage inductance.