CENTELLAX

DC to 50 GHz MMIC Low Power
Voltage Controlled Attenuator

Description

The UVD50SC is a low-power high-attenuation DC-50 GHz PHEMT FET attenuator. The performance of the device is controlled by two bias voltages, V_{series} and V_{shunt}. The bias voltages control the match and attenuation of the device when varied between -1V and +0.5V DC. Please refer to the tables of recommended bias settings optimized for flat insertion loss and flat attenuation for additional information.

Features

• Wideband operation: DC to 50 GHz
• Low Insertion Loss (<5 dB)
• Good Input/Output Match
• High Attenuation (max. 27 dB)
• Very flat Attenuation
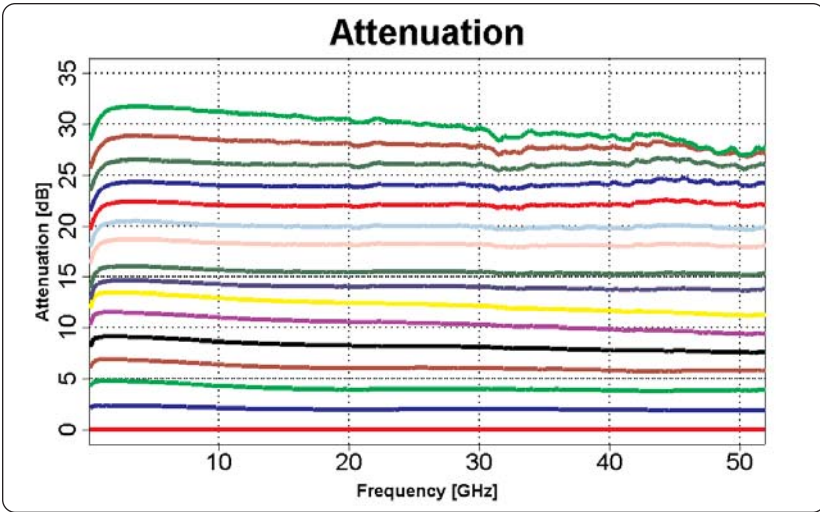• Size: 1640 x 920 µm

Application

The UVD50SC MMIC voltage controlled attenuator is ideal for high frequency and broadband applications in test equipment, commercial and military systems. The attenuator is especially suited for applications needing a large amount of adjustable attenuation and fast attenuation control from DC to millimeter frequencies. The device is also useful as a general purpose building block in communications systems.

Key Specifications

Zo=50 W

Parameter	Description	Minimum	Typical	Maximum
Attenuation (dB)	DC to 50 GHz	0	—	27
Flatness (±dB)	DC to 50 GHz	—	1.0	—
Insertion Loss (dB)	DC to 50 GHz	5	—	35
S11 (dB)	DC to 50 GHz	—	-12	-10
S22 (dB)	DC to 50 GHz	—	-12	-10
P_{-1dB} (dBm)	1dB Gain Compression 0 to 15dB Attenuation	—	6	—

Optimized for Flat Attenuation (Typical)

V_{series}(V)	V_{shunt}(V)	Att. (dB)*
-0.637	0.500	30
-0.600	0.500	28
-0.575	0.062	26
-0.555	-0.142	24
-0.539	-0.252	22
-0.527	-0.334	20
-0.509	-0.375	18
-0.478	-0.425	15.5
-0.463	-0.450	14
-0.512	-0.506	12
-0.505	-0.534	10
-0.450	-0.550	8
-0.288	-0.562	6
0.250	-0.588	4
-0.250	-0.650	2
0.500	-1.000	0

Figure 1: Typical on wafer measured performance.

Optimized for Flat Insertion Loss (Typical)

V_{series}(V)	V_{shunt}(V)	Loss (dB)*
-0.688	0.500	35.5
-0.637	0.500	33.5
-0.600	0.450	31.6
-0.600	-0.150	29.8
-0.584	-0.255	27.7
-0.567	-0.315	25.7
-0.553	-0.364	23.7
-0.541	-0.408	21.7
-0.530	-0.446	19.7
-0.550	-0.500	17.6
-0.512	-0.506	15.7
-0.503	-0.539	13.7
-0.450	-0.550	11.8
-0.250	-0.562	9.6
-0.025	-0.592	7.6
0.387	-0.638	5.6
0.500	-1.000	3.6

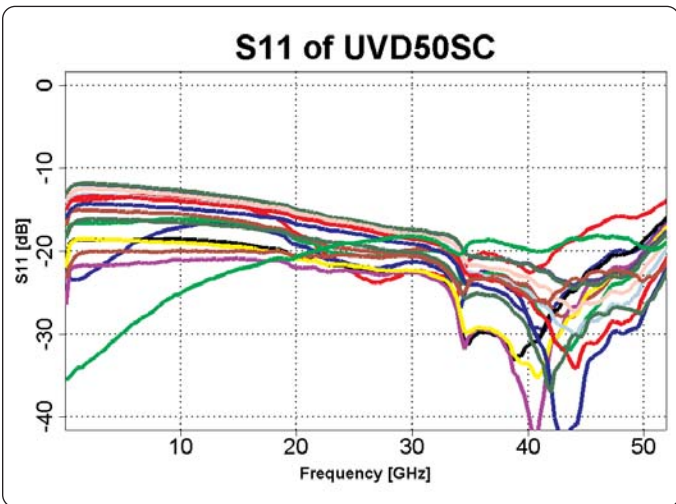**Figure 2:** Typical on wafer measured performance.

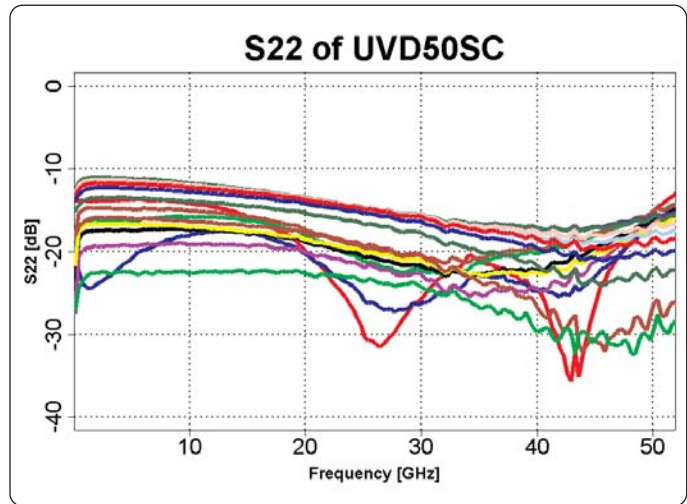**Figure 3:** Typical on wafer measured performance.

Figure 4: Typical on wafer measured performance.

Note: (*) Midband

Supplemental Specifications

Parameter	Description	Minimum	Typical	Maximum
V_{series}	Attenuation Control Voltage	-2 V	—	0.5 V
V_{shunt}	Attenuation Control Voltage	-2 V	—	0.5 V
DC_{in}	DC feedback circuit input	0 V	0.2 V	1 V
DC_{out}	DC feedback circuit output	0 V	0.2 V	1 V
GND	Backside Ground Plane			
Tch	Channel Temperature	—	—	150°C
Qch	Thermal Resistance (T_{case}=25°C)	—	60°C/Watt	—

Pick up and Chip Handling:

The chip has exposed air bridges on the top surface. Do not pick up chip with vacuum on the die center; handle at edges or with a custom collet.

ESD Handling and Bonding:

This MMIC is ESD sensitive and preventive measures should be taken during handling, die attach and bonding.

Epoxy die attach is recommended.

Please visit our website for more handling, die attach and bonding information.
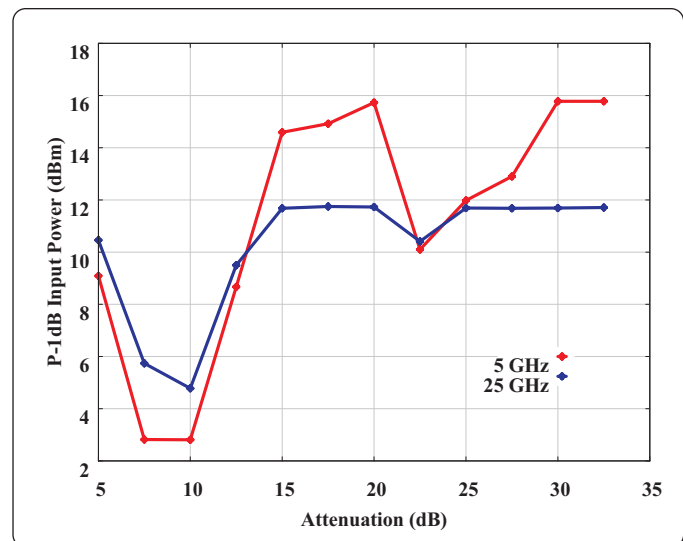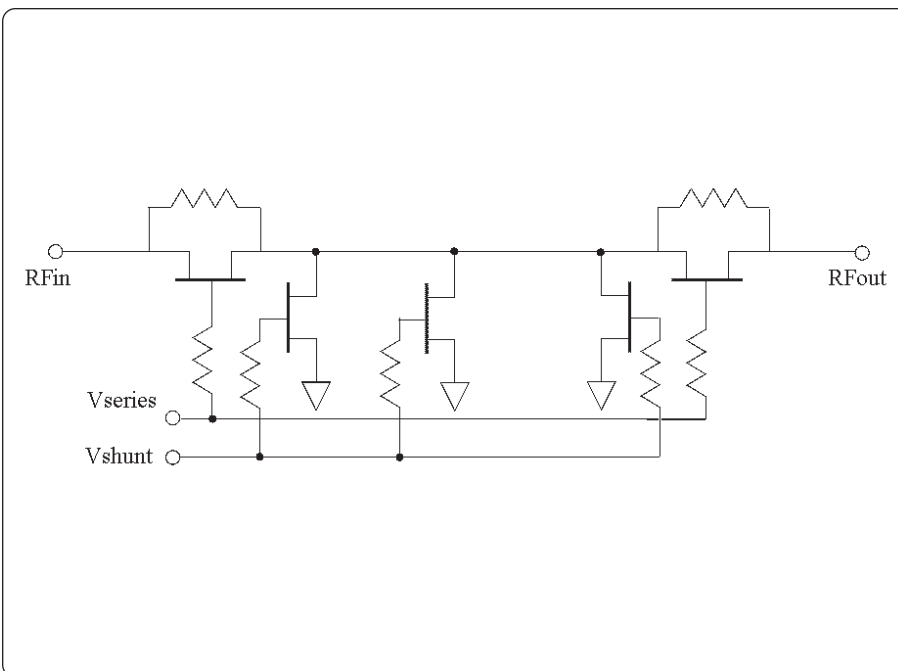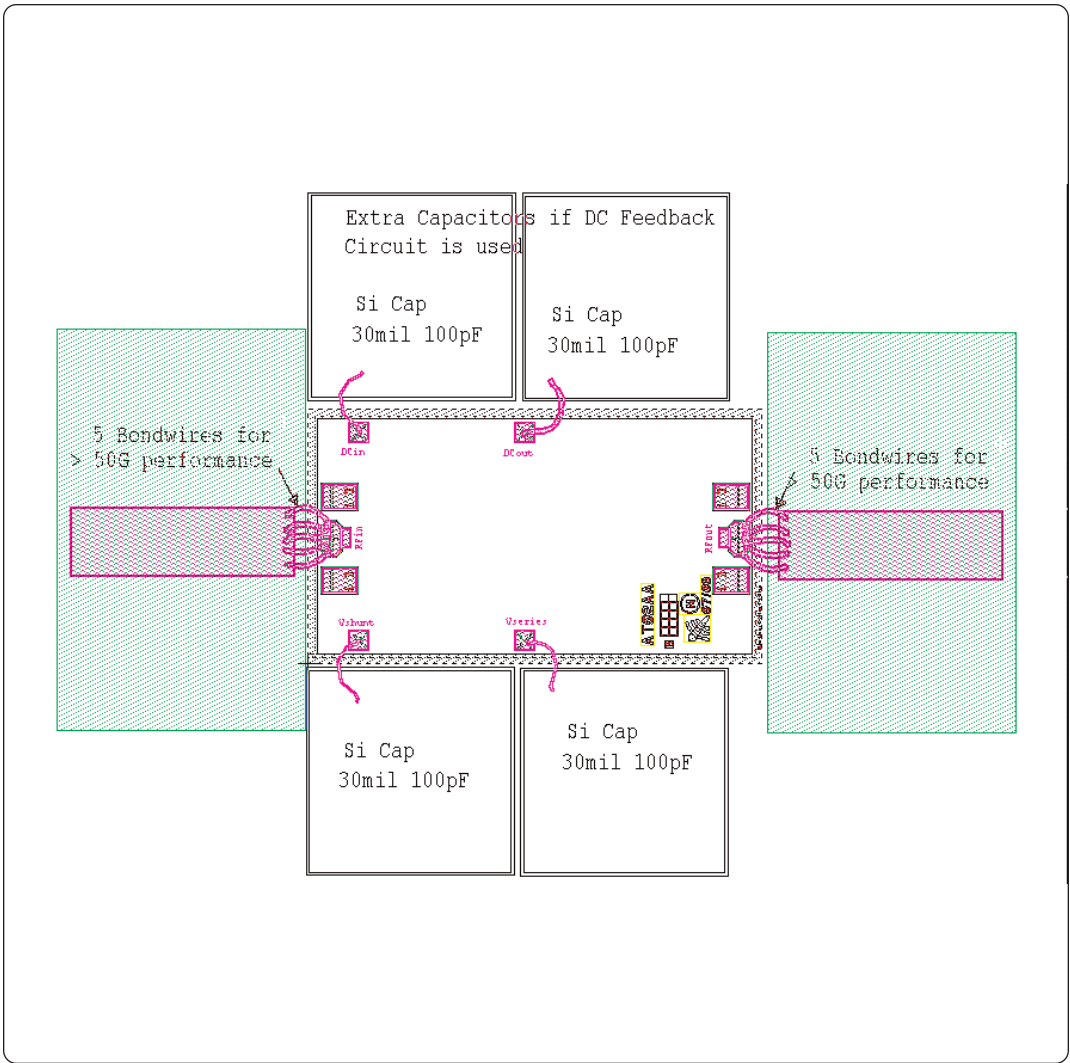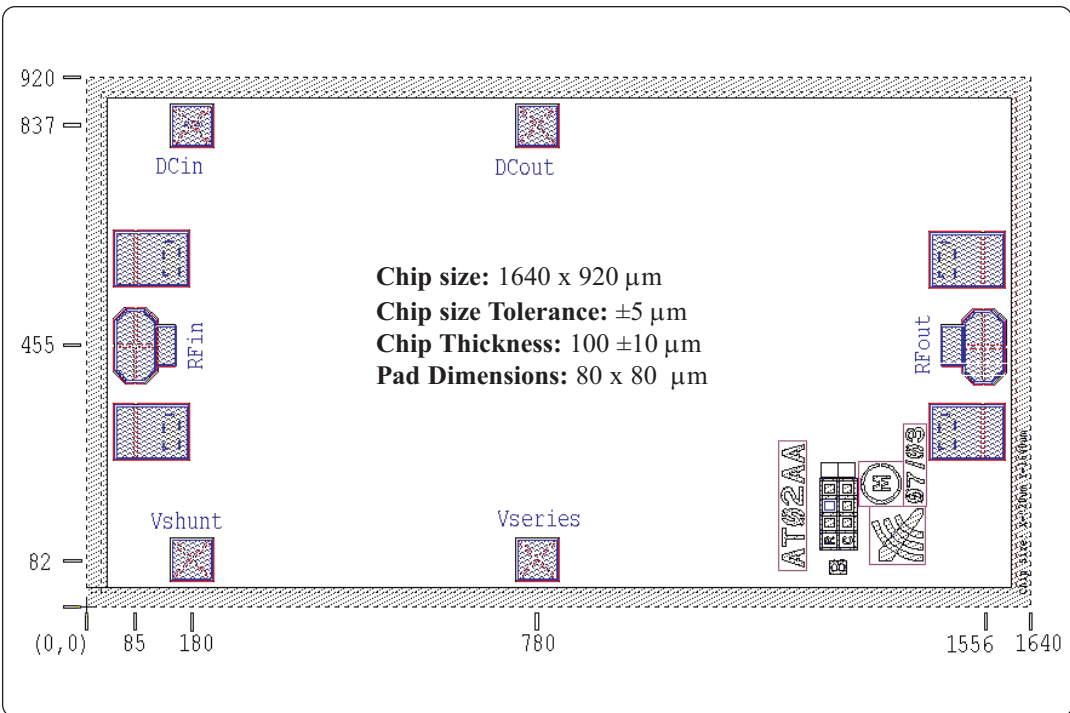
(www.centellax.com)

Figure 5: Typical on evaluated package measured performance.

UVD50SC Simplified Schematic Diagram

Assembly Diagram of
UVD50SC

Chip size: 1640 x 920 µm
Chip size Tolerance: ±5 µm
Chip Thickness: 100 ±10 µm
Pad Dimensions: 80 x 80 µm

Physical
Characteristics of
UVD50SC

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