# UXN40M7K

# Datasheet

# 40 GHz Divide-by-1-to-127 Programmable Integer Divider

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Power Matters.™

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# 1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## 1.1 Revision 1.0

Revision 1.0 was published in February 2017. It was the first publication of this document.

## 1.2 Revision 2.0

Revision 2.0 was published in April 2020. The Electrical Characteristics table was updated.

# Contents

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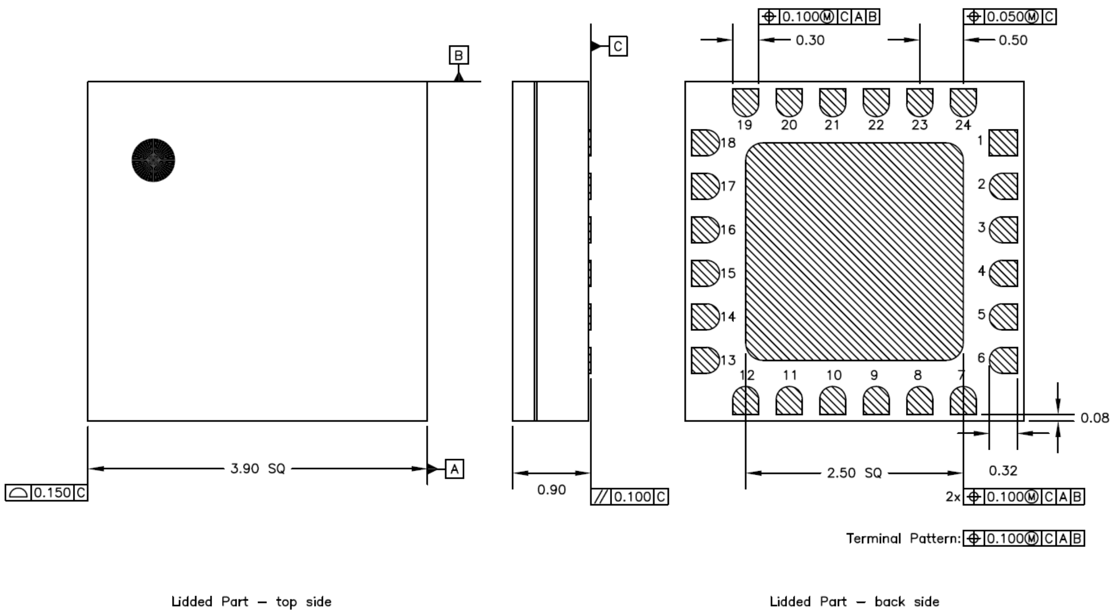
# 2 Product Overview

The UXN40M7K is a highly programmable integer divider covering all integer divide ratios between 1 and 127. The device features single-ended or differential inputs and outputs. Parallel control inputs are CMOS and LVTTL compatible for ease of system integration. The UXN40M7K is packaged in a 24-pin, 4 mm × 4 mm leadless ceramic surface mount package, shown in the following figure (dimensions are in millimeters).

**Figure 1 UXN40M7K Package Outline**




## 2.1 Applications

The UXN40M7K can be used as a general purpose, highly configurable divider in a variety of high-frequency synthesizer applications. Fast switching combined with a wide range of divide ratios make the UXN40M7K an excellent choice for fractional-N and integer-N phase-locked loops. Fractional division may be achieved by applying a sequence to the divider control lines, such as a delta-sigma modulated sequence.

## 2.2 Key Features

The following are the key features of the UXN40M7K device:

- Wide operating range: 0.5 GHz–40 GHz
- Contiguous divide ratios: 1 to 127
- Large output swings: >600 mVpp/side
- Single-ended and/or differential drive
- Small size: 4 mm × 4 mm
- Parallel control lines
- Low SSB phase noise: –153 dBc at 10 kHz offset

# 3 Electrical Specifications

This section details the electrical specifications of the UXN40M7K device.

## 3.1 Electrical Characteristics

The following table shows the electrical characteristics of the UXN40M7K device at 25 °C, where $V_{CC}$ = 3.3 V, $I_{CC}$ = 230 mA, and $Z_O$ = 50 Ω.

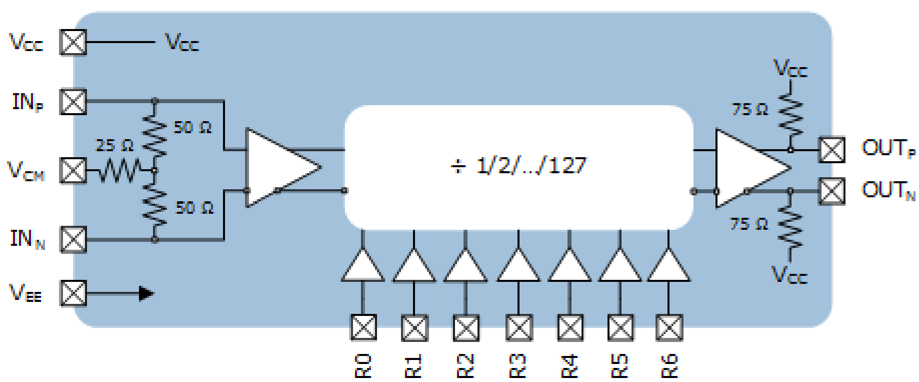
**Table 1 Electrical Characteristics**

| Parameter | Description | Min | Typ | Max |
|---|---|---|---|---|
| $F_{IN}$ (GHz) | Input frequency | 0.5 | | 50 |
| $P_{IN}$ (dBm) | Input power | | 0 | 10 |
| $P_{OUT}$ (dBm) | Output power | | 2.00 | |
| $P_{DC}$ (W) | DC power dissipation | | 0.75 | |
| $\theta_{JC}$ (°C/W) | Junction-case thermal resistance | | 26 | |

## 3.2 Functional Block Diagram

The following drawing shows the functional blocks of the UXN40M7K device.

**Figure 2 Functional Block Diagram**




## 3.3 Pin Descriptions

The following table shows the pin descriptions of the UXN40M7K device.

**Table 2 Pin Descriptions**

| Pin Name | Description | Notes |
|---|---|---|
| $IN_P$[1] | Divider input, positive terminal | CML signal levels |
| $IN_N$[1] | Divider input, negative terminal | CML signal levels |
| $OUT_P$ | Divider output, positive terminal | CML signal levels |
| $OUT_N$ | Divider output, positive terminal | CML signal levels |

| Pin Name | Description | Notes |
|---|---|---|
| R0–R6 | Divider modulus control (R6 = MSB) | CMOS levels default to logic 0 |
| $V_{CC}$ | 3.3 V at 230 mA | Positive supply voltage |
| $V_{EE}$ | RC and DC ground | The paddle is floating |
| $V_{CM}$[1] | Common mode input | |

1. $IN_P$, $IN_N$, and $V_{CM}$ require coupling capacitors at the inputs, with $V_{CM}$'s capacitor going to ground.

Use the following equation to find the divider modulus, where setting all bits to 0 results in N = 1.

$$\text{Divider Modulus} = N = P_0 \cdot 2^0 + P_1 \cdot 2^1 + P_2 \cdot 2^2 + \ldots + P_6 \cdot 2^6 \text{ for } 1 \le N \le 127$$

## 3.4 CMOS Levels

The following table shows the CMOS levels for control lines R0-R8 of the UXN40M7K device.

**Table 3 CMOS Levels for Control Lines R0-R8**

| Logic Level | Minimum | Typical |
|---|---|---|
| Supply voltage ($V_{CC}$-$V_{EE}$) | 3.6 | V |
| RF input power ($IN_P$, $IN_N$) | 10 | dBm |
| Operating temperature | –40 to 85 | °C |
| Storage temperature | –85 to 125 | °C |
| Junction temperature | 125 | °C |

The following table shows the CMOS levels for control lines R0-R8 of the UXN40M7K device.

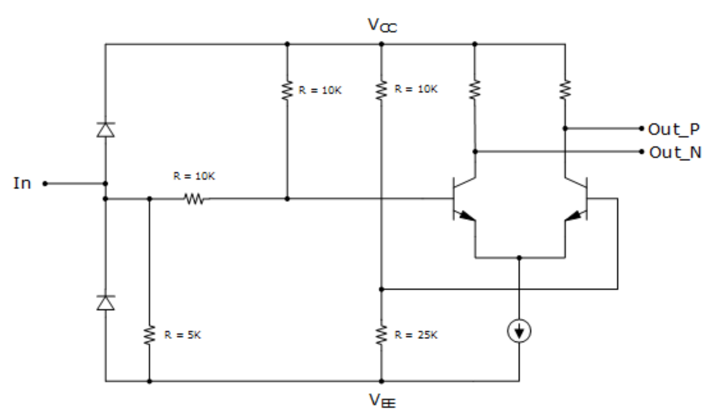
**Table 4 CMOS Levels for Control Lines R0-R8**

| Logic State ($P_i$) | Minimum | Typical | Maximum |
|---|---|---|---|
| 1 (high) | $V_{CC}$ – 1.3 V | $V_{CC}$ | $V_{CC}$ |
| 0 (low) | $V_{EE}$ | $V_{EE}$ | $V_{EE}$ + 0.8 V |

## 3.5 Simplified Control Logic Schematic

The following drawing shows the simplified control logic schematic of the UXN40M7K device.

**Figure 3 Simplified Control Logic Schematic**



## 3.6 Typical Performance Plots

This section details the typical performance plots of the UXN40M7K device.

**Figure 4 Min/Max Single-Ended Input Power Input Sensitivity Window**

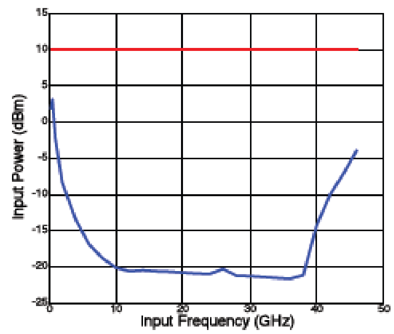



**Figure 5 Divide-by-8 Output Power, 3rd Harmonic, and Input Feed Through**

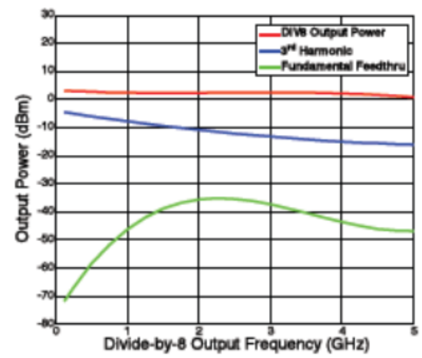



**Figure 6 Static Divide-by-80 Configuration**

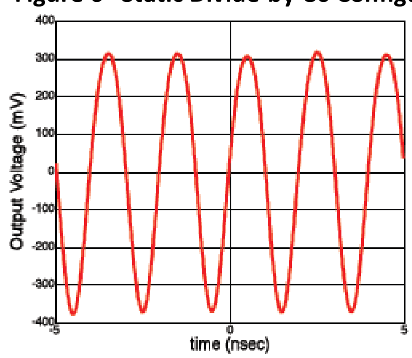



**Figure 7 Static Divide-by-127 Configuration**

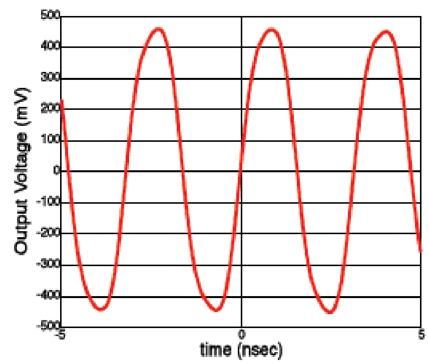



**Figure 8 Output Amplitude vs. Frequency**

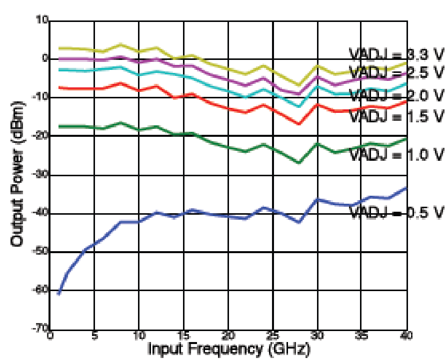



**Figure 9 Fundamental Feed Through**

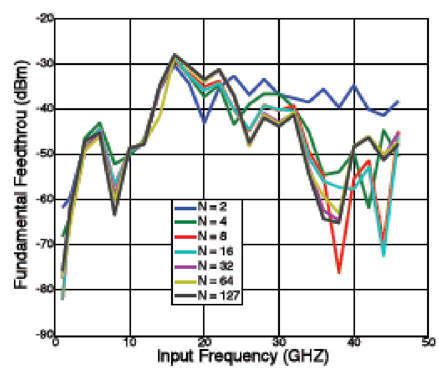


**Figure 10 Sensitivity Window vs. Supply Voltage**

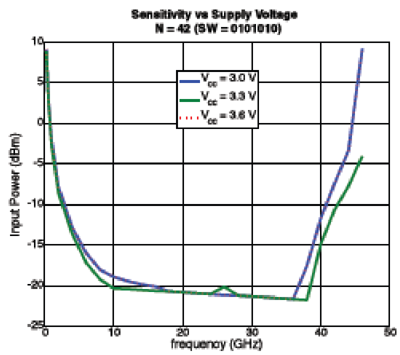



**Figure 11 Sensitivity Window vs. Temperature**

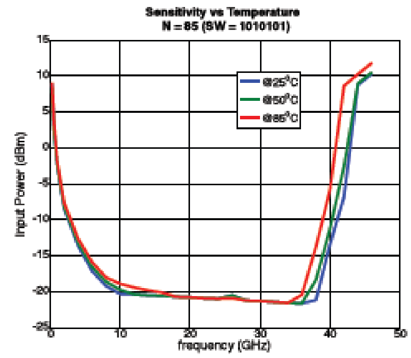



**Figure 12 S-Parameters S11**

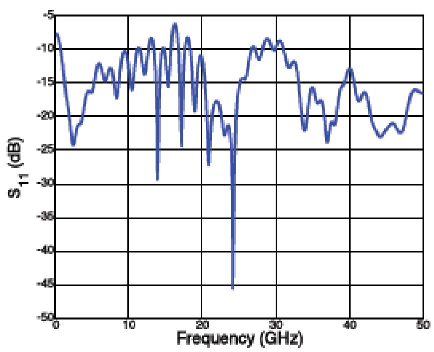



**Figure 13 S-Parameters S12**

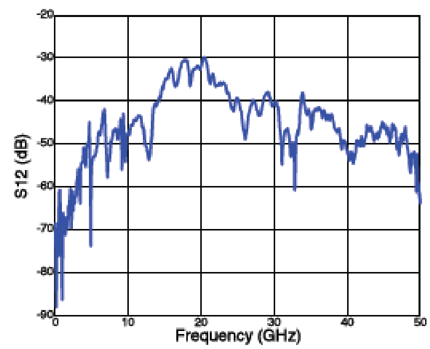



**Figure 14 S-Parameters S21**

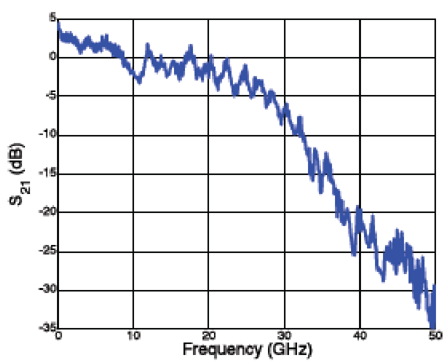
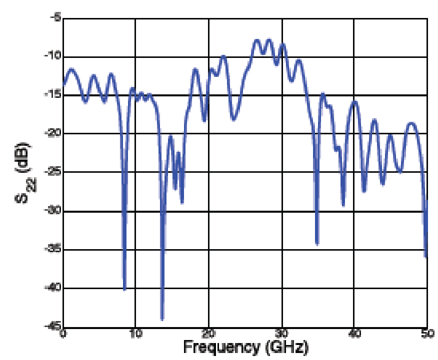



**Figure 15 S-Parameters S22**



# 4 Pin Definition and Package Outline

The UXN40M7K is packaged in a 24-pin, 4 mm × 4 mm leadless ceramic surface mount package.

## 4.1 Pin Definition

The following table shows the pin definitions for the UXN40M7K device.

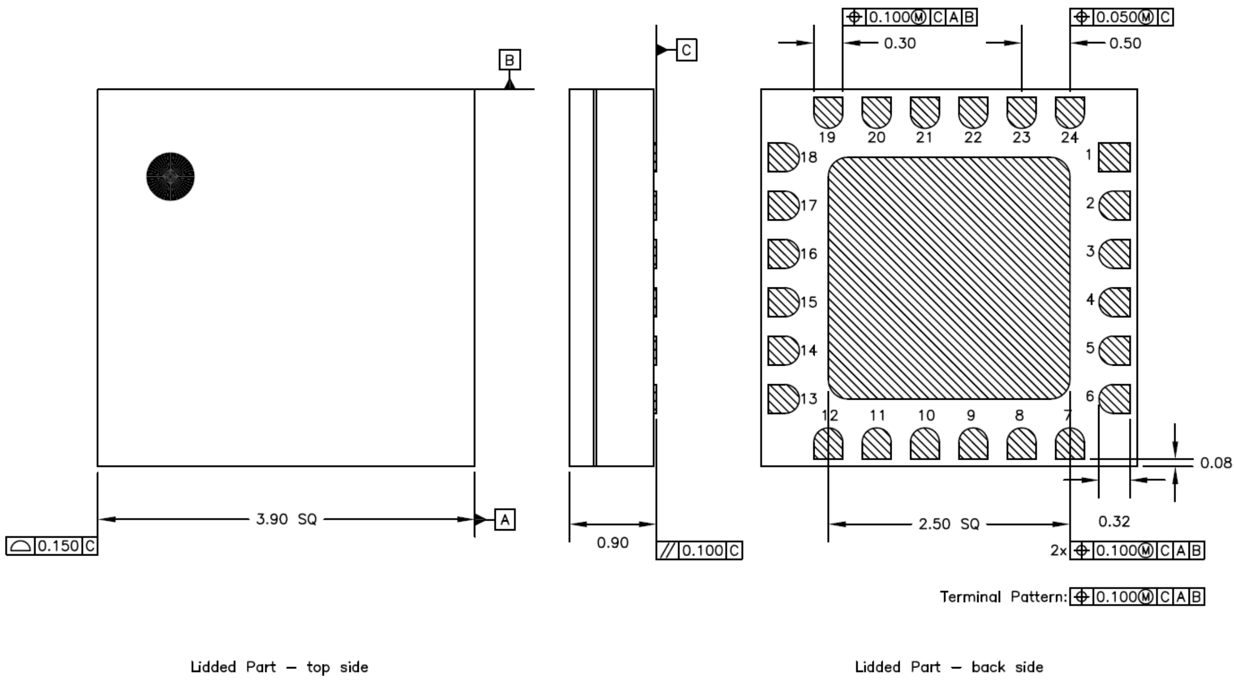
**Table 5 Pin Definitions**

| Pin | Function | Notes |
|---|---|---|
| 1 (R1) | Divide modulus control | Defaults to logic 0, connect to $V_{CC}$ for logic 1 |
| 2 (R0) | Divide modulus control (LSB) | Defaults to logic 0, connect to $V_{CC}$ for logic 1 |
| 3, 8, 9, 12, 17 (VEE) | RF and DC ground | 0 V |
| 4 (INP) | Divider input | Positive terminal of differential input |
| 5 (INN) | Divider input | Negative terminal of differential input |
| 6 (VCM) | Common mode input | Refer to functional block diagram |
| 7, 10, 11, 13, 16, 19 (VCC) | Positive supply voltage | Nominally +3.3 V |
| 14 (OUTP) | Divider output | Positive terminal of differential output |
| 15 (OUTN) | Divider output | Negative terminal of differential output |
| 18 (VADJ) | Output amplitude control | Tie to VCC for maximum swing |
| 20 (R6) | Divide modulus control (MSB) | Defaults to logic 0, connect to $V_{CC}$ for logic 1 |
| 21 (R5) | Divide modulus control | Defaults to logic 0, connect to $V_{CC}$ for logic 1 |
| 22 (R4) | Divide modulus control | Defaults to logic 0, connect to $V_{CC}$ for logic 1 |
| 23 (R3) | Divide modulus control | Defaults to logic 0, connect to $V_{CC}$ for logic 1 |
| 24 (R2) | Divide modulus control | Defaults to logic 0, connect to $V_{CC}$ for logic 1 |
| Paddle | Package paddle | Tie to heat sink |

## 4.2 Package Outline

The following drawing shows the physical characteristics of the UXN40M7K device.

**Figure 16 Package Outline**



# 5 Application Notes

## 5.1 Low-Frequency Operation

Low-frequency operation is limited by external coupling capacitors and the slew rate of the input clock. The next paragraph shows the calculations for the capacitors. Sine-wave inputs are limited to roughly 500 MHz.

The values of the coupling capacitors for the high-speed inputs and outputs (I/Os) are determined by the lowest IC operation frequency.

$$C \gg \frac{1}{2 \cdot \pi \cdot 50\,\Omega \cdot f_{lowest}}$$

For example, to use the device below 1 GHz, coupling capacitors should be larger than 3 pF.

## 5.2 IC Assembly

The device is designed to operate with either single-ended or differential inputs. The supply should be capacitively bypassed to ground to provide a good AC ground over the frequency range of interest. RF I/Os should be AC-coupled through the series capacitors. The backside of the chip should be connected to a good thermal heat sink.

## 5.3 ESD Sensitivity

Although SiGe ICs have robust ESD sensitivities, preventative ESD measures should be taken while storing, handling, and assembling.

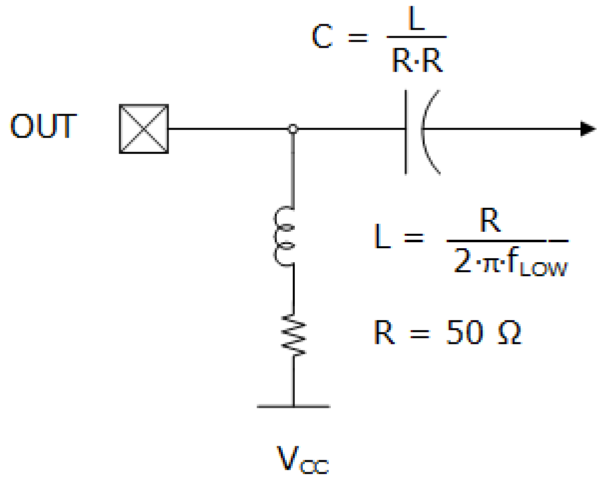
Inputs are more ESD susceptible because they could expose the base of a BJT. All control inputs are protected with ESD diodes. These inputs should withstand voltage spikes up to 400 V.

## 5.4 Differential vs. Single-Ended

The UXN40M7K is fully differential to maximize signal-to-noise ratios for high-speed operation. The high-speed outputs are terminated to $V_{CC}$ with on-chip 75 Ω resistors. The maximum DC voltage on either of the output terminals must be limited to $V_{CC}$ ± 1 V to prevent damaging the termination resistors with excessive current.

The outputs require a DC return path capable of handling approximately 24 mA per side with $V_{ADJ}$ set to $V_{CC}$. With AC coupling on the output, a bias tee circuit (for example, see Figure 17) is recommended for the fastest operation with maximum swing. The value of the capacitor should be large enough to pass the lowest frequencies of interest. The discrete R/L/C elements should be resonance free up to the maximum frequency of operation for broadband applications.

**Figure 17 Bias Tee Circuit**



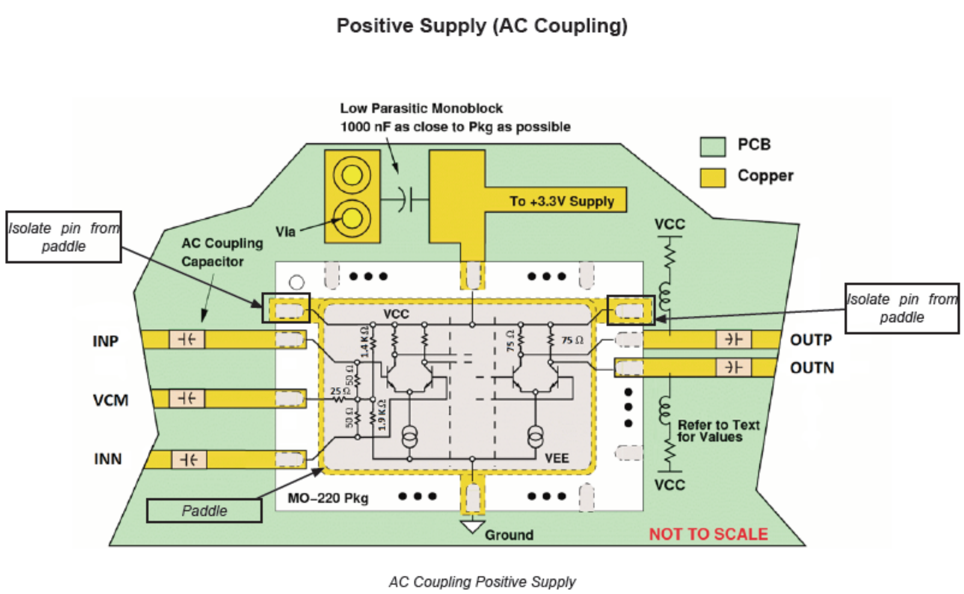

The high-speed inputs are terminated to an internal reference voltage ($V_{REF}$) set by a resistive divider between $V_{CC}$ and $V_{EE}$. For $V_{CC}$ = 3.3. V and $V_{EE}$ tied to ground, the nominal value of $V_{REF}$ is 1.9 V, and equivalent impedance from $V_{REF}$ is approximately 800 Ω. It is recommended that DC voltage on any of the input terminals be maintained between a minimum of $V_{EE}$ – 1 V and a maximum of $V_{CC}$ + 1 V.

**Note:** A potential oscillation mechanism exists if both inputs are static and have identical DC voltages—a small DC offset on either input is sufficient to prevent possible oscillations. Connecting a 10k Ω resistor between the unused input and $V_{EE}$ should provide sufficient offset to prevent oscillation.

The UXN40M7K device can also be used in single-ended applications. All unused ports should be terminated with the same loading as the ports being used.

The following diagram shows AC coupling with a positive supply.

**Figure 18 Positive Supply (AC Coupling)**



## 5.5 Duty Cycle

The UXN40M7K output duty cycle varies between 33% and 66% as a function of the divide ratio, N. When N is a power of 2, the duty cycle is exactly 50%. As N deviates from a power of 2, so too does the duty cycle deviate from 50%. For example, N = 64 has 50% duty cycle, N = 60 has 47% duty cycle, and N = 56 has 43% duty cycle.

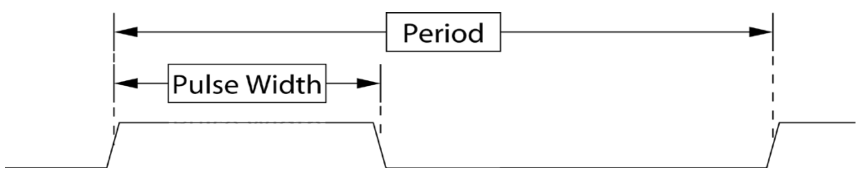
The following equations calculate pulse width and duty cycle as a function of N, for any integer N from 2 to 127.

$$Pulse\ width\ (input\ cycles) = \mathrm{N} - 2^{\mathrm{floor}\left[\log 2\left(\frac{\mathrm{N}}{3}\right)+1\right]}$$

$$Duty\ cycle\ (1\%) = \frac{Pulse\ width}{Divide\ ratio} \times 100\%$$

The following illustration shows the period–pulse width relationship for the UXN40M7K device.

**Figure 19 Period–Pulse Width Relationship**



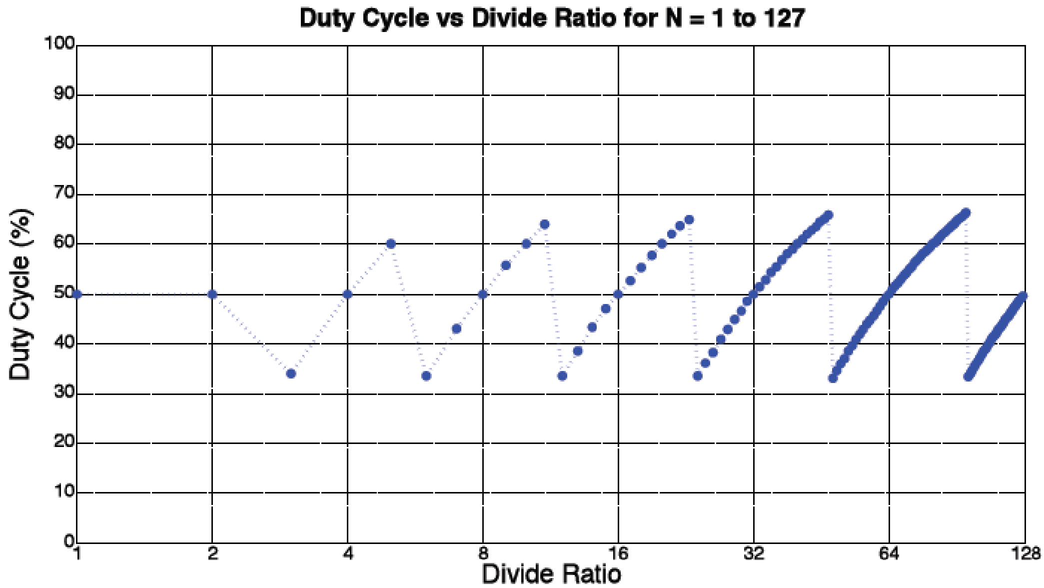

The following table shows the pulse width and duty cycle for N from 2 to 16 for the UXN40M7K device.

**Table 6 Duty Cycle Summary**

| Divide Ratio | Pulse Width (Input Cycles) | Duty Cycle (%) |
|---|---|---|
| 2 | 1 | 50 |
| 3 | 1 | 33 |
| 4 | 2 | 50 |
| 5 | 3 | 60 |
| 6 | 2 | 33 |
| 7 | 3 | 43 |
| 8 | 4 | 50 |
| 9 | 5 | 55 |
| 10 | 6 | 60 |
| 11 | 7 | 63 |
| 12 | 4 | 33 |
| 13 | 5 | 38 |
| 14 | 6 | 43 |
| 15 | 7 | 47 |
| 16 | 8 | 50 |

The following graph shows the duty cycle versus divide ratio for N = 1 to 127 for the UXN40M7K device.

**Figure 20 Duty Cycle vs. Divide Ratio**



# 6 Ordering Information

The following table shows the ordering information for the UXN40M7K device.

**Table 7 Ordering Information**

| Part Number | Package |
|---|---|
| UXN40M7K | 24-pin ceramic leadless surface mount package |