ZL70251 Ultra-Low-Power Sub-GHz RF Transceiver

Features

- Ultralow Power
  - Typical TX Current (with 50-Ω match): <2.4mA at −11dBm; <5.5mA at 0dBm
  - Typical RX Current: <2.3mA
  - Sleep Current: <500nA typical
  - Supply: 1.2V to 1.9V
- Operating Frequency Range: 779MHz to 965MHz
  - North American ISM Band: 902MHz to 928MHz
  - European SRD Band: 863MHz to 870MHz
  - Chinese Band: 779MHz to 787MHz
- Key Performance Parameters
  - Raw Data Rate: 136.5kbit/s or 186kbit/s
  - TX Power: up to 0dBm
  - RX Sensitivity: −94dBm Typical at 186kbit/s
- Very Few External Components
  - Only Crystal, Decoupling Capacitors, and Bias Resistor
- Standard Interfaces
  - SPI Bus Master for Packet Data
  - Two-Wire for Status and Control
- MAC
  - Clear Channel Assessment
  - Automatic Receive or Sleep after Sniff
  - Automatic Turn-Around in Bidirectional Mode
  - Packetization
  - Preamble and Frame Sync
  - Whitening
  - Receive on Preamble Detection or RSSI Threshold
- RoHS Compliant

Applications

- Body-Area Network
- Energy Harvesting
- Wireless Sensor Network
- Remote Control
- Voice/Compressed-Audio Communication
- RF Switch
- Active RFID
- Inventory Management

Description

The ZL70251 ultra-low-power RF transceiver provides a wireless link in applications where power consumption is of primary importance. The transceiver's ultralow power requirements allow the use of a coin-cell battery or energy-harvesting sources, enabling devices with extremely small form factors.

The ultra-low-power device operates in unlicensed frequency bands between 779MHz and 965MHz with a data rate of 136.5kbit/s or 186kbit/s. Duty cycling can be employed for applications that require lower average payload to further reduce power consumption.

Ordering Information

ZL70251UEB2	36-Pin CSP, SAC405, in T&R

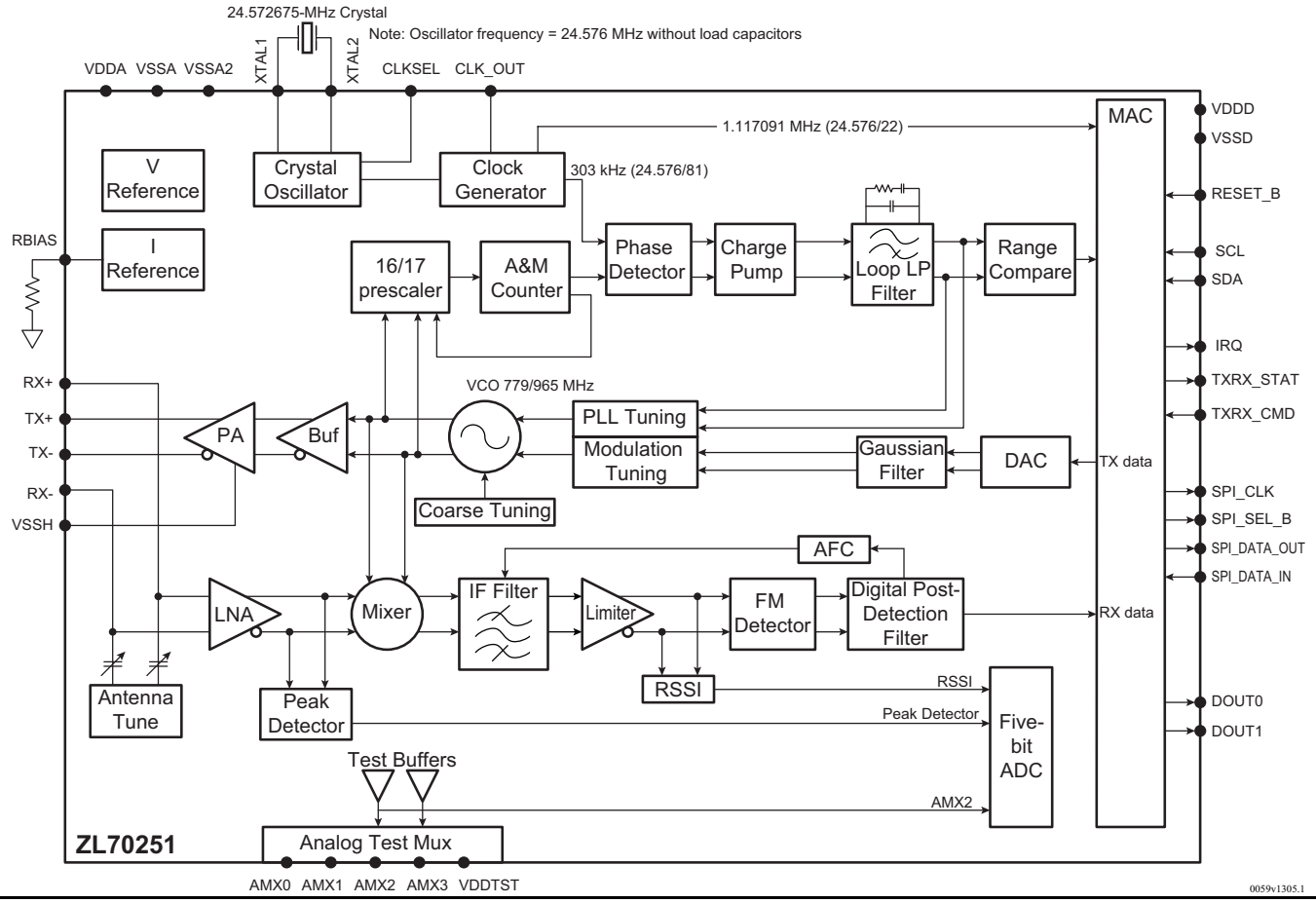


Figure 1 • **ZL70251 Block Diagram (configured for 300-kHz channel width)**

Table of Contents

List of Figures

List of Tables

1 – Overview

The ultra-low-power ZL70251 RF transceiver enables RF telemetry in applications powered by coin-cell batteries or energy harvesting, where wireless telemetry was previously unfeasible. End applications may include wireless sensors, body-area networks (principally on-body sensors), or voice communication.

With a typical peak/average current consumption below 2.4 mA in both transmit and receive, and with an upper data rate of 186 kbit/s, the ZL70251 enables bidirectional RF links over a distance of more than 100 meters (based on antenna gain and matching loss).

The output power is programmable and can be reduced to −25 dBm to save power in cases where the link budget allows it, or can be increased up to 0 dBm for more range or to allow for system losses such as a very small antenna or body tissue absorption.

To achieve the minimum possible power consumption, the ZL70251 offers many optimization parameters, all available to the user via the control interface. To streamline the setup and optimization process, most parameters have an on-chip automatic trim capability. The frequency tuning is also highly automated.

In addition to its ultra-low power consumption, the ZL70251 also includes a highly flexible Media Access Controller (MAC) that offers some basic functions. Some of the capabilities are:

- Clear channel assessment
- Transmit with automatic clear-to-send
- Sniff with automatic receive or sleep
- Preamble and frame sync generation and detection
- Whitening
- Packetization with programmable size for both transmit and receive
- Automatic sleep after receive
- Automatic turnaround for bidirectional data transfer

The ZL70251 is an ultra-low-power RF transceiver operating in unlicensed frequency bands between 779 and 965 MHz. It offers a data rate of 186 kbit/s in 300-kHz-wide channels or 136.5 kbit/s in 200-kHz-wide channels.

The ZL70251 includes a frequency synthesizer, RF transmitter and receiver (shown in Figure 1 on page I), and a MAC for performing bit and frame synchronization, transmit and receive control, and other digital functions.

The ZL70251 transceiver transmits and receives GFSK-modulated digital data over a 300- or 200-kHz-wide channel.

Registers control selective shutdown of the device in order to conserve power. The device does not contain any timing circuits necessary for periodic wake-up and channel sniffing; this is left to the system host.

The system host initiates a Clear Channel Assessment (CCA) at a high level. CCA consists of the RSSI level for the currently programmed receiver channel. CCA of other channels requires the host to set the receiver for those channels one at a time and to request and read the RSSI registers.

The ZL70251 is configurable for operation with minimal external components. In some applications the only necessary external components are an antenna, a crystal, decoupling capacitors, and a resistor (51.0 kΩ ±1%) to set the nominal bias current. The capacitors for antenna tuning and crystal oscillator trimming reside on the chip. The transmit power amplifier has a separate ground pin to isolate the PA from any interfering ground currents. Also, the PA is externally biased to allow the voltage at its end points to swing above the VDD supply.

In a typical application, the ZL70251 handles the transmission and reception of data packets via the SPI bus. For packet transmissions, the ZL70251 transmits preamble, frame sync, and data; and for reception, it performs automatic DC restore on preamble, detects a valid frame sync, and receives the data for the packet. The format of the data is user defined. The ZL70251 supports fixed- or variable-length packets. When fixed-length packets are required, the ZL70251 is programed for bit-count mode in which the user programs the length (in bits) of the data packet. In this mode, packets are terminated in transmit or receive when the programmed bit count has been reached. When variable length packets are required, the ZL70251 is programed for non-bit-count mode for which the ZL70251 terminates the packet in receive when the RF signal strength drops below the RSSI threshold or by raising the TXRX_CMD input.

2 – Functional Description

Control Interface

Functional Description

The control interface in the MAC is used to program the registers of the ZL70251 RF transceiver.

At the bit level the ZL70251 interface is a standard two-wire control interface with a maximum speed of 370kHz for a bit rate of 186kbit/s and 270kHz for a bit rate of 136.5kbit/s. The bit-level protocol is shown in "Bit-Level Protocol" below.

The ZL70251 control interface differs slightly from the standard two-wire protocol at the byte sequencing level due to the addition of some extra functionality as shown in "Byte Sequencing" on page 2-2.

Bit-Level Protocol

Figure 2-1 shows the basic bit protocol for a transfer on the two-wire bus. The first byte provides a seven-bit device ID and one bit for read/write indication. All byte transfers are nine bits, with the ninth bit being the acknowledge bit. At the bit level, the ZL70251 two-wire protocol is identical to a standard two-wire protocol.

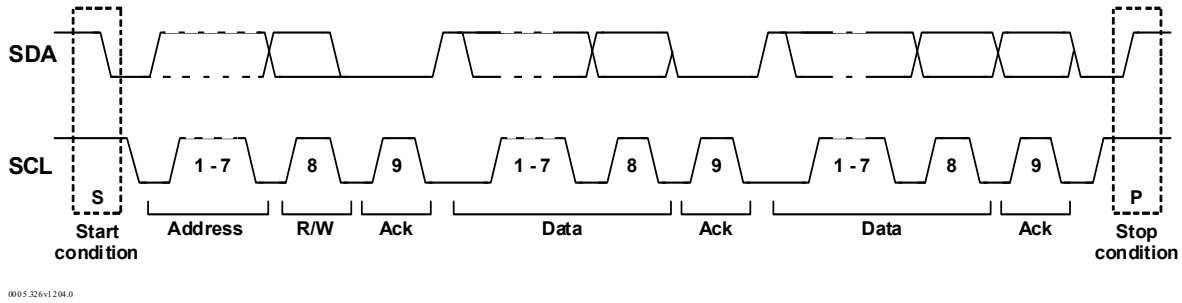


Figure 2-1 • **Bit-Level Protocol**

Byte Sequencing

The byte sequence required to control the ZL70251 is specific to the ZL70251, and is defined below. All byte definitions are shown with the MSB ([D7]) first.

Write operations are performed in one sequence of bytes (see Table 2-1). One or more bytes can be written in a write command: first (in byte 5) to the address that was specified in byte 4, then continuing to autoincrement to the next address for each of the remaining bytes.

Table 2-1 • **Write Command Sequence**

Bits	Description
Byte 1, bits [D7:D1]	Device ID for ZL70251 = 7'b1000101
Byte 1, bit [D0]	R/W bit; 0 = Write
Byte 2, bits [D7:D0]	Write command byte = 8'b00000010
Byte 3, bits [D7:D0]	Upper address bits [15:8] = 8'b00000000
Byte 4, bits [D7:D0]	Lower address bits [7:0] = Register address
Byte 5, bits [D7:D0]	First data byte to be written
Byte 5+N, bits [D7:D0]	Nth data byte to be written

Read operations are performed in two sequences of bytes. The first sequence is the read setup operation (see Table 2-2), which provides the first address to be read. The second sequence is the actual read operation (see Table 2-3). One or more bytes can be read in a read operation: first (in byte 2) from the address that was specified during the setup operation, then continuing to autoincrement to the next address for each of the remaining bytes.

Table 2-2 • **Read Setup Command Sequence**

Bits	Description
Byte 1, bits [D7:D1]	Device ID for ZL70251 = 7'b1000101
Byte 1, bit [D0]	R/W bit, 0 = Write
Byte 2, bits [D7:D0]	Read setup command byte = 8'b00000001
Byte 3, bits [D7:D0]	Upper address bits [15:8] = 8'b00000000
Byte 4, bits [D7:D0]	Lower address bits [7:0] = Register address

Table 2-3 • **Read Operation Sequence**

Bits	Description
Byte 1, bits [D7:D1]	Device ID for ZL70251 = 7'b1000101
Byte 1, bit [D0]	R/W bit, 1 = Read
Byte 2, bits [D7:D0]	First data byte read
Byte 2+N, bits [D7:D0]	Nth data byte read

Data Interface

Functional Description

The data interface in the MAC controls the transfer of data between the ZL70251 RF transceiver and an application processor. The data interface is always the master for SPI or PCM, and the data is clocked in or out at the selected data rate (136.5 or 186 kbit/s).

The data interface can be configured in either SPI or PCM mode. For PCM, both wide and narrow frame sync are supported. In PCM mode, the clock and frame sync can be any polarity.

The data interface supports five basic modes of operation:

- bidirectional transmit/receive multiple packets
- transmit one packet
- transmit multiple packets
- receive one packet
- receive multiple packets

Because SPI_DATA_OUT cannot be tristated, the ZL70251 requires a dedicated SPI bus connection to the application processor.

Table 2-4 • **Data Interface, SPI Timing Specifications**

Parameter	Symbol	Conditions	Min.	Nom.	Max.	Unit
System clock period	T_{SCP}	Data rate 186 kbit/s		895		ns
	T_{SCP}	Data rate 136.5 kbit/s		1221		ns
Rise time (20% to 80%)	T_R	C_{LOAD} = 200 pF R_{PULLUP} = 8 kΩ			50	ns
Fall time (80% to 20%)	T_F	C_{LOAD} = 200 pF I_{LOAD} = 1 mA			50	ns
Clock period	T_{CP}	Receive state	$5 \times T_{SCP}$	$6 \times T_{SCP}$	$7 \times T_{SCP}$	µs
Clock low	T_{CL}	Receive state		$3 \times T_{SCP}$		µs
Clock high	T_{CH}	Receive state		$3 \times T_{SCP}$	$4 \times T_{SCP}$	µs
RX data setup	T_{RSU}	Receive state	1.50	2.68		µs
RX data hold	T_{RH}	Receive state	−100			ns
RX data out	T_{RCO}	Receive state			200	ns
TX data setup	T_{TSU}	Transmit state	200			ns
TX data out	T_{TCO}	Transmit state			1000	ns
TX data hold	T_{TH}	Transmit state	−1000			ns

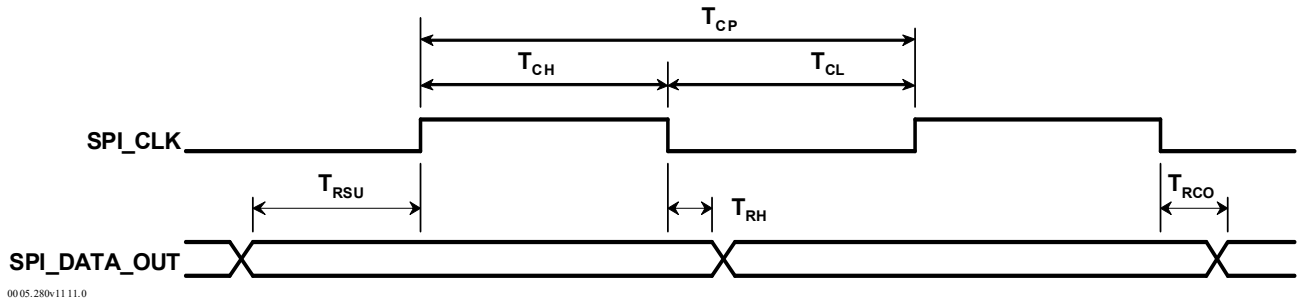


Figure 2-2 • **SPI Receive Timing, ZL70251 to External Microcontroller**

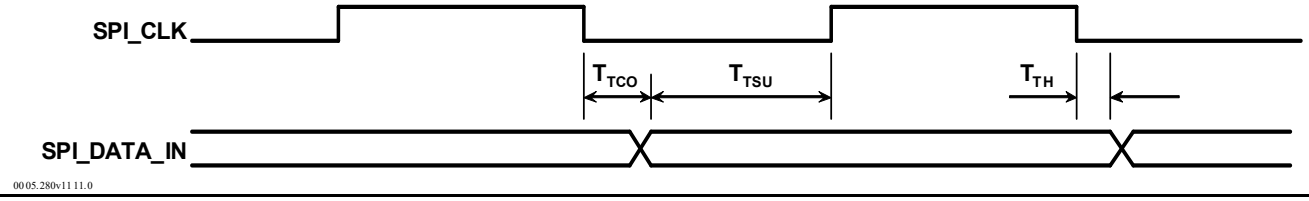
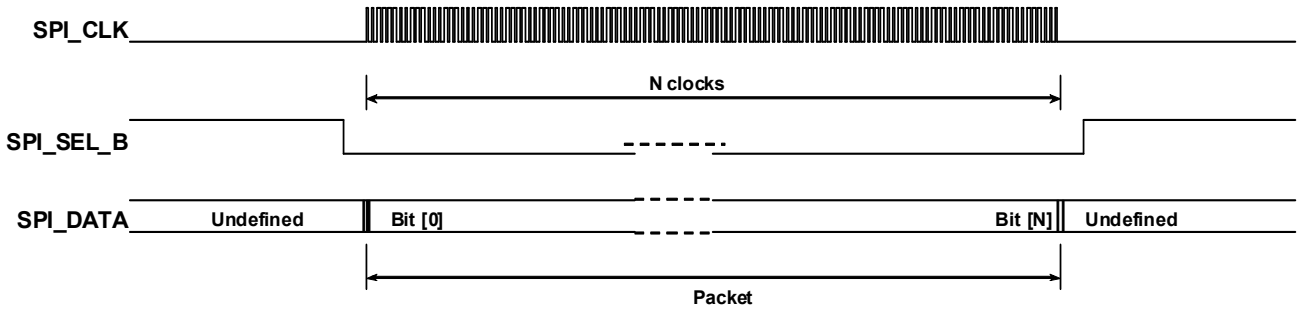


Figure 2-3 • **SPI Transmit Timing, External Microcontroller to ZL70251**

SPI Data Packet



- A packet is composed of N contiguous bits, with no data before or after packet boundaries.
- For RX, the first bit of the packet arrives on the first SPI_CLK.
- For RX, the last bit of the packet arrives on the last SPI_CLK.
- For TX, the PCM interface buffer is preloaded transmit data.
- For TX, the first bit of the first packet is transmitted on the first SPI_CLK.
- For TX, the last bit of the packet is transmitted on the last SPI_CLK.
- Data bits before the first bit of the packet , and after the last bit of the packet , are undefined and should have no effect on the SPI interface buffer for either TX or RX.
- There are no frames in SPI mode.

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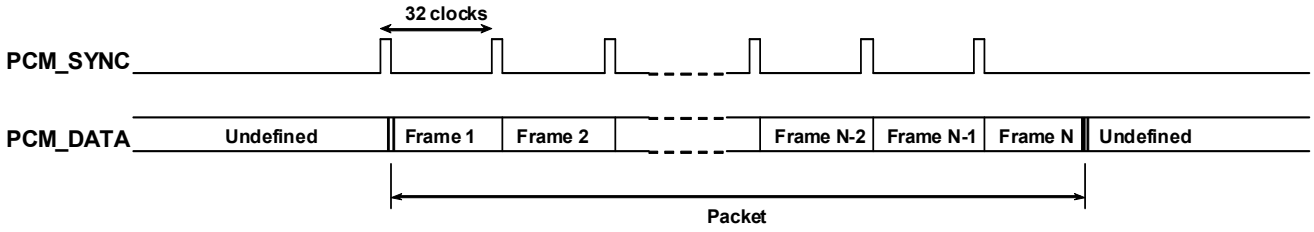
Figure 2-4 • **SPI Data Packet**

PCM Data Packet



- A packet is composed of N contiguous frames, with no data before or after packet boundaries.
- For RX, the first bit of the frame arrives during the bit-period following the PCM_SYNC.
- For RX, the last bit of the frame arrives 32 bit-periods after the last PCM_SYNC.
- For TX, the PCM interface buffer is preloaded with 8 x 32 bits.
- For TX, the first bit of the first frame is transmitted on the bit-period following the PCM_SYNC.
- For TX, the last bit of the frame is transmitted 32 bit-periods after the last PCM_SYNC.
- Data bits before the first bit of the frame, and after the last bit of the frame, are undefined and should have no effect on the PCM interface buffer for either TX or RX.

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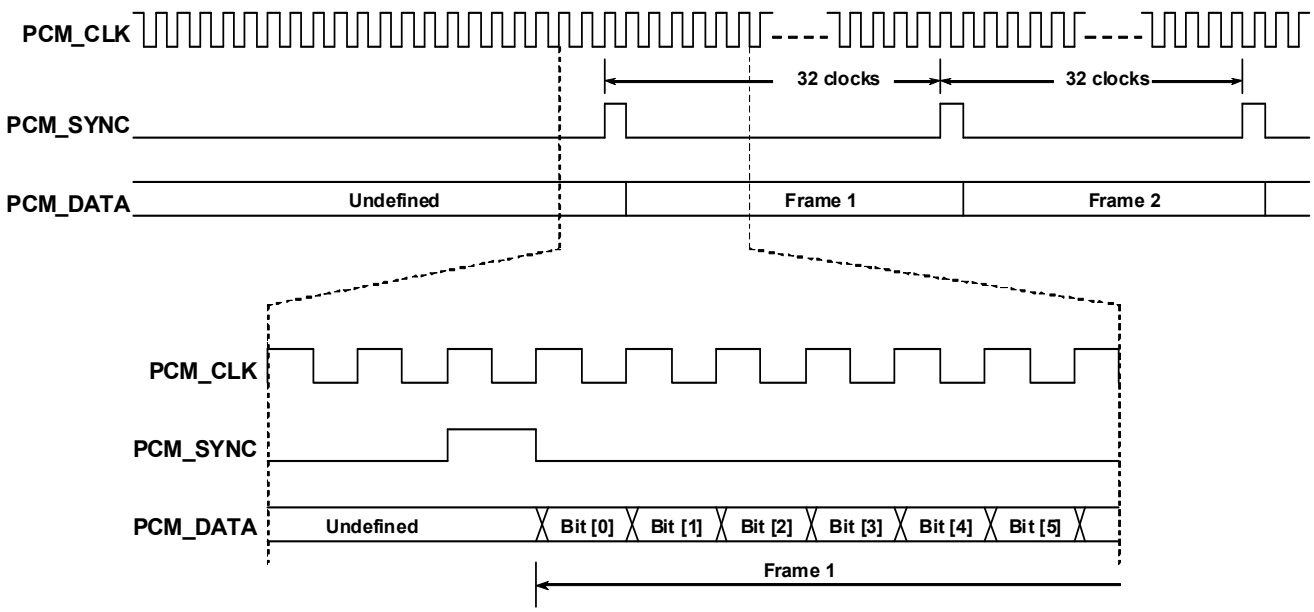
Figure 2-5 • **PCM Data Packet with 32-Bit Frame**



Note: Bit [0] is the first bit of the packet. No PCM_SYNC pulses occur prior to the pulse immediately preceding bit [0].

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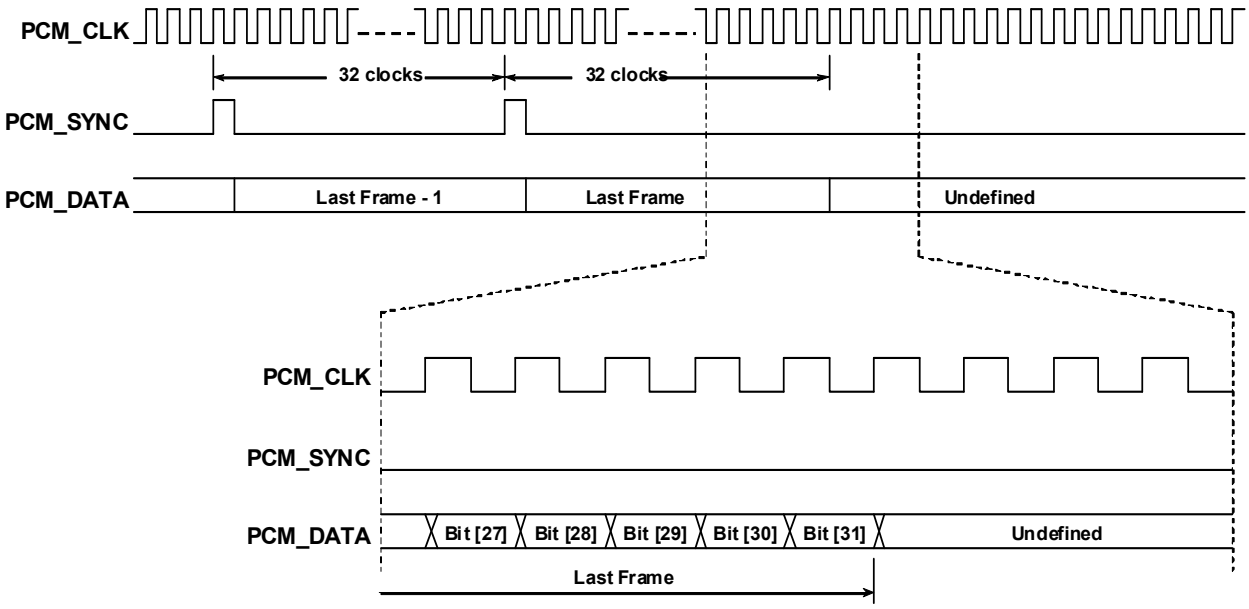
Figure 2-6 • **PCM Start of Packet**



Note: Bit [31] is the last bit of the packet. No PCM_SYNC pulses following the PCM_SYNC pulse prior to the last frame.

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Figure 2-7 • **PCM End of Packet**

3 – Electrical Reference

Absolute Maximum Ratings

Table 3-1 • **Absolute Maximum Ratings**

Parameter	Symbol	Limits			Notes
		Min.	Max.	Unit	
Supply voltage	V_{DD}	−0.3	1.98	V	Note 1
Digital and analog I/O voltage	V_{IODA}	VSS − 0.3	V_{DD} + 0.3	V	Note 2
RF I/O voltage	V_{IORF}	VSS − 0.3	2 × V_{DD}	V	Note 3
Storage temperature	T_{stg}	−40	+85	°C	
Electrostatic discharge (human body model)	V_{ESD}		RF pads: 500 All others: 1.5k	V	Note 4

Notes:

1. *Application of voltage beyond the stated absolute maximum rating may cause permanent damage to the device or reduced reliability.*
2. *Applies to digital and analog interface pins including XTAL2..1, RESET_B, CLK_OUT, TXRX_STAT, SCL, SDA, AMX3..0, SPI_CLK, SPI_DATA_IN, TXRX_CMD, SPI_DATA_OUT, SPI_SEL_B, RBIAS, DOUT1..0, IRQ, and CLKSEL.*
3. *Applies to RF frequency interface pins including TX−, RX−, RX+, and TX+.*
4. *Applied one at a time. Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.*

Recommended Operating Conditions

Table 3-2 • **Recommended Operating Conditions**

Parameter	Symbol	Min.	Max.	Unit	Notes
Supply voltage	VDD_op	1.2	1.9	V	
Operating temperature	Top	−40	+85	°C	

Digital Interface

Table 3-3 • **Digital I/O DC Specifications**

Parameter	Symbol	Conditions	Min.	Nom	Max.	Unit
Output high	V_{OH}		VDD − 0.1			V
Output low	V_{OL}				VSS + 0.1	V
Input high	V_{IH}		VDD × 0.8			V
Input low	V_{IL}				VDD × 0.2	V

Performance Characteristics

The specified performance of the ZL70251 is valid over a supply range of 1.2 to 1.9V.

Table 3-4 • **General Characteristics**

Parameter	Min.	Typ.	Max.	Unit	Notes
Operating frequency range	779		965	MHz	
Sleep state at 25°C		0.5		µA	All circuits disabled
Reference frequency		24.576		MHz	See Note 1
Symbol rate		186.182		ksps	300-kHz channel width (24.576MHz / 22 / 6)
		136.533		ksps	200-kHz channel width (24.576MHz / 30 / 6)
Channel separation		303.407		kHz	(24.576MHz / 81)
Power up		3	5	ms	From RESET_B release, assuming VDD is settled
External clock output	0.8192		6.144	MHz	(24.576MHz / N, where 4 ≤ N ≤ 30)

Note:

1. *In order to save power and reduce the number of external components, the crystal oscillator has a 3-pF load instead of a typical 8-pF or 10-pF load (refer to Table 3-7 on page 3-5). The 3-pF load is representative of the pin and PCB parasitic capacitance.*

Table 3-5 • **Receiver RF Characteristics**

Parameter	Min.	Typ.	Max.	Unit	Notes
Sensitivity at 25°C, 1.8V		−94		dBm	186kbit/s Input level resulting in BER of 10^{-3}; minimum depends on load conditions
		−95		dBm	136.5kbit/s
Maximum input power		−22		dBm	This is for the maximum LNA_GAIN of 0x0F (30dB) and maximum BER of 10^{-3}
Cascaded voltage gain		30		dB	LNA and mixer; programmable, with five settings in 3- to 4-dB steps
Current consumption		2.3		mA	Continuous RX state and maximum LNA gain
IF center frequency		606.814		kHz	(303.407kHz × 2)
RSSI range		40		dB	Digital, 32 levels of 2dB
Adjacent channel rejection		17		dB	Desired channel 3dB above the sensitivity limit; 303.407-kHz channel spacing with a modulated interferer
Alternate channel rejection		27		dB	Desired channel 3dB above the sensitivity limit; 606.814-kHz channel spacing with a modulated interferer

Table 3-6 • **Transmitter RF Characteristics**

Parameter	Min.	Typ.	Max.	Unit	Notes
Current consumption		2.4		mA	Continuous TX state; with PA trim code of 8'h08, 1 kΩ load
Maximum output power		0		dBm	1 kΩ load Refer to Figure 3-1 on page 3-4 for typical values.
Minimum output power		−24		dBm	1 kΩ load Refer to Figure 3-1 on page 3-4 for typical values.
Spurious emissions		−39 −60		dBm	868 MHz, second harmonic 868 MHz, third harmonic See Note 1
		−41 −60		dBm	915 MHz, second harmonic 915 MHz, third harmonic See Note 1
Modulation index	0.45	0.5	0.55		(±10%) A transmitted 1 is a shift to a higher frequency, 0 a shift to a lower
TX-RX or RX-TX turnaround time		2.15		ms	Programmable

Note:

1. *Test performed using a REMOTE251 ADK (refer to Figure 5-1 on page 5-1) without the optional low-pass filter. All tests conducted with the default output power of −11 dBm (pa_pwr_ctl=8) and a supply of 1.8 volts.*

Transmit Power Characteristics

Figure 3-1 and Figure 3-2 illustrate the relationship between TX power, PA trim setting, and current consumption. These measurements were made on the REMOTE251 board from a ZL70251 Application Development Kit (ADK) at room temperature and with a supply voltage of 1.8V. The figures include the losses of the matching network (approximately 2 to 3dB).

Transmit Power vs. PA Trim Value

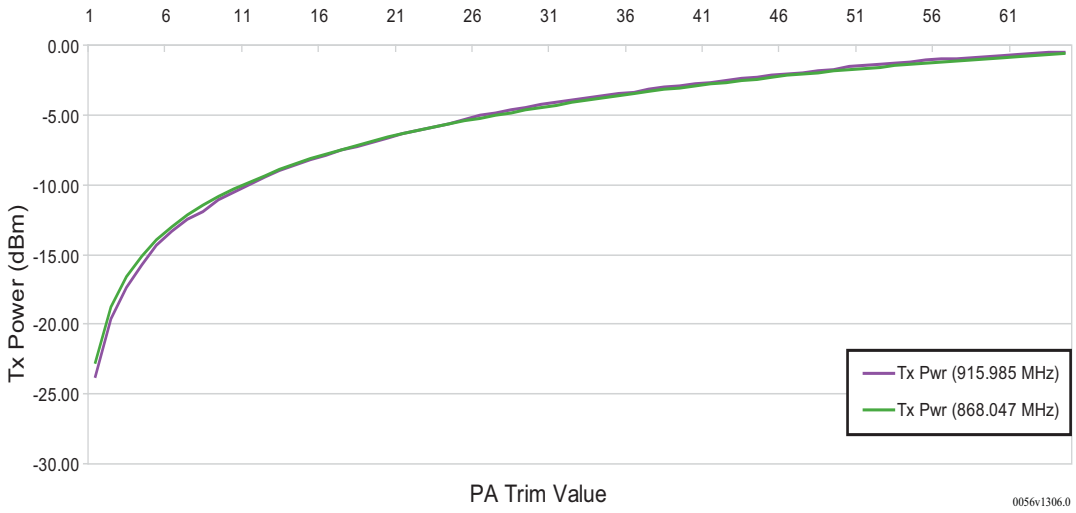


Figure 3-1 • **TX Power vs. PA Trim Value**

Transmit Power vs. Current Consumption

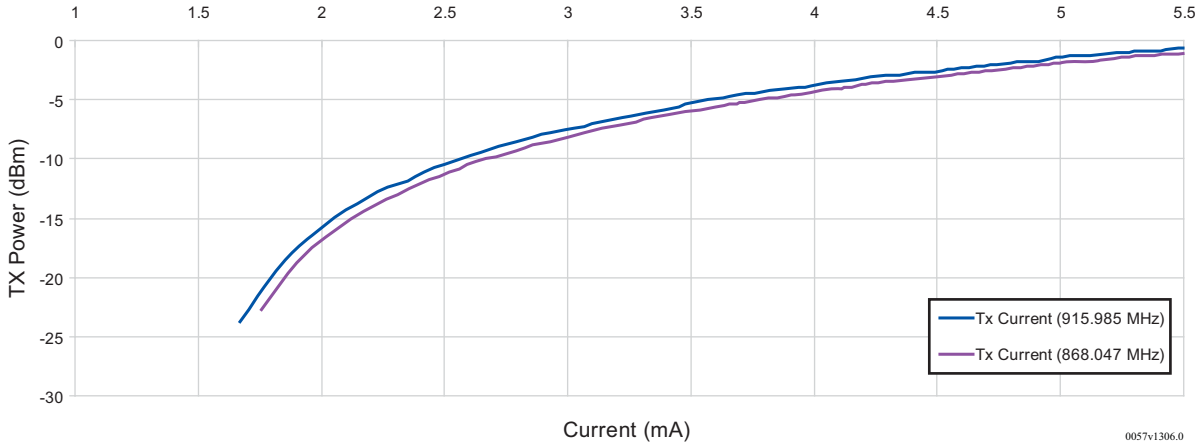


Figure 3-2 • **TX Power vs. Current Consumption**

Crystal Specifications

All frequency-related specifications are based on the crystal oscillator performance, which, in turn, is dependent on the crystal specifications. The ZL70251 specifications assume that the crystal specifications listed in Table 3-7 are met or exceeded.

Table 3-7 • **Crystal Specifications**

Parameter	Min.	Typ.	Max.	Unit	Notes
Frequency		24.576		MHz	
Frequency tolerance			±25	ppm	
Stability with temperature			±20	ppm	Over operating temp
Operating temperature range	−40		+85	°C	
Equivalent series resistance	12	63	110	ohms	
Shunt capacitance		2		pF	Note 1
Motional capacitance		1.5		fF	Note 1
Load capacitance		3		pF	Note 2
Drive level			50	µW	

Notes:

1. *A low shunt capacitance and high motional capacitance is best as it results in a larger trim range. It is particularly important if external capacitors are used, as those reduce the trim range.*
2. *In order to save power, the crystal oscillator presents a 3-pF load instead of the typical 8-pF or 10-pF load. A slight frequency pull, on the order of 100 to 150ppm, would result if using a standard crystal without additional external load capacitors. Such a deviation has no effect on the operation of the device and is generally not a problem for most applications, providing all ZL70251s have the same frequency pull (within trimmable range). If the deviation is not acceptable and power is critical, a special cut crystal may be used (that is, slightly slower to compensate for the pull). The crystal used on the BASE251 and REMOTE251 in the ZL70251 ADK (or equivalent) is recommended (Fox P/N 617-24.572675-1; call for specifications). Alternatively, if power is not as critical, external capacitors can be added, as shown in Figure 3-3 below, to bring the total load capacitance to the crystal load specification. For instance, for a crystal with an 8-pF load specification (CL), CLext = 8pF − 3pF = 5pF, so two 10-pF capacitors need to be added, one on each end of the crystal. It must be noted that this results in a reduced trim range. The frequency tolerance should therefore be tighter to compensate.*

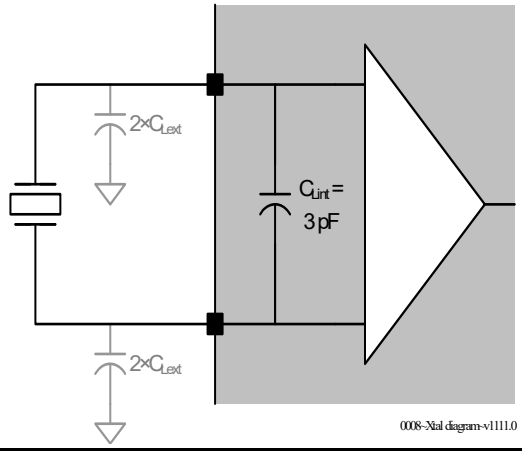


Figure 3-3 • **Crystal Oscillator with Optional Additional External Load Capacitors**

4 – Mechanical Specifications

36-Pin Chip Scale Package (CSP)

Pinout

Table 4-1 • **CSP Pinout**

CSP Pin #	Pin Name	I/O	A/D	Function	Connection
A1	XTAL1	I	A/D	Crystal connection or external clock input when CLKSEL is high. When CLKSEL is high, the input specifications are for Digital I/O (see Table 3-1 and Table 3-3 on page 3-1).	Connect to crystal.
A2	XTAL2	I	A	Crystal connection, leave open when using external clock source.	Connect to crystal.
A3	RESET_B	I	D	Reset bar (active low asynchronous reset, minimum low period 100ns). When low, the ZL70251 is in reset and all circuits are off. When transitioning from low to high, all registers are set to their power-on-reset values, the crystal oscillator starts up, all other circuits are disabled, and the ZL70251 is in the **IDLE** state.	Connects to application processor to allow for a full chip reset when driven low.
A4	CLK_OUT	I/O	D	Programmable clock output. The clock output frequency is the crystal frequency/N, where 4≤N≤30.	Recommended use is for trimming the crystal oscillator in production.
A5	NC			Reserved: do not use; no electrical connection.	
B1	VDDTEST	PWR	A	Supply voltage for test buffers.	Supply for internal analog buffers used for factory testing. Leave open for normal operation.
B2	NC			Reserved: do not use; no electrical connection.	
B3	TXRX_STAT	O	D	Transmit/receive status. When high, the device is in a transmit state. When low, the device is in a receive state.	Connects to the application processor to monitor the transmit/receive state of the ZL70251. Additionally, it can be used to control an external RF switch. This is typically done when an external LNA and/or PA are added (see the ZL70251 ADK BASE251 board schematic for an example).
B4	SCL	I	D	Serial clock (similar to two-wire); ZL70251 is slave.	An external 10-kΩ pull-up resistor is recommended.

Table 4-1 • **CSP Pinout (continued)**

CSP Pin #	Pin Name	I/O	A/D	Function	Connection
B5	SDA	I/O	D	Data input or open drain output for serial data (similar to two-wire); ZL70251 is slave.	An external 10-kΩ pull-up resistor is recommended.
C1	AMX2	O	A	Analog test bus output.	Leave open for normal operation.
C2	AMX3	O	A	Analog test bus output.	Leave open for normal operation.
C4	SPI_CLK	O	D	SPI clock (master clock). Can be configured for PCM clock. See ZL70251 Programmer User's Guide.	Connects to the application processor's SPI or PCM interface.
C5	SPI_DATA_IN	I	D	SPI data input. Can be configured for PCM data input. See ZL70251 Programmer User's Guide.	Connects to the application processor's SPI or PCM interface.
D1	AMX0	I	A	Analog test bus input.	Leave open for normal operation.
D2	AMX1	I	A	Analog test bus input.	Leave open for normal operation.
D3	TXRX_CMD	I	D	Transmit/receive control (see ZL70251 Programmer User's Guide).	Connects to the application processor to control packet transmit and receive.
D4	SPI_DATA_OUT	O	D	SPI data output. Can be configured for PCM data output (see ZL70251 Programmer User's Guide).	Connects to the application processor's SPI or PCM interface.
D5	SPI_SEL_B	O	D	SPI select output (active low). Can be configured for data frame or PCM frame output (see ZL70251 Programmer User's Guide).	Connects to the application processor's SPI or PCM interface.
E1	VDDA	PWR	A	Analog power supply (1.2V to 1.9V).	Recommend a 0.1-µF decoupling capacitor mounted close to the ZL70251 VDDA pin.
E2	RBIAS	I	A	Bias resistor used to trim the internal current reference.	Connect to an external 51.0-kΩ (±1%) resistor to ground.
E3	DOUT0	O	D	Digital test output.	Leave open or use to route out internal digital signals (e.g., sync detect).
E4	VDDD	PWR	A	Digital power supply (1.2V to 1.9V).	Recommend a 0.1-µF decoupling capacitor mounted close to the ZL70251 VDDD pin.
E5	IRQ	O	D	Interrupt output.	Connects to the application processor to detect an interrupt from the ZL70251.
F1	VSSA	PWR	A	Analog ground.	Connection to a ground plane is recommended.
F3	NC			Reserved: do not use; no electrical connection.	
F5	VSSD	PWR	A	Digital ground.	Connection to a ground plane is recommended.
G1	VSSH	PWR	A	Isolated power amplifier ground.	Connection to a ground plane is recommended.

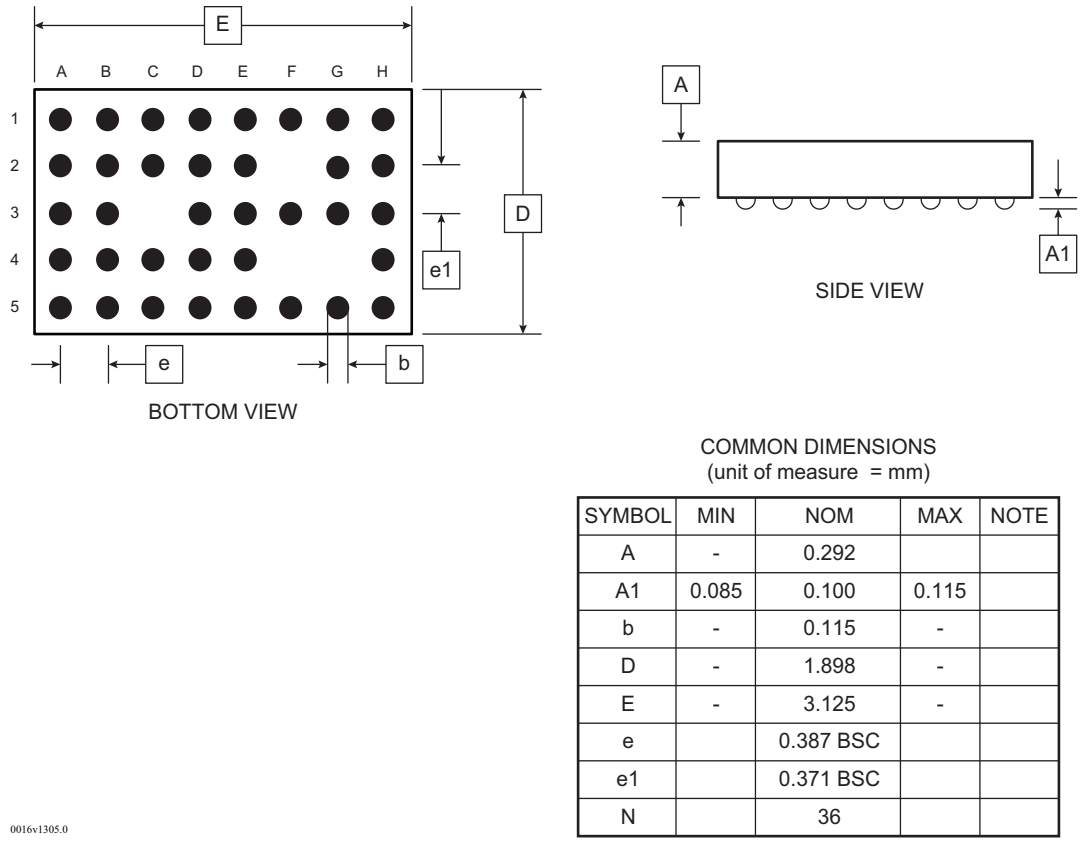
Table 4-1 • **CSP Pinout (continued)**

CSP Pin #	Pin Name	I/O	A/D	Function	Connection
G2	TX−	O	A	Transmitter RF negative output. Requires external biasing to the power supply.	Connects directly to a loop antenna or a matching network.
G3	VSSA2	PWR	A	Analog ground.	Connection to a ground plane is recommended.
G5	DOUT1	O	D	Digital test output.	Leave open or use to route out internal digital signals to the application processor (e.g., sync detect).
H1	RX−	I	A	Receiver RF negative input. This output is AC coupled and is connected to internal capacitors that can be used for automatic tuning to antennas that connect directly to the receiver inputs.	Connects directly to a loop antenna or a matching network.
H2	RX+	I	A	Receiver positive input. This input is AC coupled and is connected to internal capacitors that can be used for automatic tuning to antennas that connect directly to the receiver inputs.	Connects directly to a loop antenna or a matching network.
H3	TX+	O	A	Transmitter RF positive output. Requires external biasing to the power supply.	Connects directly to a loop antenna or a matching network.
H4	NC			Reserved: do not use; no electrical connection.	
H5	CLKSEL	I	D	Clock set. When low, the internal crystal oscillator is selected. When high, the internal oscillator is bypassed on the XTAL1 pin, allowing an external clock to be used.	This input has an internal pull-down. See Note 1.

Note:

1. ***Regarding pull-down:*** *Digital pad CLKSEL has a built-in pull-down resistor. This input has two pull-down values. When an input is driven high, a 1-MΩ resistor is enabled. When the input is driven low, a 100-kΩ resistor is enabled. This reduces power consumption for when the pin is driven high. The pull-down resistors on this input can be removed by setting bit [4] of register CLK_ENS.*

Package Mechanical Specifications



COMMON DIMENSIONS
(unit of measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	0.292		
A1	0.085	0.100	0.115	
b	-	0.115	-	
D	-	1.898	-	
E	-	3.125	-	
e		0.387 BSC		
e1		0.371 BSC		
N		36		

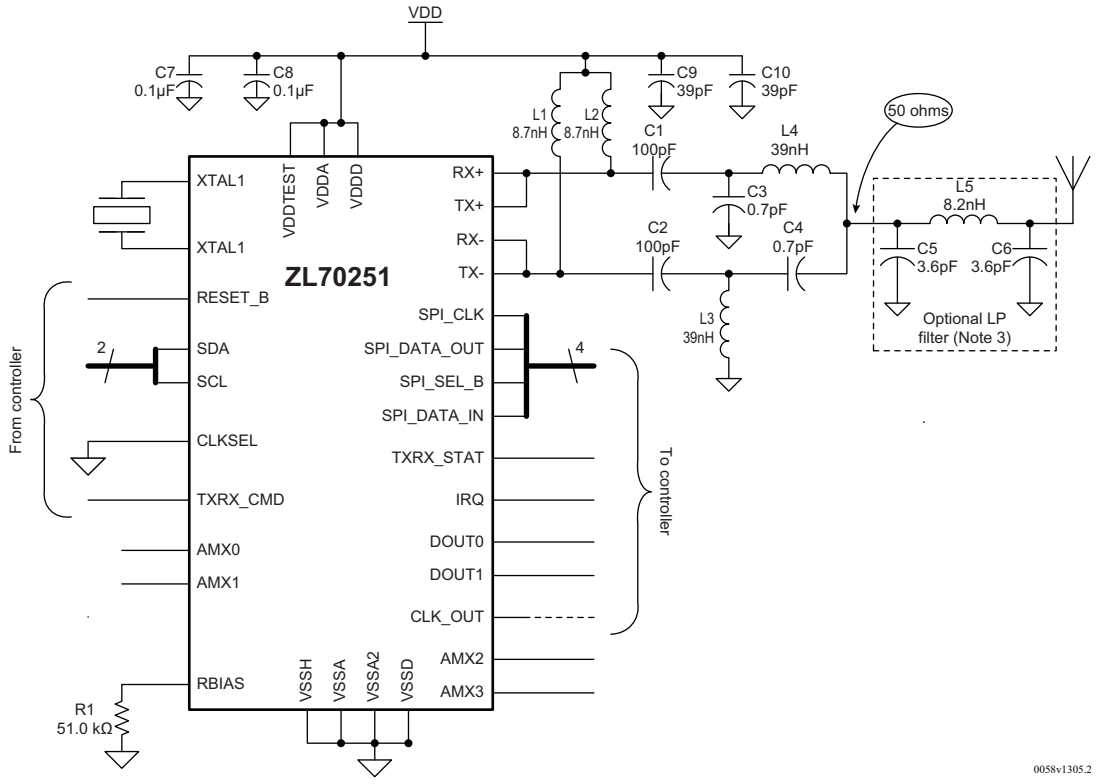
Notes:

1. *The back-side orientation mark is located on the H1 corner of the die. (This was done for consistency with our legacy bumped die devices.)*

Figure 4-1 • **ZL70251 CSP Bottom View**

5 – Typical Application Example

Figure 5-1 is representative of a 50-Ω single-ended implementation. An optional low-pass filter on the output is recommended to attenuate second and third harmonic spurious emissions to meet regulatory standards.



Notes:

1. *This schematic is based on the REMOTE251 board from the ZLE70251 Application Development Kit.*
2. *C3, C4, L3, and L4 values may change if the layout differs from the REMOTE251 board layout. To ensure optimal performance, please do not deviate from the REMOTE251 board layout.*
3. *L1 and L2 are optimized for tuning over the middle to upper frequency range (863 to 965MHz). Changing L1 and L2 to approximately 12nH allows tuning over the lower to middle frequency range (779 to 868MHz).*
4. *The optional low-pass filter reduces the transmitter spurious emissions by approximately 16dB for the second harmonic and 23dB for the third harmonic. Another option would be to replace this circuit with a SAW filter to attenuate spurious emissions and to provide protection against blockers.*

Figure 5-1 • **50-Ω Single-Ended Application Example with Optional Low-Pass Filter**

6 – Glossary

Term	Explanation
A	Analog
A/D	Analog/digital
AC	Alternating current
ACK	Acknowledgement
ADC	Analog-to-digital converter
addr	Address
ADK	Application development kit
AGC	Automatic gain control
ANT	Antenna
BER	Bit error ratio
CCA	Clear channel assessment
Clk	Clock
cmd	Command
CODEC	Coder/decoder
CSP	Chip Scale Package
Ctrl	Control
D	Digital
DAC	Digital-to-analog converter
DC	Direct current
EEPROM	Electrically erasable and programmable read-only memory
EMC	Electromagnetic compatibility
EN	European Standard (French: Norme)
ESD	Electrostatic discharge
ETS	European Telecommunications Standard
ETSI	European Telecommunications Standards Institute
Ext	External
FCC	Federal Communications Commission (US)
FM	Frequency modulation
FR4	Flame retardant 4 (printed circuit board)
Freq	Frequency
Gen	Generator
GFSK	Gaussian frequency shift keying
GPIO	General-purpose input/output

Term	Explanation
I	Current; Input
I/O	Input/output
IC	Integrated circuit
ID	Identification
IF	Intermediate frequency
ISM	Industrial, Scientific, and Medical
ksps	Thousand (or kilo) symbols per second
LO	Local oscillator
LNA	Low-noise amplifier
LP	Low pass
MAC	Media access controller
Max	Maximum
MSB	Most significant bit
Min	Minimum
mux	Multiplexer
OSC	Oscillator
NC	No connect
Nom	Nominal
P	Stop
PA	Power amplifier
PCM	Pulse code modulation
PLL	Phase-locked loop
ppm	Parts per million
pwr	Power
R/W	Read/write
ref	Reference
RF	Radio frequency
rms	Root mean square
RSSI	Received signal strength indicator
RX	Receive
S	Start
SMA	Subminiature A
SPI	Serial peripheral interface
SRD	Short-range device
SSI	Synchronous serial interface
Sym	Symbol

Term	Explanation
sync	Synchronization
synth	Synthesizer
T&R	Tape and reel
TX	Transmit
Typ	Typical
US	United States
USB	Universal serial bus
V	Voltage; Volt(s)
VCO	Voltage-controlled oscillator
VDD	Supply voltage
VDDA	Supply voltage, analog
VDDD	Supply voltage, digital
vs	Versus
VSS	Ground
Wr	Write
XTAL	Crystal

7 – Datasheet Information

List of Changes

The following table lists substantive changes that were made in the ZL70251 Ultra-Low-Power Sub-GHz RF Transceiver datasheet (146670).

Revision	Changes	Page
Revision 3 (March 2018)	Modified Table 3-1 for consistency across datasheets. Removed row for reverse supply voltage; supply voltage row now reflects reverse supply voltage in minimum rating. Modified existing notes and added new notes. Modified symbols and wording.	3-1
	Added missing unit to Table 3-3.	3-1
	In Table 4-1, changed wording of description for reserved pins.	4-1
	Replaced note in Figure 4-1.	4-4
	Corrected typographical error at GFSK in glossary.	6-1
Revision 2 (October 2013)	Under "Features" section, changed typical TX current to be 5.5mA and supply voltage range to be from 1.2V.	I
	Under "Ordering Information" section, changed to final part number (without suffix).	I
	In chapter "1 – Overview", corrected second paragraph (including changing typical peak/average current consumption).	1-1
	Under "Data Interface" > "Functional Description", corrected typo. PCB should have been PCM.	2-3
	In Table 3-2: • Changed supply voltage range to be from 1.2V. • Chinese band no longer has separate specs. Removed table row and notes.	3-1
	Under "Performance Characteristics" changed supply voltage to be from 1.2V.	3-2
	In Table 3-5: • Removed the row for parameter "1-dB compression point." • Added a row for new parameter "Maximum input power." • Edited note for cascaded voltage gain. • Changed typical value and edited note for adjacent channel rejection. • Changed typical value and edited note for alternate channel rejection.	3-2
	Under "Transmit Power Characteristics" corrected units for losses of the matching network to dB.	3-4
	In Table 4-1: • Removed references to pull-downs for pins RESET_B, SPI_DATA_IN, and TXRX_CMD (under *Connection* column). • Rewrote text in *Connection* column for pin CLKSEL. • Modified *Note 1* regarding pull-downs. • Changed supply voltage to be from 1.2V for pins E1 and E4.	4-1

Revision	Changes	Page
Revision 2, cont'd	In Figure 5-1, added a new note 3 and edited following note (renumbered 4).	5-1
	Minor grammar and formatting changes.	–
Revision 1, Preliminary (June 2013)	Initial release.	All

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