Microtips TECHNOLOGY

MODEL No: MTD0139AZOG-1

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Record of Revision

Date	Revision No.	Summary
2016-05-10	1.0	Rev 1.0 was issued

1. Scope

This data sheet is to introduce the specification of MTD0139AZOG-1 ,active matrix OLED module. It is composed of an OLED panel, driver IC and FPC. The 1.39″ display area contains 400 x 400 pixels.

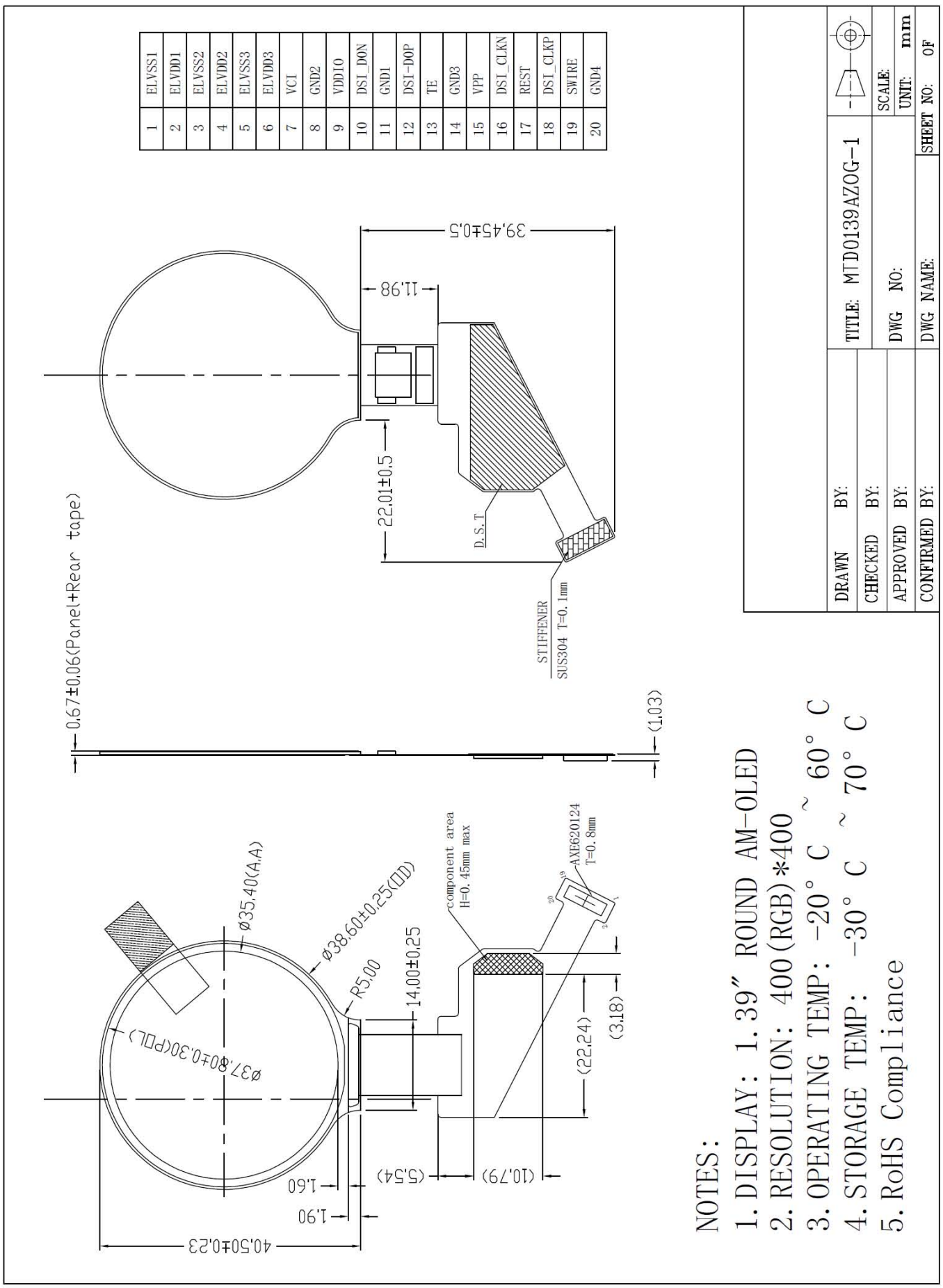
2. Application

Digital equipments which need display, instrumentation, remote control, electronic product.

3. General Information

Item	Contents	Unit
Size	1.39	inch
Resolution	400(RGB) x 400	/
Display Color	Full Color	
Interface	MIPI DSI	
Outline Dimension	38.6 x 40.5 x 0.67	mm
Active Area	Φ 35.4	mm
Weight	2	g
Operating Temperature	-20℃ ~ +60℃	
Storage Temperature	-30℃ ~ +70℃	

4. Outline Drawing



5. Interface signals

FPCA recommended connector:AXE520124

PIN NO.	PIN NAME	DESCRIPTION
1	ELVSS1	Negative power supply
2	ELVDD1	Positive power supply
3	ELVSS2	Negative power supply
4	ELVDD2	Positive power supply
5	ELVSS3	Negative power supply
6	ELVDD3	Positive power supply
7	VCI	Driver analog power supply
8	GND2	Ground
9	VDDIO	Ditital I/O power supply
10	DSI_D0N	MIPI DSI data0-
11	GND1	Ground
12	DSI_D0P	MIPI DSI data0+
13	TE	Tearing effect output
14	GND3	Ground
15	VPP	Power supply for OTP. Leave the pin to open when not in use.
16	DSI_CLKN	MIPI DSI clock-
17	REST	This signal will reset the device and must be applied to properly initialize the chip. Active low.
18	DSI_CLKP	MIPI DSI clock+
19	SWIRE	Swire protocol setting pin for power IC
20	GND4	Ground

6. Absolute maximum Ratings

6.1 Electrical Absolute max. ratings

Parameter	Symbol	MIN	MAX	Unit	Remark
Digital Power Supply	VDDIO	-0.3	5.5	V	
Analog Power Supply	VCI	-0.3	5.5	V	
ELVDD power Supply	ELVDD	-	5.0	V	
ELVSS power Supply	ELVSS	-5.0	-	V	

6.2 Environment Conditions

Item	Symbol	MIN	MAX	Unit	Remark
Operating Temperature	TOPR	-20	60	℃	
Storage Temperature	TSTG	-30	70	℃	

7. Electrical Specifications

7.1 Electrical characteristics

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Digital Power Supply	VDDIO	1.65	1.8	1.95	V	
Analog Power Supply	VCI	2.7	2.8	2.9	V	
ELVDD power Supply	ELVDD	4.55	4.60	4.65	V	
ELVSS power Supply	ELVSS	-2.45	-2.40	-2.35	V	
High logic Input Voltage	VIH	0.8*VDDIO	-	VDDIO	V	
Low logic Input Voltage	VIL	0	-	0.2*VDDIO	V	
High logic Output Voltage	VOH	0.8*VDDIO	-	VDDIO	V	
Low logic Output Voltage	VOL	0	-	0.2*VDDIO	V	

Note : The operation is guaranteed under the recommended operating conditions only. The operation is not guaranteed if a quick voltage change occurs during the operation. To prevent the noise, a bypass capacitor must be inserted into the line closed to the power pin.

7.2 Current Consumption

7.2.1 Normal Mode

Power supply: IOVCC=1.8v VCI=2.8v

Frame Frequency: F_{frame} =60HZ @ 25degC,Brightness 300 nits, Command Mode

Display Condition	Symbol	MIN	TYP	MAX	Unit
100% Pixel On 300 nits	IELVDD/ELVSS	-	21.0	25.4	mA
	IVCI	-	6.0	7.2	mA
	IVDDIO	-	2.0	2.4	mA
50% Pixel On 150 nits	IELVDD/ELVSS	-	5.2	6.2	mA
	IVCI	-	6.6	8.0	mA
	IVDDIO	-	2.0	2.4	mA
10% Pixel On 50 nits	IELVDD/ELVSS	-	0.4	0.5	mA
	IVCI	-	7.2	8.6	mA
	IVDDIO	-	2.0	2.4	mA

7.2.2 Idle Mode

Power supply: IOVCC=1.8v VCI=2.8v

Frame Frequency: F_{frame} =15HZ @ 25degC,Brightness 30 nits

Display Condition	Symbol	MIN	TYP	MAX	Unit
10% Pixel On 30 nits	IELVDD/ELVSS	-	-	-	mA
	IVCI	-	3.0	3.6	mA
	IVDDIO	-	1.0	1.2	mA

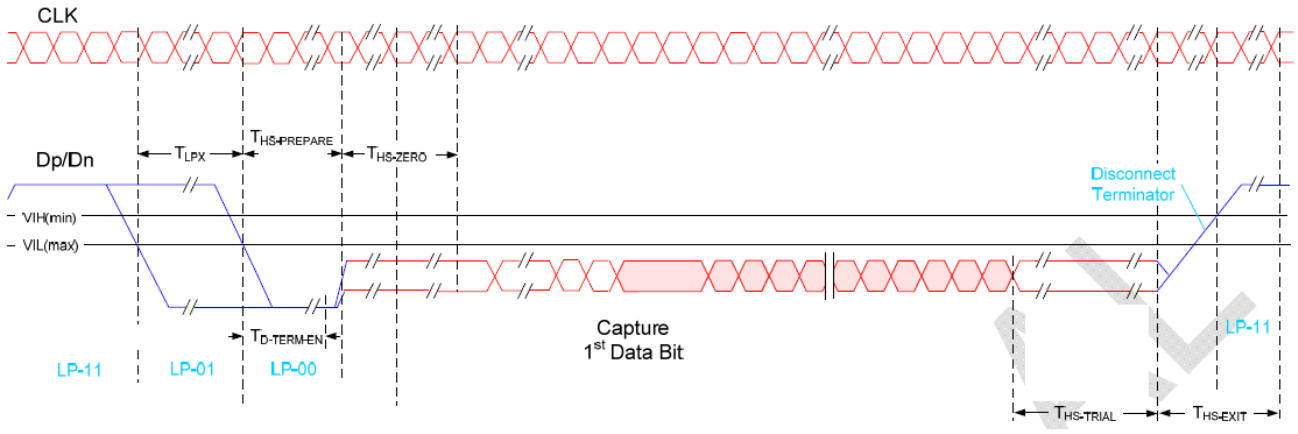
7.2.3 Deep Standby Mode

Display Condition	Symbol	MIN	TYP	MAX	Unit
Deep Standby	IVCI	-	-	1	uA
	IVDDIO	-	-	0	uA

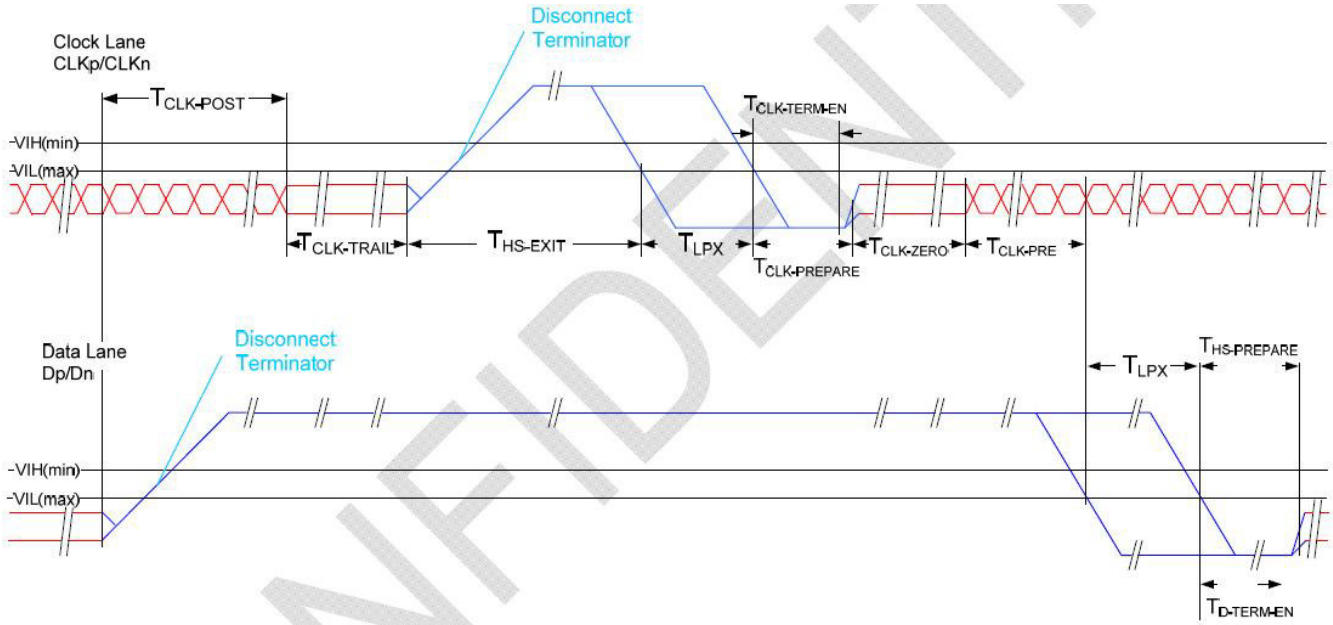
8. Command/AC Timing

8.1 MIPI Interface Characteristics

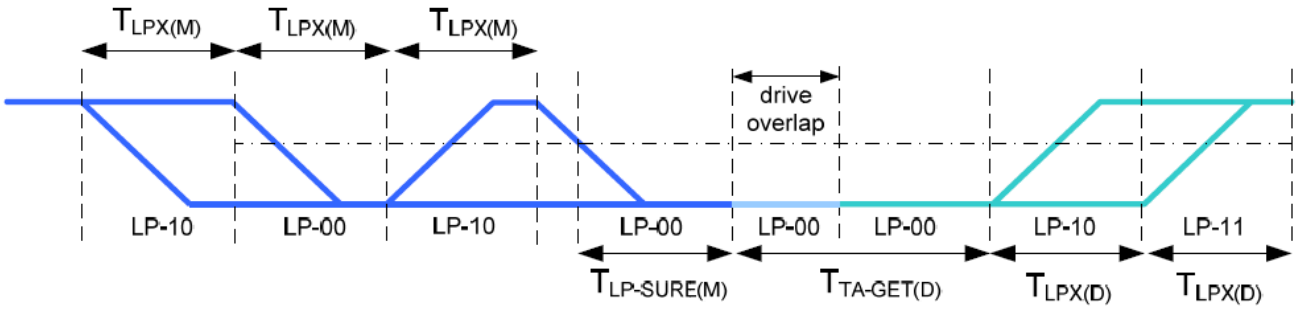
1) HS Data Transmission Burst



2) HS clock transmission



3) Turnaround Procedure



4) Timing Parameters

Symbol	Description	Min	Typ	Max	Unit
TREOT	30%-85% rise time and fall time	-	-	35	ns
TCLK-MISS	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.	-	-	60	ns
TCLK-POST*1	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL.	60ns + 52*UI (For DCS)	-	-	ns
TCLK-PRE	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8	-	-	ns
TCLK-SETTLE	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PRE.	95	-	300	ns
TCLK-TERM-EN	Time for the Clock Lane receiver to enable the HS line termination,starting from the time point when Dn crosses VIL,MAX.	Time for Dn to reach VTERM-EN		38	ns
THS-SETTLE	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from	85 ns + 6*UI		145 ns + 10*UI	ns

	the beginning of THSPREPARE.				
TEOT	Time from start of THS-TRAIL or TCLK-TRAIL period to start of LP-11 state	-	-	105ns+48*UI	ns
THS-EXIT(1)	time to drive LP-11 after HS burst	100	-	-	ns
THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40ns + 4*UI	-	85ns+6*UI	ns
THS-PREPARE + THS-ZERO	THS-PREPARE + Time to drive HS-0 before the Sync sequence	145ns + 10*UI	-	-	ns
THS-SKIP	Time-out at RX to ignore transition period of EoT	40	-	55ns+4*UI	ns
THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60 + 4*UI	-	-	ns
TLPX	Length of any Low-Power state period	50	-	-	ns
Ratio TLPX	Ratio of TLPX(MASTER)/TLPS(SLAVE) between Master and Slave side	2/3	-	3/2	ns
TTA-GET	Time to drive LP-00 by new TX	5*TLPX	5*TLPX	5*TLPX	ns
TTA-GO	Time to drive LP-00 after Turnaround Request	4*TLPX	4*TLPX	4*TLPX	ns
TTA-SURE	Time-out before new TX side starts driving	TLPX	-	2*TLPX	ns

8.2 Display RESET Timing Characteristics

8.2.1 Reset input timing

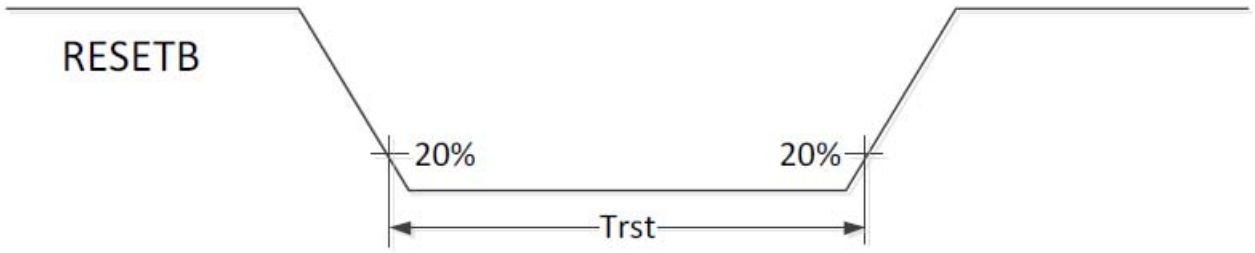


Figure: Reset timing

8.2.2 Timing Parameters

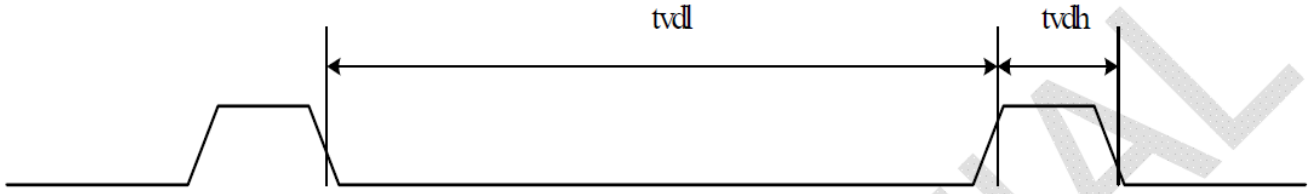
When RESETB of the reset pin equals to Low, it will be in the condition of reset.
When it is in the condition of reset, it will make the device recover the initial set.
However, in order to avoid the reset noise cause reset, there is a mechanism to judge about whether the reset is needed or not.
The closed interval of Low can be shown as the following.

(Test condition: VDDIO=1.65V~3.6V, VSS=0V, TA=-20℃~+70℃)

Parameter	Symbol	Conditions	Spec			Unit
			Min.	Typ.	Max.	
Reset low pulse width	Trst	-	20	-	-	μs

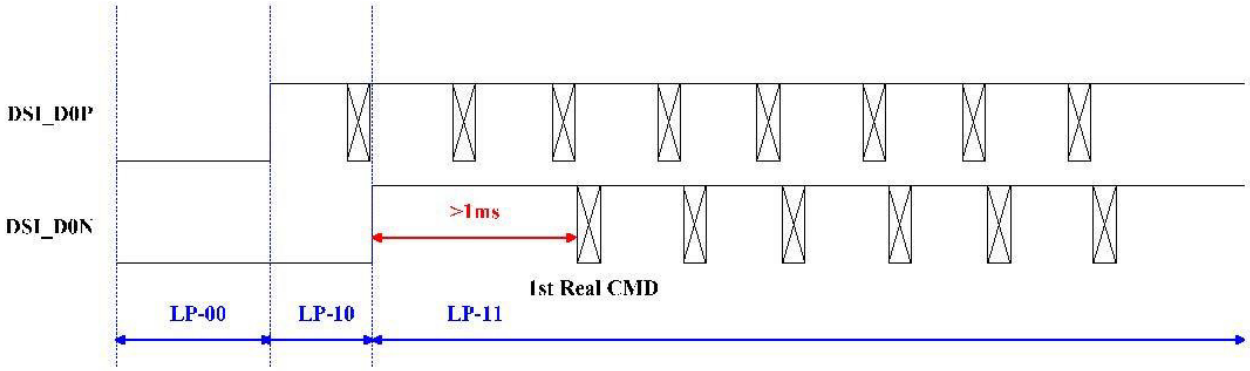
8.2.3 TE Timing Characteristics

Mode 1, the tearing effect output signal consist of V-sync information only:



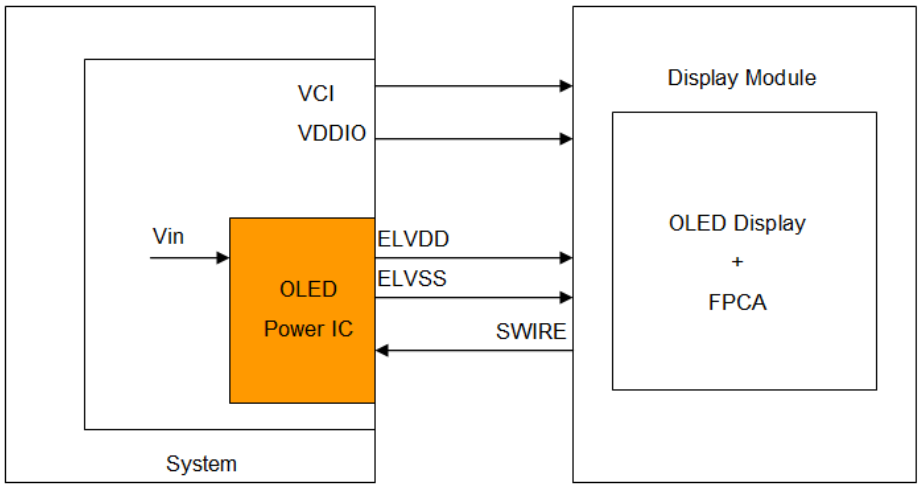
tvdh = The LCD display is not updated from the frame memory.
tvdl = The LCD display is updated from the frame memory.

8.2.4 MIPI Initial CMD Flow



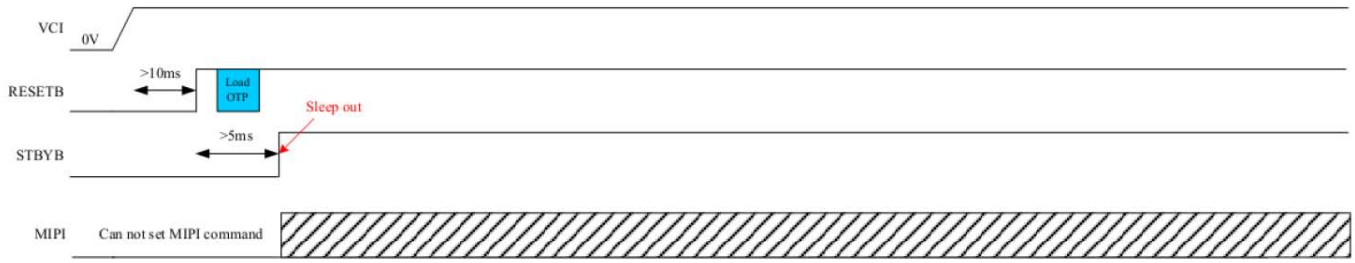
8.2.5 Operating Sequence

Power Structure

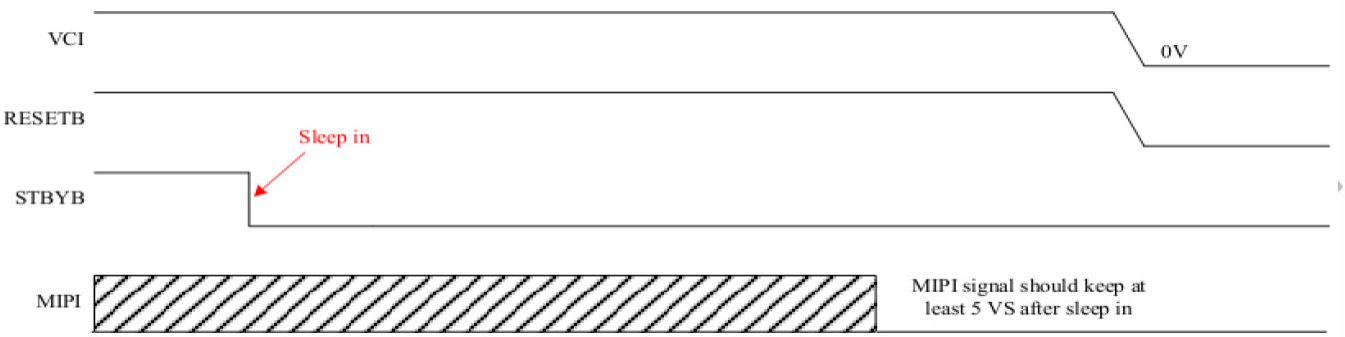


1）Display Power on/off Sequence

Power on sequence



Power off sequence



2） Display Initial Setting

Recommended Power on Initial Sequence								
Step	Instruction/Parameters	Delay time	R/W	MIPI Data Type	Address		Data hex.	Description
					MIPI	Others		
1	Turn on V_{CI}							VCI=2.8V
2	Turn on V_{DDIO}							VDDIO=1.8V
3	Delay	no limit						
4	REST pin low	20us						
5	REST pin high							
6	Delay	5 ms						
7			W	0x15	FE	FE00	05	
8			W	0x15	05	0580	00	
9			W	0x15	FE	FE00	07	
10			W	0x15	07	07A0	4F	
11			W	0x15	FE	FE00	0A	
12			W	0x15	1C	1CD0	1B	
13			W	0x15	FE	FE00	00	
14			W	0x15	35	3500	00	
15	Sleep out		W	0x05	11	1100	00	
16	Turn on peripheral packet			0x32				Video Turn On
17	Delay	300 ms						
	Display on		W	0x05	29	2900	00	

Recommended Power off Mode Sequence								
Step	Instruction/Parameters	Delay time	R/W	MIPI Data Type	Address		Data hex.	Description
					MIPI	Others		
1	Display Off		W	0x05	28	2800	00	
2	Sleep in		W	0x05	10	1000	00	
3	delay	120ms						
4	Power off							

8.2.6 Idle mode Flow

(1) Normal to Idle

Recommended Idle Initial Sequence								
Step	Instruction/Parameters	Delay time	R/W	MIPI Data Type	Address		Data hex.	Description
					MIPI	Others		
1	Enter Idle mode		W	0x05	39	3900	00	Idle mode 15HZ

(2) Idle to Normal

Recommended Power on Initial Sequence								
Step	Instruction/Parameters	Delay time	R/W	MIPI Data Type	Address		Data hex.	Description
					MIPI	Others		
1	Idle mode Off		W	0x05	38	3800	00	Normal mode 60HZ

Brightness Control

Recommended Brightness Control							
Instruction/Parameters	Delay time	R/W	MIPI Data Type	Address		Data hex.	Description
				MIPI	Others		
Brightness control		W	0x05	51	5100	Value	Value form 0~255(FF)

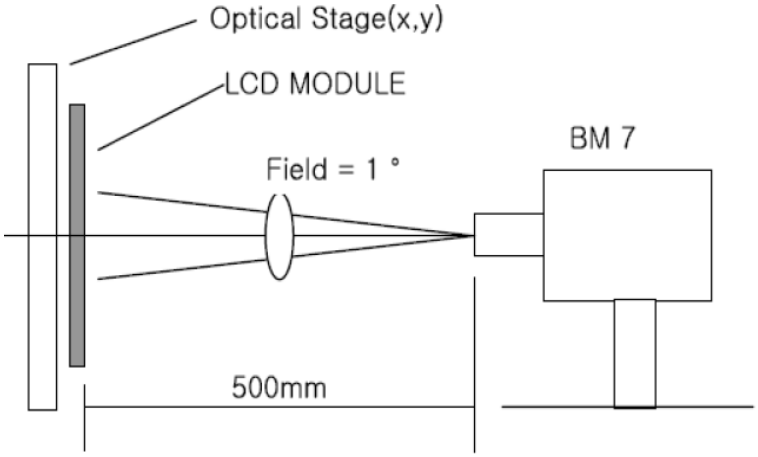
9. Optical Specification

Item		Symbol	Condition	Min	Typ.	Max.	Unit	Remark
Contrast Ratio		CR	θ=0°	5000	10000	-		Note1 Note2
View Angles		Θ	--	160	170	-	Degree	Note 4
Optical Switching Time		(Tr+Tf)/2	25℃	-	2	4	ms	Note1 Note3
Chromaticity	White	x	Brightness is on	0.27	0.30	0.33		Note5, Note1
		y		0.28	0.31	0.34		
	Red	x		-	0.66	-		
		y		-	0.34	-		
	Green	x		-	0.21	-		
		y		-	0.74	-		
	Blue	x		-	0.13	-		
		y		-	0.06	-		
Luminance		L		250	300	-	cd/m2	Note1 Note6
Brightness Uniformity				85	-	-	%	Note7
NTSC				85	100	-	%	
Gamma				1.9	2.2	2.5		Note8
Flicker				-	-30	-	db	Note9
Crosstalk				-	-	110	%	Note10

Note 1: Definition of optical measurement system.

Temperature = 25℃(±3℃)

LED back-light: ON, Environment brightness < 150 lx

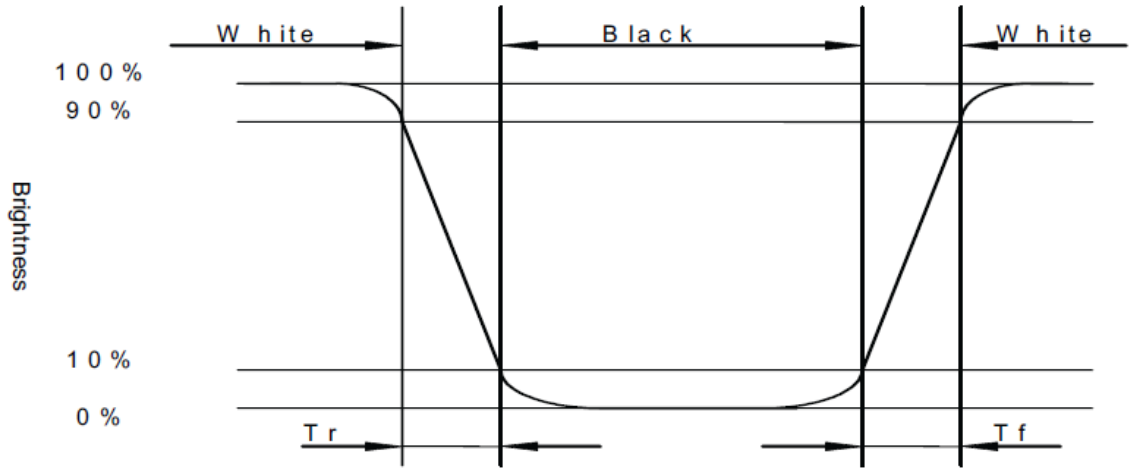


Note 2: Contrast ratio is defined as follow:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

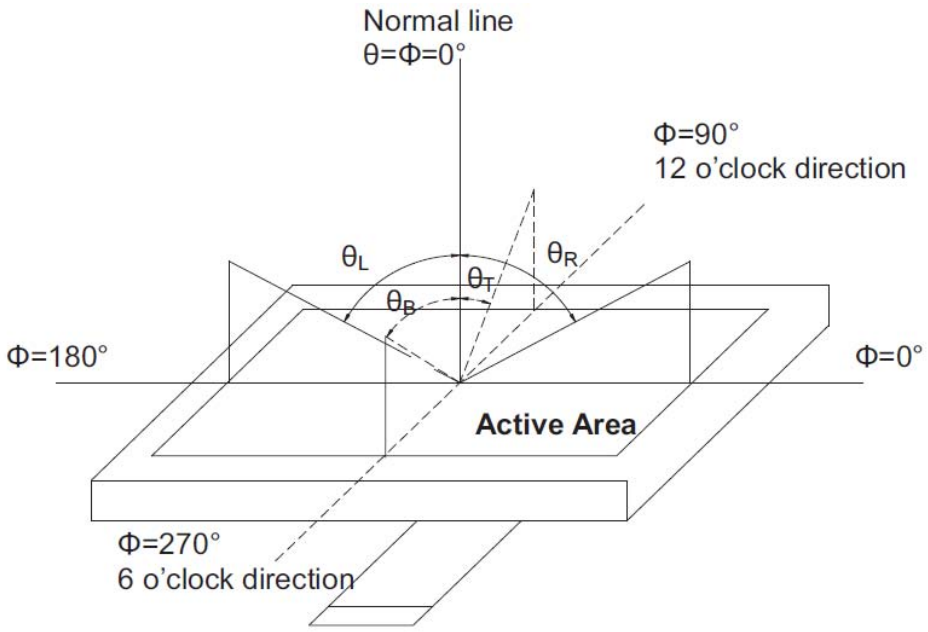
Note 3: Response time is defined as follow:

Response time is the time required for the display to transition from black to white (Rise Time, Tr) and from white to black(Decay Time, Tf).



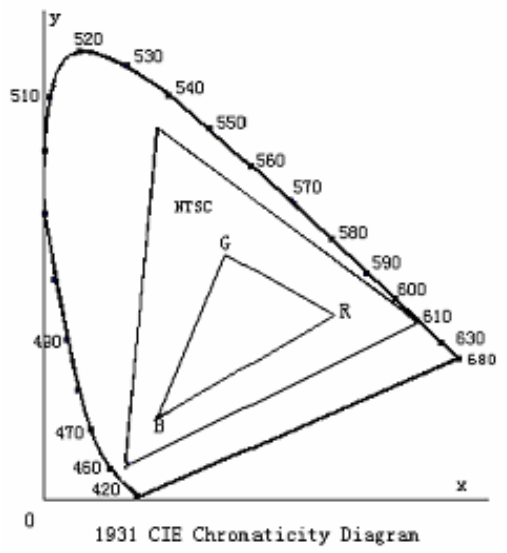
Note 4: Viewing angle range is defined as follow:

Viewing angle is measured at the center point of the LCD.



Note 5: Color chromaticity is defined as follow: (CIE1931)

Color coordinates measured at center point of LCD.

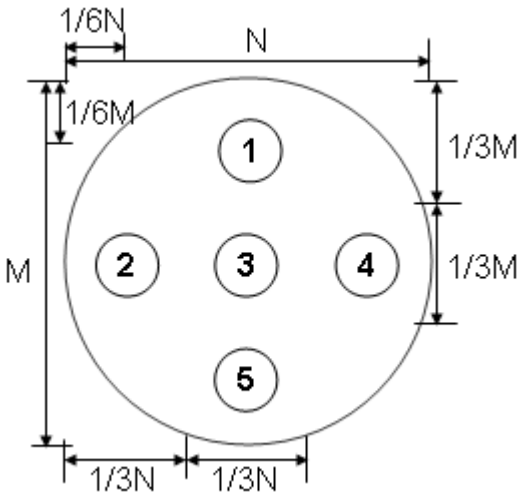


$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

Note 6: Luminance is defined as follow:

Luminance is defined as the brightness of all pixels "White" at the center of display area on optimum contrast.

Note 7: Uniformity. Refer to figure as below



- Bp = Bp (Min.) / Bp (Max.)×100 (%)
- Bp (Max.) = Maximum brightness in 5 measured spots
- Bp (Min.) = Minimum brightness in 5 measured spots.

Note 8:

Gamma spec. is based on Gray level 255, 250, 244, 240, 232, 224, 206, 192, 160, 128, 95, 63, 47 & 31.

Note 9: Flicker

The flicker level is defined using Fast Fourier Transformation (FTT) as follows:

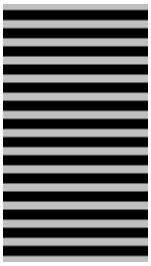
$$Flicker = 20\log_{10}\left(2\frac{f_{FFTC}(n)}{f_{FFTC}(0)}\right) + FS(Hz) \quad (dB)$$

where

fFFTC(n) is the nth FFT coefficient, and fFFTC(0) is the 0th FFT coefficient which is DC component. FS(Hz) is the flicker sensitivity as a function of frequency.

The flicker level shall be measured with the test pattern in below.

The gray leves of test pattern is 128.



Note 10: Cross-talk

• There should be no visible cross-talk in normal direction of the display when the two ”Cross-talk Test Patterns ” below are loaded.

• Measurement equipment: DMS-803 or similar equipments

• The point should be marked is, the background of Cross-talk Test Pattern-“gray “ are defined as middle gray scale . For example, RGB 24bit “gray” defined as below:

R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

•Bpn = Bpn (gray) / Bpn (white)

Which n means the dot No. In the Cross-talk Test Pattern ;

Bpn (gray) means the brightness of the No.n spots in Cross-talk Test Pattern A and B;

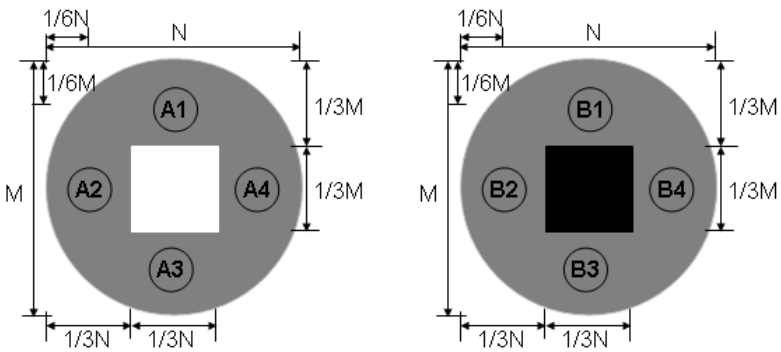
Bpn (white) means the brightness of the No.n spots in Full white Test Pattern;

•Bp (Max.) = Maximum value in A1~A4 and B1~B4.

•Bp (Min.) = Minimum value in A1~A4 and pB1~B4.

•CT=Bp (Max.)/Bp(Min.).

•CT must be less than 1.10



10. Environmental / Reliability Tests

No	Test Item	Condition	Judgment criteria
1	High Temp Operation	Ts=+60℃, 120hrs	Per table in below
2	Low Temp Operation	Ta=-20℃, 120hrs	Per table in below
3	High Temp Storage	Ta=+70℃, 120hrs	Per table in below
4	Low Temp Storage	Ta=-30℃, 120hrs	Per table in below
5	High Temp & High Humidity Storage	Ta=+65℃, 90% RH 96 hours	Per table in below (polarizer discoloration is excluded)
6	Thermal Shock (Non-operation)	-20°C ~70°C，Dwell for 30 min. 100 cycles	Per table in below
7	ESD (Operation)	Air discharge model, ±8kV, 10 times	Per table in below
8	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	Per table in below
9	Package Drop Test	Height: 80cm Sequence : 1 angleǵ 3 edges and 6 faces	Per table in below

INSPECTION	CRITERION(after test)
Appearance	No Crack on the FPC, on the OLED Panel
Alignment of OLED Panel	No Bubbles in the OLED Panel No other Defects of Alignment in Active area
Electrical current	Within device specifications Current consumption: within · 50% of initial value.
Function / Display	No Broken Circuit, No Short Circuit or No Black line No Other Defects of Display

11. Precautions for Use of OLED Modules

11.1 Safety

The liquid crystal in the OLED is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

11.2 Handling

A. The OLED and touch panel is made of plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
B. Do not handle the product by holding the flexible pattern portion in order to assure the reliability
C. Transparency is an important factor for the touch panel. Please wear clear finger sacks, gloves and mask to protect the touch panel from finger print or stain and also hold the portion outside the view area when handling the touch panel.
D. Provide a space so that the panel does not come into contact with other components.
E. To protect the product from external force, put a covering lens (acrylic board or similar board) and keep an appropriate gap between them.
F. Transparent electrodes may be disconnected if the panel is used under environmental conditions where dew condensation occurs.
G. Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in IC malfunctions.
H. To prevent such IC malfunctions, your design and mounting layout shall be done in the way that the IC is not exposed to light in actual use.

11.3 Static Electricity

A. Ground soldering iron tips, tools and testers when they are in operation.
B. Ground your body when handling the products.
C. Power on the OLED module before applying the voltage to the input terminals.
D. Do not apply voltage which exceeds the absolute maximum rating.
E. Store the products in an anti-electrostatic bag or container.

11.4Storage

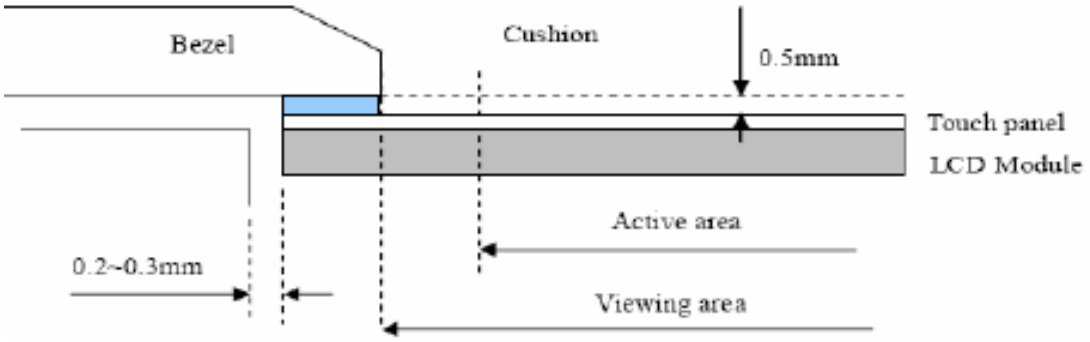
A. Store the products in a dark place at +25℃±10℃ with low humidity (40% RH to 60% RH). Don't expose to sunlight or fluorescent light.
B. Storage in a clean environment, free from dust, active gas, and solvent.

11.5 Cleaning

A. Do not wipe the touch panel with dry cloth, as it may cause scratch.
B. Wipe off the stain on the product by using soft cloth moistened with ethanol. Do not allow ethanol to get in between the upper film and the bottom glass. It may cause peeling issue or defective operation. Do not use any organic solvent or detergent other than ethanol.

11.6 Cautions for installing and assembling

Bezel edge must be positioned in the area between the Active area and View area. The bezel may press the touch screen and cause activation if the edge touches the active area. A gap of approximately 0.5mm is needed between the bezel and the top electrode. It may cause unexpected activation if the gap is too narrow. There is a tolerance of 0.2 to 0.3mm for the outside dimensions of the touch panel and tail. A gap must be made to absorb the tolerance in the case and connector.



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