# "ा山ll/ Microtips technology 

Model No: MTD0550AZOM-T-3

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## Record of Revision



1. Scope

This data sheet is to introduce the specification of MTD0550AZOM-T-3,AMOLED display module. It is composed of an AMOLED panel, driver IC, FPC and Capacitive touch panel. The 5.49 " display area contains $1080($ RGB ) x 1920 pixels.
2. Application

Digital equipments which need display, mobile phone, remote control, electronic product.
3. General Information

| Item | Contents | Unit |
| :--- | :--- | :--- |
| Size | 5.49 | inch |
| Resolution | $1080(\mathrm{RGB}) \times 1920$ | $/$ |
| Display Color | 16.7 M (RGBx8bits) |  |
| Interface | MIPI 4 lanes | mm |
| Pixel pitch | $0.0632 \times 0.0632$ | mm |
| Outline Dimension $(\mathrm{W} \times \mathrm{H} \times \mathrm{D})$ | $76.64 \times 140.74 \times 2.2$ | mm |
| Active Area(W $\times \mathrm{H})$ | $68.299 \times 121.421$ |  |
| Driver IC of AMOLED | RM 67191 |  |
| Controller of CTP | FT5436 |  |
| Polarizer | Hard Coating Polarizer |  |
| Operating Temperature | $-20^{\circ} \mathrm{C} \sim+60^{\circ} \mathrm{C}$ |  |
| Storage Temperature | $-30^{\circ} \mathrm{C} \sim+70^{\circ} \mathrm{C}$ |  |

## 4. Outline Drawing



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## 5. Interface signals

| No | Pin name | I/O | Description |
| :---: | :---: | :---: | :---: |
| 1 | NC | - | No connection |
| 2 | GND | Power | The power ground |
| 3 | NC | - | No connection |
| 4 | D3N | I/O | MIPI DSI data3- |
| 5 | NC | - | No connection |
| 6 | D3P | I/O | MIPI DSI data3+ |
| 7 | NC | - | No connection |
| 8 | GND | Power | The power ground |
| 9 | NC | - | No connection |
| 10 | DON | I/O | MIPI DSI data0- |
| 11 | NC | - | No connection |
| 12 | DOP | I/O | MIPI DSI data0+ |
| 13 | NC | - | No connection |
| 14 | GND | Power | The power ground |
| 15 | GND | Power | The power ground |
| 16 | CKN | 1 | MIPI DSI clock- |
| 17 | OLED_EN | 0 | Power IC enable |
| 18 | CKP | 1 | MIPI DSI clock+ |
| 19 | SWIRE | 0 | Power IC control pin |
| 20 | GND | Power | The power ground |
| 21 | TE | 0 | Tear effect output |
| 22 | D1N | I/O | MIPI DSI data1- |
| 23 | VDDIO | Power | Driver IC digital I/O supply |
| 24 | D1P | I/O | MIPI DSI data1+ |
| 25 | VSP | Power | PFM's Voltage |
| 26 | GND | Power | The power ground |
| 27 | VCl | Power | Driver IC analog supply |
| 28 | D2N | I/O | MIPI DSI data2- |
| 29 | RESX | 1 | This signal will reset the device and must be applied to properly initialize the chip. Active low. |
| 30 | D2P | I/O | MIPI DSI data2+ |
| 31 | VPP | Power | Power supply for OTP. <br> Leave the pin to open when not in use. |
| 32 | GND | Power | The power ground |
| 33 | GND | Power | The power ground |
| 34 | NC | - | No connection |
| 35 | ELVDD | Power | AMOLED power Positive |
| 36 | ELVSS | Power | AMOLED power Negative |
| 37 | ELVDD | Power | AMOLED power Positive |
| 38 | ELVSS | Power | AMOLED power Negative |
| 39 | ELVDD | Power | AMOLED power Positive |
| 40 | ELVSS | Power | AMOLED power Negative |

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CTP:

| PIN | Symbol | Description | Remark |
| :---: | :---: | :---: | :---: |
| 1 | REST | Reset Signal |  |
| 2 | EINT | Interrupt output Pin |  |
| 3 | SDA | Data input |  |
| 4 | SCL | Clock for the data input |  |
| 5 | VDD2V8 | Power supply |  |
| 6 | GND | Power Ground |  |

6. Absolute maximum Ratings
6.1 Electrical Absolute max. ratings

| Parameter | Symbol | MIN | MAX | Unit | Remark |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Analog/boost power voltage | VCI | -0.3 | 5.5 | V |  |
| VCI_IO voltage | VCI_IF | -0.3 | 5.5 | V |  |
| I/O voltage | VDDIO | -0.3 | 5.5 | V |  |
| VSP voltage | VSP | -0.3 | 6.6 | V |  |
| VPP(OTP power) | VPP | - | 8.64 | V |  |

6.2 Environment Conditions

| Item | Symbol | MIN | MAX | Unit | Remark |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Operating Temperature | TOPR | -20 | 60 | ${ }^{\circ} \mathrm{C}$ |  |
| Storage Temperature | TSTG | -30 | 70 | ${ }^{\circ} \mathrm{C}$ |  |

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## 7. Electrical Specifications

### 7.1 Electrical characteristics

| Item | Symbol | Min. | Typ. | Max. | Unit | Remark |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| AMOLED Power positive | ELVDD | - | 4.6 | - | V |  |
| AMOLED power Negative | ELVSS | - | -2.5 | - | V | Ref |
| Gamma Voltage | VSP | 6.3 | 6.4 | 6.5 | V | Ref |
| Digital Power supply | VDDIO | 1.65 | 1.8 | 3.6 | V | Ref |
| Analog Power supply | VCI | 2.5 | 3.3 | 4.8 | V | Ref |


| Mode | Symbol | Condition | Min. | Typ. | Max. | Unit | Remark |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 350 Nits @Full White | IELVDd/ELVSS | $\begin{gathered} \text { VELVDD }=4.6 \mathrm{~V} \\ \text { VELVSS }=-2.5 \mathrm{~V} \\ \text { VCI }=3.3 \mathrm{~V} \\ \text { VDDIO }=1.8 \mathrm{~V} \\ \text { VSP }=6.4 \mathrm{~V} \end{gathered}$ | - | 190 | 230 | mA | - |
|  | $\mathrm{I}_{\mathrm{VCl}}$ |  | - | 2 | 3 | mA | - |
|  | Ivddio |  | - | 50 | 55 | mA | - |
|  | IVSP |  | - | 15 | 20 | mA | - |
| Normal Operation | Iopr | MCLK=24MHz |  | 13.2 |  | mA | - |
| Monitor | Imon |  |  | 0.43 |  | mA | - |
| Sleep | Islp |  |  | 42 |  | uA | - |

### 7.2 Display Module Block Diagram


7.3 Application circuit


## 8. Command/AC Timing

### 8.1 AC Characteristics (MIPI)

8.1.1 HS Data Transmission Burst


### 8.1.2 HS Clock Transmission


8.1.3 Turnaround Procedure


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Module Name: MTD0550AZOM-T-3 Ver1.1
8.1.4 Timing Parameters

| Symbol | Description | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{T}_{\text {REOT }}$ | $30 \%-85 \%$ rise time and fall time | - | - | 35 | ns |
| $\mathrm{T}_{\text {clk-miss }}$ | Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX. | - | - | 60 | ns |
| $\mathrm{T}_{\text {Clk-Post }}$ | Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $\mathrm{T}_{\text {HS-tRall }}$ to the beginning of $\mathrm{T}_{\text {clk-TRALL }}$. | 60ns + 52*UI (For DCS) | - | - | ns |
| $\mathrm{T}_{\text {CLK-PRE }}$ | Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode. | 8 | - | - | ns |
| TClk-settle | Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of $\mathrm{T}_{\text {CLK-PRE }}$. | 95 | - | 300 | ns |
| Tclikterm-en | Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL, MAX. | Time for Dn to reach VTERM-EN |  | 38 | ns |
| $\mathrm{T}_{\text {HS-SEttLe }}$ | Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $\mathrm{T}_{\text {HSPREPARE }}$ | 85ns + 6*UI |  | $\begin{gathered} 145 \mathrm{~ns}+1 \\ 0 * \mathrm{UI} \end{gathered}$ | ns |
| $\mathrm{T}_{\text {EOt }}$ | Time from start of $\mathrm{T}_{\text {Hs-trail }}$ or $\mathrm{T}_{\text {CLK-TRAIL }}$ period to start of LP-11 state | - | - | $\begin{gathered} \text { 105ns+4 } \\ 8 * U I \end{gathered}$ | ns |
| $\mathrm{T}_{\text {HS-Exit }}(1)$ | time to drive LP-11 after HS burst | 100 | - | - | ns |
| Ths-prepare | Time to drive LP-00 to prepare for HS transmission | 40ns + 4*UI | - | $\begin{gathered} 85 \mathrm{~ns}+ \\ 6 * \mathrm{UI} \\ \hline \end{gathered}$ | ns |
| Ths-PREPARE + THs-zero | Ths-prepare + Time to drive HS-0 before the Sync sequence | $\begin{gathered} \hline 145 \mathrm{~ns}+ \\ 10^{*} \mathrm{UI} \\ \hline \end{gathered}$ | - | - | ns |
| THs-SKIP | Time-out at RX to ignore transition period of EoT | 40 | - | $\begin{gathered} \hline 55 \mathrm{~ns}+ \\ 4 * \mathrm{UI} \end{gathered}$ | ns |
| $\mathrm{T}_{\text {HS-trall }}$ | Time to drive flipped differential state after last payload data bit of a HS transmission burst | $60+4 * \mathrm{UI}$ | - | - | ns |
| TLPX | Length of any Low-Power state period | 50 | - | - | ns |
| Ratio $\mathrm{T}_{\text {LPX }}$ | Ratio of $\mathrm{T}_{\text {LPX(MASTER) }} / \mathrm{T}_{\text {LPS(SLAVE) }}$ between Master and Slave side | 2/3 | - | 3/2 | ns |
| $\mathrm{T}_{\text {TA,GET }}$ | Time to drive LP-00 by new TX | 5*TLPX | 5*TLPX | 5*TLPX | ns |
| $\mathrm{T}_{\text {TA-GO }}$ | Time to drive LP-00 after Turnaround Request | 4*TLPX | 4*TLPX | 4*TLPX | ns |
| $\mathrm{T}_{\text {TA-SURE }}$ | Time-out before new TX side starts driving | TLPX | - | 2*TLPX | ns |

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### 8.1.5 Timing requirements for RESETB

When RESETB of the reset pin equals to Low, it will be in the condition of reset.
When it is in the condition of reset, it will make the device recover the initial set.
However, in order to avoid the reset noise cause reset, there is a mechanism to judge about whether the reset is needed or not.

The closed interval of Low can be shown as the following.
(Test condition: VDDIO $=1.65 \mathrm{~V} \sim 3.6 \mathrm{~V}, \mathrm{VSS}=0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=-20^{\circ} \mathrm{C} \sim+85^{\circ} \mathrm{C}$ )

| Parameter | Symbol | Conditions | Spec |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min. | Typ. | Max. |  |
| Reset low pulse width | Trst | - | 20 | - | - | $\mu_{\mathrm{S}}$ |
| Table: Reset timing |  |  |  |  |  |  |
| RESETB |  |  |  |  |  |  |

Figure: Reset timing
8.2 Power on and Power off sequence
8.2.1 Power on sequence


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8.2.2 Power off sequence


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9. Optical Specification
$\mathrm{Ta}=25^{\circ} \mathrm{C}$

| Item |  | Symbol | Condition | Min | Typ. | Max. | Unit | Remark |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Contrast Ratio |  | CR | $\theta=0^{\circ}$ | 60000 | - | - |  | Note1 Note2 |
| View Angles |  | $\Theta$ | $\begin{gathered} \text { U/D/L/R } \\ \mathrm{CR} \geq 1000 \\ \hline \end{gathered}$ | 80 |  | - | Degree | Note 3 |
| Chromaticity | White | x | Without Polarizer | 0.28 | 0.30 | 0.32 |  | Note4, <br> Note1 |
|  |  | y |  | 0.30 | 0.32 | 0.34 |  |  |
|  | Red | X |  | 0.64 | 0.67 | 0.70 |  |  |
|  |  | y |  | 0.30 | 0.33 | 0.36 |  |  |
|  | Green | X |  | 0.16 | 0.20 | 0.24 |  |  |
|  |  | y |  | 0.68 | 0.72 | 0.76 |  |  |
|  | Blue | X |  | 0.10 | 0.13 | 0.16 |  |  |
|  |  | y |  | 0.03 | 0.06 | 0.09 |  |  |
| NTSC |  |  |  | 90 | 105 |  | \% |  |
| Brightness Uniformity |  |  | Full White | 75 |  |  | \% | Note6 |
| Luminance |  | L | Full White | 270 | 300 | 330 | $\mathrm{cd} / \mathrm{m}^{2}$ | Note1 <br> Note5 |

Note 1: Definition of optical measurement system.
Temperature $=25^{\circ} \mathrm{C}\left( \pm{ }^{\circ} \mathrm{C}\right)$
LED back-light: ON, Environment brightness < 150 Ix


Note 2: Contrast ratio is defined as follow:
Contrast Ratio $=\frac{\text { Surface Luminance with all white pixels }}{\text { Surface Luminance with all black pixels }}$

Note 3: Viewing angle range is defined as follow:
Viewing angle is measured at the center point of the LCD.


Note 4: Color chromaticity is defined as follow: (CIE1931)
Color coordinates measured at center point of LCD.


Note 5: Luminance is defined as follow:
Luminance is defined as the brightness of all pixels "White" at the center of display area on optimum contrast.

Note 6: Luminance Uniformity is defined as follow:
Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

## Uniformity $(\mathrm{U})=\frac{\text { Minimum Luminance(brightness) in } 9 \text { points }}{\text { Maximum Luminance(brightness) in } 9 \text { points }}$



Fig. 2 Definition of uniformity

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## 10. Environmental / Reliability Tests

| No | Test Item | Condition | Judgment criteria |
| :---: | :---: | :---: | :---: |
| 1 | High Temp Operation | Ts $=+60^{\circ} \mathrm{C}, 120 \mathrm{hrs}$ | Per table in below |
| 2 | Low Temp Operation | $\mathrm{Ta}=-20^{\circ} \mathrm{C}, 120 \mathrm{hrs}$ | Per table in below |
| 3 | High Temp Storage | Ta $=+70^{\circ} \mathrm{C}, 120 \mathrm{hrs}$ | Per table in below |
| 4 | Low Temp Storage | Ta $=-30^{\circ} \mathrm{C}, 120 \mathrm{hrs}$ | Per table in below |
| 5 | High Temp \& High Humidity Storage | $\mathrm{Ta}=+40^{\circ} \mathrm{C}, 90 \% \mathrm{RH}$ 120 hours | Per table in below (polarizer discoloration is excluded) |
| 6 | Thermal Shock (Non-operation) | $-30^{\circ} \mathrm{C} 30 \mathrm{~min} \sim+70^{\circ} \mathrm{C} 30 \mathrm{~min}$,  <br> Change time: $5 \mathrm{~min}, \quad 10$ <br> Cycles  | Per table in below |
| 7 | ESD (Operation) | $C=150 \mathrm{pF}, \quad \mathrm{R}=330 \Omega$ <br> 5points/panel <br> Air: $\pm 8 \mathrm{KV}$, 5times; <br> Contact: $\pm 4 \mathrm{KV}$, 5 times; | Per table in below |
| 8 | Vibration (Non-operation) | Frequency range:10~55Hz, Stroke:1.5mm <br> Sweep:10Hz~55Hz~10Hz 2 hours <br> for each direction of X.Y.Z. | Per table in below |
| 9 | Shock (Non-operation) | $60 \mathrm{G} 6 \mathrm{~ms}, \pm \mathrm{X}, \pm \mathrm{Y}, \pm \mathrm{Z}$ 3times, for each direction | Per table in below |
| 10 | Package Drop Test | Height:80 cm, 1 corner, 3 edges, 6 surfaces | Per table in below |


| INSPECTION | CRITERION(after test) |
| :--- | :--- |
| Appearance | No Crack on the FPC, on the OLED Panel |
| Alignment of OLED Panel | No Bubbles in the OLED Panel <br> No other Defects of Alignment in Active area |
| Electrical current | Within device specifications |
| Function / Display | No Broken Circuit, No Short Circuit or No Black line <br> No Other Defects of Display |

## 11. Precautions for Use of OLED Modules

### 11.1 Safety

The liquid crystal in the OLED is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

### 11.2 Handling

A. The OLED and touch panel is made of plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
B. Do not handle the product by holding the flexible pattern portion in order to assure the reliability
C. Transparency is an important factor for the touch panel. Please wear clear finger sacks, gloves and mask to protect the touch panel from finger print or stain and also hold the portion outside the view area when handling the touch panel.
D. Provide a space so that the panel does not come into contact with other components.
E. To protect the product from external force, put a covering lens (acrylic board or similar board) and keep an appropriate gap between them.
F. Transparent electrodes may be disconnected if the panel is used under environmental conditions where dew condensation occurs.
G. Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in IC malfunctions.
H. To prevent such IC malfunctions, your design and mounting layout shall be done in the way that the IC is not exposed to light in actual use.

### 11.3 Static Electricity

A. Ground soldering iron tips, tools and testers when they are in operation.
B. Ground your body when handling the products.
C. Power on the OLED module before applying the voltage to the input terminals.
D. Do not apply voltage which exceeds the absolute maximum rating.
E. Store the products in an anti-electrostatic bag or container.

### 11.4Storage

A. Store the products in a dark place at $+25^{\circ} \mathrm{C} \pm 0^{\circ} \mathrm{C}$ with low humidity ( $40 \% \mathrm{RH}$ to $60 \% \mathrm{RH}$ ). Don't expose to sunlight or fluorescent light.
B. Storage in a clean environment, free from dust, active gas, and solvent.

### 11.5 Cleaning

A. Do not wipe the touch panel with dry cloth, as it may cause scratch.
B. Wipe off the stain on the product by using soft cloth moistened with ethanol. Do not allow ethanol to get in between the upper film and the bottom glass. It may cause peeling issue or defective operation. Do not use any organic solvent or detergent other than ethanol.

### 11.6 Cautions for installing and assembling

Bezel edge must be positioned in the area between the Active area and View area. The bezel may press the touch screen and cause activation if the edge touches the active area. A gap of approximately 0.5 mm is needed between the bezel and the top electrode. It may cause unexpected activation if the gap is too narrow. There is a tolerance of 0.2 to 0.3 mm for the outside dimensions of the touch panel and tail. A gap must be made to absorb the tolerance in the case and connector.


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LPP5N00000 OLED-128Y032A-WPP3N00000 OLED-100H016A-WPP5N00000 OLED-100H016H-GPP5N00000 OLED-016O002B-
BPP5N00000 OLED-096Y064A-LPP3N00000 OLED-096O064A-BPP3N00000 OLED-128Y064C-LPP3N00000 OLED-096Y064B-
LPP3N00000 OLED-128Y032A-LPP3N00000 OLED-096Y064B-BPP3N00000 REX009616AWPP3N00000 REG010016FBPP5N00100
REG010016FGPP5N00100 REG010016FWPP5N00100 REG010032AWPP5N00100 REX064128AWPP3N0Y000 14747
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REG010016CRPP5N00000 REG010016DBPP5N00000 REG010016ERPP5N00000 REG010032BYPP5N00000 REX012832EWAP3N00000 DEP 100032A-W DEP 100032A-Y DEP 128064J-Y DEP 16202-Y DEP 20203-Y DEP 20401-Y 17009 OLED-016N002B-RPP5N00000 OLED-016N002B-WPP5N00000 OLED-016N002H-RPP5N00000 OLED-020N004B-WPP5N00000 OLED-100H008A-WPP5N00000 OLED-100H016B-BPP5N00000 OLED-100H016B-WPP5N00000

