MINGDA MICROELECTRONICS

MD8933
28V, 570KHz, 3A Step-Down Converter

FEATURES

- 3.5 to 28V Input Voltage Range
- Adjustable Output Voltage Down to 0.8V
- Integrated 60mΩ High-Side MOSFET Supports up to 3A Continuous Output Current
- High Efficiency at Light Loads With a Pulse Skipping Eco-mode™
- Fixed 570kHz Switching Frequency
- Typical 1μA Shutdown Quiescent Current
- Adjustable Slow-Start Limits Inrush Currents
- Programmable UVLO Threshold
- Overvoltage Transient Protection
- Cycle-by-Cycle Current Limit, Frequency Fold Back, and Thermal Shutdown Protection
- Available in Easy-to-Use SOP8 Package or Thermally Enhanced ESOP8 PowerPAD Package

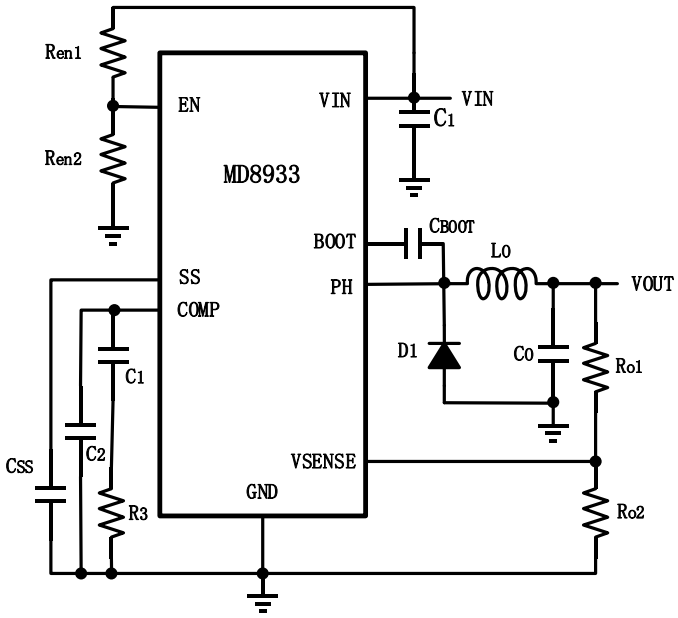
APPLICATIONS

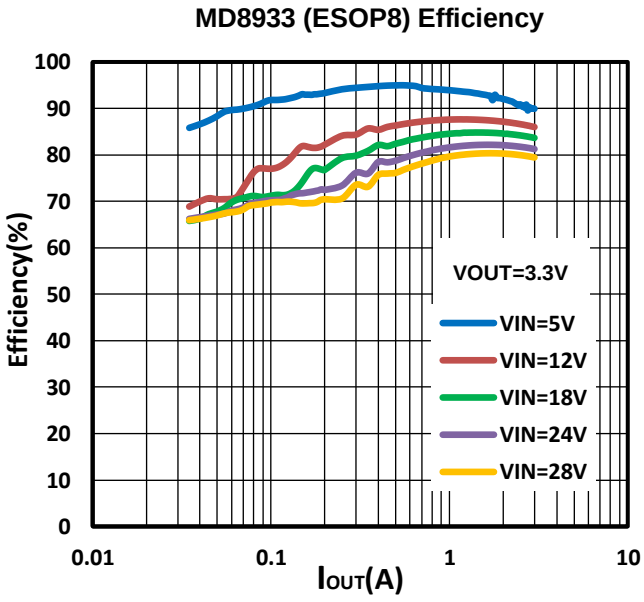
- Consumer Applications such as Set-Top Boxes, CPE Equipment, LCD Displays, Peripherals, and Battery Chargers
- Industrial and Car-Audio Power Supplies
- 5V, 12V, and 24V Distributed Power Systems

PRODUCT DESCRIPTION

The MD8933 device is a 28V, 3A non- synchronous buck converter that integrates a low RDS(on) high-side MOSFET. To increase efficiency at light loads, a pulse skipping Eco-mode feature is automatically activated. Furthermore, the 1μA shutdown supply-current allows the device to be used in battery-powered applications. Current mode control with internal slope compensation simplifies the external compensation calculations and reduces component count while allowing the use of ceramic output capacitors. A resistor divider programs the hysteresis of the input undervoltage lockout. An overvoltage transient protection circuit limits voltage overshoots during startup and transient conditions. A cycle-by-cycle current-limit scheme, frequency foldback and thermal shutdown protect the device and the load in the event of an overload condition. The MD8933 device is available in an 8-pin SOIC package and 8-pin SOIC PowerPAD package that have been internally optimized to improve thermal performance.

SIMPLIFIED SCHEMATIC

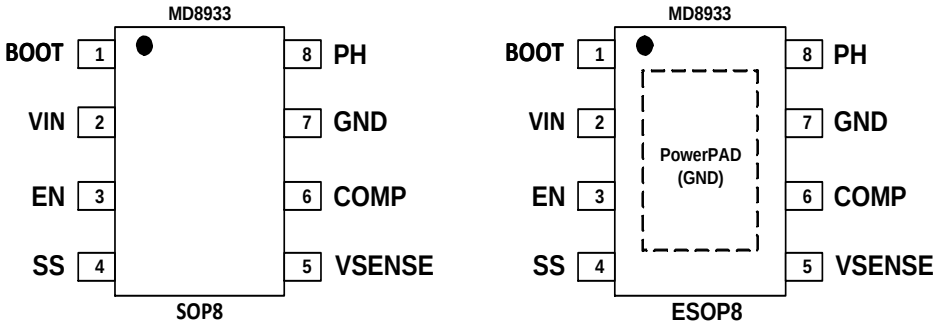




ORDER INFORMATION

Product Name	Package	Ordering Name	Marking	Package Information
MD8933	SOP8	MD8933ERF4	8933	Tape and Reel, 4000
MD8933	ESOP8	MD8933ESF4	8933	Tape and Reel, 4000

PACKAGE REFERENCE



Pin Functions

PIN		I/O	DESCRIPTION
NO	NAME		
1	BOOT	O	A 0.1μF bootstrap capacitor is required between the BOOT and PH pins. If the voltage on this capacitor falls below the minimum requirement, the high-side MOSFET is forced to switch off until the capacitor is refreshed.
2	VIN	I	This pin is the 3.5V to 28V input supply voltage.
3	EN	I	This pin is the enable pin. To disable, pull below 0.5V. Float this pin to enable. Programming the input undervoltage lockout with two resistors is recommended.
4	SS	I	This pin is slow-start pin. An external capacitor connected to this pin sets the output rise time.
5	VSENSE	I	This pin is the inverting node of the transconductance (gm) error amplifier.
6	COMP	O	This pin is the error-amplifier output and the input to the PWM comparator. Connect frequency compensation components to this pin.
7	GND	—	Ground pin
8	PH	O	The PH pin is the source of the internal high-side power MOSFET.
	PowerPAD	—	The PowerPAD is only available on the Esop8 package. For proper operation, the GND pin must be connected to the exposed pad

ABSOLUTE MAXI MUM RATINGS (Unless otherwise indicated: Ta=25℃)

			MIN	MAX	UNIT
Input voltage	VIN		-0.3	30	V
	EN		-0.3	6	
	BOOT			38	
	VSENSE		-0.3	3	
	COMP		-0.3	3	
	SS		-0.3	3	
Output voltage	BOOT-PH			8	V
	PH		-0.6	30	
	PH (10-ns transient from ground to negative peak)			-5	
Source current	EN			100	μA
	BOOT			100	mA
	VSENSE			10	μA
	PH			9	A
Sink current	VIN			9	A
	COMP			100	μA
	SS			200	
Operating Ambient Temperature	Topr		-40	150	°C
Storage temperature range	Tstg		-65	150	°C
ESD Protection	HBM		-2500	2500	V
	CDM		-2000	2000	
Package Thermal Parameter					
Power Dissipation	P_D	SOP8	1068		mW
		ESOP8	1500		
Thermal Resistance	$R_{\theta JA}$	SOP8	125		°C/W
		ESOP8	66		
Humidity sensitive level	MSL	3			

NOTE:

1) Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device.
2) These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied.
3) Exposure to absolute maximum rating conditions for extended periods may affect device reliability

ELECTRICAL CHARACTERISTICS

T_J= –40°C to 150°C, VIN = 3.5 to 28 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)					
Internal undervoltage lockout threshold	Rising and falling			3.5	V
Shutdown supply current	EN = 0V, VIN = 12V, –40°C to 85°C		1.2	4	µA
Operating – non-switching supply current	VSENSE = 0.85 V		100	190	µA
ENABLE AND UVLO (EN PIN)					
Enable threshold	Rising		1.2		V
Enable threshold	Falling			0.5	V
Input current	Enable rise threshold – 50mV		3.2		µA
Input current	Enable rise threshold + 50mV		3.5		µA
VOLTAGE REFERENCE					
Voltage reference		0.772	0.8	0.828	V
HIGH-SIDE MOSFET					
On resistance	BOOT-PH = 3V, VIN = 3.5V		66		mΩ
	BOOT-PH = 6V, VIN = 12V		60		
ERROR AMPLIFIER					
Error amplifier transconductance (gm)	–2µA < $I_{(COMP)}$ < 2µA, $V_{(COMP)}$ = 1V		90		µmhos
Error amplifier DC gain(1)	VSENSE = 0.8V		800		V/V
Error amplifier unity gain bandwidth(1)	5pF capacitance from COMP to GND pins		2.7		MHz
Error amplifier source/sink current	$V_{(COMP)}$ = 1V, 100-mV overdrive		±8		µA
Switch current to COMP transconductance	VIN = 12V		10		A/V
PULSE SKIPPING ECO-MOD					
Pulse skipping Eco-mode switch current threshold			220		mA
CURRENT LIMIT					
Current-limit threshold	VIN = 12V	3.5	5.0		A
THERMAL SHUTDOWN					
Thermal Shutdown			165		°C
SLOW START (SS PIN)					
Charge current	$V_{(SS)}$ = 0.4V		2		µA
SS to VSENSE matching	$V_{(SS)}$ = 0.4V		-35		mV
SLOW START (SS PIN)					
Switching Frequency	VIN = 12V	456	570	684	KHz
Minimum controllable on time	VIN = 12V		160	200	ns
Maximum controllable duty ratio(1)	BOOT-PH = 6V	90%	93%		

(1) Specified by design

TYPICAL PERFORMANCE CHARACTERISTICS

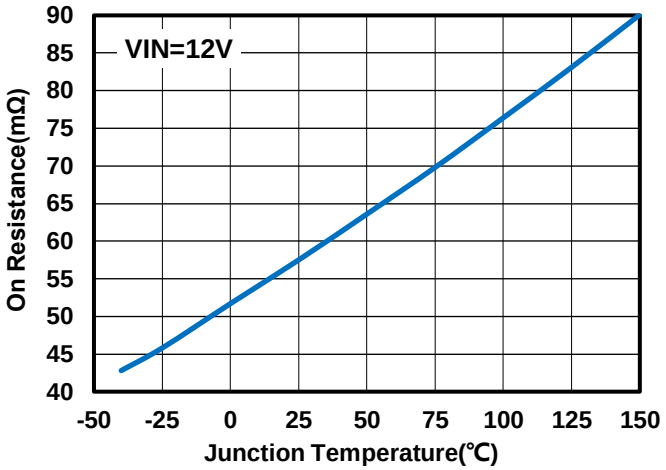


Figure 1.ON Resistance vs Junction Temperature

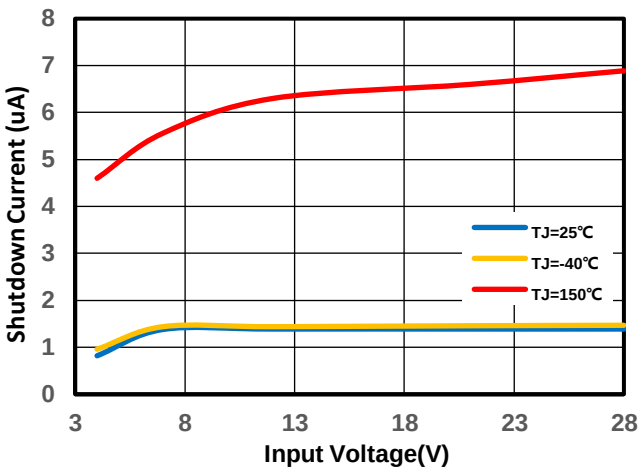


Figure 2.Shutdown Quiescent Current vs Input Voltage

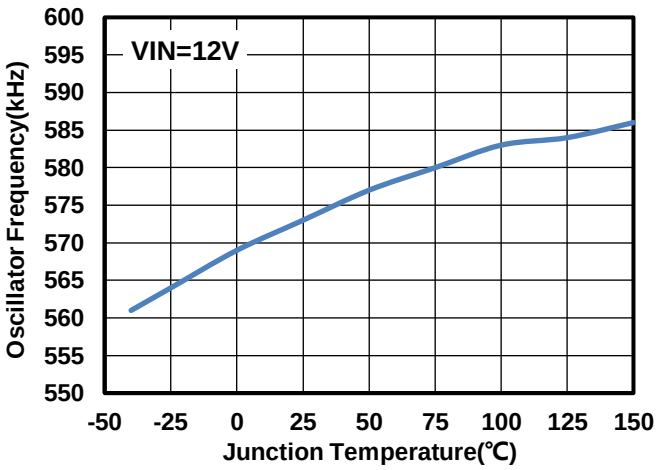


Figure 3.Oscillator Frequency vs Junction Temperature

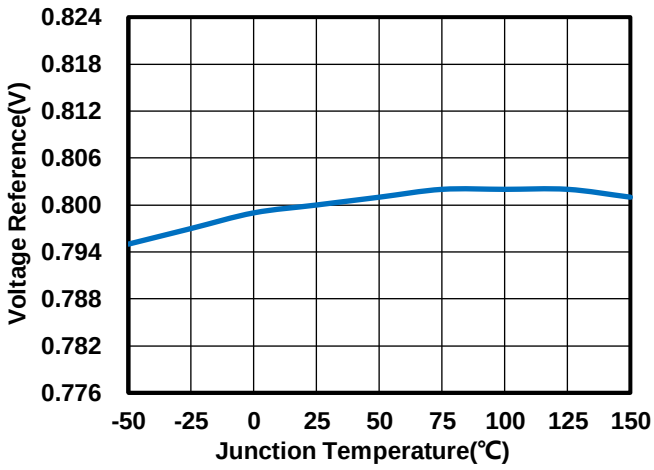


Figure 4.Voltage Reference vs Junction Temperature

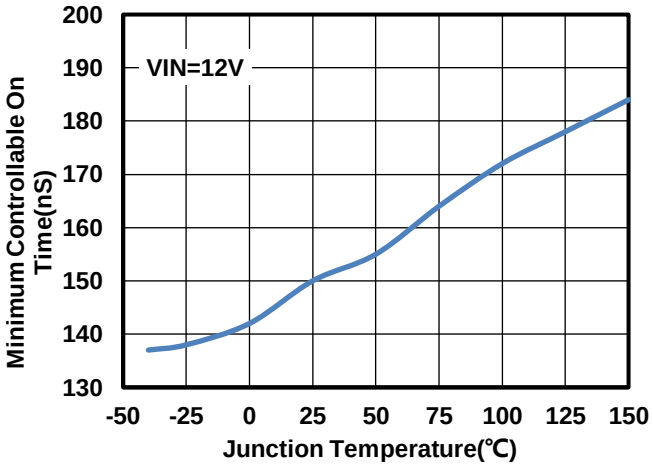


Figure 5.Minimum Controllable ON Time vs Junction Temperature

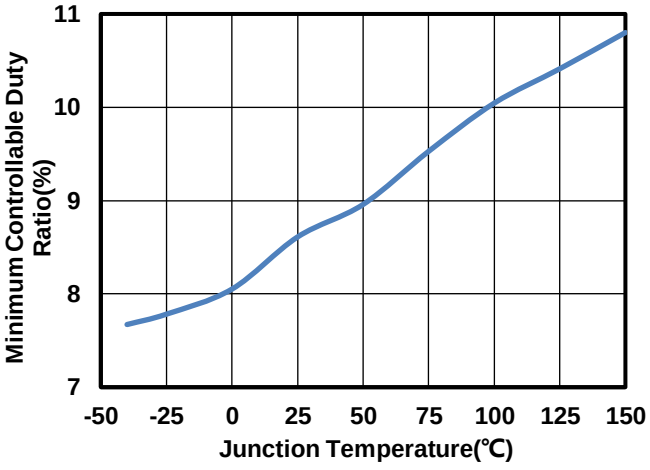


Figure 6.Minimum Controllable Duty Ratio vs Junction Temperature

TYPICAL PERFORMANCE CHARACTERISTICS（CONTINUED）

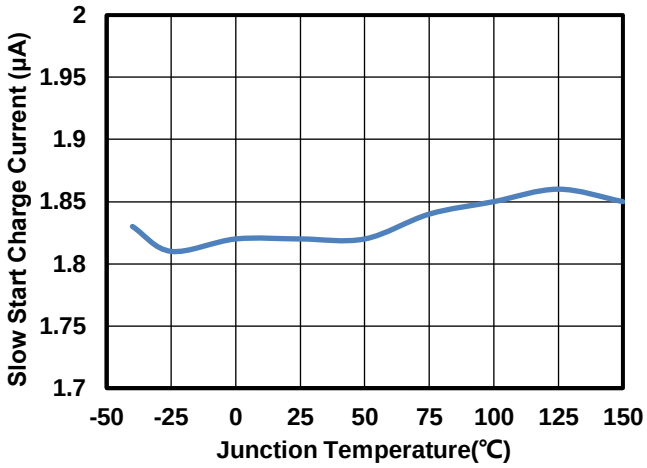


Figure 7.SS Charge Current vs Junction Temperature

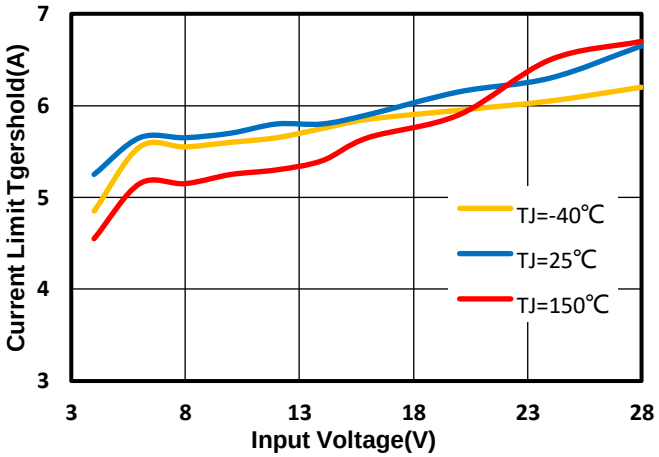


Figure 8.Current-Limit Threshold vs Input Voltage

DETAILED DESCRIPTION

Overview

The MD8933 device is a 28V, 3A, step-down (buck) converter with an integrated high-side n-channel MOSFET. To improve performance during line and load transients, the device implements a constant-frequency,current mode control which reduces output capacitance and simplifies external frequency compensation design.The MD8933 device has a preset switching frequency of 570kHz.

The MD8933 device requires a minimum input voltage of 3.5V for normal operation. The EN pin has an internal pullup current source that can adjust the input-voltage undervoltage lockout (UVLO) with two external resistors. In addition, the pullup current provides a default condition when the EN pin is floating for the device to operate. The operating current is 100μA (typical) when not switching and under no load. When the device is disabled, the supply current is 1.2μA (typical).

The integrated 60mΩ high-side MOSFET allows for high-efficiency power-supply designs with continuous output currents up to 3A.

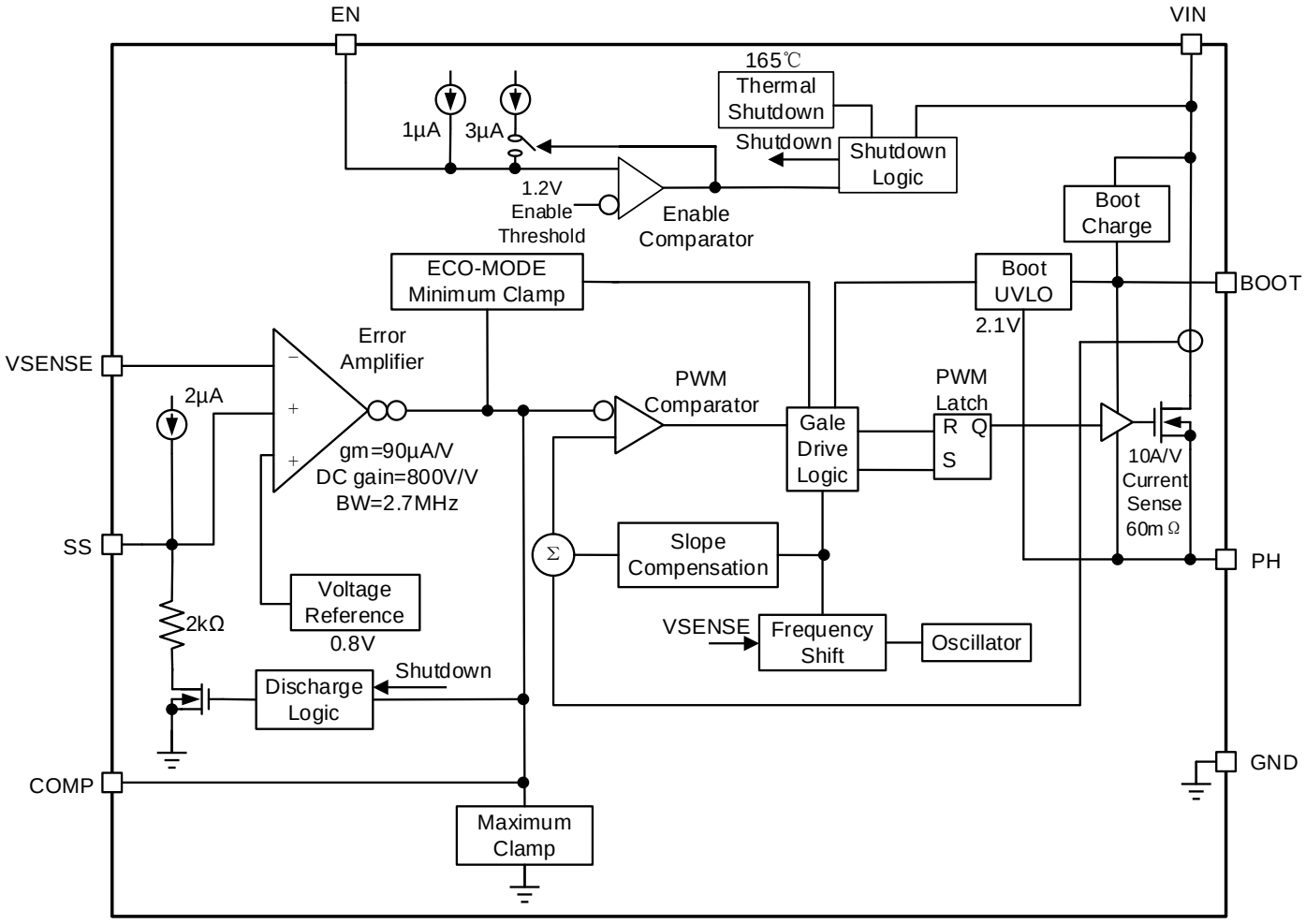
The MD8933 device reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by an external capacitor on the BOOT to PH pin. The boot capacitor voltage is monitored by an UVLO circuit and turns the high-side MOSFET off when the voltage falls below a preset threshold of 2.1V (typical). The output voltage can be stepped down to as low as the reference voltage.

By adding an external capacitor, the slow-start time of the MD8933 device can be adjustable which enables flexible output filter selection.

To improve the efficiency at light load conditions, the MD8933 device enters a special pulse skipping Eco-mode when the peak inductor current drops below 200mA (typical).

The frequency foldback reduces the switching frequency during startup and overcurrent conditions to help control the inductor current. The thermal shutdown provides additional protection under fault condition

FUNCTION BLOCK DIAGRAM



FEATURE DESCRIPTION

Fixed-Frequency PWM Control

The MD8933 device uses a fixed-frequency, peak-current mode control. The internal switching frequency of the MD8933 device is fixed at 570kHz

Voltage Reference (Vref)

The voltage reference system produces a ±2% initial accuracy voltage reference (±3.5% over temperature) by scaling the output of a temperature-stable bandgap circuit. The typical voltage reference is designed at 0.8V.

Bootstrap Voltage (BOOT)

The MD8933 device has an integrated boot regulator and requires a 0.1μF ceramic capacitor between the BOOT and PH pins to provide the gate-drive voltage for the high-side MOSFET. A ceramic capacitor with an X7R or X5R grade dielectric is recommended because of the stable characteristics over temperature and voltage. To improve drop out, the MD8933 device is designed to operate at 100% duty cycle as long as the BOOT-to-PH pin voltage is greater than 2.1V (typical).

Feature Description (continued)

Enable and Adjustable Input Undervoltage Lockout (VIN UVLO)

The EN pin has an internal pullup current-source that provides the default condition of the device while operating when the EN pin floats.

The MD8933 device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. Using an external VIN UVLO to add hysteresis is recommended unless the VIN voltage is greater than (VOUT + 2V). To adjust the VIN UVLO with hysteresis, use the external circuitry connected to the EN pin as shown in Figure 9.When the EN pin voltage exceeds 1.2V, an additional 3μA of hysteresis is added. Use Equation 1 and Equation 2 to calculate the resistor values required for the desired VIN UVLO threshold voltages. The V_{STOP} threshold should always be greater than 3.5V.

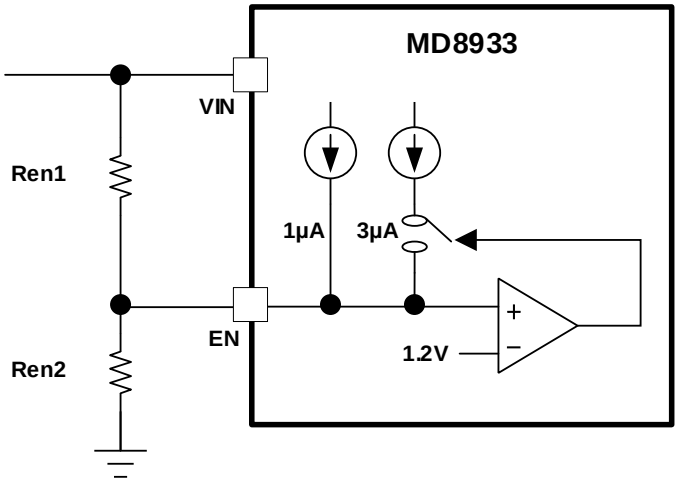


Figure 9. Adjustable Input Undervoltage Lockout

$$Ren1=\frac{V_{START}-V_{STOP}}{3\mu A} \quad (1)$$

where

- V_{START} is the input start threshold voltage
- V_{STOP} is the input stop threshold voltage

$$Ren2=\frac{V_{EN}}{\frac{V_{START}-V_{EN}}{Ren1}+1\mu A} \quad (2)$$

where

- V_{EN} is the enable threshold voltage of 1.2V

Feature Description (continued)

Programmable Slow Start Using SS Pin

Programming the slow-start time externally is highly recommended because no slow-start time is implemented. The MD8933 device effectively uses the lower voltage of the internal voltage reference or the SS pin voltage as the reference voltage of the power supply that is fed into the error amplifier and regulates the output accordingly. A capacitor (C_{SS}) on the SS pin to ground implements a slow-start time.The MD8933 device has an internal pullup current-source of 2μA that charges the external slow-start capacitor. Use Equation 3 to calculate the slow-start time (10% to 90%).

$$T_{SS}(ms)=\frac{C_{ss}(nF)\times V_{ref}(V)}{I_{SS}(\mu A)}$$

where

- Vref = 0.8V
- I_{SS} = 2μA （3）

The slow-start time should be set between 1ms to 10ms to ensure good startup behavior. The value of the slow-start capacitor should not exceed 27nF.

During normal operation, the MD8933 device stops switching if the input voltage drops below the VIN UVLO threshold, the EN pin is pulled below 0.5V, or a thermal shutdown event occurs.

Error Amplifier

The MD8933 device has a transconductance amplifier for the error amplifier. The error amplifier compares the VSENSE voltage to the internal effective voltage reference presented at the input of the error amplifier. The transconductance of the error amplifier is 90μA/V during normal operation. Frequency compensation components are connected between the COMP pin and ground.

Slope Compensation

To prevent the sub-harmonic oscillations when operating the device at duty cycles greater than 50%, the MD8933 device adds a built-in slope compensation which is a compensating ramp to the switch-current signal.

Current-Mode Compensation Design

To simplify design efforts using the MD8933 device, the typical designs for common applications are listed in Table 1. For designs using ceramic output capacitors, proper derating of ceramic output capacitance is recommended when performing the stability analysis because the actual ceramic capacitance drops considerably from the nominal value when the applied voltage increases. See the Detailed Design Procedure section for the detailed guidelines

Feature Description (continued)

Table 1. Typical Designs (Refer to the Simplified Schematic)

VIN (V)	VOUT (V)	Fsw (kHz)	L_O (μH)	C_O	R_{O1} (kΩ)	R_{O2} (kΩ)	C_2 (pF)	C_1 (pF)	R_3 (kΩ)
12	5	570	6.8	Ceramic 33 μF, ×2	10	1.91	39	4700	49.9
12	3.3	570	6.8	Ceramic 47μF, ×2	10	3.24	47	1000	29.4
12	1.8	570	4.7	Ceramic 100 μF	10	8.06	68	5600	29.4
12	0.9	570	3.3	Ceramic 100 μF, ×2	10	80.6	56	5600	29.4
12	5	570	6.8	Aluminum 330 μF, 160 mΩ	10	1.91	68	120	29.4
12	3.3	570	6.8	Aluminum 470 μF, 160 mΩ	10	3.24	82	220	10
12	1.8	570	4.7	SP 100 μF, 15 mΩ	10	8.06	68	5600	29.4
12	0.9	570	3.3	SP 330 μF, 12 mΩ	10	80.6	100	1200	49.9

Overcurrent Protection and Frequency Shift

The MD8933 device implements current mode control that uses the COMP pin voltage to turn off the high-side MOSFET on a cycle-by-cycle basis. During each cycle the switch current and the COMP pin voltage are compared. When the peak inductor current intersects the COMP pin voltage, the high-side switch is turned off.During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, causing the switch current to increase. The COMP pin has a maximum clamp internally, which limit the output current.

The MD8933 device provides robust protection during short circuits. Overcurrent runaway is possible in the output inductor during a short circuit at the output. The MD8933 device solves this issue by increasing the off time during short-circuit conditions by lowering the switching frequency. The switching frequency is divided by 1,2, 4, and 8 as the voltage ramps from 0 to 0.8 V on VSENSE pin. The relationship between the switching frequency and the VSENSE pin voltage is listed in Table 2.

Table 2. Switching Frequency Conditions

SWITCHING FREQUENCY	VSENSE PIN VOLTAGE
570kHz	VSENSE ⩾ 0.6V
570kHz / 2	0.6V > VSENSE ⩾ 0.4V
570kHz / 4	0.4V > VSENSE ⩾ 0.2V
570kHz / 8	0.2V > VSENSE

Overvoltage Transient Protection

The MD8933 device incorporates an overvoltage transient-protection (OVTP) circuit to minimize output voltage overshoot when recovering from output fault conditions or strong unload transients. The OVTP circuit includes an overvoltage comparator to compare the VSENSE pin voltage and internal thresholds. When the VSENSE pin voltage goes above 109% × Vref , the high-side MOSFET is forced off. When the VSENSE pin voltage falls below 107% × Vref , the high-side MOSFET is enabled again.

Thermal Shutdown

The device implements an internal thermal shutdown to protect the device if the junction temperature exceeds 165°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. When the die temperature decreases below 165°C, the device reinitiates the power-up sequence

DEVICE FUNCTIONAL MODES

Eco-mode

The MD8933 device is designed to operate in pulse skipping Eco-mode at light load currents to boost light load efficiency. When the peak inductor current is lower than 220mA (typical), the COMP pin voltage falls to 0.5 V(typical) and the device enters Eco-mode. When the device is in Eco-mode, the COMP pin voltage is clamped at 0.5 V internally which prevents the high-side integrated MOSFET from switching. The peak inductor current must rise above 220mA for the COMP pin voltage to rise above 0.5V and exit Eco-mode. Because the integrated current comparator catches the peak inductor current only, the average load current entering Eco-mode varies with the applications and external output filters.

Operation With V IN < 3.5 V

The device is recommended to operate with input voltages above 3.5V. The typical VIN UVLO threshold is not specified and the device can operate at input voltages down to the UVLO voltage. At input voltages below the actual UVLO voltage, the device does not switch. If the EN pin is externally pulled up or left floating, the device becomes active when the VIN pin passes the UVLO threshold. Switching begins when the slow-start sequence is initiated.

Operation With EN Control

The enable threshold voltage is 1.2V (typical), When the EN pin is below 0.5V, the device is disabled and switching is inhibited even if the VIN pin is above the UVLO threshold, The IC quiescent current is reduced in this state. If the EN voltage increases above the threshold while the VIN pin is above the UVLO threshold, the device becomes active. Switching is enabled, and the slow-start sequence is initiated. Between 0.5V and 1.2V, the device output voltage is below its design value.

APPLICATION AND IMPLEMENTATION

NOTE

Information in the following applications sections is not part of the MD component specification, and MD does not warrant its accuracy or completeness. Customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Typical Application

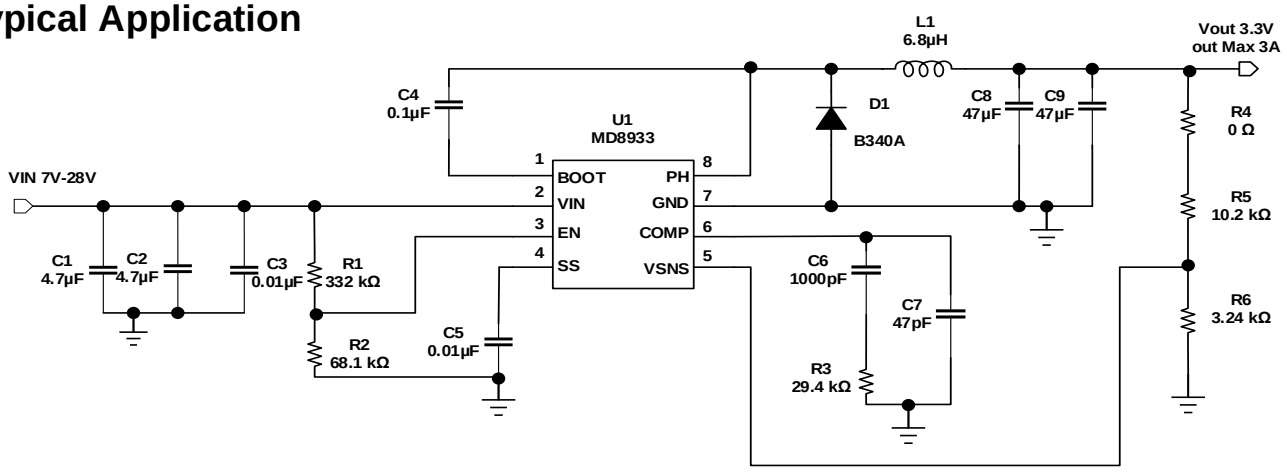


Figure 10. Typical Application Schematic

Design Requirements

For this design example, use the values listed in Table 3 as the input parameters.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	7 to 28 V
Output voltage	3.3 V
Input ripple voltage	300 mV
Output ripple voltage	30 mV
Output current rating	3 A
Operating Frequency	570 kHz

Detailed Design Procedure

The following design procedure can be used to select component values for the MD8933 device.

■ Switching Frequency

The switching frequency for the MD8933 device is fixed at 570kHz.

■ Output Voltage Set Point

The output voltage of the MD8933 device is externally adjustable using a resistor divider network. As shown in Figure 10, this divider network is comprised of R5 and R6. The relationship of the output voltage to the resistor divider is given by Equation 4 and Equation 5..

$$R6=\frac{R5\times V_{ref}}{V_{OUT}-V_{ref}} \quad (4)$$

$$V_{OUT}=V_{ref}\times\left[\frac{R5}{R6}+1\right] \quad (5)$$

Select a value of R5 to be approximately 10 kΩ. Slightly increasing or decreasing the value of R5 can result in closer output-voltage matching when using standard value resistors. In this design, R5 = 10.2kΩ and R6 = 3.24kΩ, resulting in a 3.31V output voltage. The 0Ω resistor, R4, is provided as a convenient location to break the control loop for stability testing.

■ Input Capacitors

The MD8933 device requires an input decoupling capacitor and depending on the application, a bulk input capacitor. The typical recommended value for the decoupling capacitor is 10 µF. A high-quality ceramic type X5R or X7R is recommended. The voltage rating should be greater than the maximum input voltage. A smaller value can be used as long as all other requirements are met; however a value of 10µF has been shown to work well in a wide variety of circuits. Additionally, some bulk capacitance may be required, especially if the MD8933 circuit is not located within about 2 inches from the input voltage source. The value for this capacitor is not critical but should be rated to handle the maximum input voltage including ripple voltage, and should filter the output so that input ripple voltage is acceptable. For this design two 4.7µF capacitors are used for the input decoupling capacitor. The capacitors are X7R dielectric rated for 50V. The equivalent series resistance (ESR) is approximately 2mΩ and the current rating is 3A. Additionally, a small 0.01µF capacitor is included for high frequency filtering.

Use Equation 6 to calculate the input ripple voltage.

$$\Delta VIN=\frac{I_{O(MAX)}\times 0.25}{C_{BULK}\times f_{SW}}+(I_{O(MAX)}\times ESR_{MAX})$$

where

- $I_{OUT(MAX)}$ is the maximum load current.
- f_{SW} is the switching frequency.
- C_{BULK} is the bulk capacitor value.
- ESR_{MAX} is the maximum series resistance of the bulk capacitor. （6）

The maximum RMS ripple current must also be checked. For worst case conditions, use Equation 7 to calculate the maximum-RMS input ripple current, $I_{CIN(RMS)}$.

$$I_{CIN(RMS)}=\frac{I_{O(MAX)}}{2} \quad （7）$$

In this case, the input ripple voltage is 143mV and the RMS ripple current is 1.5A.

NOTE

The actual input voltage ripple is greatly affected by parasitics associated with the layout and the output impedance of the voltage source.

The actual input voltage ripple for this circuit is listed in Table 3 and is larger than the calculated value. This measured value is still below the specified input limit of 300mV. The maximum voltage across the input capacitors would be V IN(MAX) + ΔV IN / 2. The selected bulk and bypass capacitors are each rated for 50V and the ripple current capacity is greater than 3A, both providing ample margin. The maximum ratings for voltage and current must not be exceeded under any circumstance.

■ Output Filter Components

Two components must be selected for the output filter, L1 and C2. Because the MD8933 device is an externally compensated device, a wide range of filter component types and values can be supported.

● Inductor Selection

To calculate the minimum value of the output inductor, use Equation 8.

$$L_{MIN}=\frac{V_{OUT(MAX)}\times (V_{IN(MAX)}-V_{OUT})}{V_{IN(MAX)}\times K_{IND}\times I_{OUT}\times f_{SW}}$$

where

- K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. （8）

In general, this value is at the discretion of the designer; however, the following guidelines may be used. For designs using low-ESR output capacitors, such as ceramics, a value as high as K_{IND} = 0.3 may be used. When using higher ESR output capacitors, K_{IND} = 0.2 yields better results.

For this design example, use K_{IND} = 0.3 and the minimum inductor value is calculated as 5.7μH. For this design, a large value was selected: 6.8μH.

For the output filter inductor, do not exceed the RMS current and saturation current ratings. Use Equation 9 to calculate the inductor ripple current (I_{LPP}).

$$I_{LPP}=\frac{V_{OUT}\times (V_{IN(MAX)}-V_{OUT})}{V_{IN(MAX)}\times L_{OUT}\times f_{SW}\times 0.8} \quad （9）$$

Use Equation 10 to calculate the RMS inductor current.

$$I_{LPP(RMS)}=\sqrt{I^2_{OUT(MAX)}+\frac{1}{2}+I^2_{LPP}} \quad （10）$$

Use Equation 11 to calculate the peak inductor current.

$$I_{L(PK)}=I_{OUT(MAX)}+\frac{I_{LPP}}{2} \quad (11)$$

For this design, the RMS inductor current is 3.01A and the peak inductor current is 3.47A. The selected inductor is a Sumida CDRH103-6R8, 6.8μH. This inductor has a saturation current rating of 3.84A and an RMS current rating of 3.6A, which meets these requirements. Smaller or larger inductor values can be used depending on the amount of ripple current the designer wants to allow, so long as the other design requirements are met. Larger value inductors will have lower AC current and result in lower output voltage ripple, while smaller inductor values will increase AC current and output voltage ripple. In general, inductor values for use with the MD8933 device are in the range of 6.8 to 47μH.

■ Capacitor Selection

The important design factors for the output capacitor are DC voltage rating, ripple current rating, and equivalent series resistance (ESR). The DC voltage and ripple current ratings cannot be exceeded. The ESR is important because along with the inductor current it determines the amount of output ripple voltage. The actual value of the output capacitor is not critical, but some practical limits do exist. Consider the relationship between the desired closed-loop crossover frequency of the design and LC corner frequency of the output filter. In general, keeping the closed-loop crossover frequency at less than 1/5 of the switching frequency is desired. With high switching frequencies such as the 570kHz frequency of this design, internal circuit limitations of the MD8933 device limit the practical maximum crossover frequency to about 25 kHz. In general, the closed-loop crossover frequency should be higher than the corner frequency determined by the load impedance and the output capacitor. Use Equation 12 to calculate the limits of the minimum capacitor value.

$$C_{O(MIN)}=1/(2\times\pi\times R_O\times F_{CO(MAX)})$$

where

- R_O is the output load impedance (V_O / I_O).
- $F_{CO(MAX)}$ is the desired crossover frequency. (12)

For a desired maximum crossover of 25kHz the minimum value for the output capacitor is approximately 5.8 μF. This value may not satisfy the output ripple voltage requirement. The output ripple voltage consists of two components; the voltage change because of the charge and discharge of the output filter capacitance and the voltage change because the ripple current times the ESR of the output filter capacitor. Use Equation 13 to estimate the output ripple voltage.

$$V_{OPP}=I_{LPP}\left[\frac{(D-0.5)}{4\times f_{SW}\times C_O}+R_{ESR}\right] \quad (13)$$

The maximum ESR of the output capacitor can be determined from the amount of allowable output ripple as specified in the initial design parameters. The contribution to the output ripple voltage because the ESR is the inductor ripple current times the ESR of the output filter. Therefore, use Equation 14 to calculate the maximum specified ESR as listed in the capacitor data sheet.

$$ESR_{MAX}=\frac{V_{OPP(MAX)}}{I_{LPP}}-\frac{(D-0.5)}{4\times f_{SW}\times C_O}$$

where

- $V_{OPP(MAX)}$ is the desired maximum peak-to-peak output ripple. (14)

Use Equation 15 to calculate the maximum RMS ripple current.

$$I_{COUT(RMS)}=\frac{1}{\sqrt{2}}\times\left(\frac{V_{OUT}\times(V_{IN(MAX)}-V_{OUT})}{V_{IN(MAX)}\times L_{OUT}\times f_{SW}\times N_C}\right)$$

where

• N_C is the number of output capacitors in parallel. （15）

For this design example, two 47μF ceramic output capacitors are selected for C8 and C9. These capacitors are TDK C3216X5R0J476MT, rated at 6.3V with a maximum ESR of 2mΩ and a ripple current rating in excess of 3AThe calculated total RMS ripple current is 161mA (80.6mA each) and the maximum total ESR required is 43mΩ. These output capacitors exceed the requirements by a wide margin and result in a reliable, high-performance design.

NOTE

The actual capacitance in circuit may be less than the catalog value when the output is operating at the desired output of 3.3V.

The selected output capacitor must be rated for a voltage greater than the desired output voltage plus half of the ripple voltage. Any derating amount must also be included. Other capacitor types work well with the MD8933 device, depending on the needs of the application.

■ Compensation Components

The external compensation used with the MD8933 device allows for a wide range of output filter configurations. A large range of capacitor values and types of dielectric are supported. The design example uses ceramic X5R dielectric output capacitors, but other types are supported. A Type II compensation scheme is recommended for the MD8933 device. The compensation components are selected to set the desired closed-loop crossover frequency and phase margin for output filter components. The Type II compensation has the following characteristics: a DC gain component, a low frequency pole, and a midfrequency zero-pole pair.

Use Equation 16 to calculate the DC gain.

$$G_{DC} = \frac{V_{ggm} \times V_{REF}}{V_O}$$

where

• V_{ggm} = 800.

• V_{REF} = 0.8V. （16）

Use Equation 17 to calculate the low-frequency pole.

$$V_{PO} = 1/(2 \times \pi \times R_{OO} \times C_Z) \quad （17）$$

Use Equation 18 to calculate the mid-frequency zero.

$$F_{Z1} = 1/(2 \times \pi \times R_Z \times C_Z) \quad （18）$$

Use Equation 19 to calculate the mid-frequency pole

$$V_{P1} = 1/(2 \times \pi \times R_Z \times C_P) \quad （19）$$

The first step is to select the closed-loop crossover frequency. In general, the closed-loop crossover frequency should be less than 1/8 of the minimum operating frequency. However, for the MD8933 device, not exceeding 25 kHz for the maximum closed-loop crossover frequency is recommended. The second step is to calculate the required gain and phase boost of the crossover network. By definition, the gain of the compensation network must be the inverse of the gain of the modulator and output filter. For this design example, where the ESR zero is much higher than the closed-loop crossover frequency, the gain of the modulator and output filter can be approximated by Equation 20.

$$Gain = -20 \log(2 \times \pi \times R_{SENSE} \times F_{CO} \times C_O)$$

where

• R_{SENSE} = 1Ω / 12.

• F_{CO} = Closed-loop crossover frequency.

• C_O = Output capacitance. （20）

Use Equation 21 to calculate the phase loss.

$$PL = a\tan(2 \times \pi \times F_{CO} \times R_{ESR} \times C_O) - a\tan(2 \times \pi \times F_{CO} \times R_O \times C_O)$$

where

- R_{ESR} = Equivalent series resistance of the output capacitor.
- $R_O = V_O / I_O$. (21)

The actual closed-loop crossover frequency is higher than intended at about 25kHz which is primarily because variation in the actual values of the output filter components and tolerance variation of the internal feed-forward gain circuitry. Overall, the design has greater than 60 degrees of phase margin and will be completely stable over all combinations of line and load variability.

Now that the phase loss is known, the required amount of phase boost to meet the phase margin requirement can be determined. Use Equation 22 to calculate the required phase boost.

$$PB = (PM - 90\,\mathrm{deg}) - PL$$

where

- PM = the desired phase margin. (22)

A zero-pole pair of the compensation network will be placed symmetrically around the intended closed-loop frequency to provide maximum phase boost at the crossover point. The amount of separation can be calculated with Equation 23. Use Equation 24 and Equation 25 to calculate the resultant zero and pole frequencies.

$$k = \tan\left(\frac{PB}{2} + 45\mathrm{deg}\right) \quad (23)$$

$$F_{Z1} = \frac{F_{CO}}{k} \quad (24)$$

$$F_{P1} = F_{CO} \times k \quad (25)$$

The low-frequency pole is set so that the gain at the crossover frequency is equal to the inverse of the gain of the modulator and output filter. Because of the relationships established by the pole and zero relationships, use Equation 26 to calculate the value of R_Z .

$$RZ = \frac{2 \times \pi \times F_{CO} \times C_O \times R_{OA}}{GM_{ICOMP} \times V_{ggm} \times V_{REF}}$$

where

- V_O = Output voltage.
- C_O = Output capacitance.
- F_{CO} = Desired crossover frequency.
- R_{OA} = 8 MΩ.
- GM_{COMP} = 10A/V.
- Vggm = 800.
- V_{REF} = 0.8V. (26)

With the value of R Z known, use Equation 27 and Equation 28 to calculate the values of C_Z and C_P .

$$C_Z = \frac{1}{2 \times \pi \times F_{Z1} \times R_Z} \quad (27)$$

$$C_P = \frac{1}{2 \times \pi \times F_{P1} \times R_Z} \quad (28)$$

For this design, the two 47μF output capacitors are used. For ceramic capacitors, the actual output capacitance is less than the rated value when the capacitors have a DC bias voltage applied which occurs in

a DC-DC converter. The actual output capacitance may be as low as 54µF. The combined ESR is approximately 0.001Ω.Using Equation 20 and Equation 21, the output stage gain and phase loss are equivalent as:

Gain = –2.26 dB.

PL = –83.52 degrees.

For 70 degrees of phase margin, Equation 22 requires 63.52 degrees of phase boost.

Use Equation 23, Equation 24, and Equation 25 to calculate the zero and pole frequencies of the following values:

F_{Z1} = 5883 Hz.

F_{P1} = 106200 Hz.

Use Equation 26, Equation 27, and Equation 28 to calculate the values of R_Z , C_Z , and C_P .

$$R_Z = \frac{2 \times \pi \times 2500 \times 3.3 \times 54 \times 10^{-6} \times 8 \times 10^{6}}{12 \times 800 \times 0.8} = 29.2k\Omega \quad (29)$$

$$C_Z = \frac{1}{2 \times \pi \times 6010 \times 29200} = 928pF \quad (30)$$

$$C_P = \frac{1}{2 \times \pi \times 103900 \times 29200} = 51pF \quad (31)$$

Referring to Figure 10 and using standard values for R3, C6, and C7, the calculated values are as follows:

R3 = 29.4kΩ

C6 = 1000pF

C7 = 47pF

■ Bootstrap Capacitor

The MD8933 design requires a bootstrap capacitor, C4. The bootstrap capacitor must have a value of 0.1µF.The bootstrap capacitor is located between the PH pin and BOOT pin. The bootstrap capacitor should be a high-quality ceramic type with X7R or X5R grade dielectric for temperature stability.

■ Catch Diode

The MD8933 device is designed to operate using an external catch diode between the PH and GND pins. The selected diode must meet the absolute maximum ratings for the application. The reverse voltage must be higher than the maximum voltage at the PH pin, which is V IN(MAX) + 0.5 V. The peak current must be greater than I OUT(MAX) plus half the peak-to peak-inductor current. The forward-voltage drop should be small for higher efficiencies. The catch diode conduction time is (typically) longer than the high-side FET on time, so attention paid to diode parameters can make a marked improvement in overall efficiency. Additionally, check that the selected device is capable of dissipating the power losses. For this design, a Diodes, Inc. B340A was selected,with a reverse voltage of 40 V, forward current of 3 A, and a forward-voltage drop of 0.5 V.

■ Output Voltage Limitations

Because of the internal design of the MD8933 device, any given input voltage has both upper and lower output voltage limits. The upper limit of the output-voltage set point is constrained by the maximum duty cycle of 91% and is calculated with Equation 32.

$$V_{O(MAX)} = 0.91 \times ((V_{IN(MIN)} - I_{O(MAX)} \times R_{DS(ON)MAX}) + V_D) - (I_{O(MAX)} \times R_L) - V_D$$

where

• $V_{IN(MIN)}$ = Minimum input voltage.

- $I_{O(MAX)}$ = Maximum load current.
- V_D = Catch diode forward voltage.
- R_L = Output inductor series resistance. （32）

The equation assumes the maximum ON resistance for the internal high-side FET.

The lower limit is constrained by the minimum controllable on time which can be as high as 200ns. Use Equation 33 to calculate the approximate minimum output voltage for a given input voltage and minimum load current.

$$V_{O(MAX)} = 0.089 \times ((V_{IN(MIN)} - I_{O(MAX)} \times R_{DS(ON)MAX}) + V_D) - (I_{O(MAX)} \times R_L) - V_D$$

where

- $V_{IN(MIN)}$ = Minimum input voltage.
- $I_{O(MAX)}$ = Maximum load current.
- V_D = Catch diode forward voltage.
- R_L = Output inductor series resistance. （33）

The nominal on-resistance for the high-side FET in Equation 33 is assumed. Equation 33 accounts for the worst case variation of operating-frequency set point. Any design operating near the operational limits of the device should be carefully checked to ensure proper functionality.

■ Power Dissipation Estimate

The following formulas show how to estimate the device power dissipation under continuous-conduction mode (CCM) operations. These formulas should not be used if the device is working in the discontinuous-conduction mode (DCM) or pulse-skipping Eco-mode.

The device power dissipation includes:

1. Conduction loss:

$$Pcon = I_{OUT}^2 \times R_{DS(on)} \times V_{OUT} / V_{IN}$$

where

- I_{OUT} is the output current (A).
- RDS(on) is the on-resistance of the high-side MOSFET (Ω).
- VOUT is the output voltage (V).
- VIN is the input voltage (V).

2. Switching loss:

$$Psw = 0.5 \times 10^{-9} \times V_{IN}^2 \times I_{OUT} \times f_{SW}$$

where

- f_{SW} is the switching frequency (Hz).

3. Gate charge loss:

$$Pgc = 22.8 \times 10^{-9} \times f_{SW}$$

4. Quiescent current loss:

$$Pq = 0.1 \times 10^{-3} \times V_{IN}$$

Therefore:

$$Ptot = Pcon + Psw + Pgc + Pq$$

where

- Ptot is the total device power dissipation (W).

For given T_A:

$$T_J = T_A + Rth \times Ptot$$

where

- T_J is the junction temperature (°C).
- T_A is the ambient temperature (°C).
- Rth is the thermal resistance of the package (°C/W).

For given T_{JMAX} = 150°C:

$T_{AMAX} = T_{JMAX} – Rth \times Ptot$

where

- T_{JMAX} is maximum junction temperature (°C).
- T_{AMAX} is maximum ambient temperature (°C).

APPLICATION CURVES

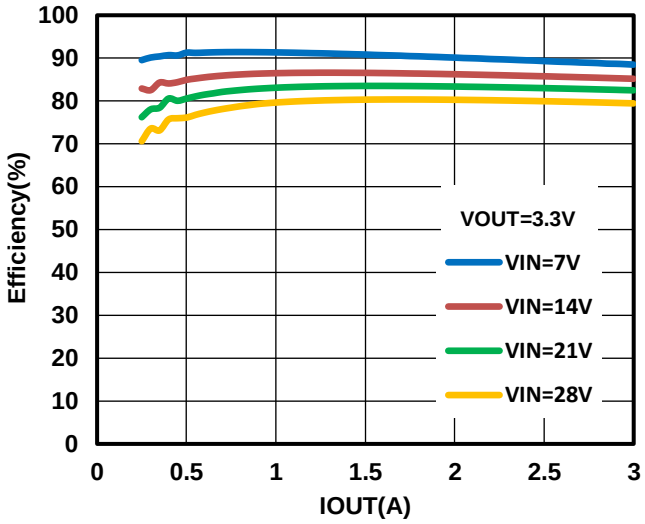


Figure 11. Efficiency

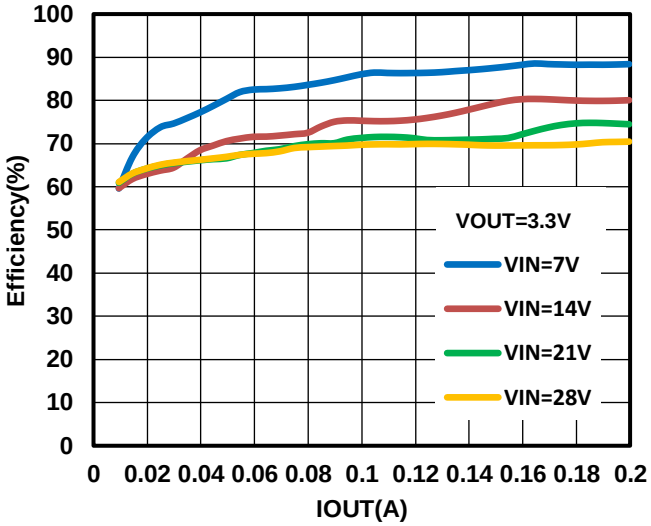


Figure 12. Low Current Efficiency

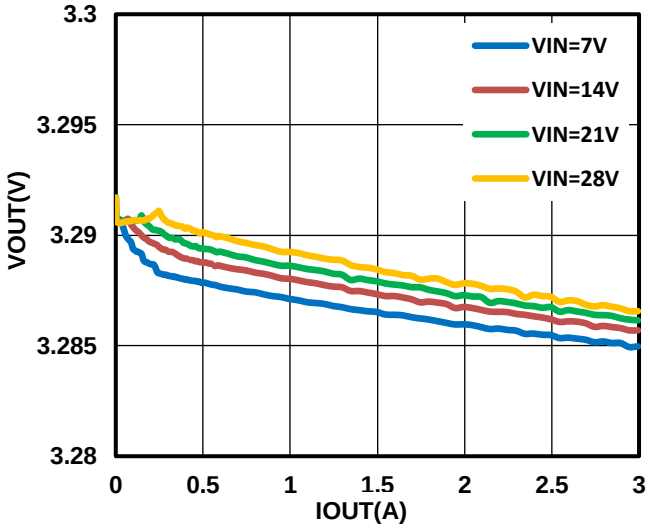


Figure 13. Load Regulation

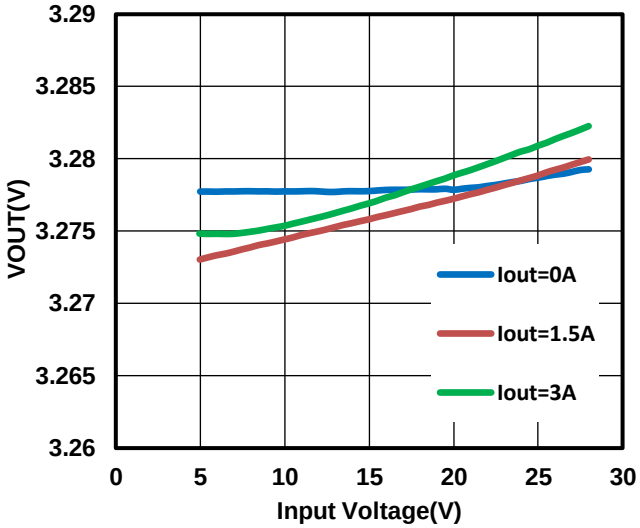


Figure 14. Line Regulation

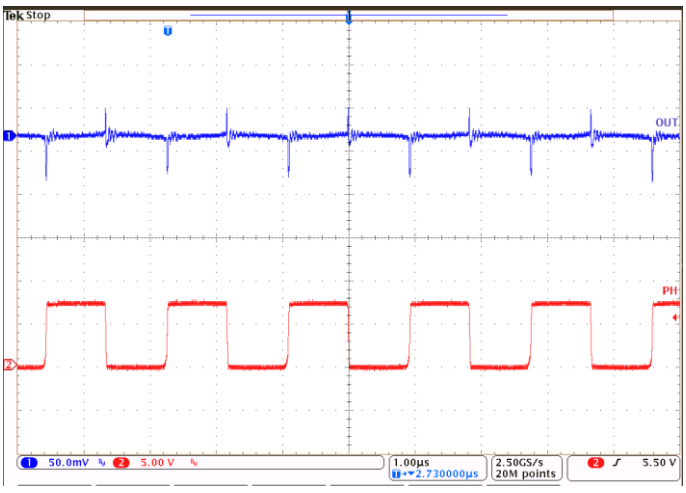


Figure 15. Output Ripple

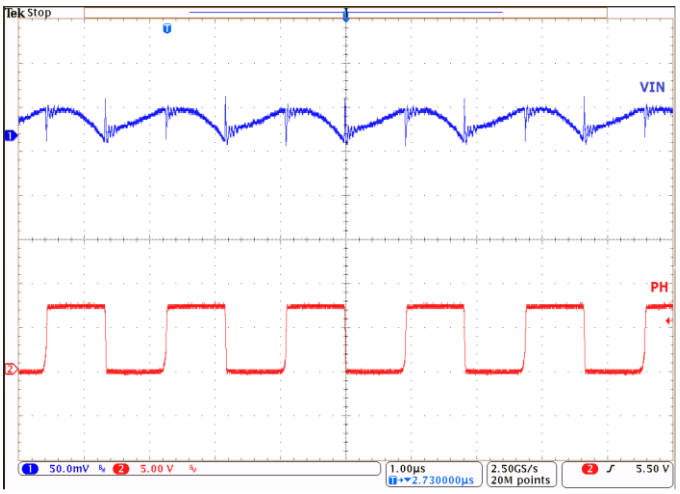


Figure 16. Input Ripple

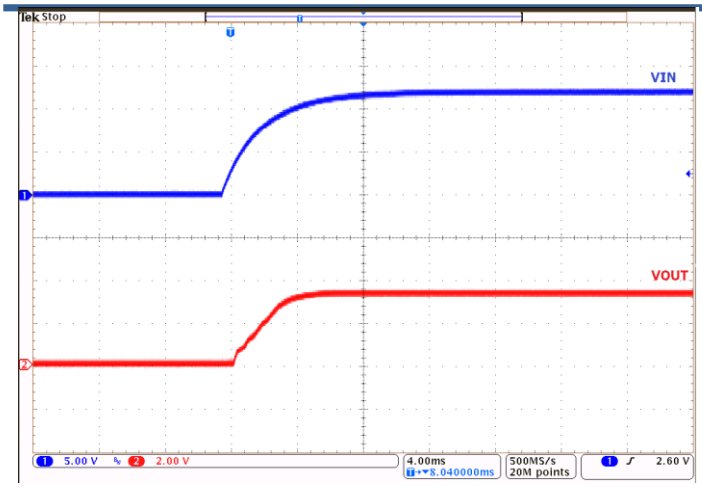


Figure 17. Startup

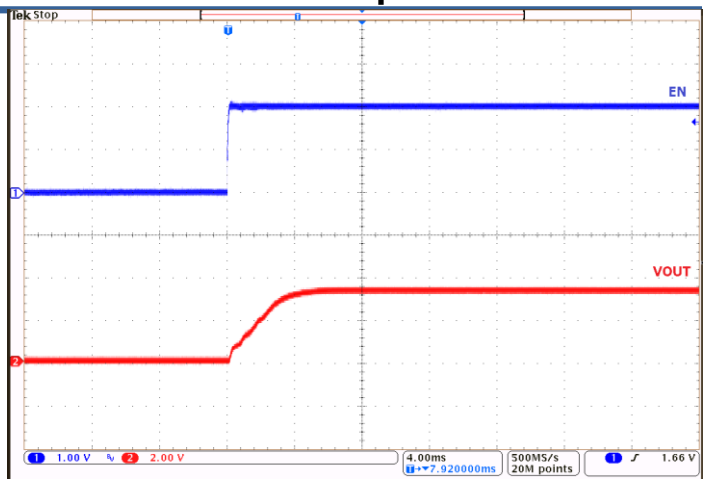


Figure 18. Startup Relative to Enable

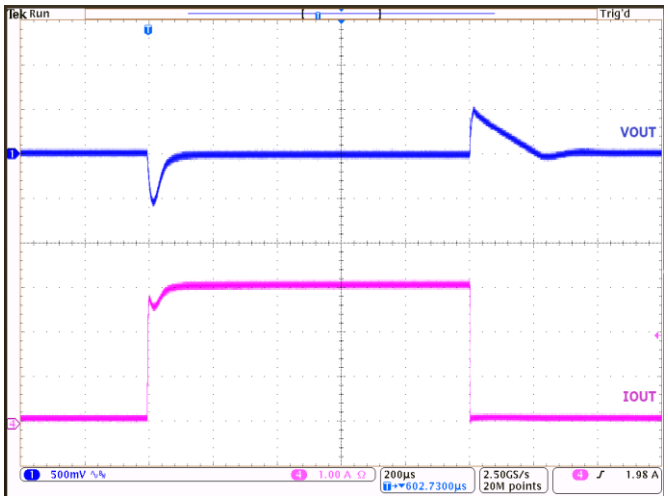


Figure 19. Load Transient

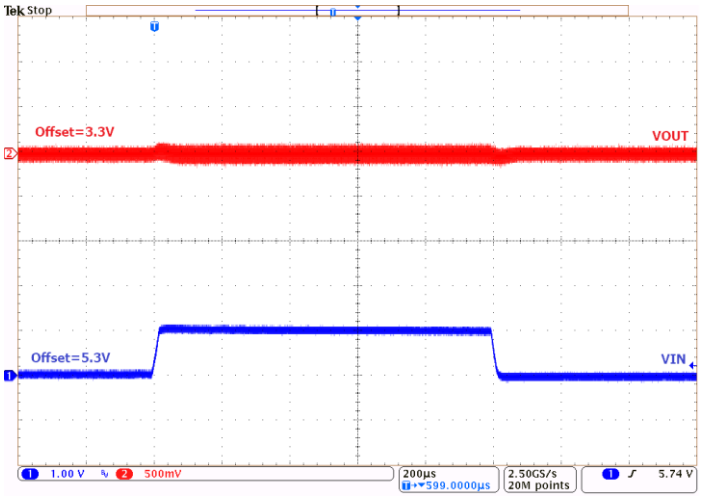
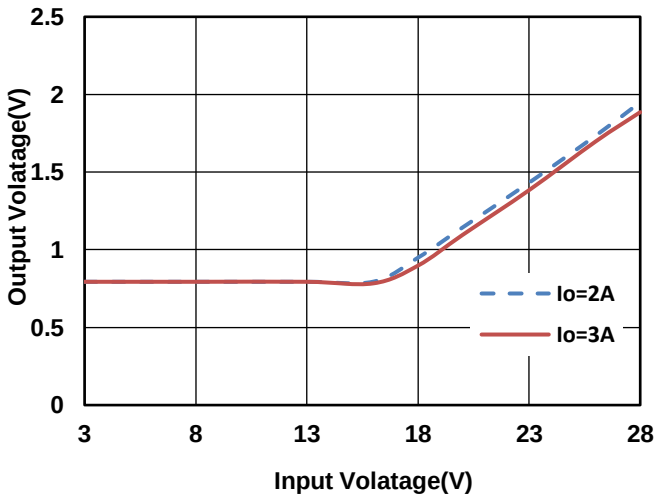
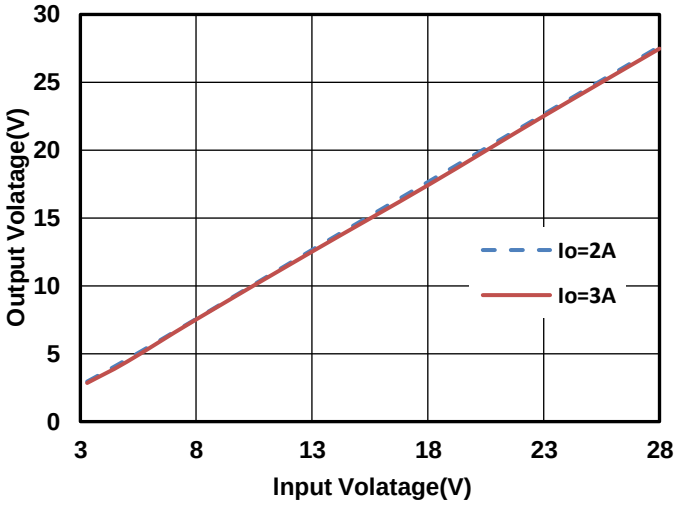


Figure 19. Line Transient





POWER SUPPLY RECOMMENDATIONS

The devices are designed to operate from an input-voltage supply range between 3.5V and 28V. This input supply should be well regulated. If the input supply is located more than a few inches from the converter additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 100μF is a typical choice.

LAYOUT

Layout Guidelines

The VIN pin should be bypassed to ground with a low-ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the anode of the catch diode. The typical recommended bypass capacitor is 10μF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the VIN pins and the source of the anode of the catch diode. Figure 25 shows a PCB layout example. The GND pin should be tied to the PCB ground plane at the pin of the device. The source of the low-side MOSFET should be connected directly to the top side PCB ground area used to tie together the ground sides of the input and output capacitors as well as the anode of the catch diode. The PH pin should be routed to the cathode of the catch diode and to the output inductor. Because the PH connection is the switching node, the catch diode and output inductor should be located very close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. For operation at full rated load, the top-side ground area must provide adequate heat dissipating area. The MD8933 device uses a fused lead frame so that the GND pin acts as a conductive path for heat dissipation from the die. Many applications have larger areas of internal or back-side ground plane available, and the top-side ground area can be connected to these areas using multiple vias under or adjacent to the device to help dissipate heat. The additional external components can be placed approximately as shown. Obtaining acceptable performance with alternate layout schemes may be possible, however this layout has been shown to produce good results and is intended as a guideline.

Layout Example

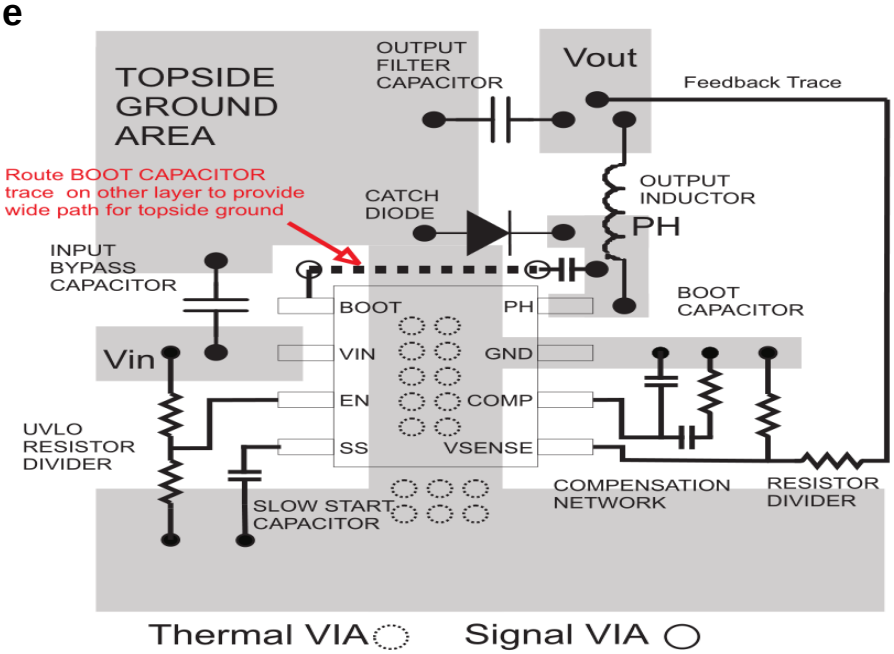


Figure 25. MD8933 device Board Layout

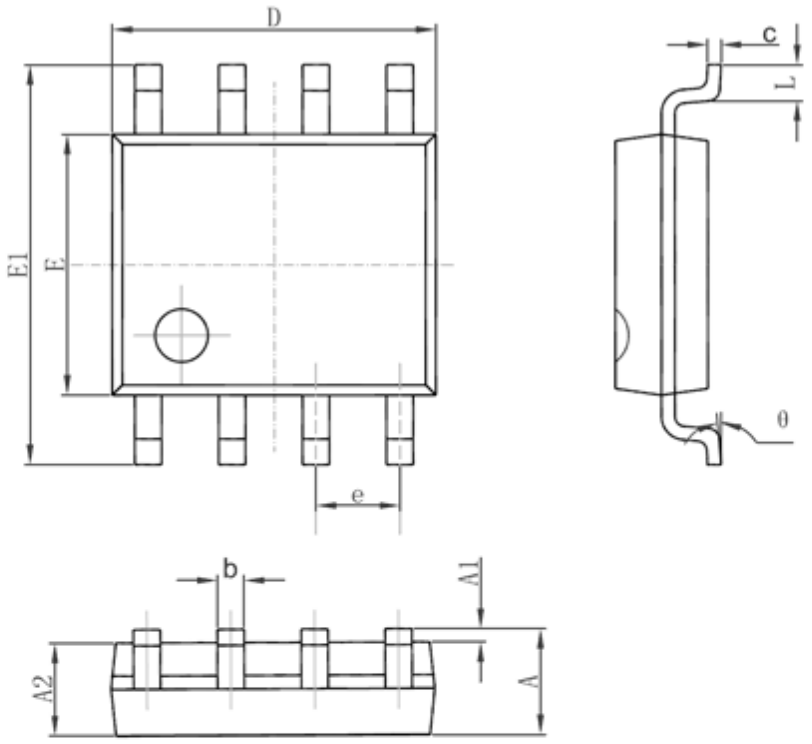
Electromagnetic Interference (EMI) Considerations

As EMI becomes a rising concern in more and more applications, the internal design of the MD8933 device includes features to reduce the EMI. The high-side MOSFET gate drive is designed to reduce the PH pin voltage ringing. The internal IC rails are isolated to decrease the noise sensitivity. A package bond wire scheme is used to lower the parasitics effects.

To achieve the best EMI performance, external component selection and board layout are equally important. Follow the steps listed in the Detailed Design Procedure section to prevent potential EMI issues.

PACKAGING INFORMATION

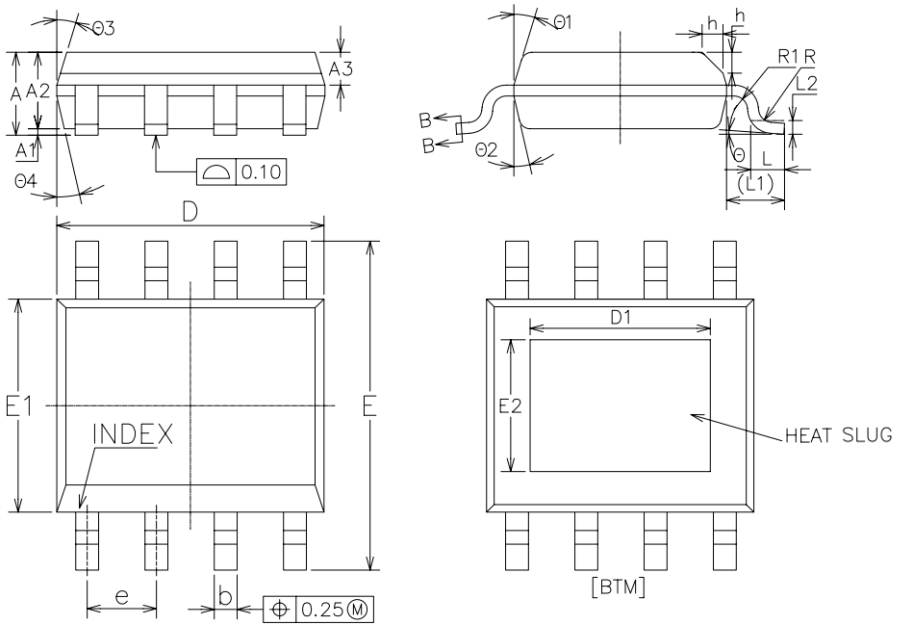
SOP8 PACKAGE OUTLINE DIMENSIONS

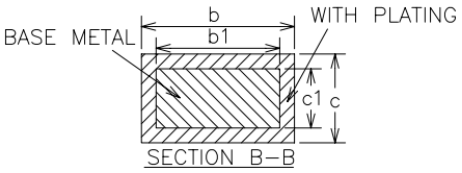


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

PACKAGING INFORMATION(CONTINUED)

ESOP8 PACKAGE OUTLINE DIMENSIONS





COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL		MIN	NOM	MAX
A		1.35	1.55	1.70
A1		0	0.10	0.15
A2		1.25	1.40	1.65
A3		0.50	0.60	0.70
b		0.38	–	0.51
b1		0.37	0.42	0.47
c		0.17	–	0.25
c1		0.17	0.20	0.23
D		4.80	4.90	5.00
D1	Option 1	3.10	3.30	3.50
	Option 2	2.09	2.29	2.49
E		5.80	6.00	6.20
E1		3.80	3.90	4.00
E2	Option 1	2.20	2.40	2.60
	Option 2	2.09	2.29	2.49
e		1.17	1.27	1.37
L		0.45	0.60	0.80
L1		1.04REF		
L2		0.25BSC		
R		0.07	–	–
R1		0.07	–	–
h		0.30	0.40	0.50
θ		0°	–	8°
θ1		15°	17°	19°
θ2		11°	13°	15°
θ3		15°	17°	19°
θ4		11°	13°	15°

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