

80V N-Channel Power MOSFET

DESCRIPTION

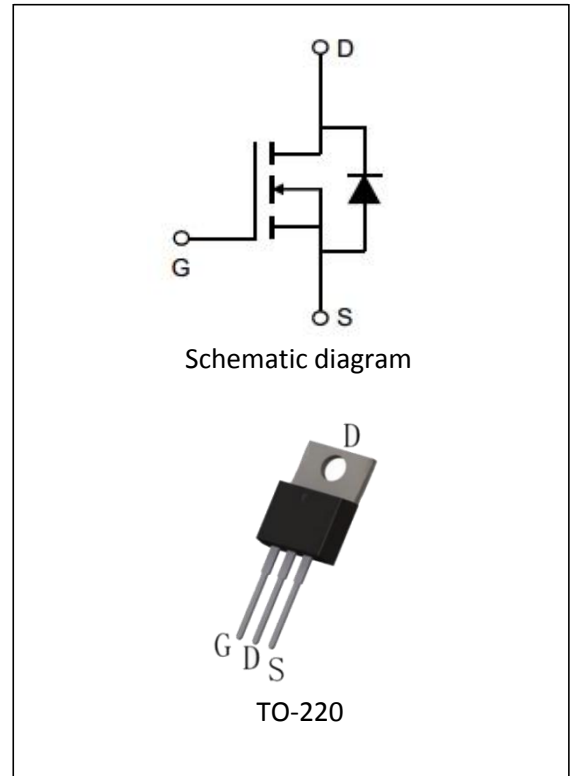
The IRFB3077 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.

KEY CHARACTERISTICS

- ① $V_{DS} = 80V, I_D = 200A, R_{DS(ON)} < 4m\Omega @ V_{GS}=10V$
- ② High density cell design for lower R_{dson}
- ③ Fully characterized avalanche voltage and current
- ④ Good stability and uniformity with high EAS
- ⑤ Excellent package for good heat dissipation

Application

- ① Power switching application
- ② Hard switched and High frequency circuits
- ③ Uninterruptible power supply



Package Marking And Ordering Information

Ordering Codes	Package	Product Code	Packing
IRFB3077	TO-220	IRFB3077	Tube

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	80	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	200	A
Drain Current-Pulsed ^(Note 1)	I_{DM}	800	A
Maximum Power Dissipation(Tc=25°C)	P_D	270	W
Single pulse avalanche energy ^(Note 2)	E_{AS}	1600	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	°C

Thermal Characteristic

Thermal Resistance,Junction-to-Case	$R_{\theta JC}$	0.41	°C/W
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Electrical Characteristics (TA=25 °C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	80	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=80V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V
Drain-Source On-State Resistance ^(Note 3)	$R_{DS(ON)}$	$V_{GS}=10V, I_D=50A$	-	3.5	4	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=15A$	-	17	-	S
Dynamic Characteristics						
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V, f=1.0MHz$	-	13200	-	pF
Output Capacitance	C_{oss}		-	-950	-	pF
Reverse Transfer Capacitance	C_{rss}		-	810	-	pF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=40V, I_D=40A, V_{GS}=10V, R_{GEN}=3\Omega$	-	26	-	nS
Turn-on Rise Time	t_r		-	20	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	50	-	nS
Turn-Off Fall Time	t_f		-	18	-	nS
Total Gate Charge	Q_g	$V_{DS}=64V, I_D=80A, V_{GS}=10V$	-	257	-	nC
Gate-Source Charge	Q_{gs}		-	76	-	nC
Gate-Drain Charge	Q_{gd}		-	80	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=80A$	-	-	1.2	V

Notes:

- 1.Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2.EAS condition :T j=25 °C ,VDD=50V,VG=10V,L=0.5mH,Rg=1 Ω
- 3.Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
- 4.Guaranteed by design, not subject to production.

Characteristics Curves

Figure 1 Output Characteristics

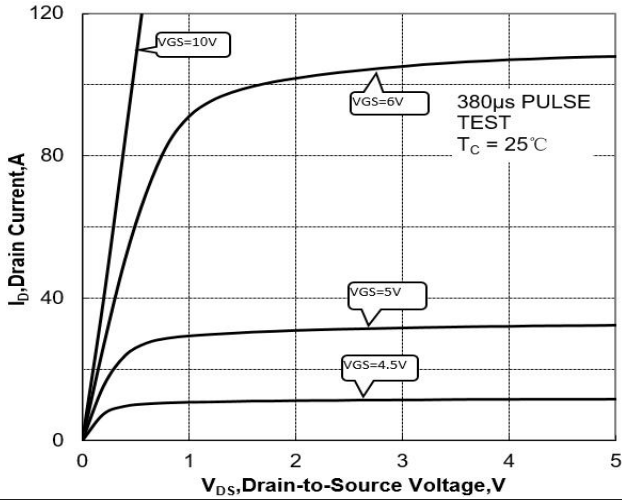


Figure 2 Transfer Characteristics

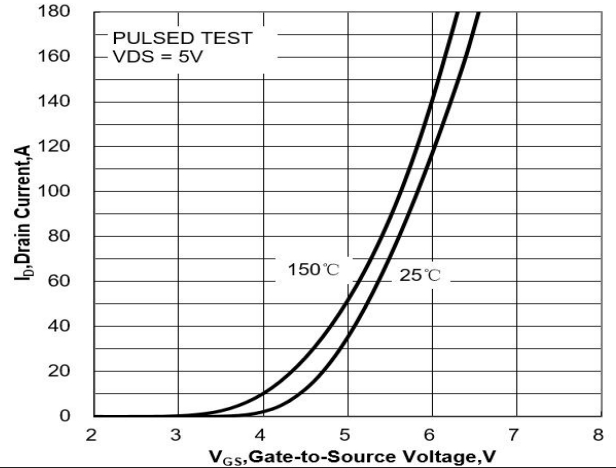


Figure 3 On-Resistance vs. ID and VGS

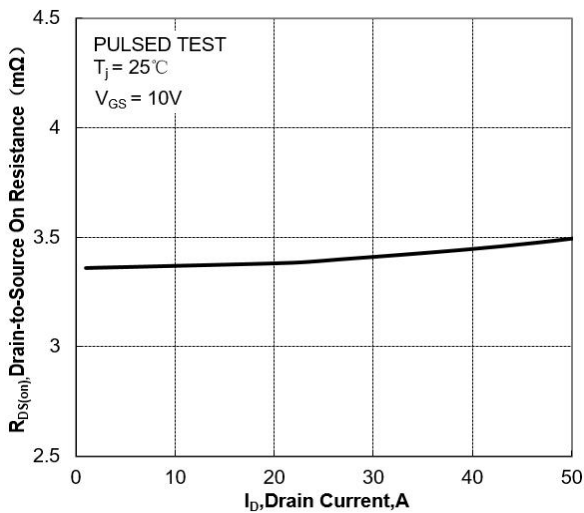


Figure 4 On-Resistance vs. Junction Temperature

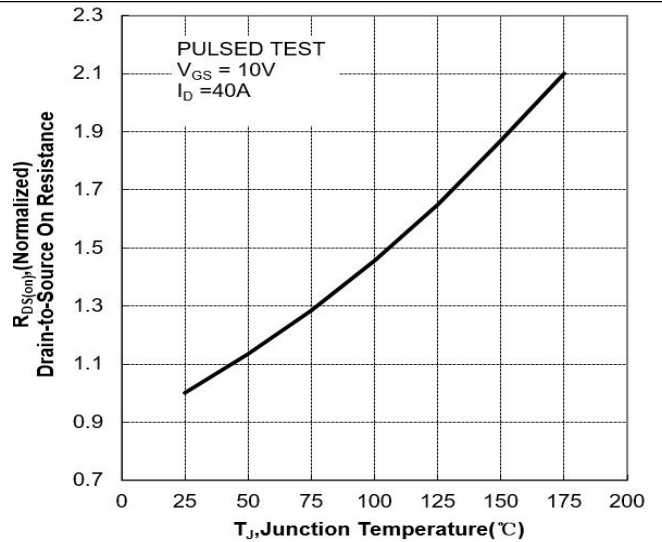


Figure 5 On-Resistance vs. VGS

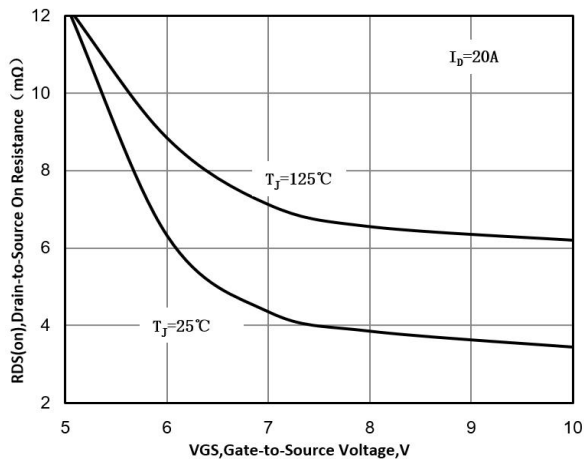


Figure 6 Body Diode Forward Voltage

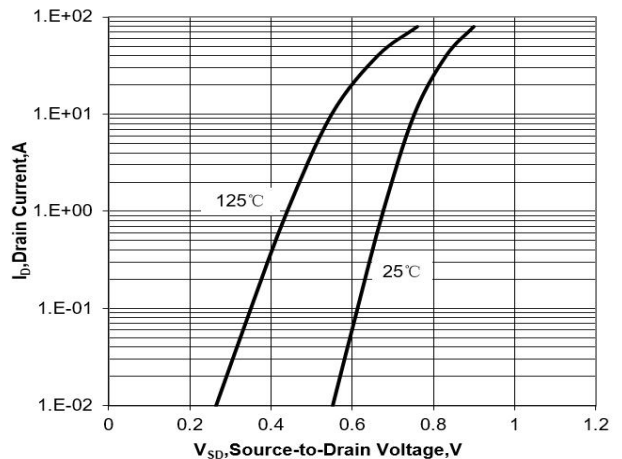


Figure 7 Gate-Charge Characteristics

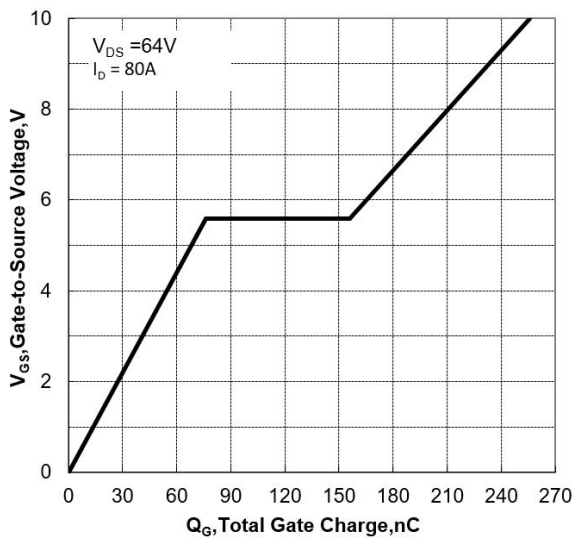


Figure 8 Capacitance Characteristics

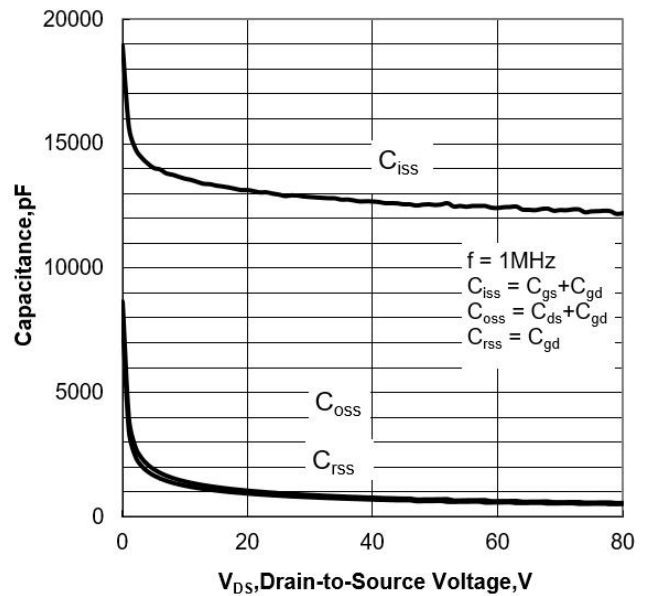


Figure 9 Maximum Forward Biased Safe Operation

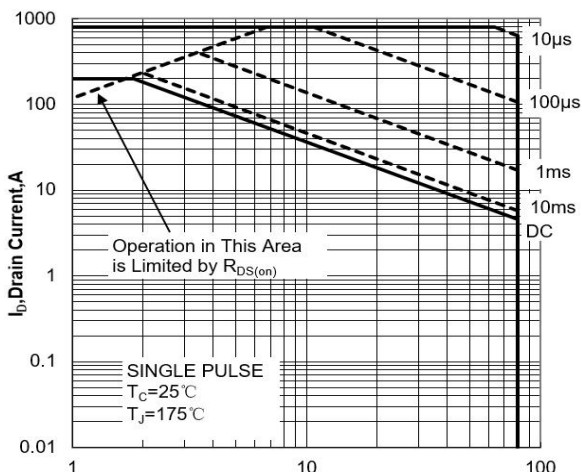


Figure 10 Single Pulse Power Rating Junction-to-Ambient

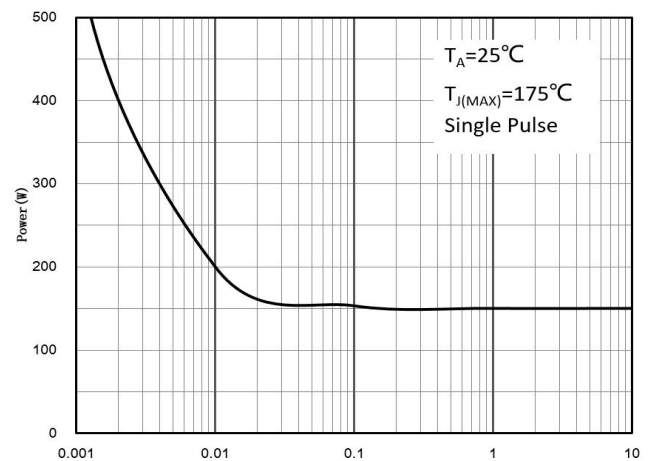
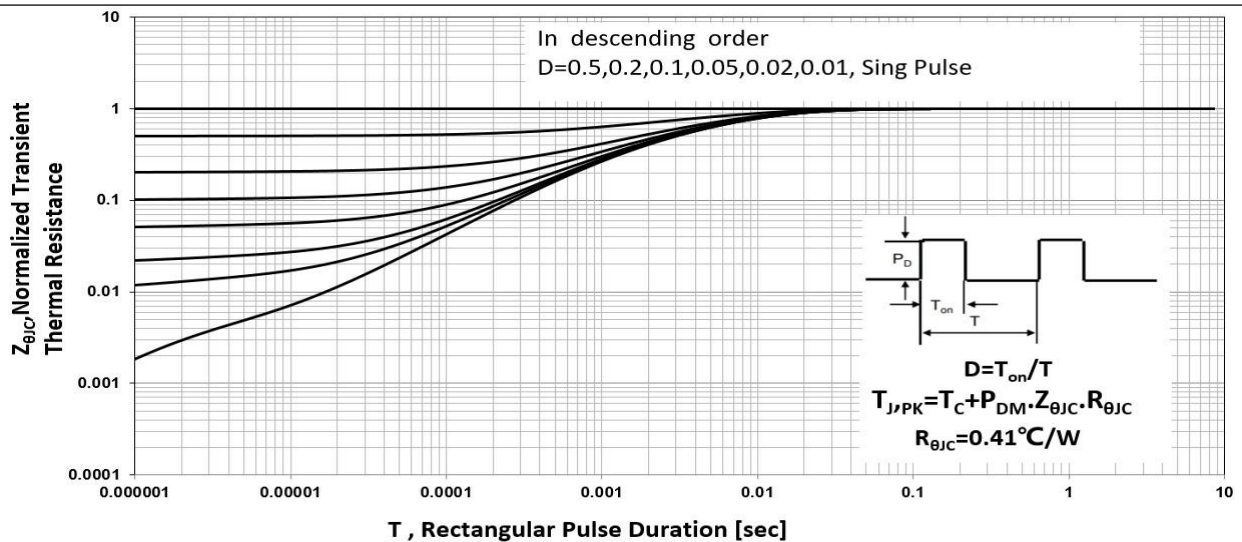
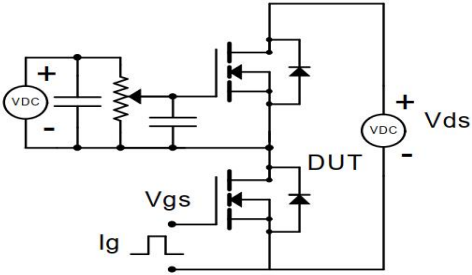
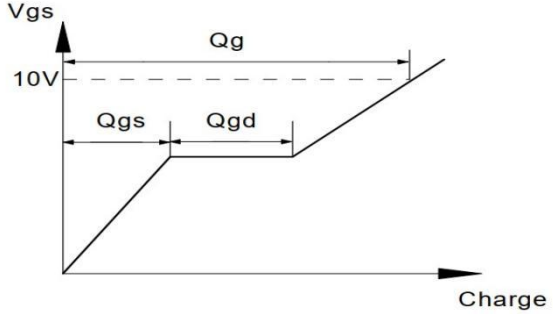
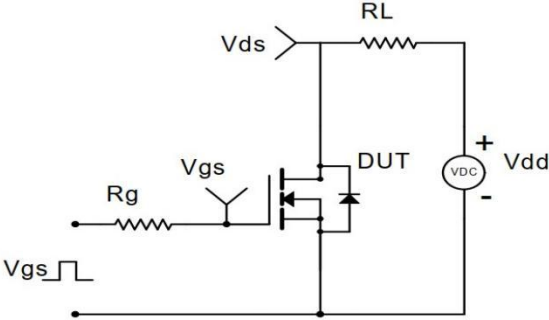
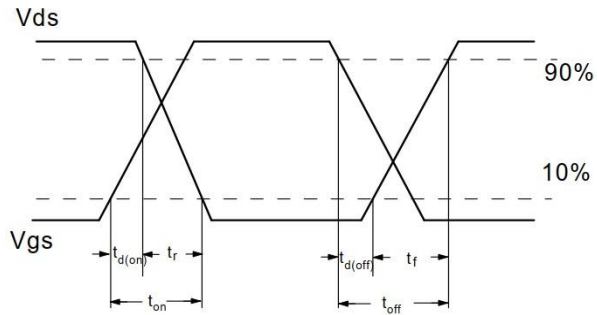
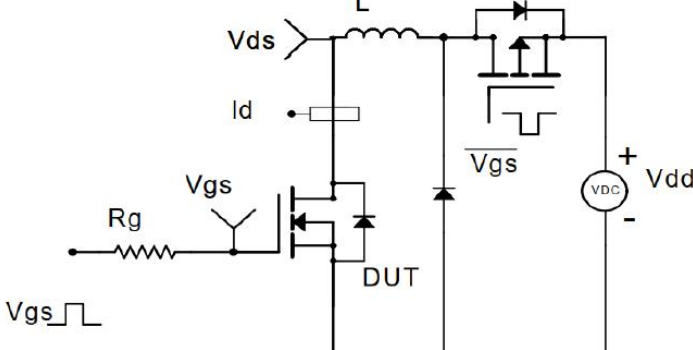
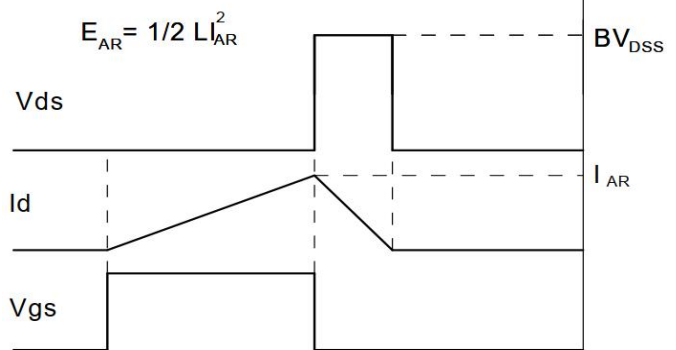
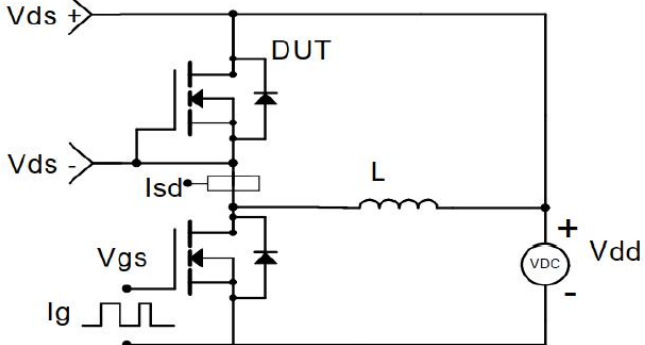
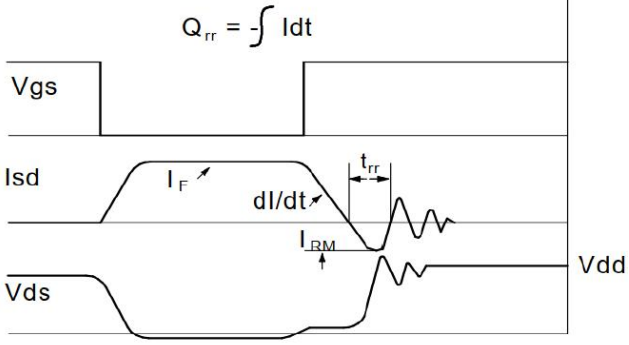


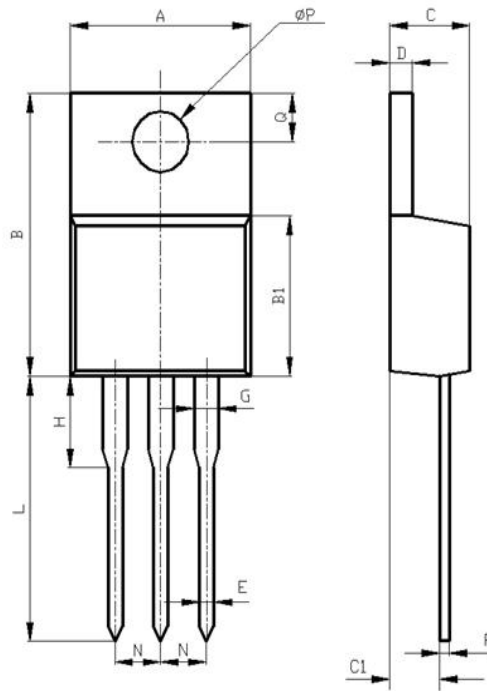
Figure 11 Normalized Maximum Transient Thermal Impedance



Test Circuit and Waveform

Gate Charge Test Circuit	Gate Charge Test Waveform
 <p>The diagram shows a MOSFET (DUT) with its gate connected to a pulse generator (Ig) through a resistor. The drain is connected to a DC source (VDC) through a resistor. The source is connected to ground. The gate-source voltage is labeled Vgs.</p>	 <p>The graph plots Vgs against Charge. It shows a linear ramp up to a plateau at 10V, followed by a linear ramp down. The area under the ramp is labeled Qg. The area under the plateau is labeled Qgd. The gate-source voltage is labeled Vgs.</p>
Resistive Switching Test Circuit	Resistive Switching Test Waveforms
 <p>The diagram shows a MOSFET (DUT) with its gate connected to a pulse generator (Vgs) through a resistor (Rg). The drain is connected to a load resistor (RL) and a DC source (VDD). The source is connected to ground. The drain-source voltage is labeled Vds.</p>	 <p>The graph shows Vds and Vgs waveforms. Vds is a trapezoidal pulse. Vgs is a square wave. The 90% and 10% levels of Vds are indicated. The turn-on time (ton) and turn-off time (toff) are labeled. The delay time (td(on)) and fall time (tr) are also labeled.</p>
Unclamped Inductive Switching (UIS) Test Circuit	Unclamped Inductive Switching (UIS) Test Waveforms
 <p>The diagram shows a MOSFET (DUT) with its gate connected to a pulse generator (Vgs) through a resistor (Rg). The drain is connected to an inductor (L) and a diode. The source is connected to ground. The drain-source voltage is labeled Vds. The current through the inductor is labeled Id. The DC source is labeled VDD.</p>	 <p>The graph shows Vds, Id, and Vgs waveforms. Vds is a trapezoidal pulse. Id is a triangular pulse. Vgs is a square wave. The energy stored in the inductor is given by the equation $E_{AR} = 1/2 L I_{AR}^2$. The maximum drain-source voltage is labeled BV_{DSS} and the average current is labeled I_{AR}.</p>
Diode Recovery Test Circuit	Diode Recovery Test Waveforms
 <p>The diagram shows a MOSFET (DUT) with its gate connected to a pulse generator (Vgs) through a resistor (Rg). The drain is connected to a diode and an inductor (L). The source is connected to ground. The drain-source voltage is labeled Vds. The current through the diode is labeled Isd. The DC source is labeled VDD.</p>	 <p>The graph shows Vgs, Isd, and Vds waveforms. Vgs is a square wave. Isd is a trapezoidal pulse. Vds is a trapezoidal pulse. The reverse recovery time (trr) is labeled. The reverse current (IRM) is labeled. The equation for reverse recovery charge is given as $Q_{rr} = \int Idt$.</p>

Package Description



Items	Values(mm)	
	MIN	MAX
A	9.60	10.6
B	15.0	16.0
B1	8.90	9.50
C	4.30	4.80
C1	2.30	3.10
D	1.20	1.40
E	0.70	0.90
F	0.30	0.60
G	1.17	1.37
H	2.70	3.80
L	12.6	14.8
N	2.34	2.74
Q	2.40	3.00
ϕP	3.50	3.90

TO-220 package



NOTE:

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. Please do not exceed the absolute maximum ratings of the device when circuit designing.
2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
3. MOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. Shenzhen Minos reserves the right to make changes in this specification sheet and is subject to change without prior notice.

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