

60V N-Channel Power MOSFET

DESCRIPTION

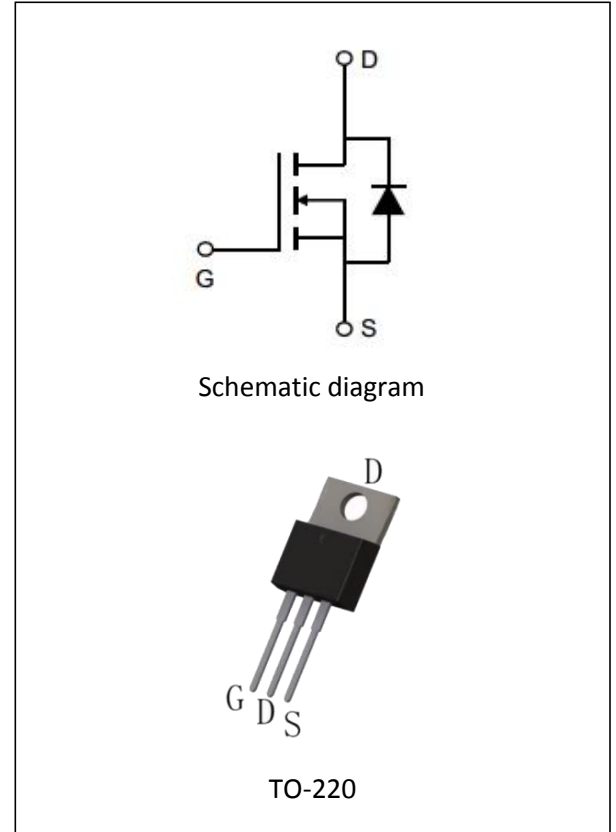
The IRFB3306 uses advanced trench technology to provide excellent RDS(ON), low gate charge. It can be used in a wide variety of applications.

KEY CHARACTERISTICS

- ① $V_{DS} = 60V, I_D = 150A$
 $R_{DS(ON)} < 4.2m\Omega @ V_{GS}=10V$
- ② High density cell design for lower Rds on
- ③ Fully characterized avalanche voltage and current
- ④ Good stability and uniformity with high EAS
- ⑤ Excellent package for good heat dissipation

Application

- ① Power switching application
- ② Hard switched and High frequency circuits
- ③ Uninterruptible power supply



Package Marking And Ordering Information

Ordering Codes	Package	Product Code	Packing
IRFB3306	TO-220	IRFB3306	Tube

Absolute Maximum Ratings (TA=25 °C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	150	A
Drain Current-Pulsed (Note 1)	I_{DM}	600	A
Maximum Power Dissipation (Tc=25 °C)	P_D	210	W
Single pulse avalanche energy (Note 2)	E_{AS}	1000	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.7	°C/W
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Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V
Drain-Source On-State Resistance(Note 3)	$R_{DS(on)}$	$V_{GS}=10V, I_D=50A$	-	3.5	4.2	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=50V, I_D=75A$	-	180	-	S
Dynamic Characteristics						
Input Capacitance	C_{iss}	$V_{DS}=25V,$ $V_{GS}=0V,$ $f=1.0MHz$	-	8200	-	pF
Output Capacitance	C_{oss}		-	760	-	pF
Reverse Transfer Capacitance	C_{rss}		-	680	-	pF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, I_D=40A,$ $V_{GS}=10V, R_{GEN}=3\Omega$	-	27	-	nS
Turn-on Rise Time	t_r		-	25	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	90	-	nS
Turn-Off Fall Time	t_f		-	40	-	nS
Total Gate Charge	Q_g	$V_{DS}=60V, I_D=40A, V_{GS}=10V$	-	186	-	nC
Gate-Source Charge	Q_{gs}		-	46	-	nC
Gate-Drain Charge	Q_{gd}		-	70	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=150A$	-	-	1.2	V

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. E_{AS} condition : $T_j=25^\circ C, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production.

Characteristics Curves

Figure 1 Output Characteristics

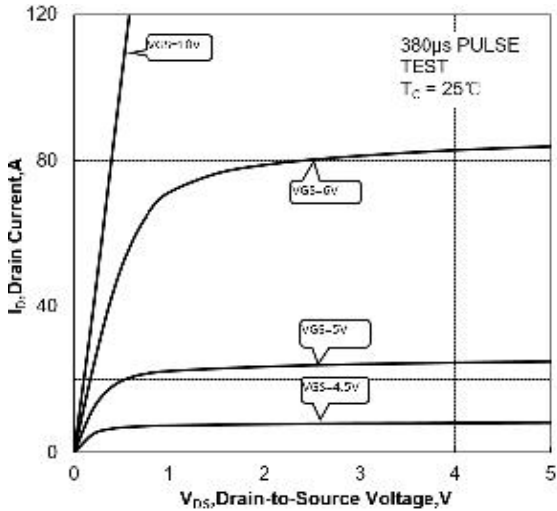


Figure 2 Transfer Characteristics

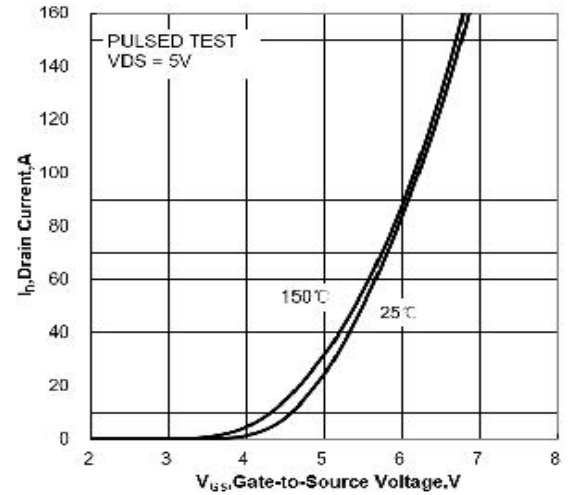


Figure 3 On-Resistance vs. ID and VGS

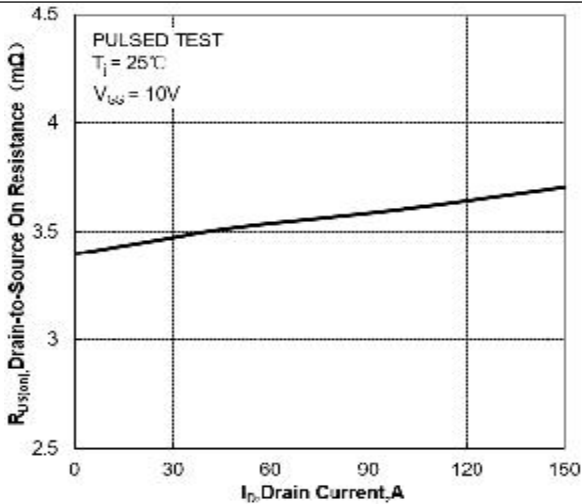


Figure 4 On-Resistance vs. Junction Temperature

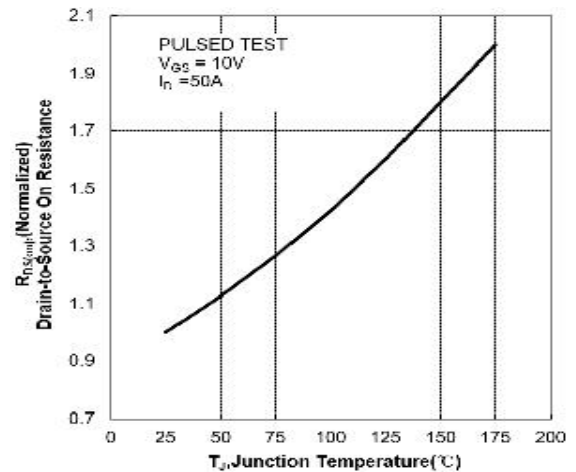


Figure 5 On-Resistance vs. VGS

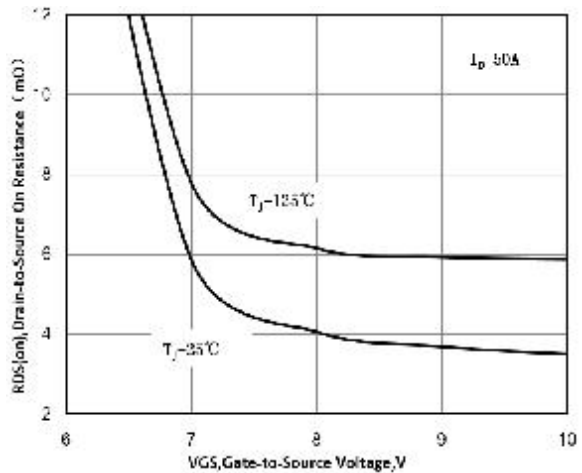


Figure 6 Body Diode Forward Voltage

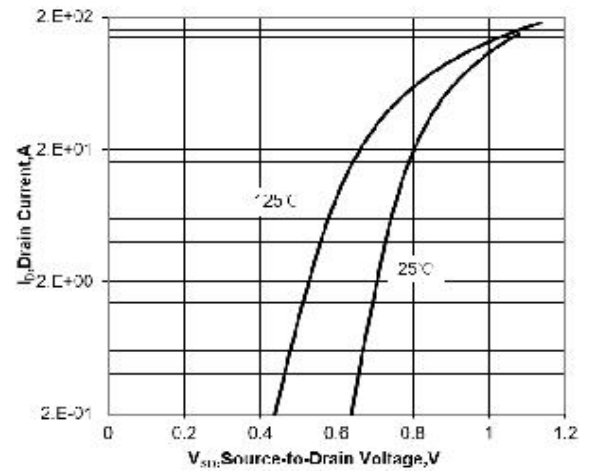


Figure 7 Gate-Charge Characteristics

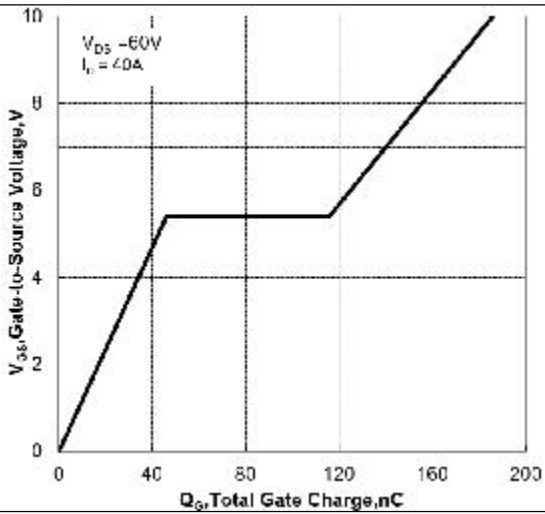


Figure 8 Capacitance Characteristics

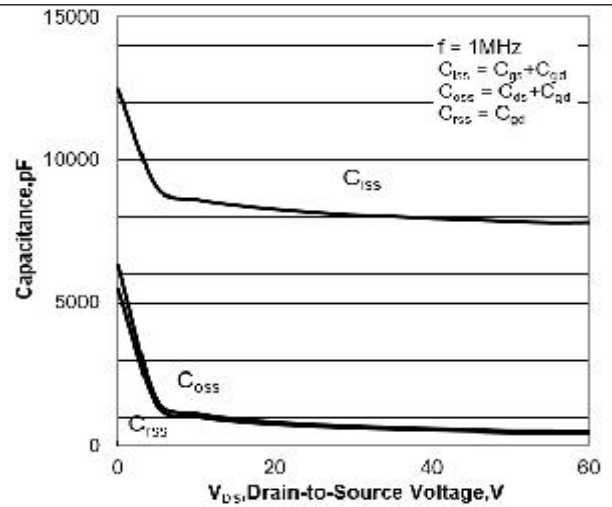


Figure 9 Maximum Forward Biased Safe Operation Area

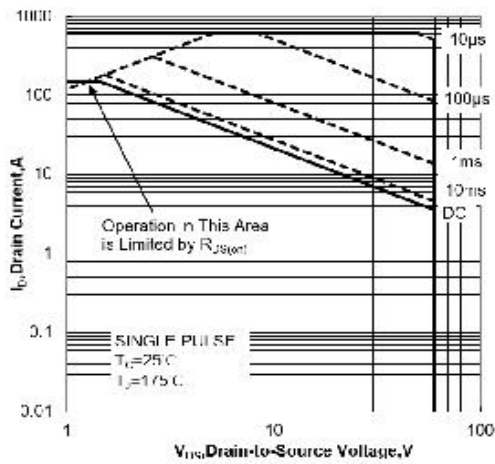


Figure 10 Single Pulse Power Rating Junction-to-Ambient

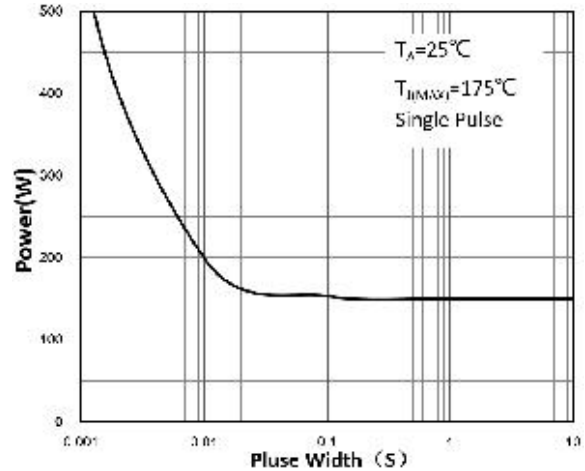
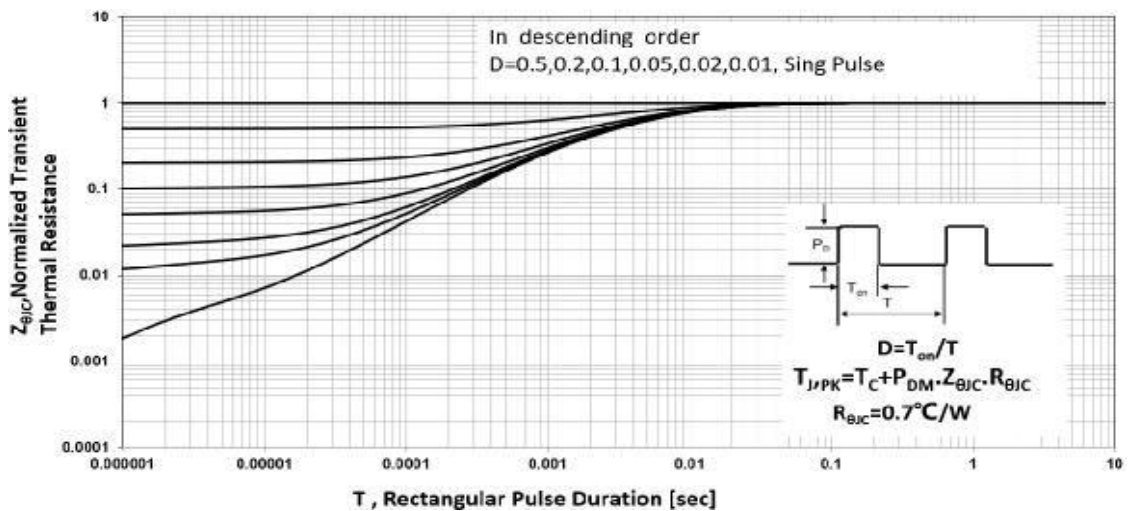
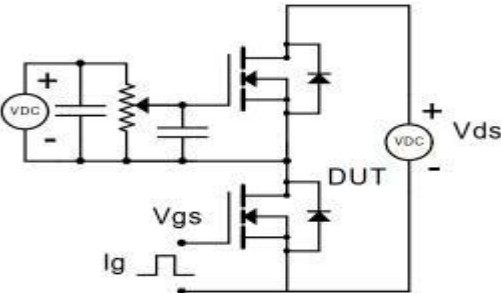
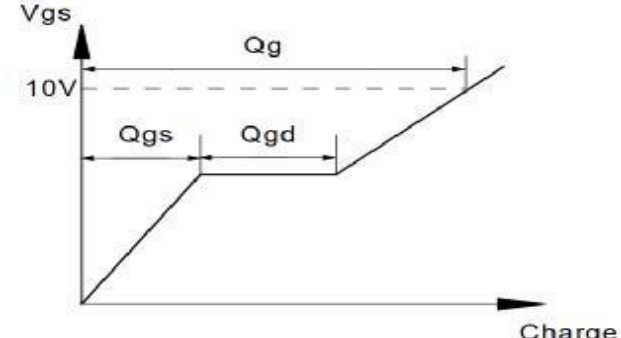
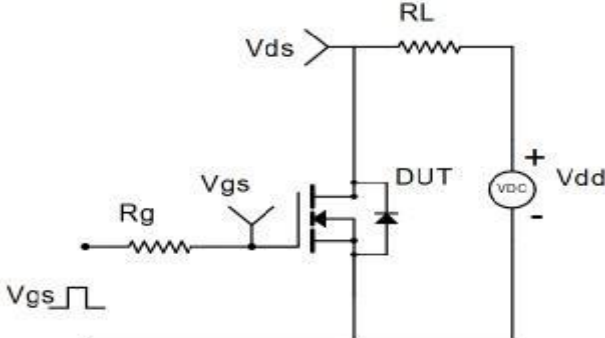
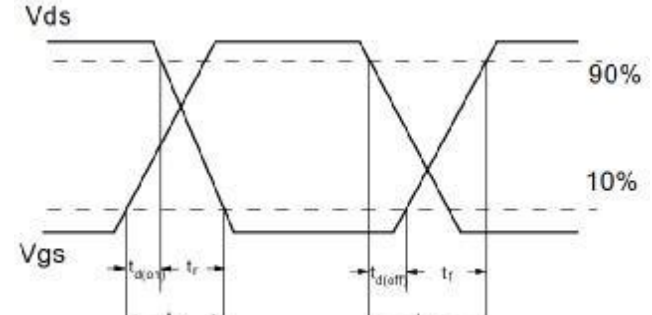
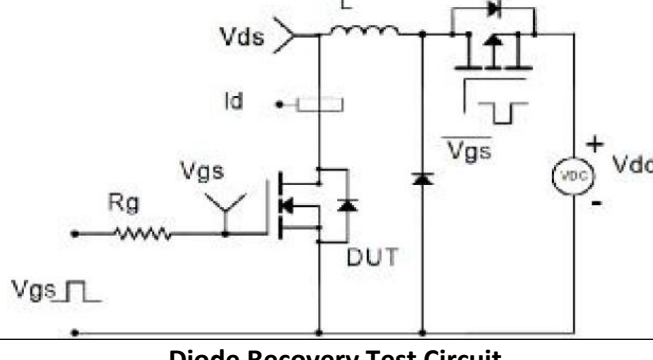
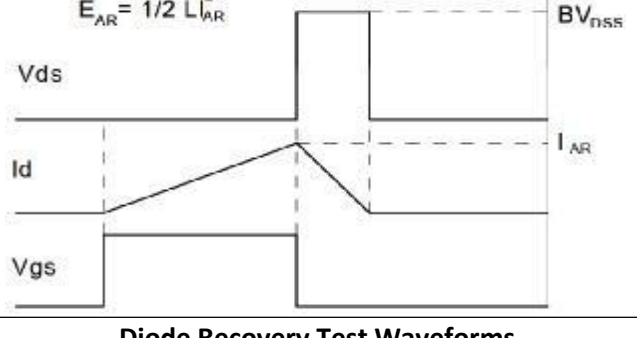
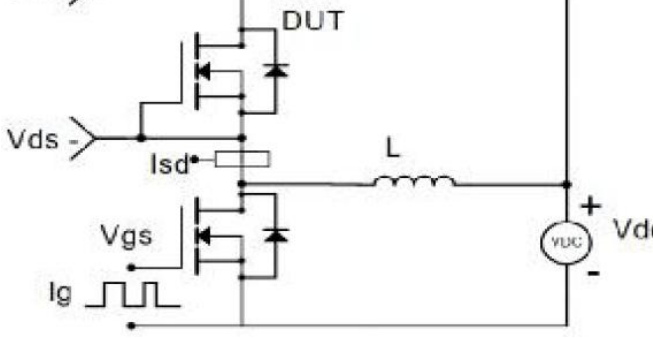
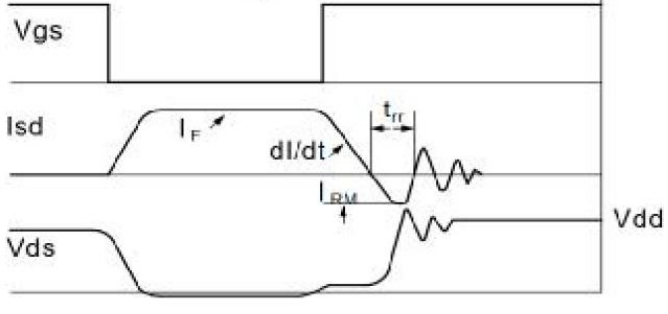


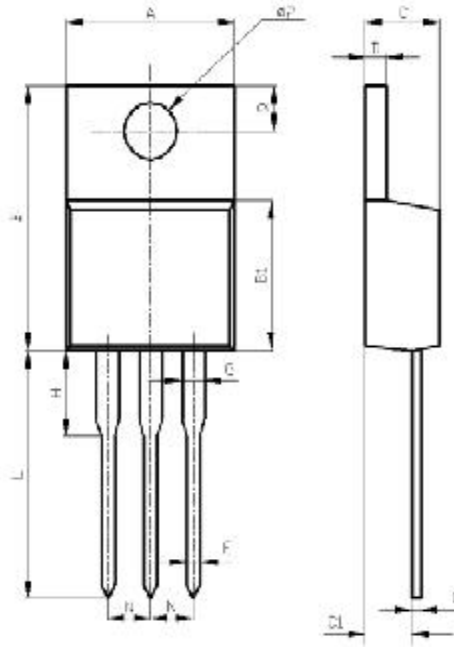
Figure 11 Normalized Maximum Transient Thermal Impedance



Test Circuit and Waveform

Gate Charge Test Circuit	Gate Charge Test Waveform
 <p>The diagram shows a MOSFET (DUT) with its gate connected to a V_{gs} terminal. A V_{ds} terminal is connected to a VDC source. A gate resistor R_g is connected between the gate and a V_{gs} terminal. A gate current I_g is shown as a pulse. The MOSFET is connected to a load resistor and a diode.</p>	 <p>The graph plots V_{gs} against Charge. It shows a linear ramp up to 10V, a flat plateau, and a linear ramp down. The total area under the curve is labeled Q_g. The area under the rising ramp is Q_{gs}, and the area under the falling ramp is Q_{gd}.</p>
Resistive Switching Test Circuit	Resistive Switching Test Waveforms
 <p>The diagram shows a MOSFET (DUT) with its gate connected to a V_{gs} terminal. A V_{ds} terminal is connected to a load resistor R_L and a VDC source V_{dd}. A gate resistor R_g is connected between the gate and a V_{gs} terminal. A gate current I_g is shown as a pulse.</p>	 <p>The graph plots V_{ds} and V_{gs} against time. It shows a trapezoidal V_{ds} waveform and a square-wave V_{gs} waveform. The V_{ds} waveform is defined by 90% and 10% voltage levels. Key timing parameters are labeled: t_{di(on)}, t_r, t_{di(off)}, and t_{off}.</p>
Unclamped Inductive Switching (UIS) Test Circuit	Unclamped Inductive Switching (UIS) Test Waveforms
 <p>The diagram shows a MOSFET (DUT) with its gate connected to a V_{gs} terminal. A V_{ds} terminal is connected to an inductor L and a diode. A VDC source V_{dd} is connected to the diode. A gate resistor R_g is connected between the gate and a V_{gs} terminal. A gate current I_g is shown as a pulse. The current through the inductor is labeled I_d.</p>	 <p>The graph plots V_{ds}, I_d, and V_{gs} against time. It shows a trapezoidal V_{ds} waveform, a triangular I_d waveform, and a square-wave V_{gs} waveform. The energy stored in the inductor is given by the equation $E_{AR} = 1/2 L I_{AR}^2$. The V_{ds} waveform reaches a peak value of BV_{DSS}. The I_d waveform reaches a peak value of I_{AR}.</p>
Diode Recovery Test Circuit	Diode Recovery Test Waveforms
 <p>The diagram shows a MOSFET (DUT) with its gate connected to a V_{gs} terminal. A V_{ds} terminal is connected to an inductor L and a diode. A VDC source V_{dd} is connected to the diode. A gate resistor R_g is connected between the gate and a V_{gs} terminal. A gate current I_g is shown as a pulse. The current through the diode is labeled I_{sd}.</p>	 <p>The graph plots V_{gs}, I_{sd}, and V_{ds} against time. It shows a square-wave V_{gs} waveform, a trapezoidal I_{sd} waveform, and a V_{ds} waveform. The I_{sd} waveform is defined by I_F and dl/dt. The V_{ds} waveform shows a reverse recovery transient with a peak value of I_{RM} and a time constant of t_{rr}. The equation $Q_{rr} = \int I_{sd} dt$ is shown.</p>

Package Description



Items	Values(mm)	
	MIN	MAX
A	9.60	10.6
B	15.0	16.0
B1	8.90	9.50
C	4.30	4.80
C1	2.30	3.10
D	1.20	1.40
E	0.70	0.90
F	0.30	0.60
G	1.17	1.37
H	2.70	3.80
L	12.6	14.8
N	2.34	2.74
Q	2.40	3.00
φ P	3.50	3.90

TO-220 package



NOTE:

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. Please do not exceed the absolute maximum ratings of the device when circuit designing.
2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
3. MOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. Shenzhen Minos reserves the right to make changes in this specification sheet and is subject to change without prior notice.

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