

Silicon N-Channel Power MOSFET

Description

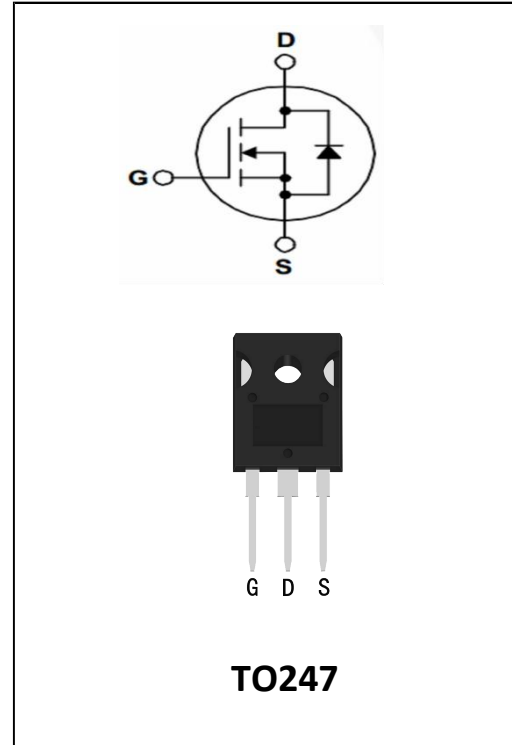
MD50N20 the silicon N-channel Enhanced MOSFETs, is obtained by advanced MOSFET technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor is suitable device for SMPS, high speed switching and general purpose applications.

General Features

- ①  $V_{DS}=250V$ ,  $R_{dson}<48m\Omega$  @ $V_{GS}=10V$ ,  $I_D=40A$  (Typ:30m $\Omega$ )
- ② Fast switching
- ③ 100% avalanche tested
- ④ Improved dv/dt capability

Application

- ① Switch Mode Power Supply (SMPS)
- ② Uninterruptible Power Supply (UPS)
- ③ Power Factor Correction (PFC)



Package Marking And Ordering Information:

Ordering Codes	Package	Product Code	Packing
MD50N20	TO-247	MD50N20	Tube

Absolute Maximum Ratings TC = 25°C, unless otherwise noted

Parameter	Symbol	Value	Unit
		TO-247	
Drain-Source Voltage	$V_{DSS}$	200	V
Continuous Drain Current	$I_D$	50	A
Pulsed Drain Current (note2)	$I_{DM}$	200	A
Gate-Source Voltage	$V_{GSS}$	$\pm 20$	V
Single Pulse Avalanche Energy (note2)	$E_{AS}$	780	mJ
Avalanche Current (note1)	$I_{AR}$	39.5	V/ns
Repetitive Avalanche Energy (note1)	$E_{AR}$	468	W
Power Dissipation (TC = 25°C)	$P_D$	250	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 175	°C

## Thermal Resistance

Parameter	Symbol	Value		Unit
		TO-247		
Thermal Resistance, Junction-to-Case	$R_{thJC}$	0.5		°C/W
Thermal Resistance, Junction-to-Ambient	$R_{thJA}$	45		

## Specifications $T_J = 25^\circ\text{C}$ , unless otherwise noted

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	200	--	--	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 200V, V_{GS} = 0V, T_J = 25^\circ\text{C}$	--	--	1	$\mu A$
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = +20V, V_{DS} = 0V$	--	--	100	nA
		$V_{GS} = -20V, V_{DS} = 0V$	--	--	-100	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.0	--	4.0	V
Drain-Source On-Resistance (Note3)	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 25A$	--	30	48	m $\Omega$
Input Capacitance	$C_{iss}$	$V_{GS} = 0V, V_{DS} = 25V, f = 1.0\text{MHz}$	--	3538	--	pF
Output Capacitance	$C_{oss}$		--	657	--	
Reverse Transfer Capacitance	$C_{rss}$		--	280	--	
Total Gate Charge	$Q_g$	$V_{DD} = 160V, I_D = 25A, V_{GS} = 0 \text{ to } 10V$	--	244	--	nC
Gate-Source Charge	$Q_{gs}$		--	16	--	
Gate-Drain Charge	$Q_{gd}$		--	144	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 100V, I_D = 25A, V_{GS} = 10V, R_G = 25\Omega$	--	53	--	ns
Turn-on Rise Time	$t_r$		--	65	--	
Turn-off Delay Time	$t_{d(off)}$		--	689	--	
Turn-off Fall Time	$t_f$		--	230	--	
Continuous Body Diode Current	$I_S$	$T_C = 25^\circ\text{C}$	--	--	50	A
Pulsed Diode Forward Current	$I_{SM}$		--	--	200	
Body Diode Voltage	$V_{SD}$	$T_J = 25^\circ\text{C}, I_{SD} = 25A, V_{GS} = 0V$	--	--	1.5	V
Reverse Recovery Time	$t_{rr}$	$V_{GS} = 0V, I_S = 25A, dI_F/dt = 100A/\mu s$	--	208	--	ns
Reverse Recovery Charge	$Q_{rr}$		--	2.04	--	$\mu C$

### Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2.  $I_{AS} = 30A, V_{DD} = 30V, R_G = 25\Omega, \text{Starting } T_J = 25^\circ\text{C}$
3. Pulse Test: Pulse width  $\leq 300\mu s, \text{Duty Cycle } \leq 1\%$

Typical Characteristics  $T_J = 25^\circ\text{C}$ , unless otherwise noted

Figure 1. Output Characteristics ( $T_J = 25^\circ\text{C}$ )

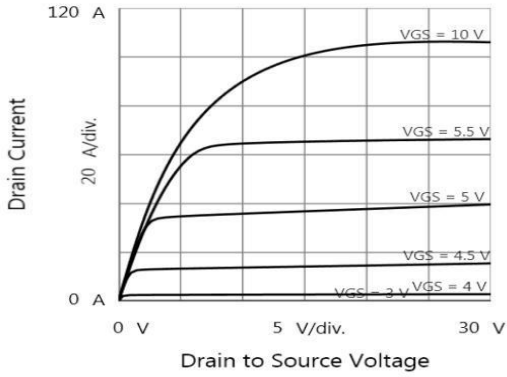


Figure 2. Transfer Characteristics

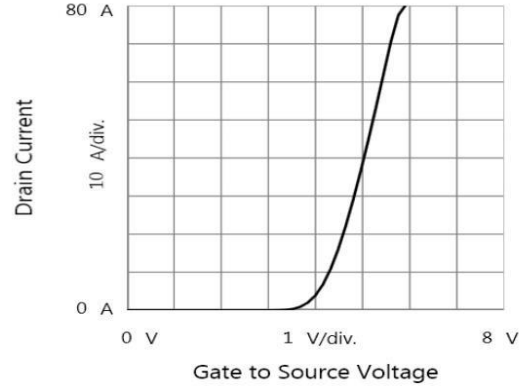


Figure 3. Maximum Continuous Drain Current vs Case Temperature

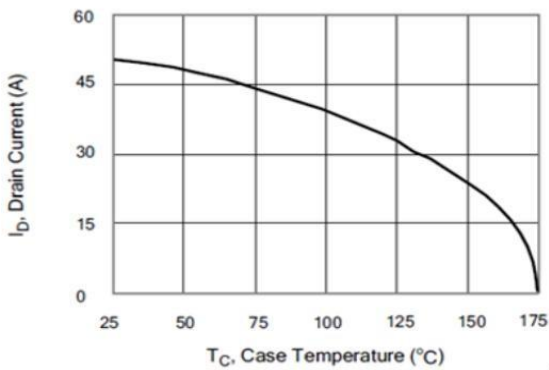


Figure 4. Drain to Source Voltage vs. Gate to Source Voltage

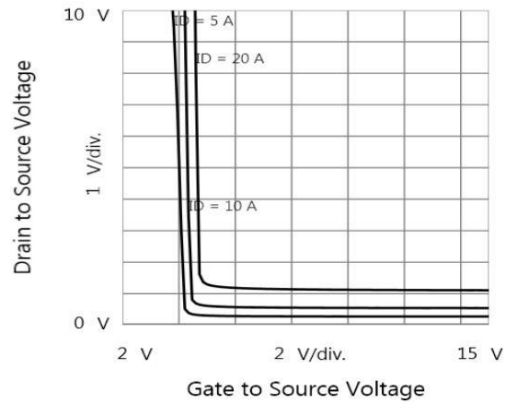


Figure 5. Typical Breakdown Voltage vs Junction Temperature

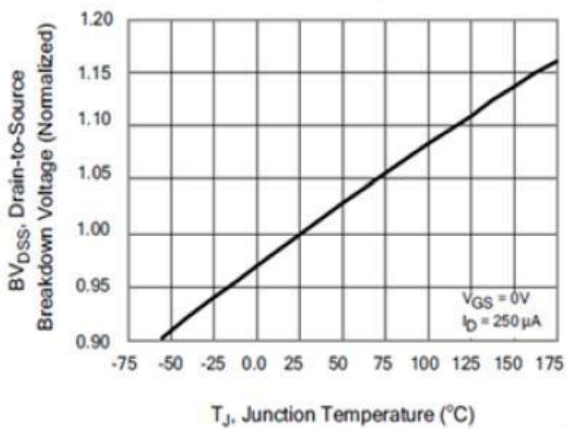
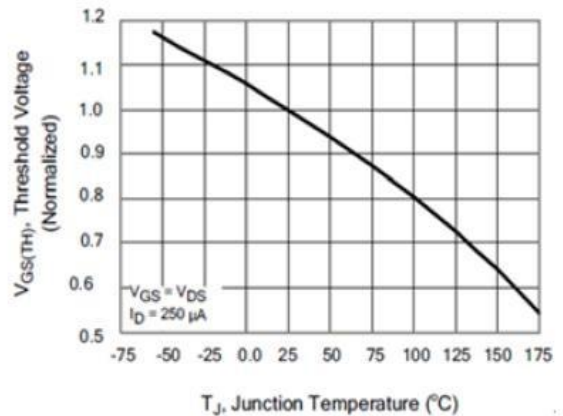


Figure 6. Typical Threshold Voltage vs Junction Temperature



Typical Characteristics  $T_J = 25^\circ\text{C}$ , unless otherwise noted

Figure 7. Capacitance

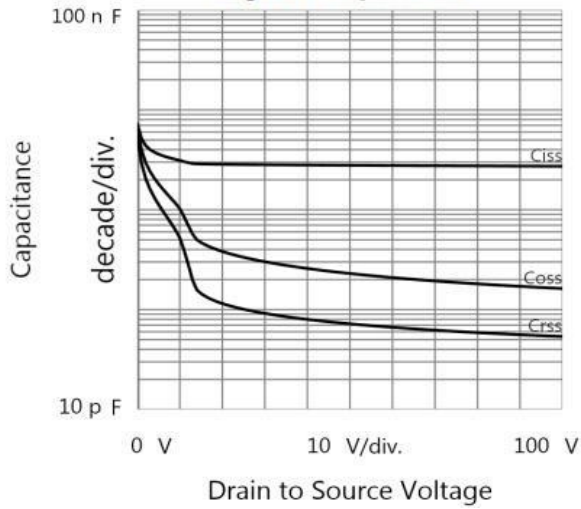


Figure 8. Gate Charge

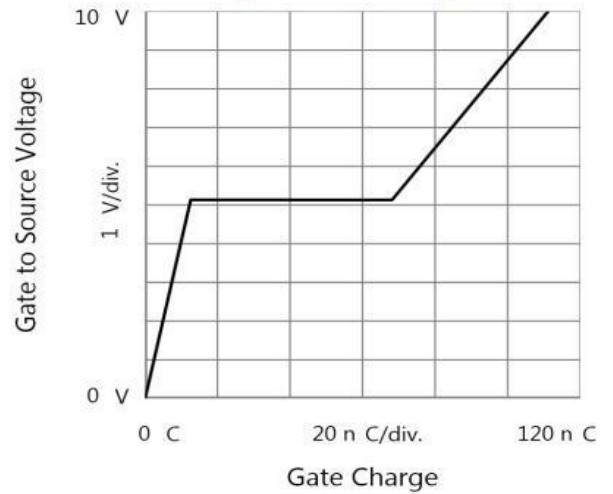


Figure 9. Transient Thermal Impedance  
TO-247, TO-3P

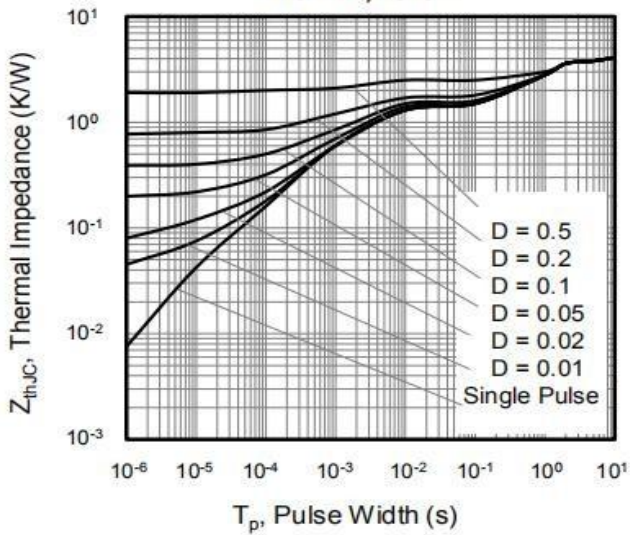


Figure 10. Maximum Forward Bias Safe  
Operating Area

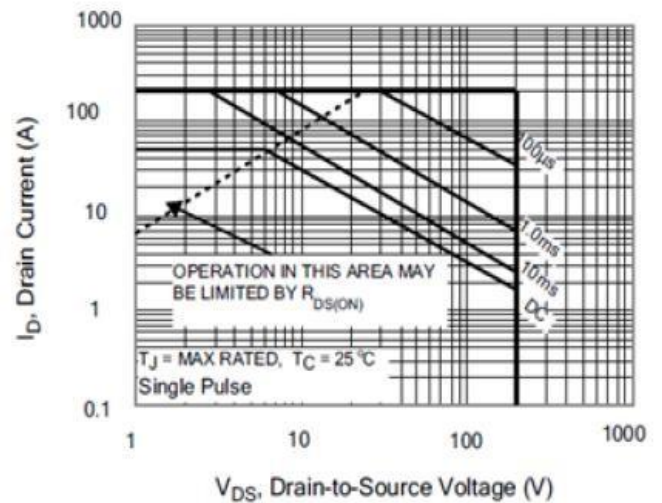


Figure A: Gate Charge Test Circuit and Waveform

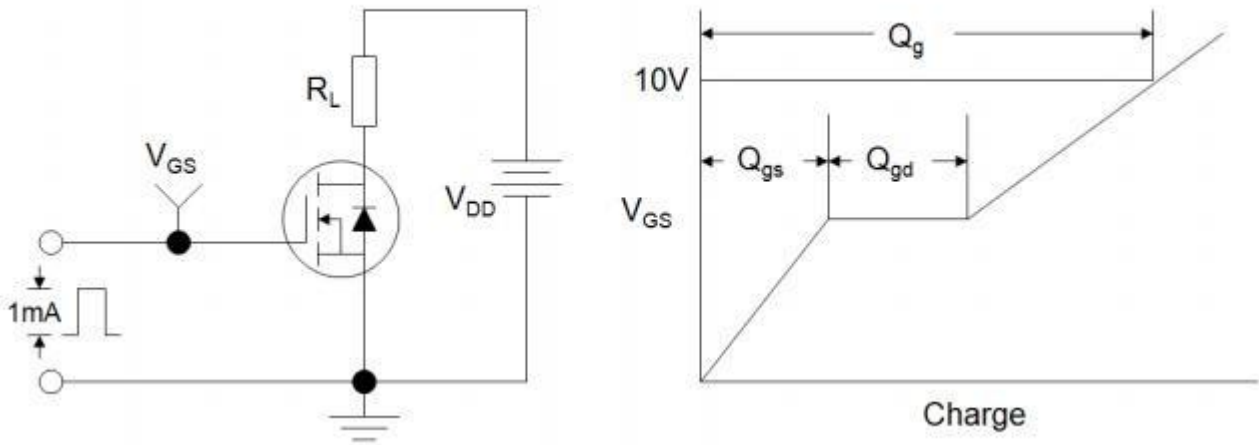


Figure B: Resistive Switching Test Circuit and Waveform

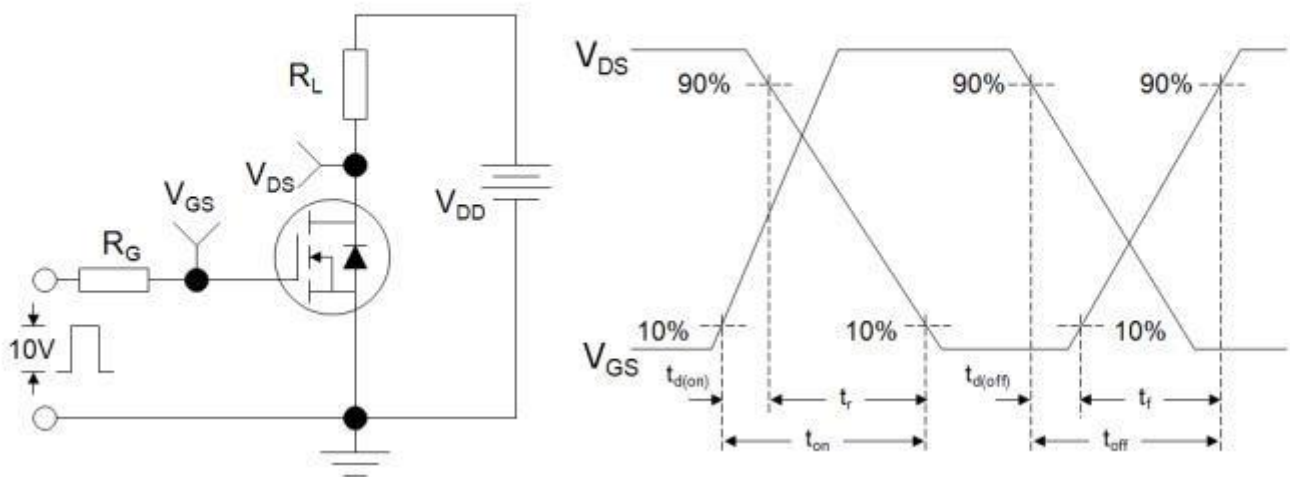
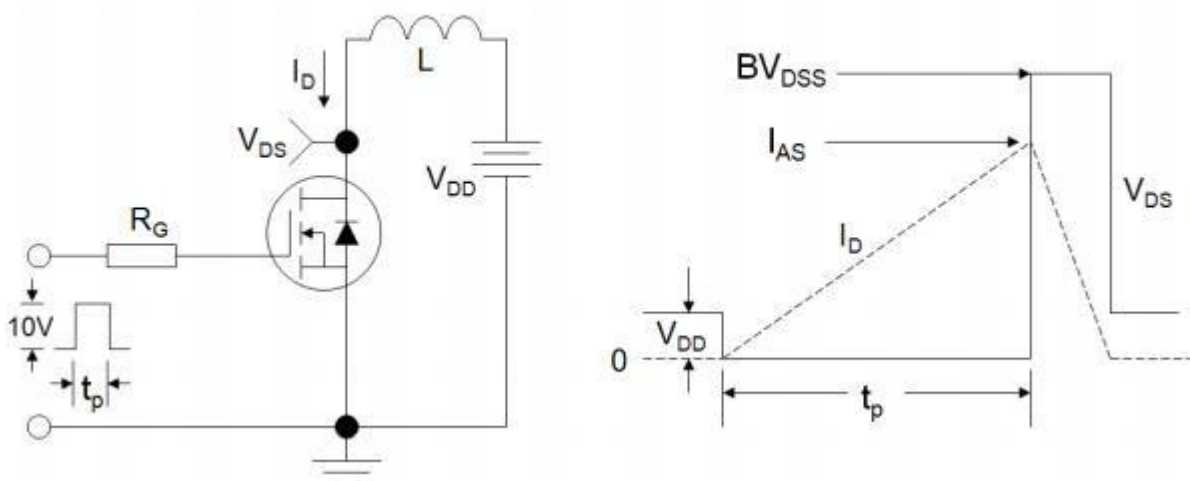
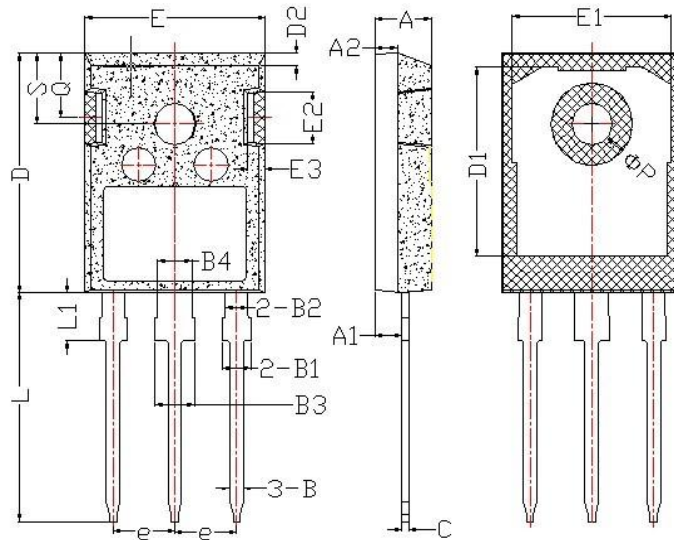


Figure C: Unclamped Inductive Switching Test Circuit and Waveform



Package Description



Items	Values(mm)	
	MIN	MAX
A	4.6	5.2
A1	2,2	2.6
B	0.9	1.4
B1	1.75	2.35
B2	1.75	2.15
B3	2.8	3.35
B4	2.8	3.15
C	0.5	0.7
D	20.60	21.30
D1	16	18
E	15.5	16.10
E1	13	14.7
E2	3.80	5.3
E3	0.8	2.60
e	5.2	5.7
L	19	20.5
L1	3.9	4.6
ΦP	2.5	3.70
Q	5.2	6.00
S	5.8	6.6



**NOTE:**

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. Please do not exceed the absolute maximum ratings of the device when circuit designing.
2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
3. MOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. Shenzhen Minos reserves the right to make changes in this specification sheet and is subject to change without prior notice.

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