

Description

MP20N40, the silicon N-channel Enhanced MOSFETs, is obtained by advanced MOSFET technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor is suitable device for SMPS, high speed switching and general purpose applications.

KEY CHARACTERISTICS

Parameter	Value	Unit
V_{DS}	400	V
I_D	20	A
$R_{DS(ON).Typ}$	0.22	Ω

FEATURES

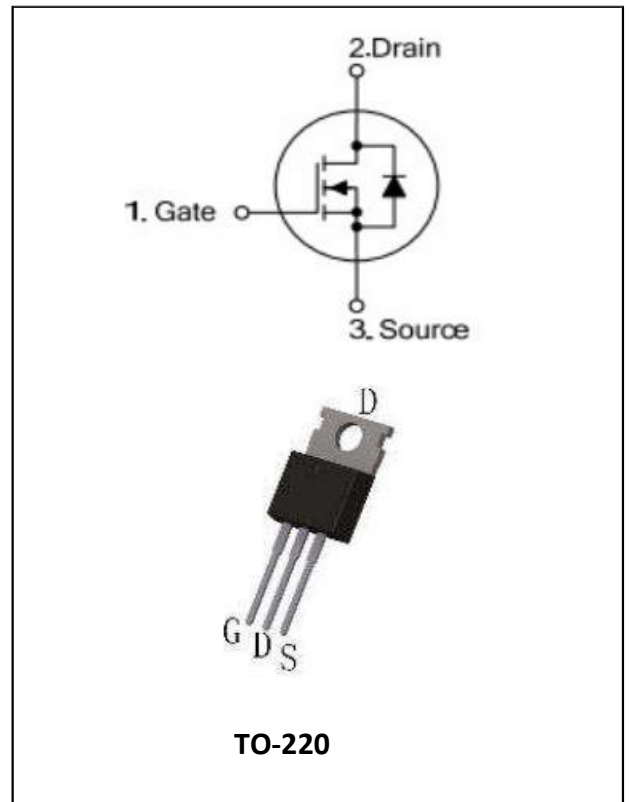
- ① Fast Switching
- ② Low C_{rss}
- ③ 100% avalanche tested
- ④ Improved dv/dt capability
- ⑤ RoHS product

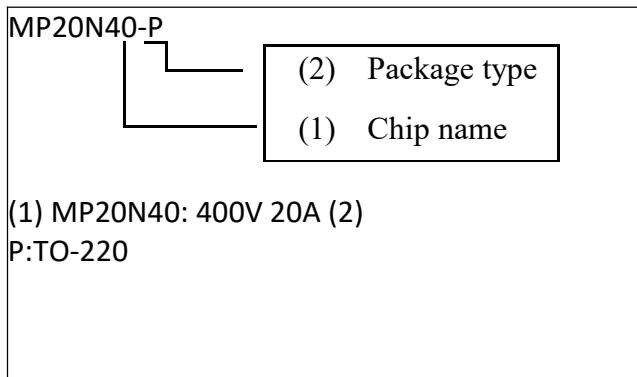
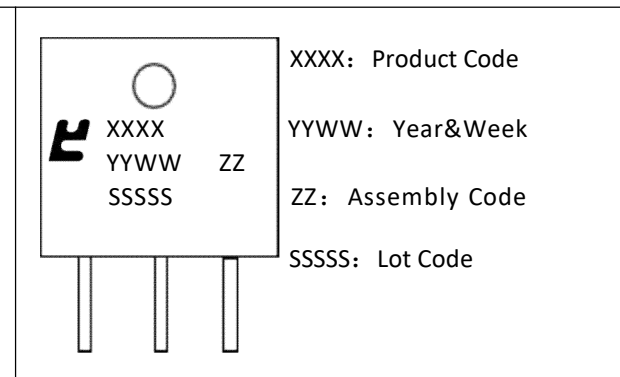
APPLICATIONS

- ① High frequency switching mode power supply
- ② Electronic ballast

ORDERING INFORMATION

Ordering Codes	Package	Product Code	Packing
MP20N40-P	TO-220	20N40	Tube



<p>MP20N40-P</p>  <p>(1) MP20N40: 400V 20A (2) P:TO-220</p>	 <p>XXXX: Product Code YYWW: Year&Week ZZ: Assembly Code SSSS: Lot Code</p>
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ABSOLUTE RATINGS

at TC = 25°C, unless otherwise specified

Symbol	Parameter	Rating	Units
V _{DSS}	Drain-to-Source Voltage	400	V
I _D	Continuous Drain Current	20	A
	Continuous Drain Current TC = 100 °C	12.6	A
I _{DM}	Pulsed Drain Current ^(Note1)	76	A
V _{GS}	Gate-to-Source Voltage	±30	V
E _{AS}	Single Pulse Avalanche Energy ^(Note2)	900	mJ
dv/dt	Peak Diode Recovery dv/dt ^(Note3)	5.0	V/ns
P _D	Power Dissipation TO-220	278	W
	Derating Factor above 25°C	2.2	W/°C
T _J , T _{stg}	Operating Junction and Storage Temperature Range	150, -55 to 150	°C
T _L	Maximum Temperature for Soldering	300	°C

Thermal characteristics

Thermal characteristics TO-220

Symbol	Parameter	RATINGS	Units
R _{θJC}	Junction-to-Case	0.45	°C/W
R _{θJA}	Junction-to-Ambient	62.5	°C/W

Electrical Characteristics

at TC = 25°C, unless otherwise specified

OFF Characteristics						
Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	400	--	--	V
$\Delta BVDSS/\Delta T_J$	Bvdss Temperature Coefficient	$I_D=250\mu A$, Reference 25°C	--	0.45	--	V/°C
I_{DSS}	Drain to Source Leakage Current	$V_{DS}=400V, V_{GS}=0V$, $T_j=25^\circ C$	--	--	1	μA
		$V_{DS}=320V, V_{GS}=0V$, $T_j=125^\circ C$	--	--	10	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	$V_{GS}=+30V$	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	$V_{GS}=-30V$	--	--	-100	nA

ON Characteristics						
Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On- Resistance	$V_{GS}=10V, I_D=4A^{(Note4)}$	--	0.22	0.27	Ω
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu A^{(Note4)}$	2	3	4	V
g_{fs}	Forward Transconductance	$V_{DS}=15V$, $I_D=9.5A^{(Note4)}$	--	10.0	--	S

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
R_g	Gate resistance	$f=1.0MHz$	--	1.4	--	Ω
C_{iss}	Input Capacitance	$V_{GS}=0V$ $V_{DS}=25V$ $f=1.0MHz$	--	2300	--	PF
C_{oss}	Output Capacitance		--	210	--	
C_{rss}	Reverse Transfer Capacitance		--	3.3	--	

Switching Characteristics						
Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	$I_D=20A$ $V_{DD}=250V$ $V_{GS}=10V$ $R_G=10\Omega$	--	32	--	ns
t_r	Rise Time		--	26	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	80	--	
t_f	Fall Time		--	35	--	
Q_g	Total Gate Charge	$I_D=20A$ $V_{DD}=320V$ $V_{GS}=10V$	--	40	--	nC
Q_{gs}	Gate to Source Charge		--	12.5	--	
Q_{gd}	Gate to Drain ("Miller") Charge		--	10.5	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current (Body Diode)	$T_C=25^\circ C$	--	--	20	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	76	A
V_{SD}	Diode Forward Voltage	$I_S=20A$, $V_{GS}=0V$ (Note4)	--	--	1.2	V
T_{rr}	Reverse Recovery Time	$I_S=20A$, $T_j=25^\circ C$ $dI_F/dt=100A/\mu s$,	--	285	--	ns
Q_{rr}	Reverse Recovery Charge		--	3900	--	nC

Note1: Pulse width limited by maximum junction temperature

Note2: $L=10mH$, $V_{DS}=50V$, Start $T_J=25^\circ C$

Note3: $I_{SD}=20A$, $dI/dt \leq 100A/\mu s$, $V_{DD} \leq BV_{DS}$, Start $T_J=25^\circ C$

Note4: Pulse width $t_p \leq 300\mu s$, $\delta \leq 2\%$

Characteristics Curves

Figure 1a Safe Operating Area (No FullPAK)

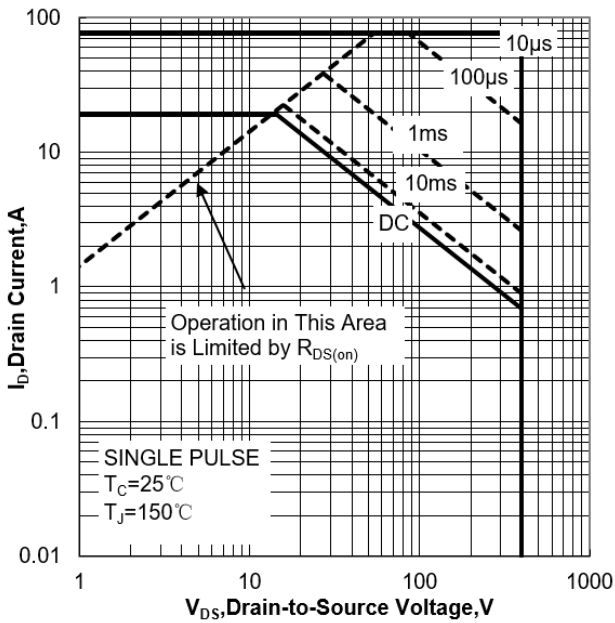


Figure 1b Safe Operating Area (FullPAK)

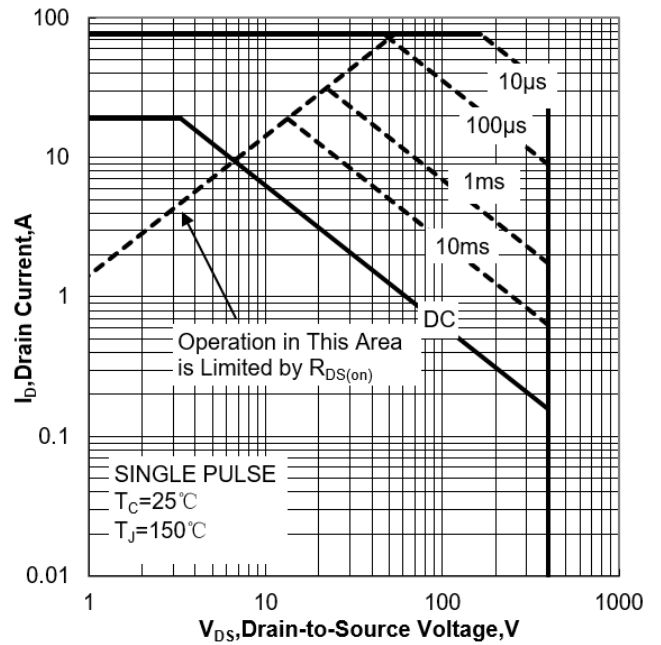


Figure 2a Power Dissipation (No FullPAK)

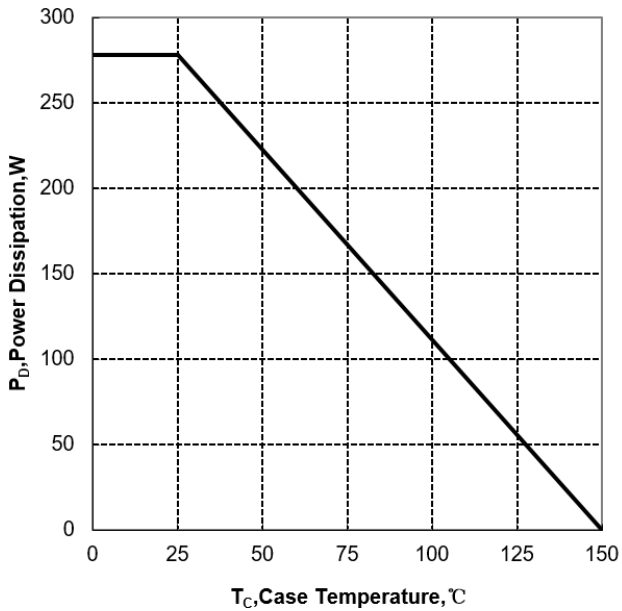


Figure 2b Power Dissipation (FullPAK)

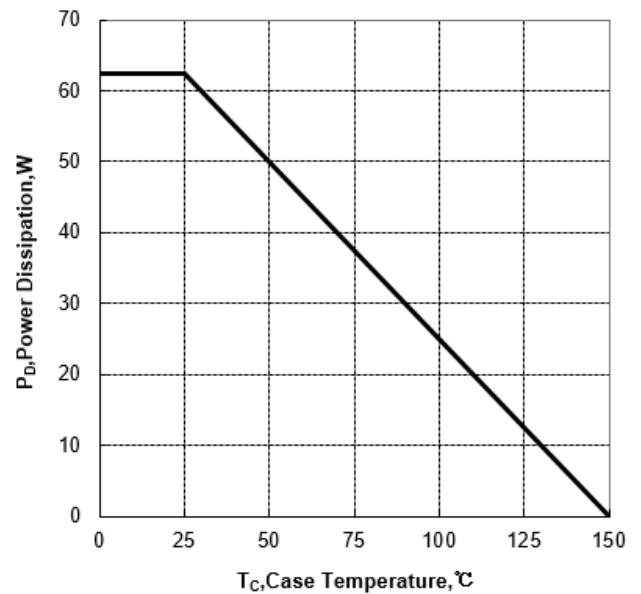


Figure 3a Max Thermal Impedance (No FullPAK)

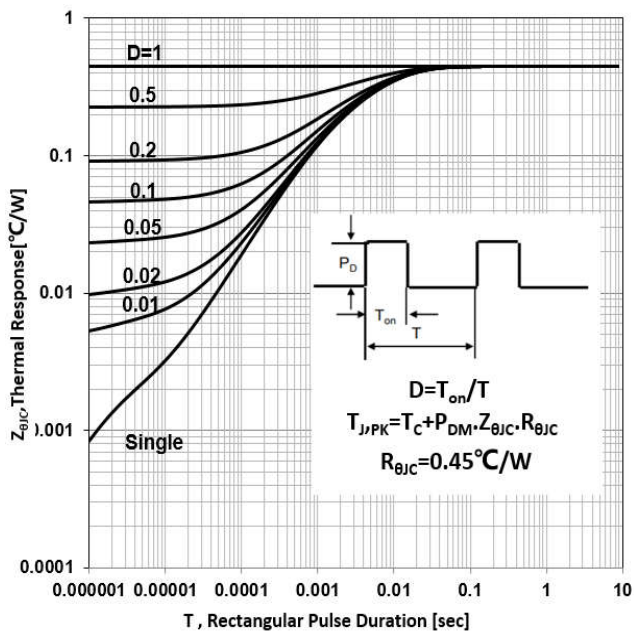


Figure 3b Max Thermal Impedance (FullPAK)

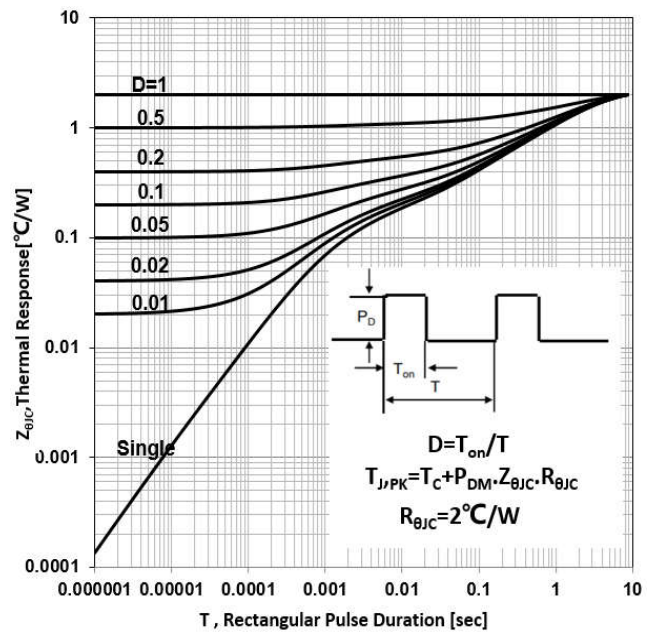


Figure 4 Typical Output Characteristics

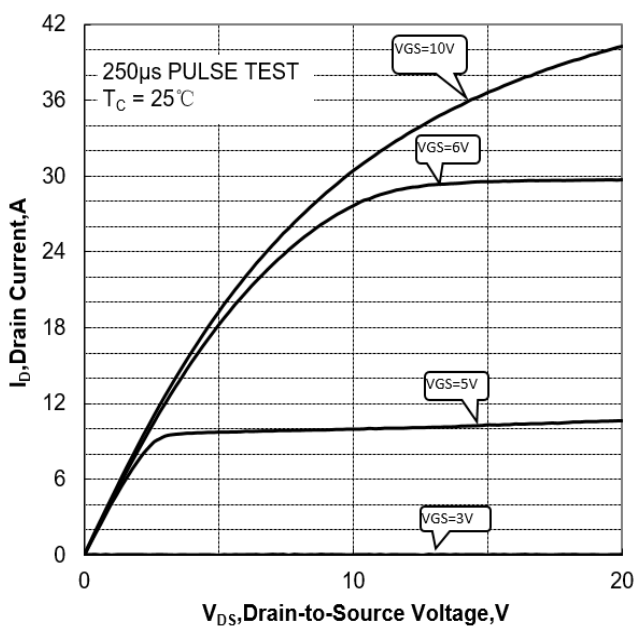


Figure 5 Typical Transfer Characteristics

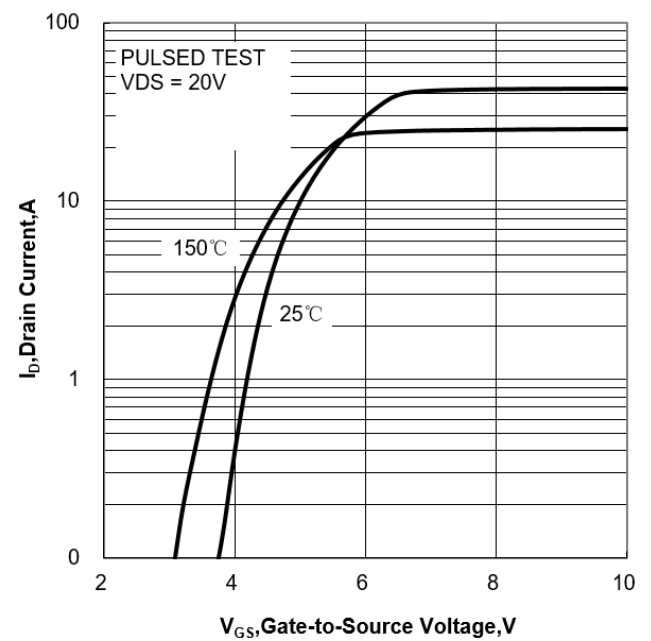


Figure 6 Typical Drain to Source ON Resistance vs Drain Current

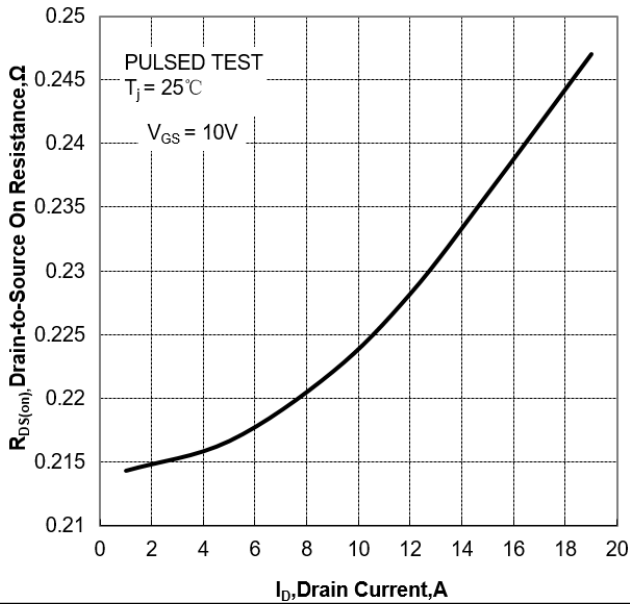


Figure 7 Typical Drian to Source on Resistance vs Junction Temperature

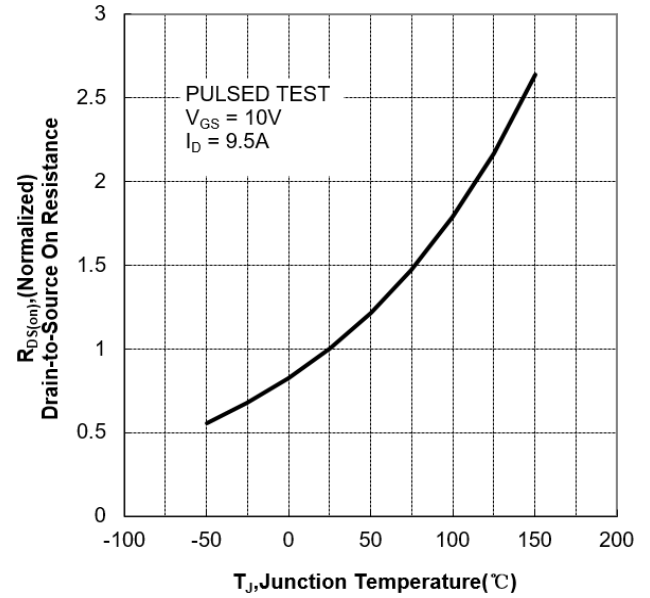


Figure 8 Typical Theshold Voltage vs Junction Temperature

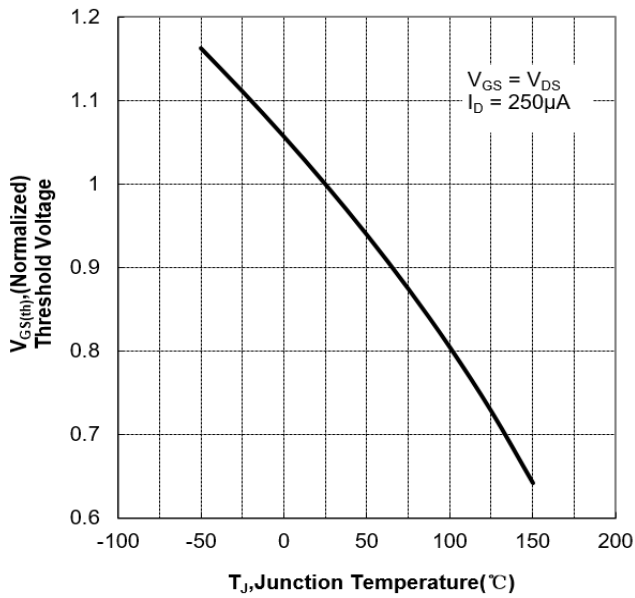


Figure 9 Typical Breakdown Voltage vs Junction Temperature

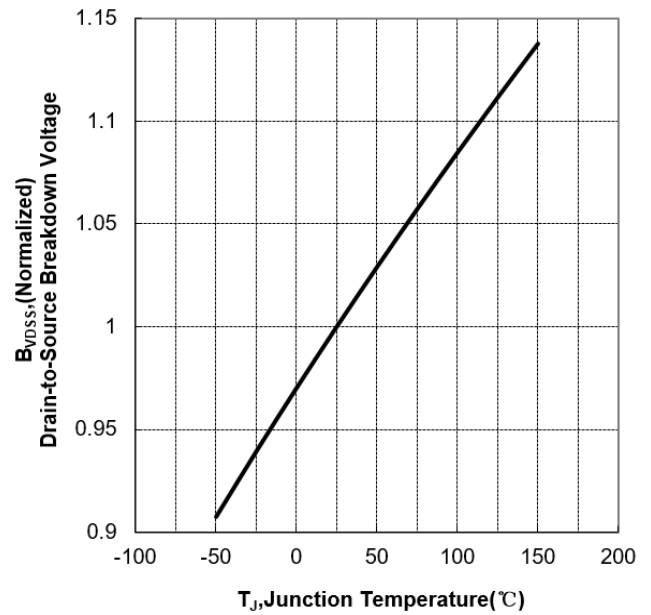


Figure 10 Typical Capacitance vs Drain to Source Voltage

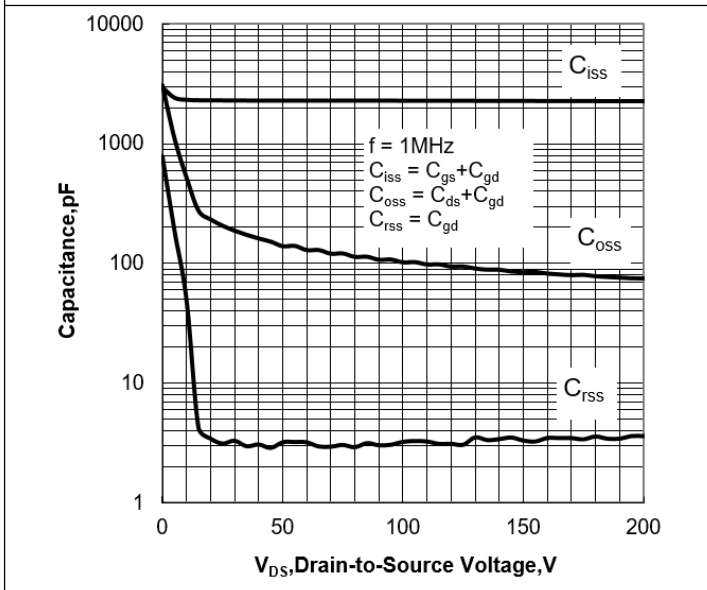
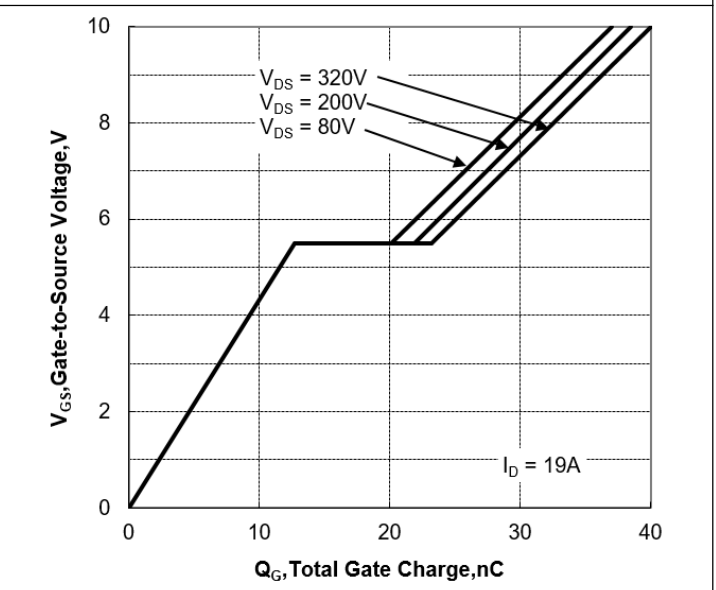
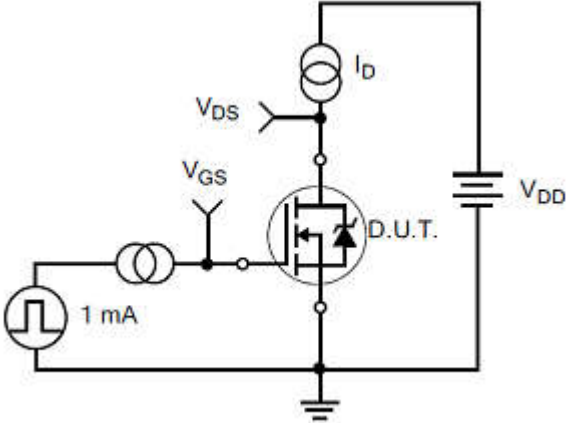
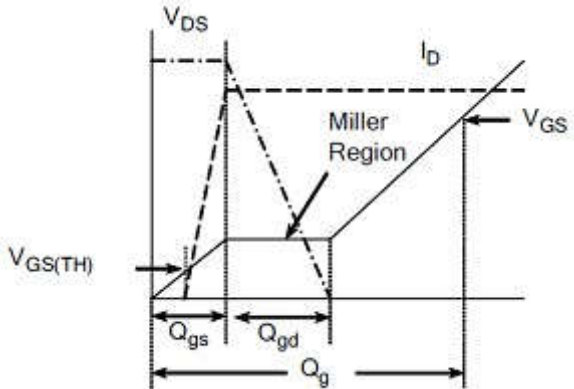
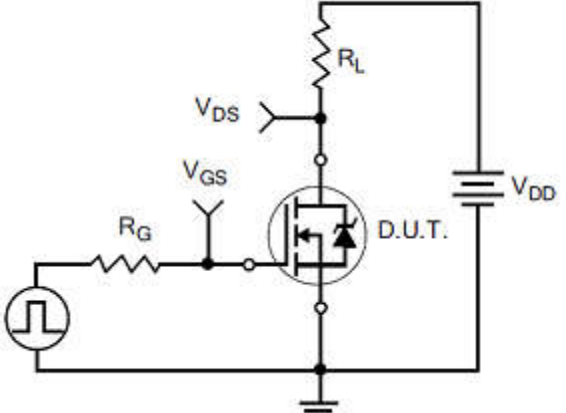
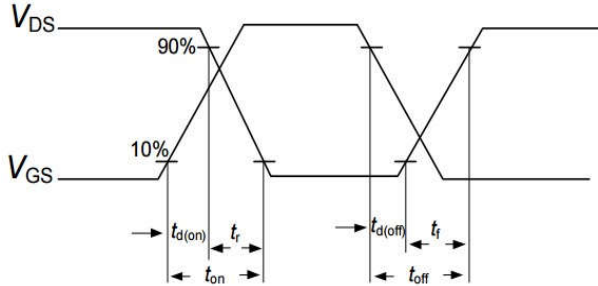
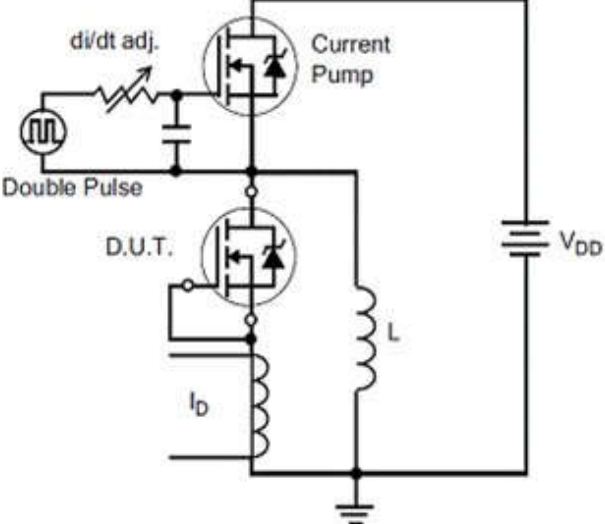
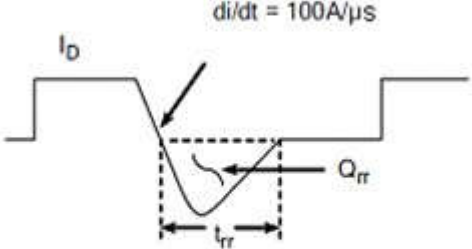
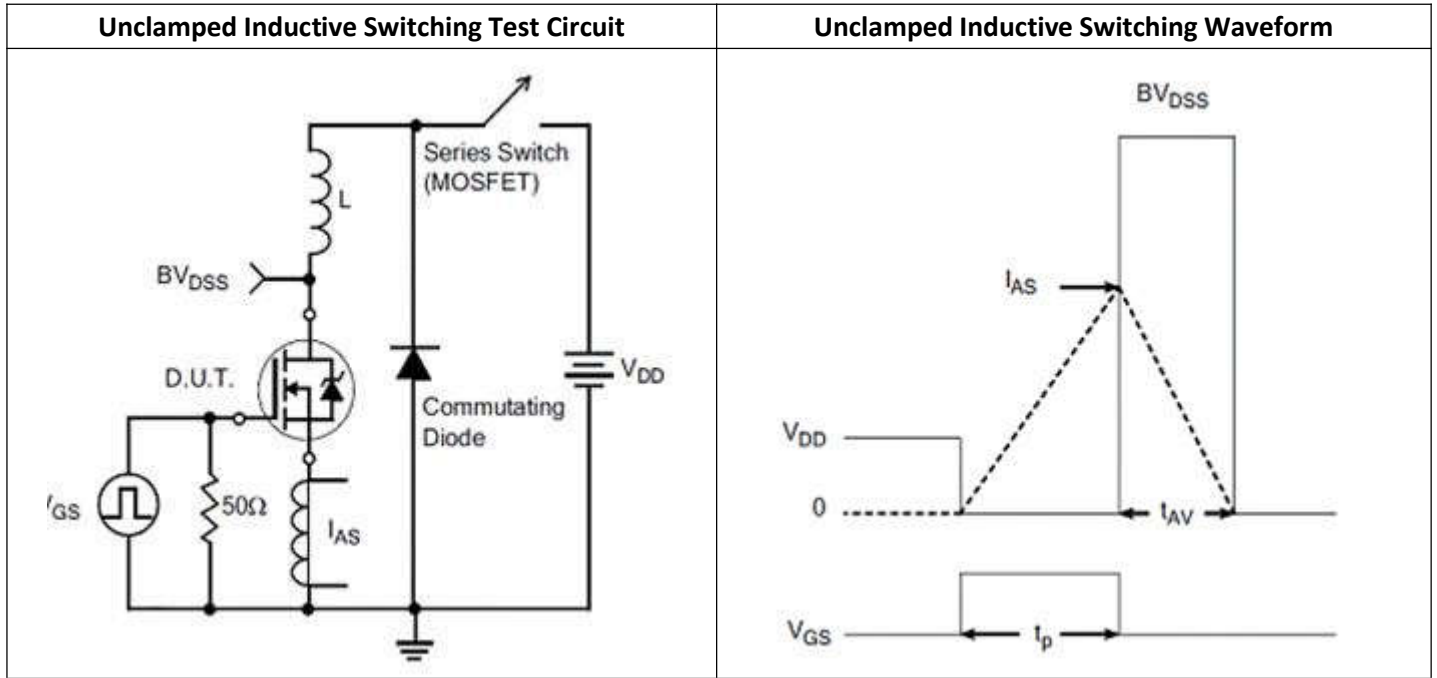


Figure 11 Typical Gate Charge vs Gate to Source Voltage

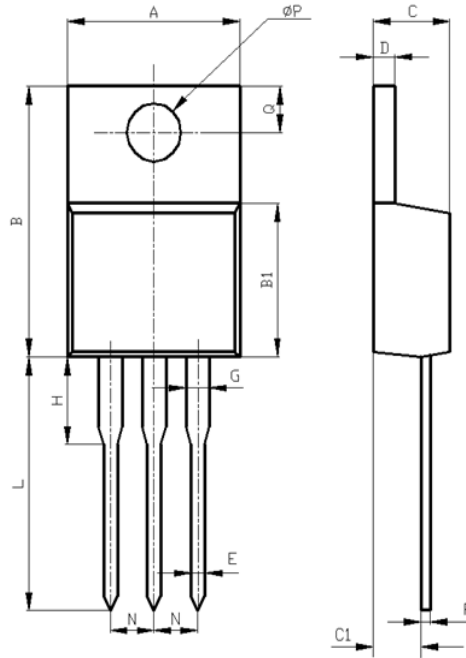


Test Circuit and Waveform

Gate Charge Test Circuit	Gate Charge Waveforms
 <p>The diagram shows a MOSFET (D.U.T.) in a common-emitter configuration. The gate is driven by a 1 mA current source. The drain is connected to a load resistor and a current source I_D. The supply voltage is V_{DD}. The gate-source voltage is V_{GS} and the drain-source voltage is V_{DS}.</p>	 <p>The graph shows V_{GS} and I_D versus time. Key parameters include $V_{GS(TH)}$ (threshold voltage), Q_{gs} (gate-source charge), Q_{gd} (gate-drain charge), Q_g (total gate charge), and the Miller Region where V_{GS} is constant while V_{DS} is high.</p>
Resistive Switching Test Circuit	Resistive Switching Waveforms
 <p>The diagram shows a MOSFET (D.U.T.) in a common-emitter configuration. The gate is driven by a current source through a resistor R_G. The drain is connected to a load resistor R_L and a supply voltage V_{DD}. The gate-source voltage is V_{GS} and the drain-source voltage is V_{DS}.</p>	 <p>The graph shows V_{DS} and V_{GS} versus time. Key parameters include $t_{d(on)}$, t_r, t_{on}, $t_{d(off)}$, t_f, and t_{off}. The V_{DS} waveform shows a 90% rise and 10% fall.</p>
Diode Reverse Recovery Test Circuit	Diode Reverse Recovery Waveform
 <p>The diagram shows a MOSFET (D.U.T.) in a common-emitter configuration. The gate is driven by a double pulse source through a di/dt adjustable circuit. The drain is connected to a load resistor L and a supply voltage V_{DD}. The gate-source voltage is V_{GS} and the drain-source voltage is V_{DS}. The current source is labeled "Current Pump" and the load is I_D.</p>	 <p>The graph shows I_D versus time. Key parameters include $di/dt = 100A/\mu s$ and Q_{rr} (reverse recovery charge).</p>



Package Description



Items	Values(mm)	
	MIN	MAX
A	9.60	10.6
B	15.0	16.0
B1	8.90	9.50
C	4.30	4.80
C1	2.30	3.10
D	1.20	1.40
E	0.70	0.90
F	0.30	0.60
G	1.17	1.37
H	2.70	3.80
L	12.6	14.8
N	2.34	2.74
Q	2.40	3.00
Ø P	3.50	3.90

TO-220 Package



NOTE:

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. Please do not exceed the absolute maximum ratings of the device when circuit designing.
2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
3. MOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. Shenzhen Minos reserves the right to make changes in this specification sheet and is subject to change without prior notice.

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