

100V N-Channel Power MOSFET

DESCRIPTION

The MPG150N10 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge. It can be used in a wide variety of applications.

KEY CHARACTERISTICS

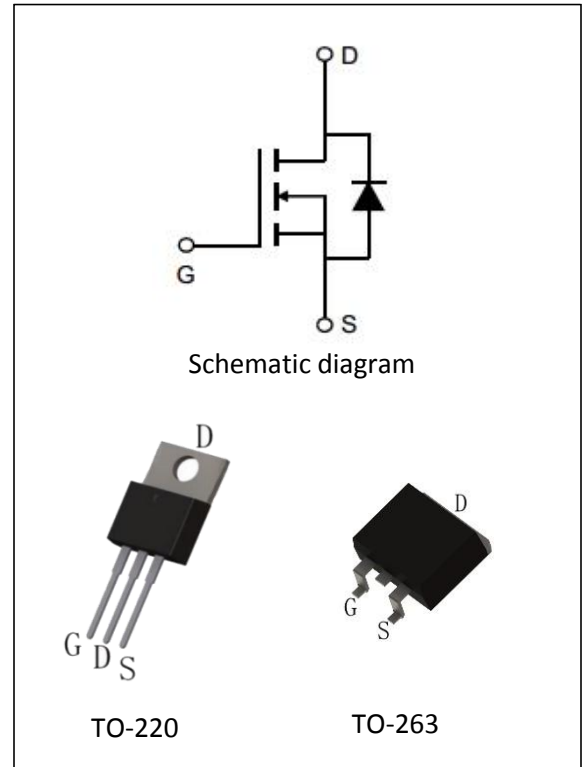
- ①  $V_{DS} = 100V, I_D = 150A R_{DS(ON)} < 6m\Omega @ V_{GS}=10V$
- ② Special process technology for high ESD capability
- ③ High density cell design for lower  $R_{dson}$
- ④ Fully characterized avalanche voltage and current
- ⑤ Good stability and uniformity with high EAS
- ⑥ Excellent package for good heat dissipation

Application

- ① Power switching application
- ② Hard switched and High frequency circuits
- ③ Uninterruptible power supply

Package Marking And Ordering Information

Ordering Codes	Package	Product Code	Packing
MPG150N06-P	TO-220	MPG150N10P	Tube
MPG150N06-S	TO-263	MPG150N10S	Tape Reel



Absolute Maximum Ratings ( $T_A=25^\circ C$  unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	330	A
Drain Current-Pulsed (Note 1)	$I_{DM}$	720	A
Maximum Power Dissipation( $T_c=25^\circ C$ )	$P_D$	211	W
Single pulse avalanche energy(Note 2)	$E_{AS}$	1200	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance,Junction-to-Case	$R_{\theta JC}$	0.36	$^\circ C/W$
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**Electrical Characteristics (TA=25 °C unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	100	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=100V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V
Drain-Source On-State Resistance <sup>(Note 3)</sup>	$R_{DS(ON)}$	$V_{GS}=10V, I_D=50A$	-	5	6	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=10V, I_D=40A$	170	-	-	S
<b>Dynamic Characteristics</b>						
Input Capacitance	$C_{ISS}$	$V_{DS}=25V, V_{GS}=0V,$ $f=1.0MHz$	-	6600	-	pF
Output Capacitance	$C_{OSS}$		-	590	-	pF
Reverse Transfer Capacitance	$C_{RSS}$		-	210	-	pF
<b>Switching Characteristics</b> <sup>(Note 4)</sup>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=50V, I_D=20A,$ $V_{GS}=10V, R_{GEN}=3\Omega$	-	29	-	nS
Turn-on Rise Time	$t_r$		-	23	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	44	-	nS
Turn-Off Fall Time	$t_f$		-	15	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=50V, I_D=30A, V_{GS}=10V$	-	108	-	nC
Gate-Source Charge	$Q_{gs}$		-	29	-	nC
Gate-Drain Charge	$Q_{gd}$		-	40	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage	$V_{SD}$	$V_{GS}=0V, I_S=50A$	-	-	1.2	V

**Notes:**

- 1.Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2.EAS condition :T j=25 °C ,VDD=50V,VG=10V,L=1mH,Rg=25 $\Omega$
- 3.Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
- 4.Guaranteed by design, not subject to production.

Characteristics Curves

Figure 1 Output Characteristics

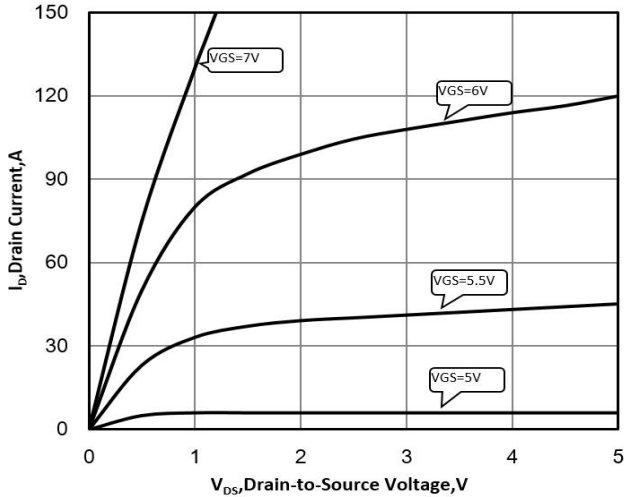


Figure 2 Transfer Characteristics

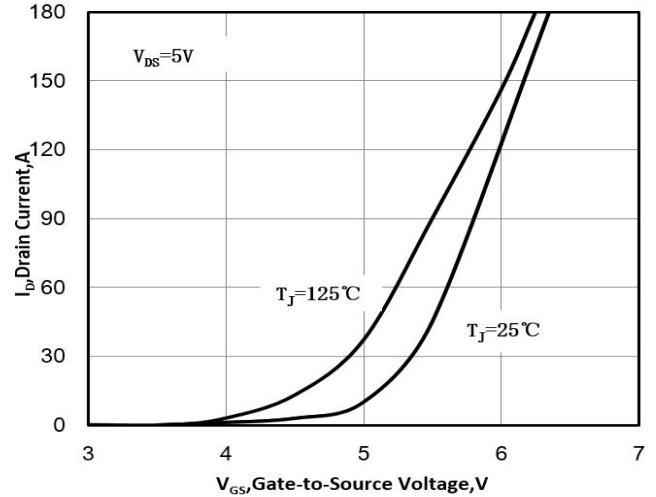


Figure 3 On-Resistance vs.  $I_D$  and  $V_{GS}$

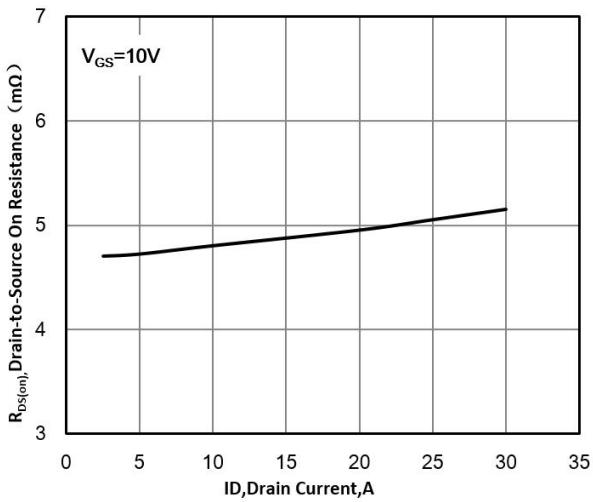


Figure 4 On-Resistance vs. Junction Temperature

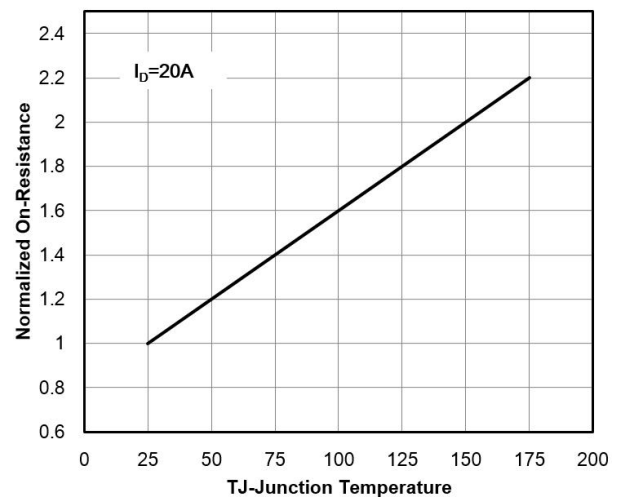


Figure 5 On-Resistance vs.  $V_{GS}$

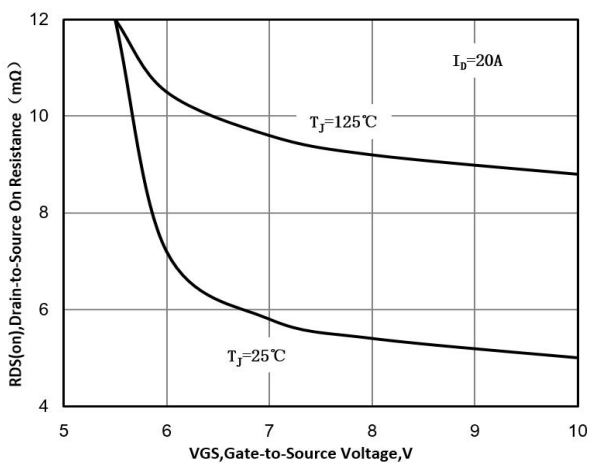


Figure 6 Body Diode Forward Voltage

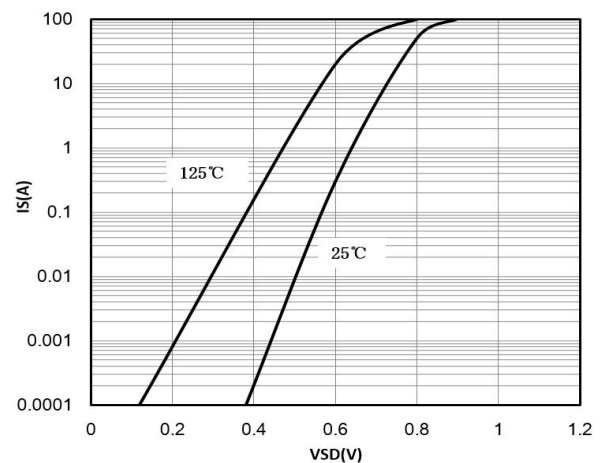


Figure 7 Gate-Charge Characteristics

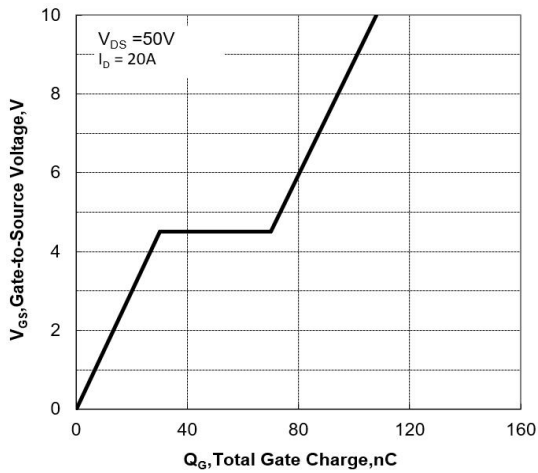


Figure 8 Capacitance Characteristics

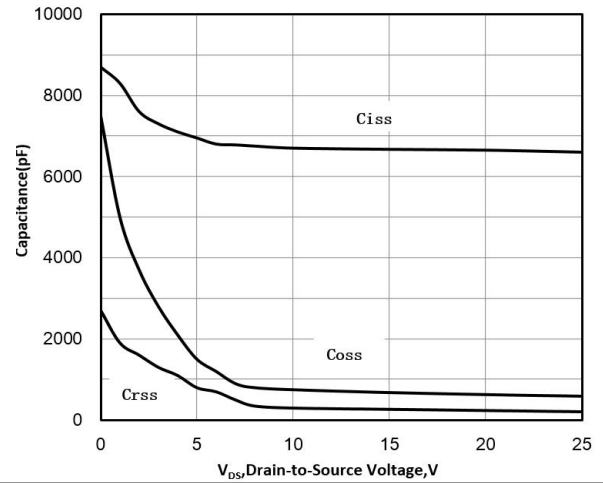


Figure 9 Maximum Forward Biased Safe Operation Area

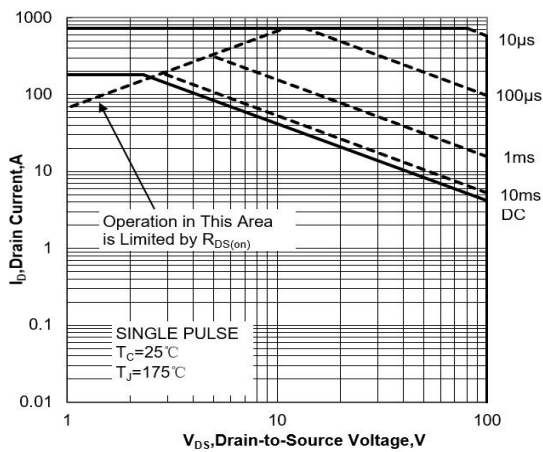


Figure 10 Single Pulse Power Rating Junction-to-Ambient

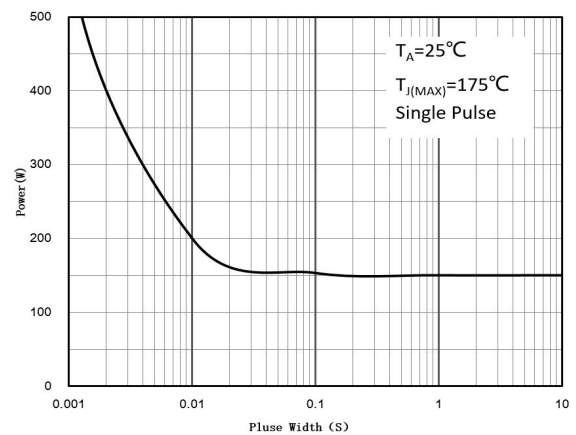
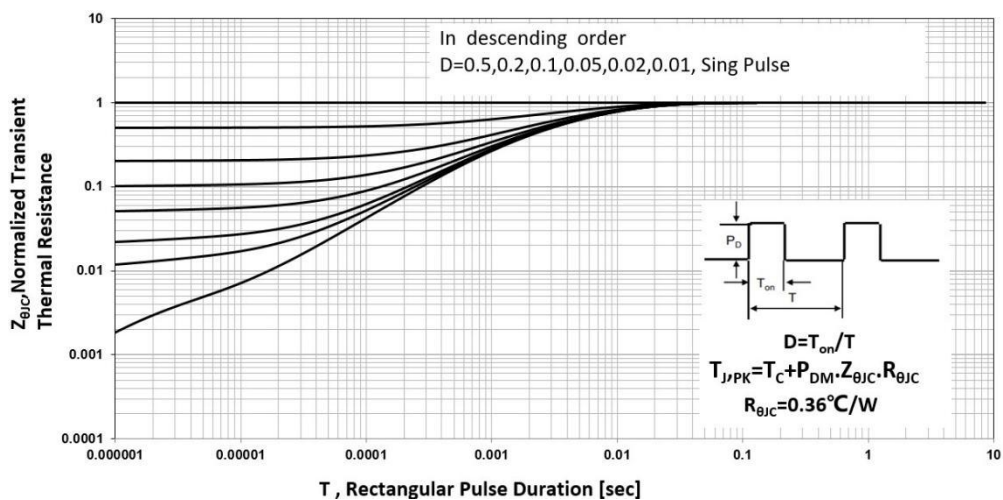
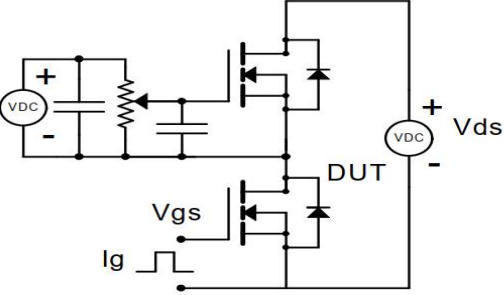
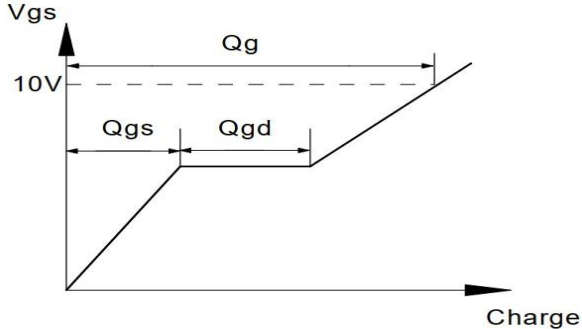
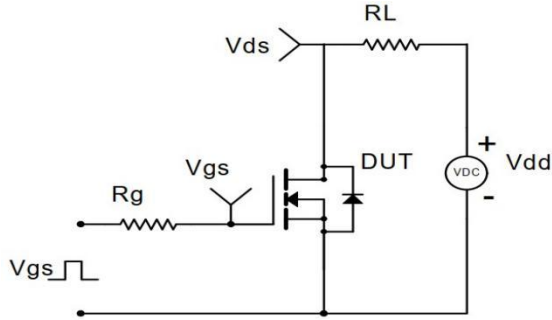
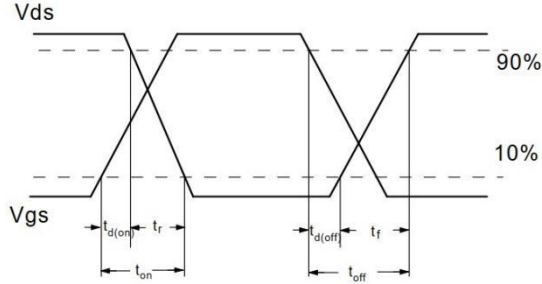
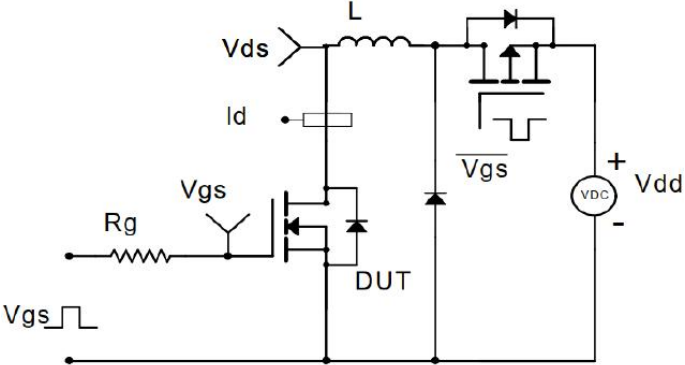
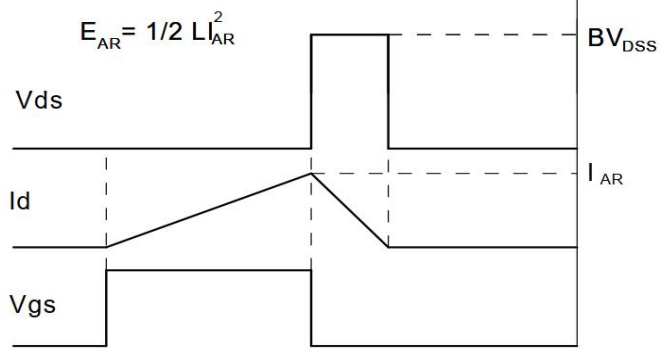
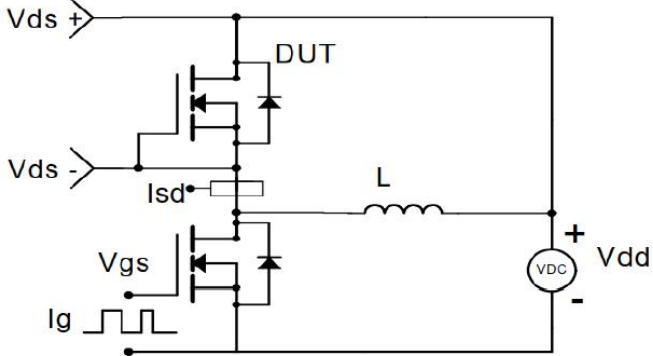
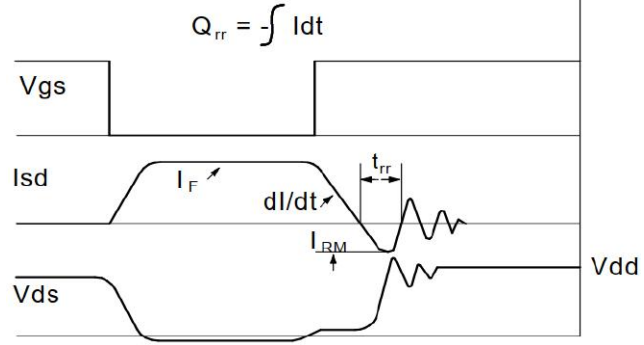


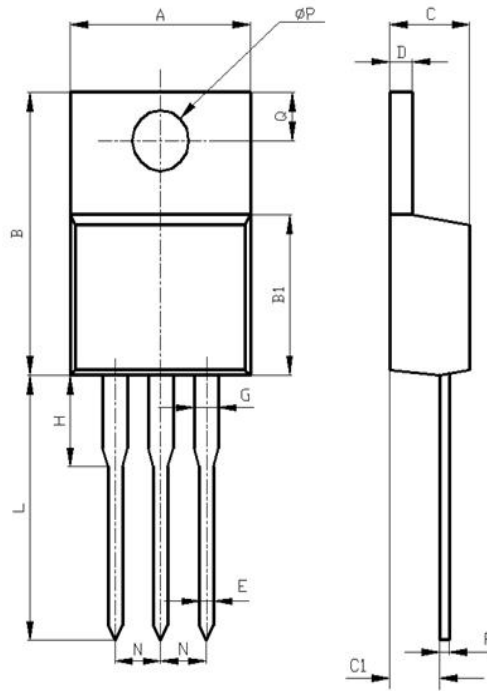
Figure 11 Normalized Maximum Transient Thermal Impedance



Test Circuit and Waveform

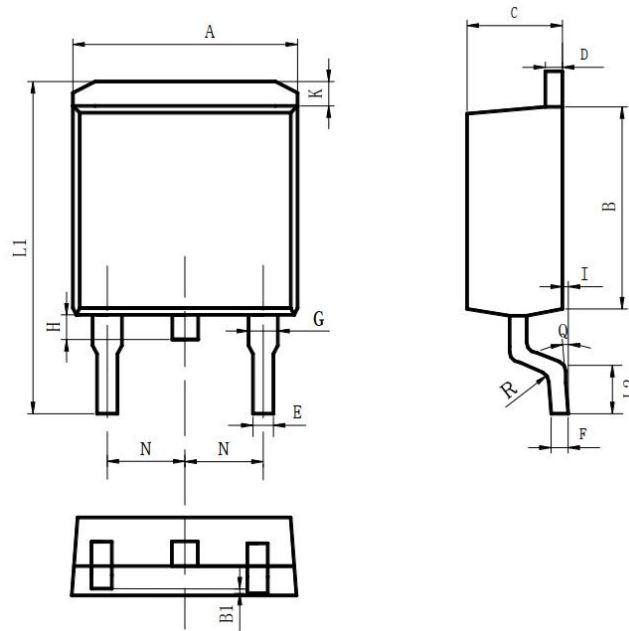
Gate Charge Test Circuit	Gate Charge Test Waveform
 <p>The diagram shows a MOSFET circuit for gate charge testing. A VDC source is connected to the drain through a resistor. The gate is driven by a pulse source Ig through a resistor. The MOSFET is connected to a load resistor and a diode. The DUT (Device Under Test) is the MOSFET.</p>	 <p>The graph plots Vgs (Gate-Source Voltage) against Charge. It shows a linear ramp up to 10V, a constant plateau, and a linear ramp down. The total area under the curve is labeled Qg. The area under the ramp up is Qgs, and the area under the ramp down is Qgd.</p>
Resistive Switching Test Circuit	Resistive Switching Test Waveforms
 <p>The diagram shows a MOSFET switching a load resistor RL. The drain is connected to Vdd through RL. The gate is driven by a pulse source Vgs through a resistor Rg. The DUT is the MOSFET.</p>	 <p>The graph shows Vds (Drain-Source Voltage) and Vgs (Gate-Source Voltage) waveforms. Vds transitions from 0V to Vdd and back. Vgs transitions from 0V to a plateau and back. Key timing parameters are labeled: t_d(on) (delay to turn on), t_r (rise time), t_on (turn on time), t_d(off) (delay to turn off), t_f (fall time), and t_off (turn off time). The 90% and 10% levels are indicated for the Vds transitions.</p>
Unclamped Inductive Switching (UIS) Test Circuit	Unclamped Inductive Switching (UIS) Test Waveforms
 <p>The diagram shows a MOSFET switching an inductive load L. The drain is connected to Vdd through L. The gate is driven by a pulse source Vgs through a resistor Rg. A diode is connected in parallel with the load. The DUT is the MOSFET.</p>	 <p>The graph shows Vds (Drain-Source Voltage), Id (Drain Current), and Vgs (Gate-Source Voltage) waveforms. Vds shows a sharp spike during the switching transient. Id shows a linear ramp up and down. Vgs shows a pulse. The equation <math>E_{AR} = 1/2 L I_{AR}^2</math> is shown. The peak Vds is labeled BV<sub>DSS</sub> and the peak Id is labeled I<sub>AR</sub>.</p>
Diode Recovery Test Circuit	Diode Recovery Test Waveforms
 <p>The diagram shows a MOSFET switching an inductive load L. The drain is connected to Vdd through L. The gate is driven by a pulse source Vgs through a resistor Rg. A diode is connected in parallel with the load. The DUT is the MOSFET.</p>	 <p>The graph shows Vgs (Gate-Source Voltage), Isd (Drain Current), and Vds (Drain-Source Voltage) waveforms. Vgs shows a pulse. Isd shows a linear ramp up and down. Vds shows a sharp spike during the switching transient. The equation <math>Q_{rr} = \int Idt</math> is shown. Key parameters are labeled: I<sub>F</sub> (forward current), dI/dt (rate of change of current), t<sub>rr</sub> (reverse recovery time), and I<sub>RM</sub> (reverse recovery current).</p>

Package Description



Items	Values(mm)	
	MIN	MAX
A	9.60	10.6
B	15.0	16.0
B1	8.90	9.50
C	4.30	4.80
C1	2.30	3.10
D	1.20	1.40
E	0.70	0.90
F	0.30	0.60
G	1.17	1.37
H	2.70	3.80
L	12.6	14.8
N	2.34	2.74
Q	2.40	3.00
Φ P	3.50	3.90

TO-220 package



Items	Values(mm)	
	MIN	MAX
A	9.80	10.40
B	8.90	9.50
B1	0	0.10
C	4.40	4.80
D	1.16	1.37
E	0.70	0.95
F	0.30	0.60
G	1.07	1.47
H	1.30	1.80
K	0.95	1.37
L1	14.50	16.50
L2	1.60	2.30
I	0	0.2
Q	0°	8°
R	0.4	
N	2.39	2.69

TO-263 package



**NOTE:**

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. Please do not exceed the absolute maximum ratings of the device when circuit designing.
2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
3. MOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. Shenzhen Minos reserves the right to make changes in this specification sheet and is subject to change without prior notice.

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