

1. Description

MPT65N08, the N-channel Enhanced Power MOSFETs, is obtained by advanced double trench technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. This is suitable device for motor drivers and high speed switching applications.

KEY CHARACTERISTICS

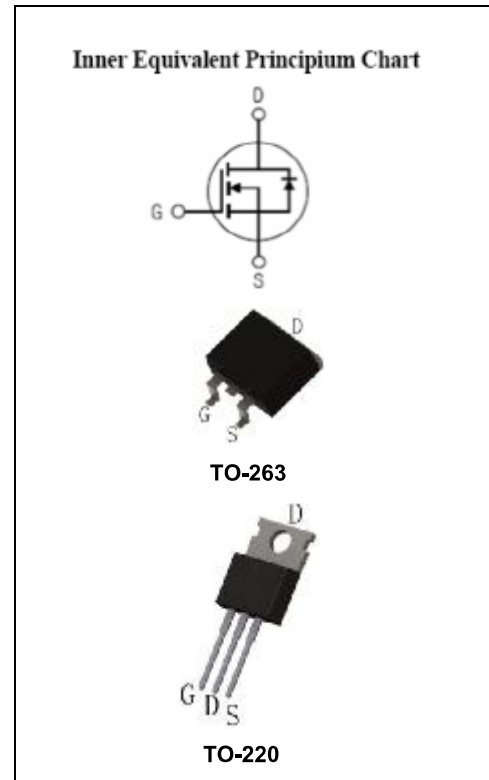
Parameter	Value	Unit
V_{DSS}	85	V
I_D	80	A
$R_{DS(on),typ}$	5.4	$m\Omega$

FEATURES

- Fast Switching
- Low On-Resistance ($R_{DS(on)} \leq 6.5m\Omega$)
- Low Gate Charge
- Low Reverse transfer capacitances
- High avalanche ruggedness
- RoHS product

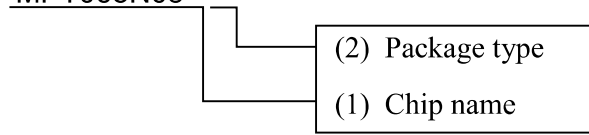
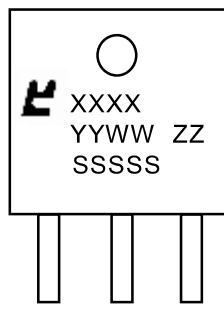
APPLICATIONS

- Switching applications
- Motor drivers



ORDERING INFORMATION

Ordering Codes	Package	Product Code	Packing
MPS065N08G-B	TO-263	065N08	Reel
MPT065N08G-P	TO-220	065N08	Tube

<p>MPT065N08</p>  <p>(1) MPT065N08: 6.5mΩ/85V (2) B: TO-263 P: TO-220</p>	 <p>XXXX: Product Code YYWW: Year&Week ZZ: Assembly Code SSSSS: Lot Code</p>
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2. ABSOLUTE RATINGS

at $T_C=25^{\circ}\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-Source Voltage	85	V
I_D	Continuous Drain Current, Silicon Limited	118	A
	Continuous Drain Current, Package Limited	80	A
	Continuous Drain Current @ $T_C=100^{\circ}\text{C}$, Silicon Limited	75	A
I_{DM} ^{Note1}	Pulsed Drain Current	320	A
V_{GS}	Gate-Source Voltage	± 20	V
E_{AS} ^{Note2}	Avalanche Energy	100	mJ
P_D	Power Dissipation	156.2	W
	Derating Factor above 25°C	1.25	W/ $^{\circ}\text{C}$
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150, -55 to 150	$^{\circ}\text{C}$
T_L	Maximum Temperature for Soldering	260	$^{\circ}\text{C}$

Note1: Repetitive Rating: Pulse width limited by maximum junction temperature

Note2: $L=0.5\text{mH}$, $I_{as}=20\text{A}$, Start $T_J=25^{\circ}\text{C}$

3. Thermal characteristics

Symbol	Parameter	Max	Units
$R_{\theta JC}$	thermal resistance, Junction-Case	0.8	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	thermal resistance, Junction-Ambient	62.5	$^{\circ}\text{C}/\text{W}$

4. Electrical Characteristics

at $T_C=25^{\circ}\text{C}$, unless otherwise specified

OFF Characteristics						
Symbol	Parameter	Test Conditions	Values			Units
			Min	Typ	Max	
V_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	85	--	--	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=85\text{V}, V_{GS}=0\text{V}$	--	--	1	μA
		$V_{DS}=68\text{V}, V_{GS}=0\text{V}$ @ $T_C=125^{\circ}\text{C}$	--	--	100	μA
$I_{GSS(F)}$	Gate-Source Forward Leakage	$V_{GS}=+20\text{V}$	--	--	100	nA
$I_{GSS(R)}$	Gate-Source Reverse Leakage	$V_{GS}=-20\text{V}$	--	--	-100	nA

ON Characteristics

Symbol	Parameter	Test Conditions	Values			Unit
			Min	Typ	Max	
$R_{DS(on)}$	Drain-Source On-Resistance	$V_{GS}=10V, I_D=50A$	--	5.4	6.5	$m\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0	3.0	4.0	V

Pulse width $t_p \leq 300\mu s, \delta \leq 2\%$

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Values			Units
			Min	Typ	Max	
C_{iss}	Input Capacitance	$V_{DS}=40V,$ $V_{GS}=0,$ $f=1MHz$	--	3217	--	pF
C_{oss}	Output Capacitance		--	510	--	
C_{rss}	Reverse Transfer Capacitance		--	13.5	--	
Q_g	Total Gate Charge	$V_{DD}=40V,$ $I_D=50A,$ $V_{GS}=10V$	--	64	--	nC
Q_{gs}	Gate-Source charge		--	18.4	--	
Q_{gd}	Gate-Drain charge		--	19	--	

Switching Characteristics

Symbol	Parameter	Test Conditions	Values			Units
			Min	Typ	Max	
$t_{d(on)}$	Turn-On Delay Time	$V_{DD}=40V,$ $I_D=50A,$ $V_{GS}=10V,$ $R_G=3\Omega,$ Resistive Load	--	17	--	ns
t_r	Rise Time		--	30	--	
$t_{d(off)}$	Turn-Off Delay Time		--	37	--	
t_f	Fall Time		--	20	--	

Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions	Values			Units
			Min	Typ	Max	
I_S	Continuous Source Current		--	--	80	A
I_{SM}	Maximum Pulsed Current		--	--	320	A
V_{SD}	Diode Forward Voltage	$V_{GS}=0V, I_S=50A$	--	--	1.2	V
T_{rr}	Reverse Recovery Time	$I_S=20A,$ $di/dt=100A/us$	--	57	--	ns
Q_{rr}	Reverse Recovery Charge		--	65	--	μC

5. Characteristics Curves

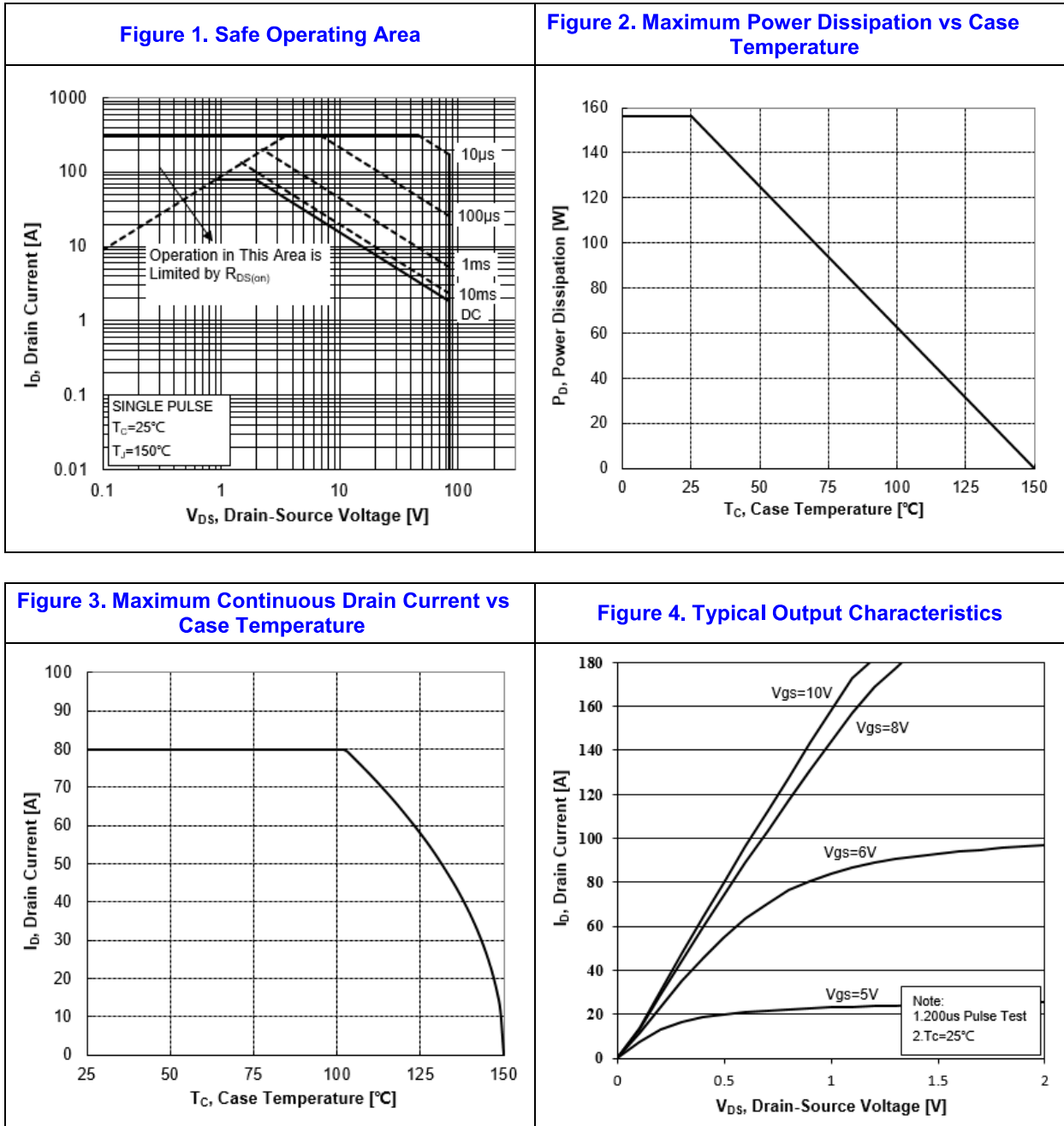


Figure 5. Transient Thermal Impedance

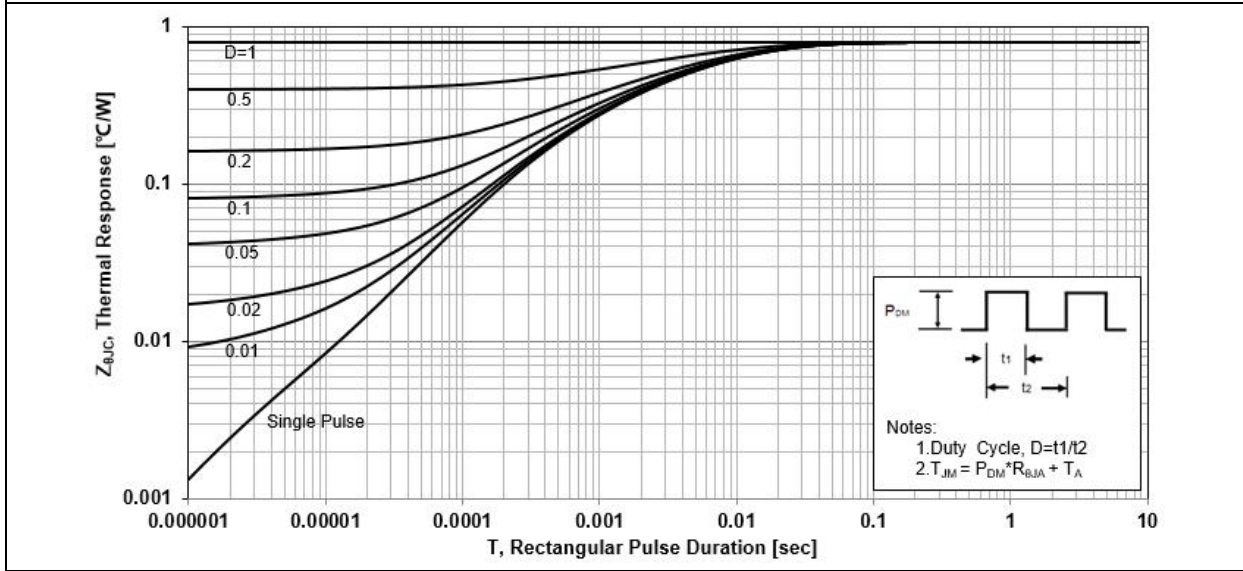


Figure 6. Typical Transfer Characteristics

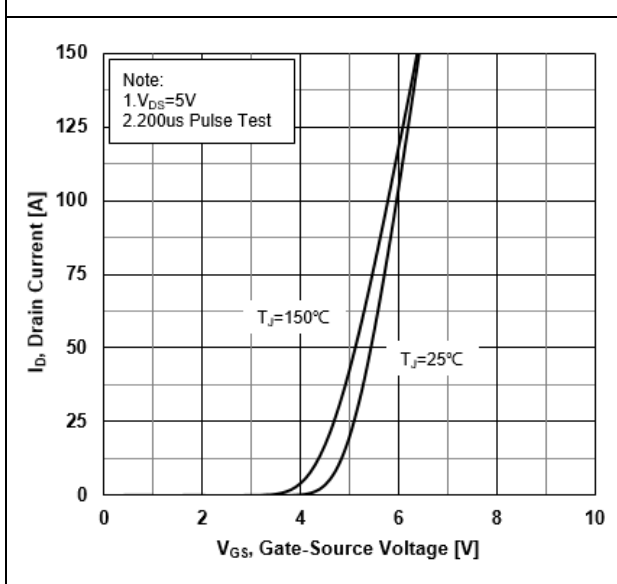


Figure 7. Source-Drain Diode Forward Characteristics

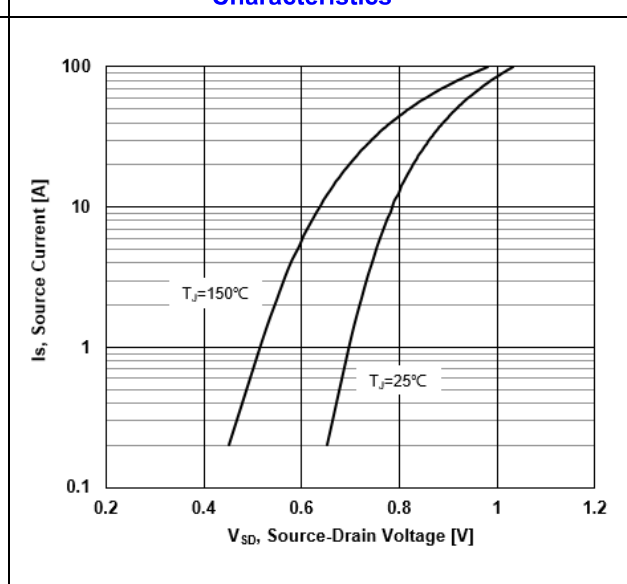


Figure 8. Drain-Source On-Resistance vs Drain Current

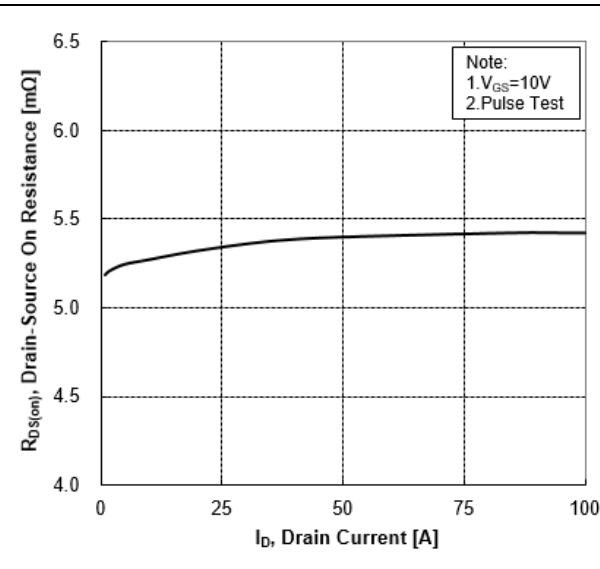


Figure 9. Normalized On-Resistance vs Junction Temperature

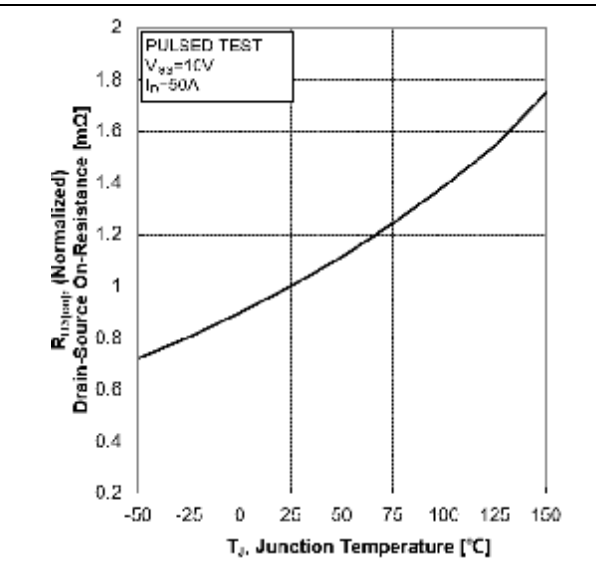


Figure 10. Normalized Threshold Voltage vs Junction Temperature

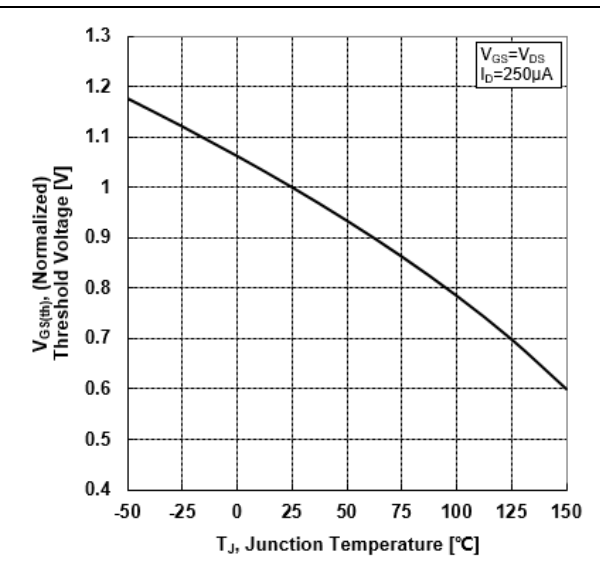


Figure 11. Normalized Breakdown Voltage vs Junction Temperature

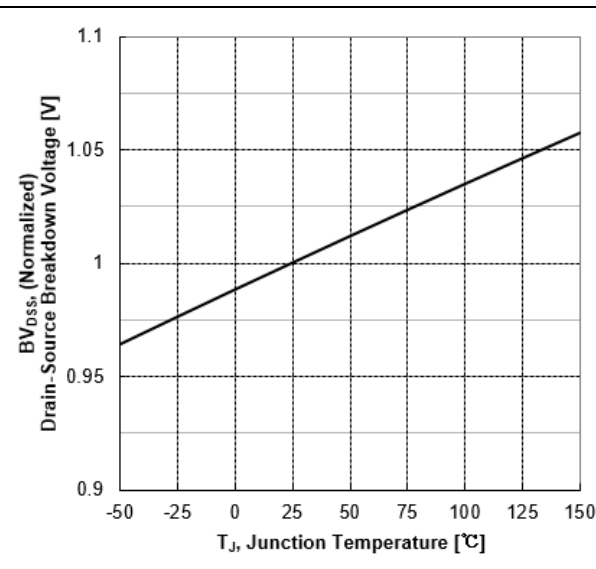


Figure 12. Capacitance Characteristics

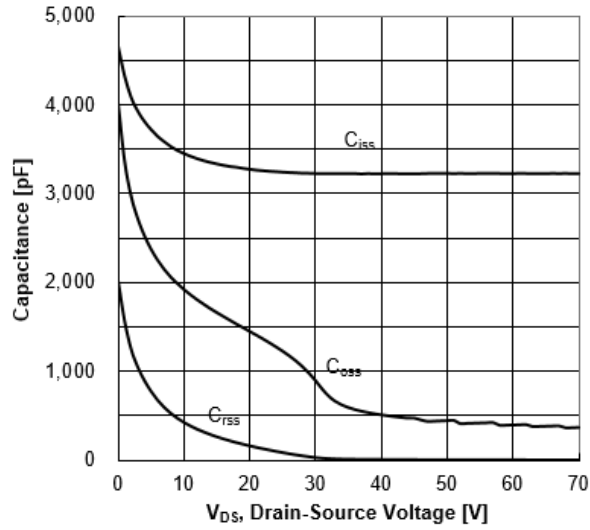
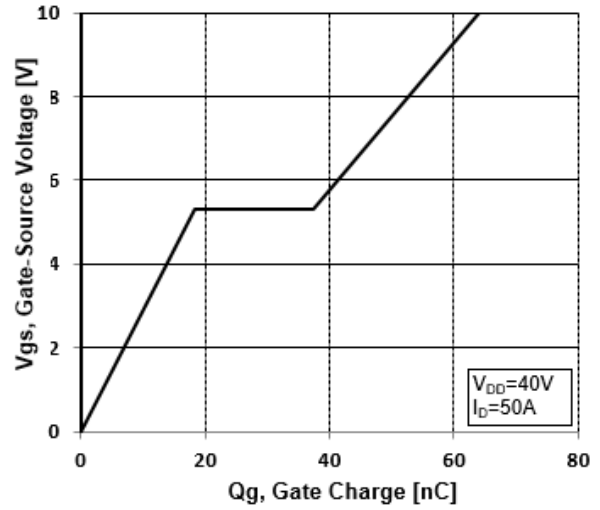


Figure 13. Typical Gate Charge vs Gate-Source Voltage



6. Test Circuit and Waveform

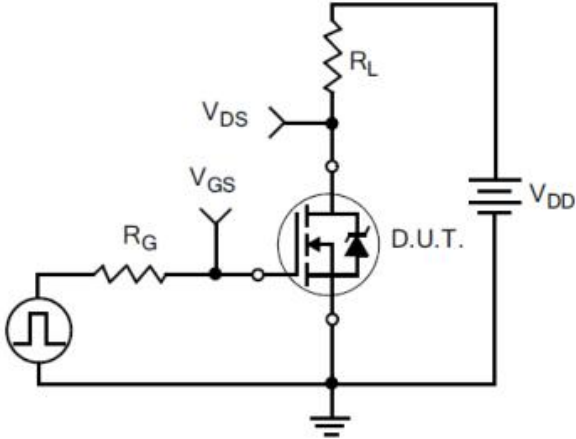
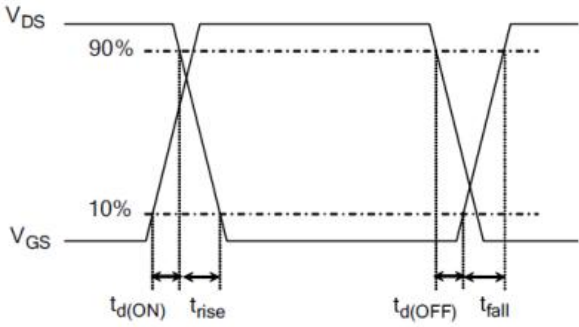
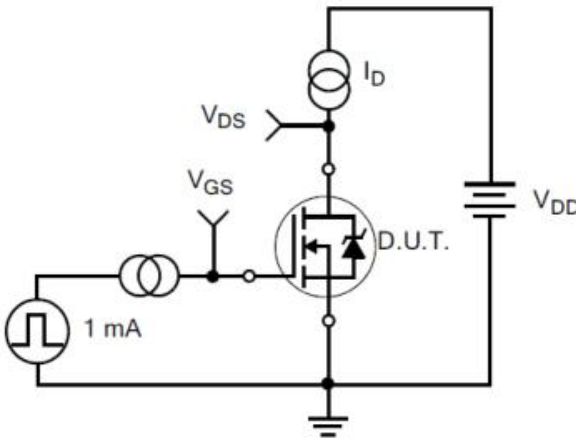
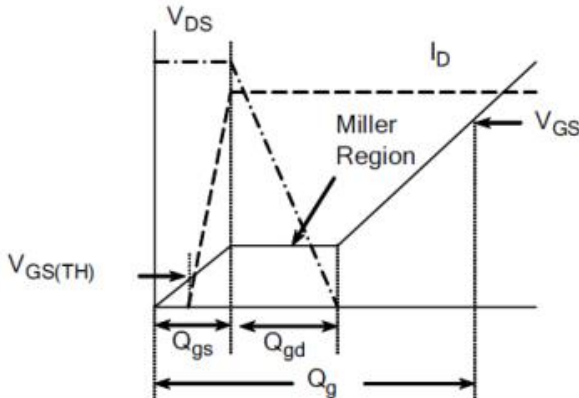
Figure 14. Resistive Switching Test Circuit	Figure 15. Resistive Switching Waveforms
 <p>The diagram shows a MOSFET (D.U.T.) in a common-source configuration. The gate is driven by a square wave pulse through a gate resistor R_G. The drain is connected to a load resistor R_L and a supply voltage V_{DD}. The drain voltage is labeled V_{DS} and the gate voltage is labeled V_{GS}.</p>	 <p>The diagram shows the waveforms for V_{DS} and V_{GS}. V_{GS} is a square wave pulse. V_{DS} shows a trapezoidal waveform during the pulse. Key parameters are marked: $t_{d(ON)}$ (delay time to turn on), t_{rise} (rise time), $t_{d(OFF)}$ (delay time to turn off), and t_{fall} (fall time). The 90% and 10% levels of the V_{DS} waveform are indicated with dashed lines.</p>
Figure 16. Gate Charge Test Circuit	Figure 17. Gate Charge Waveforms
 <p>The diagram shows a MOSFET (D.U.T.) in a common-source configuration. The gate is driven by a square wave pulse through a gate resistor R_G. The drain is connected to a load resistor R_L and a supply voltage V_{DD}. The drain current is labeled I_D and the gate voltage is labeled V_{GS}. A 1 mA current source is connected to the gate.</p>	 <p>The diagram shows the waveforms for V_{DS} and I_D during a gate charge test. V_{GS} is a square wave pulse. V_{DS} shows a trapezoidal waveform during the pulse. Key parameters are marked: $V_{GS(TH)}$ (threshold voltage), Q_{gs} (gate-source charge), Q_{gd} (gate-drain charge), and Q_g (total gate charge). The Miller Region is indicated by a dashed line.</p>

Figure 18. Diode Reverse Recovery Test Circuit

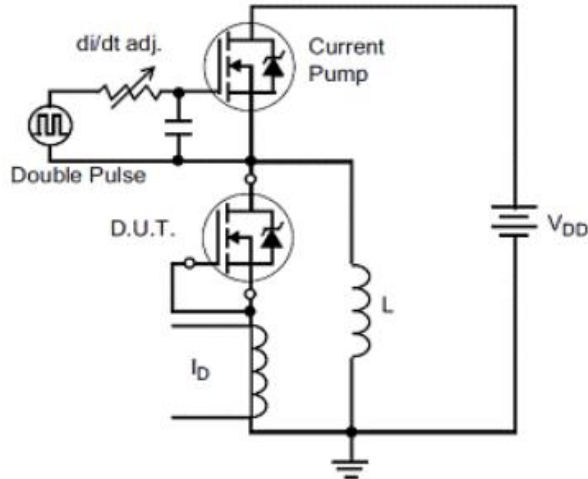


Figure 19. Diode Reverse Recovery Waveform

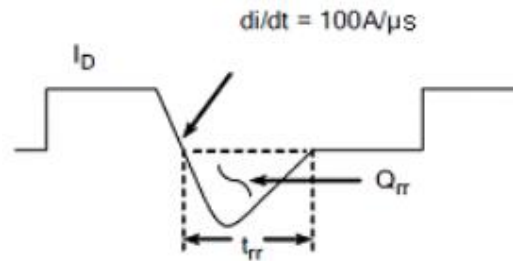


Figure 20. Unclamped Inductive Switching Test Circuit

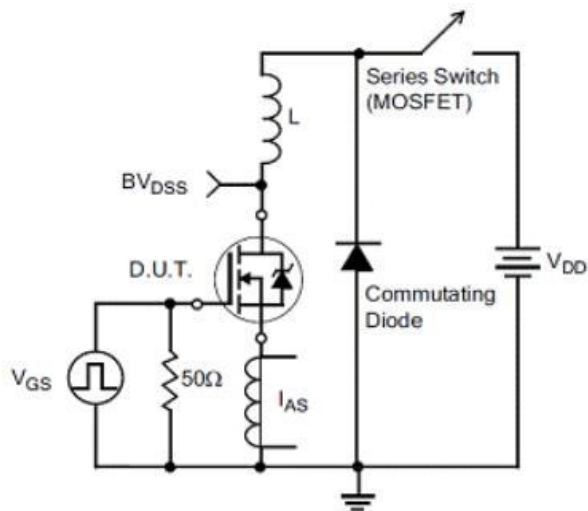
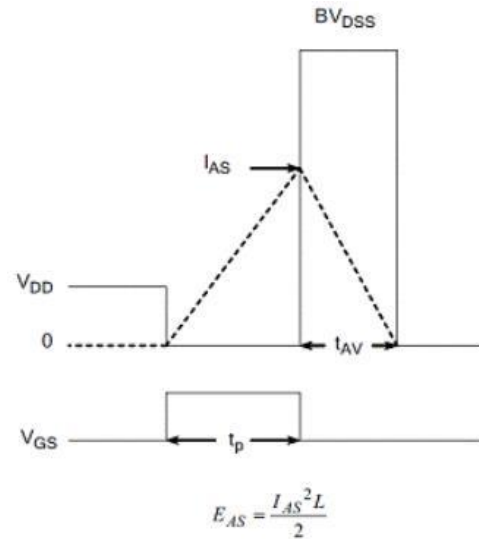
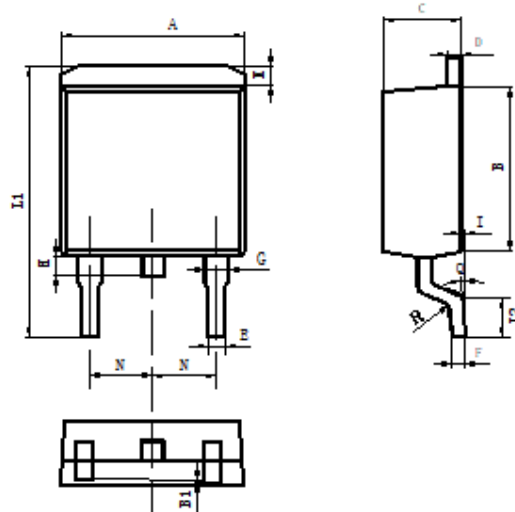


Figure 21. Unclamped Inductive Switching Waveform

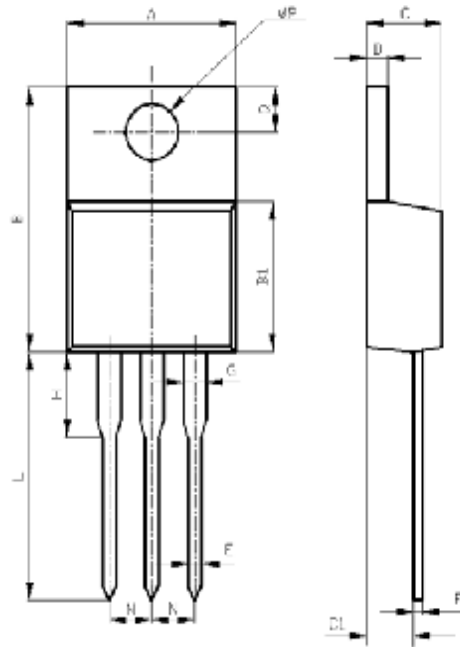


7. Package Description



Items	Values(mm)	
	MIN	MAX
A	9.80	10.40
B	8.90	9.50
B1	0	0.10
C	4.40	4.80
D	1.16	1.37
E	0.70	0.95
F	0.30	0.60
G	1.07	1.47
H	1.30	1.80
K	0.95	1.37
L1	14.50	16.50
L2	1.60	2.30
I	0	0.2
Q	0°	8°
R	0.4	0.4
N	2.39	2.69

TO-263 Package



Items	Values(mm)	
	MIN	MAX
A	9.60	10.6
B	15.0	16.0
B1	8.90	9.50
C	4.30	4.80
C1	2.30	3.10
D	1.20	1.40
E	0.70	0.90
F	0.30	0.60
G	1.17	1.37
H	2.70	3.80
L	12.6	14.8
N	2.34	2.74
Q	2.40	3.00
ΦP	3.50	3.90

TO-220 Package

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