Industrial eMMC 5.1 MLC Specification

Version 1.0

MK Founder Technology Co., Limited

MK may make changes to specifications and product description at any time without notice.

REVISION HISTORY

Revision	Date	History	Author
V1.0	2023/4	First release	Yukin Liu

PRODUCT OVERVIEW

- Packaged NAND flash memory with *eMMC* 5.1 interface
  - Compliant with *eMMC* Specification Ver. 4.3, 4.4, 4.41, 4.5, 4.51, 5.0, 5.1
  - Device can be converted to *eMMC* 4.3, 4.41 (Shows 4.4), 4.51 (Shows 4.5), 5.0 via initializing
- Package Form
  - 153 Ball FBGA(TFBGA) Package
- Bus mode
  - High-speed *eMMC* protocol
  - Clock frequency: 0-200MHz.
  - Ten-wire bus (clock, 1-bit command, 8-bit data bus) and a hardware reset.
- Supports three different data bus widths: 1 bit(default), 4 bits, 8 bits
  - Data transfer rate: up to 52Mbyte/s (using 8 parallel data lines at 52 MHz)
  - Single data rate: up to 200Mbyte/s @ 200MHz
  - Dual data rate: up to 400Mbyte/s @ 200MHz
- Operating voltage range
  - Core Voltage (V_{CC}): 2.7-3.6 V
  - I/O (V_{CCQ}) Voltage: 1.7-1.95V/2.7-3.6V
- Error free memory access
  - Internal error correction code (ECC) to protect data communication
  - Internal enhanced data management algorithm
  - Solid protection of sudden power failure safe-update operations for data content
- Security
  - Support secure erase/trim commands
  - Enhanced write Protection with permanent and partial protection options
- Quality
  - RoHS compliant (for detailed RoHS declaration, please contact your MK representative.)

- Major Supported Features
  - HS400, Field Firmware Update(FFU), Power Off Notification, Pre EOL information, Enhanced Device Life time, Optimal Size
- Major Supported *eMMC* 5.1 Features:
  - Enhanced Strobe, Cache Flushing Report, BKOPS Control, Cache Barrier, RPMB Throughput Improve, Secure Write Protection.
- Ambient Operating Temperature Range
  - Industrial: -40℃ to 85℃

TABLE OF CONTENTS

REVISION HISTORY **3**

PRODUCT OVERVIEW **4**

TABLE OF CONTENTS **6**

LIST OF FIGURES **8**

LIST OF TABLES **9**

1. INTRODUCTION **10**

2. POWER CONSUMPTION **11**

2.1. Operating Voltage 11

2.2. Power Consumption 11

3. PERFORMANCE **13**

3.1. Typical Sequential Performance 13

3.2. Typical Random Performance 15

4. OPERATING CONDITIONS **17**

4.1. Operating and Storage Temperature 17

5. USER DENSITY **17**

5.1. Capacity According to Partition 17

5.2. User Density Size 17

6. EMMC DEVICE AND SYSTEM **18**

6.1. eMMC System Overview 18

6.2. Memory Addressing 18

6.3. eMMC Device Overview 19

6.3.1. Clock (CLK) *19*

6.3.2. Data Strobe(DS) *19*

6.3.3. Command (CMD) *19*

6.3.4. Input/Outputs (DAT0-DAT7) *19*

7. EMMC FUNCTIONAL DESCRIPTION **21**

7.1. Pseudo Technology (pSLC) 21

7.2. Field Firmware Update(FFU) 21

7.3. Power off Notification for Sleep 22
7.4. Enhanced User Data Area 23
7.5. Write Cache 24
7.6. Cache Enhancement Barrier 24
7.7. Cache Flushing Policy 26
7.8. Production State Awareness (PSA) 26
8. REGISTER SETTINGS 28
8.1. OCR Register 28
8.2. CID Register 28
8.3. CSD Register 29
8.4. Extended CSD Register 30
9. PACKAGE CONNECTIONS 36
10. SIGNAL ASSIGNMENT (153 BALL) 37
11. SIGNAL DESCRIPTION 38

LIST OF FIGURES

Figure 6-1 eMMC System Overview 18

Figure 9-1 Package Dimension..... 37

Figure 10-1 153 Ball Assignment 37

LIST OF TABLES

Table 1-1 Product Summary (Industrial: -40℃ to +85℃ Ambient) 10
Table 2-1 Operating Voltage 11
Table 2-2 Device Power Consumption RMS 11
Table 2-3 Device Power Consumption Standby 12
Table 3-1 Sequential Burst Performance (PSA Pseudo-SLC Burst Status) 13
Table 3-2 Sequential Sustained Performance (Normal Status) 14
Table 3-3 Random Burst Performance (PSA Pseudo-SLC Burst Status) 15
Table 3-4 Random Sustained Performance (Normal Status) 16
Table 4-1 Operating and Storage Temperatures: Industrial Grade 17
Table 5-1 Capacity According to Partition 17
Table 5-2 User Density Size 17
Table 6-1 Communication Interface 20
Table 8-1 OCR Register 28
Table 8-2 CID Register 28
Table 8-3 CSD Register 29
Table 8-4 Extended CSD Register 30
Table 11-1 Signal Description 38

1. INTRODUCTION

MK *eMMC* products follow the JEDEC *eMMC* 5.1 standard. It is an ideal universal storage solution for many electronic devices, including smartphones, tablets, PDAs, eBook readers, digital cameras, recorders, MP3, MP4 players, electronic learning products, digital TVs and set-top boxes. *eMMC* encloses the 2D-MLC NAND and *eMMC* controller inside as one JEDEC standard 153 ball FBGA(TFBGA) package, providing a standard interface to the host. The *eMMC* controller directly manages NAND flash, including ECC, wear-leveling, IOPS optimization and read sensing.

Table 1-1 Product Summary (Industrial: -40℃ to +85℃ Ambient)

Capacity	Part Number	No. of Dies	NAND Flash Type	P/E	Package Size (mm)	Weight (g)
8GB	MKEMF008GT1E-I	1	2D-MLC	5,000	11.5 x 13 x 1.0	0.18
16GB	MKEMF016GT2E-I	2	2D-MLC	5,000	11.5 x 13 x 1.0	0.18

2. POWER CONSUMPTION

2.1. Operating Voltage

Table 2-1 Operating Voltage

Symbol	Min	Max	Unit
V_{CCQ}	1.7/2.7	1.95/3.6	V
V_{CC}	2.7	3.6	V

2.2. Power Consumption

Table 2-2 Device Power Consumption RMS

Speed Mode & Operation			Industrial		
			8GB	16GB	
HS400	Read	I_{CC}	45	45	mA
		I_{CCQ}	175	175	mA
	Write	I_{CC}	40	75	mA
		I_{CCQ}	80	85	mA
HS200	Read	I_{CC}	40	40	mA
		I_{CCQ}	140	145	mA
	Write	I_{CC}	40	75	mA
		I_{CCQ}	80	85	mA
DDR52	Read	I_{CC}	25	25	mA
		I_{CCQ}	130	130	mA
	Write	I_{CC}	40	65	mA
		I_{CCQ}	70	75	mA
SDR52	Read	I_{CC}	20	20	mA
		I_{CCQ}	100	100	mA
	Write	I_{CC}	40	60	mA
		I_{CCQ}	70	75	mA

NOTES:

1. The measurement for max RMS current is done as average RMS current consumption over a period of 100ms.
2. The RMS current is measured at T_A=25℃, VCC=3.3V, VCCQ=1.8V in HS400 & HS200 mode and at VCC=3.3V, VCCQ=3.3V in DDR52MHz & SDR52MHz mode, 8-bit bus width without clock frequency.
3. Current numbers might be subject to changes without notice.

4.

Table 2-3 Device Power Consumption Standby

Speed Mode & Operation		Industrial		Unit
		8GB	16GB	
HS400	Sleep	85	90	uA
	Standby I_{CCQ}	130	140	uA
	Standby I_{CC}	40	50	uA
HS200	Sleep	85	90	uA
	Standby I_{CCQ}	130	140	uA
	Standby I_{CC}	40	50	uA
DDR52	Sleep	90	95	uA
	Standby I_{CCQ}	140	150	uA
	Standby I_{CC}	40	55	uA
SDR52	Sleep	90	95	uA
	Standby I_{CCQ}	140	150	uA
	Standby I_{CC}	40	55	uA

NOTES:

1. Standby current is measured at T_A=25℃, VCC=3.3V, VCCQ=1.8V in HS400 & HS200 mode and at VCC=3.3V, VCCQ=3.3V in DDR52MHz & SDR52MHz mode, 8-bit bus width without clock frequency.
2. Current numbers might be subject to changes without notice.

3. PERFORMANCE

3.1. Typical Sequential Performance

Table 3-1 Sequential Burst Performance (PSA Pseudo-SLC Burst Status)

Speed Mode & Operation			Industrial		Unit
			8GB	16GB	
HS400	Write Cache on	Read	225	225	MB/s
		Write	105	140	MB/s
	Write Cache off	Read	225	225	MB/s
		Write	100	125	MB/s
HS200	Write Cache on	Read	160	160	MB/s
		Write	105	125	MB/s
	Write Cache off	Read	160	160	MB/s
		Write	95	115	MB/s
DDR52	Write Cache on	Read	80	80	MB/s
		Write	65	70	MB/s
	Write Cache off	Read	80	80	MB/s
		Write	65	65	MB/s
SDR52	Write Cache on	Read	45	45	MB/s
		Write	40	40	MB/s
	Write Cache off	Read	45	45	MB/s
		Write	35	40	MB/s

NOTES:

1. Values given for an 8-bit bus width, running from MK proprietary tool.
2. Performance is measured at V_{CC}=3.3V, V_{CCQ}=1.8V in HS400 & HS200 mode and at V_{CC}=3.3V, V_{CCQ}=3.3V in DDR52MHz & SDR52MHz mode.
3. Performance numbers might be subject to changes without notice.
4. The write cache size is 128KB.

Table 3-2 Sequential Sustained Performance (Normal Status)

Speed Mode & Operation			Industrial		Unit
			4GB	8GB	
HS400	Write Cache on	Read	225	225	MB/s
		Write	105	140	MB/s
	Write Cache off	Read	225	225	MB/s
		Write	100	125	MB/s
HS200	Write Cache on	Read	160	160	MB/s
		Write	105	125	MB/s
	Write Cache off	Read	160	160	MB/s
		Write	95	115	MB/s
DDR52	Write Cache on	Read	80	80	MB/s
		Write	65	70	MB/s
	Write Cache off	Read	80	80	MB/s
		Write	65	65	MB/s
SDR52	Write Cache on	Read	45	45	MB/s
		Write	40	40	MB/s
	Write Cache off	Read	45	45	MB/s
		Write	35	40	MB/s

NOTES:

1. Values given for an 8-bit bus width, running from MK proprietary tool.
2. Performance is measured at V_{CC}=3.3V, V_{CCQ}=1.8V in HS400 & HS200 mode and at V_{CC}=3.3V, V_{CCQ}=3.3V in DDR52MHz & SDR52MHz mode.
3. Performance numbers might be subject to changes without notice.
4. The write cache size is 128KB.

3.2. Typical Random Performance

Table 3-3 Random Burst Performance (PSA Pseudo-SLC Burst Status)

Speed Mode & Operation			Industrial		Unit
			4GB	8GB	
HS400	Write Cache on	Read	5200	5300	IOPS
		Write	9800	10200	IOPS
	Write Cache off	Read	2200	2200	IOPS
		Write	1300	1400	IOPS
HS200	Write Cache on	Read	5300	5300	IOPS
		Write	9700	10100	IOPS
	Write Cache off	Read	5300	5300	IOPS
		Write	2200	2200	IOPS
DDR52	Write Cache on	Read	4900	4800	IOPS
		Write	7100	7900	IOPS
	Write Cache off	Read	4900	4900	IOPS
		Write	2200	2100	IOPS
SDR52	Write Cache on	Read	4100	4000	IOPS
		Write	6100	6200	IOPS
	Write Cache off	Read	4100	4100	IOPS
		Write	2000	2000	IOPS

NOTES:

1. Values given for an 8-bit bus width, running from MK proprietary tool.
2. Performance is measured at V_{CC}=3.3V, V_{CCQ}=1.8V in HS400 & HS200 mode and at V_{CC}=3.3V, V_{CCQ}=3.3V in DDR52MHz & SDR52MHz mode.
3. Performance numbers might be subject to changes without notice.
4. The write cache size is 128KB.

Table 3-4 Random Sustained Performance (Normal Status)

Speed Mode & Operation			Industrial		Unit
			8GB	16GB	
HS400	Write Cache on	Read	4900	4900	IOPS
		Write	6400	6400	IOPS
	Write Cache off	Read	4900	4900	IOPS
		Write	1500	1400	IOPS
HS200	Write Cache on	Read	4900	5000	IOPS
		Write	6200	6300	IOPS
	Write Cache off	Read	4900	5000	IOPS
		Write	1400	1400	IOPS
DDR52	Write Cache on	Read	4500	4600	IOPS
		Write	5800	5900	IOPS
	Write Cache off	Read	4500	4600	IOPS
		Write	1400	1400	IOPS
SDR52	Write Cache on	Read	3900	3900	IOPS
		Write	5200	5400	IOPS
	Write Cache off	Read	3800	3900	IOPS
		Write	1300	1300	IOPS

NOTES:

1. Values given for an 8-bit bus width, running from MK proprietary tool.
2. Performance is measured at V_{CC}=3.3V, V_{CCQ}=1.8V in HS400 & HS200 mode and at V_{CC}=3.3V, V_{CCQ}=3.3V in DDR52MHz & SDR52MHz mode.
3. Performance numbers might be subject to changes without notice.
4. The write cache size is 128KB.

5.

4. OPERATING CONDITIONS

4.1. Operating and Storage Temperature

Table 4-1 Operating and Storage Temperatures: Industrial Grade

Condition	Temperature
Minimum and Maximum Ambient[1] Temperature	-40℃ to 85℃
Maximum Case Operating Temperature	95℃
Minimum and Maximum Non-operating Temperature[2]	-40℃ to 85℃

NOTES:

1. To achieve optimized power and performance, case temperature should not exceed maximum ambient operating temperature.
2. After being soldered onto PCBA.

5. USER DENSITY

5.1. Capacity According to Partition

Table 5-1 Capacity According to Partition

Device	Boot Partition 1	Boot Partition 2	RPMB
8GB	4096 KB	4096 KB	4096 KB
16GB	4096 KB	4096 KB	4096 KB

5.2. User Density Size

Total user density depends on device type.

Table 5-2 User Density Size

Grade	Flash Mode	Device	User Density Size
Industrial	MLC	8GB	7,837,581,312 Bytes
	MLC	16GB	15,675,162,624 Bytes

6. eMMC DEVICE AND SYSTEM

6.1. eMMC System Overview

The *eMMC* specification covers the behavior of the interface and the device controller. As part of this specification the existence of a host controller and a memory storage array are implied but the operation of these pieces is not fully specified.

MK NAND Device consists of a single chip MMC controller and NAND flash memory module. The micro-controller interfaces with a host system allowing data to be written to and read from the NAND flash memory module. The controller allows the host to be independent from details of erasing and programming the flash memory.

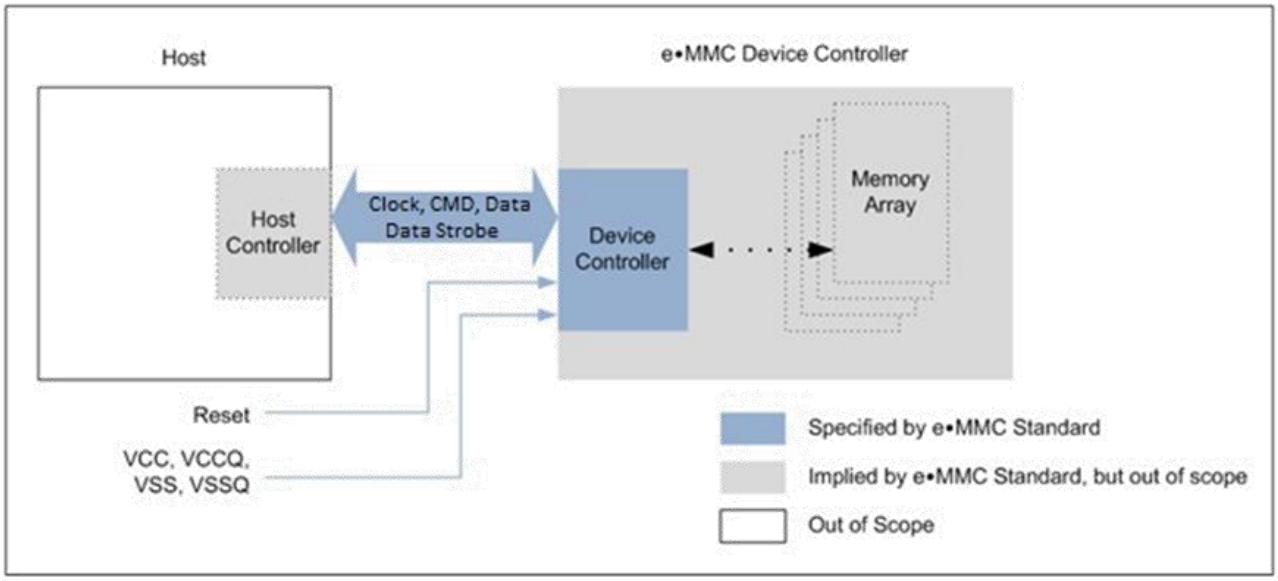


Figure 6-1 eMMC System Overview

6.2. Memory Addressing

Previous implementations of the eMMC specification are following byte addressing with 32-bit field. This addressing mechanism permitted for eMMC densities up to and including 2 GB.

To support larger density, the addressing mechanism was update to support sector addresses (512 B sectors). The sector addresses shall be used for all devices with capacity larger than 2 GB.

To determine the addressing mode, use the host should read bit [30:29] in the OCR register.

6.3. eMMC Device Overview

The eMMC device transfers data via a configurable number of data bus signals. The communication signals are:

6.3.1. Clock (CLK)

Each cycle of this signal directs a one-bit transfer on the command and either a one bit (1x) or a two bits transfer (2x) on all the data lines. The frequency may vary between zero and the maximum clock frequency.

6.3.2. Data Strobe(DS)

This signal is generated by the device and used for output in HS400 mode. The frequency of this signal follows the frequency of CLK. For data output each cycle of this signal directs two bits transfer(2x) on the data - one bit for positive edge and the other bit for negative edge. For CRC status response output and CMD response output (enabled only HS400 enhanced strobe mode), the CRC status is latched on the positive edge only, and don't care on the negative edge.

6.3.3. Command (CMD)

This signal is a bidirectional command channel used for Device initialization and transfer of commands. The CMD signal has two operation modes: open-drain for initialization mode, and push-pull for fast command transfer. Commands are sent from the eMMC host controller to the eMMC Device and responses are sent from the Device to the host.

6.3.4. Input/Outputs (DAT0-DAT7)

These are bidirectional data channels. The DAT signals operate in push-pull mode. Only the Device or the host is driving these signals at a time. By default, after power up or reset, only DAT0 is used for data transfer. A wider data bus can be configured for data transfer, using either DAT0-DAT3 or DAT0-DAT7, by the eMMC host controller. The eMMC Device includes internal pull-ups for data lines DAT1-DAT7. Immediately after entering the 4-bit mode, the Device disconnects the internal pull ups of lines DAT1, DAT2, and DAT3. Correspondingly, immediately after entering to the 8-bit mode the Device disconnects the internal pull-ups of lines DAT1–DAT7.

Table 6-1 Communication Interface

Name	Type[1]	Description
CLK	I	Clock
DAT0	I/O/PP	Data
DAT1	I/O/PP	Data
DAT2	I/O/PP	Data
DAT3	I/O/PP	Data
DAT4	I/O/PP	Data
DAT5	I/O/PP	Data
DAT6	I/O/PP	Data
DAT7	I/O/PP	Data
CMD	I/O/PP/OD	Command/Response
RST_n	I	Hardware reset
VCC	S	Supply voltage for Core
VCCQ	S	Supply voltage for I/O
VSS	S	Supply voltage ground for Core
VSSQ	S	Supply voltage ground for I/O
DS	O/PP	Data strobe
VDDi		Connect capacitor from VDDi to GND for stabilize internal power.

NOTES:

1. I: input; O: output; PP: push-pull; OD: open-drain; NC: Not connected (or logical high); S: power supply.

7. eMMC FUNCTIONAL DESCRIPTION

7.1. Pseudo Technology (pSLC)

Each cell in an TLC NAND can be programmed to store 3 bits of data with 8 total voltage states. In Pseudo-SLC (pSLC) mode, the memory cell is used in 2-bit or 1-bit mode, thus resulting in higher endurance, lower error rates and extended temperature range. MK firmware optimizes the *eMMC* device with Pseudo technology to achieve industrial and automotive level reliability. For MK *eMMC* device, Pseudo SLC (pSLC) mode provides one quarter capacity of TLC mode.

7.2. Field Firmware Update(FFU)

Field Firmware Updates (FFU) enables features enhancement in the field. Using this mechanism, the host downloads a new version of the firmware to the *eMMC* device and, following a successful download, instructs the *eMMC* device to install the new downloaded firmware into the device.

In order to start the FFU process the host first checks if the *eMMC* device supports FFU capabilities by reading SUPPPORTED_MODES and FW_CONFIG fields in the EXT_CSD. If the *eMMC* device supports the FFU feature the host may start the FFU process. The FFU process starts by switching to FFU Mode in MODE_CONFIG field in the EXT_CSD. In FFU Mode host should use closed-ended or open ended commands for downloading the new firmware and reading vendor proprietary data. In this mode, the host should set the argument of these commands to be as defined in FFU_ARG field. In case these commands have a different argument the device behavior is not defined and the FFU process may fail. The host should set Block Length to be DATA_SECTOR_SIZE. Downloaded firmware bundle must be DATA_SECTOR_SIZE size aligned (internal padding of the bundle might be required). Once in FFU Mode the host may send the new firmware bundle to the device using one or more write commands.

The host could regain regular functionality of write and read commands by setting MODE_CONFIG field in the EXT_CSD back to Normal state. Switching out of FFU Mode may abort the firmware download operation. When host switched back to FFU Mode, the host should check the FFU Status to get indication about the number of sectors which were downloaded successfully by reading the NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED in the extended CSD. In case the number of sectors which were downloaded successfully is zero the host should re-start downloading the new firmware

bundle from its first sector. In case the number of sectors which were downloaded successfully is positive the host should continue the download from the next sector, which would resume the firmware download operation.

In case MODE_OPERATION_CODES field is not supported by the device the host sets to NORMAL state and initiates a CMD0/HW_Reset/Power cycle to install the new firmware. In such case the device doesn't need to use NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED.

In both cases occurrence of a CMD0/HW_Reset/Power occurred before the host successfully downloaded the new firmware bundle to the device may cause the firmware download process to be aborted.

7.3. Power off Notification for Sleep

The host should notify the device before it powers the device off. This allows the device to better prepare itself for being powered off. Power the device off means to turn off all its power supplies. In particular, the host should issue a power off notification (POWER_OFF_LONG, POWER_OFF_SHORT) if it intends to turn off both VCC and VCCQ power I or it may use to a power off notification (SLEEP_NOTIFICATION) if it intends to turn-off VCC after moving the device to Sleep state.

To indicate to the device that power off notification is supported by the host, a supporting host shall first set the POWER_OFF_NOTIFICATION byte in EXT_CSD [34] to POWERED_ON (0x01). To execute a power off, before powering the device down the host will changes the value to either POWER_OFF_SHORT (0x02) or POWER_OFF_LONG (0x03). Host should wait for the busy line to be de-asserted. Once the setting has changed to either 0x02 or 0x03, host may safely power off the device.

The host may issue SLEEP_AWAKE (CMD5) to enter or to exit from Sleep state if POWER_OFF_NOTIFICATION byte is set to POWERED_ON. Before moving to Standby state and then to Sleep state, the host sets POWER_OFF_NOTIFICATION to SLEEP_NOTIFICATION and waits for the DAT0 line de-assertion. While in Sleep (slp) state VCC (Memory supply) may be turned off as defined in 4.1.6. Removing power supplies other than VCC while the device is in the Sleep (slp) state may result in undefined device behavior. Before removing all power supplies, the host should transition the device out of Sleep (slp) state back to Transfer state using CMD5 and CMD7 and then execute a power off notification setting POWER_OFF_NOTIFICATION byte to either POWER_OFF_SHORT or POWER_OFF_LONG.

If host continues to send commands to the device after switching to the power off setting (POWER_OFF_LONG, POWER_OFF_SHORT or SLEEP_NOTIFICATION) or performs HPI during its busy condition, the device shall restore the POWER_OFF_NOTIFICATION byte to POWERED_ON.

If host tries to change POWER_OFF_NOTIFICATION to 0x00 after writing another value there, a SWITCH_ERROR is generated.

The difference between the two power-off modes is how urgent the host wants to turn power off. The device should respond to POWER_OFF_SHORT quickly under the generic CMD6 timeout. If more time is acceptable, POWER_OFF_LONG may be used and the device shall respond to it within the POWER_OFF_LONG_TIME timeout.

While POWER_OFF_NOTIFICATION is set to POWERED_ON, the device expects the host to host shall:

- Keep the device power supplies alive (both VCC and VCCQ) and in their active mode
- Not power off the device intentionally before changing POWER_OFF_NOTIFICATION to either POWER_OFF_LONG or POWER_OFF_SHORT
- Not power off VCC intentionally before changing POWER_OFF_NOTIFICATION to SLEEP_NOTIFICATION and before moving the device to Sleep state

Before moving to Sleep state hosts may set the POWER_OFF_NOTIFICATION byte to SLEEP_NOTIFICATION (0x04) if aware that the device is capable of autonomously initiating background operations for possible performance improvements. Host should wait for the busy line to be de-asserted. Busy line may be asserted up the period defined in SLEEP_NOTIFICATION_TIME byte in EXT_CSD [216]. Once the setting has changed to 0x04 host may set the device into Sleep mode (CMD7+CMD5). After getting out from Sleep the POWER_OFF_NOTIFICATION byte will restore its value to POWERED_ON. HPI may interrupt the SLEEP_NOTIFICATION operation. In that case POWER_OFF_NOTIFICATION byte will restore to POWERED_ON.

7.4. Enhanced User Data Area

MK *eMMC* supports Enhanced User Data Area feature which allows the User Data Area of *eMMC* to be

configured as SLC Mode. Therefore, when host set the Enhanced User Data Area, the area will occupy more size of original set up size. The Max Enhanced User Data Area size is defined as - (MAX_ENH_SIZE_MULT x HC_WP_GRP_SIZE x HC_ERASE_GRP_SIZE x 512 KBytes). The Enhanced use data area size is defined as - (ENH_SIZE_MULT x HC_WP_GRP_SIZE x HC_ERASE_GRP_SIZE x 512 KBytes). The host shall follow the flow chart of JEDEC spec for configuring the parameters of General Purpose Area Partitions and Enhanced User Data Area.

7.5. Write Cache

Cache is a temporary storage space in an *eMMC* device. The cache should in typical case reduce the access time and increase the speed (compared to an access to the main nonvolatile storage). The cache is not directly accessible by the host. This temporary storage space may be utilized also for some implementation specific operations like as an execution memory for the memory controller and/or as storage for an address mapping table etc. However, there is data inconsistence risk when using nonvolatile cache. It's recommend only turning on the cache for the application which requires not too high reliability.

The cache shall be OFF by default after power up, RST_n assertion or CMD0. All accesses shall be directed to the nonvolatile storage like defined elsewhere in this specification. The cache function can be turned ON and OFF by writing to the CACHE_CTRL byte (EXT_CSD byte [33]). Turning the cache ON shall enable behavior model defined in this section. Turning the cache OFF shall trigger flushing of the data to the nonvolatile storage.

7.6. Cache Enhancement Barrier

Barrier function provides a way to perform a delayed in-order flushing of a cached data. The main motivation for using barrier commands is to avoid the long delay that is introduced by flush commands. There are cases where the host is not interested in flushing the data right away, however it would like to keep an order between different cached data batches. The barrier command enables the host achieving the in-order goal but without paying the flush delay, since the real flushing can be delayed by the device to some later idle time. The formal definition of the barrier rule is as follows:

Denote a sequence of requests Ri, i=0,..,N. Assuming a barrier is set between requests Rx and Rx+1 (0<x<N) then all the requests R0..Rx must be flushed to the non-volatile memory before any of the requests

Rx+1..RN.

Between two barriers the device is free to write data into the non-volatile memory in any order. If the host wants to preserve a certain order it shall flush the cache or set another barrier at a point where order is important.

The barrier is set by writing to the BARRIER bit of the FLUSH_CACHE byte (EXT_CSD byte [32]). Any error resulted can be read from the status register by CMD13 after the completion of the programming as defined for a normal write request. The error could affect any data written to the cache since the previous flush operation.

The device shall support any number of barrier commands between two flush commands. In case of multiple barrier commands between two flush commands a subset of the cached data may be committed to the non-volatile memory according to the barrier rule. Internally, a device may have an upper limit on the barrier amount it can absorb without flushing the cache. That is, if the host exceeds this barrier amount, the device may issue, internally, a normal flush.

The device shall expose its barrier support capability via the BARRIER_SUPPORT byte (EXT_CSD byte [486]). If a device does not support barrier function this register shall be zero. If a device supports barrier function this register shall be one.

Assuming the device supports barrier function, if the BARRIER bit of the FLUSH_CACHE byte is set, a barrier operation shall be executed.

If the cache gets totally full and/or the cache is not able to receive the data of the next access (per block count indicated in CMD23 or per initiated single / open ended multiple block write in general) then it shall still be the responsibility of the *eMMC* device to store the data of the next access within the timeouts that are specified elsewhere in this specification. The actual algorithm to handle the new data and possible flush of some older cached data is left for the implementation.

Note: When issuing a force-programming write request (CMD23 with bit 24 on) or a reliable write request (CMD23 with bit 31 on), the host should be aware that the data will be written to the non-volatile memory,

potentially, before any cached data, even if a barrier command was issued. Therefore, if the writing order to the non-volatile memory is important, it is the responsibility of the host to issue a flush command before the force-programming or the reliable-write request.

In order to use the barrier function, the host shall set bit 0 of BARRIER_EN (EXT_CSD byte [31]). The barrier feature is optional for an *eMMC* device.

7.7. Cache Flushing Policy

The host may require the device to flush data from the cache in an in-order manner. From time to time, to guarantee in-order flushing, the host may command the device to flush the device cache or may use a barrier command.

However, if the *eMMC* device flushing policy is to flush data from the cache in an in-order manner, cache barrier commands or flush commands operations (In case goal is to guarantee the flushing order) are redundant and impose a needless overhead to the device and host.

FIFO bit in CACHE_FLUSH_POLICY field (EXT_CSD byte [240]) is used by the device to indicate to the host that the device cache flushing policy is First-In-First-Out; this means that the device guarantees that the order of the flushing of data would be the in same order which data was written to the cache. When the FIFO bit is set it is recommended for the host not to send cache barrier commands or flush operations which goal is to guarantee the flushing order as they are redundant and impose a burden to the system.

However, if the FIFO bit is set to 1b and the device supports the cache barrier mechanism, the host may still send barrier commands without getting an error. Sending these commands will not change the device behavior as device flushes cache in-order anyway.

The CACHE_FLUSH_POLICY field is read-only field and never change its value either by the host or device.

7.8. Production State Awareness (PSA)

eMMC device could utilize the information of whether it is in production environment and operate differently than it operates in the field.

For example, content that was loaded into the storage device prior to soldering might get corrupted, at higher probability, during device soldering. The *eMMC* device could use “special” internal operations for loading content prior to device soldering that would reduce production failures and use “regular” operations post-soldering.

PRODUCTION_STATE_AWARENESS [133] field in extended CSD is used as a mechanism through which the host should report to the device whether it is pre or post soldering state.

This standard defines two methods, Manual Mode and Auto Mode, to manage the device production state.

The trigger for starting or re-starting the process is setting correctly PRE_LOADING_DATA_SIZE field. Before setting this field the host is expected to make sure that the device is clean and any data that was written before to the device is expected to be erased using CMD35, CMD36 and CMD38.

In case the host erased data, overrode existing data or performed re-partition during production state awareness it should restart the production state awareness process by re-setting PRE_LOADING_DATA_SIZE. MK defines Pseudo SLC mode as special internal operation of PSA to have better reliability during the soldering process in production (reflow). MK has adopted mechanisms to recover the TLC behavior after the end of production. Once the host used over the threshold, the PSA feature is disabled and the firmware will start to merge pSLC blocks to TLC block to make drive returns to original situation. Threshold values of PSA are different according to NAND mode:

- TLC – 33% of user capacity

8. REGISTER SETTINGS

Within the Device interface six registers are defined: OCR, CID, CSD, EXT_CSD, RCA and DSR. These can be accessed only by corresponding commands (see Section 6.10 of JESD84-B51).

8.1. OCR Register

The 32-bit operation conditions register (OCR) stores the VDD voltage profile of the Device and the access mode indication. In addition, this register includes a status information bit. This status bit is set if the Device power up procedure has been finished. The OCR register shall be implemented by all Devices.

Table 8-1 OCR Register

OCR bit	VDD voltage window	High Voltage Value	Dual Voltage Value
[6:0]	Reserved	00 00000b	00 00000b
[7]	1.70 - 1.95V	0b	1b
[14:8]	2.0-2.7V	000 0000b	000 0000b
[23:15]	2.7-3.6V	1 1111 1111b	1 1111 1111b
[28:24]	Reserved	0 0000b	0 0000b
[30:29]	Access Mode	00b (byte mode) 10b (sector mode)	00b (byte mode) 10b (sector mode)
[31]	Device power up status bit (busy)[1]		

NOTES:

1. This bit is set to LOW if the Device has not finished the power up routine.

8.2. CID Register

The Card Identification (CID) register is 128 bits wide. It contains the Device identification information used during the Device identification phase (eMMC protocol). For details, refer to JEDEC Standard Specification.

Table 8-2 CID Register

CID Fields Name	Field	Width	CID slice	Value
Manufacturer ID	MID	8	[127:120]	F2
Reserved	-	6	[119:114]	0h
Device/BGA	CBX	2	[113:112]	1h
OEM/Application ID	OID	8	[111:104]	1h
Product name	PNM	48	[103:56]	MK008I (8GB) / MK016I (16GB)
Product revision	PRV	8	[55:48]	50h*
Product serial number	PSN	32	[47:16]	Random by Production
Manufacturing date	MDT	8	[15:8]	Month, Year
CRC7 checksum	CRC	7	[7:1]	- (Note 1)
Reserved	-	1	[0:0]	1h

NOTE1: The descriptions are same as *e.MMC* ™ JEDEC standard.

8.3. CSD Register

The Card-Specific Data (CSD) register provides information on how to access the contents stored in eMMC. The CSD registers are used to define the error correction type, maximum data access time, data transfer speed, data format…etc. For details, refer to section 7.3 of the JEDEC Standard Specification No. JESD84-B51.

Table 8-3 CSD Register

Name	Field	Width	Cell Type	CSD-slice	Value
CSD structure	CSD_STRUCTURE	2	R	[127:126]	3h
System specification version	SPEC_VERS	4	R	[125:122]	4h
Reserved	-	2	R	[121:120]	-
Data read access-time 1	TAAC	8	R	[119:112]	4Fh
Data read access-time 2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	1h
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	32h
Device command classes	CCC	12	R	[95:84]	8F5h
Max. read data block length	READ_BL_LEN	4	R	[83:80]	9h
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0h
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0h
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0h
DSR implemented	DSR_IMP	1	R	[76:76]	0h
Reserved	-	2	R	[75:74]	0h
Device size	C_SIZE	12	R	[73:62]	FFFh
Max. read current @ VDD min	VDD_R_CURR_MIN	3	R	[61:59]	7h
Max. read current @ VDD max	VDD_R_CURR_MAX	3	R	[58:56]	7h
Max. write current @ VDD min	VDD_W_CURR_MIN	3	R	[55:53]	7h
Max. write current @ VDD max	VDD_W_CURR_MAX	3	R	[52:50]	7h
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	7h
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	8G-0Fh 16G-1Fh
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	1Fh
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	0Fh
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	1h
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	0h
Write speed factor	R2W_FACTOR	3	R	[28:26]	2h
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	9h
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0h
Reserved	-	4	R	[20:17]	0h
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0h
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0h
Copy flag (OTP)	COPY	1	R/W	[14:14]	0h
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0h
Temporary write protection	TMP_WRITE_PROTECT	1	R/W	[12:12]	0h
File format	FILE_FORMAT	2	R/W	[11:10]	0h

ECC code	ECC	2	R/W	[9:8]	0h
CRC	CRC	7	R/W	[7:1]	8G-64h 16G-2Eh
Reserved	-	1	-	[0:0]	1h

8.4. Extended CSD Register

The Extended CSD register defines the Device properties and selected modes. It is 512 bytes long. The most significant 320 bytes are the Properties segment, which defines the Device capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the Device is working in. These modes can be changed by the host by means of the SWITCH command.

Table 8-4 Extended CSD Register

Name	Field	Size (Bytes)	CSD-slice	Value
Reserved	–	6	[511:506]	0h
Extended Security Commands Error	EXT_SECURITY_ERR	1	[505]	0h
Supported Command Sets	S_CMD_SET	1	[504]	1h
HPI features	HPI_FEATURES	1	[503]	1h
Background operations support	BKOPS_SUPPORT	1	[502]	1h
Max packed read commands	MAX_PACKED_READS	1	[501]	3Ch
Max packed write commands	MAX_PACKED_WRITES	1	[500]	3Ch
Data Tag Support	DATA_TAG_SUPPORT	1	[499]	1h
Tag Unit Size	TAG_UNIT_SIZE	1	[498]	3h
Tag Resources Size	TAG_RES_SIZE	1	[497]	0h
Context management capabilities	CONTEXT_CAPABILITIES	1	[496]	5h
Large Unit size	LARGE_UNIT_SIZE_M1	1	[495]	17h
Extended partitions attribute support	EXT_SUPPORT	1	[494]	3h
Supported modes	SUPPORTED_MODES	1	[493]	1h
FFU features	FFU_FEATURES	1	[492]	0h
Operation codes timeout	OPERATION_CODE_TIME_OUT	1	[491]	0h
FFU Argument	FFU_ARG	4	[490:487]	65535h
Barrier support	BARRIER_SUPPORT	1	[486]	1h
Reserved	Reserved	177	[485:309]	–
CMDQ support	CMDQ_SUPPORT	1	[308]	0h
CMDQ depth	CMDQ_DEPTH	1	[307]	0h
Reserved	Reserved	1	[306]	0h
Number of FW sectors correctly programmed	NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	4	[305:302]	0h
Vendor proprietary health report	VENDOR_PROPRIETARY_HEALTH_REPORT	32	[301:270]	–

Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	1	[269]	1h
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	1	[268]	1h
Pre EOL information	PRE_EOL_INFO	1	[267]	1h
Optimal read size	OPTIMAL_READ_SIZE	1	[266]	1h
Optimal write size	OPTIMAL_WRITE_SIZE	1	[265]	8h
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	[264]	1h
Device version	DEVICE_VERSION	2	[263:262]	0
Firmware version	FIRMWARE_VERSION	8	[261:254]	2h*
Power class for 200MHz, DDR at VCC=3.6V	PWR_CL_DDR_200_360	1	[253]	0h
Cache size	CACHE_SIZE	4	[252:249]	512
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	[248]	32h
Power off notification(long) timeout	POWER_OFF_LONG_TIME	1	[247]	FFh
Background operations status	BKOPS_STATUS	1	[246]	0h
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	[245:242]	0h
1st initialization time after partitioning	INI_TIMEOUT_AP	1	[241]	64h
Cache Flushing Policy	CACHE_FLUSH_POLICY	1	[240]	1h
Power class for 52MHz, DDR at 3.6V	PWR_CL_DDR_52_360	1	[239]	0h
Power class for 52MHz, DDR at 1.95V	PWR_CL_DDR_52_195	1	[238]	0h
Power class for 200MHz at 3.6V	PWR_CL_200_195	1	[237]	0h
Power class for 200MHz, at 1.95V	PWR_CL_200_130	1	[236]	0h
Minimum Write Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	[235]	0h
Minimum Read Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	[234]	0h
Reserved	–	1	[233]	0h
TRIM Multiplier	TRIM_MULT	1	[232]	11h
Secure Feature support	SEC_FEATURE_SUPPORT	1	[231]	55h
Secure Erase Multiplier	SEC_ERASE_MULT	1	[230]	F7h
Secure TRIM Multiplier	SEC_TRIM_MULT	1	[229]	F7h
Boot information	BOOT_INFO	1	[228]	7h
Reserved	–	1	[227]	0h
Boot partition size	BOOT_SIZE_MULTI	1	[226]	20h
Access size	ACC_SIZE	1	[225]	7h-08GB 8h-16GB
High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	[224]	1h
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	[223]	11h

Reliable write sector count	REL_WR_SEC_C	1	[222]	1h
High-capacity write protect group size	HC_WP_GRP_SIZE	1	[221]	10h
Sleep current (VCC)	S_C_VCC	1	[220]	Ah
Sleep current (VCCQ)	S_C_VCCQ	1	[219]	Bh
Production state awareness Timeout	PRODUCTION_STATE_AWARENESS_TIMEOUT	1	[218]	14h
Sleep/awake timeout	S_A_TIMEOUT	1	[217]	15h
Sleep Notification timeout	SLEEP_NOTIFICATION_TIME	1	[216]	0h
Sector Count	SEC_COUNT	4	[215:212]	15307776-08GB* 30615552-16GB*
Security write protect information	SECURE_WP_INFO	1	[211]	1h
Minimum Write Performance for 8bit at 52MHz	MIN_PERF_W_8_52	1	[210]	8h
Minimum Read Performance for 8bit at 52MHz	MIN_PERF_R_8_52	1	[209]	8h
Minimum Write Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	1	[208]	8h
Minimum Read Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	1	[207]	8h
Minimum Write Performance for 4bit at 26MHz	MIN_PERF_W_4_26	1	[206]	8h
Minimum Read Performance for 4bit at 26MHz	MIN_PERF_R_4_26	1	[205]	8h
Reserved	–	1	[204]	0h
Power class for 26MHz at 3.6V 1 R	PWR_CL_26_360	1	[203]	0h
Power class for 52MHz at 3.6V 1 R	PWR_CL_52_360	1	[202]	0h
Power class for 26MHz at 1.95V 1 R	PWR_CL_26_195	1	[201]	0h
Power class for 52MHz at 1.95V 1 R	PWR_CL_52_195	1	[200]	0h
Partition switching timing	PARTITION_SWITCH_TIME	1	[199]	3h
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	[198]	FFh
I/O Driver Strength	DRIVER_STRENGTH	1	[197]	1Fh
Device type	DEVICE_TYPE	1	[196]	57h
Reserved	–	1	[195]	0h
CSD structure version	CSD_STRUCTURE	1	[194]	2h
Reserved	–	1	[193]	0h
Extended CSD revision	EXT_CSD_REV	1	[192]	8h
Command set	CMD_SET	1	[191]	0h
Reserved	–	1	[190]	0h
Command set revision	CMD_SET_REV	1	[189]	0h

Reserved	–	1	[188]	0h
Power class	POWER_CLASS	1	[187]	0h
Reserved	–	1	[186]	0h
High-speed interface timing	HS_TIMING	1	[185]	1h (note 3)
Strobe support	STROBE_SUPPORT	1	[184]	1h
Bus width mode	BUS_WIDTH	1	[183]	2h (note 4)
Reserved	–	1	[182]	0h
Erased memory content	ERASED_MEM_CONT	1	[181]	0h
Reserved	–	1	[180]	0h
Partition configuration	PARTITION_CONFIG	1	[179]	0h
Boot config protection	BOOT_CONFIG_PROT	1	[178]	0h
Boot bus Conditions	BOOT_BUS_CONDITIONS	1	[177]	0h
Reserved	–	1	[176]	0h
High-density erase group definition	ERASE_GROUP_DEF	1	[175]	0h
Boot write protection status registers	BOOT_WP_STATUS	1	[174]	0h
Boot area write protection register	BOOT_WP	1	[173]	0h
Reserved	–	1	[172]	0h
User area write protection register	USER_WP	1	[171]	0h
Reserved	–	1	[170]	0h
FW configuration	FW_CONFIG	1	[169]	0h
RPMB Size	RPMB_SIZE_MULT	1	[168]	20h
Write reliability setting register	WR_REL_SET	1	[167]	1Fh
Write reliability parameter register	WR_REL_PARAM	1	[166]	14h
Start Sanitize operation	SANITIZE_START	1	[165]	0h
Manually start background operations	BKOPS_START	1	[164]	0h
Enable background operations handshake	BKOPS_EN	1	[163]	0h
H/W reset function	RST_n_FUNCTION	1	[162]	0h
HPI management	HPI_MGMT	1	[161]	0h
Partitioning Support	PARTITIONING_SUPPORT	1	[160]	7h
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	[159:157]	467-8GB 934-16GB
Partitions attribute	PARTITIONS_ATTRIBUTE	1	[156]	0h
Partitioning Setting	PARTITION_SETTING_COMPLETED	1	[155]	0h
General Purpose Partition Size	GP_SIZE_MULT 4	3	[154:152]	0h
General Purpose Partition Size	GP_SIZE_MULT3	3	[151:149]	0h
General Purpose Partition Size	GP_SIZE_MULT2	3	[148:146]	0h

General Purpose Partition Size	GP_SIZE_MULT1	3	[145:143]	0h
Enhanced User Data Area Size	ENH_SIZE_MULT	3	[142:140]	0h
Enhanced User Data Start Address	ENH_START_ADDR	4	[139:136]	0h
Reserved	–	1	[135]	0h
Bad Block Management mode	SEC_BAD_BLK_MGMNT	1	[134]	0h
Production state awareness	PRODUCTION_STATE_AWARENESS	1	[133]	0h
Package Case Temperature is controlled	TCASE_SUPPORT	1	[132]	0h
Periodic Wake-up	PERIODIC_WAKEUP	1	[131]	0h
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_SUPPORT	1	[130]	1h
Reserved	–	2	[129:128]	0h
Vendor Specific Fields	VENDOR_SPECIFIC_FIELD	61	[127:67]	–
Error code	ERROR_CODE	2	[66:65]	0h
Error type	ERROR_TYPE	1	[64]	0h
Native sector size	NATIVE_SECTOR_SIZE	1	[63]	0h
Sector size emulation	USE_NATIVE_SECTOR	1	[62]	0h
Sector size	DATA_SECTOR_SIZE	1	[61]	0h
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	[60]	0h
Class 6 commands control	CLASS_6_CTRL	1	[59]	0h
Number of addressed group to be Released	DYNCAP_NEEDED	1	[58]	0h
Exception events control	EXCEPTION_EVENTS_CTRL	2	[57:56]	0h
Exception events status	EXCEPTION_EVENTS_STATUS	2	[55:54]	0h
Extended Partitions Attribute	EXT_PARTITIONS_ATTRIBUTE	2	[53:52]	0h
Context configuration	CONTEXT_CONF	15	[51:37]	-
Packed command status	PACKED_COMMAND_STATUS	1	[36]	0h
Packed command failure index	PACKED_FAILURE_INDEX	1	[35]	0h
Power Off Notification	POWER_OFF_NOTIFICATION	1	[34]	0h
Control to turn the Cache ON/OFF	CACHE_CTRL	1	[33]	0h
Flushing of the cache	FLUSH_CACHE	1	[32]	0h
Barrier control	BARRIER CTRL	1	[31]	0h
Mode config	MODE_CONFIG	1	[30:30]	0h
Mode operation codes	MODE_OPERATION_CODES	1	[29:29]	0h
Reserved	Reserved	2	[28:27]	0h
FFU status	FFU_STATUS	1	[26:26]	0h
Pre loading data size	PRE_LOADING_DATA_SIZE	4	[25:22]	0h
Max pre loading data size	MAX_PRE_LOADING_DATA_SIZE	4	[21:18]	15307776-8GB 30615552-16GB

Product state awareness enablement	PRODUCT_STATE_AWARENESS_ENABLEMENT	1	[17:17]	1h
Secure removal type	SECURE_REMOVAL_TYPE	1	[16:16]	1h
Command Queue Mode enable	CMQ_MODE_EN	1	[15:15]	0h
Reserved	Reserved	15	[14:0]	–

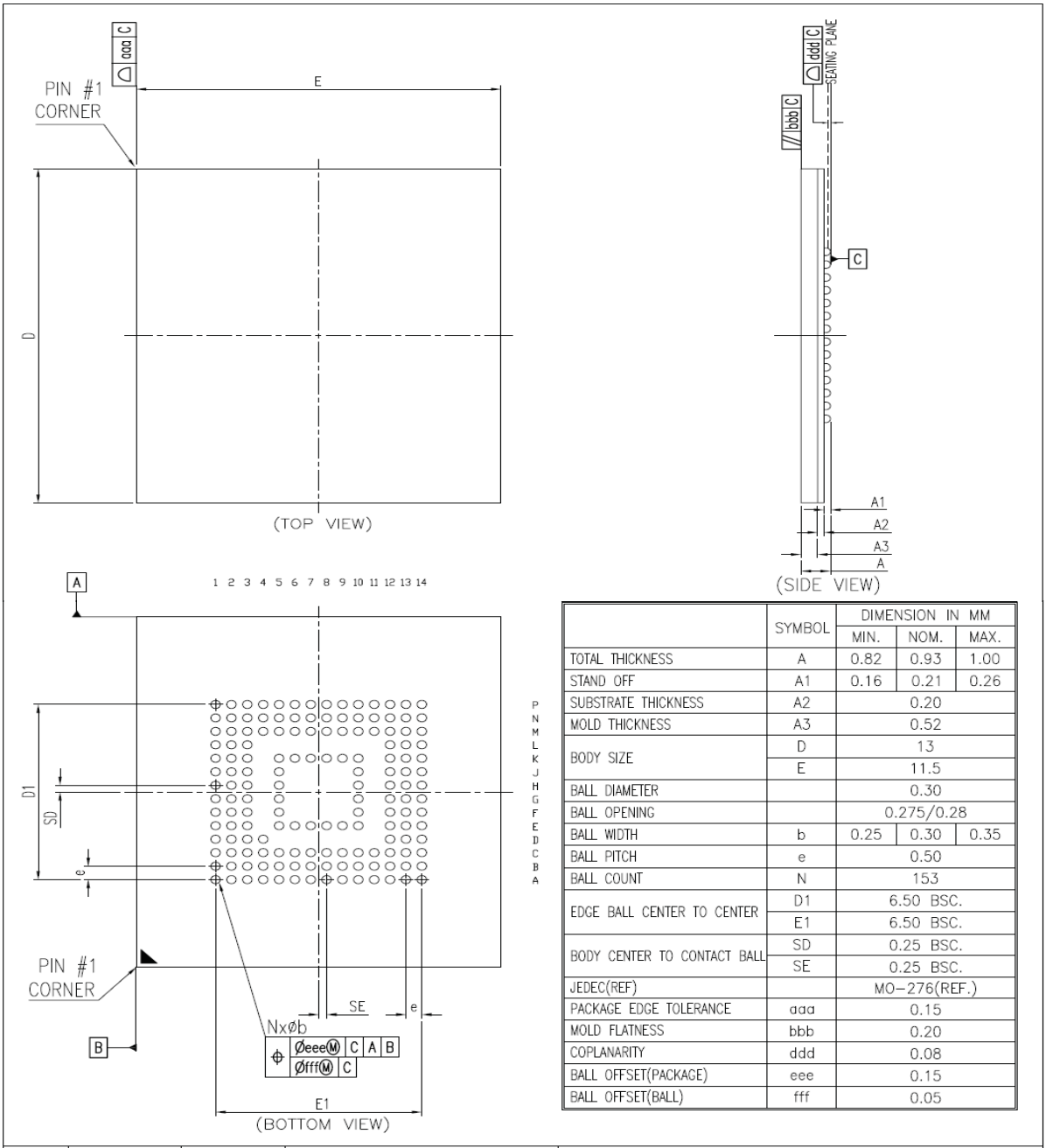
NOTES:

1. Reserved bits should read as “0.”
2. Obsolete values should be don’t care.
3. This field is 0 after power-on, H/W reset or software reset, thus selecting the backwards compatibility interface timing for the Device. If the host sets 1 to this field, the Device changes its timing to high speed interface timing (see Section 10.6.1 of JESD84-B50). If the host sets value 2 the Device changes its timing to HS200 interface timing (see Section 10.8.1 of JESD84-B50), If the host sets HS_TIMING[3:0] to 0x3,the device changes its timing to HS400 interface timing (see10.10).
4. It is set to ‘0’ (1 bit data bus) after power up and can be changed by a SWITCH command.
5. * Changed by Firmware release note.
6. The values of Device version, Cache size, Sector Count, Max Enhanced Area Size, Enhanced User Data Area Size and Max pre loading data size are expressed in Decimal, while the value of h is the abbreviation of Hexadecimal.

9. PACKAGE CONNECTIONS

■ Package Mechanical (11.5 x 13.0 x 1.0mm)

MEMA Series is assembled in a JEDEC standard 153 ball FBGA(TFBGA) package. Please refer below figure for relevant parameters of package dimension.

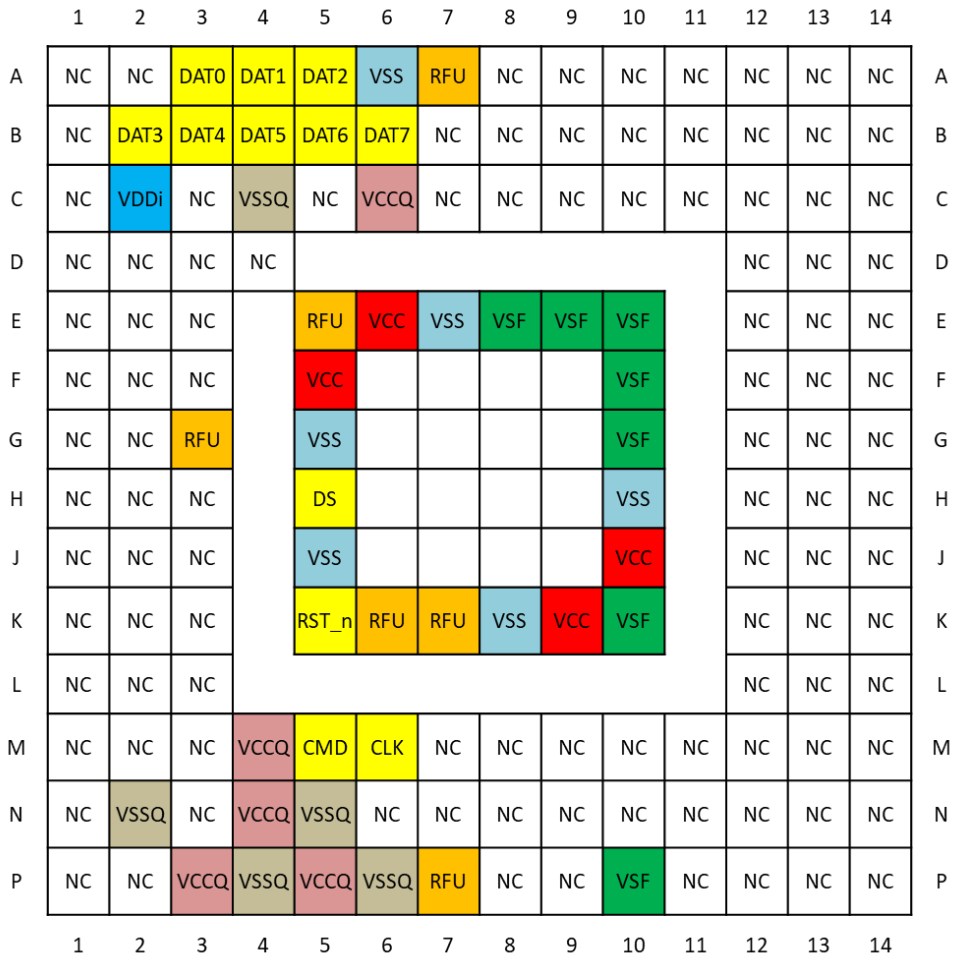


	SYMBOL	DIMENSION IN MM		
		MIN.	NOM.	MAX.
TOTAL THICKNESS	A	0.82	0.93	1.00
STAND OFF	A1	0.16	0.21	0.26
SUBSTRATE THICKNESS	A2		0.20	
MOLD THICKNESS	A3		0.52	
BODY SIZE	D		13	
	E		11.5	
BALL DIAMETER			0.30	
BALL OPENING			0.275/0.28	
BALL WIDTH	b	0.25	0.30	0.35
BALL PITCH	e		0.50	
BALL COUNT	N		153	
EDGE BALL CENTER TO CENTER	D1		6.50 BSC.	
	E1		6.50 BSC.	
BODY CENTER TO CONTACT BALL	SD		0.25 BSC.	
	SE		0.25 BSC.	
JEDEC(REF)			MO-276(REF.)	
PACKAGE EDGE TOLERANCE	aaa		0.15	
MOLD FLATNESS	bbb		0.20	
COPLANARITY	ddd		0.08	
BALL OFFSET(PACKAGE)	eee		0.15	
BALL OFFSET(BALL)	fff		0.05	

UNLESS OTHERWISE SPECIFIED	DECIMAL .X ± .XX ±.10 .XXX ±.05	ANGULAR ±3°	THIRD ANGLE PROJECTION :	
DRAWN	Vivian Lin 2021.07.15	UNIT: mm	SCALE: 8:1	TITLE: Package Outline Dimension Drawing For eMMC SiP 11.5x13x1.0mm Ball Pitch 0.5mm, Ball Size 0.3mm, For Phison Only
CHECKED	Vivian Lin 2021.07.15	JEDEC NO.:	MO-276(REF.)	
APPROVED	Curt Chiang	PACKAGE CODE :	PSMC	
APPROVED	Dave Yang	DWG. NO.: PD-PS67-P26	DOC. NO.: PD-PS67	REV.: E SHEET : 26 OF 26 A3

Figure 9-1 Package Dimension

10. SIGNAL ASSIGNMENT (153 BALL)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	NC	NC	DAT0	DAT1	DAT2	VSS	RFU	NC	NC	NC	NC	NC	NC	NC	A
B	NC	DAT3	DAT4	DAT5	DAT6	DAT7	NC	NC	NC	NC	NC	NC	NC	NC	B
C	NC	VDDi	NC	VSSQ	NC	VCCQ	NC	NC	NC	NC	NC	NC	NC	NC	C
D	NC	NC	NC	NC								NC	NC	NC	D
E	NC	NC	NC		RFU	VCC	VSS	VSF	VSF	VSF		NC	NC	NC	E
F	NC	NC	NC		VCC					VSF		NC	NC	NC	F
G	NC	NC	RFU		VSS					VSF		NC	NC	NC	G
H	NC	NC	NC		DS					VSS		NC	NC	NC	H
J	NC	NC	NC		VSS					VCC		NC	NC	NC	J
K	NC	NC	NC		RST_n	RFU	RFU	VSS	VCC	VSF		NC	NC	NC	K
L	NC	NC	NC									NC	NC	NC	L
M	NC	NC	NC	VCCQ	CMD	CLK	NC	NC	NC	NC	NC	NC	NC	NC	M
N	NC	VSSQ	NC	VCCQ	VSSQ	NC	NC	NC	NC	NC	NC	NC	NC	NC	N
P	NC	NC	VCCQ	VSSQ	VCCQ	VSSQ	RFU	NC	NC	VSF	NC	NC	NC	NC	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 10-1 153 Ball Assignment

11. SIGNAL DESCRIPTION

Table 11-1 Signal Description

Pin	Description
CLK	Clock Signal.
CMD	Command Signal.
DS	Data Strobe Signal , Used in HS400 mode.
DAT0~7	Data Bus.
RST_N	Hardware Reset Signal.
VCC	Supply voltage for controller and Flash memory power.
VCCQ	Supply voltage for controller and Flash memory IO power.
VDDi	Connect capacitor from VDDi to GND for stabilize internal power.
VSS	Supply voltage ground for controller and Flash memory. Can be short with VSSQ.
VSSQ	Supply voltage ground for controller and IO Flash memory. Can be short with VSSQ.
NC	In eMMC chip is no connect. Left it floating.
RFU	Reserved for future use. Left it floating for future use.
VSF	Vendor Specific Function. Reserved for test points on the PCB, default NU (Not Used)

Some balls could be floated to achieve eMMC 4.5 force conversion.

- A6 VSS → Float NC
- J5 VSS → Float NC
- H5 DS → Float NC

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for eMMC ***category:***

Click to view products by Mk ***manufacturer:***

Other Similar products are found below :

SDINBDG4-8G-ZA2 S40FC004C1B2I00300 FEMDRW128G-88A19 ZDEMDCM064G-95A8 KLM8G1GEUF-B04P FEMDNN016G-A3A55 FEMDMW016G-88A43 FEMDMW064G-88A19 FEMDRW016G-88A43 FEMDME064G-A8A58 THGAMRG7T13BAIL KLM8G1GETF-B041006 KLMCG2UCTB-B041 KLMCG2UCTA-B041 KLMCG4JEUD-B04Q H26M41208HPRA H26M51002KPR ZDEMMC16GA FEMDME032G-A8A58 THGAMRG8T13BAIL SDINBDV4-32G SDDDC4DR-64G SDADA4DR-64G FEMDME004G-A8A39 MKEMF008GT1E-I MKEV008GCB-SC510 MKEMF064GT1E-C MKEMF032GT1E-C MKEMC004GT1E-IE MKEMC008GT2M-C MKEMC004GT1M-C MKEV004GCB-SC510 MKEMF008GT1E-IE ZDEMDCM004G-BG25 MKEMF032GT2E-IE SDINBDG4-16G SDINBDG4-8G SDINBDG4-8G-XI1 SDINBDG4-8G-I1 SDINBDG4-16G-I1 SDINADF4-16G-H SDINBDG4-32G SDINBDG4-8G-ZA SDINBDG4-64G-I1 SFEM032GB1EA1TO-I-LF-111-STD SDINBDG4-32G-ZA SDINBDG4-32G-XA THGBMNG5D1LBAIT THGBMNG5D1LBAIL SDINBDG4-64G-XI1