MK NAND FLASH Product Datasheet

Product List

MKPV8G08CT-KS
8Gbit NAND Flash

http://www.mkfounder.com

Revision History

Version	Date	Description
Rev 1.0	2021/4/20	Original version

Notice :

The datasheet is prepared and approved by MK Founder semiconductor co., LTD.

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1 Introduction

1.1 General Description

The MK 8Gb SD NAND is offered in 3.3 VCC with x8 I/O interface,and compliant with ONFI1.0. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.

1.2 Features

- **Density**：8 Gbit (4Gb*2)
- **Architecture**

Architecture (for each 4 Gb device)
Input / Output Bus Width: 8 bits
Page Size
4 Gb: (2048 + 128) bytes; 128-byte spare area
Block Size: 64 Pages
4 Gb: 128 KB + 8 KB
Plane Size
4 Gb: 2048 blocks per plane or (256 MB + 16 MB)
Device Size
4 Gb: Two planes per device or 512 MB

- **NAND Flash Interface**

Open NAND Flash Interface (ONFI) 1.0 compliant
Address, Data, and Commands multiplexed

- **Supply Voltage**

3.3 V device：VCC = 2.7 V ~ 3.6 V

- **Performance**

Page Read / Program
Read Page Time (tR):
➢ 45 µs (Typ) / Single Plane
➢ 55 µs (Typ) / Multiplane
Program time / Multiplane Program time: 350 µs (Typ)

- **Block Erase / Multiplane Erase**

Block Erase time: 4 ms (Typ)

- **Reliability**

60,000 Program / Erase cycles (Typ)
10 Year Data retention (Typ)
Blocks 0-7 are good at the time of shipment

- **Security**

OTP area
Serial number (unique ID)
Hardware program/erase disabled during power transition

Volatile and Permanent Block Protection

- **Electronic Signature**

Manufacturer ID: ADh

Device ID: Follow industry standard for single and stacked die implementation

- **Operating Temperature**

Industrial: –40 °C to 85 °C

- **Additional Features**

Multiplane Program and Erase commands

Copy Back Program

Multiplane Copy Back Program

Reset (FFh) command is required after power-on as a first command

- **Package Options**

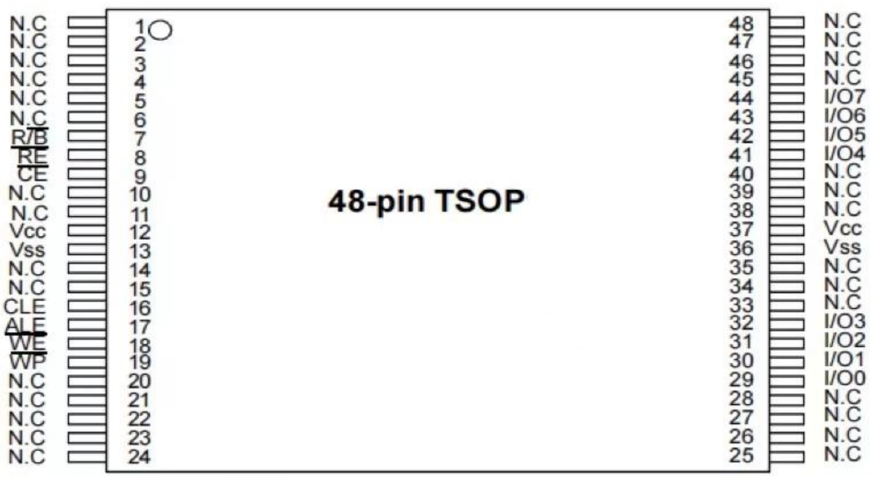
48-Pin TSOP

1.3 Product List

Part Number	Density	Interface	VCC Range	PACKAGE
MKPV8G08CT-KS	8Gbit	ONFI 1.0	2.7V ~ 3.6V	TSOP48

2 Connection Diagram

Figure 1. 48-Pin TSOP



3 Pin Description

Table 1. Pin Description

Pin Name	Description
I/O0 - I/O7	**Inputs/Outputs**. The I/O pins are used for command input, address input, data input, and data output. The I/O pins float to High-Z when the device is deselected or the outputs are disabled.
CLE	**Command Latch Enable.** This input activates the latching of the I/O inputs inside the Command Register on the rising edge of Write Enable (WE#).
ALE	**Address Latch Enable.** This input activates the latching of the I/O inputs inside the Address Register on the rising edge of Write Enable (WE#).
CE#	Chip Enable. This input controls the selection of the device. When the device is not busy, CE# LOW selects the memory.
WE#	Write Enable. This input latches Command, Address, and Data. The I/O inputs are latched on the rising edge of WE#.
RE#	**Read Enable.** The RE# input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid t_{REA} after the falling edge of RE# which also increments the internal column address counter by one.
WP#	**Write Protect.** The WP# pin, when LOW, provides hardware protection against undesired data modification (program / erase).
R/B#	**Ready Busy**. The Ready/Busy output is an Open Drain pin that signals the state of the memory.
VCC	**Supply Voltage**. The V_{CC} supplies the power for all the operations (Read, Program, Erase). An internal lock circuit prevents the insertion of Commands when V_{CC} is less than V_{LKO}.
VSS	Ground.
NC	Not Connected.

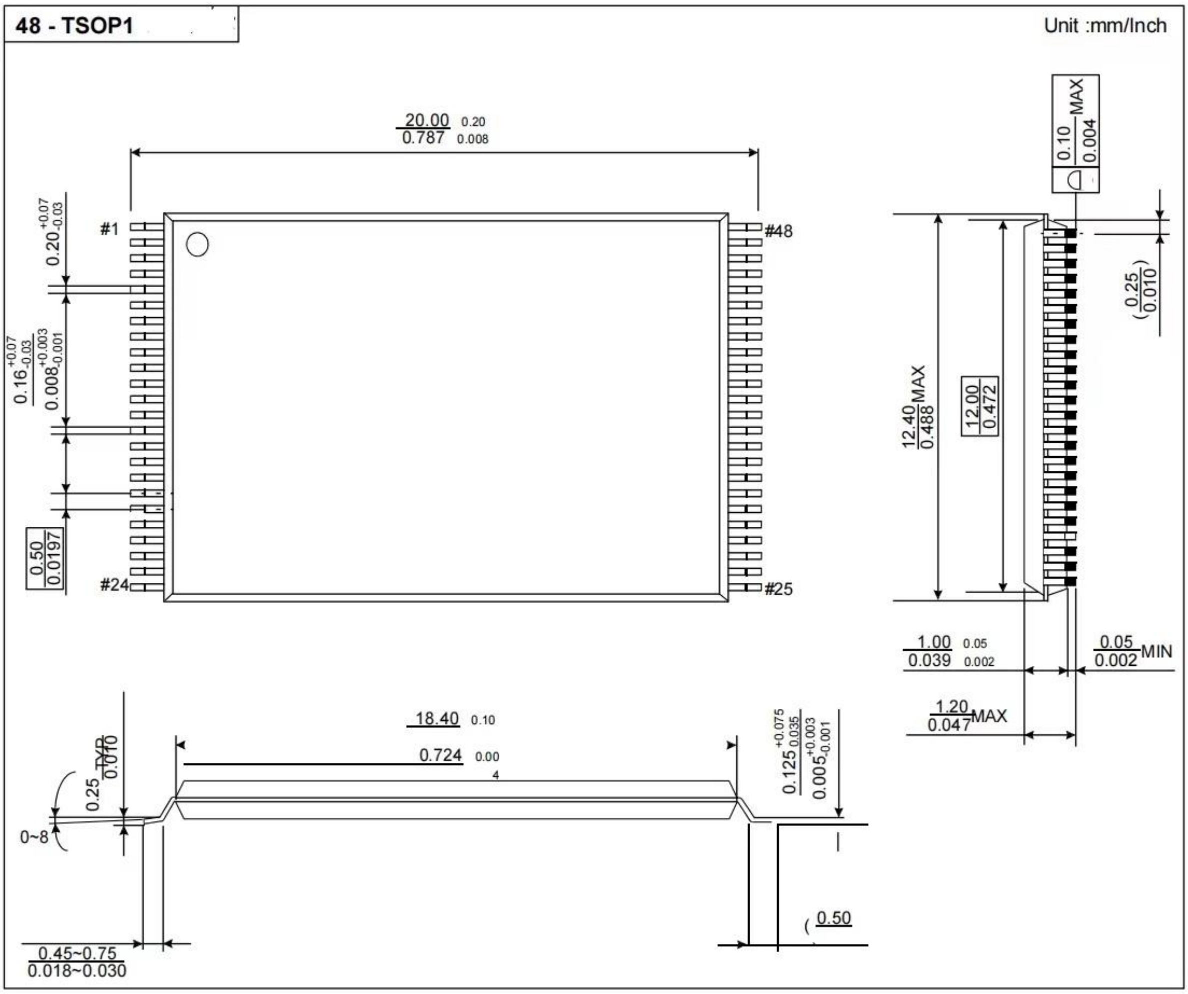
Notes

A 0.1 µF capacitor should be connected between the VCC Supply Voltage pin and the VSS Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.

An internal voltage detector disables all functions whenever VCC is below 1.8V to protect the device from any involuntary program/erase during power transitions.

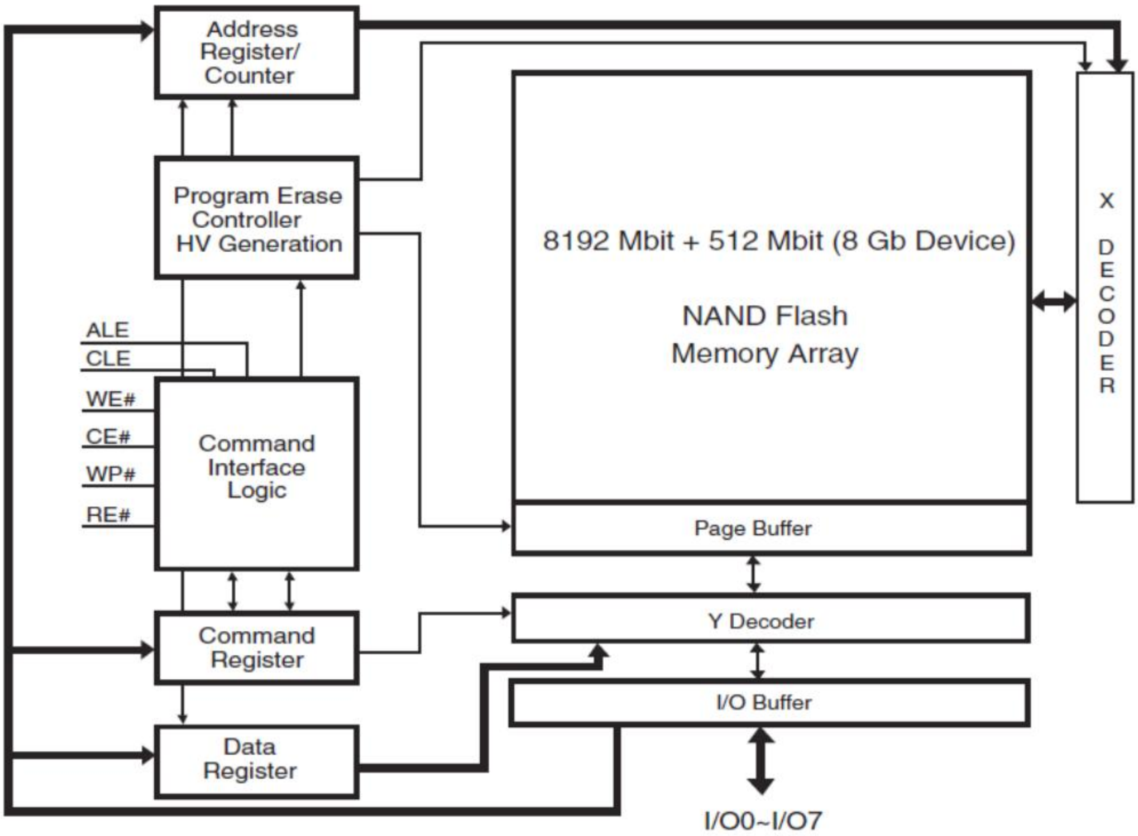
4 Package Diagrams

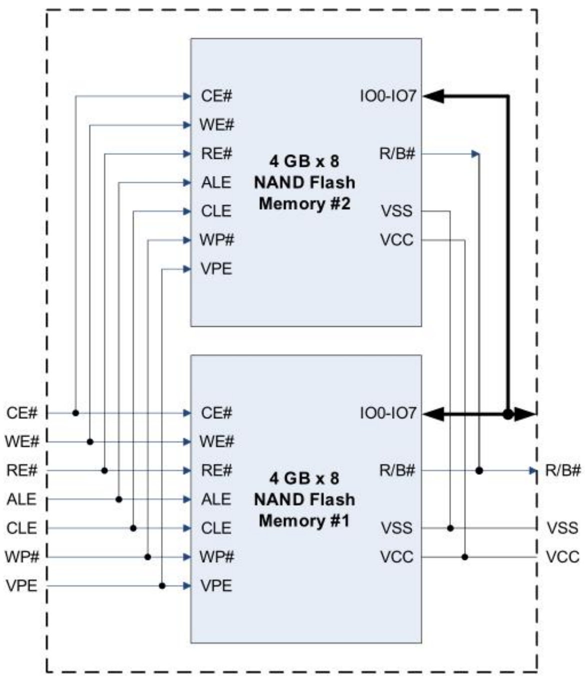
4.1 48-Pin Thin Small Outline Package (TSOP)



5 Block Diagrams

Figure 3. Functional Block Diagram





6 Addressing

Table 2 provides the address phase cycles for the X8 mode of operation.

Table 2. Address Phase Cycles for X8 Mode of Operation

Bus Cycle	Name	IO[7]	IO[6]	IO[5]	IO[4]	IO[3]	IO[2]	IO[1]	IO[0]
1st	Col Add 1 (C1)	CA[7]	CA[6]	CA[5]	CA[4]	CA[3]	CA[2]	CA[1]	CA[0]
2nd	Col Add 2 (C2)	L	L	L	CA[12]	CA[11]	CA[10]	CA[9]	CA[8]
3rd	Row Add 1 (R1)	BA[1]	BA[0]	PA[5]	PA[4]	PA[3]	PA[2]	PA[1]	PA[0]
4th	Row Add 2 (R2)	BA[9]	BA[8]	BA[7]	BA[6]	BA[5]	BA[4]	BA[3]	BA[2]
5th	Row Add 3 (R3)	L	L	L	L	L	BA[12]	BA[11]	BA[10]

Legend
CAx = Column Address bit.
PAx = Page Address bit.
BAx = Block Address bit.

Note . Block address concatenated with page address = actual page address, also known as the row address.

Density_Page Size	x8 Bus Width	Additional Notes
	CA[12:0]	
8Gb_2KB	CA[12]=L,CA[11:0]	

Note . Block address
BA[12:0]

Density_Page Size	#of LUNs	# of Planes	#Blocks per Plane	BA	Additional Notes
8Gb_2KB	1	2	2048	BA[12:0]	BA[0] controls plane selection.

7 Read Status Enhanced

Read Status Enhanced is used to retrieve the status value for a previous operation in the following cases:

In the case of concurrent operations on a multi-die stack: When two dies are stacked to form a dual-die package (DDP), it is possible run one operation on the first die, then activate a different operation on the second die. For example: Erase while Read, Read while Program, and so on.

In the case of multiplane operations in the same die.

8 Read ID

The device contains a product identification mode, initiated by writing 90h to the Command Register, followed by an address input of 00h.

Note If you want to execute Read Status command (0x70) after Read ID sequence, you should input dummy command (0x00) before Read Status command (0x70).

For the devices, five read cycles sequentially output the manufacturer code , and the device code and 3rd, 4th, and 5th cycle ID, respectively. The Command Register remains in Read ID Mode until further commands are issued to it.

Table 3. Read ID for Supported Configurations

Density	Org	V_{CC}	1st	2nd	3rd	4th	5th
8 Gb	x8	3.3V	ADh	DCh	01h	05h	04h

Table 4. Read ID Bytes

Device Identifier Byte	Description
1st	Manufacturer Code
2nd	Device Identifier
3rd	Internal chip number, cell type
4th	Page Size, Block Size, Spare Size, Organization
5th	Multiplane information

3rd ID Data

Table 5. Read ID Byte 3 Description

	Description	I/O7	I/O6	I/O5 I/O4	I/O3 I/O2	I/O1 I/O0
Internal Chip Number	1 2 4 8					0 0 0 1 1 0 1 1
Cell type	2-level cell 4-level cell 8-level cell 16-level cell				0 0 0 1 1 0 1 1	
Reserved	0	0	0	0		

4th ID Data

Table 6. Read ID Byte 4 Description

	Description	I/O7	I/O6	I/O5 I/O4	I/O3	I/O2	I/O1 I/O0
Page Size (without spare area)	2 KB 4 KB						0 1 1 0
Block Size (without spare area)	128 KB 256 KB	0 0		0 0 0 1			
Spare Area Size	128B 256B				0 1	1 0	
Organization	×8		0				

5th ID Data

Table 7. Read ID Byte 5 Description

	Description	I/O7	I/O6 I/O5 I/O4	I/O3 I/O2	I/O1 I/O0
Plane Number	1 2 4 8			00 01 10 11	
Reserved		0	0		0

9 Read Parameter Page

The device supports the ONFI Read Parameter Page operation, initiated by writing ECh to the Command Register, followed by an address input of 00h. The host may monitor the R/B# pin or wait for the maximum data transfer time (tR) before reading the Parameter Page data. The Command Register remains in Parameter Page Mode until further commands are issued to it. If the Status Register is read to determine when the data is ready, the Read Command (00h) must be issued before starting read cycles. Table 8 explains the parameter fields.

Table 8. Parameter Page Description

Byte	O/M	Description	Values
Revision Information and Features Block			
0-3	M	Parameter page signature Byte 0: 4Fh, “O” Byte 1: 4Eh, “N” Byte 2: 46h, “F” Byte 3: 49h, “I”	4Fh, 4Eh, 46h, 49h
4-5	M	Revision number 2-15 Reserved (0) 1 1 = supports ONFI version 1.0 0 Reserved (0)	02h, 00h
6-7	M	Features supported 5-15 Reserved (0) 4 1 = supports odd to even page Copyback 3 1 = supports interleaved operations 2 1 = supports non-sequential page programming 1 1 = supports multiple LUN operations 0 1 = supports 16-bit data bus width	18h, 00h
8-9	M	Optional commands supported 6-15 Reserved (0) 5 1 = supports Read Unique ID 4 1 = supports Copyback 3 1 = supports Read Status Enhanced 2 1 = supports Get Features and Set Features 1 1 = supports Read Cache commands 0 1 = supports Page Cache Program command	3Ch, 00h

Byte	O/M	Description	Values
10-31		Reserved (0)	00h
Manufacturer Information Block			
32-43	M	Device manufacturer (12 ASCII characters)	53h, 50h, 41h, 4Eh, 53h, 49h, 4Fh, 4Eh, 20h, 20h, 20h, 20h
44-63	M	Device model (20 ASCII characters)	53h, 33h, 34h, 4Dh, 4Ch, 30h, 38h, 47h, 33h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	M	JEDEC manufacturer ID	ADh
65-66	O	Date code	00h
67-79		Reserved (0)	00h
Memory Organization Block			
80-83	M	Number of data bytes per page	00h, 08h, 00h, 00h
84-85	M	Number of spare bytes per page	80h, 00h
86-89	M	Number of data bytes per partial page	00h, 02h, 00h, 00h
90-91	M	Number of spare bytes per partial page	20h, 00h
92-95	M	Number of pages per block	40h, 00h, 00h, 00h
96-99	M	Number of blocks per logical unit (LUN)	00h, 20h, 00h, 00h
100	M	Number of logical units (LUNs)	01h
101	M	Number of address cycles 4-7 Column address cycles 0-3 Row address cycles	23h
102	M	Number of bits per cell	01h
103-104	M	Bad blocks maximum per LUN	50h, 00h
105-106	M	Block endurance	08h, 04h (–40°C to 85°C)

			06h, 04h (–40°C to 105°C)
107	M	Guaranteed valid blocks at beginning of target	08h
108-109	M	Block endurance for guaranteed valid blocks	00h, 00h
110	M	Number of programs per page	04h
111	M	Partial programming attributes 5-7 Reserved 4 1 = partial page layout is partial page data followed by partial page spare 1-3 Reserved 0 1 = partial page programming has constraints	00h
112	M	Number of bits ECC correctability	00h
113	M	Number of interleaved address bits 4-7 Reserved (0) 0-3 Number of interleaved address bits	01h
114	O	Interleaved operation attributes 4-7 Reserved (0) 3 Address restrictions for program cache 2 1 = program cache supported 1 1 = no block address restrictions 0 Overlapped / concurrent interleaving support	00h
115-127		Reserved (0)	00h
Electrical Parameters Block			
128	M	I/O pin capacitance	0Ah

Table 8. Parameter Page Description (Continued)

Byte	O/M	Description	Values
129-130	M	Timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0, shall be 1	3Fh, 00h
131-132	O	Program cache timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0	00h, 00h
133-134	M	t_{PROG} Maximum page program time (µs)	58h, 02h
135-136	M	t_{BERS} Maximum block erase time (µs)	10h, 27h
137-138	M	t_R Maximum page read time (µs)	C2h, 01h
139-140	M	t_{CCS} Minimum Change Column setup time (ns)	C8h, 00h
141-163		Reserved (0)	00h
Vendor Block			
164-165	M	Vendor specific Revision number	00h
166-253		Vendor specific	00h
254-255	M	Integrity CRC	87h, 95h (–40°C to 85°C) 0Dh, BDh (–40°C to 105°C)

Redundant Parameter Pages			
256-511	M	Value of bytes 0-255	Repeat Value of bytes 0-255
512-767	M	Value of bytes 0-255	Repeat Value of bytes 0-255
768+	O	Additional redundant parameter pages	FFh

Note "O" Stands for Optional, "M" for Mandatory.

10 OTP

The device contains a OTP area, that consists of one block (64 pages), which is accessed in two different ways:

1、Legacy Vendor Command Method

2、SET FEATURE Method

OTP Access

Legacy Vendor Method: The OTP area is located in block #6.

The OTP entry/program/read sequences are as follows:

Entry: 29h - 17h - 04h - 19h

Program: 80h - 00h - 00h - 80h - 01h - 00h - 10h

Read: 00h - 00h - 00h - 80h - 01h - 00h - 30h

SET FEATURE Method: Issue SET FEATURE (EFh) command followed by feature address 90h and the data P1 = 09h, P2 = 00h, P3 = 00h, and P4 = 00h.

Once in OTP Mode, all subsequent Page Read and Page Program commands are applied to the OTP area. ERASE commands are not valid in OTP Mode.

Copyback and Reprogram commands shown in the commands Set are not supported in OTP Mode.

10.1 OTP Protection

Legacy Vendor Method: Issue OTP protection vendor command sequence 4Ch-03h-1Dh-41h-80h followed by an address of 00h/ 00h/00h/00h/00h and 10h command.

SET FEATURE Method: Issue SET FEATURE (EFh) command followed by feature address 90h and the data P1 = 0Bh, P2 = 00h, P3 = 00h, and P4 = 00h.

The Status Register read command can be used to poll the Status Register to determine when the programming operation is completed and verify that the OTP area is protected.

The OTP protection sequences described above assume the device is in OTP Mode.

However, if the OTP entry is executed by issuing Set Feature (EFh) command with Feature Address 90h, then the OTP protect will be applicable to both the first and second die.

OTP Exit

Legacy Vendor Method: Issue the Reset (FFh) command to exit the OTP Mode.
SET FEATURE Method: Issue SET FEATURE (EFh) command with feature address 90h and the data P1 = 08h, P2 = 00h, P3 = 00h, and P4 = 00h
The OTP area is of a single erase block size (64 pages), and hence only row addresses between 00h and 3Fh are allowed. The Block Erase command is not allowed in the OTP Mode.

11 Security Features

The security features below provide block protection from program and erase operations.
Two security methods are supported:

- Volatile Block Protection (VBP)

The VBP parameter settings are volatile. Power cycling will reset the settings to the default status (all blocks protected if VPE pin is HIGH). This VBP method can protect one range of contiguous blocks.
This method requires use of a Volatile Protection Enable (VPE) input pin. To activate the VBP method using the VPE input, the host must power up the device with VPE input HIGH during the Power-on Reset (POR) period and issue a set of commands to set the VBP parameter settings which consist of a Lower Boundary Address (LB_ADD) and an Upper Boundary Address (UB_ADD).

- Permanent Block Protection (PBP)

The PBP parameter settings are nonvolatile. These settings will be maintained after a power cycle. The PBP method can protect up to 64 blocks (block 0 to 63) organized in groups of 4 contiguous blocks. Each group can be protected individually and are permanently protected. Once a group is protected, the group can no longer be unprotected.

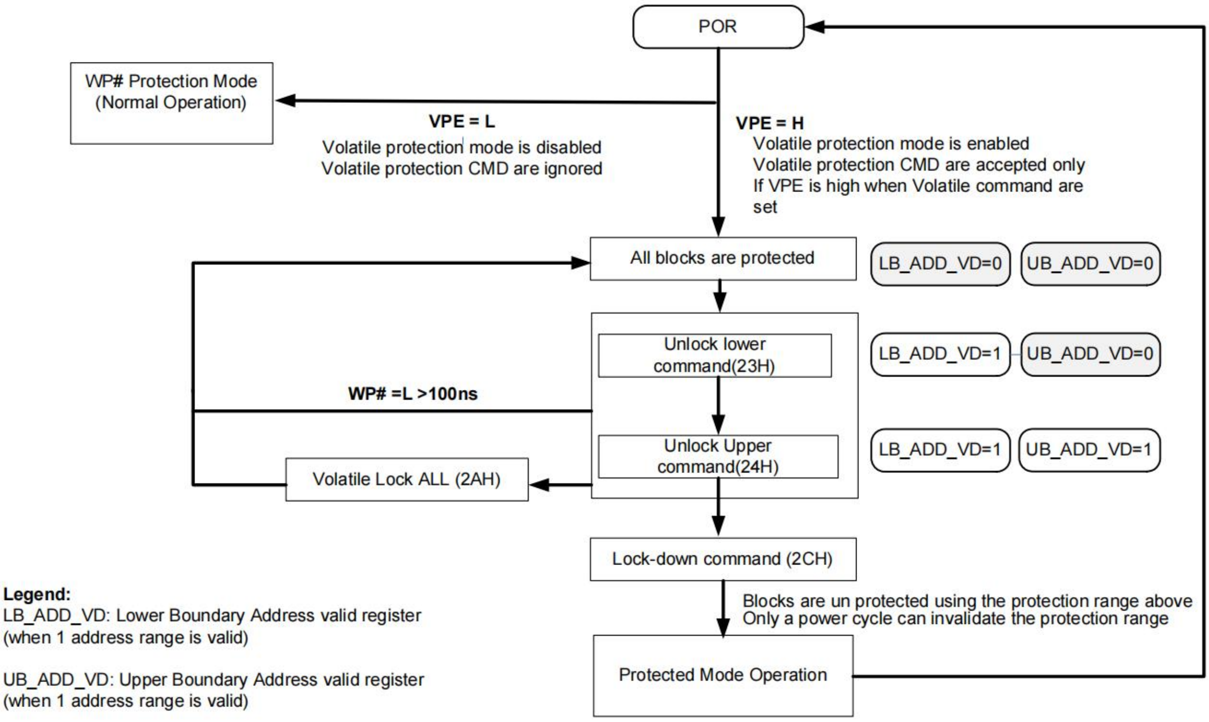
11.1 Volatile Block Protection (VBP) Overview

The VBP feature can protect all blocks, or one selected range of contiguous blocks, from erase and program operations. The VBP parameter settings are reset to default value after a power-cycle (all blocks protected if VPE input is HIGH) and must be re-programmed by the host.
The VPE input level, latched during POR, determines whether the VBP is enabled or disabled. If the VPE input is LOW at power-on, the VBP feature is disabled and the Write Protect (WP#) input controls the protection of all blocks. If the VPE input is HIGH at power-on, all blocks are protected from programming or erasing even if the WP# input is HIGH. VPE must be HIGH (VPE=H) when issuing all VBP function commands.
The Unlock Block commands (23h & 24h) are used to unprotect a range of blocks. The Unlock Block commands set the protection registers (UB_ADD and LB_ADD).
Once the selected blocks are unprotected, those blocks can be protected again by using a Lock All Blocks (2Ah) commands or by asserting WP# LOW for more than 100ns.
Once the selected blocks are unprotected, the host can issue a Lock-down command (2Ch) to lock the VBP protection range configuration until the next power off to on cycle.
After, the Lock-down command is issued:
VPE signal value and the VBP commands are ignored until the next power cycle.

WP# can be used to protect all the blocks from program and erase, but will no longer invalidate the volatile protection parameter registers.

Figure 5. provides an overview of the VBP mechanism.

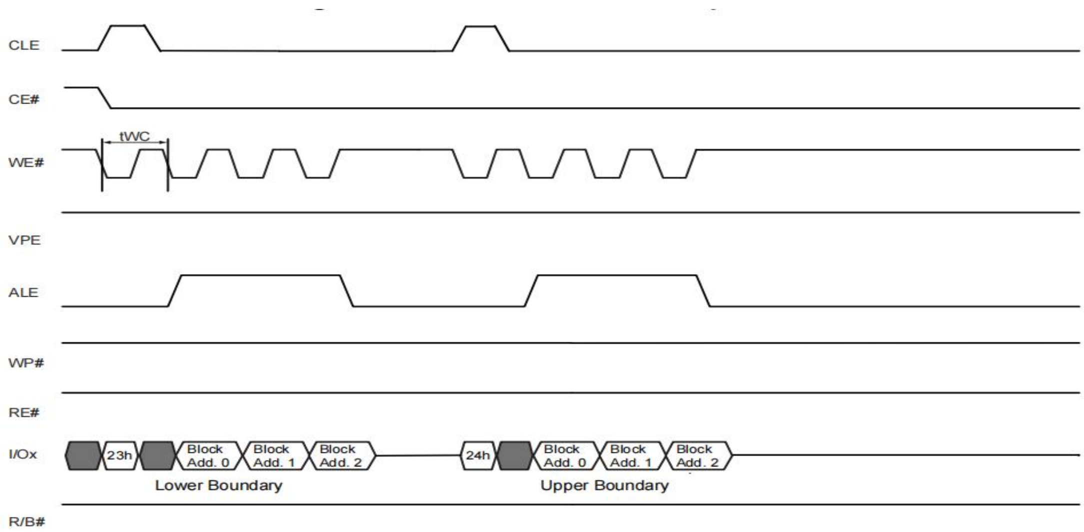
Figure 5. VBP Flowchart



11.1.1 VBP Unlock Block (23h and 24h) Commands Waveforms

The Unlock Block commands define the range of blocks to be unprotected. The Unlock Lower command (23h) sets the lower block address, and must be followed by the Unlock Upper command (24h) that sets the upper block address (see Figure 6).

Figure 6. Waveforms for Block unprotected



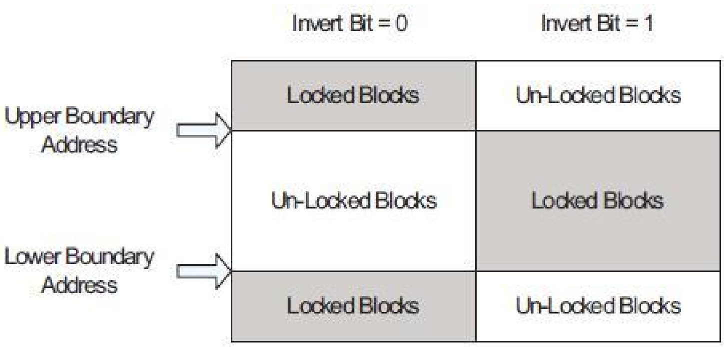
To unprotected the complementary range of block (see Figure 7), the host can set an invert-bit in the Unlock command address field (see Table 9). If the invert-bit is set to 0, the unprotected area is within and inclusive of the upper and lower block addresses; if the bit is set to 1, the unprotected area is outside and exclusive of the upper and lower block addresses.

Table 9. Address Definition of Unlock Block

Address Cycle Mapping									
	Bus Cycle	IO[7]	IO[6]	IO[5]	IO[4]	IO[3]	IO[2]	IO[1]	IO[0]
BlockAddress 1	1st	BA[1]	BA[0]	L	L	L	L	L	InvertBit[7]
BlockAddress 2	2nd	BA[9]	BA[8]	BA[7]	BA[6]	BA[5]	BA[4]	BA[3]	BA[2]
BlockAddress 3	3rd	L		L	L	L	BA[12]	BA[11]	BA[10]
BA[0] controls plane selection.									

Note: The Invert bit is set by 24h command to select whether the unprotected range is inside or outside of the range boundary. The bit is a don't care for the 23h command.

Figure 7. Unlock Range Option



In multiplane operations, the lower and upper address range BA[0] is internally respectively set to 0 and 1. For example, if a block range being protected is defined to be between 1 and 4, the device will protect block 0 to 5.

Table 10 illustrates how internally the blocks are being protected for single and multiplane operations (shaded area) when the lower and upper addresses are respectively set to 1 and 4.

Table 10. Single and Dual Plane Block Protection Example

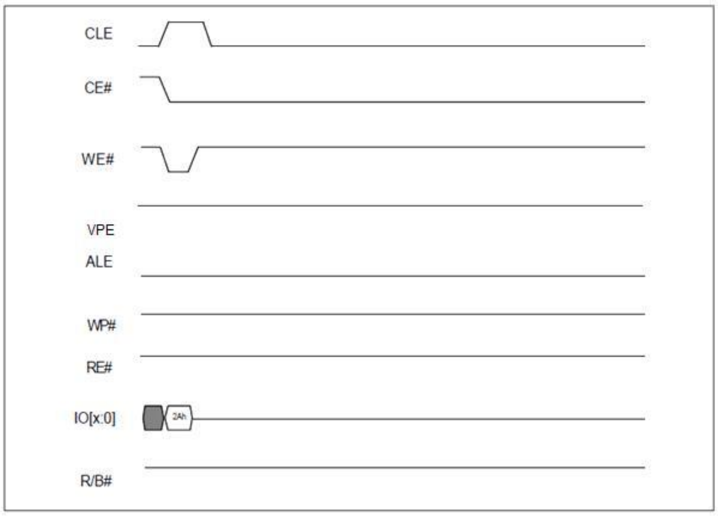
Single Plane Operation		Multi plane Operation	
Block 0	Block 1	Block0	Block 1
Block 2	Block 3	Block2	Block 3
Block 4	Block 5	Block4	Block 5

Note: Shaded boxes are protected by VBP.

11.1.2 VBP Lock All (2Ah) Command Waveforms

The Lock All command (2Ah) can be used to protect all the blocks in the device. This command is useful to program a new unprotected range as shown in Figure 5.

Figure 8. Waveforms for Lock All Blocks



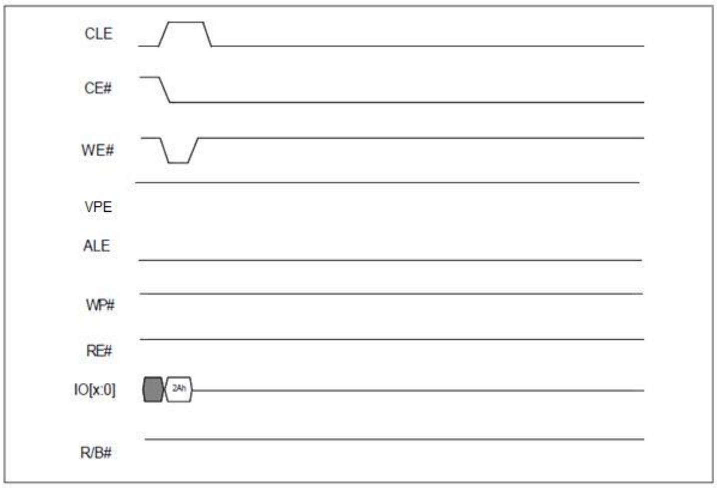
11.1.3 VBP Lock-down (2Ch) Command Waveforms

The Lock-down Command (2Ch) maintains the block protection parameters at the time the command is issued; the protected blocks cannot be unprotected and the unprotected blocks cannot be protected by software. Once the Lock-down command is issued, only a power off to power on cycle will change the block protection status by returning to the default state (all blocks protected state if VPE input is HIGH on power on). The WP# input and VPE input must be HIGH before issuing the Lock-down command.

After, the Lock-down command is issued:

- VPE signal value and the VBP commands are ignored until the next power cycle or hardware reset.
- WP# can be used to protect all the blocks from program and erase, but will no longer invalidate the volatile protection parameter registers.

Figure 9. Waveforms for the Lock-down Command



11.1.4 Permanent Block Protection (PBP) Overview

The PBP feature provides protection of up to sixteen groups (64 blocks total) from program and erase operations.

The device ships from the factory with no blocks protected by the PBP method.

Because this block protection is permanent, a power-on to power-off sequence does not affect the block protection status after the PBP command is issued.

The PBP method is used to select a group of blocks in the main array to be protected from program and erase operation. Multiple groups of blocks can be protected at the same time. Once a group of blocks is protected, the group of blocks can no longer be unprotected.

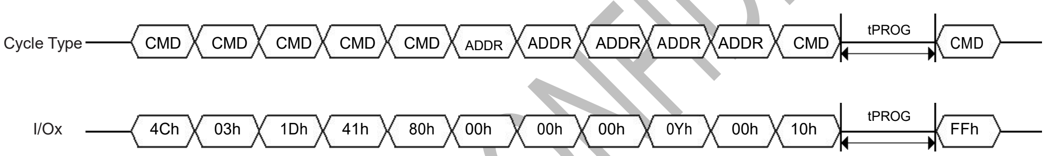
Additional unprotected groups can still be protected using the PBP sequence until the host issues a Permanent Block Protection Lock-down (PBPLDL) command.

When this PBPLDL command is issued, all groups of blocks protected by PBP are permanently protected from program and erase operations and a PBP operation can no longer be used to protect additional groups.

Issuing of the PBPLDL sequence will both protect and lock down the protected group. Each PBP and PBPLDL sequence must be exited using the reset command (FFh).

The timing diagram in Figure 10 shows the PBP sequence.

Figure 10. Timing Diagram for the PBP Sequence



The group of blocks being protected is determined by the value of Y (see Table 11) on the fourth address cycle.

During PBP PGM busy, if FFh or power-off occurs, PBP cannot be guaranteed.

Table 11. Fourth Address Cycle (ADDR 4) Protection Scheme Table

Y Value	Protected Group	Protected Blocks
0000	0	0,1,2,3
0001	1	4,5,6,7
0010	2	8,9,10,11
0011	3	12,13,14,15
0100	4	16,17,18,19
0101	5	20,21,22,23
0110	6	24,25,26,27
0111	7	28,29,30,31
1000	8	32,33,34,35
1001	9	36,37,38,39
1010	10	40,41,42,43
1011	11	44,45,46,47
1100	12	48,49,50,51
1101	13	52,53,54,55
1110	14	56,57,58,59
1111	15	60,61,62,63

Note Maximum number of PBP and PBPLDL sequences allowed are 16. Any generated sequence is considered as one attempt. The user should avoid issuing a sequence to protect a group that was previously protected.

Table 12. PBP and PBPLDL Sequences

Description	Entry Sequence				CMD Cycle	Address Cycles	CMD Cycle	Read Status or Monitor RB# Output Cycles	Reset (Exit)
PBP sequence	CMD1 (4Ch)	CMD2 (03h)	CMD3 (1Dh)	CMD4 (41h)	80h	00h, 00h,00h, 0Yh ,00h	10h	70h or 78h (Program Operation forces RDBY low)	FFh
PBPLDL sequence	CMD1 (4Ch)	CMD2 (03h)	CMD3 (1Dh)	CMD4 (41h)	80h	00h, 00h,00h, 1Y,00h	10h	70h or 78h (Program Operation forces RDBY low)	FFh

11.1.5 Block Protection Status Read Command (7Ah) Waveform

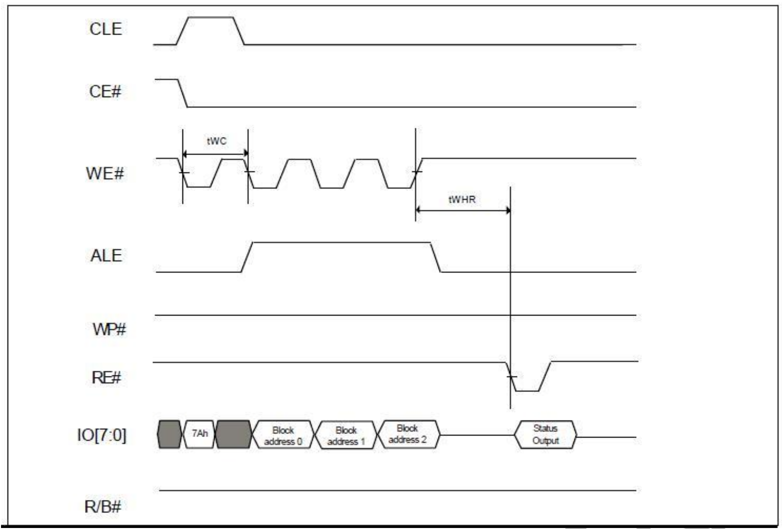
Figure 11 shows the Block Protection Status Read waveform. The Block Protection Status Read command (7Ah) is followed by three address cycles and one data cycle.

This register indicates whether a given block (addressed in the Block protection read address command field: BA[11:0]) is locked-down, locked or unlocked using the VBP or PBP protection methods.

Address Cycle Mapping for Block Protection Read Command (7Ah)

	Bus Cycle	IO[7]	IO[6]	IO[5]	IO[4]	IO[3]	IO[2]	IO[1]	IO[0]
BlockAddress 1	1st	BA[1]	BA[0]	L	L	L	L	L	L
BlockAddress 2	2nd	BA[9]	BA[8]	BA[7]	BA[6]	BA[5]	BA[4]	BA[3]	BA[2]
BlockAddress 3	3rd	L		L	L	L	BA[12]	BA[11]	BA[10]
BA[0] controls plane selection.									

Figure 11. Waveforms for Block Protection Status Read Operation



11.1.6 Block Lock Status Register

This register indicates whether a given block (addressed in the Block protection read address command field is locked-down, locked or unlocked using the VBP or PBP protection methods. Table 13 provides the BLS Register definition.

Table 13. Block Lock Status Register

Bits	Function	Field Name	Default State	Description
7	Reserved	Reserved	0	
6	Reserved	Reserved	0	
5	Reserved	Reserved	0	
4	PBP Lock Down Status	PBP lock down Status	0	0: The PBP block range is not locked down by PBP 1: The PBP block range is locked down by PBP
3	Permanent Block Protection Status	Permanent Block Protect	1	0: The address selected block is locked by PBP 1: The address selected block is not locked by PBP
2		VBP Block-unlock	1	0: The address selected block is locked by VBP 1: The address selected block is not locked by VBP
1	Volatile Block Protection Status	VBP Not Locked-down	1	0: The VBP block range is locked down 1: The VBP block range is not locked down
0		VBP Lock-down	0	0: The VBP block range is not locked down 1: The VBP block range is locked down

12 Electrical Characteristics

12.1 Valid Blocks

Table 14. Valid Blocks

Device	Symbol	Min	Typ	Max	Unit
MKPV8G08CT-KS	N_{VB}	8032	–	8192	Blocks

12.2 Absolute Maximum Ratings

Table 15. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Ambient Operating Temperature (Industrial Temperature Range)	T_A	–40 to +85	
Temperature under Bias	T_{BIAS}	–50 to +125	
Storage Temperature	T_{STG}	–65 to +150	
Input or Output Voltage	V_{IO}[10]	–0.6 to +4.6	V
Supply Voltage	V_{CC}	–0.6 to +4.6	

Notes

Except for the rating "Operating Temperature Range", stresses above those listed in the Section 15. Absolute Maximum Ratings on page 19 may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Minimum Voltage may undershoot to -2V during transition and for less than 20 ns during transitions. Maximum Voltage may overshoot to VCC +2.0V during transition and for less than 20 ns during transitions.

12.3 Recommended Operating Conditions

Table 16. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Vcc Supply Voltage	Vcc	2.7	3.3	3.6	V
Ground Supply Voltage	Vss	0	0	0	

12.4 AC Test Conditions

Table 17. AC Test Conditions

Parameter	Value
Input Pulse Levels	0.0V to VCC
Input Rise and Fall Times	5 ns
Input and Output Timing Levels	VCC / 2
Output Load (2.7V - 3.6V)	1 TTL Gate and CL = 50 pF

12.5 DC Characteristics

Table 18. DC Characteristics and Operating Conditions

(Values listed are for each 4 Gb NAND, 8 Gb (4 Gb x 4) will differ accordingly)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
Power On Current		I_{CC0}	FFh command input after power on	–	–	50 per device	mA
Operating Current	Sequential Read	I_{CC1}	tRC = tRC (min) CE# = VIL, Iout = 0 mA	–	25	35	
	Program	I_{CC2}	Normal	–	25	35	
	Erase	I_{CC3}	–	–	15	30	
Standby Current, (TTL)		I_{CC4}	CE# = VIH, WP# = 0V/Vcc	–	–	1	
Standby Current, (CMOS)		I_{CC5}	CE# = VCC-0.2, WP# = 0/VCC VPE = 0/VCC	–	20	100	µA
Input Leakage Current		I_{LI}	VIN = 0 to VCC(max)	–	–	±10	
Output Leakage Current		I_{LO}	VOUT = 0 to VCC(max)	–	–	±10	
Input High Voltage		V_{IH}	—	VCC × 0.8	–	VCC + 0.3	V
Input Low Voltage		V_{IL}	—	–0.3	–	VCC × 0.2	
Output High Voltage		V_{OH}	IOH = –400 µA	2.4	–	–	
Output Low Voltage		V_{OL}	IOL = 2.1 mA	–	–	0.4	
Output Low Current (R/B#)		$I_{OL(R/B\#)}$	VOL = 0.4V	8	10	–	mA
Erase and Program Lockout Voltage		V_{LKO}	–	–	1.8	–	V

Notes:

All V_{CC} pins, and V_{SS} pins respectively, are shorted together.
Values listed in this table refer to the complete voltage range for V_{CC} and to a single device in case of device stacking.
All current measurements are performed with a 0.1 µF capacitor connected between the V_{CC} Supply Voltage pin and the V_{SS} Ground pin.
Standby current measurement can be performed after the device has completed the initialization process at power up.

12.6 Pin Capacitance

Table 19. Pin Capacitance (TA = 25°C, f = 1.0 MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input	C_{IN}	V_{IN} = 0V	–	10	pF
Input / Output	C_{IO}	V_{IL} = 0V	–	10	

Note：

For the stacked devices version the Input is 10 pF x [number of stacked chips] and the Input/Output is 10 pF x [number of stacked chips].